

Design of Variable Gain Amplifier in CMOS Technology

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SUMMARY

The variable gain amplifier (VGA), as one of the critical components in modern wireless transceiver designs, is widely used to provide a fixed output power for different input signals to improve the transceiver's dynamic range. Based on the targeted frequency, VGA is categorized as general purpose VGA for narrow bandwidth applications, and high-frequency VGA for applications with stringent bandwidth requirement. The challenges in VGA design is mainly the realization of accurate dB-linear characteristic with minimum power consumption and die area, as well as achieving the required bandwidth for the targeted application.

In this thesis, a new design approach which is the "cell-based" design method is proposed. The advantage of cell-based VGA design is that the number of unit cells to be cascaded can be chosen according to the system requirements. Moreover, a reconfigurable approach, by means of a digital control, can be implemented based on the unit cell to realize re-configurability and power scalability. As a result, multiple application standards can be satisfied with options for wide gain variation range, small gain error or low power consumption.

There are mainly two types of cells designed for the proposed cell-based design method. One is the gate-tuned VGA cell and the other one is the body-tuned VGA cell. Both of the cells achieved accurate dB-linear characteristic with minimum power consumption. The gate-tuned VGA cell is also combined with gate peaking technique for bandwidth extension, such that it is suitable in high-frequency VGA design.

Based on the proposed cells, three VGAs are designed, which are a gate-tuned general purpose VGA, a body-tuned general purpose VGA and a gate-tuned high-frequency VGA

with gate peaking technique. Measurement results show that the proposed cell-based design method is not only feasible, but also achieved very good performance in terms of accuracy, bandwidth, power consumption and die area. The body-tuned reconfigurable VGA can also work as a tunable PGA with variable gain step, which demonstrated the re-configurability, power scalability and versatility of the proposed cell-based design method.

Chapter 1

Introduction

1.1 Motivation

The variable gain amplifier (VGA) is widely used to provide a fixed output power for different input signals to improve the transceiver's dynamic range [1]. It is one of the critical components in modern wireless transceiver designs [1-9]. The location of the VGA in a RF system is circled by dashed line as shown in Figure 1-1. The VGA can be placed either before or after the low-pass filter (LPF), based on actual requirement of amplification first or filtering first.

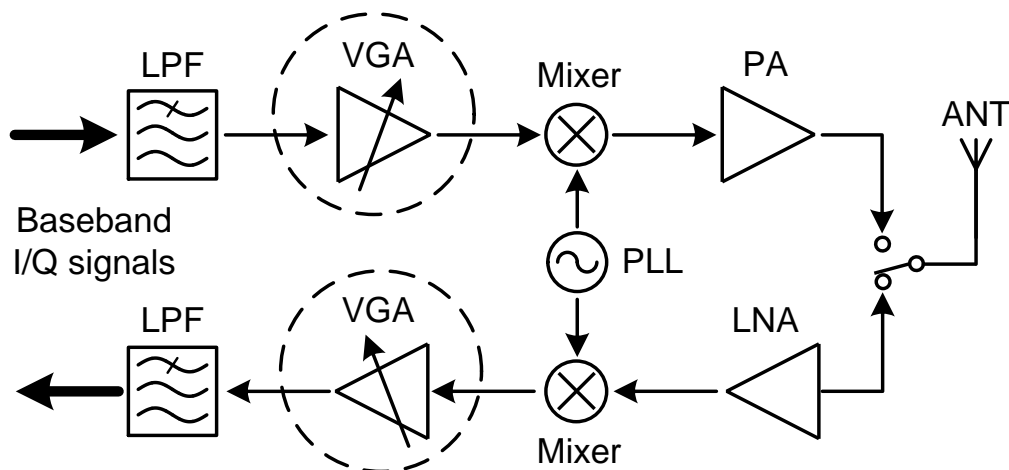


Figure 1-1 A simple RF system showing the location of VGA

Based on the different gain switching/tuning mechanisms, variable gain amplifiers can be categorized as analog controlled VGA and digital controlled programmable gain amplifier (PGA). VGAs are tuned continuously by analog control signals, whereas PGAs are tuned discretely by digital control signals. Although the design specifications of a VGA/PGA can vary significantly in terms of bandwidth, power consumption, noise and linearity for different applications, a common specification of the VGA/PGA is to accurately realize the dB-linear characteristic.

In order to achieve the dB-linear characteristic, PGAs utilizing feedback resistor arrays as well as switches are adopted for wireless communication receiver designs [2, 3, 10, 11]. However, there are several drawbacks for those designs. First of all, numerous resistors and switches must be used when a small gain step is required. As a result, it occupies a large die area. Secondly, the bandwidth using PGAs is usually not wide due to the nature of the closed loop structure. Finally, the gain control of PGAs is implemented at the digital baseband rather than at the analog front-end, which may have latency issue depending on the targeted application. Therefore, extensive research has been done on the design of accurate dB-linear VGAs [4-9, 12-26].

In order to achieve accurate dB-linear characteristic, the implementation of an exponential function is required. Although it is natural to design an accurate dB-linear VGA in bipolar technology due to its intrinsic exponential characteristic [11, 12], it is better implemented in a standard CMOS technology so that the cost of integration can be low. In general, due to the linear and square-law characteristic of the MOSFET itself, only the first-order and second-order terms of the Taylor's series of the exponential function are realized. The omitted high order terms are the major sources for the gain error. When small gain error and good accuracy is required, additional circuits need to be added to approximate the high

order terms of the exponential function, leading to higher power consumption and smaller bandwidth.

During the last decade, the researches on millimeter-wave integrated circuit designs have attracted tremendous attention [1]. In particular, the usage of unlicensed 9 GHz band from 57 GHz to 66 GHz is emerging as a dominant force for short range and high data rate wireless communication [27]. To achieve the required dynamic range, both RF front-end and analog baseband need to have the gain tuning capability [27]. At the RF front-end, the digital controlled tuning scheme is preferred, because it is usual to only have coarse gain tuning, such as high gain and low gain modes [27]. Then, the fine gain tuning should be provided at the analog baseband by means of VGAs [27-30].

Due to the limited gain bandwidth product of the active device, the gain of single-stage wideband amplifier is usually limited. To enhance the gain, the single-stage amplifier can be used as a cell, so that several identical cells can be cascaded to achieve the required gain. Such cell-based design strategy has been widely used for wideband limiting amplifier design [31-33]. The advantage of adopting the cell-based design strategy into the wideband VGA design is that the gain of unit cell can be traded for bandwidth, which could significantly reduce the design challenge of the unit cell. Consequently, there will be more space for the implementation of accurate dB-linear characteristic.

In short, the motivation of VGA design is driven by the requirements for better dB-linear accuracy, wider bandwidth and lower power consumption. Other than that, smaller size, higher yield and better robustness are always the driving force in practice.

1.2 Thesis organization

In Chapter 1, the importance and the motivation of VGA design is presented. The overview of VGA design status and difficulty are briefly discussed, followed by an introduction to the contents of each chapter.

In Chapter 2, the VGA performance parameters and design considerations are firstly reviewed. Design considerations like the gain variation range, gain error, bandwidth, noise, linearity, power consumption and process variation are discussed in details. Other than that, the VGA is categorized as general purpose VGA and high-frequency VGA according to different targeted frequency. Finally, detailed literature review for state-of-the-art VGA designs in each category is presented.

In Chapter 3, the idea of cell-based design is proposed. The bandwidth of a cascaded system is firstly reviewed, followed by the definition of dB-linear. The importance of dB-linear and the principle on how dB-linear can be achieved are then discussed. Finally, the advantages, disadvantages and design challenges of this cell-based design method are discussed in details.

In Chapter 4, the proposed VGA cells based on the above mentioned cell-based design method is presented. The design procedure and considerations are discussed in details. Comprehensive analysis supported by mathematical equations and simulation results are provided to give a full description of the proposed VGA cells. Depending on how the control signal is applied, a gate-tuned VGA cell and a body-tuned VGA cell are proposed for general purpose VGA, while a high-frequency VGA cell is proposed for high-frequency VGA. Analysis and implementation of the gate peaking technique is discussed in details. This

technique is employed in order to extend the bandwidth, so that the gate-tuned VGA cells can be turned into high-frequency VGA cells.

In Chapter 5, the actual implementation and measurement results of the gate-tuned VGA are presented. The 5-cell gate-tuned general purpose VGA is implemented in 0.18 μm CMOS technology. Measurement results show that the general purpose VGA is accurate and wideband, with ultra-low power consumption and small area. Therefore, the presented gate-tuned VGA is suitable for many applications, where ultra-low power, high frequency and accurate dB-linear characteristic are required.

In Chapter 6, the actual implementation and measurement results of the body-tuned VGAs are presented. Single-cell, 5-cell, 10-cell body-tuned general purpose VGAs are implemented in 0.18 μm CMOS technology. AC-coupled 10-cell body-tuned VGA and 15-cell reconfigurable body-tuned VGA are also fabricated. Measurement results show that the body-tuned general purpose VGA achieved extremely accurate dB-linear characteristic across a wide tuning range, with low power consumption and wide bandwidth. Therefore, the presented body-tuned VGA design may be suitable for many applications, where high accuracy, low power and high frequency are required.

In Chapter 7, the actual implementation and measurement results of the 11-cell high-frequency VGA are presented. The high-frequency VGA is implemented in 65 nm CMOS technology. DC offset cancellation circuits and control generation circuits are also presented. Measurement results show that the VGA achieved accurate dB-linear characteristic with very wide bandwidth. Therefore, the presented high-frequency VGA design may be suitable for high frequency applications, like the 60 GHz communication system.

In Chapter 8, the conclusion for the whole work is drawn and possible future works are proposed.

Chapter 2

Review of VGA design

2.1 Parameters and challenges in VGA design

2.1.1 Gain variation range and gain error

An example plot of the gain characteristic vs. frequency with various V_{CTRL} is presented in Figure 2-1.

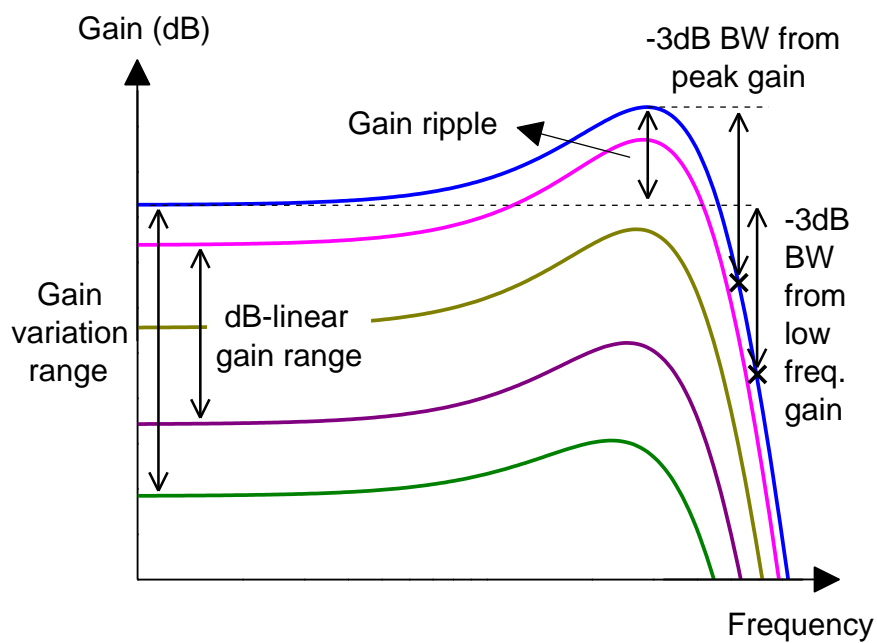


Figure 2-1 An example plot of the gain characteristic vs. frequency with various V_{CTRL}

As shown in Figure 2-1, the gain variation range is the difference between the highest gain and the lowest gain that a VGA can provide. The gain variation range should be large enough to cover the whole possible input signal range, and is best to be dB-linear. Large gain variation range or dB-linear gain range can be realized in a single stage, or by cascading multiple stages. Cascading multiple stages usually result in higher power consumption, larger die area and poorer linearity and noise performance. However, with properly designed VGA cell, these drawbacks are not obvious and the performance of the overall VGA is similar or better than other state-of-the-art ones [34-36].

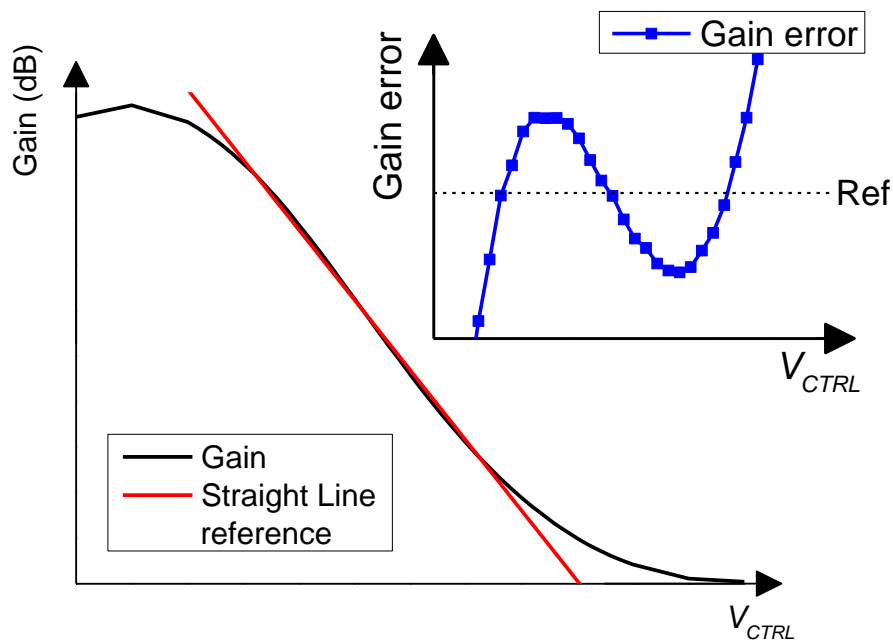


Figure 2-2 An example plot of gain and gain error vs. V_{CTRL} at one frequency point

An example plot of gain and gain error vs. V_{CTRL} at one frequency point is presented in Figure 2-2. The gain error is the deviation of the gain from an ideal straight line as shown in Figure 2-2. Smaller gain error and better accuracy are desired, and will alleviate the burden of

the automatic gain control (AGC), analog-to-digital, digital-to-analog converter design, as well as improve the performance of the overall system.

2.1.2 *Bandwidth*

The bandwidth is defined as the frequency where the gain is reduced by 3 dB w.r.t the flat gain. Thus its unit is Hz. This definition is trivial for monotone frequency response. However in some cases where the gain expands before it compresses, the bandwidth can be defined as -3 dB w.r.t the low frequency gain or the peak gain, as shown in Figure 2-1. In this thesis, the bandwidth calculated -3 dB from the low frequency gain is used. The difference between the peak gain and the low frequency gain is defined as gain ripple, and will be presented separately when it is significant. It is obvious that the gain ripple also affects the gain error. Thus when the gain ripple appears as a result of bandwidth extension, it must be controlled or compensated carefully.

VGAs can be categorized into two types based on the targeted operation frequency range. One type is general purpose VGA, whose bandwidth is normally much larger than required, for low bandwidth applications. The other type is high-frequency VGA, whose bandwidth is very large as they are designed for advanced communication scheme where bandwidth requirement is very stringent.

General purpose VGA

General purpose VGA refers to those VGAs whose bandwidth is in the range of tens or hundreds of MHz. Most of the wireless communication bandwidth falls in this range [37-42]. A summary of communication standard and the corresponding bandwidth is shown in Table 2-1. The bandwidth requirement is different for various applications. For general

purpose VGAs, the bandwidth is normally designed wide enough and a separate low pass filter will set the proper bandwidth for a specific application.

High-frequency VGA

High-frequency VGA refers to those VGAs whose bandwidth is beyond 1 GHz. In certain applications like the 60 GHz communication system, the bandwidth requirement becomes very stringent. Thus high-frequency VGA is required. The Institute of Electrical and Electronics Engineers (IEEE) 802.15.3c task group defines the standard that provides single carrier (SC) low complexity modulation scheme, such as binary phase-shift keying (BPSK) and quadrature phase-shift keying (QPSK), with a cyclic prefix [43]. When one of the four 2.16 GHz channels in the 57 ~ 66 GHz band is used, an un-coded bit rate of around 3 Gbit/s can be achieved by QPSK modulation. If the direct conversion architecture is applied to the receiver, a cut-off frequency of 880 MHz, as shown in Table 2-1, is required for the analog baseband, which is usually effectively controlled by the channel selection filter. On the other hand, for IEEE 802.11ad WiGig standard, the single carrier physical layer function (PHY) normally uses a bandwidth of 1760 MHz, while the orthogonal frequency-division multiplexing (OFDM) PHY uses 1830 MHz [44], as shown in Table 2-1. The bandwidth of the VGAs needs to be within the range of GHz, so that any additional poles of VGA will not affect the frequency response of the filter [27-30]. For the applications of short range and high data rate, 20 dB gain variation range is considered to be sufficient at the analog baseband [27-30].

Table 2-1 IEEE 802.11 network PHY standards

Protocol	Carrier Frequency (GHz)	Channel Bandwidth (MHz)
IEEE 802.11 [37]	2.4	22
IEEE 802.11a [38]	5/3.7	20
IEEE 802.11b [39]	2.4	22
IEEE 802.11g [40]	2.4	20
IEEE 802.11n [41]	2.4/5	20/40
IEEE 802.11ac [42]	5	20/40/80/160
IEEE 802.15.3c [43]	60	2160 (880)
IEEE 802.11ad [44]	60	2160 (1760/1830)

*Number in bracket is the actual bandwidth of data.

2.1.3 Noise and linearity

At low frequency, the circuit is usually not matched and the input referred noise (IRN) is normally measured. However for high frequency, the parasitic capacitance is providing a low impedance path to ground and the circuit must match to the measurement equipment. Thus noise figure (NF), which is calculated from the noise factor F , is more popular in high-frequency VGA measurement. The unit for IRN is $\text{nV}/\sqrt{\text{Hz}}$, and the unit for NF is dB. The IRN, noise factor and NF are expressed as:

$$\text{IRN} = \frac{V_{n,out}}{A} \text{ nV}/\sqrt{\text{Hz}}, \quad (2-1)$$

$$F = \frac{V_{n,out}^2}{A^2} \frac{1}{4kTR_S}, \quad (2-2)$$

$$NF = 10 \log F \text{ dB}, \quad (2-3)$$

where A is the gain of the amplifier. If the source resistance is matched to 50Ω , then an IRN of $1 \text{ nV}/\sqrt{\text{Hz}}$ is equivalent to 0.82 dB of NF, and any doubling or 10 times of IRN will result in 3 dB or 10 dB increase in NF, respectively.

The linearity is expressed by either the third-order interception point (IP_3) or the 1 dB compression point (P_{1dB}), both of the unit of dBm . The relationship between IP_3 and P_{1dB} , either both taken at the input or both taken at the output, for a typical amplifier can be approximated as:

$$IP_3 - P_{1dB} \approx 9.6 \text{ dBm}. \quad (2-4)$$

The resultant noise factor F_{tot} and input third-order interception point $IIP_{3,tot}$ for a cascaded system can be written as [45]:

$$F_{tot} = F_1 + \frac{F_2 - 1}{A_1} + \frac{F_3 - 1}{A_1 \cdot A_2} \cdots + \frac{F_m - 1}{A_1 \cdots A_{(m-1)}}, \quad (2-5)$$

$$\frac{1}{IIP_{3,tot}} = \frac{1}{IIP_{3,1}} + \frac{A_1}{IIP_{3,2}} + \frac{A_1 \cdot A_2}{IIP_{3,3}} \cdots + \frac{A_1 \cdots A_{(m-1)}}{IIP_{3,m}}, \quad (2-6)$$

where F_n is the noise factor of the n th component, and $IIP_{3,n}$ is the input third-order interception point of the n th component.

The noise and linearity performance of a VGA is crucial. Noise is mostly related to the sensitivity of the VGA, which determines the smallest signal that a VGA can amplify. Linearity is mostly related to the compression or saturation due to circuit nonlinearity, which in contrast determines the largest signal that a VGA can amplify. Obviously that low noise and high linearity are desirable, however, from (2-5) and (2-6) it can be seen that there always exhibits a trade-off between noise and linearity. A high gain stage can be either placed at front to suppress the noise, or at the back to alleviate the linearity requirement of the preceding stages.

2.1.4 Power and supply voltage

Either current or power will be reported for a certain VGA, and they are easily converted to each other with the given supply voltage. The current/power consumption is commonly reported with the output buffer de-embedded. In actual case where the VGA is implemented in a whole system and the load impedance of the VGA is high, the output buffer is unnecessary and excluding it gives a more precise description of the VGA core itself.

The power consumption of a VGA is crucial especially for low power applications. The power consumption has to be small to extend the battery life as well as to generate less heat. The challenge of ultra-low power VGA design is mainly the noise and linearity degradation, which then significantly deteriorates the overall performance of the VGA.

2.1.5 Process variation and temperature

Monte Carlo simulation is commonly used for the performance under various process conditions, and corner simulation is used for the extreme case. If a VGA operates well across all corners, then the final yield is close to 100%. Performance variation across various

temperatures is also desirable to be as small as possible, such that the VGA is able to operate under various conditions and the robustness is improved. The VGA design is best to be process variation insensitive as well as temperature insensitive to improve the yield and reliability, which in turn reduces the cost of mass production. Thus it is very crucial in practical situations.

2.2 Review of state-of-the-art VGAs

The design methodology and considerations for general purpose VGA and high-frequency VGA are quite different. Thus the literature review is done separately to address the key design considerations for each type.

2.2.1 *General purpose VGA*

Designing a general purpose VGA to meet all the requirements of accurate dB-linear gain characteristic, large gain variation range, low power, low noise, wide bandwidth and high linearity is in all likelihood impossible. Several design trade-offs must be taken into account to meet different system specifications. In this Section, some of the classical design techniques from previously presented CMOS dB-linear VGAs are discussed.

In general, the design of a CMOS based analog VGA with accurate dB-linear gain characteristic is realized by the circuit implementations of pseudo-exponential or Taylor's series approximation functions [19-24]. A typical approximation is shown below:

$$e^{2x} \approx \frac{1+x}{1-x}. \quad (2-7)$$

Based on the approximation in (2-7), less than 15 dB of dB-linear gain range with a gain error of less than 0.5 dB [19] can be achieved for a single cell.

Although the gain variation range of the VGA can be extended by cascading several stages of the VGA cell, the gain error of such a VGA will be deteriorated significantly. To increase the gain variation range of the VGA, there are several variations of a pseudo-exponential model for approximating the exponential gain control mechanism as presented in [4-6, 13-18], a typical one is given below [4]:

$$e^{2x} \approx \frac{k + (1 + ax)^2}{k + (1 - ax)^2} \quad (2-8)$$

where k is a constant. The simplified schematic for the implementation of this approximation is illustrated in Figure 2-3.

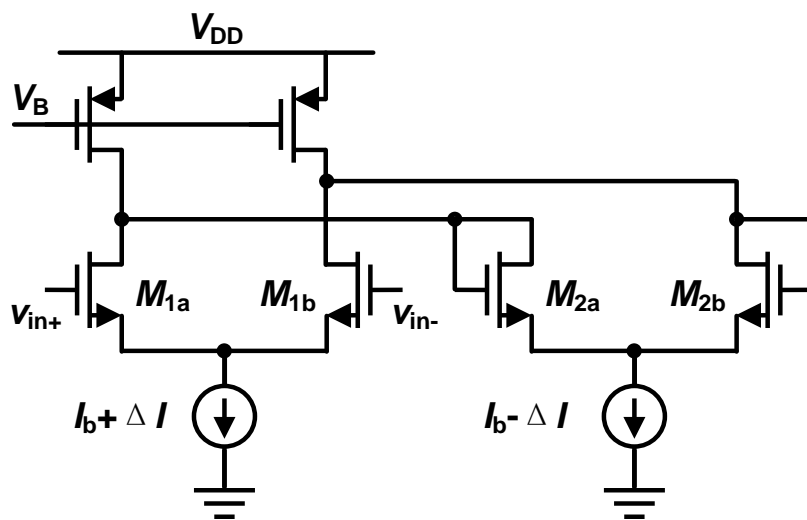


Figure 2-3 Schematic of a typical VGA with exponential approximation

The numerator and denominator of (2-8) are quadratic functions of the variable x . For k less than unity, the dB-linear range of (2-8) extends drastically and reaches its maximum

value at around $k = 0.12$ [4]. As can be seen from Figure 2-3, the resultant gain is given by the transconductance ratio between the input transistor and the diode-connected load, which can be controlled by varying the currents of the transconductance stages. As a result, respectable dB-linear gain range was achieved [4]. However, the bandwidth of the VGA is limited at high gain settings [4], due to the fact that the output impedance of this structure is dominated by the transconductance of the diode-connected transistors. Moreover, two current sources are required for both the input and load stages. Thus, the power consumption is relatively higher than the one sharing the current between the input and load stages.

A current steering VGA with an exponential control voltage circuit is another popular VGA technique [8, 21, 23], which also provides a large gain variation range. This technique is illustrated in Figure 2-4. Due to the square-law characteristic of a MOS device, an exponential control generator is required. Moreover, any noise on the control voltage will be coupled to the output node.

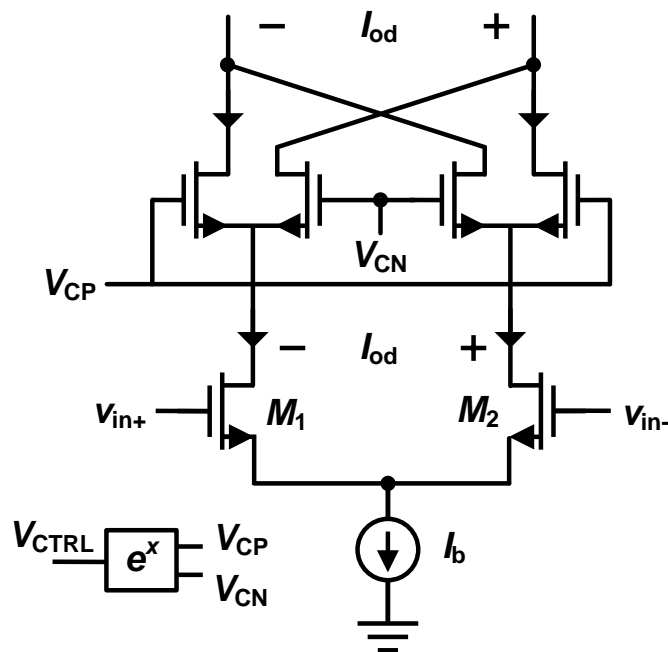


Figure 2-4 Schematic of current steering VGA with exponential control generator

Recently, a novel pseudo-exponential approximation is proposed in [6]. By cascading several linear functions, a high order pseudo-exponential approximation can be realized, as shown below:

$$e^x \approx \left(1 + \frac{x}{n}\right)^n, \quad (2-9)$$

where n is the number of cascaded linear terms. The simplified schematic is shown in Figure 2-5.

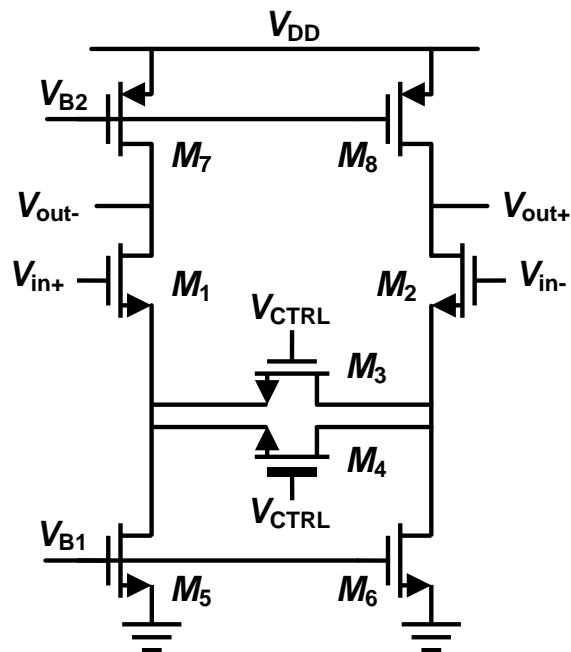


Figure 2-5 Schematic of a VGA with novel pseudo-exponential approximation

In [6], three stages are cascaded to achieve a gain variation range of 50 dB with a gain error of less than 0.5 dB. Although the implementation of a linear function in CMOS can be realized by biasing the transistor in triode region, the bandwidth of this structure is relatively small. It is mainly due to the fact that the gain variation range of the VGA is controlled by the slope of the linear function. In order to have a reasonable gain variation range, a large

transistor needs to be used at the input. Consequently, the bandwidth of the presented VGA is limited by the parasitic capacitance. Another drawback of this structure is that devices with different threshold voltages may be required to assist in the implementation of the linear function, which may not be available for standard CMOS technology.

In contrast to the topologies discussed above, a closed loop topology can be used. A VGA based on a differential ramp generator is presented in [7], and the simplified schematic is shown in Figure 2-6.

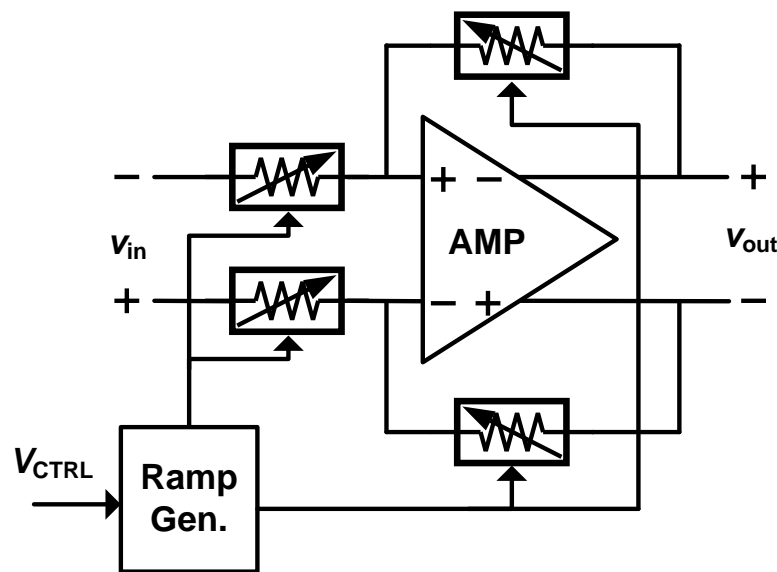


Figure 2-6 Schematic of a VGA with differential ramp generator

Utilizing a differential ramp generator, the feedback resistance can be gradually changed so that continuous gain tuning is achieved without implementing any pseudo-exponential function. By adopting a high gain amplifier, the linearity degradation caused by the large signal swing at the inputs of the VGA is reduced, which helps to improve the linearity of the VGA. However, the bandwidth of the VGA may be limited due to the closed loop topology. In addition, a large number of ramps are required to achieve continuous gain tuning with minimum error, which increases the area and layout complexity.

2.2.2 High-frequency VGA

Among the recent published high-frequency VGAs with accurate dB-linear characteristic, the digital controlled VGAs are dominant [27-30, 46], only a few works are reported based on the analog controlled ones [47, 48]. In [48], an AGC in a 0.13 μm SiGe BiCMOS is presented. By taking advantage of heterojunction bipolar transistor (HBT) devices, the designed amplifier can operate up to 5 Gb/s. The dB-linear characteristic is realized by the bipolar junction transistor (BJT) device in this technology as shown in Figure 2-7. The BJT itself is intrinsically exponential and thus dB-linear. Although the performance of this design is good, the SiGe BiCMOS process is not aiming for low power and low cost applications. For low power applications, it is still preferred to design the system in CMOS process.

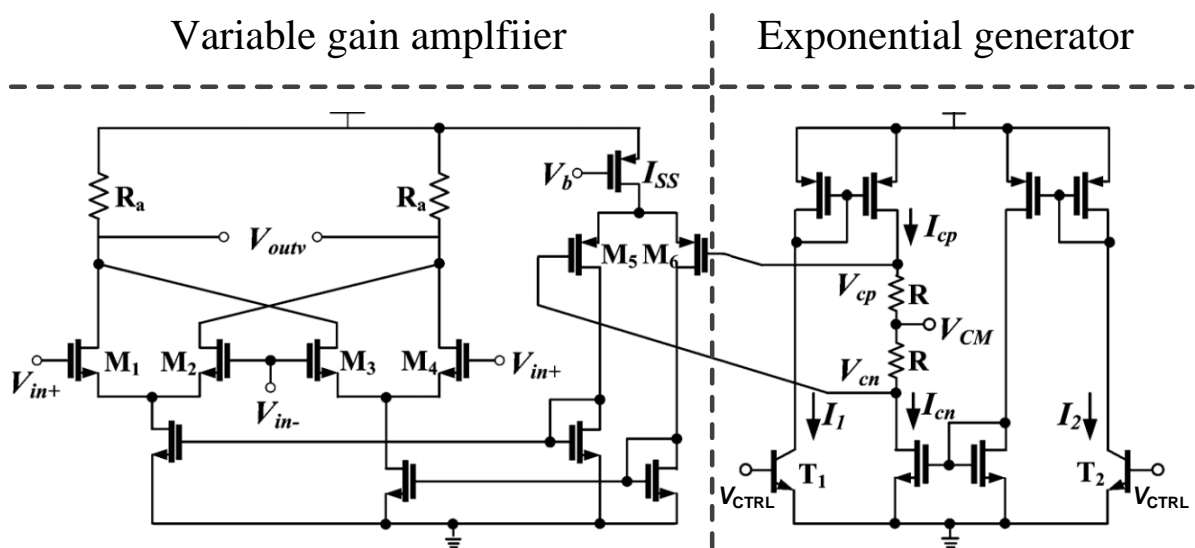


Figure 2-7 Schematic of a 5 Gb/s AGC in a 0.13 μm SiGe BiCMOS

One of the design challenges for wideband amplifier is that the operation frequency of the amplifier is limited by the parasitic capacitance associated at the output. The pros and cons of different wideband amplifier topologies have been well analyzed in the literature [31-

33, 49]. Although these wideband amplifiers cannot meet all the requirements to be used as a solution of 60 GHz application, the analysis of their characteristic gives a direction when designing a wideband VGA for 60 GHz application. To extend the bandwidth of the amplifier, on-chip inductors are often used [31], as shown in Figure 2-8. As a result, such amplifier occupies large die area.

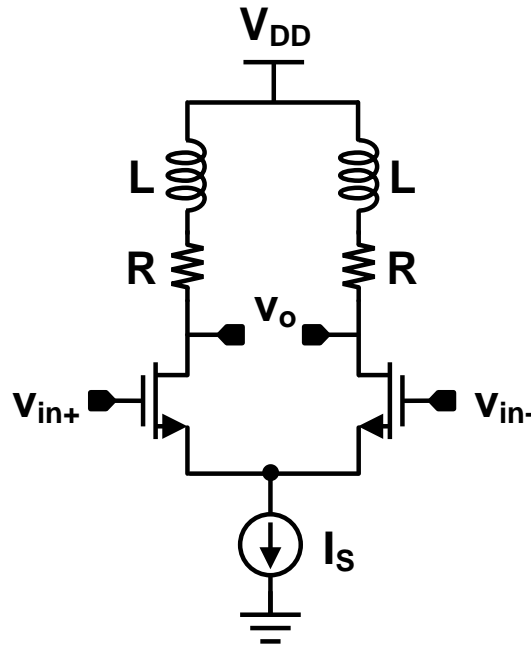


Figure 2-8 Schematic of a VGA with on-chip inductors for bandwidth extension

To reduce the required die area, active inductor can be utilized to replace the on-chip inductors [32], as shown in Figure 2-9. However, the drawback of such structure is that the active inductors introduce additional parasitic capacitances to the output, which could significantly limit the operation frequency.

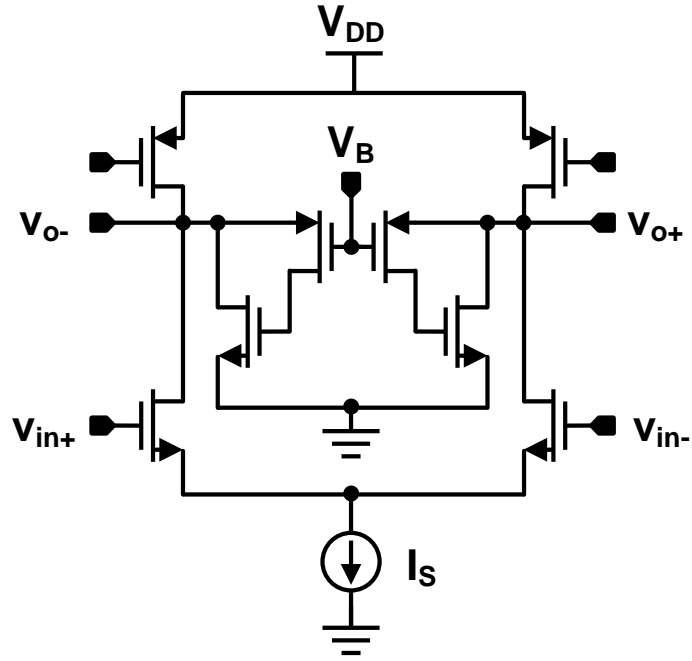


Figure 2-9 Schematic of a VGA with on-chip inductor replaced by active inductor

Another approach that can be used to extend the bandwidth of the amplifier is the “gate peaking”, as shown in Figure 2-10 [33].

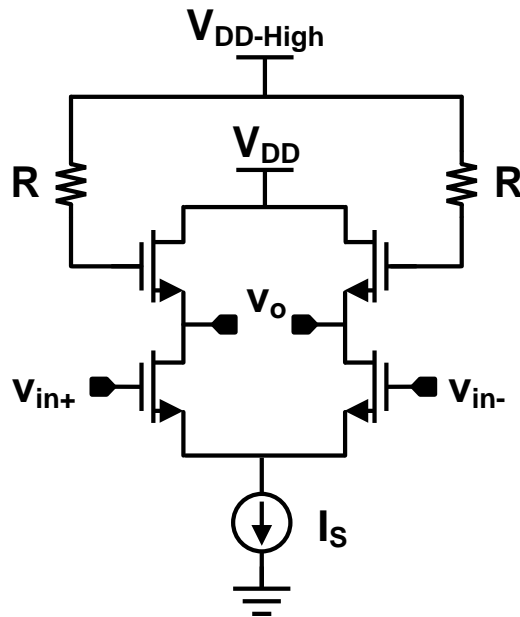


Figure 2-10 Schematic of a VGA with gate peaking for bandwidth extension

However, it requires a high supply voltage to maintain reasonable voltage headroom. Moreover, such approach may not be appropriate for the VGA design, due to the fact that the bandwidth of such amplifier strongly depends on the transconductance value of transistors as well as the value of “gate peaking” resistors. Consequently, it may lead a large bandwidth variation while the gain is varied, which is very undesirable.

In [49], a classical approach, “Cherry-Hooper”, is proposed, as shown in Figure 2-11. This approach and its variation are properly the most popular approaches that have been used for wideband VGA designs, as shown in Figure 2-12 [47].

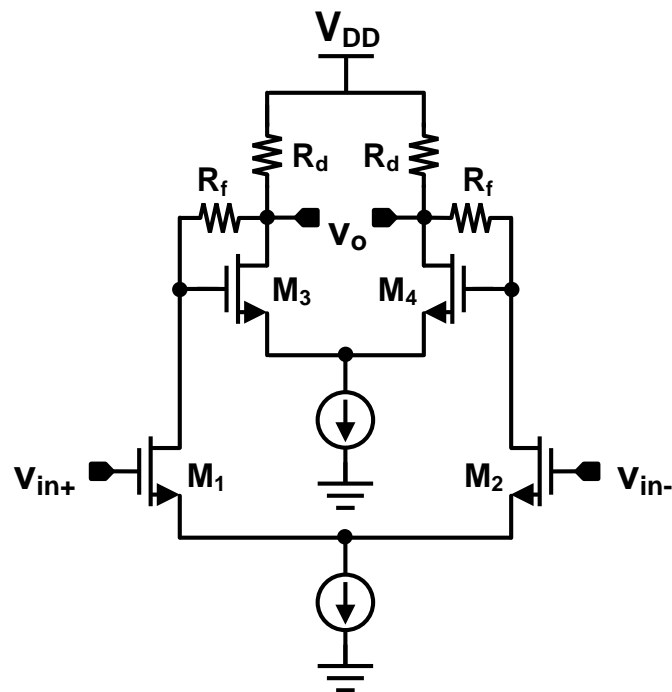


Figure 2-11 Schematic of a VGA with Cherry-Hooper approach

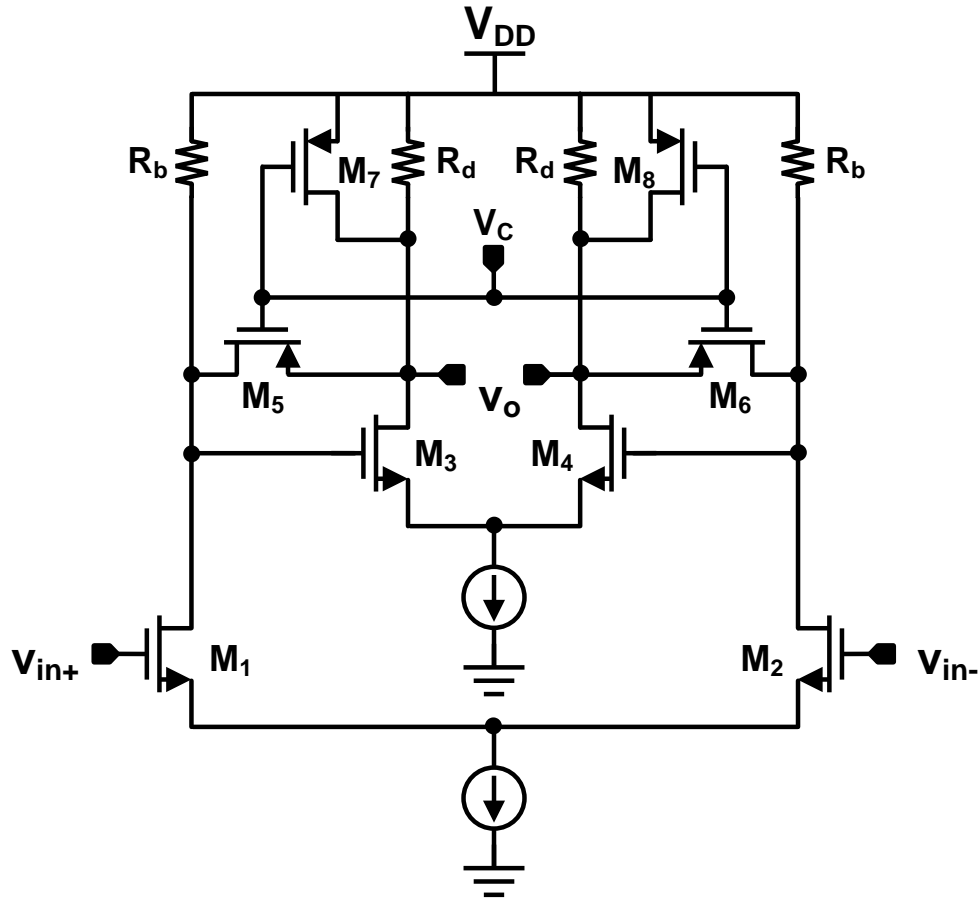


Figure 2-12 Schematic of a VGA with varied Cherry-Hooper approach

This is mainly due to the fact that the Cherry-Hooper amplifier approach could enlarge the bandwidth without the penalty of losing significant gain, comparing to the conventional feedback approach [29]. However, it is difficult to adopt this approach to the low voltage application, unless the low threshold voltage device is applied [47]. Moreover, it is also difficult to adopt this approach to the analog controlled VGA design, because there is no exponential relationship between the voltage gain and control voltage [47].

Detailed performance summary of the state-of-the-art VGAs will be provided with quantitative comparison to the respective proposed VGA in Section 5.4, Section 6.4 and Section 7.6.

Chapter 3

Cell-based design method

3.1 Idea of cell-based design

Conventionally, a VGA is realized in a single stage, or by cascading only two or three stages. Cascading too many stages has several difficulties, such as high power consumption, large die area and limited bandwidth. In particular, the gain error requirement for a single-stage amplifier is very crucial, because the overall gain error of a VGA will be accumulated when many stages are cascaded. Thus, the conventional designs are primarily focused on how to increase the dB-linear gain range of a single-stage VGA so that the number of single-stage amplifiers cascaded can be minimized. In contrast, a novel design method is proposed in this Section. The simplified block diagram of the proposed VGA is shown in Figure 3-1.

Instead of focusing on how to increase the dB-linear gain range of a single-stage amplifier, our primary goal is focused on how to design a unit cell with minimized gain error, power consumption and die area, as well as maximized bandwidth. Consequently, several of such unit cells can be cascaded to provide the required dB-linear gain range without consuming too much power and area. In order to differentiate our proposed design method with the conventional cascaded designs, the proposed method is named as “cell-based” design method.

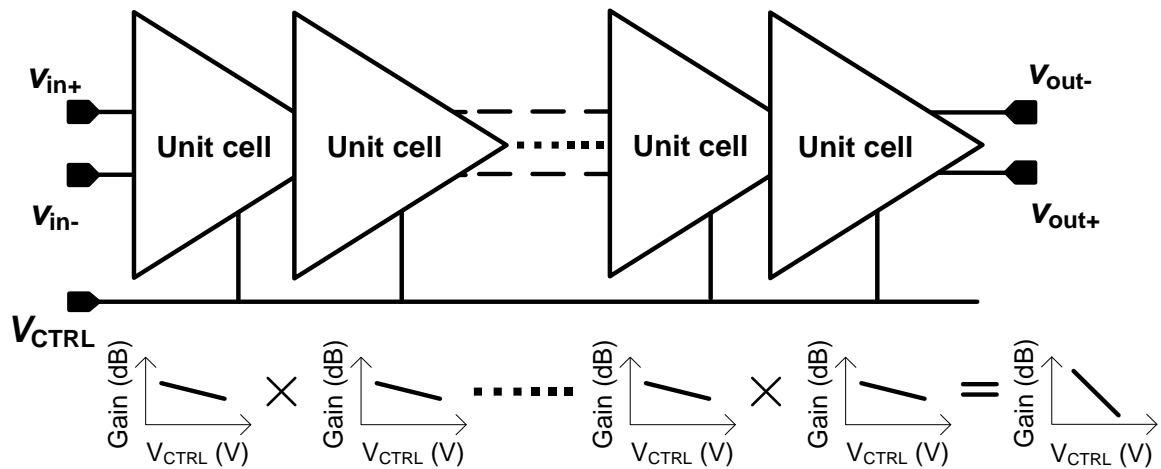


Figure 3-1 Simplified block diagram of the proposed VGA

The advantage of cell-based design method is that the number of unit cells to be cascaded can be chosen according to the system requirements. No additional circuitry, such as differential ramp or exponential generators is required. Moreover, a reconfigurable approach by means of a digital control can be implemented based on the unit cell to realize re-configurability and power scalability. As a result, multiple application standards can be satisfied with options for wide gain variation range, small gain error or low power consumption. Moreover, once the basic cell is carefully designed, the design effort for a new VGA with arbitrary number of cells will be minimal. The new VGA can be simply generated by selecting the suitable number of unit cells based on the requirements of the targeted application.

3.2 Bandwidth calculation

If each gain stage is identical and having a bandwidth of BW_c , the overall bandwidth BW_{tot} of the cascaded system is [31]:

$$BW_{tot} = BW_c \cdot \sqrt[m]{2^{1/n} - 1}, \quad (3-1)$$

where n is the number of stages cascaded, and m is equal to 2 for first-order stages and 4 for second-order stages. If the gain of each cell is defined as A_c , the achieved gain variation range of the overall cascaded system A_{tot} can be written as:

$$A_{tot} = A_c \cdot n. \quad (3-2)$$

For a total gain of A_{tot} , the required gain bandwidth product of each cell, GBW_c , can be written as:

$$GBW_c = \frac{GBW_{tot}}{A_{tot}^{(1-\frac{1}{n})} \cdot \sqrt[m]{2^{1/n} - 1}}. \quad (3-3)$$

where $GBW_c = A_{tot}^{1/n} BW_c$, and $GBW_{tot} = A_{tot} BW_{tot}$.

For a first-order system where $m = 2$, if $A_{tot} = 30$ dB and $BW_{tot} = 2$ GHz are targeted, the calculated A_c , BW_c and GBW_c requirements for each identical cell is shown in

Table 3-1.

Table 3-1 Calculated A_c and BW_c requirement for $A_{tot} = 30$ dB and $BW_{tot} = 2$ GHz

n	BW_c (GHz)	A_c (dB)	GBW_c (dBGHz)
1	2.00	30.00	33.01
2	3.11	15.00	19.92
3	3.92	10.00	15.94
4	4.60	7.50	14.13
5	5.19	6.00	13.15
6	5.72	5.00	12.57
7	6.20	4.29	12.21
8	6.65	3.75	11.98
9	7.07	3.33	11.83
10	7.47	3.00	11.73
11	7.84	2.73	11.67
12	8.20	2.50	11.64
13	8.55	2.31	11.63
14	8.88	2.14	11.63
15	9.20	2.00	11.64

3.3 Realization of dB-linear characteristic

The VGA is very important in modern wireless communication systems. This is due to the fact that the received signal power level is unpredictable and an AGC loop is needed. A VGA is usually used in a feedback loop to form the AGC circuit, and is to produce a known output voltage magnitude with various input signal levels [50]. In an AGC loop, an exponential gain control, or dB-linear characteristic, may be required to maintain the settling time independent of the input signal levels and to achieve a large gain variation range [51].

As discussed in Section 2.2, there are basically two types of dB-linear VGAs. One type is a VGA whose device is intrinsically dB-linear. In other words, the device itself exhibits exponential relationship. However, such exponential relationship is only available in BJT devices but not in CMOS. The other type is a linear VGA whose gain is controlled by an exponential voltage or current, which must be generated separately. In CMOS technology, there is no intrinsically exponential device, but square-law device only, and the realization of an ideal exponential function is also a difficult task. Thus many designs are based on pseudo-exponential expression, which uses an approximation of the ideal exponential function. Several approximation equations have been used and explored as summarized in Section 2.2.

However, in this design, the dB-linear characteristic is simply realized by a n-MOS transistor operating in the sub-threshold region, or by varying the body of a p-MOS transistor. Although these methods are well-known with certain disadvantages such as limited control voltage range, limited accuracy and large bandwidth variation due to the large change in transconductance, some better accuracy can still be achieved with the proposed cell-based method. This is due to the fact that any approximation, even a straight line, is an accurate exponential function for a very small range. Consequently, if many such cells are to be

cascaded and the gain variation range of each cell is small enough, the gain error introduced by any exponential approximation is very small, and the main gain error comes from the aggregation over all cells.

3.4 Versatility for cell-based design

3.4.1 Reconfigurable VGA perspective

As shown in Figure 3-1, the cell-based design method can provide other configurations by switching one or several cells on or off, such that the design becomes a reconfigurable VGA. Several advantages can be obtained from this re-configurability. Firstly, the overall gain variation range can be scaled, as well as the gain error which follows the change of gain variation range, resulting in a more accurate VGA. Secondly, the power consumption only depends on how many cells are on, and thus it is scalable and significant power can be saved for low gain mode. Finally, the bandwidth can be extended with fewer cells on, so that if the VGA can satisfy the bandwidth requirement for the highest gain setting, having fewer cells on will not cause any bandwidth problem.

3.4.2 Tunable PGA perspective

By considering the signals to switch cells on and off as digital control signal, the cell-based reconfigurable VGA can also be treated as a tunable PGA. An example of conventional PGA with coarse and fine gain tuning and the proposed tunable PGA is shown in Figure 3-2. As can be seen from Figure 3-2, instead of using fixed gain amplifiers for the coarse gain tuning, the proposed tunable PGA utilizes multiple cascaded unit cells in a binary-weighted manner.

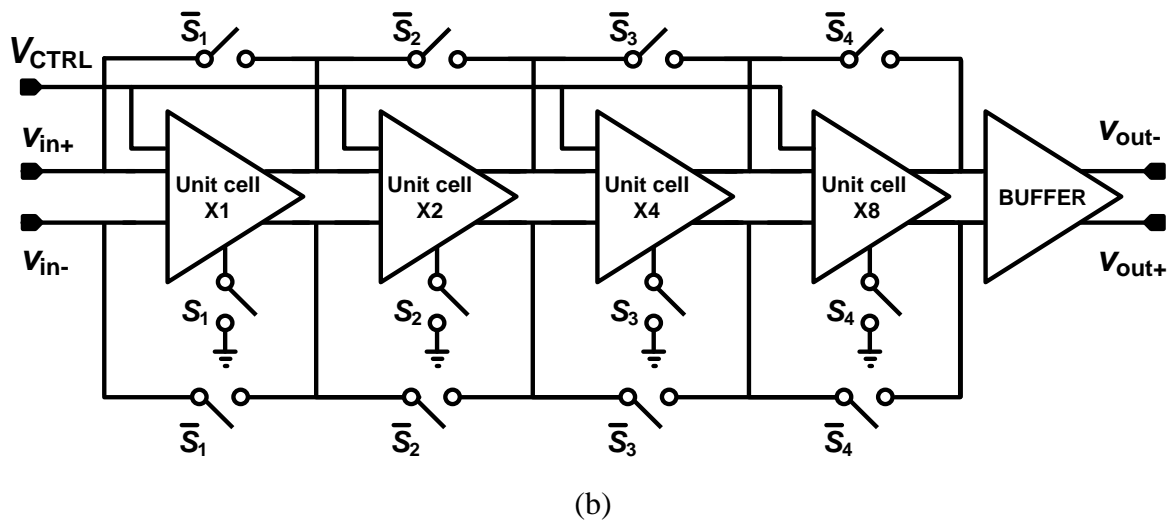
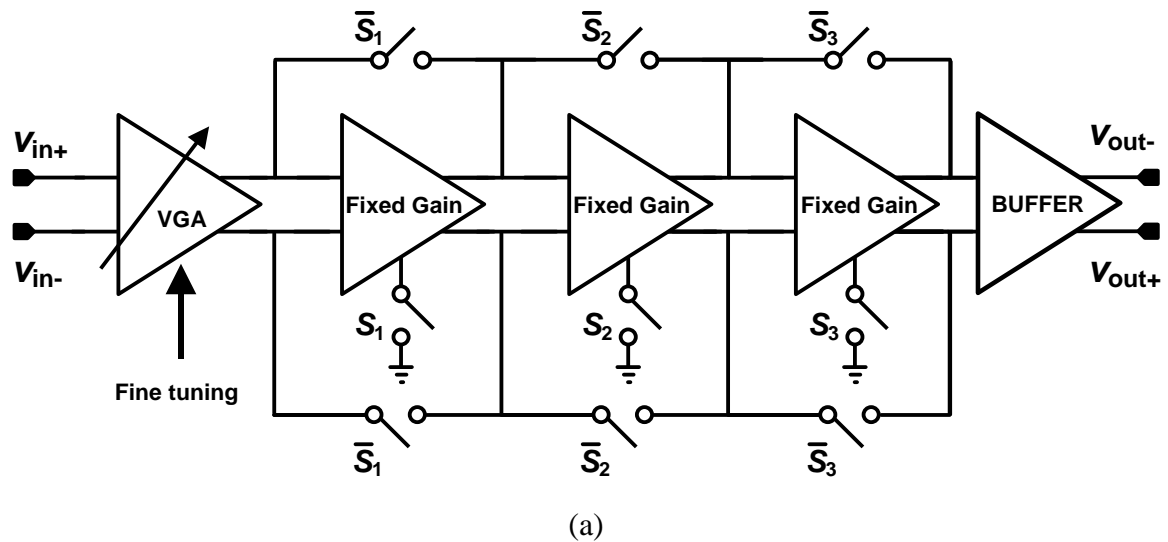


Figure 3-2 Block diagrams of (a) example of conventional PGA (b) proposed structure

The proposed configuration provides several advantages over the conventional designs. On one hand, the designed PGA is tunable, and the discrete gain steps are realized with the freedom of varying V_{CTRL} to change the step size and the overall gain variation range. On the other hand, the power efficiency of the proposed PGA is improved.

A power consumption comparison between the example of conventional PGA and the proposed one is presented in Figure 3-3. As illustrated in Figure 3-3, the power consumption of the proposed PGA is scaled to 1/16, while the power consumption of the conventional

PGA is only scaled to 1/4. In other words, the ratio of gain/power consumption of the proposed PGA is kept constant. As long as the gain is changed, the power consumption is also changed accordingly, so that there is no additional power wasted for low gain mode.

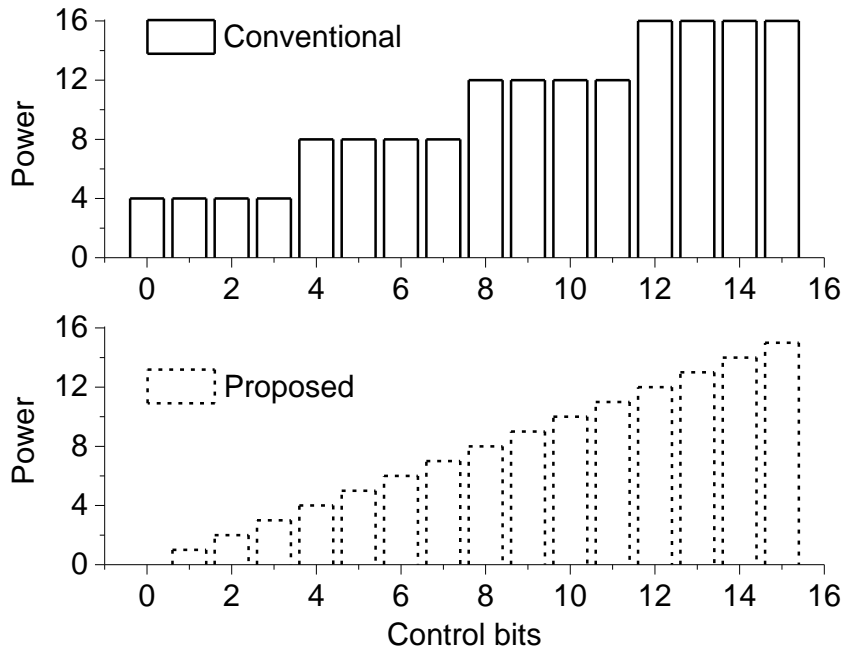


Figure 3-3 Histogram of power consumption for the example of conventional PGA and proposed structure against control bits

3.5 Challenges for cell-based design

The VGA must be designed with several stages to alleviate the gain bandwidth product requirement. As can be seen from Table 3-1, the required gain of each cell is relatively small, if multiple stages can be cascaded. This is a great advantage for the design of high gain and wideband amplifier in deep submicron process. Due to the short channel effect, it is difficult to achieve a high DC gain for an amplifier without any gain compensation technique [52].

To compensate the gain of the amplifier, neither adding negative resistance to the output nodes nor using stacked transistors would be ideal for the requirements of the low voltage, low power and wide bandwidth. To extend the bandwidth of the unit cell, simple structure is preferred. Another advantage of cascading more cells is that the bandwidth variation of each cell has limited impact on the overall bandwidth variation of the cascaded amplifier, which is extremely important for a wideband VGA design.

However, the design of such unit cell still faces some great challenges. In particular, extremely accurate dB-linear characteristic is required for accurate gain adjustment.

First of all, the gain error of each unit cell needs to be extremely small so that the accumulated gain error can be maintained within a reasonable range. For example, if the overall gain error of a 10-cell VGA needs to be less than 1 dB, then the gain error of the unit cell needs to be less than 0.1 dB.

Secondly, since very wide bandwidth for each cell is required when many cells are to be cascaded, as shown in Table 3-1, special techniques must be adopted to extend the bandwidth for the design of high-frequency VGA.

Thirdly, an exponential generator must be designed so that the accurate dB-linear characteristic can be achieved. However, such generator has additional parasitic capacitance, which could limit the bandwidth of the overall VGA as mentioned above [4, 6, 7, 12]. Thus, again, some novel techniques need to be adopted to balance the requirements of wide bandwidth and accurate dB-linear characteristic.

Fourthly, the power consumption as well as the die area of the unit cell needs to be minimized, as these parameters will also be multiplied directly by the number of stages. Thus, simple structure with minimum area and power consumption is preferred.

Finally, a reasonably large control voltage range is required, as a single voltage source will be used to control the overall gain of a VGA. If the control voltage range is small, although the performance of a unit cell will not be significantly affected, the overall gain of the VGA may be very sensitive to the control voltage variation.

Therefore, the VGA cell used in this cell-based design must be a simple but robust structure with minimum power consumption and die area, as well as maximum bandwidth. The cell must also be very accurately dB-linear. The design of such cells will be presented in details in Chapter 4.

Chapter 4

VGA cell design

4.1 Topology and analysis of the proposed VGA cell

The simplest basic cell consists of a differential pair and is shown in Figure 4-1.

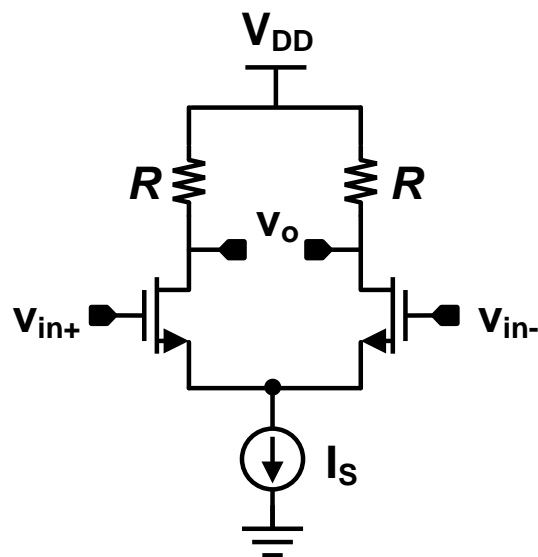


Figure 4-1 The simplest basic cell with a differential pair

This is the most conventional differential amplifier with a pair of n-MOS transistors as input and resistors as load. The gain of this differential amplifier is given by:

$$A_v = \frac{v_{out}}{v_{in}} = g_m R, \quad (4-1)$$

In order for the gain to be variable, the resistor R must be variable. Thus it is replaced by a diode-connected MOSFET, which acts like a variable resistor with better accuracy. The small signal impedance of such device is simply $1/g_m$. However, single MOSFET load with resistance $1/g_m$ cannot change the gain as g_m is only related to the drain current I_D , which is determined by the current source and is constant throughout the operation range. Thus, two of such transistor loads are placed in parallel to realize current steering, such that the overall load resistance is variable. The diagram is shown in Figure 4-2. In Figure 4-2, one diode-connected n-MOS transistor and one p-MOS diode-connected transistor are used for illustration purpose only. They can be of the same type.

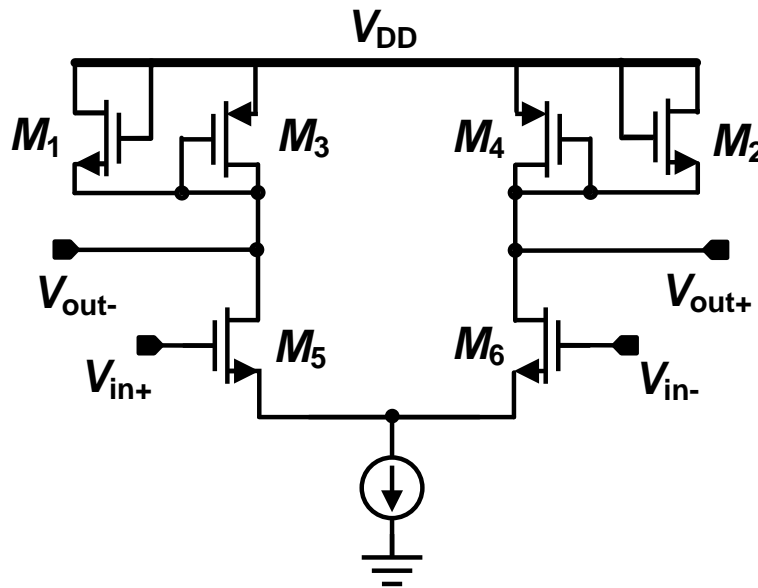


Figure 4-2 A differential pair with n-MOS and p-MOS active loads

The small signal equivalent circuit of the load seen by the output node, Z_{Load} , is shown in Figure 4-3. The gain expression is now expressed as:

$$A_v = \frac{v_{out}}{v_{in}} = \frac{g_{m,5,6}}{g_{m,1,2} + g_{m,3,4}}. \quad (4-2)$$

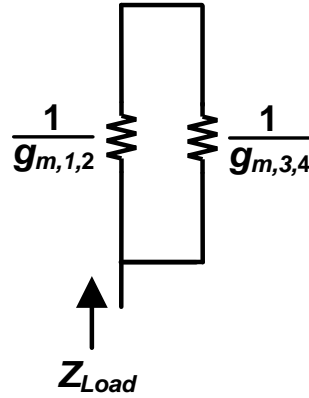


Figure 4-3 Small signal equivalent circuit of the load

This is the fundamental structure and expression of the designed VGA cell, and depending on how the control signal is implemented as well as how other techniques are applied, various VGAs suitable for multiple applications can be realized.

4.2 Control implementation

4.2.1 Gate-tuned VGA cell for general purpose VGA

In order for the gain to be tunable, the control signal must be applied to the circuit. One way to apply the control signal is at the gate of one of the load transistors. The schematic is shown in Figure 4-4. The reason for not applying complimentary control signal at both gates of the transistors is that one of the transistors must be used to set the DC conditions. The DC operating point should not drift in order to directly cascade multiple cells.

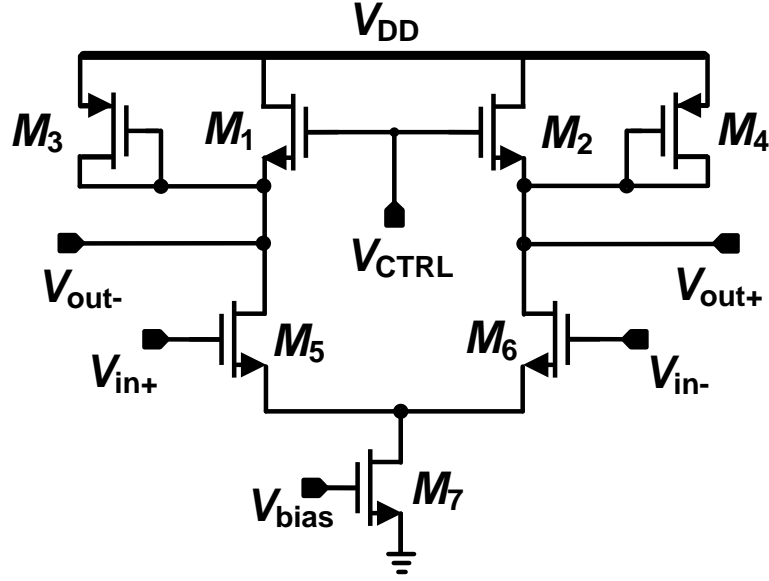


Figure 4-4 The proposed gate-tuned VGA cell

As shown in Figure 4-4, if the change in g_m can be represented by their respective Δg_m , (4-2) can be rewritten as:

$$A_v = \frac{g_{m,5,6}}{g_{m,1,2} + g_{m,3,4} + \Delta g_{m,1,2} + \Delta g_{m,3,4}}. \quad (4-3)$$

The bias condition of the input differential pair transistors M_5 and M_6 are fixed at all times, thus the current relationship between $I_{DS,5,6}$, $I_{DS,1,2}$ and $I_{DS,3,4}$ can be expressed as:

$$I_{DS,5,6} = I_{DS,1,2} + I_{DS,3,4}, \quad (4-4)$$

and thus:

$$\Delta I_{DS,1,2} = -\Delta I_{DS,3,4}. \quad (4-5)$$

As the n-MOS transistors M_1 and M_2 are biased in the sub-threshold region, the

transconductance $g_{m,1,2}$ can be expressed as:

$$g_{m,1,2} = \frac{2I_{DS,1,2}}{nV_T}. \quad (4-6)$$

Meanwhile, the p-MOS transistors M_3 and M_4 are biased in the saturation region, and $g_{m,3,4}$ can be expressed as:

$$g_{m,3,4} = \sqrt{2\mu_P C_{ox} \left(\frac{W}{L}\right)_{3,4}} \cdot \sqrt{I_{DS,3,4}}. \quad (4-7)$$

Differentiating $g_{m,1,2}$ w.r.t $I_{DS,1,2}$ and $g_{m,3,4}$ w.r.t $I_{DS,3,4}$ gives:

$$\Delta g_{m,1,2} = \frac{2}{nV_T} \Delta I_{DS,1,2}, \quad (4-8)$$

$$\Delta g_{m,3,4} = \frac{\mu_P C_{ox} \left(\frac{W}{L}\right)_{3,4}}{g_{m,3,4}} \Delta I_{DS,3,4}. \quad (4-9)$$

Substituting (4-4), (4-8) and (4-9) into (4-3) leads to

$$A_v = \frac{g_{m,5,6}}{g_{m,1,2} + g_{m,3,4} + \left(\frac{2}{nV_T} - \frac{\mu_P C_{ox} \left(\frac{W}{L}\right)_{3,4}}{g_{m,3,4}}\right) \Delta I_{DS,1,2}}. \quad (4-10)$$

As M_1 and M_2 are biased in the sub-threshold region, the current $I_{DS,1,2}$ can be expressed as:

$$I_{DS,1,2} = I_{O,1,2} \left(\frac{W}{L}\right)_{1,2} \exp\left(\frac{\kappa V_{G,1,2} - V_{S,1,2}}{nV_T}\right), \quad (4-11)$$

where $I_{O,1,2}$ is the sub-threshold base current, κ is the gate coupling coefficient which can be treated as 0.7 throughout the sub-threshold region. Differentiating $I_{DS,1,2}$ w.r.t $V_{G,1,2}$ gives the expression of $\Delta I_{DS,1,2}$ as:

$$\Delta I_{DS,1,2} = \frac{\kappa}{nV_T} I_{O,1,2} \left(\frac{W}{L}\right)_{1,2} e^{\left(\frac{\kappa V_{G,1,2} - V_{S,1,2}}{nV_T}\right)} \Delta V_{G,1,2}, \quad (4-12)$$

The control voltage V_{CTRL} is applied at $V_{G,1,2}$, which is the gate node of the n-MOS load transistors M_1 and M_2 . The overall gain A_v is close to an inverse exponential function for an appropriate V_{CTRL} range.

The simulated resistance at the output node is shown in Figure 4-5. The resistance is plotted in dB scale, and the resultant resistance is similar to the final gain curve, with a difference of a factor of $g_{m,5,6}$.

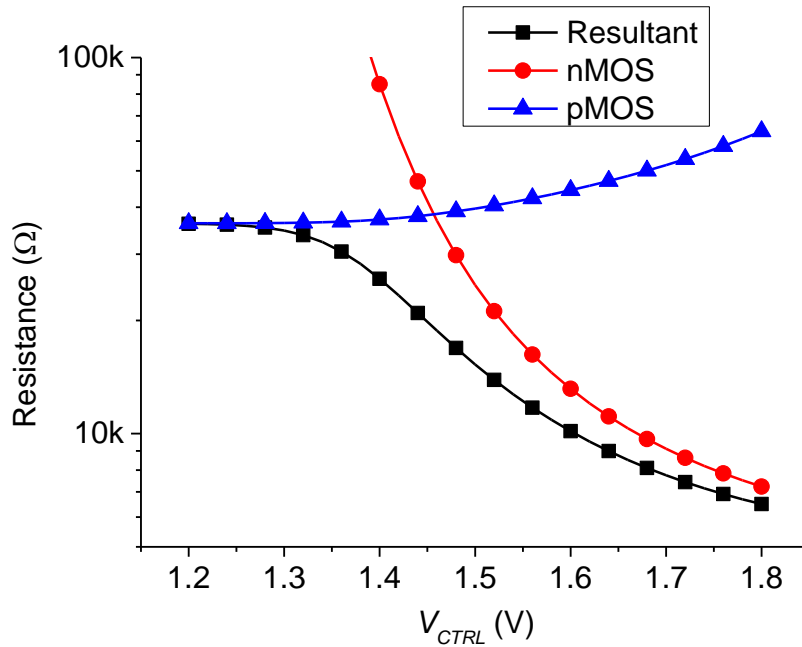


Figure 4-5 Simulated resistance at the output node for the gate-tuned VGA cell

According to (4-2) and (4-4), the design procedure of the unit cell can be summarized as follows:

- 1) According to the required power consumption, the sizes of the current source transistor M_7 can be chosen, and with M_5 and M_6 being large, the g_m is fixed.
- 2) The selection of the size of M_3 and M_4 can be made based on the required gain of the unit cell.
- 3) The size of M_1 and M_2 can be optimized accordingly.

As illustrated in Figure 4-6, the dB-linear gain range and gain error are dependent on the size of M_1 and M_2 .

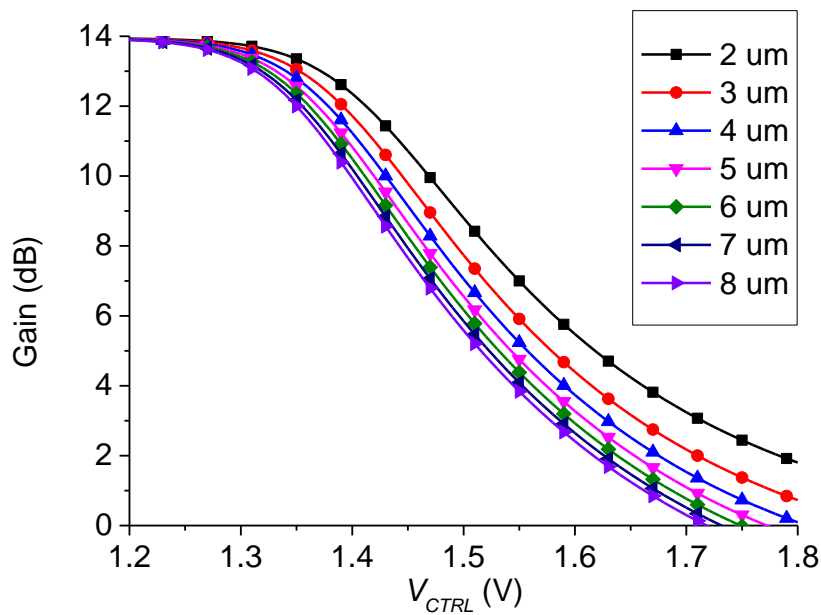


Figure 4-6 Simulated gain of the unit cell vs. width of M_1 and M_2

The final device size for the gate-tuned VGA cell is listed in Table 4-1.

Table 4-1 Device size list for gate-tuned VGA cell

Component	Width (um)	Length (um)
n-MOS M_1 and M_2	5	0.36
p-MOS M_3 and M_4	1	0.36
M_5 and M_6	4	0.36
M_7	3	0.36

4.2.2 Body-tuned VGA cell for general purpose VGA

The other way to apply the control signal is at the body node of the p-MOS transistor. The schematic is shown in Figure 4-7. The reason for not applying at body node of n-MOS transistor is to avoid the use of deep n-well.

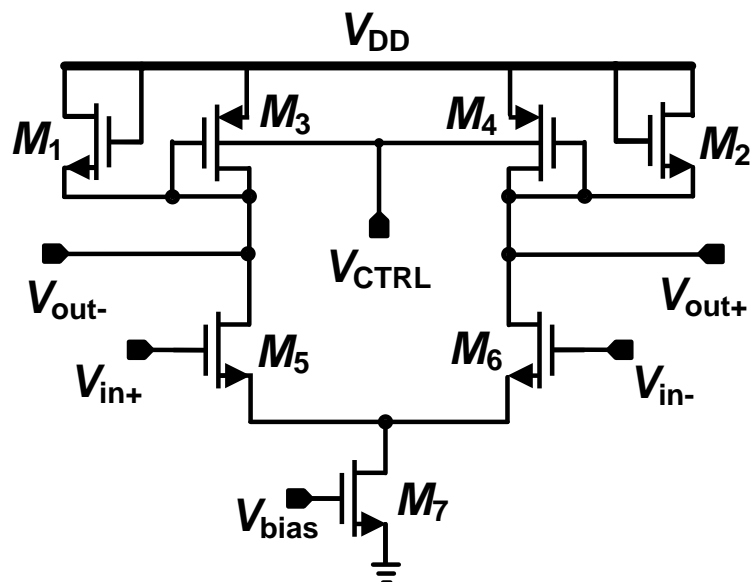


Figure 4-7 The proposed body-tuned VGA cell

In this design, the n-MOS load M_1 and M_2 , are biased in the sub-threshold region, while the p-MOS load M_3 and M_4 are biased in the saturation region. Thus the change in their transconductance $\Delta g_{m,1,2}$ and $\Delta g_{m,3,4}$ can be expressed as:

$$\Delta g_{m,1,2} = \frac{2\Delta I_{DS,1,2}}{nV_T}, \quad (4-13)$$

$$\Delta g_{m,3,4} = \frac{2I_{DS,3,4}}{V_{OV,3,4} + \Delta V_{OV,3,4}} \left(\frac{\Delta I_{DS,3,4}}{I_{DS,3,4}} - \frac{\Delta V_{OV,3,4}}{V_{OV,3,4}} \right), \quad (4-14)$$

As all other conditions are the same, (4-3) is also valid for this cell. Substituting (4-13) and (4-14) into (4-3) leads to:

$$A_v = \frac{g_{m,5,6}}{g_{m,1,2} + g_{m,3,4} + \frac{2\Delta I_{DS,1,2}}{nV_T} + \frac{2I_{DS,3,4}}{V_{OV,3,4} + \Delta V_{OV,3,4}} \left(\frac{\Delta I_{DS,3,4}}{I_{DS,3,4}} - \frac{\Delta V_{OV,3,4}}{V_{OV,3,4}} \right)}, \quad (4-15)$$

where $V_{OV,3,4}$ is the overdrive voltage and $V_{OV,3,4} = V_{GS,3,4} - V_{TH,3,4}$. According to (4-5), (4-15) can be rewritten as following as is only related to M_3 and M_4 :

$$A_v = \frac{g_{m,5,6}}{g_{m,1,2} + g_{m,3,4} - \frac{2\Delta I_{DS,3,4}}{nV_T} + \frac{2I_{DS,3,4}}{V_{OV,3,4} + \Delta V_{OV,3,4}} \left(\frac{\Delta I_{DS,3,4}}{I_{DS,3,4}} - \frac{\Delta V_{OV,3,4}}{V_{OV,3,4}} \right)}, \quad (4-16)$$

The basic p-MOS I-V equations for M_3 and M_4 with channel-length modulation neglected can be written as:

$$I_{DS,3,4} = \frac{1}{2}K_P V_{OV,3,4}^2 = \frac{1}{2}K_P (V_{GS,3,4} - V_{TH,3,4})^2, \quad (4-17)$$

where

$$K_P = \mu_P C_{ox} \left(\frac{W}{L} \right)_{3,4}. \quad (4-18)$$

The percentage change in $I_{DS,3,4}$ is larger than the percentage change in $V_{OV,3,4}$ due to their quadratic relationship as shown in (4-17) and of the same polarity. On the other hand, $V_{OV,3,4} + \Delta V_{OV,3,4}$ is always much larger than nV_T due to their different operation region. Thus the following inequality is established:

$$\left| \frac{2I_{DS,3,4}}{V_{OV,3,4} + \Delta V_{OV,3,4}} \left(\frac{\Delta I_{DS,3,4}}{I_{DS,3,4}} - \frac{\Delta V_{OV,3,4}}{V_{OV,3,4}} \right) \right| < \left| \frac{2\Delta I_{DS,3,4}}{V_{OV,3,4} + \Delta V_{OV,3,4}} \right| \ll \left| \frac{2\Delta I_{DS,3,4}}{nV_T} \right|. \quad (4-19)$$

Thus the last term in the denominator of (4-16) can be ignored and the gain can be approximated as:

$$A_v \approx \frac{g_{m,5,6}}{g_{m,1,2} + g_{m,3,4} - \frac{2\Delta I_{DS,3,4}}{nV_T}}. \quad (4-20)$$

The threshold voltage with body effect considered can be expressed as follows:

$$V_{TH,3,4} = V_{TH0} - \gamma_P (\sqrt{V_{SB,3,4} + 2\phi_F} - \sqrt{2\phi_F}), \quad (4-21)$$

where V_{TH0} is the threshold voltage without considering body effect, γ_P and ϕ_F are body effect related parameters.

As long as the n-MOS load transistors M_1 and M_2 are large enough and stays in sub-threshold region, the change in $V_{GS,1,2} = -V_{GS,3,4}$ can be ignored and $\Delta I_{DS,3,4}$ only depends on

the change in $V_{TH,3,4}$. With (4-21) substituted into (4-17) and $V_{GS,3,4}$ constant, $\Delta I_{DS,3,4}$ can be obtained by taking the derivative of $I_{DS,3,4}$ w.r.t. $V_{SB,3,4}$ multiplied by $\Delta V_{SB,3,4}$:

$$\Delta I_{DS,3,4} = \frac{0.5\gamma_P * \sqrt{2I_{DS,3,4}K_P}}{\sqrt{V_{SB,3,4} + 2\phi_F}} \Delta V_{SB,3,4}. \quad (4-22)$$

The range for $V_{SB,3,4}$ is from 0 V to 0.6 V due to physical limitations. A negative $V_{SB,3,4}$ requires a voltage higher than V_{DD} and a separate source must be used, while $V_{SB,3,4} > 0.6$ V will forward bias the body-source junction, leading to observable body current. A center $V_{SB,3,4}$ of 0.3 V is used and $\Delta V_{SB,3,4}$ is within ± 0.3 V. All other constant terms are calculated at $V_{SB,3,4} = 0.3$ V.

The calculated relationship between $V_{SB,3,4}$, $\Delta I_{DS,3,4}$ and the overall voltage gain in dB is plotted in Figure 4-8.

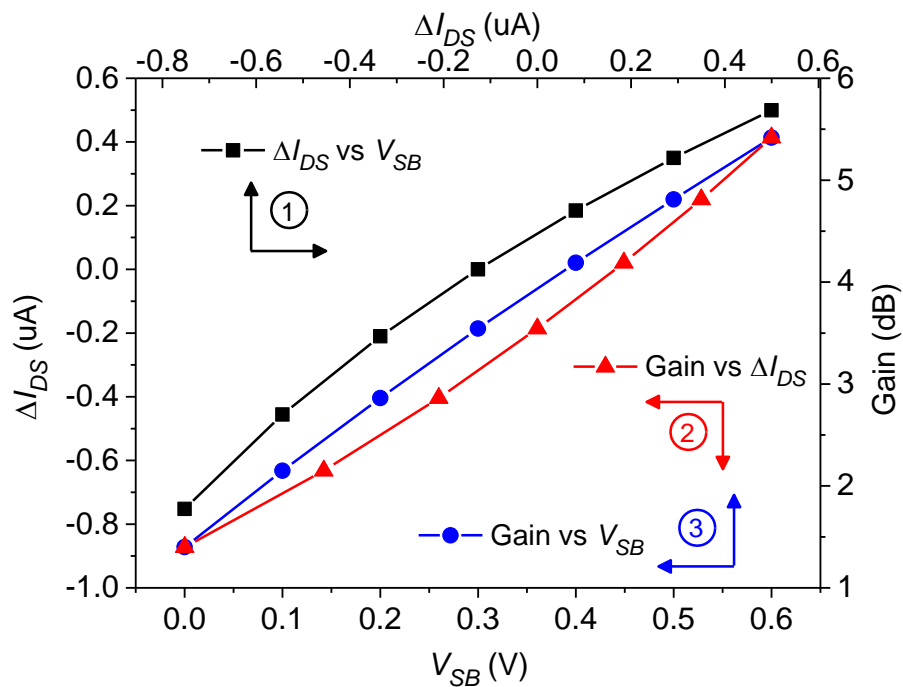


Figure 4-8 Calculated $\Delta I_{DS,3,4}$, $V_{SB,3,4}$ and gain relationship for the body-tuned VGA cell

The calculation is as follows:

- 1) The ΔI_{DS} vs. V_{SB} is plotted at the left-Y bottom-X axis,
- 2) The gain is plotted with ΔI_{DS} at the right-Y top-X axis,
- 3) The gain vs. V_{SB} is plotted at the right-Y bottom-X axis. Because ΔI_{DS} is directly related to V_{SB} based on (4-22), and the gain is directly related to ΔI_{DS} based on (4-20), the gain vs. V_{SB} is indirectly calculated.

As can be seen from Figure 4-8, $\Delta I_{DS,3,4}$ vs. $V_{SB,3,4}$ is plotted based on (4-22) and forms a convex relationship, and the gain vs. $\Delta I_{DS,3,4}$ is plotted based on (4-20) and forms a concave relationship. Although these two curves alone are not dB-linear, the resultant relationship of gain vs. $V_{SB,3,4}$ is compensated to be dB-linear. The size of the n-MOS load transistors and the p-MOS load transistors should be selected properly for the best gain compensation.

The simulated resistance at the output node is shown in Figure 4-9. The resistance is plotted in dB scale, and again the resultant resistance is similar to the final gain curve, with a difference of a factor of $g_{m,5,6}$. It can be seen from Figure 4-9 that the resultant load resistance is very straight, and the circuit is expected to be quite dB-linear.

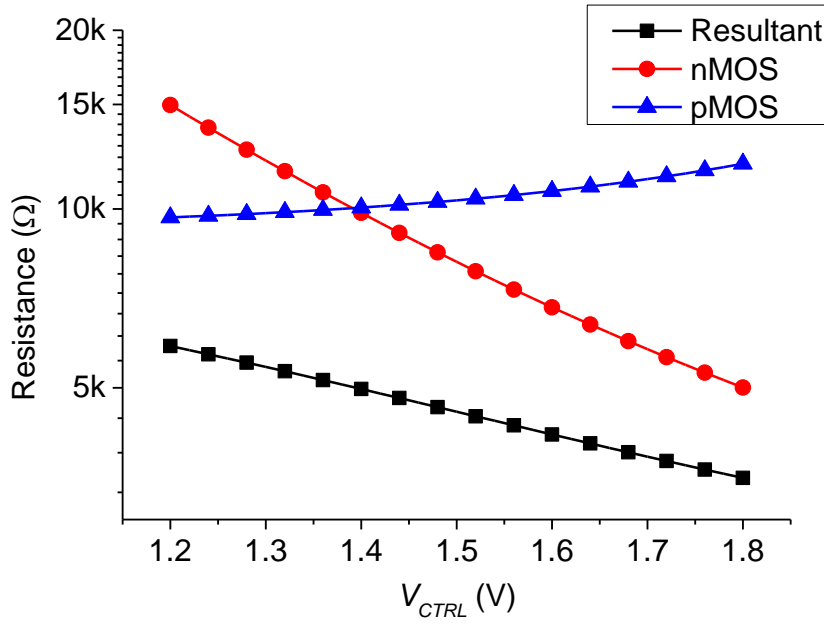


Figure 4-9 Simulated resistance at the output node for body-tuned VGA cell

The selection for the sizes of p-MOS transistors M_3 and M_4 to satisfy all the above mentioned equations is critical. When other conditions hold unchanged, varying the sizes of M_3 and M_4 changes K_p , as it is related to the W/L ratio as shown in (4-18), and thus to $I_{DS,3,4}$ according to (4-17). For a smaller device, both K_p and $I_{DS,3,4}$ are smaller, resulting in a smaller $\Delta I_{DS,3,4}$ and a smaller gain variation range. To increase the gain variation range, larger device can be used. If a larger device is selected, $I_{DS,3,4}$ are larger, resulting in a larger $\Delta I_{DS,3,4}$ and gain variation range. As long as the above mentioned equations still hold, the larger device is used, the larger voltage gain can be achieved. However, further increasing the size of the device is undesirable, as M_3 and M_4 cannot draw more current and $\Delta I_{DS,3,4}$ is almost flat, leading to curvy gain characteristic and significant gain error. As shown in Figure 4-10, the width of the p-MOS transistor is selected to be 2 μm for a 360 nm long device in 0.18 μm CMOS technology.

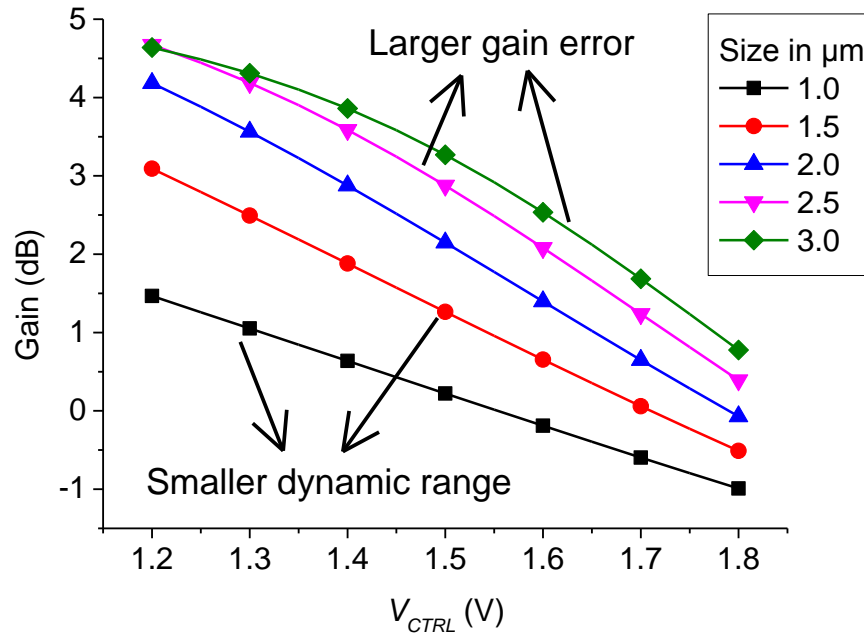


Figure 4-10 Simulated gain for various p-MOS sizes of the body-tuned VGA cell

On the other hand, the selection for the size of n-MOS transistors M_1 and M_2 is also important and is as follows. As can be seen from Figure 4-11, as long as the n-MOS transistor is large enough to be biased in the sub-threshold region, the accurate dB-linear characteristic can be achieved. Following the same discussion, that for a large n-MOS transistor, the current distribution between the p-MOS load and the n-MOS load will follow the former, as the current in a sub-threshold n-MOS transistor can vary significantly and the change in $V_{GS,1,2}$ can be ignored. Thus, for large n-MOS transistors, $\Delta I_{DS,3,4}$ will follow the same trend and the resultant gain is always dB-linear with a large gain variation range. For a small n-MOS transistor, sharing $\Delta I_{DS,3,4}$ will drive the n-MOS transistors out of the sub-threshold region, with a trend of decreasing $\Delta I_{DS,3,4}$. Thus the gain characteristic is curvy with a smaller gain variation range. In this design, an optimized n-MOS transistor width of $4.5 \mu\text{m}$ is selected for a 360 nm long device in $0.18 \mu\text{m}$ CMOS technology.

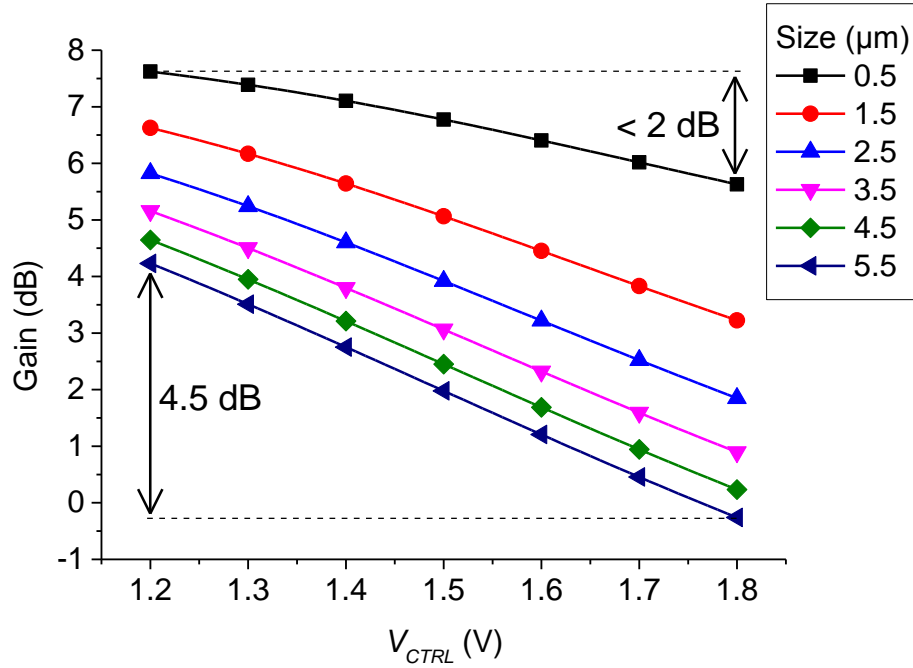


Figure 4-11 Simulated gain for various n-MOS sizes of the body-tuned VGA cell

The final device size for the body-tuned VGA cell is listed in Table 4-2.

Table 4-2 Device size list for body-tuned VGA cell

Component	Width (μm)	Length (μm)
n-MOS M_1 and M_2	4.5	0.36
p-MOS M_3 and M_4	2	0.36
M_5 and M_6	4	0.36
M_7	3	0.36

4.3 Bandwidth extension for high-frequency VGA

4.3.1 Gate peaking technique for bandwidth extension

The schematic of a classical gate peaking technique and its modified version are shown in Figure 4-12(a) and Figure 4-12(b), respectively.

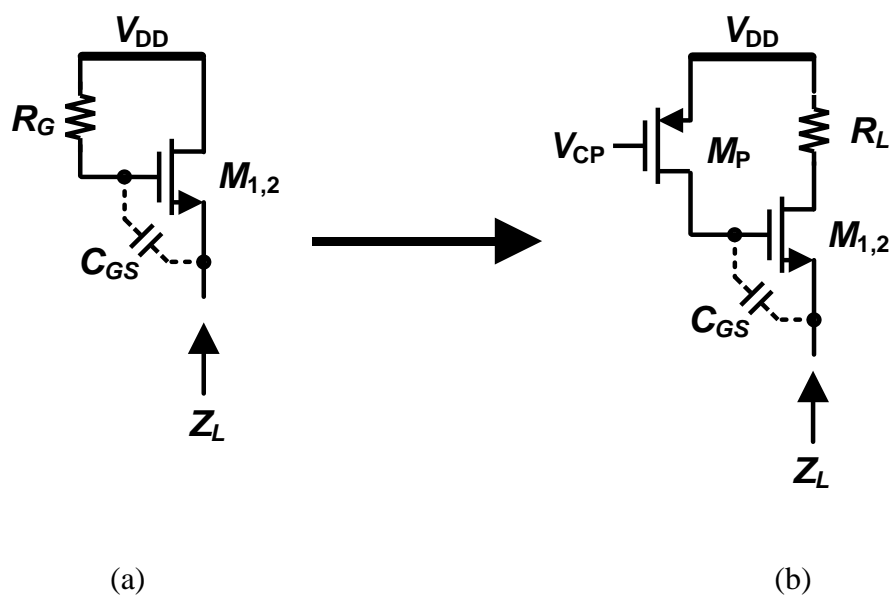


Figure 4-12 Schematic of (a) classical gate peaking (b) modified topology

The impedance looking into the source of $M_{1,2}$, Z_L , can be expressed as:

$$Z_L = \frac{1 + sC_{GS}R_G}{g'_{m,1,2} + sC_{GS}} \quad (4-23)$$

The impedance is plotted in Figure 4-13. As can be seen from Figure 4-13, for a certain frequency range, this behaves as an active inductor. The equivalent circuit of the active inductor is shown in Figure 4-14.

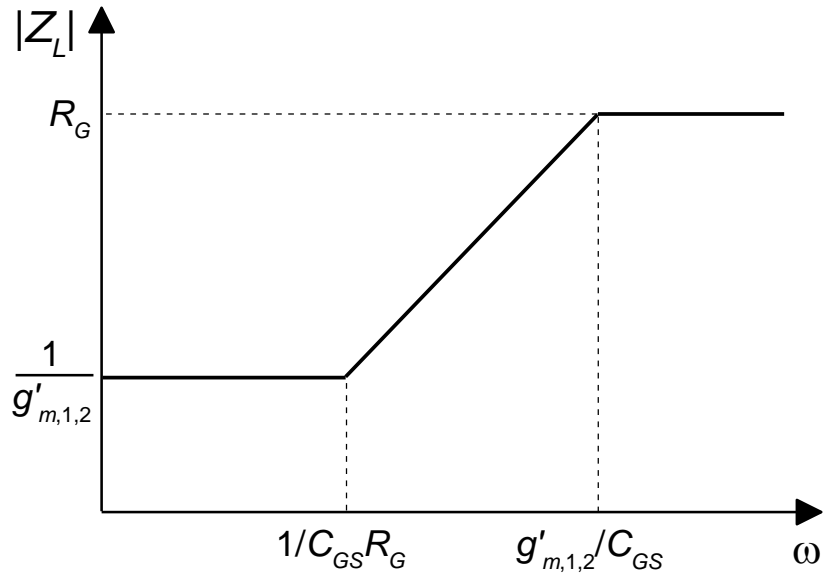


Figure 4-13 Impedance of an active inductor

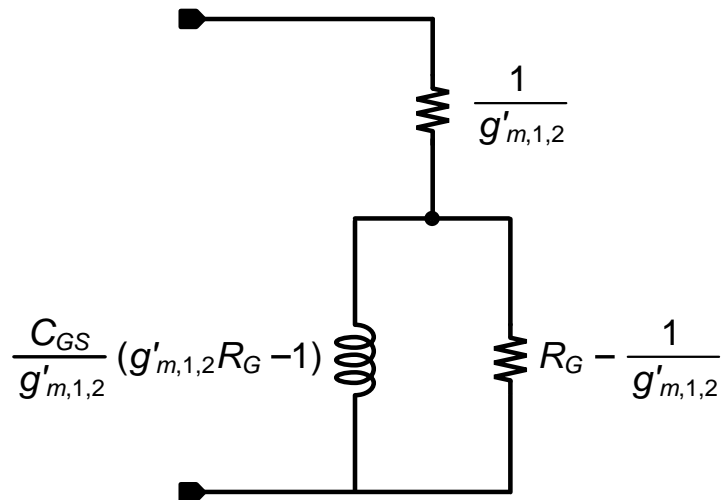


Figure 4-14 Equivalent circuit of the active inductor

This gate peaking technique is applied to the gate-tuned VGA cell as shown in Figure 4-4, and thus (4-23) can be substituted in (4-2) as $1/g_{m,1,2}$, and the new gain expression, A_{new} , is as follows:

$$A_{new} = \frac{g_{m,5,6}(1 + sC_{GS}R_G)}{g'_{m,1,2} + sC_{GS} + g_{m,3,4}(1 + sC_{GS}R_G)}. \quad (4-24)$$

It can be seen that one zero is introduced in (4-24), due to the existence of the gate resistor, R_G . The corner angular frequency of the zero $\omega_z = -1/C_{GS}R_G$.

4.3.2 Gain ripple control

By observation, the dominant pole of the output node, $\omega_{P,out}$ is expressed as:

$$\omega_{P,out} = -\frac{g_{m,1,2} + g_{m,3,4}}{C_{total,out}}, \quad (4-25)$$

where $C_{total,out}$ is the total capacitance at the output node.

To effectively trade off the bandwidth and gain flatness, several scenarios for the location of poles and zeroes are investigated and plotted in Figure 4-15. It can be seen from Figure 4-15 that depending on the relative frequency location of the poles and zeroes, the gain characteristic at higher frequency is different. One of the observations is that when the frequency of the zero is small enough, wide bandwidth can be achieved with a cost of large gain ripple. In practice, the gain ripple must be controlled within an acceptable range, which is required to be less than 1 dB for our targeted application [27]. In addition, the variation in gain ripple will result in significant gain error at the frequency where the gain peaks, thus it should also be made as small as possible. Nevertheless, a zero helps to improve the bandwidth in all cases.

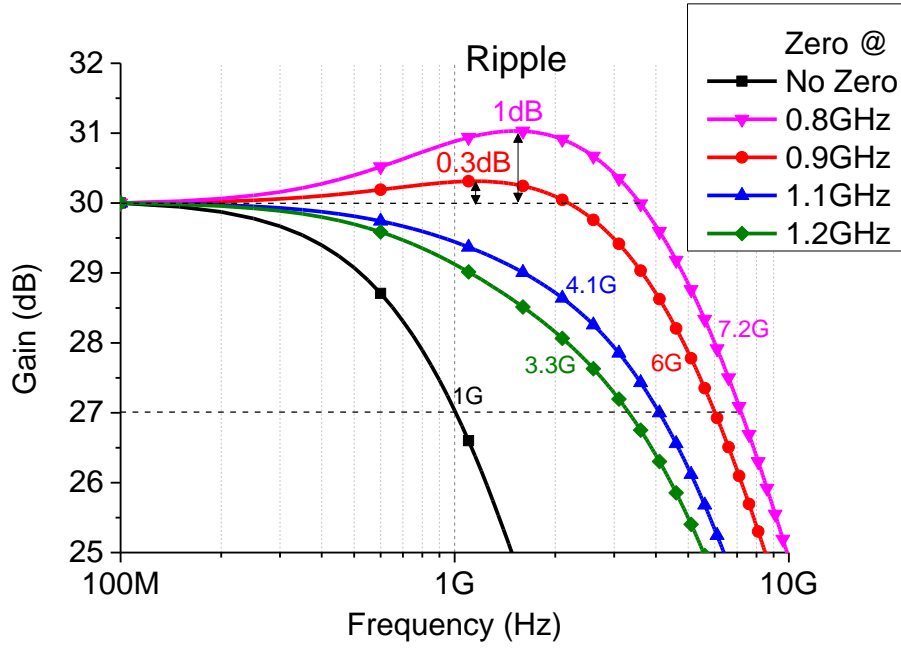


Figure 4-15 Simulated gain characteristics with two poles at 1 GHz and 5 GHz, one zero at 0.8/0.9/1.1/1.2 GHz or no zero

In this design, when the VGA is tuned from its highest gain setting to its lowest, $\omega_{P,out}$ also changed as the sum of $g_{m,1,2}$ and $g_{m,3,4}$ is changed. Thus, ω_Z must also be varied simultaneously with $\omega_{P,out}$ so that relatively large frequency variations due to undesired gain peaking (pink line, ▼) or early gain roll off (green line, ◆) can be prevented, which is demonstrated in Figure 4-15.

In order for the zero to be tunable, the fixed resistor R_G is replaced by a p-MOS transistor M_P operating in the triode region as shown in Figure 4-12(b) and the final complete schematic of the high-frequency VGA cell is shown in Figure 4-16. Note that in Figure 4-16, the control voltage is represented as V_{CN} , which is equivalent to V_{CTRL} in Figure 4-4.

To minimize the design complexity of the VGA cell as well as effectively control the location of zero, a control voltage generator is designed. In such a way, V_{CP} can be generated,

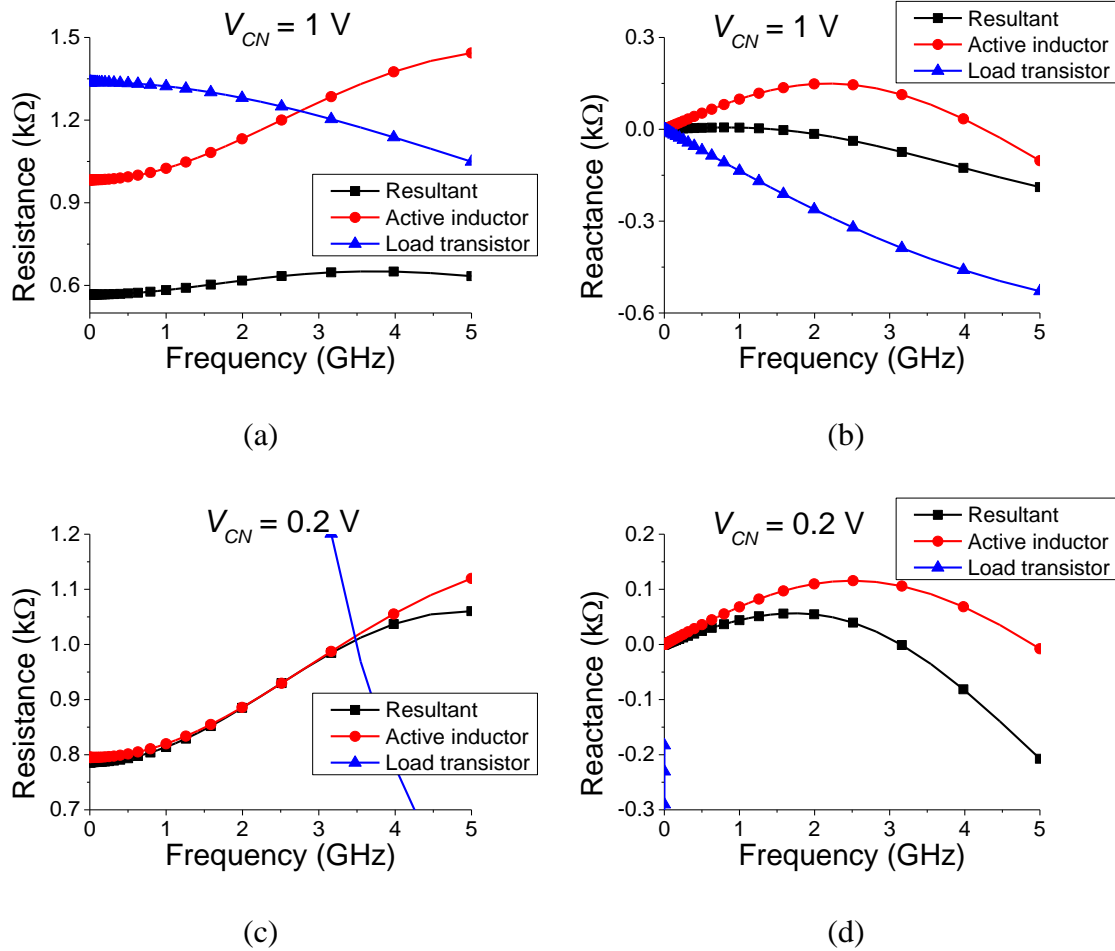
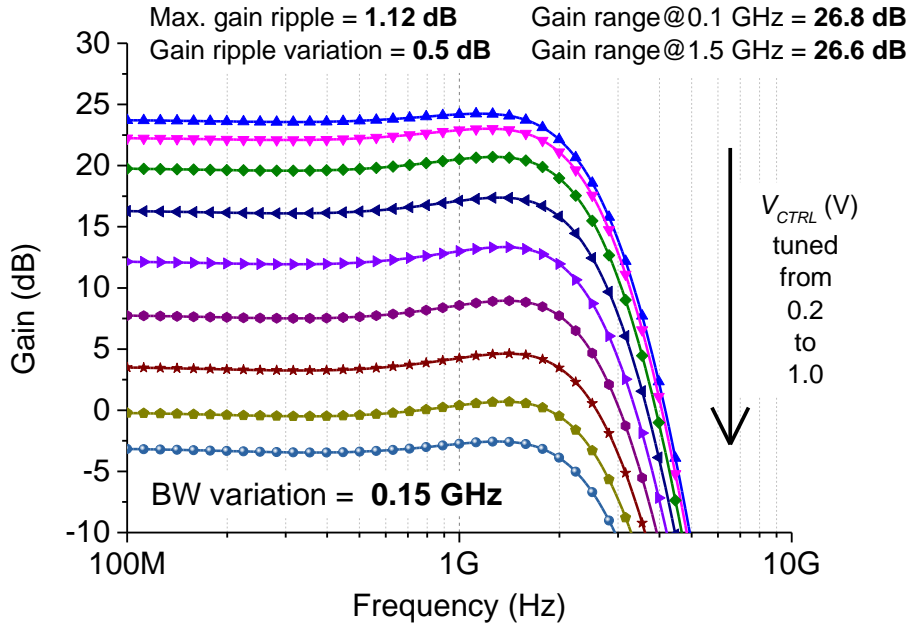


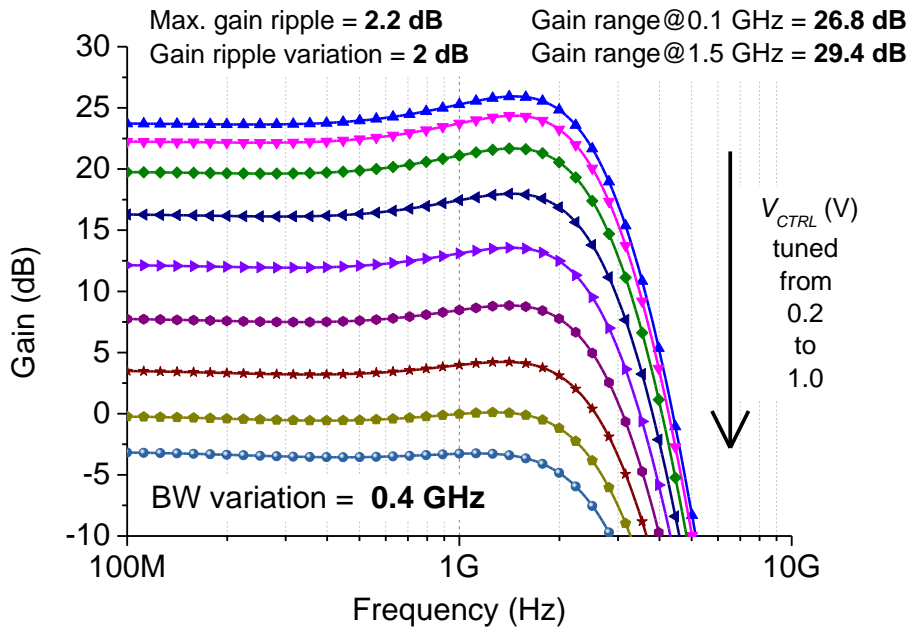
Figure 4-17 Simulated impedance at the output node for high-frequency VGA cell

(a) real (b) imaginary for 1 V V_{CN} , (c) real (d) imaginary for 0.2 V V_{CN}

To further investigate the performance variation caused by V_{CP} , the frequency responses of the overall VGA with different bias schemes is compared and shown in Figure 4-18. It can be seen from Figure 4-18, if M_P is biased by the dynamically controlled V_{CP} , the overall performance of the maximum gain ripple, ripple variation and bandwidth variation are better than biased by a fixed V_{CP} . The optimized maximum gain ripple, ripple variation and bandwidth variation is 1.12 dB, 0.5 dB and 0.15 GHz, respectively. In this way, the gain variation range can be kept constant throughout the entire frequency range, while the gain error at various frequencies is minimized.



(a)



(b)

Figure 4-18 Simulated gain characteristics for the 11-cell cascaded high-frequency VGA

(a) dynamic V_{CP} biased (b) fixed V_{CP} biased

The overall design procedure of the wideband inductorless unit cell is summarized as follows.

- 1) The resistor R_L is properly selected such that the gain variation range is wide enough.
- 2) The sizes of load transistors M_1 and M_2 are selected based on the trade-off between bandwidth extension and dB-linear characteristic.
- 3) M_P and their bias voltages are optimized for best gain flatness.

The simulated frequency responses for the optimized high-frequency VGA cell that is used for the 11-cell cascaded high-frequency VGA design are shown in Figure 4-19. It can be seen from Figure 4-19 that the simulated bandwidth of the unit cell is around 8 GHz, while a dB-linear gain range of 1.6 dB is achieved. Moreover, the designed unit cell only consumes 200 μA from a 1.2 V power supply.

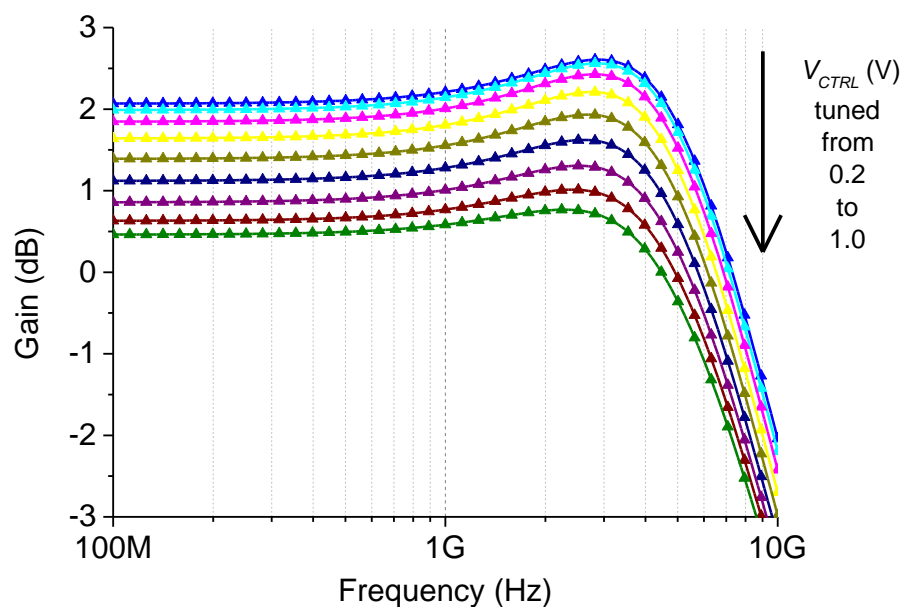


Figure 4-19 Simulated gain characteristic of the high-frequency VGA cell

Finally, again, the optimized device size for the high-frequency VGA cell based on the gate-tuned VGA cell with gate peaking technique is listed in Table 4-3.

Table 4-3 Device size list for high-frequency VGA cell

Component	Width (um)	Length (um)
n-MOS M_1 and M_2	4	0.15
n-MOS M_3 and M_4	4	0.15
M_5 and M_6	25.6	0.15
M_p	2	0.15
M_7	100	1

Chapter 5

Gate-tuned VGA in 0.18 μm CMOS

5.1 Overall VGA structure

The proposed gate-tuned VGA cell is implemented in a 5-cell gate-tuned VGA in 0.18 μm CMOS technology. The schematic of the VGA cell is the same as in Figure 4-4, and the block diagram is shown in Figure 5-1.

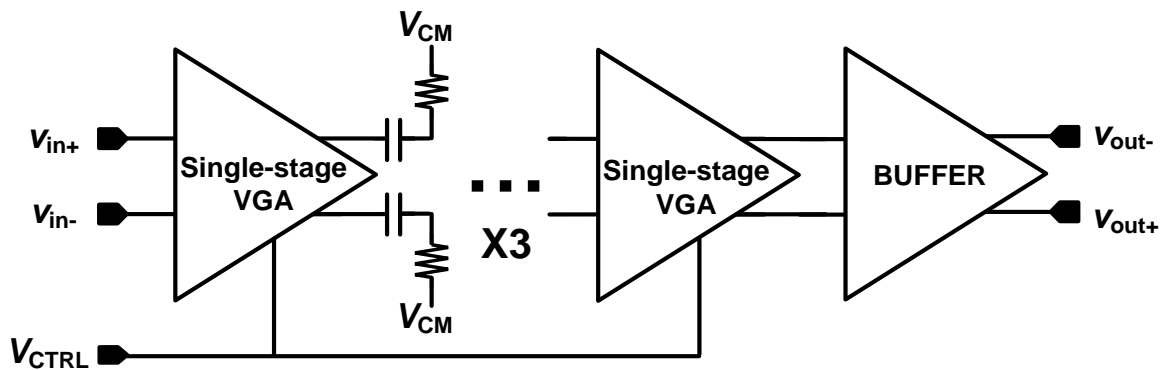


Figure 5-1 The proposed gate-tuned VGA in 0.18 μm CMOS technology

Simulation results showed that the designed unit cell only consumes 16 μA from a 1.8 V power supply, while a gain error of 0.2 dB over a dB-linear gain range of 9 dB is achieved.

5.2 DC offset issue

The number of unit cells to be cascaded is determined according to the system specification. From a practical design point of view, DC-coupled VGA can be designed for compactness and simplicity. However, the frequency response of such VGA may suffer from the DC-offset issue. In addition, the AC-coupled VGA with common-mode bias voltage applied at each stage can handle much larger DC-offset even with a high gain setting, although it occupies relatively larger area than the DC-coupled one. Thus, it guarantees the final yield. To demonstrate the usefulness of the cascaded VGA, an AC-coupled 5-cell VGA is presented.

5.3 Implementation and measurement

To verify the performance, the presented VGA in Figure 5-1 is fabricated in Globalfoundries' 0.18 μm CMOS technology. The on-wafer measurement was performed using an Agilent E8364B vector network analyzer (VNA), which operates from 10 MHz to 50 GHz. In order to drive the 50 Ω VNA, a differential buffer was included after the VGA and was also fabricated separately. The buffer is measured to have 16 dB of attenuation at all frequency. In the following discussion, the attenuation of the buffer is always de-embedded from the measurement, so that the performance of the "core" circuit can be effectively reflected. Moreover, a fixed frequency of 20 MHz is used for all the gain and gain error characterization, output $P_{1\text{dB}}$ and IRN measurements.

Figure 5-2 shows the measured and simulated dB-linear gain characteristics of the fabricated gate-tuned VGA. A gain variation range of 71 dB is measured, among which 45

dB is dB-linear with less than 1 dB gain error. The power consumption of the gate-tuned VGA is only 81 μA under a 1.8 V power supply.

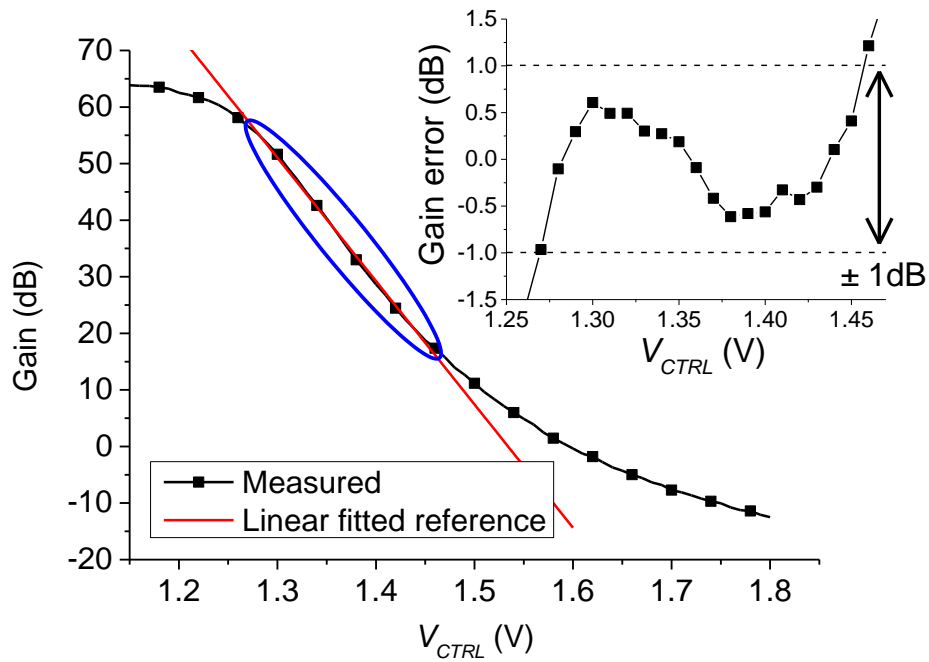


Figure 5-2 Measured gain characteristics and gain error for the gate-tuned VGA

The measured frequency responses of the gate-tuned VGA against V_{CTRL} are shown in Figure 5-3. The bandwidth is varied from 50 MHz to 209 MHz while the gain setting is varied from the highest to the lowest. The simulated -3 dB low cut-off frequency as determined by the RC circuit in AC-coupling circuitry is 36 kHz, which is below the measureable frequency of the VNA, thus it is not measured.

Moreover, both the measured output P_{1dB} and IRN vs. V_{CTRL} are presented in Figure 5-4. As can be seen from Figure 5-4, the output P_{1dB} is around 0 dBm, while the minimum IRN is 7.5 $\text{nV}/\sqrt{\text{Hz}}$ at the highest gain setting.

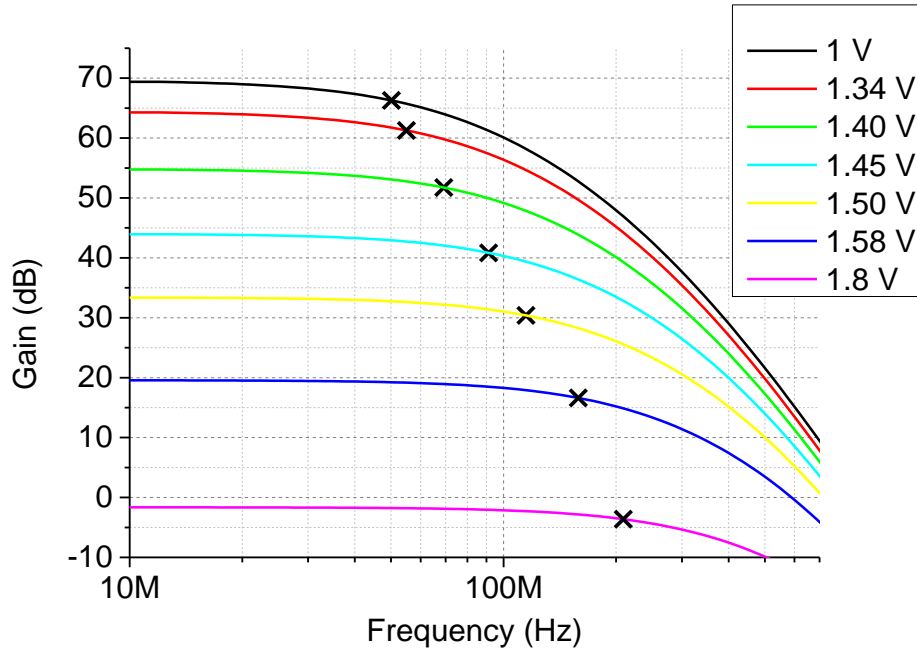


Figure 5-3 Measured frequency response for the gate-tuned VGA

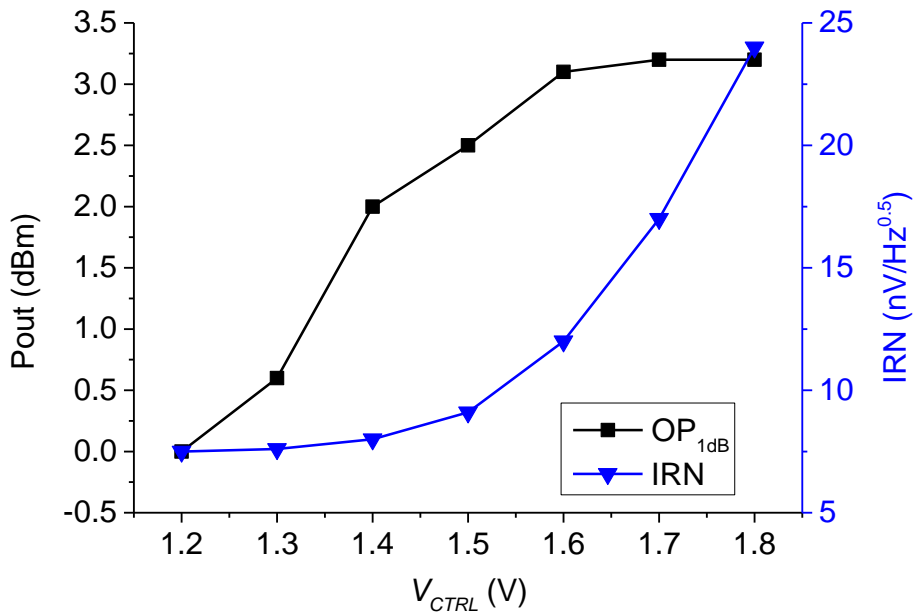


Figure 5-4 Measured output P_{1dB} and IRN vs. V_{CTRL} for the gate-tuned VGA

Figure 5-5 shows the die photo of the fabricated VGA. It can be seen that the gate-tuned VGA cell is very compact as $24 \mu\text{m} \times 7 \mu\text{m}$, and the main area-consuming block is the AC-coupling capacitors. The overall area with AC-coupling circuitry is $200 \mu\text{m} \times 170 \mu\text{m}$, and can be effectively reduced if a higher -3 dB low cut-off frequency is acceptable. Even with the AC-coupling circuitry, the size is still not large and is very comparable to other published VGAs.

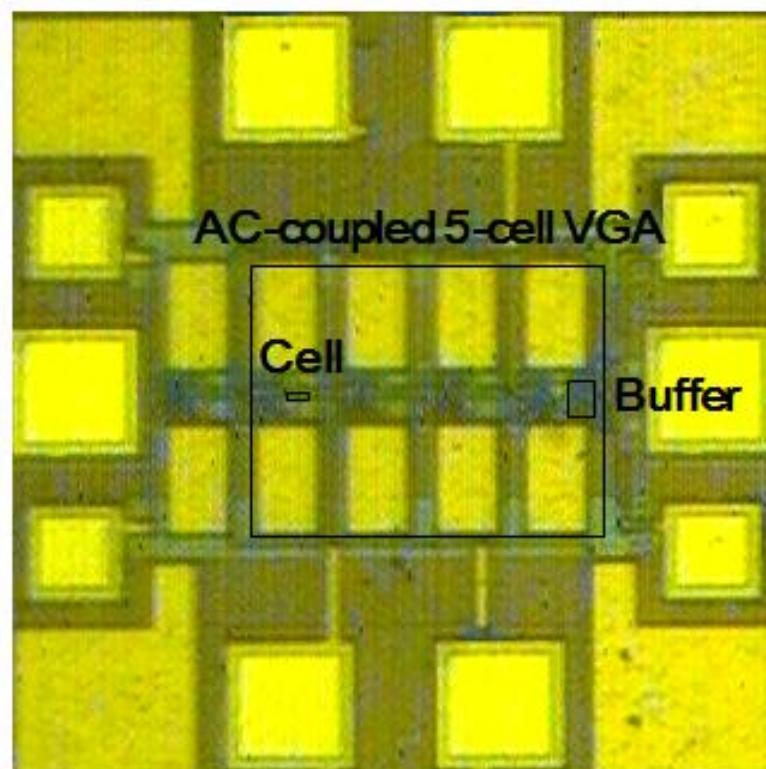


Figure 5-5 Die photo of the fabricated gate-tuned VGA with size: VGA core $200 \times 170 \mu\text{m}^2$,
unit cell $24 \times 7 \mu\text{m}^2$, buffer $43 \times 30 \mu\text{m}^2$

5.4 Summary and Comparison

A simple cell-based approach is presented for the design of ultra-low power and high-frequency VGA. To utilize the proposed approach, the design and analysis of a unique gate-

tuned VGA cell has been presented, which utilizes complementary devices as the load. Since this gate-tuned VGA cell requires no extra circuit to generate an exponential-like function, it drastically reduces the power consumption. Therefore, the presented approach is suitable for many applications, where ultra-low power, high frequency and accurate dB-linear characteristic are required. A comparison between the proposed gate-tuned VGA with recently published work is summarized in Table 5-1.

Table 5-1 Performance summary and comparisons of the proposed gate-tuned VGA with other state-of-the-art works

	[4] TCAS-I 2006	[5] EL 2007	[6] JSSC 2013	[7] JSSC 2009	[8] TCAS-I 2012	This work
DC power (mW)	6.5	1.4	2.2	2.2	5	0.15
f_{-3dB} (MHz)	32	23	15	40	76	50
Gain range (dB)	95	86	76	65	65	71
dB-lin. gain (dB)	95	68	50	40	40	45
Gain error (dB)	1	1	0.5	0.8	1	1
OP _{1dB} (dBm)	-7	-15	2*	12*	2.3	0
IRN (nV/ $\sqrt{\text{Hz}}$)	n/a	n/a	3.5	11	n/a	7.5
V _{DD} (V)	1.8	1.8	1.2	1.2	1.8	1.8
Technology (nm)	180	180	65	65	180	180

*Estimated from IP3 result

Chapter 6

Body-tuned VGA in 0.18 μm CMOS

6.1 Body-tuned 10-cell VGA in 0.18 μm CMOS

6.1.1 Overall cell-based VGA structure

Using the proposed body-tuned VGA cell, a 10-cell body-tuned VGA can be simply implemented by directly cascading 10 cells. The simplified block diagram of the presented 10-cell body-tuned VGA is shown in Figure 6-1.

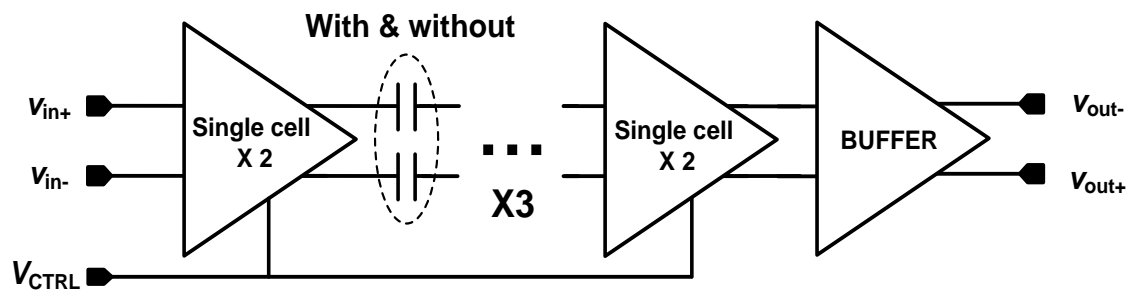


Figure 6-1 Block diagram of the 10-cell body-tuned VGA with and without AC-coupling

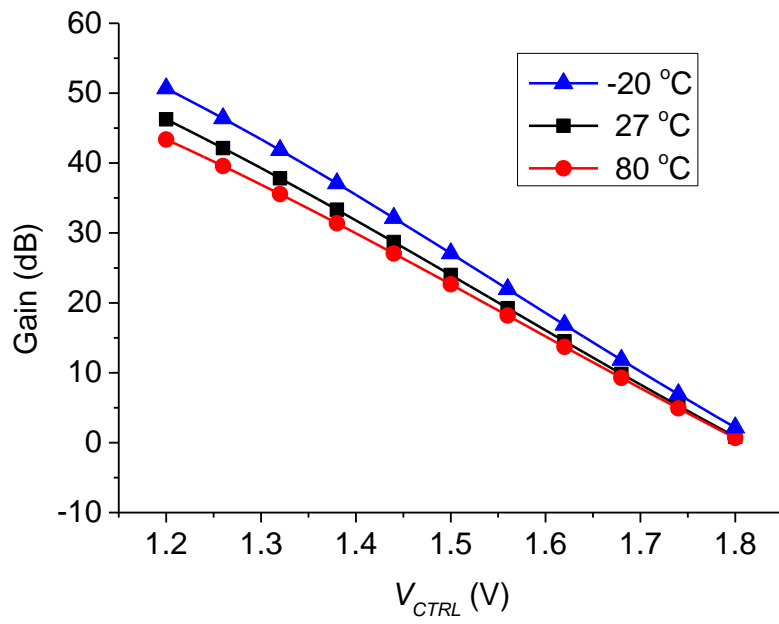
Simulation results showed that the body-tuned VGA cell as shown in Figure 4-7 exhibits low power consumption, small area and wide bandwidth beyond 1 GHz. It can also achieve an extremely small gain error of 0.015 dB over a gain variation range of 4 dB, or 0.4% of the gain variation range.

6.1.2 *DC offset issue*

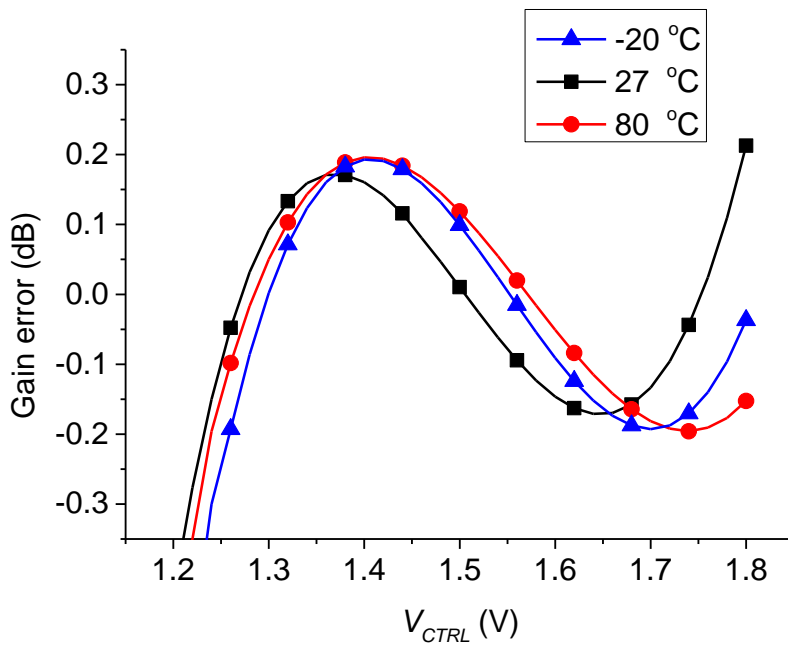
From a practical design point of view, the mismatch of transistors should be taken into account. As shown in Figure 4-10 and Figure 4-11, the unit cell has a gain variation range of 4 dB. Therefore, 10 body-tuned VGA cells should achieve a dB-linear gain range of 40 dB. However, directly cascading 10 such cells may lead to a DC offset issue at high gain settings. Thus, two approaches, with and without DC offset cancellation are implemented. Although both AC-coupling [8] and DC feedback loop can be used to eliminate the DC offset issue, AC-coupling is chosen for its simplicity. To demonstrate the feasibility of the proposed method, AC-coupling circuitry is inserted between every two cells to guarantee the overall performance.

6.1.3 *Temperature variation consideration*

The simulated dB-linear characteristic of the designed 10-cell body-tuned VGA in terms of dB-linear gain range and gain error with three typical temperature, -20°C , 27°C and 80°C , are shown in Figure 6-2(a) and Figure 6-2(b), respectively. As can be seen from Figure 6-2(a), the temperature variation does affect the dB-linear gain range. As the temperature goes higher, the dB-linear gain range is reduced. On the other hand, the gain error is almost insensitive to temperature variations, as illustrated in Figure 6-2(b).



(a)



(b)

Figure 6-2 Simulated gain characteristic with temperature variations for the 10-cell body-tuned VGA (a) gain variation range (b) gain error

The simulated body current of the p-MOS transistor in the designed VGA cell with various temperature is plotted in Figure 6-3. The 0.6 V source-body bias for the p-MOS transistor is constant and reliable across various corners although not shown, becomes an issue when the temperature is very high. The body current is in the range of tens of μA . Thus some room should be reserved when it is used under high temperature.

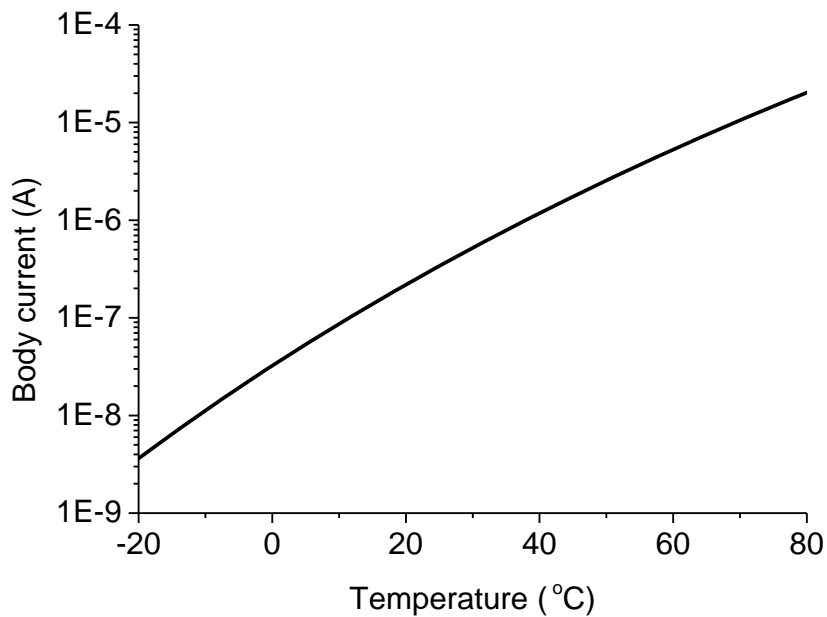


Figure 6-3 Body current with various temperature

6.1.4 Design consideration for “skew” process variations

To further demonstrate the robustness and usefulness of the presented approach, the impact of process variations on the dB-linear characteristic of the 10-cell body-tuned VGA is investigated. For simplicity, in Figure 4-7, “self-biased” n-MOS transistors are used at the load so that no additional bias voltage is required. Since both the n-MOS and p-MOS transistors are used in the design, the parameters of both transistors may not have identical

tendency with respect to process variations, despite that they work well within a wide range of temperature.

To guarantee the performance under “skew” case, such as SF and FS corners, the body-tuned VGA cell can be modified as shown in Figure 6-4. In order to weight and divert the current between the n-MOS and p-MOS devices of the presented VGA cell, a one-time calibration voltage V_{CAL} at the gate nodes of the n-MOS transistors M_1 and M_2 is introduced. The value of such calibration voltage can be selected according to the results of the process control monitoring (PCM) on the same reticle. In contrast to the circuit presented in Figure 4-7 where $V_{CAL} = V_{DD}$, this one-time calibration voltage can be varied to force the n-MOS device to operate in sub-threshold region. With an appropriate selection on V_{CAL} , the dB-linear gain characteristic of the 10-cell body-tuned VGA, as shown in Figure 6-5, can be restored and tuned insensitive to process variations.

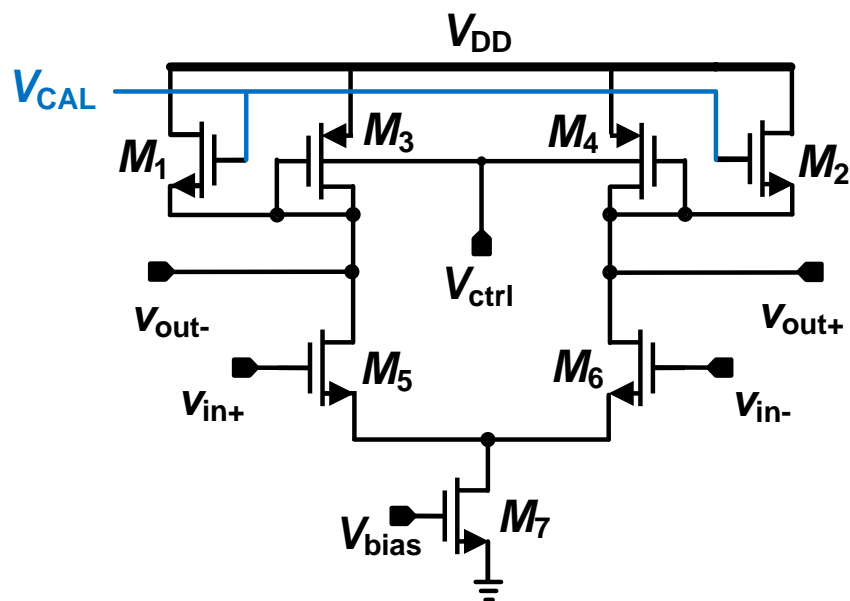


Figure 6-4 Schematic of the modified 10-cell body-tuned VGA cell

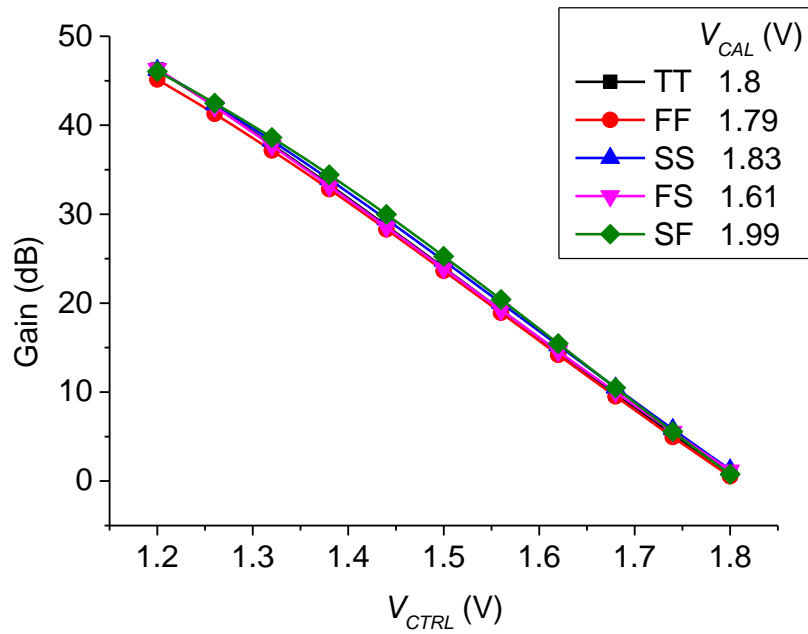


Figure 6-5 Simulated gain characteristic with process variations for the 10-cell body-tuned VGA with modified VGA cell

6.2 Body-tuned 15-cell reconfigurable VGA in 0.18 μm CMOS

6.2.1 Overall VGA structure

The presented “cell-based” method can be used for a cascaded VGA design, as well as to design a reconfigurable VGA which can also be used as tunable PGA. The simplified block diagram of the designed 15-cell reconfigurable VGA consisting 0 to 15 cells with AC coupling circuitry is shown in Figure 6-6.

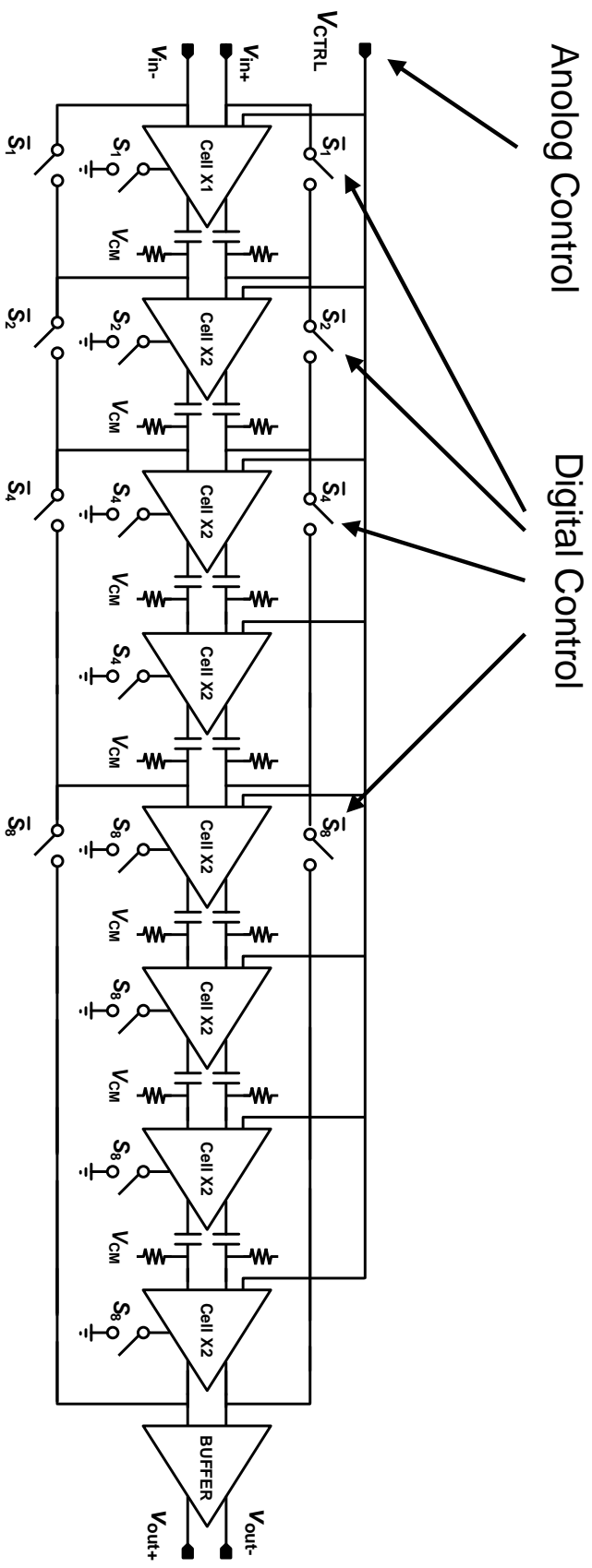


Figure 6-6 Block diagram of the fabricated reconfigurable body-tuned VGA

As can be seen from Figure 6-6, 15 body-tuned VGA cells are cascaded and controlled by a 4-bit digital signal so that gain re-configurability and power scalability can be demonstrated. Again, AC-coupling circuitry is inserted between every two cells. The power consumption stepped from 0 to 15 times that of the unit cell depending on the digital bits, and it consumes 0.62 mA at the highest gain setting. The details of this design working as reconfigurable VGA and tunable PGA are discussed in the following Sections.

6.2.2 Reconfigurable VGA

The simulated gain of the VGA as a function of the analog control voltage is plotted in Figure 6-7.

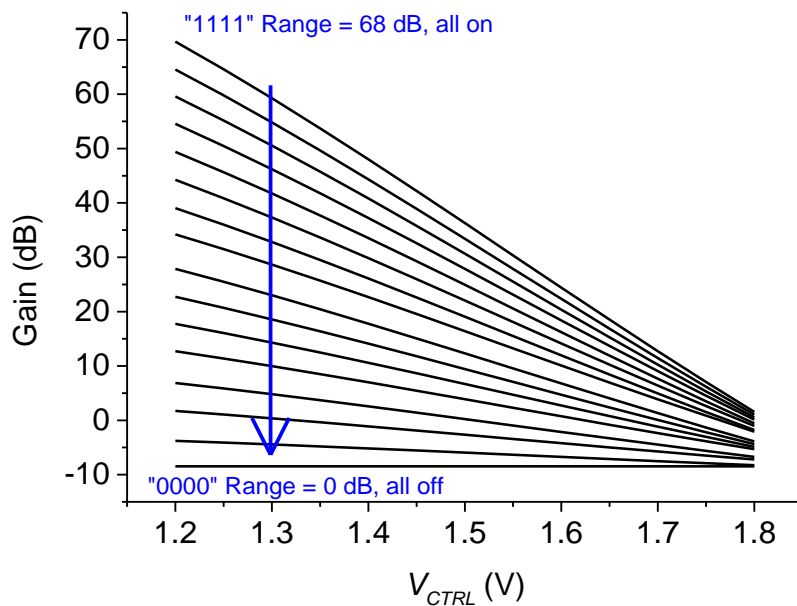


Figure 6-7 Simulated gain characteristic of the reconfigurable body-tuned VGA

When it is working as a VGA, 16 different gain settings can be configured accordingly, while the 4-bit digital control signal is varied from “0000” to “1111”. As can be seen from Figure 6-7, that the overall gain variation range can be reconfigured from 0 dB to

68 dB based on the digital bits. The tuning sensitivity as well as the gain error will also be scaled accordingly. Moreover, the power consumption depends on how many cells are on, and will also be scaled with digital bits.

6.2.3 Tunable PGA

The simulated gain of the VGA as a function of the digital control stream is plotted in Figure 6-8. When it is working as a PGA, digital control and discrete gain steps are realized with the freedom of varying V_{CTRL} to change the step size and the overall gain variation range. Other than that, the power consumption is true binary-weighted as discussed in Section 3.4.2.

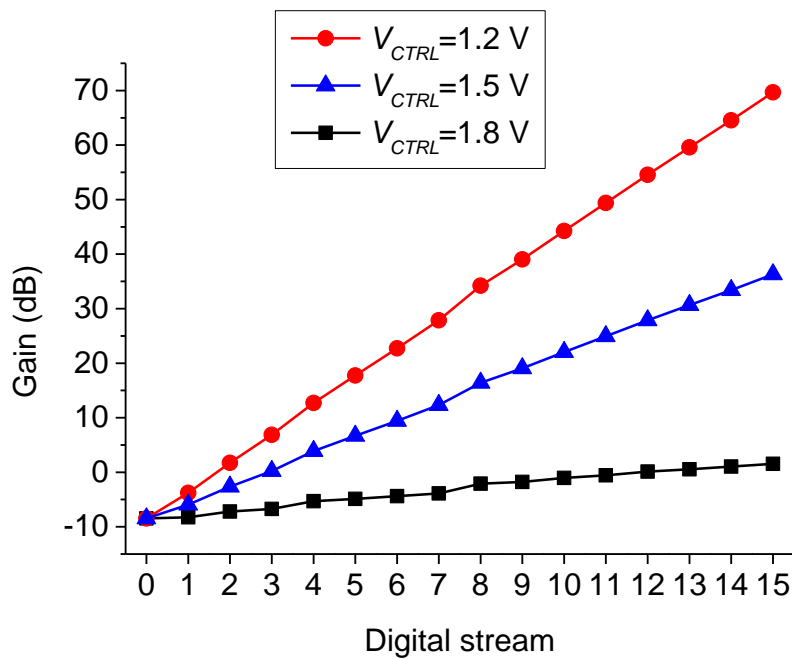


Figure 6-8 Simulated gain characteristic of the tunable body-tuned PGA

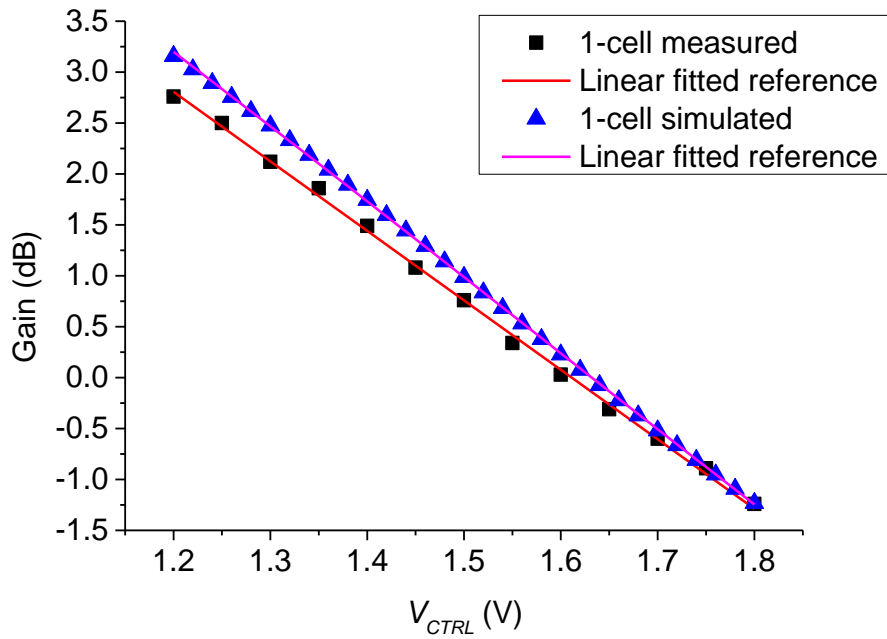
6.3 Implementation and measurement

6.3.1 Implementation and measurement setup

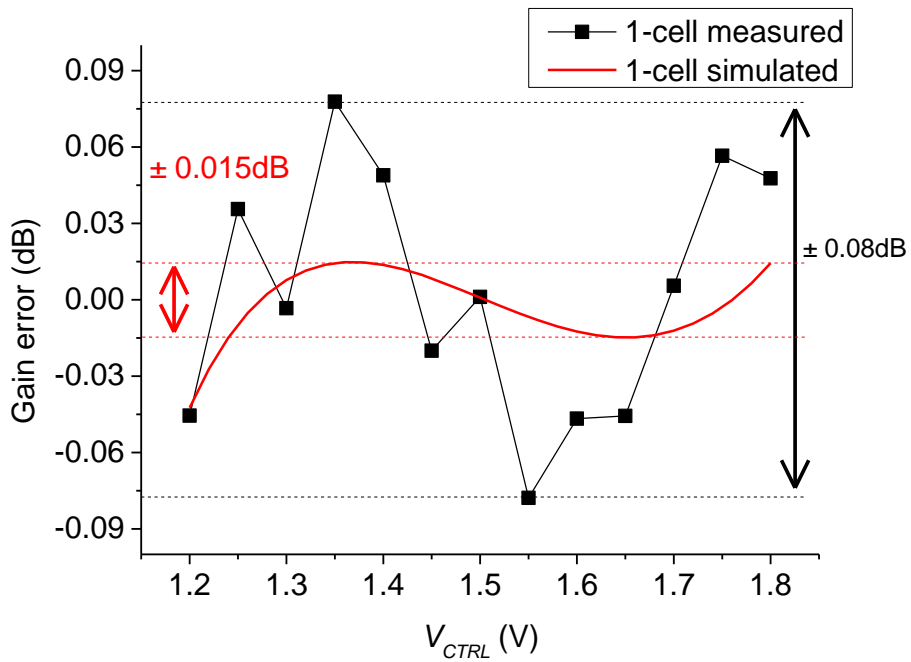
To verify the proposed design method, the VGAs shown in Figure 6-1 and Figure 6-6 were fabricated in Globalfoundries' 0.18 μm CMOS technology. Other than that, a single-cell and a 5-cell VGA without any DC offset cancellation circuitry were also fabricated for evaluation purpose. The on-wafer measurement was performed using an Agilent E8364B VNA, which operates from 10 MHz to 50 GHz. In order to drive the 50 Ω VNA, a differential buffer is included after each VGA and is also fabricated separately for de-embedding purpose. The buffer is measured to have 16 dB of attenuation at all frequency. In the following discussion, the attenuation of the buffer is always de-embedded from the measurement, so that the performance of the "core" circuit can be effectively reflected. Again, a fixed frequency of 20 MHz is used for all of the dB-linear gain characterization, output P1dB and IRN measurements.

6.3.2 Gain variation, dB-linear range and gain error

The measured and simulated gain characteristic in terms of gain variation range and gain error of the single-cell VGA are presented in Figure 6-9(a) and Figure 6-9(b), respectively. As illustrated in Figure 6-9(a), a gain variation range of 4 dB is achieved from a single body-tuned VGA cell. Moreover, the measured and simulated gain error of the single-cell VGA is shown Figure 6-9(b). The measured gain error is 0.08 dB, which is much larger than the simulated 0.015 dB. Such discrepancy between the simulation and measurement is mainly due to the limited equipment accuracy. A more reasonable comparison between simulation and measurement in terms of gain error will be indirectly presented based on 1/10



(a)



(b)

Figure 6-9 Gain characteristic of the single-cell body-tuned VGA

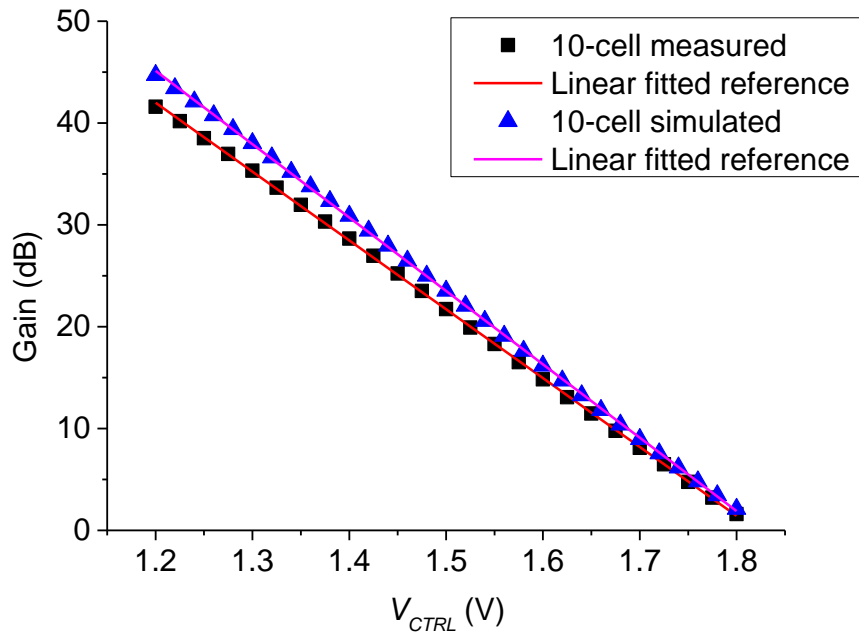
(a) dB-linear gain range (b) gain error

that of the 10-cell body-tuned VGA. The power consumption of the single-cell body-tuned VGA is only 41 μA under a 1.8 V power supply.

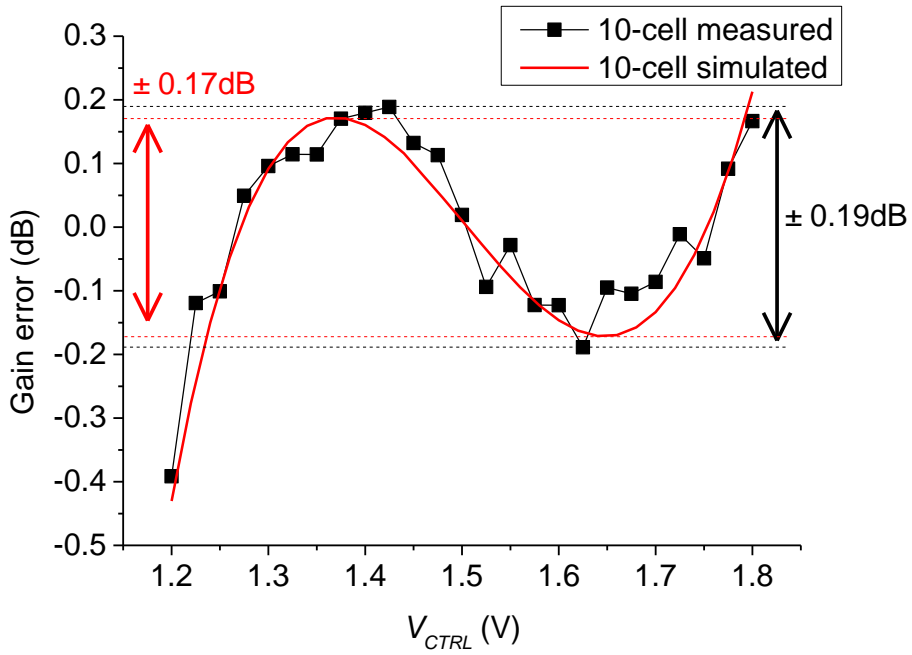
Figure 6-10(a) shows the measured and simulated gain characteristic of the 10-cell body-tuned VGA with AC coupling circuitry, and Figure 6-10(b) shows the measured and simulated gain error of it. A gain variation range of 38.6 dB is achieved while V_{CTRL} is swept from 1.225 V to 1.8 V. Within this gain variation range, the measured gain error is 0.19 dB (0.49% of gain variation range), which is reasonably close to the simulated value of 0.17 dB. The gain error of the single body-tuned VGA cell is thus derived as 0.019 dB, which is also close to the simulated result in Figure 6-9(b). The power consumption for this VGA core is 412 μA , which is as expected being 10 times that of the single cell.

Figure 6-11(a) shows the measured and simulated gain characteristic of the 15-cell reconfigurable VGA and Figure 6-11(b) shows the measured and simulated gain error of it. A maximum gain variation range of 63 dB is achieved while V_{CTRL} is swept from 1.2 V to 1.8 V. The measured gain error is 0.3 dB with the dB-linear gain range being 56 dB (0.54%) while V_{CTRL} is swept from 1.25 V to 1.775 V, which is also quite close to the simulated value of 0.26 dB. The power consumption for this VGA core is 620 μA at its highest gain setting, which is as expected being 15 times that of the single cell.

Figure 6-12 shows the measured gain error across digital bits when the designed 15-cell reconfigurable VGA is working as a tunable PGA. It can be seen that the gain error is slightly larger than the VGA configuration, being 0.4 dB. The power consumption for this PGA core is binary-weighted depending on the control bits, and is 1.1 mW at its highest gain setting.



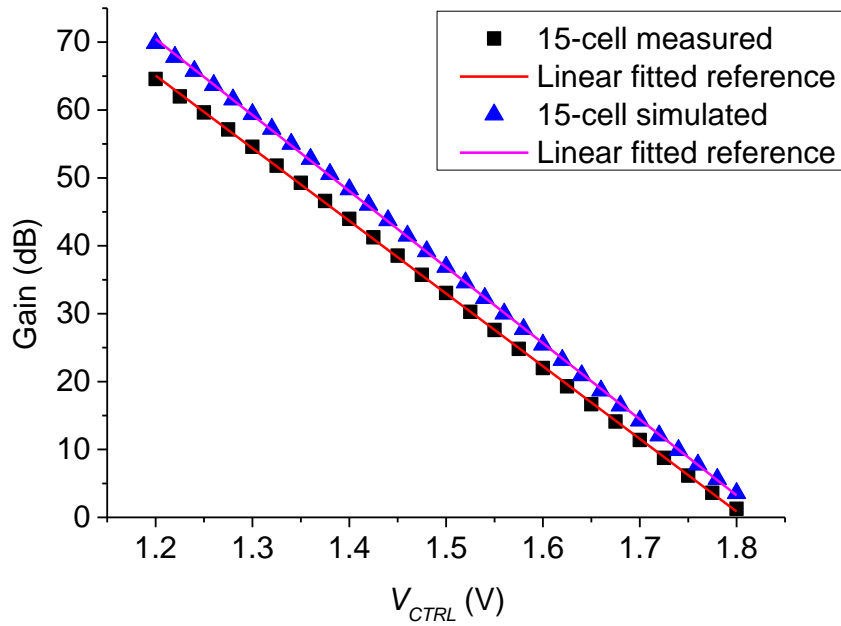
(a)



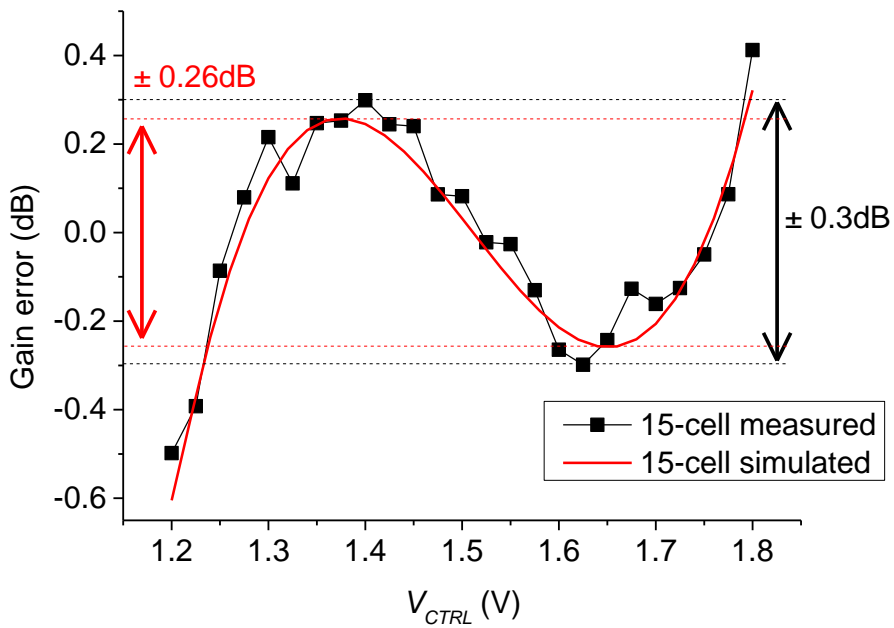
(b)

Figure 6-10 Gain characteristic of the 10-cell body-tuned VGA

(a) dB-linear gain range (b) gain error



(a)



(b)

Figure 6-11 Gain characteristic of the reconfigurable body-tuned VGA

(a) dB-linear gain range (b) gain error

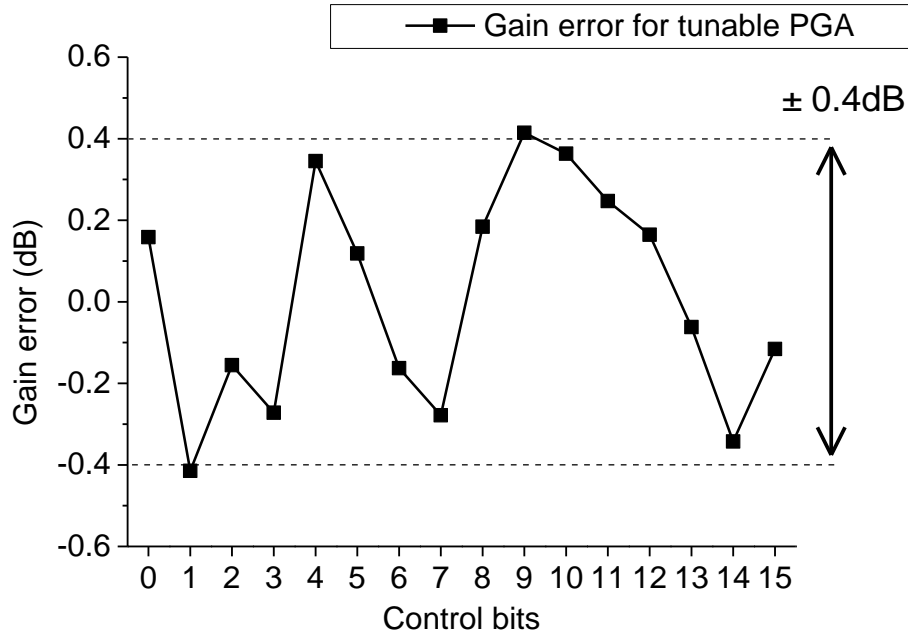


Figure 6-12 Measured gain error of the tunable body-tuned PGA

6.3.3 Frequency response

Figure 6-13, Figure 6-14 and Figure 6-15 show the measured frequency responses of the fabricated VGAs under various V_{CTRL} values, for single-cell, 10-cell and 15-cell body-tuned VGA, respectively. The impact of the parasitic capacitance on the frequency response of the designed VGA is negligible. The measured results are almost identical to the post layout simulation. As can be seen from the figures, the bandwidth for single-cell, 10-cell and 15-cell reconfigurable VGAs are 284 MHz, 149 MHz and 63.5 MHz, respectively, under the highest gain setting. It can be seen from Figure 6-13, Figure 6-14 and Figure 6-15 that the bandwidth of the VGA is reduced while more cells are cascaded. Due to the simple gain compensation structure, the bandwidth of the unit cell is relatively wide, thus the resultant bandwidth of the cascaded VGA is still reasonable for many applications. The simulated -3 dB low cut-off frequency as determined by the RC circuit in AC-coupling circuitry is 44 kHz,

which is below the measurable frequency of the VNA, thus it is not measured.

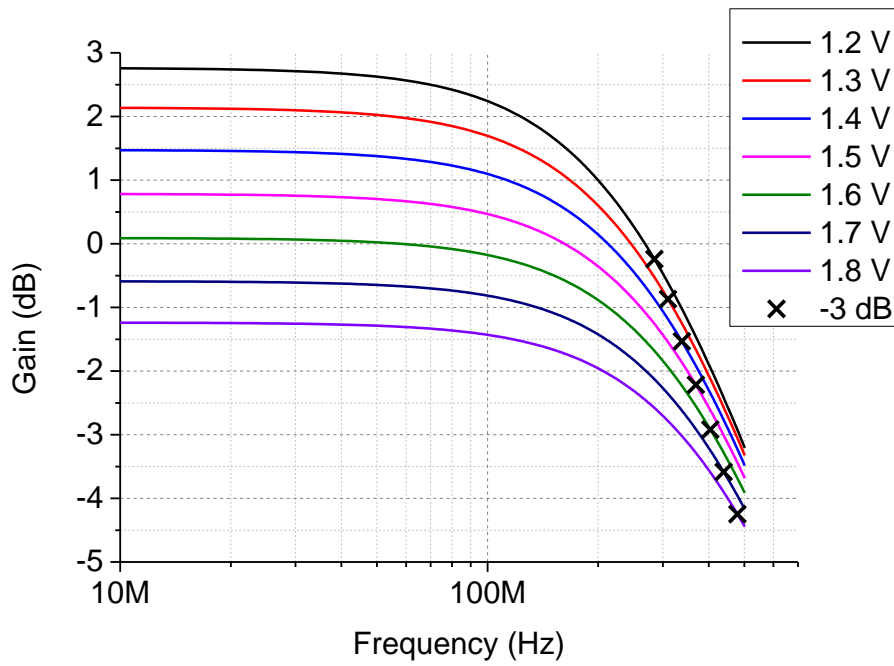


Figure 6-13 Measured frequency response of the single-cell body-tuned VGA

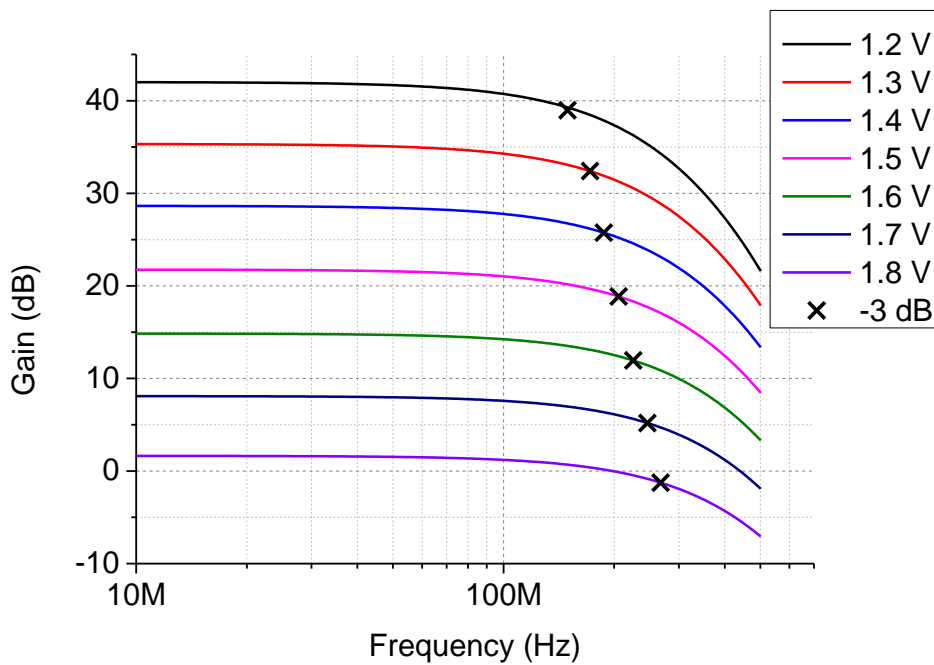


Figure 6-14 Measured frequency response of the 10-cell body-tuned VGA

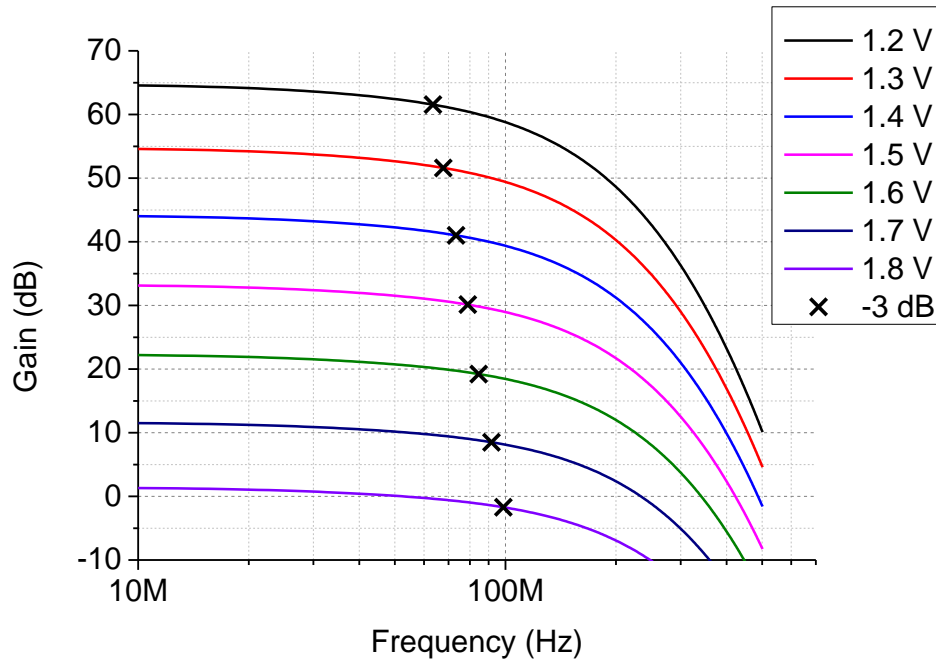


Figure 6-15 Measured frequency response of the reconfigurable body-tuned VGA

As discussed in Section 6.1.2, the mismatch of transistors should be taken into account to evaluate the DC offset issue. Therefore, the 10-cell body-tuned VGA without any AC coupling circuitry is also fabricated. It exhibits DC offset problem at high gain settings, and the voltage gain is dB-linear only for the V_{CTRL} between 1.8 V and 1.4 V.

To further evaluate the DC offset issue, the fabricated 5-cell VGA is also measured. The measurement result shows that the 5-cell body-tuned VGA can produce around 20 dB of gain variation range and no DC offset problem is observed. As each body-tuned VGA cell is directly connected to each other without having any AC-coupling circuitry, the core of 5-cell VGA only occupies an area of 0.0007 mm^2 ($23 \times 32 \text{ } \mu\text{m}^2$), which indicates that if smaller size is required, the AC-coupling circuitry can be inserted between every 5 cells. The gain error and power consumption of 5-cell body-tuned VGA are around half of that for the 10-cell

body-tuned VGA as the cascaded structure is the same.

6.3.4 Noise and linearity

The measured output P_{1dB} and IRN for the 10-cell body-tuned VGA is shown in Figure 6-16. The measured output P_{1dB} is around -3 dBm for the highest gain setting, while the IRN is around $10.6 \text{ nV}/\sqrt{\text{Hz}}$.

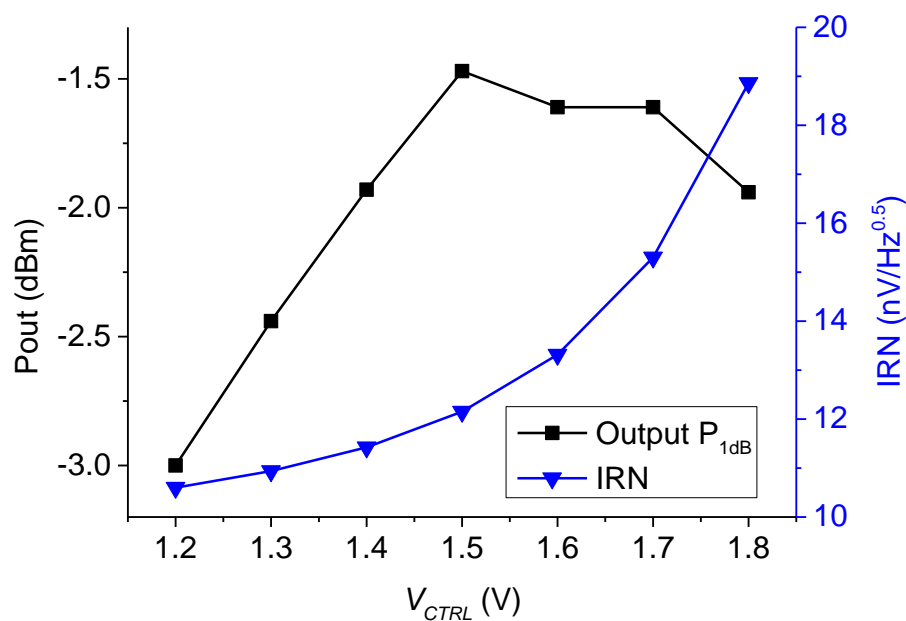
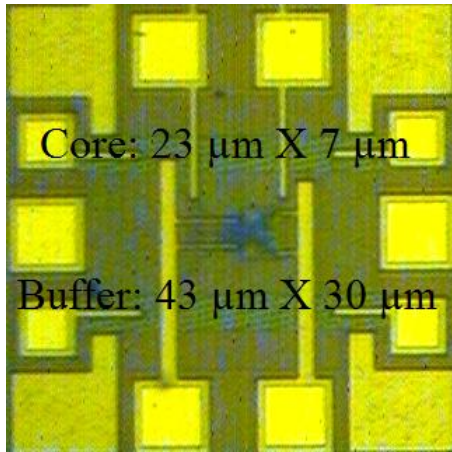


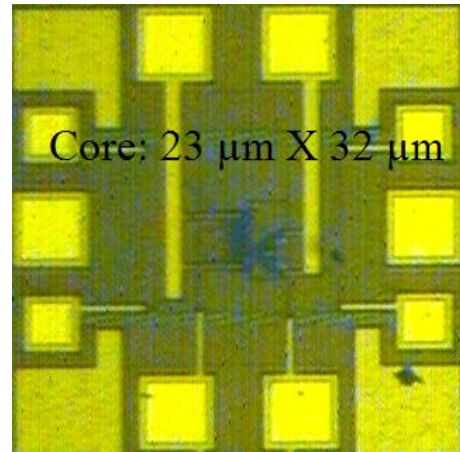
Figure 6-16 Measured output P_{1dB} and IRN vs. V_{CTRL} for the 10-cell body-tuned VGA

6.3.5 Die photo

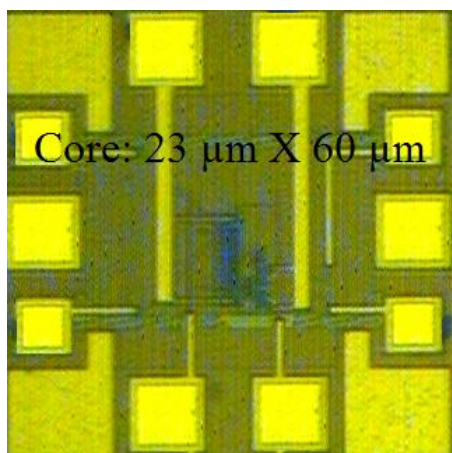
Figure 6-17 shows the die photos of the fabricated body-tuned VGAs. The designed body-tuned VGA cell is very compact with a die size of only $23 \mu\text{m} \times 7 \mu\text{m}$. The 5-cell and 10-cell directly cascaded body-tuned VGA occupies roughly 5 times and 10 times area of the single cell, being $23 \mu\text{m} \times 32 \mu\text{m}$ and $23 \mu\text{m} \times 60 \mu\text{m}$, respectively. Those VGAs are very compact and much smaller than other published VGAs. For AC-coupled 10-cell body-tuned



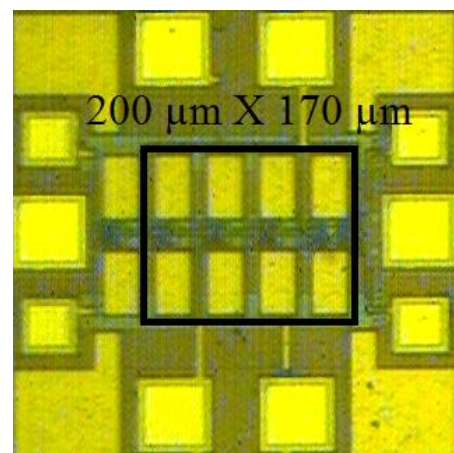
(a)



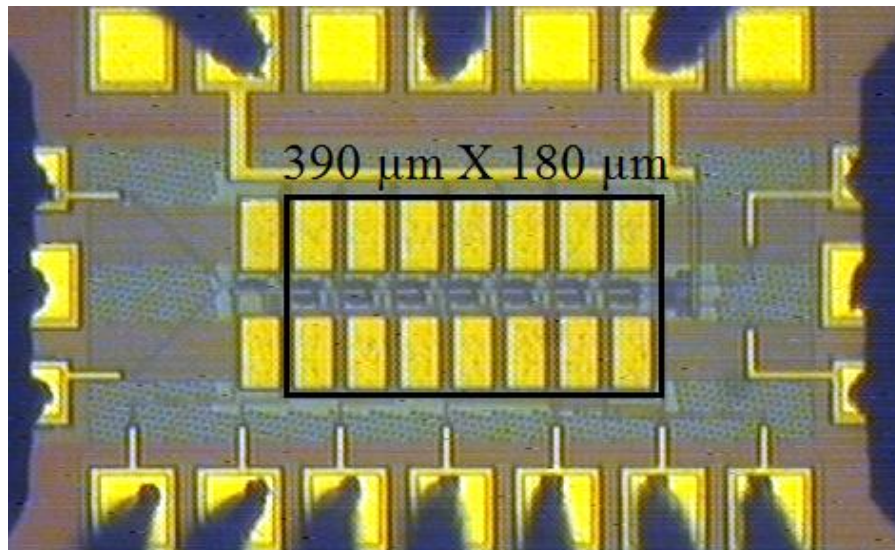
(b)



(c)



(d)



(e)

Figure 6-17 Die photos of the body-tuned VGAs: (a) single-cell, (b) 5-cell, (c) 10-cell with DC coupling, (d) 10-cell with AC coupling, (e) 15-cell reconfigurable

VGA, the main area-consuming block is the AC-coupling circuitry. With this, the size is $200 \mu\text{m} \times 170 \mu\text{m}$. Thus, even with the AC-coupling circuitry, the size is still comparable to other published VGAs. The reconfigurable VGA consumes an area of $390 \mu\text{m} \times 180 \mu\text{m}$, and again the main area-consuming block is the AC-coupling circuitry. Again, the area can be effectively reduced if a higher -3 dB low cut-off frequency is acceptable. The buffer used for all these VGAs is the same and the size is $43 \mu\text{m} \times 30 \mu\text{m}$.

6.4 Summary and comparison

A comparison between the proposed VGAs with other state-of-the-art designs is given in Table 6-1, while the comparison of the 15-cell reconfigurable VGA working as a PGA with other state-of-the-art PGA designs is given in Table 6-2.

In summary, a simple and robust cell-based method is presented for the design of VGAs with accurate dB-linear characteristic. The presented body-tuned VGA cell achieved extremely accurate dB-linear characteristic across a wide tuning range, based on a unique gain compensation method with a combination of sub-threshold n-MOS and body-tuned p-MOS transistors as active loads. Several such highly dB-linear body-tuned VGA cells can be cascaded to provide the required gain variation range for a VGA while achieving low power consumption and wide bandwidth. Re-configurability and power scalability are also demonstrated. Among the previously published works in the literature, the performance of the presented cell-based VGAs are very competitive in terms of gain error. Therefore, the presented cell-based designs may be suitable for many applications, where low power and high frequency are required.

Table 6-1 Performance summary and comparisons of the proposed body-tuned VGA with other state-of-the-art works

	[2] TMTT 2012	[4] TCAS-I 2006	[6] JSSC 2013	[7] JSSC 2009	[10] TCAS-II 2009	[26] TCAS-I 2014	This work 10-cell	This work 15-cell
Gain range (dB)	-16~32	-43~52	-13~63	-18~47	-21~21	-5.5~28	1.6~40.2	3.6~59.6
dB-lin. gain (dB)	48	95	50	40	42	34	38.6	56
V_{CTRL} range (V)	N/A	1	0.21	0.65	N/A	0.7	0.575	0.525
Gain error / Gain Step (dB)	6	1	0.5	0.8	1.31	N/A	0.19	0.3
BW (MHz)	60	32	14.8	40	60	60	149	63.5
Output P_{1dB} (dBm)	-2	-7	N/A	N/A	4	5.6	-3	-3
OIP3 (dBm)	N/A	N/A	11.5	22	10	13	8	8
IRN (nV/\sqrt{Hz})	N/A	N/A	3.5	11	N/A	11.4	10.6	10.6
Supply (V)	1	1.8	1.2	1.2	1.5	1.8	1.8	1.8
Power (mW)	1.2	6.48	2.16	1.44	3.2	7.56	0.74	1.12
Size (mm^2)	0.1	0.4	0.01	0.17	0.08	0.05	0.034	0.07
Technology (nm)	130	180	65	65	180	150	180	180

Table 6-2 Performance summary and comparisons of the proposed tunable PGA with other state-of-the-art works

	[2] MWCL 2010	[3] TMTT 2012	[26] TCAS-I 2014	PGA_L	PGA_H
Gain (dB)	-22~31	-16~32	-5~28	-8~2	-8~70
Gain step (dB)	1	6	4	0.67	5.2
BW (MHz)	65	60	60	99	64
Output P _{1dB} (dBm)	5.6	-3	5.6	-1.9	-3
IRN (nV/ $\sqrt{\text{Hz}}$)	11.4	N/A	11.4	19	10.6
Supply (V)	1.8	1	1.8	1.8	1.8
Power (mW)	2.2	1.2	7.6	1.1	1.1
Size (mm ²)	0.39	0.1	0.05	0.07	0.07
Tech. (nm)	180	130	150	180	180

Chapter 7

High-frequency VGA in 65 nm CMOS

7.1 Choice of device length for a robust design

Unlike the 90nm CMOS devices used in [47], the threshold voltage of the low V_T device is only 0.25 V. In this design, the Globalfoundries' 65 nm CMOS technology is adopted. The threshold voltage V_{TH} is relatively high, even low V_T device is adopted. Moreover, as can be seen in Figure 4-16, the n-MOS transistors are used as loads, which further increase the threshold voltage of the device due to body effect. Thus, the length of device needs to be carefully selected rather than simply choosing the minimum length [47]. However, using the minimum length of the device could minimize the power consumption as well as maximize the bandwidth due to the reduced parasitic capacitance. Therefore, there are trade-offs between low voltage, low power, wide bandwidth and robustness. Moreover, as lithographic limits are being pushed to keep pace with Moore's law, the associated statistical variations of circuit relevant parameters within the transistors are increasing. These process corners, such as threshold voltage variations, fail to adequately represent the effect of process variations on the circuits. Therefore, the relationship between the device length and the variation of threshold voltage also needs to be investigated so that a robust design can be achieved.

The simulated V_{TH} and V_{TH} variation for three V_{SB} values of 0 V, 0.25 V and 0.7 V, which is the DC condition for transistor M_3 , $M_{1,2}$ and M_{4-7} in the high-frequency VGA cell, is shown in Figure 7-1. It can be seen from Figure 7-1(a) to Figure 7-1(c) that V_{TH} reduces with increasing length of device. In addition, as shown in Figure 7-1(d), the minimum variation of V_{TH} across the process variations is appeared for the device's length of 120 nm. Therefore, there is another trade-off between the threshold voltage and its variation across different processes. In this design, the device's length of 150 nm is selected as a compromise of low V_{TH} and small V_{TH} variation.

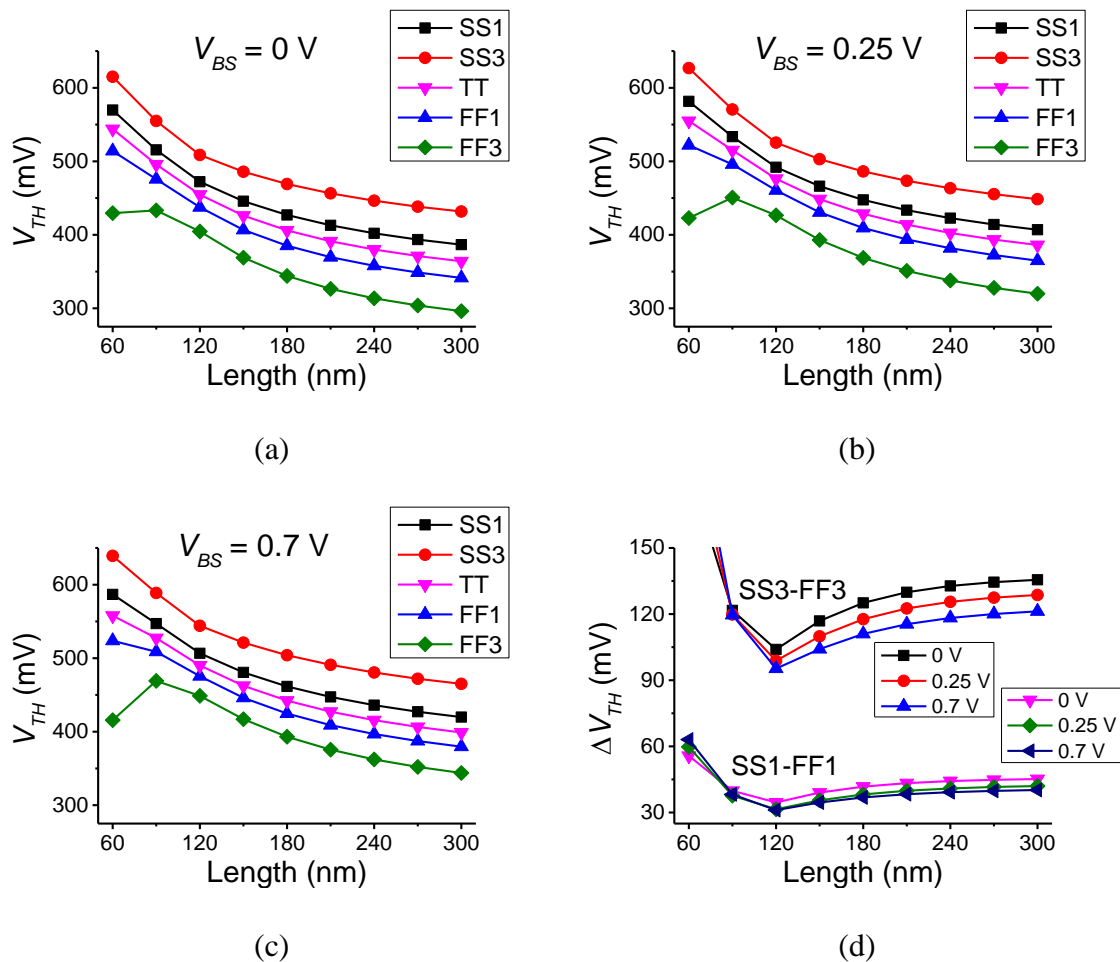


Figure 7-1 The V_{TH} of various device length with (a) $V_{SB} = 0$ V (b) $V_{SB} = 0.25$ V (c) $V_{SB} = 0.7$ V (d) V_{TH} variation across all corners

7.2 Overall VGA architecture

As mentioned above, the simulated bandwidth for a single high frequency cell is 8 GHz. As calculated from Table 3-1 for $BW_c = 8$ GHz, the maximum number of cascaded cells to guarantee a 2 GHz bandwidth with a reasonable gain variation range is 11. The block diagram of the proposed 11-cell VGA is depicted in Figure 7-2. As shown in Figure 7-2, cell₁ refers to the unit cell discussed in Section 4.3.1. The other cell, cell₂ is the modified version of the unit cell that is used for DC offset cancellation. FB is the DC offset cancellation feedback circuit. The gain of the VGA is directly controlled by the voltage V_{CTRL} . The required control voltages, V_{CN} and V_{CP} , are automatically generated by the control voltage generator circuit. To further boost the gain, the VGA is followed by a fixed gain amplifier as well as a buffer for the purpose of measurement.

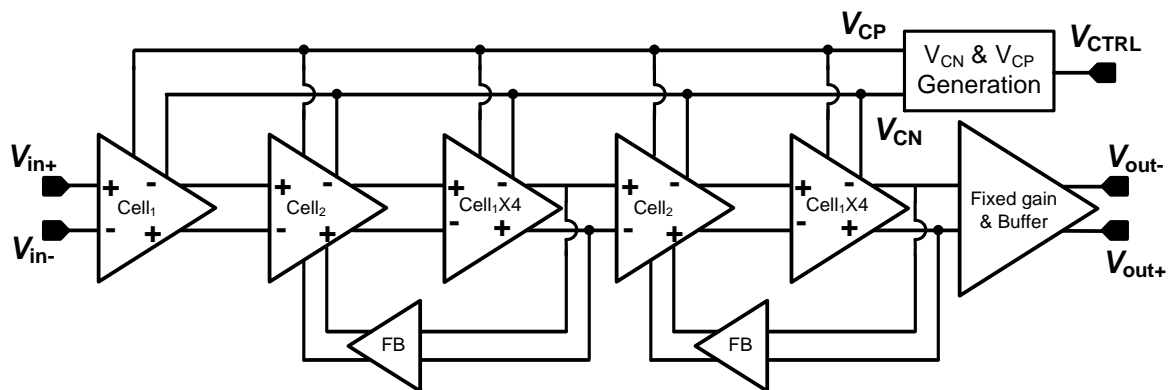


Figure 7-2 Overall block diagram of proposed high-frequency VGA

7.3 Other key building blocks

7.3.1 DC offset cancellation circuit

To stabilize the DC condition, two feedback loops are used for DC offset cancellation [47, 53]. As shown in Figure 7-2, the feedback loop consists of a cell₂ and a feedback cell, FB. The schematic of cell₂ is shown in Figure 7-3(a). In this cell, the main amplifying transistor pair is evenly divided into two parts, $M_{1a/2a}$ and $M_{1b/2b}$ while the DC conditions are kept same as cell₁. $M_{1a/2a}$ is for the signal input and $M_{1b/2b}$ is for the DC offset feedback input.

The schematic of FB is shown in Figure 7-3(b). The input RC low pass filter is realized by two cascaded p-MOS transistors in series serving as resistor, and one n-MOS transistor serving as capacitor. In this way, large resistance and capacitance can be realized with very small area. The simulated -3 dB cut-off frequency is around 400 kHz.

7.3.2 Control voltage generator

The schematic of the control voltage generation circuit is depicted in Figure 7-4. Due to the limited range of V_{CN} (around 200 mV), it is scaled up to the real input control voltage V_{CTRL} which is full swing, for easier and more accurate tuning and measurement. The relationship between V_{CN} and V_{CTRL} in this case can be expressed as:

$$V_{CN} = \frac{3}{4}V_{DD} + \frac{1}{4}V_{CTRL}. \quad (7-1)$$

As discussed in Section 4.3.2, a dynamically controlled V_{CP} is required for better compensation of the varied location of pole so that the gain ripple variation can be minimized. To achieve this goal, a source follower is adopted to generate the control voltage V_{CP} .

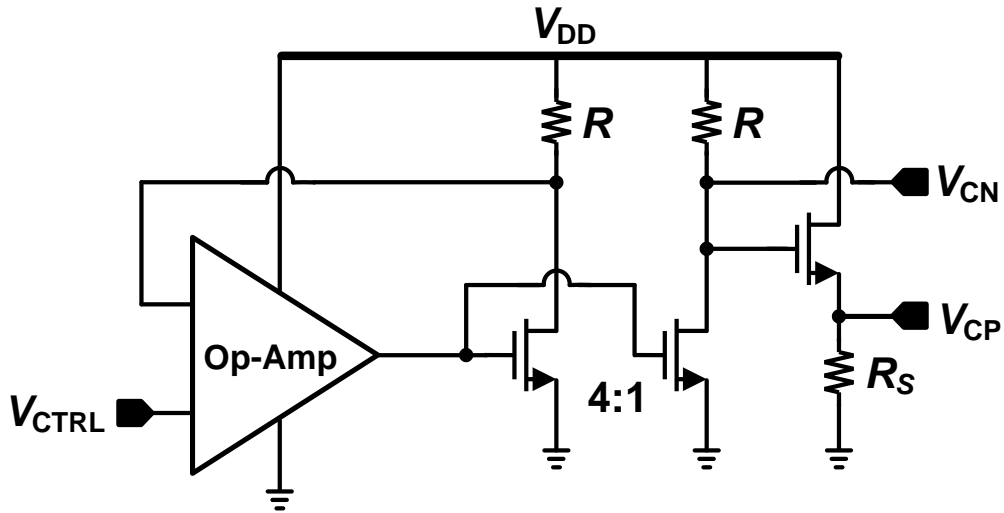


Figure 7-4 Control generation circuit

7.3.3 Fixed gain amplifier and buffer

The schematics of the fixed gain amplifier and the buffer are shown in Figure 7-5. This amplifier provides a fixed gain of 10.5 dB to the circuit to compensate the buffer loss, so that the resultant lowest gain can be boosted from -10.5 to 0 dB.

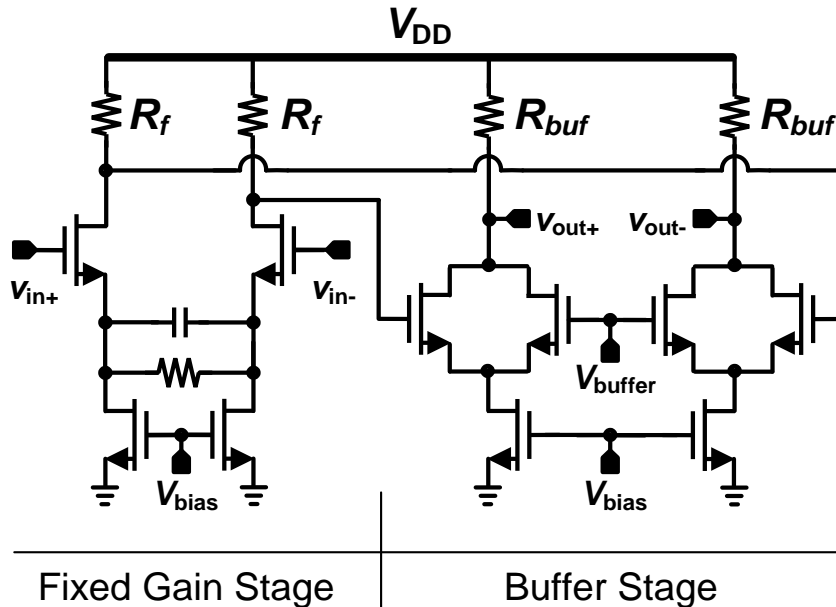


Figure 7-5 Fixed gain amplifier and buffer

Although this amplifier is mainly used to boost the overall gain of the VGA, it can be enabled in bypass mode so that the overall gain variation range can be increased by another 10.5 dB. In addition, this amplifier can be added at the front to achieve better noise performance, as well as at the back to alleviate the linearity requirement of other cells as in this work.

Finally, a differential buffer is designed and added as the last stage to drive the 50Ω load in measurement. The buffer is simulated having a loss of 10.8 dB at all frequencies.

7.4 Monte Carlo simulation

To demonstrate the robustness of the designed VGA, the Monte Carlo simulation is adopted. The simulated gain characteristic of designed VGA with Monte Carlo simulation results of 100 runs is shown in Figure 7-6. The designed VGA is robust enough against process variation as well as device mismatch. This is mainly due to the following reasons. First of all, existence of DC offset cancellation circuit can minimize the effects caused by device mismatch. Secondly, as demonstrated in Section 7.1, the proper selection of device size helps to minimize the variation of threshold voltage. Finally, the designed unit cell is almost constructed as an all n-MOS design, with p-MOS transistors only serving as variable resistors [10]. The variation in gain at highest gain setting and lowest gain setting are 6.8 dB and 4 dB, respectively.

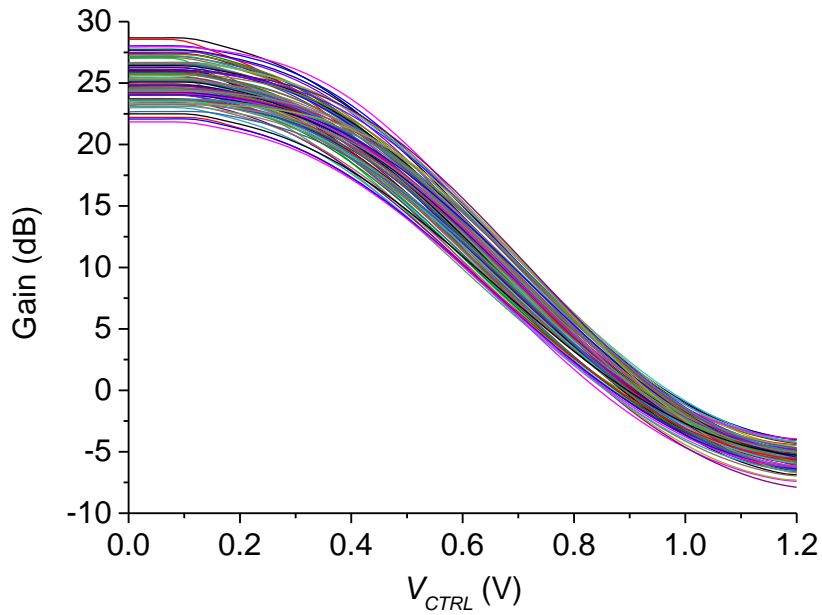


Figure 7-6 Monte Carlo simulation result of 100 runs

7.5 Implementation and measurement

To verify the proposed structure, the high-frequency VGA shown in Figure 7-2 is fabricated in Globalfoundries' 65 nm CMOS technology. Input matching is simply achieved through a shunt 50Ω resistor. As mentioned above, a differential buffer is included after the VGA and is fabricated separately for de-embedding purpose. The on-wafer measurement is performed using an Agilent E8364B VNA, which operates from 10 MHz to 50 GHz. The buffer was measured to have 10.8 dB of attenuation at all frequency. Moreover, a fixed 1 GHz signal is used for all of the dB-linear gain characterization, output P_{1dB} and NF measurements.

The measured gain characteristic of the high-frequency VGA is presented in Figure 7-7. As illustrated in Figure 7-7, a gain variation range of 24.3/24.0/23.4/22.8 dB is achieved

at 0.5/1/1.5/2 GHz, respectively, for V_{CTRL} from 0.2 to 1 V. Although the exact gain value is slightly different, the dB-linear gain range is almost the same, which is around 17.3 dB and is for V_{CTRL} from 0.3 to 0.8 V. This is in accordance to the simulated results in Figure 4-18(a) and the dynamic compensation to achieve constant gain variation range is demonstrated.

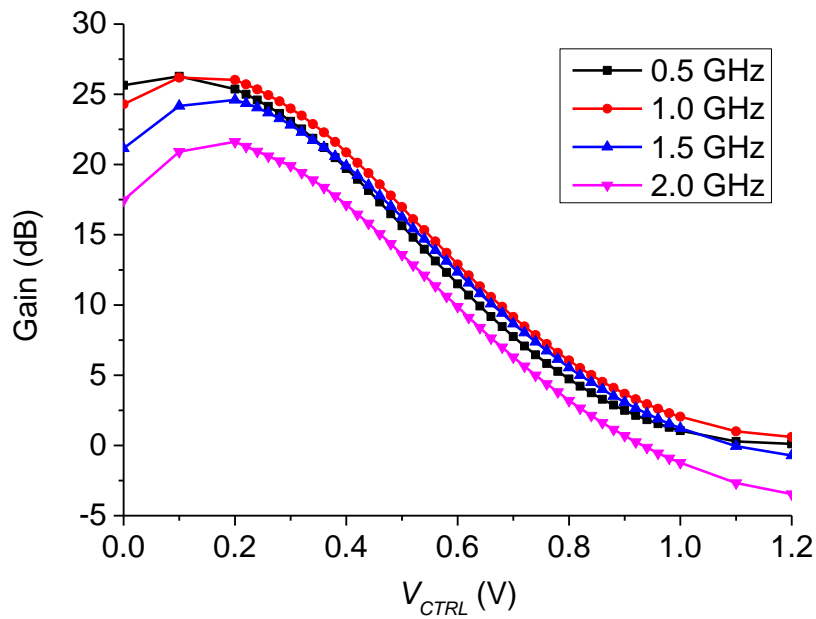


Figure 7-7 Measured gain characteristic of the high-frequency VGA at 0.5/1/1.5/2 GHz

Moreover, the measured gain error of the high-frequency VGA can be seen from Figure 7-8. The measured gain error is less than 0.3 dB for all the four frequency points. The DC current of the high-frequency VGA core is only 2.9 mA, and the current of the buffer is 5.4 mA, both under a 1.2 V power supply.

Figure 7-9 shows the measured frequency responses of the high-frequency VGA. As can be seen from Figure 7-9, the minimum and maximum bandwidth for the high-frequency VGA is from 2.03 GHz to 2.23 GHz, with only 200 MHz bandwidth variation. The gain flatness is within 1 dB. Due to the gate peaking technique and dynamic gain ripple

compensation, the bandwidth of the high-frequency VGA is wide and constant. The simulated -3 dB low cut-off frequency as determined by the DC offset cancellation circuit is 440 kHz, which is below the measurable frequency of the VNA, thus it is not measured.

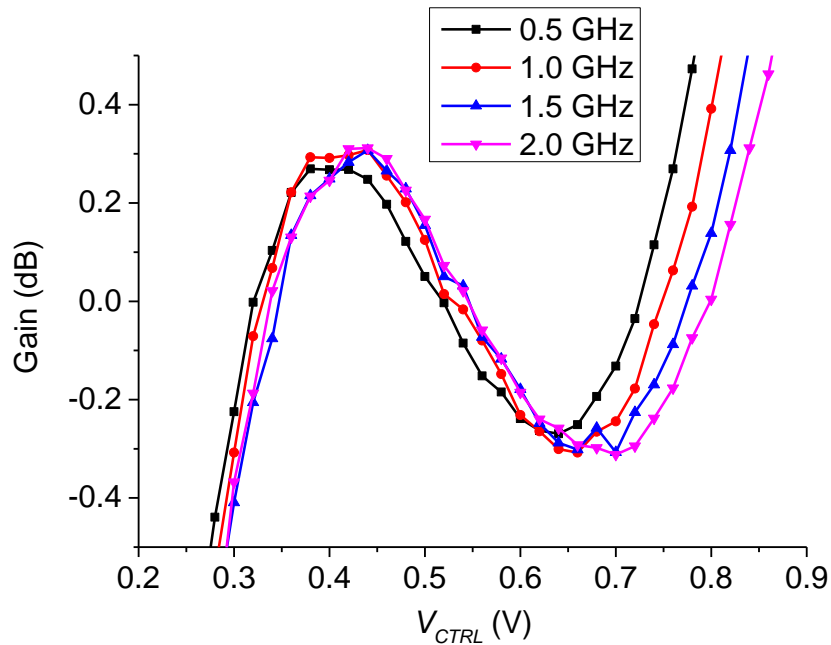


Figure 7-8 Measured gain error of the high-frequency VGA at 0.5/1.5/2 GHz

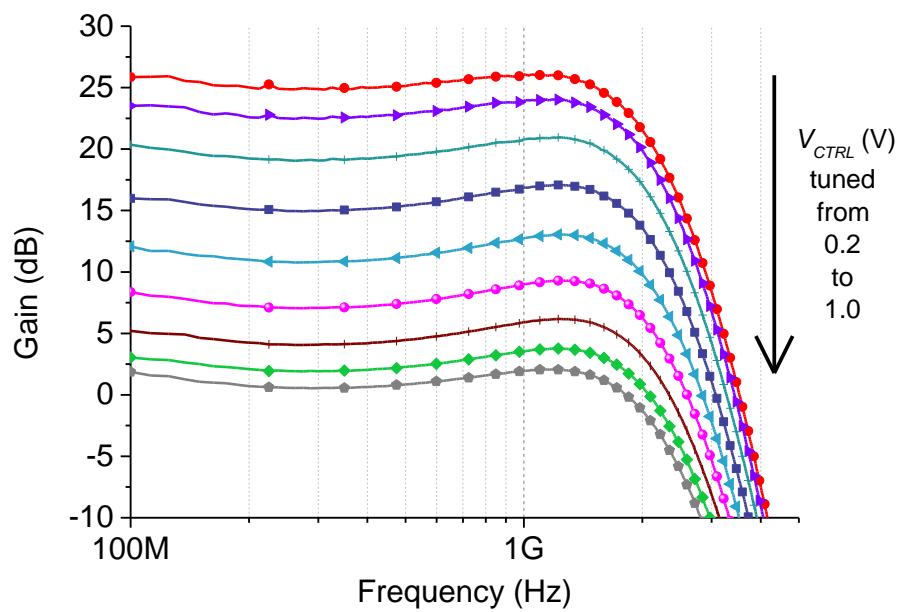


Figure 7-9 Measured frequency response of the high-frequency VGA

The measured output P_{1dB} and noise figure for the VGA is shown in Figure 7-10. The measured output P_{1dB} is from 1.8 to -4 dBm and the NF is from 24 to 29 dB, while the VGA is tuned from the highest gain setting to the lowest.

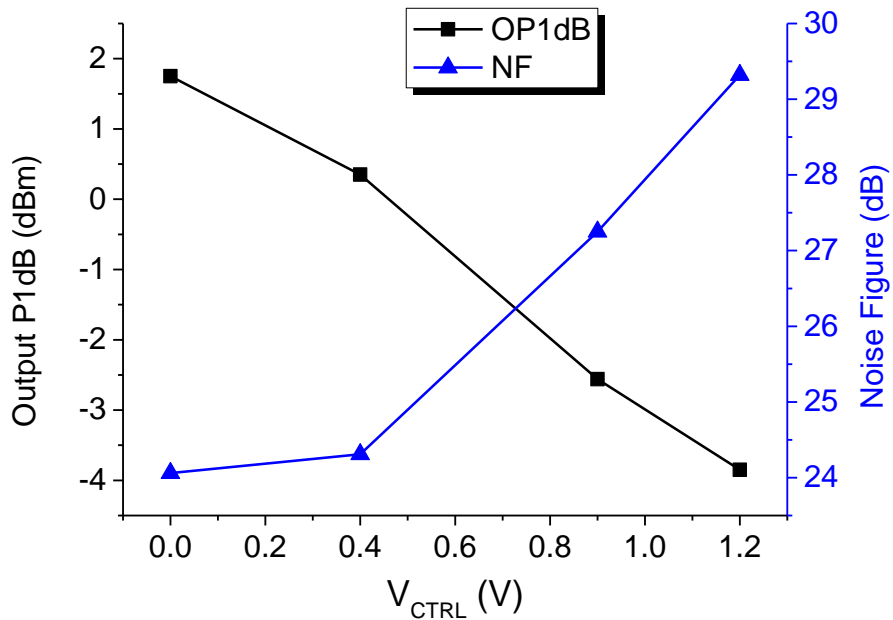


Figure 7-10 Measured output P_{1dB} and NF of the high-frequency VGA

Figure 7-11 shows the die photos of the fabricated high-frequency VGA. The 11-cell high-frequency VGA is very compact and the size with pads excluded is only $225 \mu\text{m} \times 45 \mu\text{m}$, with the size of the output buffer being $50 \mu\text{m} \times 30 \mu\text{m}$. In this case, the DC offset cancellation circuit is not the main area-consuming block, and the size is difficult to reduce in a similar way to the previously discussed VGAs.

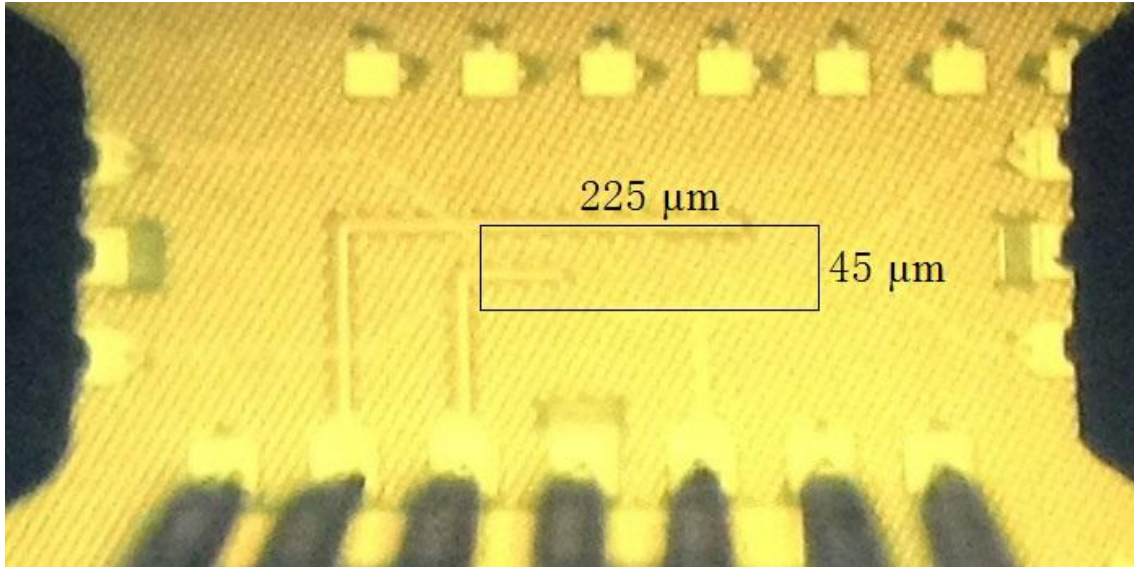


Figure 7-11 Die photo of the fabricated high-frequency VGA

7.6 Performance summary

The performance summary of the high-frequency VGA is given in Table 7-1. For fair comparisons, the high-frequency VGA is only compared with other state-of-the-art designs that also designed in CMOS technology and targeted for 60 GHz application. In [28-30], the designed VGAs are all digitally controlled. To achieve a fine gain resolution of approximately 1 dB, all of them require at least 5 bits of digital control codes. In contrast, our designed analog controlled high-frequency VGA can achieve a fine gain resolution of approximately 0.3 dB. Since channel selection filter is not included in our presented work, it is difficult to provide an apple to apple comparison in terms of power consumption. The 3.5 mW overall power consumption of the high-frequency VGA leaves a reasonable power budget for the design of low power channel selection filter [52]. Although an analog controlled VGA in [47] has greater gain variation range and less power consumption than our presented work, that VGA does not have accurate dB-linear characteristic, which is the most

critical requirement for the analog controlled VGA design. Moreover, we intentionally leave enough design margins while demonstrating the robustness of the high-frequency VGA, which is not previously presented in [43-45, 34].

Table 7-1 Performance summary and comparisons of the proposed high-frequency VGA with other state-of-the-art works

	[28] RFIC 2012	[29] RFIC 2011	[30] ESSCIRC 2010	[47] TCAS-I 2012	This work
Gain range (dB)	11 ~ 30	0 ~ 19.6	4 ~ 33	-10 ~ 50	2 ~ 24
Gain step (dB)	0.8	1	1	N/A	N/A
Gain error (dB)	N/A	N/A	N/A	N/A	±0.3
BW (GHz)	0.97 ~ 1	0.865 ~ 0.915	0.9	2.2	2.0 ~ 2.2
Output P _{1dB} (dBm)	1.4	-5	-1	-5	-1
Noise	4.2 mV (rms) Output	-145 dBm/Hz Input	-160 dBm/Hz Input	17 ~ 30 dB NF	24 ~ 29 dB NF
Supply (V)	1.1	1	1.2	1	1.2
Current* (mA)	N/A	N/A	N/A	2.5	2.9
Size (mm ²)	N/A	N/A	N/A	0.014	0.01
Technology (nm)	40	90	65	90	65

In summary, design of a robust wideband inductorless high-frequency VGA with accurate gain adjustment for 60 GHz application is presented. To justify the trade-off between gain and bandwidth, the system level analysis of gain and bandwidth requirements for VGA cell is given. Based on the analysis, a simple but robust high-frequency VGA cell is presented. This high-frequency VGA cell adopts a unique gain control method, which can accurately adjust the gain of the VGA without compromising any other performance. Moreover, the gate peaking technique is also adopted to extend the bandwidth without using any on-chip spiral inductors. Therefore, the presented high-frequency VGA can be used for analog baseband processing of 60 GHz application as well as many other applications that require low power consumption and wide bandwidth.

Chapter 8

Conclusion and future works

8.1 Conclusion

The design of VGA in CMOS technology is presented in this work. Motivations and literature reviews of various VGA designs are presented in the first two chapters.

In Chapter 3, a new design approach which is the “cell-based” design method is proposed. The advantage of cell-based VGA design is that the number of unit cells to be cascaded can be chosen according to the system requirements. Moreover, a reconfigurable approach, by means of a digital control, can be implemented based on the unit cell to realize re-configurability and power scalability. As a result, multiple application standards can be satisfied with options for wide gain variation range, small gain error or low power consumption.

In Chapter 4, the proposed VGA cells based on the cell-based design method are presented. Depending on how the control signal is applied, a gate-tuned VGA cell and a body-tuned VGA cell are proposed for general purpose VGA, while a high-frequency VGA cell is proposed for high-frequency VGA. Detailed analysis of the gate peaking technique shows that it can effectively extend the bandwidth. This technique is combined with the gate-tuned VGA cell, so that it can be turned into high-frequency VGA cells.

In Chapter 5, the 5-cell gate-tuned general purpose VGA is implemented in 0.18 μm CMOS technology. Measurement results show that the general purpose VGA is accurate and wideband, with ultra-low power consumption and small area. A gain variation range of 71 dB is measured, among which 45 dB is dB-linear with less than 1 dB gain error. The power consumption is only 81 μA under a 1.8 V power supply. The bandwidth is varied from 50 MHz to 209 MHz from the highest to the lowest gain. The output $P_{1\text{dB}}$ is around 0 dBm, while the minimum IRN is $7.5 \text{ nV}/\sqrt{\text{Hz}}$ at the highest gain setting. The die is $200 \mu\text{m} \times 170 \mu\text{m}$. Therefore, the presented gate-tuned VGA is suitable for many applications, where ultra-low power, high frequency and accurate dB-linear characteristic are required.

In Chapter 6, single-cell, 10-cell and 15-cell reconfigurable body-tuned general purpose VGAs are implemented in 0.18 μm CMOS technology. AC-coupled 10-cell body-tuned VGA and 15-cell reconfigurable body-tuned VGA are also fabricated. Measurement results show that the body-tuned general purpose VGA achieved extremely accurate dB-linear characteristic across a wide tuning range, with low power consumption and wide bandwidth. A gain variation range of 4 dB, 38.6 dB and 63 dB with gain error of 0.019 dB, 0.19 dB and 0.3 dB is achieved, respectively. When the 15-cell reconfigurable VGA is working as tunable PGA, the gain error across digital control bits is 0.4 dB. The power consumptions are only 41 μA , 410 μA and 620 μA under a 1.8 V power supply, respectively. The bandwidth are 284 MHz, 149 MHz and 63.5 MHz, respectively, under the highest gain setting. The measured output $P_{1\text{dB}}$ is around -3 dBm for the highest gain setting, while the IRN is around $10.6 \text{ nV}/\sqrt{\text{Hz}}$. The die area are $23 \mu\text{m} \times 7 \mu\text{m}$, $200 \mu\text{m} \times 170 \mu\text{m}$ and $390 \mu\text{m} \times 180 \mu\text{m}$, respectively. Therefore, the presented body-tuned VGA design may be suitable for many applications, where high accuracy, low power and high frequency are required.

In Chapter 7, the high-frequency VGA is implemented in 65 nm CMOS technology. Measurement results show that the VGA achieved accurate dB-linear characteristic with very wide bandwidth. A gain variation range of 24.3/24.0/23.4/22.8 dB is achieved at 0.5/1/1.5/2 GHz, respectively, for V_{CTRL} from 0.2 to 1 V. The dB-linear gain range is constant as 17.3 dB for V_{CTRL} from 0.3 to 0.8 V. The measured gain error is less than 0.3 dB for all the four frequency points. The DC current is only 2.9 mA, and the current of the buffer is 5.4 mA, both under a 1.2 V power supply. The minimum and maximum bandwidth is from 2.03 GHz to 2.23 GHz, with only 200 MHz bandwidth variation. The gain flatness is within 1 dB. Due to the gate peaking technique and dynamic gain ripple compensation, the bandwidth of the high-frequency VGA is wide and constant. The measured output P_{1dB} is from 1.8 to -4 dBm and the NF is from 24 to 29 dB from the highest gain setting to the lowest. The die area is only $225 \mu\text{m} \times 45 \mu\text{m}$, with the size of the output buffer being $50 \mu\text{m} \times 30 \mu\text{m}$. Therefore, the presented high-frequency VGA design may be suitable for high frequency applications, like the 60 GHz communication system.

8.2 Future works

Based on the proposed cell-based design method and the designed VGAs, several possible future works can be considered.

Firstly, the power consumption of the proposed VGA cells should be reduced, as well as higher bandwidth should be realized. By achieving this, more cells could be cascaded in a chain, and stronger re-configurability, power scalability and versatility may be possible. One possible way is to reduce the supply voltage, which will effectively reduce the power consumption of the whole VGA.

Secondly, other VGA cells could possibly be designed, with wider bandwidth and better accuracy. As shown in (4-2), in this work, only the denominator is varied, but not the numerator. Intuitively, the numerator can also be varied, by modifying the input differential pair. The same control method could still be applied. When the correct operation region is guaranteed, the resultant gain of the VGA cell should behave like the cells presented in this work. Possible combination or compensation may also be achieved by simultaneously varying the input differential pair and the load.

Thirdly, as in all of our proposed VGAs, the most area consuming block is either the AC-coupling circuitry or the DC offset cancellation circuit. The die area could be effectively reduced if smaller capacitors and resistors are used. This could be achieved with a better and more effective DC offset cancellation circuit, such that the size can be shrunk without sacrificing the -3 dB low cut-off frequency.

Finally, with the excellent dB-linear performance of the proposed VGAs, high performance AGCs should be designed based on these, and the performance of the AGC can be expected to be good. Other types of PGAs could also be designed based on the proposed cells to satisfy different application requirements. The vision is that a VGA or AGC could re-configure itself either for general purpose low frequency applications with small power consumption and better accuracy or for high frequency applications with sufficient bandwidth.

RELATED PUBLICATIONS

- (1) **H. Liu**, X. Zhu, C. C. Boon and X. F. He, "Cell-based variable-gain amplifiers with accurate dB-linear characteristic in CMOS 0.18 μm technology," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 586-596, Feb, 2015.
- (2) **H. Liu**, X. Zhu, and C. C. Boon, "A 71 dB 150 μW variable-gain amplifier in 0.18 μm CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, available online.
- (3) **H. Liu**, C. C. Boon and X. Zhu, "A reconfigurable programmable-gain amplifier with gain step adjustment and binary-weighted power consumption," *Int. Microw. Symp.*, Phoenix, AZ, May, 2015
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- (5) **H. Liu**, X. Zhu, C. C. Boon, and X. Yi, "Design of an oscillator with low phase noise and medium output power in a 0.25 μm GaN-on-SiC HEMT technology," *IET Microwaves, Antennas and Propagation*, available online.
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