

# A Fixed-frequency Hysteretic Controlled Buck DC-DC Converter with Improved Load Regulation

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**Abstract**— Hysteretic control is widely adopted in the power management units (PMUs) for modern electronic devices due to their simple and stable control architecture, as well as the fast load transient response. However, the switching frequency of a traditional hysteretic converter is not fixed. It changes with operating condition and component aging, and hence brings in electro-magnetic interference (EMI) problems and multiphase interleaving difficulties. In this work, a hysteretic buck converter with frequency-locking capability is presented, where the switching frequency is adjusted by tuning the hysteretic window. In addition, the current-mode hysteretic control in this work utilizes a simple feedback network, which consists of only passive components and yet provides significant improvement on output voltage regulation. To achieve good reliability at high temperature and high voltage, the proposed buck converter has been fabricated in a 1 $\mu\text{m}$  SOI process with a chip area of 6mm<sup>2</sup>. Experimental results measured at 1MHz fixed switching frequency with 12V-to-5V voltage conversion and 0.9A load current shows a peak efficiency of 91%.

**Keywords**—DC-DC converter; Fixed-frequency; Hysteretic control

## I. NOMENCLATURE

List of Signals		List of Components	
$V_{IN}$	Input voltage	$L$	Filtering inductor
$V_{OUT}$	Output voltage	$r_L$	ESR of $L$
$V_X$	Switching node voltage	$C$	Filtering capacitor
$f_{sw}$	Switching frequency	$r_C$	ESR of $C$
$D$	Duty signal	$R$	Load resistor
$V_{REF}$	Reference voltage	$R_{fb}$	Feedback resistor
$CLK_{REF}$	Reference clock	$C_{fb}$	Feedback capacitor
$V_H$	Hysteretic window		

## II. INTRODUCTION

The voltage regulator module (VRM) for modern high performance microprocessors must be capable of providing large output current (approaching 150A) with fast transient speed (upto 50A/ $\mu\text{s}$ ) while performing dynamic voltage scaling (DVS) at the same time [1]. The increased dynamic range (for both current and voltage) makes the VRM design more challenging as it requires a high speed controller to maintain or shorten the transient time.

For stability reason, a VRM designed and operated according to the linear control theory [e.g., pulse width

modulation (PWM)] normally has to limit its bandwidth at 20%~30% of the switching frequency [2]. Thus for VRMs targeting fast transient response, an extremely high switching frequency is required. Although this will help to reduce the inductor and capacitor sizes, it results in low efficiency due to the extra switching loss. On the other hand, if a VRM is operated with nonlinear control method (e.g., hysteretic control), the transient response is no longer limited by its switching frequency. Instead of responding to load transient after a few switching cycles in PWM control, the hysteretic control can provide nearly instantaneous response, and therefore the switching frequency of a VRM can be reduced while still maintaining fast transient speed.

Fig. 1 shows two typical control structures for traditional hysteretic VRM: the voltage-mode hysteretic control (VMHC) and current-mode hysteretic control (CMHC), where the inductor current information is excluded from or included in the feedback signals respectively. In both cases, a hysteretic comparator with window  $V_H$  is used. The switching frequencies under continuous conduction mode (CCM) can be derived as

$$f_{sw(VMHC)} = \frac{V_{OUT}(V_{IN} - V_{OUT})r_C}{LV_H V_{IN}} \quad (1)$$

$$f_{sw(CMHC)} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{R_{fb} C_{fb} V_{IN} V_H} \quad (2)$$

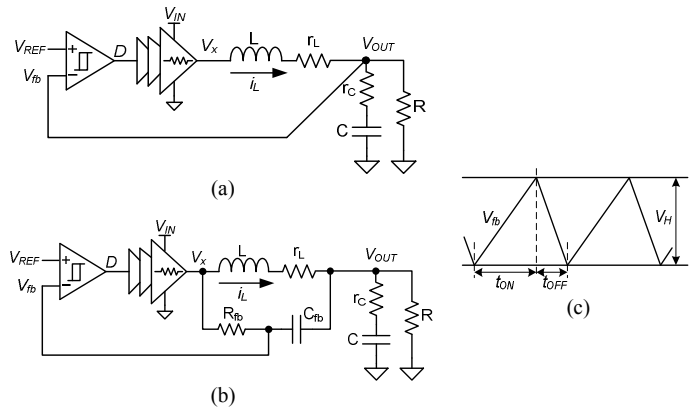


Fig. 1. Typical hysteretic buck converters: (a) with VMHC structure, (b) with CMHC structure, and (c) CCM operation waveform of the feedback signal oscillating within the hysteresis window for converters under VMHC with significant  $r_C$  or under CMHC.

These equations show a drawback of the traditional hysteretic control: the frequency is a variable depending on hysteretic window, converter input/output voltages and component values. This brings in potential electro-magnetic interference (EMI) failure for noise-sensitive systems (e.g., RF transceiver) and phase interleaving problem for high current multiphase designs (e.g., VRM for microprocessor). Therefore, fixed-frequency hysteretic control becomes more attractive, which can be briefly classified into four categories:

1) *Frequency locking by adjusting the on/off duty period in the fixed-on-time or fixed-off-time control schemes [3-5]*

- Pros: simple frequency controller.
- Cons: tradeoff between voltage regulation and frequency locking range.

2) *Frequency locking by adding in an adjustable delay [3], [6]*

- Pros: very simple frequency controller.
- Cons: tradeoff between voltage regulation and frequency locking range.

3) *Frequency locking by adjusting hysteretic window [7-9]*

- Pros: implementation through discrete components is possible.
- Cons: complicated controller (large silicon area and power consumption), bad voltage regulation, narrow frequency locking range.

4) *Frequency locking by injecting periodic synchronization signal at  $V_{REF}$  [10], [11]*

- Pros: simplest frequency controller.
- Cons: very narrow frequency locking range, frequency control is not precise, unstable operation when frequency is out of range.

In all these reported works, the output voltage regulation is affected by the frequency controller, unless a dedicated voltage regulation loop is utilized [9]. But then the compensation network in the voltage loop requires additional operational amplifier or trans-conductance amplifier, and will increase design difficulty and slow down the transient response. In this work, a new frequency locking structure for hysteretic VRM is proposed, which will be shown in Section III. It controls the frequency by adjusting the hysteretic window. A simple current/voltage feedback network is adopted, which consists of only passive components and yet provides significant improvement of output voltage regulation when working together with the proposed dedicated high-speed comparator. The circuit implementation of the proposed design will be discussed in Section IV. The experimental verification and conclusions will be presented in Section V.

### III. PROPOSED FIXED-FREQUENCY CMHC

The traditional frequency-locking methods as mentioned in the previous section have some common drawbacks, e.g., complicated design with large silicon area and power consumption, difficult or sacrificed output voltage regulation, and limited frequency-tuning range. To solve these problems, a new method is proposed in this work, as shown in Fig. 2.

#### A. Frequency Tuning through adjusting the hysteretic window

In the proposed architecture, the switching duty signal  $D$  is compared with a reference clock  $CLK_{REF}$  by a phase-frequency detector (PFD). After going through a charge pump (CP) and a low-pass filter (LPF), its output  $V_c$  will control the value of a variable resistor  $R_I$ , thus adjusting the hysteretic window of the comparator. At steady state, the frequency can be derived as

$$f_{sw} = \left[ \frac{V_{DD}R_1}{R_1 + R_2} \frac{R_{fb}C_{fb}V_{IN}}{2V_{REF}(V_{IN} - 2V_{REF})} + \tau_{ON} \frac{V_{IN}}{V_{IN} - 2V_{REF}} + \tau_{OFF} \frac{V_{IN}}{2V_{REF}} \right]^{-1} \quad (3)$$

where  $V_{DD}$  is the comparator supply voltage,  $\tau_{ON}/\tau_{OFF}$  are the delay time before turning on/off the control switch, and  $R_I$  is implemented by a PMOS transistor operating in triode region with the expression

$$R_1 \approx 1/[\mu_p C_{ox}(W/L)(V_{REF} - V_c - V_{th})] \quad (4)$$

Parameters  $\mu_p$ ,  $C_{ox}$ ,  $V_{th}$ ,  $W$  and  $L$  are effective charge-carrier mobility, gate oxide capacitance (per unit area), threshold voltage, channel width and length of the PMOS transistor.

#### B. Improved Load Regulation

When adjusting the hysteretic window, the typical  $R_{fb}$ - $C_{fb}$  feedback network as in Fig. 1(b) will result in a variable output voltage error:

$$\Delta = V_{REF} - \langle V_{out} \rangle = \underbrace{\frac{V_H}{2}}_{1st} + \underbrace{\frac{V_{REF}}{2R_{fb}C_{fb}}\tau_{ON} - \frac{V_{IN} - V_{REF}}{2R_{fb}C_{fb}}\tau_{OFF}}_{2nd} + \underbrace{r_L \langle i_L \rangle}_{3rd} \quad (5)$$

It implies that the typical feedback network is not suitable for this design as  $V_H$  will be adjusted in a large range to make the frequency-locking function more robust. Thus, an improved feedback network consisting of two equal resistors  $R_{fb}$  and one capacitor  $C_{fb}$  is adopted, as shown in Fig. 2. The output voltage error with the improved  $R_{fb}$ - $R_{fb}$ - $C_{fb}$  network can be derived as

$$\begin{aligned} \Delta &= 2V_{REF} - \langle V_{out} \rangle \\ &= \underbrace{2V_{REF} \frac{R_1}{R_1 + R_2} - V_{DD} \frac{R_1}{R_1 + R_2}}_{1st} + \underbrace{\frac{2V_{REF}}{R_{fb}C_{fb}}\tau_{ON} - \frac{V_{IN} - 2V_{REF}}{R_{fb}C_{fb}}\tau_{OFF}}_{2nd} + \underbrace{r_L \langle i_L \rangle}_{3rd} \end{aligned} \quad (6)$$

The output regulation will not be affected when adjusting the hysteretic window (i.e., adjusting  $R_I$ ) because the first term in (6) is equal to zero as two conditions satisfied: 1) comparator is supplied by converter output (i.e.,  $V_{DD} = V_{out}$ ), and

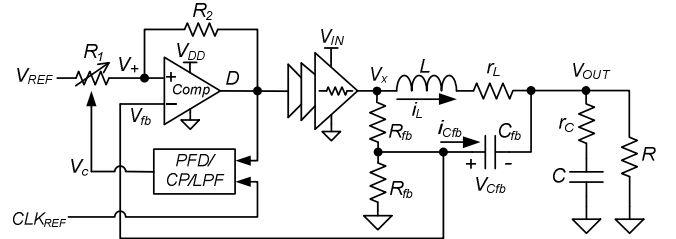


Fig. 2. Illustration of the proposed fixed-frequency CMHC buck converter with tunable hysteretic window.

2) difference between the converter real output voltage and nominal output voltage is negligible (i.e.,  $V_{out}=V_{OUT}=2V_{REF}$ ). The delays  $\tau_{ON}$  and  $\tau_{OFF}$  introduce an undesired term (second term) in (6), which also introduce non-ideal terms in (3). Their effect can be reduced when a high-speed comparator is adopted, as the one is going to be described in the next section. The third term in (6) is due to inductor ESR. It is sometimes considered as a desired feature as it helps the adaptive voltage positioning (AVP) [12] and droop method of multiphase current sharing [13].

#### IV. CIRCUIT IMPLEMENTATION

##### A. High-speed Comparator

To reduce the impact of the delays ( $\tau_{ON}$  and  $\tau_{OFF}$ ) on converter switching frequency and output regulation [as derived in (3) and (6)], a dedicated high-speed comparator is proposed in this work. As shown in Fig. 3(a), the proposed comparator has separated rising-edge detection (RED) circuit and falling-edge detection (FED) circuit, and uses an SR flip-flop to generate the final output. The RED can be understood as having a constant-current ( $I_{B1}$ ) biased input pair  $M_{14}\sim M_{15}$ , cascoded on top of an adaptively biased (by  $M_{11}$ ) input pair  $M_{12}\sim M_{13}$ . Constant biasing can limit power consumption and adaptive biasing can speed up transient response (output low-to-high) by providing large transient current. Thus the RED will have slow falling-edge response and fast rising-edge response as shown by signal “A” in Fig. 3(b), which is the origin of the name RED. On the other hand, the FED provides

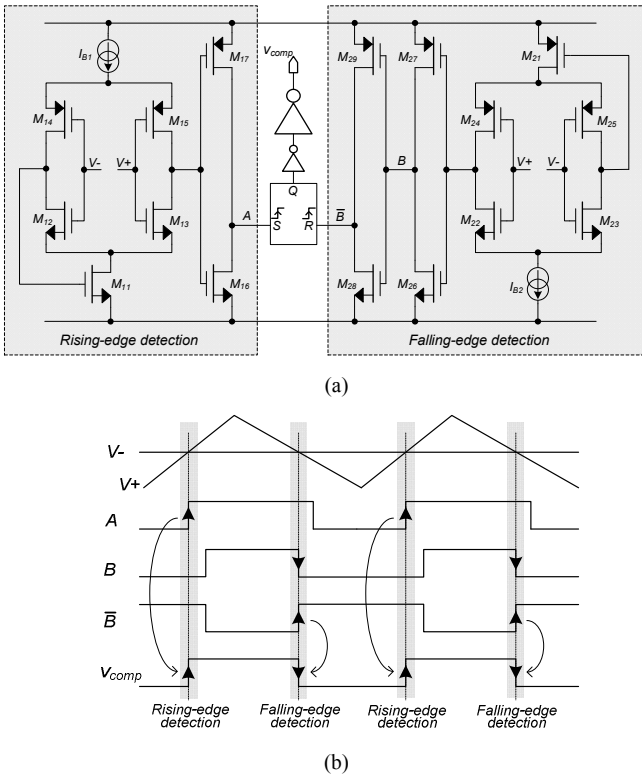


Fig. 3. Proposed high-speed comparator (a) circuit diagram and (b) operation waveforms.

slow rising-edge response and fast falling-edge response. By combining them, the proposed comparator can achieve very high speed, thus reduces the impact of  $\tau_{ON}$  and  $\tau_{OFF}$  in (3) and (6). A simulation result comparing the rising-edge responses of the proposed comparator and the traditional clamped push-pull output comparator [14] is shown in Fig. 4. It shows the delay has been reduced from 38ns to 15ns by the RED. The FED also achieves similar performance and thus it is not shown here.

##### B. Frequency-tuning Circuits: PFD, CP, and LPF

Fig. 5(a) shows the PFD used in the frequency-tuning circuit. It provides the control signals to the CP as shown in Fig. 5(b). The output  $V_C$  of the CP is used to tune the variable resistor  $R_I$  so as to adjust the hysteretic window  $V_H$ , as illustrated in Fig. 2 previously. Because  $R_I$  is implemented by a PMOS operating in triode region, a large tuning range for  $V_C$  (i.e. the PMOS gate voltage) is required in order to achieve sufficient  $V_H$  adjusting range. Therefore, a special CP is used, as shown in Fig. 5(b). It consists of a positive voltage generator and a negative voltage generator, thus its output  $V_C$  achieves a very wide range.

#### V. MEASUREMENT RESULTS AND CONCLUSION

To ensure the reliability at high temperature and high voltage, the proposed fixed-frequency hysteretic buck converter

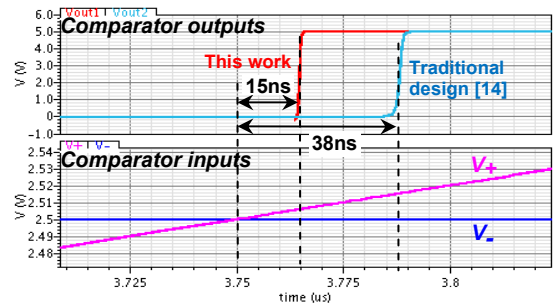


Fig. 4. Comparison of comparator simulation results between the proposed design and the traditional design [14].

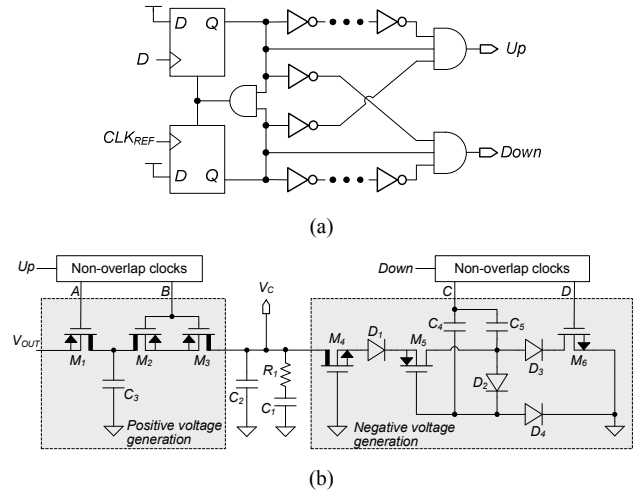


Fig. 5. Frequency tuning circuits (a) PFD and (b) CP with wide output range (transistors with thick Drain terminals are high voltage devices).

has been fabricated in XFAB 1 $\mu$ m SOI process with a chip area of 6mm<sup>2</sup>, as shown in Fig. 6. The converter specifications are listed in Table I. Without the frequency control, the converter switches at 1.28MHz at 20V input, and changes to 1.1MHz at 12V input. After enabling the frequency control, the hysteretic window  $V_H$  is adjusted, as shown in Fig. 7. The glitch on  $V_H$  is because a small capacitor is added in parallel with  $R_2$  (in Fig. 2) to enhance the positive feedback during transient. Fig. 8 shows the operating waveforms at 12V to 5V conversion, where the switching node voltage  $V_X$  (same frequency as the duty signal) is synchronized with  $CLK_{REF}$  at 1MHz. While the switching frequency in traditional hysteretic buck converter varies with input voltage, the frequency locking capability of the proposed converter is verified for a wide input voltage range, as shown in Fig. 9. In addition, owing to the improved feedback network, the output regulation achieves a constant voltage droop at -0.025V/A, eliminating the impact of frequency tuning as in conventional design.

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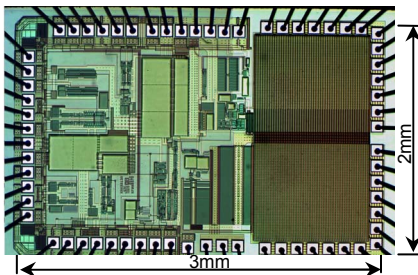


Fig. 6. Die photo of the proposed design.

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TABLE I. DESIGN SPECIFICATIONS

Technology	XFAB 1 $\mu$ m SOI
Die size	3mm x 2mm
Filtering inductor	10 $\mu$ H
Filtering capacitor	4.7 $\mu$ F
Input voltage	20V
Output voltage	5V
Load current (max)	1.2A
Free-running frequency	1.28MHz (@ 20V $V_{IN}$ )
Locked frequency	1MHz
Peak efficiency	91%

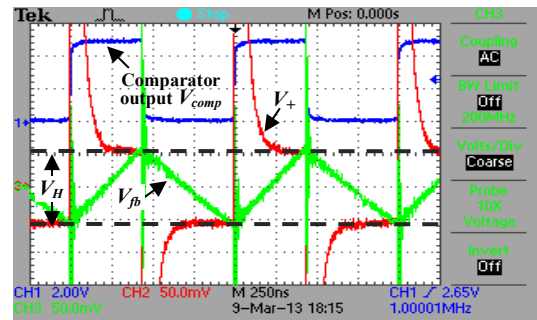


Fig. 7. Experimental waveforms for measurement of hysteretic window while the frequency is locked at 1MHz.

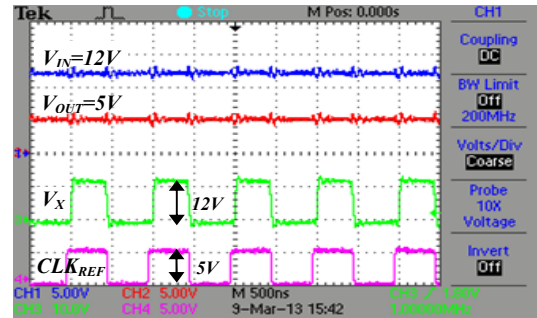


Fig. 8. Converter operating waveforms showing 1MHz fixed switching frequency for 12V to 5V conversion.

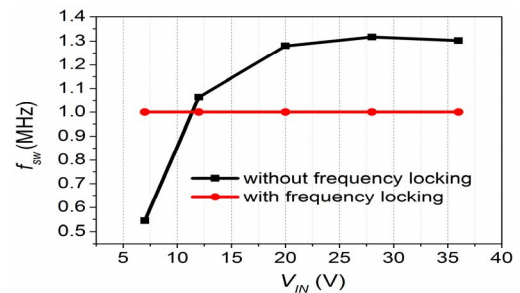


Fig. 9. The converter switching frequency is locked at 1MHz for wide input range.