

**NANYANG**  
**TECHNOLOGICAL**  
**UNIVERSITY**

**WAFER-LEVEL FINE PITCH CU-CU BONDING  
FOR 3-D STACKING OF INTEGRATED CIRCUITS**

**PENG LAN**  
**SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING**  
**2012**

**WAFER-LEVEL FINE PITCH CU-CU BONDING  
FOR 3-D STACKING OF INTEGRATED CIRCUITS**

**PENG LAN**

(B. Eng., Nanyang Technological University)

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## Executive Summary

The increasing demand for system performance enhancement and more functionality has led to the exploration of 3-D IC technology, which possesses attractive benefits in form factor, density, performance, heterogeneous integration, and lower cost. One of the key challenges to realize 3-D integration is to develop a robust bonding technique. While solder-based technology appears to be a convenient way (since it is widely used in the packaging community) for 3-D stacking, it is inadequate to meet the increasing needs for fine pitch and reliable vertical interconnection in stacked ICs. Among various emerging bonding methods, Cu-Cu bonding is an attractive option because it is able to provide strong mechanical strength to support stacked layers and conduct current effectively with its intrinsic bonding medium. In addition, wafer-to-wafer (W2W) bonding scheme is gaining favorable attention for the feature of higher manufacturing throughput than chip-to-wafer or chip-to-chip.

Conventionally, reliable Cu-Cu bond is formed by using thermo-compression bonding (TCB) which makes use of contact pressure and high temperature ( $> 350\text{ }^{\circ}\text{C}$ ) to facilitate inter-diffusion of Cu atoms in order to promote bonding adhesion. However, high temperature TCB process limits its attractiveness due to the stringent thermal budget control of the stacked device. Lowering down the bonding temperature has become extremely difficult due to the ease of Cu surface oxidation which degrades the bonding reliabilities. Therefore, it is important to explore a robust approach to realize high density Cu-Cu bonding at low temperature.

This thesis proposes a low temperature wafer-to-wafer fine pitch (5-15  $\mu\text{m}$ ) Cu-Cu bonding technology. This technology incorporates bonding enhancement methods such as self-assembled monolayer (SAM) passivation and hermetic Cu seal

ring. SAM passivation provides a temporary protection on the Cu surface prior to bonding. It is found to effectively reduce Cu oxidation and particle contamination. The monolayer is also able to be desorbed by thermal annealing process. On the other hand, an introduction of Cu seal ring which can be simultaneous formed during the bonding process exhibits excellent hermetic properties to encapsulate the stacked device. The overall bonding reliability is enhanced with the combination of both two methods. Finally, the applications of SAM and hermetic seal are extended to the practical 3-D integration, where the seamless development of Cu TSV and Cu-Cu bonding are explored in wafer-scale, resulting in promising technology advancement for the future wafer-to-wafer implementation of 3-D ICs.

The discussion on Cu-Cu bonding technology in this thesis is divided into the following 4 parts: 1) the fundamental study of thermo-compression Cu-Cu bonding; 2) the development of wafer level fine-pitch Cu-Cu bonding; 3) the characterization of Cu-Cu bonding contact with enhancement methods; 4) the characterization of fine pitch Cu-Cu bonding system and 3-D stacking demonstration of TSV and Cu-Cu bonding integration.

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# List of Abbreviations

2-D	Two-Dimensional
3-D	Three-Dimensional
3-D IC	Three-Dimensional Integrated Circuit
AFM	Atomic Force Microscopy
Ar	Argon
BCB	Benzocyclobuten
BOE	Buffered Oxide Etchant
CMP	Chemical-Mechanical Polishing
CTE	Coefficient of Thermal Expansion
DBI	Direct Bond Inteconnect
ECP	Electro-Chemical Plating
EDX	Energy-dispersive X-ray Spectroscopy
EELS	Electron Energy Loss Spectroscopy
EM	Electromigration
F2F	Face-to-face
FIB	Focused Ion Beam
ILD	Inter Layer Dielectric
IMC	Inter-metallic Compound
IMD	Inter-metal Dielectric
ITRS	International Technology Roadmap for Semiconductors
KGD	Known-Good-Die
M1	Metal 1
M2	Metal 2
MEMS	Micro-Electro-Mechanical System

MtM	More-than-Moore
N <sub>2</sub>	Nitrogen
PEVCD	Plasma-Enhanced Chemical Vapor Deposition
PoP	Package-on-Package
PVD	Physical Vapor Deposition
RDL	Redistribution Layer
RIE	Reactive Ion Etching
RMS	Root-Mean-Square
SAB	Surface Activated Bonding
SAM	Self-Assembled Monolayer
SiN	Silicon Nitride
SiO <sub>2</sub>	Silicon Dioxide
SiP	System-in-package
SoC	System-on-Chip
SOI	Silicon on Insulator
TaN	Tantalum Nitride
TMAH	Tetra-methyl-ammonium-hydroxide
TSV	Through Silicon Via
TTV	Total Thickness Variation
VLSI	Very-large-scale Integration
W2W	Wafer-to-Wafer

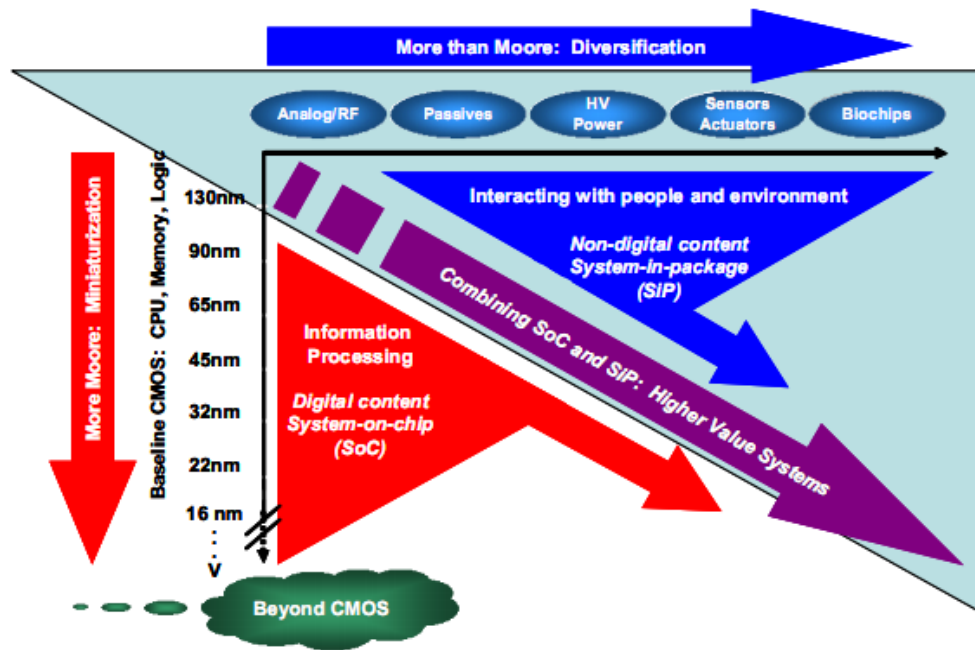
# Chapter 1

## Introduction

### 1.1 Introduction

Technological advancement of electronic devices has been dramatically progressed over the past few decades. Two decades ago, people used to work on a bulky desktop computer with simple functionalities. Today a large cohort has become fans of Apple's portable devices' with millions of applications ranging from entertainment to work. Thanks to Moore's law, the dimension of integrated circuit (IC) has been scaled down rigorously while the performance keeps improving with the feasibility of transistor shrinkage. However, the conventional device scaling has become challenging due to the physical limits of transistor size even though various enabling technologies have been implemented to sustain the improvement [1.1, 1.2].

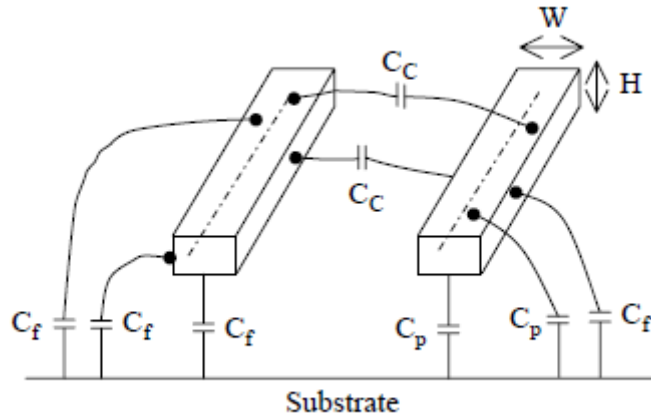
While people are still striving to follow Moore's law for the 20 nm node and beyond, there are two major directions that industry is moving towards to augment this principle: 1. "More Moore": Density and performance improvement by continuous planar scaling of the physical feature size with new process techniques and materials. 2. "More-than-Moore" (MtM): Value added approaches without the necessary scaling such as System-on-Chip (SoC), System-in-package (SiP) and heterogeneous integration. Figure 1.1 depicts both categories of More Moore and More-than-Moore, which focus on miniaturization of feature size and diversification to multiple functionalities, respectively [1.3].



**Figure 1.1:** Categories of miniaturization of the digital functions (“More Moore”) and functional diversification (“More-than-Moore”). [1.3]

Among the various implementations of MtM, the opportunities on the third dimension, which provide a vertical platform for multifunctional integration, have been favourably discussed and explored over the past few years [1.4, 1.5]. The new term, three-dimensional integrated circuits (3-D ICs), further current technology by adding more device layers on a single chip, and open up a new era to boost both economic and technological growth with promising benefits [1.6].

On the other hand, it is also worthwhile to point out that the advancement of transistor scaling has inevitable problems at the global interconnect regime. In the earlier technology node, the parallel plate capacitance ( $C_p$ ) is the dominant factor of the interconnect wiring. Figure 1.2 shows the effect of different parasitic capacitances induced when the wires become denser and the width ( $W$ ) of Cu interconnect keeps



**Figure 1.2:** Parasitic capacitance between two interconnect wires on the same level [1.7].

shrinking. The fringe capacitance  $C_f$  and the coupling capacitance  $C_c$  are no longer negligible while estimating the parasitic capacitive effect. Due to the charging effect of induced parasitic capacitors, signal transfer is slowed down between functional blocks.

At the same time, more interconnect wires are needed to connect within functional blocks and to link them, in a millimetre range due to larger chip size and more downscaled transistors. Therefore, the lengths of both intermediate and global interconnects are adversely affected with the transistor scaling [1.8]. The combined effect of both resistance and capacitance ( $RC$ ) product is given in equation (1.1) [1.9], which represents a large proportion of power consumption and signal delay.

$$R \cdot C = \frac{\rho \cdot l}{h \cdot d} \cdot \alpha K_{\text{eff}} \epsilon_0 \frac{h \cdot l}{d} \quad (1.1)$$

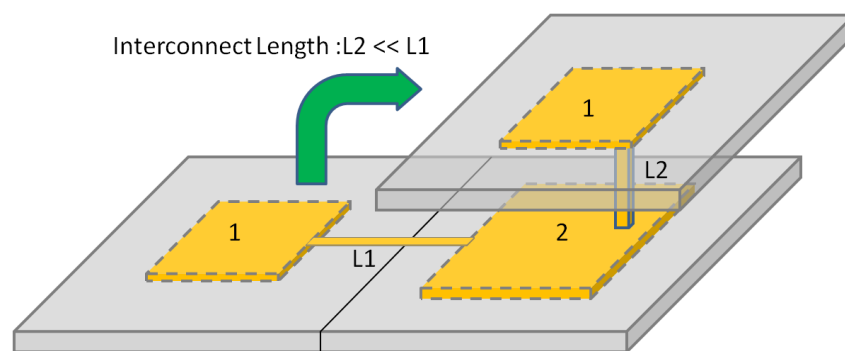
## Chapter 1- Introduction

where  $\rho$  is the line resistivity,  $\alpha$  is the structural factor,  $K_{\text{eff}}$  is the effective dielectric constant,  $\epsilon_0$  is the permittivity in vacuum, and  $l$ ,  $h$ , and  $d$  are the length, height, and half pitch of the interconnect line. The structural factor  $\alpha$  depends on the neighbouring interconnect existence. The  $R$  and  $C$  are in a trade-off relationship with  $h$ , which affects both the electron scattering effect and parasitic capacitance of the inter-metal dielectric (IMD). Moreover, reliability challenges are posed on back-end-of-line (BEOL) copper/ low- $k$  interconnects with reduced dimensions where electromigration (EM) significantly affects copper line performance [1.10]. Therefore, planar circuits suffer from a significant performance loss at the interconnect-limited stage if conventional 2-D scaling is further pursued.

## 1.2 Motivations of 3-D ICs

### 1.2.1 Improvement of RC delay

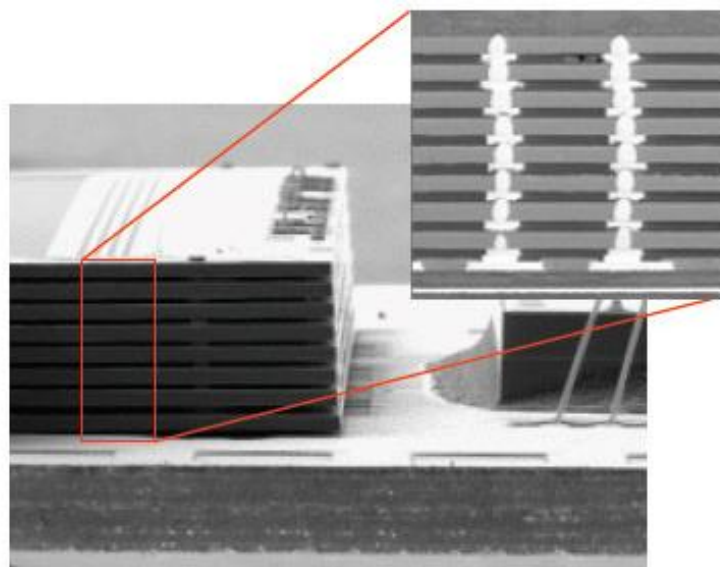
Due to planar scaling becoming more challenging, it is a right time to explore the opportunity in the vertical dimension to continue Moore's prediction. Three-dimensional integrated circuits (3-D ICs), enable vertical access between ICs, has been given a tremendous focus for the advantage of multiplying IC stacking performance and system integration to meet the increasing demand of system performance and functionality. Instead of wiring different functional blocks on a planar substrate, vertical interconnection between adjacent stacking layers will significantly decrease the global interconnect length which in turns, reduce the *RC* delay, as shown in Figure 1.3.



**Figure 1.3:** Transformation from 2-D to 3-D integration with a much shorter interconnect length.

*1.2.2 Device multiplication through 3-D technology*

3-D ICs technology provides an indirect improvement on the circuit density without necessary scaling effort. Figure 1.2 shows a 16-Gbit memory device composed of eight stacked, 50-micron thick, 2-Gbit NAND flash die demonstrated by Samsung [1.11]. The stacked device is reported with a smaller footprint (15%) and a thinner thickness (30%) than a wire-bonded device. The total length of the equivalent global interconnects is significantly reduced due to replacing conventional millimetre-range of planar wires with micrometre-range of vertical interconnects, resulting in an approximately 30 percent increase in performance due to the reduced electrical resistance. More active IC layers could be stacked using the existing technology node. It is also worthwhile to point out that the inter-chip connection provided by the micro-bumps has a pitch size of  $> 50 \mu\text{m}$ . Future 3-D IC applications have an inevitable trend of pitch scaling to further improve the performance for the stacked devices. Therefore, a substantial interest will be focused on the development of ultrahigh density interconnection.



**Figure 1.4:** Memory stacking through 3-D TSV implementation [1.11].

## Chapter 1- Introduction

### *1.2.3 Bandwidth enhancement*

Historically, both logic and memory devices are placed on a single board where the data is transferred through off-chip buses. Today, the limited bus channels restrain the overall system performance despite constant technology advancement for individual devices. Using 3-D interconnect architecture to place the memory chip on top of the logic device, the number of channels extend to the whole chip area. Therefore, the bottleneck of planar off-chip buses is overcome by >100X increment in the connection density. And the power efficiency is substantially improved. Consequently, the 3-D technology has been profoundly addressed by the International Technology Roadmap for Semiconductor (ITRS), for the ability to suppress RC delay by shorter vertical interconnects and to enable bandwidth enhancement with wide I/O interfaces [1.12].

Furthermore, more advantages of 3-D ICs are summarized below,

1. Form factor: Chip footprint is reduced as compared to 3-D packaging methods such as wire-bonds and package-on-package (PoP).
2. Performance: Improvement on interconnect delay and power consumption favours 3-D architecture for the flexibility in system design, functional placement and wire routing.
3. High volume low cost production: 3-D ICs implementation requires less processing complexity and integration costs as compared to the demand for SoC.
4. New applications: Heterogeneous integration enables multifunctional device to be implemented [1.13].

### **1.3 Scope of Project**

In this dissertation, technology development of a wafer level fine pitch bonding approach is explored to meet the needs for future high density 3-D IC applications. This study will focus on thermo-compression Cu-Cu bonding based on the advantages such as scaling, electrical performance and mechanical properties. Fundamental characterization of Cu-Cu bond will be presented with the incorporation of enhancement methods. Fine pitch Cu-Cu bonding circuits are also fabricated and investigated. We further examine this proposed method which can be seamlessly integrated into the state-of-the-art TSV technology for future ultrahigh density 3D applications.

The specific objectives of this research include:

(1) Design, fabrication and optimization of fine pitch (5-15  $\mu\text{m}$ ) Cu-Cu bonding using wafer-to-wafer stacking to provide the research platform for high density 3-D IC application.

(2) Exploration of a reliable and robust Cu-Cu bonding technology by incorporating bonding enhancement methods.

(3) Investigation and characterization of the bonding properties of designed vehicles including fine pitch daisy chain and Kelvin structures utilizing the explored enhancement methods.

(4) Extension of enhanced Cu-Cu bonding platform, to be integrated with Cu TSV for advanced demonstration of 3-D integration.

## **1.4 Thesis Organization**

The main focus of this work is on technology development of a reliable and compatible bonding scheme for the application of high density 3-D ICs.

Chapter 2 starts with the literature study in the current research effort on exploring and analyzing potential bonding options for the stacking of 3-D ICs. Particularly, Cu-Cu bonding technology is favourably discussed and compared.

In Chapter 3, we investigate the key parameters of wafer-to-wafer (W2W) thermo-compression Cu-Cu bonding. The effect of microstructural evolution of Cu grains towards bonding process is studied. Bonding enhancement techniques using self-assembled monolayer (SAM) passivation and hermetic Cu seal are discussed and applied to the technology development of wafer level fine-pitch Cu-Cu bonding.

Chapter 4 introduces the mask design of wafer level Cu-Cu bonding with the test structures incorporated. The process flow and key process challenges are presented. Mechanical properties are characterized based on the bonded wafer with optimized fabrication process.

Chapter 5 presents the characterization of Cu-Cu bonding contact including the effects of enhanced bonding methods, bonding temperature, thermal reliability and encapsulation of Cu seal ring.

In Chapter 6, a study of fine-pitch Cu-Cu bonding system is presented. The daisy chain containing 15  $\mu\text{m}$  pitch to 6  $\mu\text{m}$  pitch of Cu-Cu contacts are demonstrated. Electrical and thermal properties are characterized. Finally, a successful demonstration of 3-D integration process is presented utilising Cu-Cu bonding and TSV. Integration challenges and system reliabilities are focused.

Finally, Chapter 7 summaries and concludes the contribution of this doctoral work and makes suggestions to the future work.

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## **Chapter 2**

# **Overview of 3-D IC Technology**

### **2.1 Technology Advancement of 3-D IC**

3-D IC originated from the silicon-on-insulator (SOI) technology during the 1980s when Moore's law was expected to reach the limit of miniaturization [2.1]. It is an MtM approach which brings a stack of active devices together to form local on-chip interconnects in the vertical direction. 3-D IC provides higher density achievable without further transistor shrinkage by stacking several layers with vertical interconnections. As technology evolves, the performance of electronic devices has become more interconnect-dominated, which results in longer global interconnects, a smaller transistor dimension and larger chip size. As such, more electrical power is needed to compensate the resistance-capacitance coupled effect. Furthermore, 3-D IC can also be used to separate different functional blocks into different vertical layers to reduce the total interconnect length. Consequently, lower RC delay and lower power consumption can be expected to improve the overall device performance.

Figure 2.1 shares a long term projection viewed by LETI. 3-D ICs are expected to realise more functionalities with high density 3-D interconnects, utilising separated process technology for different applications and stacking approaches. Beyond year 2014, a 3-D SoC system may seem to attract more attentions with cost-effective solutions. In the meantime, it is important to develop a reliable technology with the minimum pitch of vertical interconnect to be  $< 10 \mu\text{m}$ , to meet the demand of ultrahigh density 3-D applications.

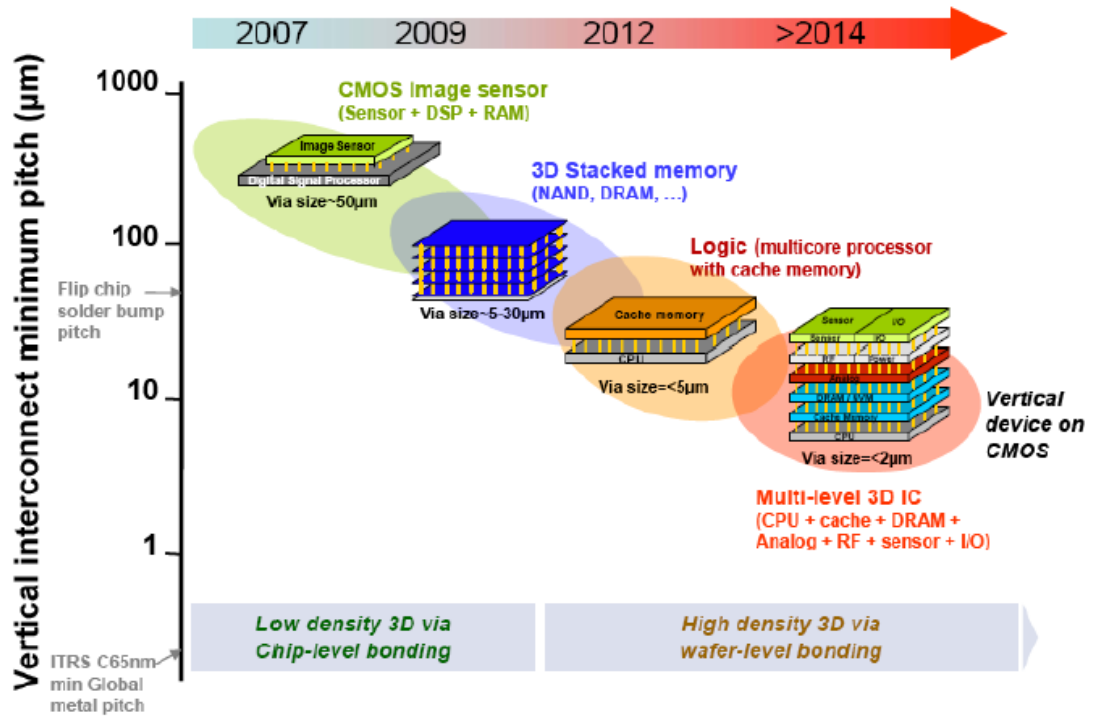
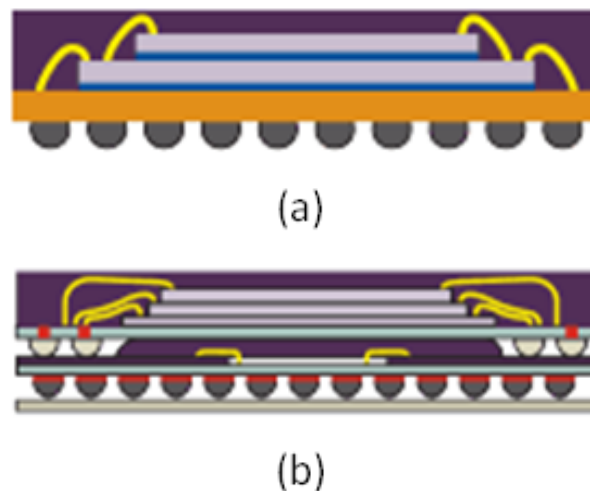


Figure 2.1: Outlook of 3-D IC applications [2.2].

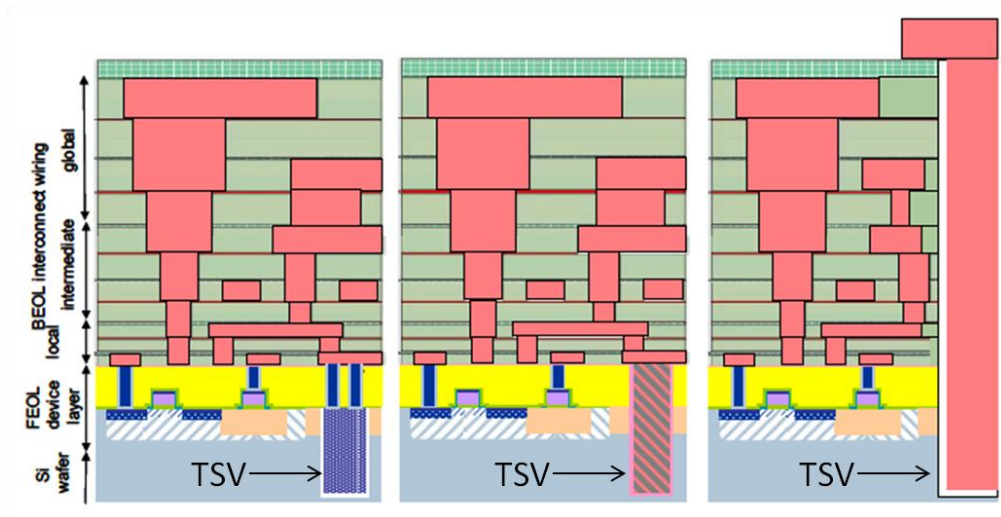
## **2.2 3-D Packaging and 3-D IC Integration**

There are two major categories of 3-D implementation: 3-D packaging and 3-D IC integration. Presently, 3-D packaging has been adopted in the industry for mass production due to the demand of small form factor. Figure 2.2 (a) shows the stacking of IC chips using wire bonding technique. Au/Cu wires are normally employed to connect I/O from the periphery of chip to the substrate [2.3]. It is a cost effective way to achieve a reduction in footprint. However, limited number of wires can be applied due to the small boundary area of the chip. In Figure 2.2 (b), package-on-package (PoP) technology is considered as the evolved technology for 3-D packaging, in which an increasing demand for a more efficient packaging approach is desired. Individual packages are integrated in a vertical fashion with flexible fan-outs to the substrate. Particularly, PoP enables the integration of logic and memory chips with the same package form factor. Both methods are 3-D packaging implementations and no direct inter-chip connection is used for the stacked device.



**Figure 2.2:** 3-D packaging implementations. (a) Chips are stacked vertically using wirebonding to connect with the substrate. (b) Illustration of two packages stacked together (PoP) [2.4].

For 3-D IC integration, active IC layers are directly interconnected without using external wires. Through silicon via (TSV) is the key driver that integrates the stacked devices. A TSV connection is a galvanic connection through the Silicon wafer, in which the power and the signal can be effectively delivered [2.5]. Figure 2.3 illustrates three types of TSV fabrication methods with different integration capabilities [2.6-2.8]. Utilising inter-wafer connections, TSV technology enables much denser I/O interfaces for 3-D integration [2.9].



**Figure 2.3:** TSV “Via First”, “Via Middle” and “Via Last” process flows [2.5].

## **2.3 3-D IC Integration Approaches**

### *2.3.1 Monolithic approaches*

The implementation of monolithic approach makes use of a single substrate, on which active layers and vertical interconnections are built sequentially in a bottom-up process. This method is compatible with mainstream processes and it provides high alignment accuracy between different layers. The implementation can be achieved through various alternatives such as silicon epitaxial growth [2.10], beam recrystallization [2.11] and solid phase crystallization [2.12]. However, the disadvantages of the bottom-up process are associated with difficulties in forming high quality layer formation and low efficiency in manufacturing cycle. Furthermore, it also has difficulties in realizing heterogeneous integration due to technology differences. In contrast, the stacking of ICs using multiple substrates offers less process complexity of integrating devices with different functionalities.

### *2.3.2 Stacking approaches*

In general, there are three types of stacking approaches in terms of processing stages such as chip-to-chip, chip-to-wafer and wafer-to-wafer. Chip-to-chip stacking is a method using fully tested IC chips to form the vertical stack [2.13]. This method can provide off-chip signal travelling with bond wires or on-chip transfer using TSV techniques. The capability of multiple chips stacking is widely accepted and employed in today's portable devices, which demand small form factors. On the other hand, chip-to-wafer stacking often uses pick-and-place equipment to bond known-good-dies (KGDs) to good dies in the substrate wafer with a high yield level [2.14]. However, there is a trade-off between the alignment accuracy and the throughput

when a large number of dies are present on the substrate wafer. Therefore, this method is less favourable for high density 3-D applications in the manufacturing perspective.

In wafer-to-wafer (W2W) stacking, all dies on the pairing wafers are precisely aligned at the same time and bonded [2.15]. Therefore, when the die size is small and precise alignment is needed, W2W stacking is preferred over C2W stacking. Vertical through-wafer connections are accomplished by direct bonds between wafers using various bonding methods such as oxide bonding, metal bonding, hybrid bonding and glue bonding. However, it possesses potential issues such as yield loss, mechanical reliability and bonding uniformity. In this work, W2W stacking is explored and implemented for the demonstration of 3-D ICs.

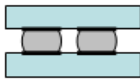
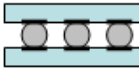

## 2.4 Wafer-to-Wafer (W2W) Bonding Methods

There are various available technologies to assemble fully processed wafers for 3-D IC integration based on the needs of different applications. Wafer-level stacking can be achieved by metal-to-metal bonding, oxide-to-oxide bonding, adhesive bonding and hybrid bonding. Following is the classification of these technologies,

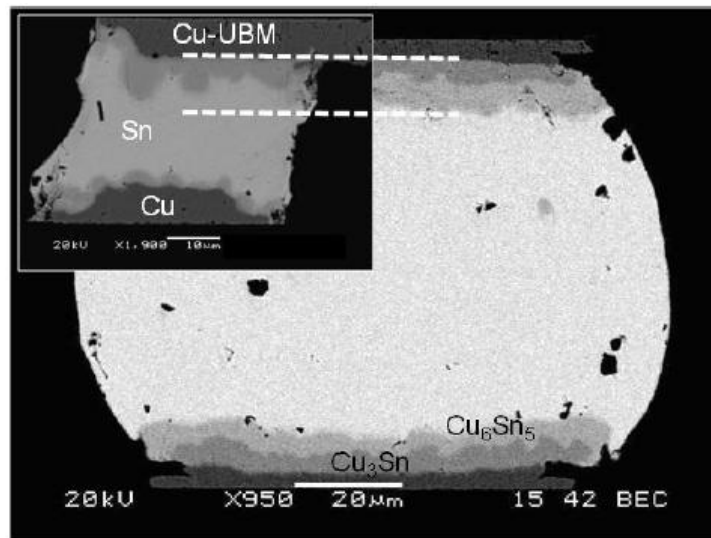
### 2.4.1 Metal-to-metal bonding

Cu-Cu bonding is a typical metal-to-metal bonding method and it has been reported with merits in providing strong mechanical strength to support stacked layers and conducting current effectively with its intrinsic bonding medium [2.16]. Besides the good mechanical properties, Cu-Cu bonding is also attractive because Cu-Cu bond has better scalability, and excellent electrical properties due to the absence of inter-metallic compound as compared to solder-based connection, as shown in Table 2.1. As such, Cu-Cu bonding can be implemented with the via-first process, and high density of vertical interconnects are formed when wafers are bonded.

**Table 2.1:** Progression in the density of IC-to-IC interconnects in future 3-D IC. Bump-less Cu-Cu bonding demonstrates better scalability in pad size and pitch as compared to micro-bump.

<b>Ball Grid Array</b> (Package-on- Package)	<b>Micro-Bump</b> (Chip-on-Chip, Chip-on-Wafer)	<b>Bump-less Cu-Cu</b> (Chip-on-Wafer, Wafer-on-Wafer)
		
Size ~ 450 $\mu\text{m}$	60-120 $\mu\text{m}$	< 10 $\mu\text{m}$
Pitch ~ 1000 $\mu\text{m}$	120-240 $\mu\text{m}$	< 20 $\mu\text{m}$

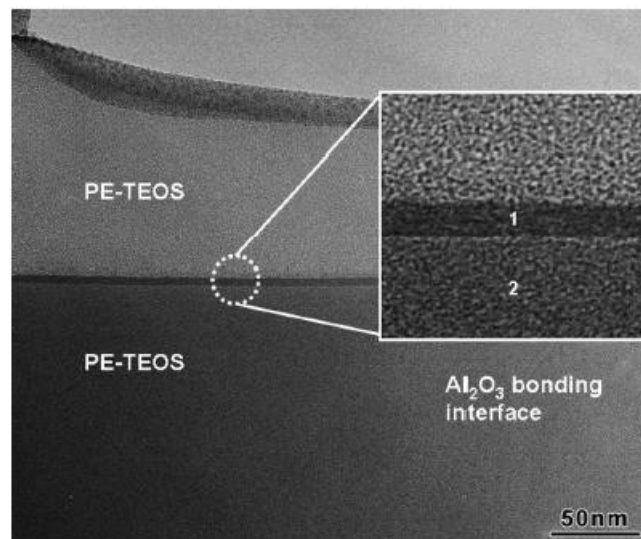
Another interesting metal-to-metal bonding system is based on solid-liquid inter-diffusion bonding (SLID). A typical example is Cu/Sn-Cu bonding, in which tin (Sn) is melted at a relatively lower temperature of 232°C in between Cu layers to form intermetallic compound (IMC) layers. As the resulted IMC has a much higher melting temperature up to 600 °C, the bonding interface will sustain from high temperature treatment [2.17]. Figure 2.4 shows Cu-Sn-Cu joints with different dimensions result in different stand-off height and IMC/solder ratio [2.18]. It is worthwhile to point out that the difference in the solder size has profound effect on electrical and mechanical reliabilities of the bonded wafer. Therefore, the use of this type of bonding poses serious challenges on the scaling for ultrahigh density 3-D application.



**Figure 2.4:** Cu/Sn-Cu bonding interfaces with different dimensions of solder joints [2.18].

*2.4.2 Oxide-to-oxide bonding*

Oxide-to-oxide bonding requires a very stringent surface smoothness which can be accomplished by polishing and plasma activation [2.19]. Wafer-level oxide-to-oxide bonding is also affected by wafer warp which significantly reduces the bonding strength. The bonding strength enhancement has been demonstrated by adding a thin capping layer of high- $k$  dielectric on PE-TEOS oxide, as shown in Figure 2.5 [2.20]. After the bonding process, the vertical interconnection of 3-D IC is achieved by forming a TSV with a high aspect ratio as there is no electrical conduction at the bonding interface. An important application of oxide-to-oxide bonding is the fabrication of SOI wafer, which provides a profound advancement in device isolation with a buried oxide layer [2.21].



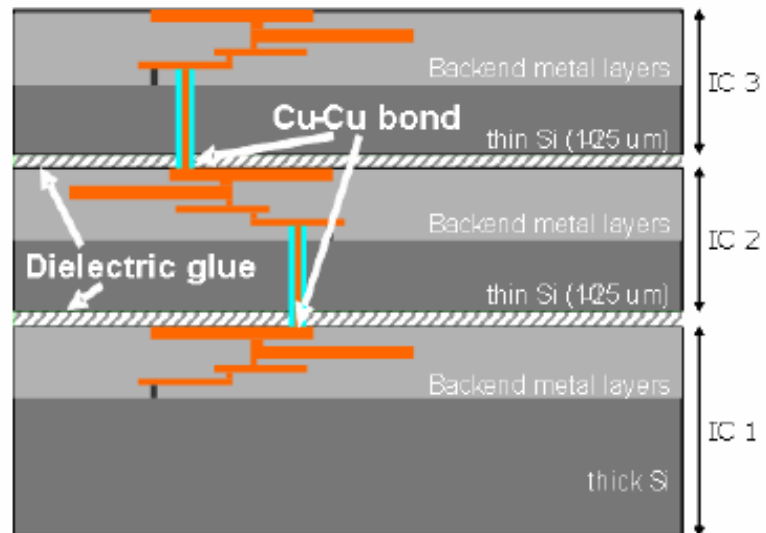
**Figure 2.5:** Cross-sectional TEM image showing a seamless bonding interface of Al<sub>2</sub>O<sub>3</sub>/PE-TEOS wafers [2.20].

### *2.4.3 Adhesive bonding*

Adhesive bonding (polymer-to-polymer) refers to contact interface gluing with an intermediate adhesive layer by applying heat and pressure [2.22]. Similar to oxide-to-oxide bonding, adhesive bonding provides mechanical support and adhesion for wafer stacking. At the same time, it has fewer requirements for surface roughness as compared to metal-to-metal bonding and oxide-to-oxide bonding. Therefore, adhesive bonding possesses advantages of stacking ICs with different technologies for a heterogeneous integration. Benzocyclobute (BCB) is the most widely used polymer in the adhesive bonding process and it has been intensively studied for 3-D IC, MEMS, and VLSI packaging applications [2.23-2.25]. The major issue associated with this bonding scheme is the fabrication of a high aspect ratio TSV thereafter, which poses process challenges to the 3-D integration [2.26].

### *2.4.4 Hybrid bonding*

Generally, a direct metal-to-metal bonding inevitably leaves behind air gaps between metal bonded structures. The concerns raised due to the air gaps include corrosion due to moisture and mechanical reliability. In order to tackle this issue, hybrid bonding emerges as an enabling technology which combines metal-to-metal bonding with adhesive or oxide-to-oxide bonding [2.27-2.29]. A seamless bonding interface across wafer-level can be achieved by Cu-Cu bonds and an underfill layer formed by adhesives, as shown in Figure 2.6. Therefore, the overall mechanical stability will be improved with the collective bonding strength. However, hybrid bonding also brings new challenges such as surface planarity and partial contact between Cu and the dielectric due to possible W2W misalignment.



**Figure 2.6:** Schematic integration scheme of multi-level stacking using hybrid bonding [2.27].

## 2.5 Comparison between Micro-bump and Cu-Cu Bonding

Presently, industry is actively pursuing 3-D IC stacking by utilising solder micro-bump to achieve vertical interconnections between the strata layers. The technology is promising at a pitch of  $\sim 50 \mu\text{m}$  with reported results [2.30]. Cu-Cu bonding technology in contrast, offers a more scalable option with the pitch of  $< 10 \mu\text{m}$ . Table 2.2 lists the major differences between both alternatives. The key distinctions are: 1) Conventional thermo-compression Cu-Cu bonding requires a much higher temperature to form a reliable bond; 2) Cu-Cu bonding enables ultrahigh density 3-D application as the size of the Cu pad can be scaled aggressively; 3) Solder micro-bump is less reliable due to the presence of IMC. The interconnection resistance is also higher than that of Cu; 4) Stringent surface requirements need to be taken into account of for Cu-Cu bonding.

**Table 2.2:** Comparison between solder micro-bump and bump-less Cu-Cu.

	<b>Solder Micro-bump</b>	<b>Pad-to-Pad (Bump-less)</b>
<b>Bonding Method</b>	Reflow	Thermo-compression bonding
<b>Bonding Temperature</b>	$\sim 250\text{-}300 \text{ }^\circ\text{C}$ (Sn)	$350 - 450 \text{ }^\circ\text{C}$ (Cu-Cu)
<b>Bump Size</b>	$30\text{-}120 \mu\text{m}$	$< 10 \mu\text{m}$
<b>Pitch</b>	$50\text{-}240 \mu\text{m}$	$< 20 \mu\text{m}$
<b>EM Reliability</b>	Low, due to IMC	High, no IMC
<b>Resistivity</b>	$8.93 \mu\Omega\text{.cm}$ ( $\text{Cu}_3\text{Sn}$ ) $17.5 \mu\Omega\text{.cm}$ ( $\text{Cu}_6\text{Sn}_5$ )	$\sim 1.7 \mu\Omega\text{.cm}$ (Cu)
<b>Surface Requirement</b>	Tolerant to particle, roughness	Free from surface oxide/contamination, stringent roughness
<b>Throughput</b>	High	Low to moderate

**Table 2.3:** The 2009 ITRS Roadmap for Global/3-D Interconnect [2.31].

<i>Global Level, W2W, D2W or D2D 3D- stacking</i>	<i>2009-2012</i>	<i>2012-2015</i>
Minimum TSV diameter	4-8 $\mu\text{m}$	2-4 $\mu\text{m}$
Minimum TSV pitch	8-16 $\mu\text{m}$	4-8 $\mu\text{m}$
Minimum TSV depth	20-50 $\mu\text{m}$	20-50 $\mu\text{m}$
Minimum TSV aspect ratio	5:1-10:1	10:1-20:1
Bonding overlay accuracy	1.0-1.5 $\mu\text{m}$	0.5-1.0 $\mu\text{m}$
Minimum contact pitch (thermo-compression)	10 $\mu\text{m}$	5 $\mu\text{m}$
Minimum contact pitch (solder micro-bump)	20 $\mu\text{m}$	10 $\mu\text{m}$

In line of the effort put in for both bonding options, the ITRS roadmap for global interconnect level as shown in Table 2.3 is drawn up to highlight the desired outcome [2.31]. It can be seen from the same table that within 3 years from now, the pitch of the solder micro-bump needs to be scaled down to 10  $\mu\text{m}$  and the pitch of bump-less thermo-compression bonding needs to scale down to 5  $\mu\text{m}$ .

Comparing the resistance of single bonded structure between Cu/Sn solder micro-bump and bump-less Cu-Cu contact, Figure 2.7 (a) presents a homogeneously bonded Cu layer with a diameter of 10  $\mu\text{m}$  and Figure (b) shows the details of the thickness for each IMC layer with the same diameter. As such, the resistance for each can be calculated using equation (2.1) as follows,

$$R = \frac{\rho \cdot l}{s} \quad (2.1)$$

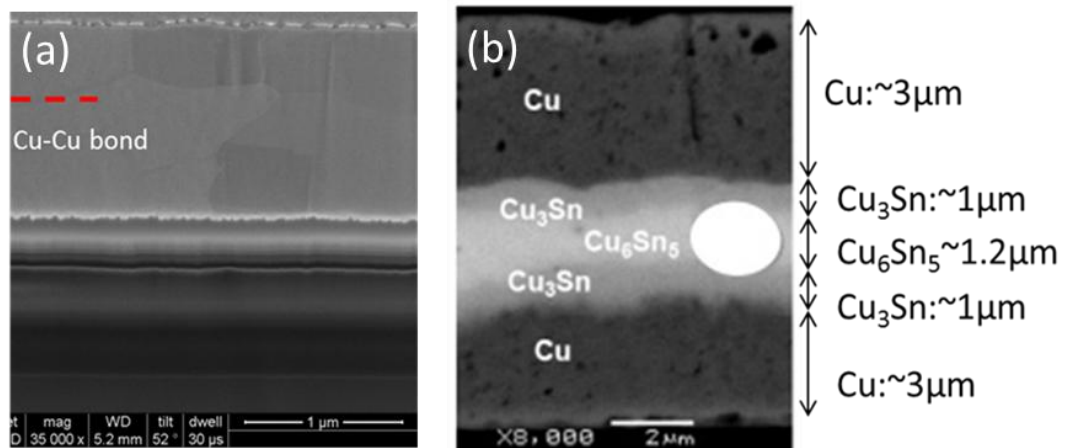
(1) Cu/Sn micro-bump, with total thickness of  $\sim 9.2 \mu\text{m}$  (Figure 2.7 (b)),

$$R_{total} = R_{cu} + R_{Cu_3Sn} + R_{Cu_6Sn_5} + R_{Cu_3Sn} + R_{cu} = 6.247 \text{ m}\Omega$$

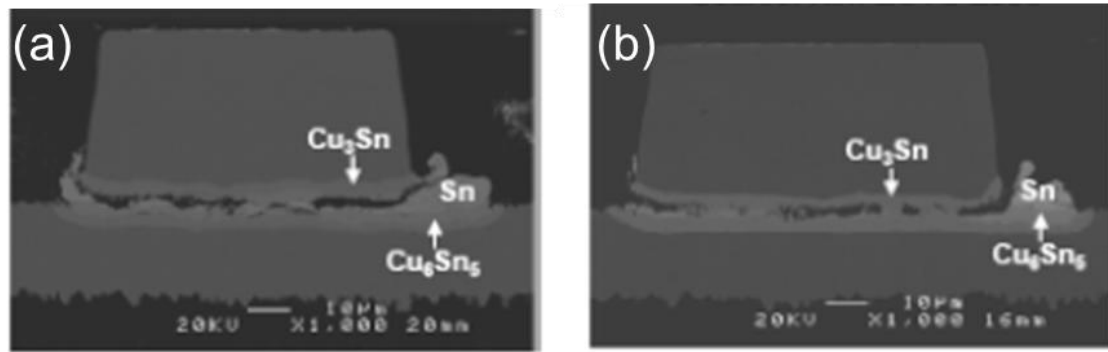
(2) Homogeneous Cu-Cu bonded layer with the same size and thickness,

$$R_{total} = R_{cu} + R_{cu} = 1.991 \text{ m}\Omega$$

The resistivity of Cu,  $\text{Cu}_3\text{Sn}$  and  $\text{Cu}_6\text{Sn}_5$  are  $\sim 1.7 \mu\Omega\cdot\text{cm}$ ,  $\sim 8.93 \mu\Omega\cdot\text{cm}$ , and  $\sim 17.5 \mu\Omega\cdot\text{cm}$ , respectively. Therefore, it can be seen that the resistance of a single Cu/Sn micro-bump is 3X larger than that of a Cu bonded layer. When the bonding material is applied to 3-D IC with high density vertical interconnections, the differences turn out to be even greater with regard to the power consumption at 3-D interconnect level.



**Figure 2.7:** SEM images showing (a) Cu-Cu bonding with seamless interface; (b) Interface layers composition for Cu/Sn solder micro-bump.



**Figure 2.8:** SEM images of void formation between micro-bumps due to EM (a) under a temperature anneal of 150 °C for 200 hr; (b) under current stressing of  $5 \times 10^4$  A/cm<sup>2</sup>, in addition to the anneal [2.33].

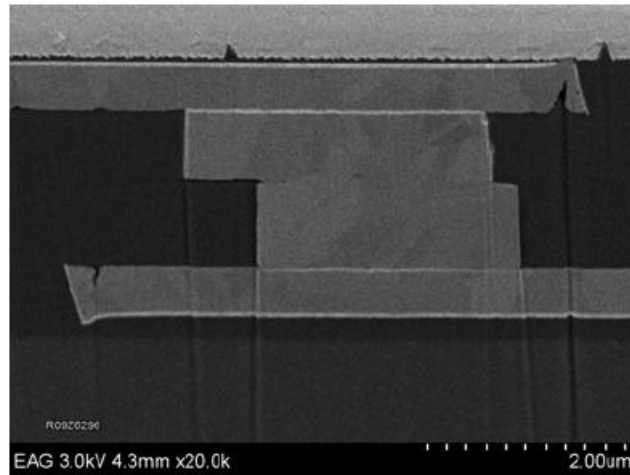
In addition, it is also understood that at fine pitch condition, IMC consumes all solder, decreases mechanical reliability as IMC is brittle, and potential Kirkendall void formation could occur between Cu and solder [2.32]. In addition, Figure 2.8 (a)-(b) shows significant EM failures during annealing and current stressing [2.33]. Therefore, the scaling of solder micro-bump poses reliability challenges for 3-D fine pitch applications.

## **2.6 Cu-Cu Bonding Options**

### *2.6.1 Low temperature Cu-Cu bonding techniques*

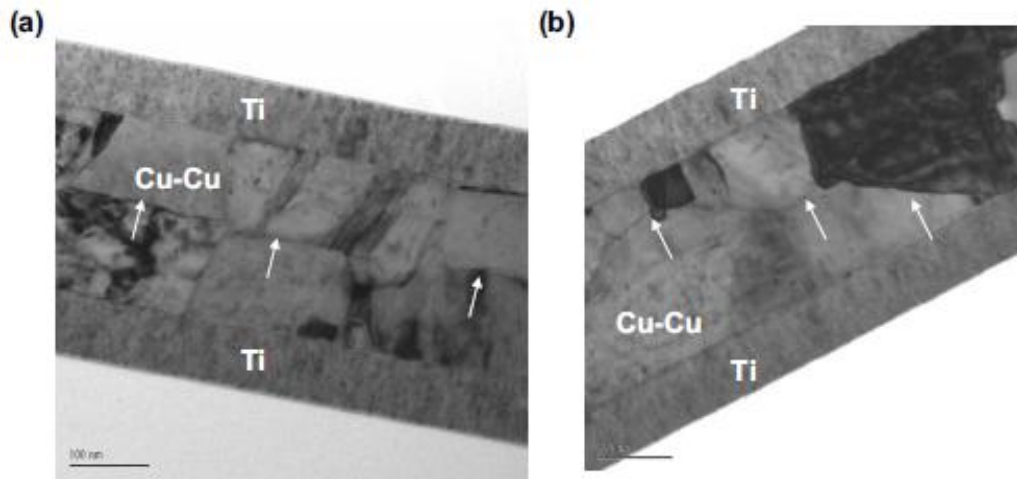
Cu-Cu bonding is a promising candidate as Cu has excellent scalability and electrical properties as a bonding medium. Research on Cu-Cu bonding has been attracting considerable attention in recent years. Thermo-compression bonding is often used for Cu-Cu bond formation under parallel application of heat and pressure. Bonding is typically performed at temperature range of 350-400°C [2.34, 2.35]. However, the development of low temperature process is needed for the thermal budget control as the pairing wafers are fully processed prior to bonding [2.36].

One of the low temperature Cu-Cu bonding methods is surface activation bonding (SAB), which makes use of argon (Ar) at ultra-low vacuum ( $10^{-7}$  Torr) to remove the surface oxide with energetic ions so that Cu-Cu can be bonded at room temperature, but this method is less manufacturing worthy [2.37]. CEA-LETI investigated room temperature hydrophilic Cu-Cu bonding with low root mean square roughness ( $< 0.5$  nm) and free particle contamination. The surface requirement may pose challenges to industrial applications due to the difficulties in achieving particle-free wafers [2.38]. In Figure 2.9, a method demonstrated by Ziptronix is a copper-based Direct Bond Interconnect (DBI), based on the difference in coefficient of thermal expansion (CTE) between Cu and oxide. Low temperature process is achieved by oxide-oxide bonding in the first place. Subsequently the bonded wafer is subjected to an annealing process, in which Cu compression is involved at bonding interface to form a good metallic bond [2.39].



**Figure 2.9:** Cross-sectional SEM image of copper DBI approach [2.39].

Based on the above reports, concerns are associated with surface oxidation, bonding uniformity, and low temperature bonding for thermal budget consideration. Therefore, a non-UHV and non-corrosive method is desirable to accomplish thermo-compression bonding at low temperature. An organic monolayer passivation has been studied for the application of Cu-Cu bonding. Self-assembled monolayer (SAM) of alkanethiol is applied on Cu surface to slow down Cu surface oxidation due to exposure in the clean room. This layer can be desorbed effectively by a proper annealing process. Bonded Cu layers present clear inter-diffusion and substantial grain growth after thermo-compression bonding, as shown in Figure 2.10 [2.40].



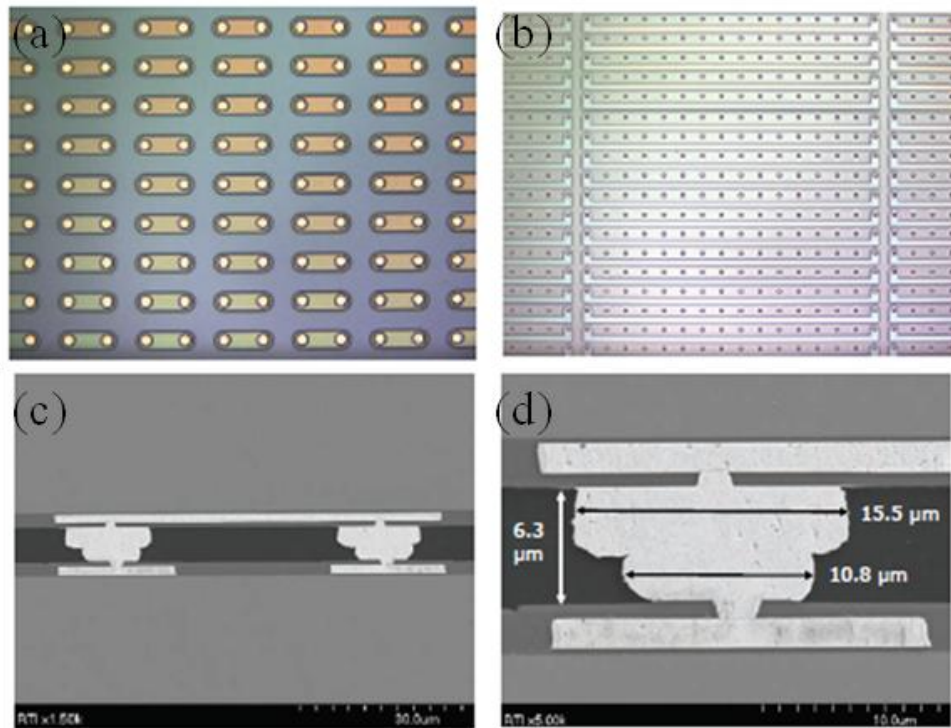
**Figure 2.10:** TEM micrographs of bonded Cu layers, (a) without SAM passivation (b) with SAM passivation and desorption prior to bonding [2.40].

### *2.6.2 Demonstrations of fine pitch Cu-Cu bonding*

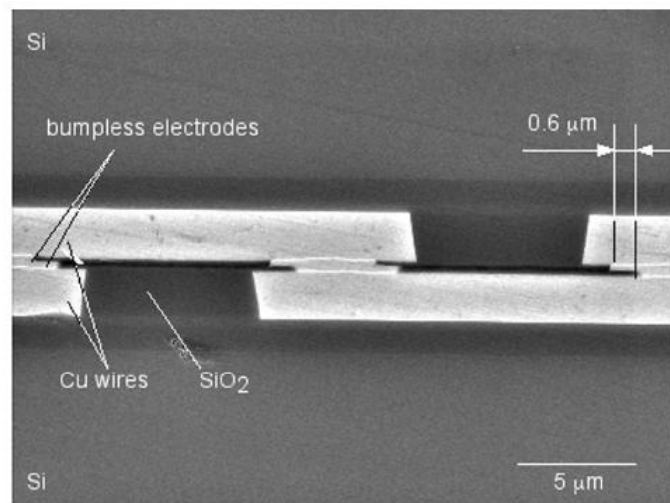
Local on-chip interconnects for 3-D ICs require a high interconnect density which needs to be realized in bonding technology. Cu-Cu bonding has a promising scalability and it can provide  $< 20 \mu\text{m}$  of pitch size. Several studies have been carried out for high density Cu-Cu bonding at narrow pitch using flip-chip bonder. Wafer-to-wafer bonding requires more stringent process control when the pitch size is small.

Research Triangle Institute (RTI) [2.41] has demonstrated high density Cu-Cu bonding daisy chain ( $50 \mu\text{m}$  pitch) with 176 interconnects, as shown in Figure 2.11. Flip chip bonding is used and bonding parts are cleaned in a weak sulfuric acid solution for surface oxide removal. At bonding temperature of  $300 \text{ }^\circ\text{C}$ , the result shows a continuous and a reliable electrical connectivity. In particular, characterizations of both Cu-Cu, Cu/Sn-Cu are performed and compared. Higher

mechanical strength of Cu-Cu bonds is observed, suggesting a more reliable option for the integration of heterogeneous materials.



**Figure 2.11:** Daisy chain of high density Cu-Cu bonding. (a) Optical micrograph of device array. (b) Daisy chain of test structure. (c) Cross-sectional image of Cu-Cu bonds. (d) Dimensions of Cu-Cu bond [2.41].



**Figure 2.12:** FIB SEM image of Cu-Cu bonds by SAB method [2.43].

*Suga et al.* [2.42] explored the formation of Cu-Cu bonds at room temperature by the surface-activated (SAB) method. An integrated SAB flip-chip bonder is invented with high alignment accuracy in ultra-high vacuum (UHV) condition ( $10^{-7}$  Torr). This allows for prevention of surface oxide generation at a critical vacuum pressure. In addition, Cu electrodes are developed using damascene process and reactive ion etching (RIE). 100,000 bump-less electrodes are formed with the bonding electrodes of 3  $\mu\text{m}$ , as shown in Figure 2.12 [2.43].

## **2.7 Summary**

In this chapter, an overview of 3-D technology is presented. TSV is the key technique that differentiates 3-D IC integration from 3-D packaging, providing performance improvement in various aspects. The stacking of ICs can be achieved by a bottom-up process from a single substrate or integrating multiple ICs via C2C, C2W and W2W. W2W stacking is preferred in a manufacturing perspective with better throughput. Various bonding mediums are discussed with different features. Metal-to-metal bonding system enables both electrical conduction and mechanical support for 3-D ICs. Cu-Cu bonding is favourably compared with solder micro-bump for better scalability and reliability. Different Cu-Cu bonding techniques are reviewed to achieve a robust bond at low bonding temperature. SAM passivation offers a promising advantage of suppressing surface oxidation prior to bonding. Finally, reports of high density Cu-Cu contacts are presented. Hence, potential application of W2W fine pitch Cu-Cu bonding by surface passivation is interesting to be explored.

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Chapter 2- Overview of 3-D IC Technology

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## **Chapter 3**

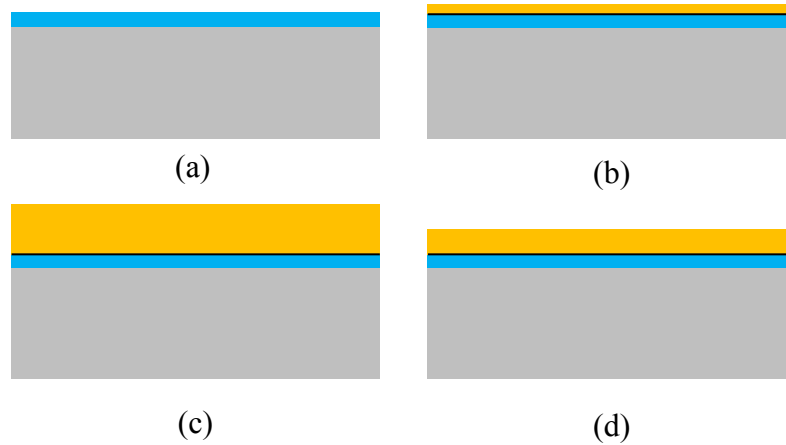
# **Fundamental Study of Thermo-compression Cu-Cu Bonding**

### **3.1 Introduction**

In this chapter, key parameters of wafer-to-wafer (W2W) thermo-compression Cu-Cu bonding are investigated and discussed. Different interfacial behaviours of Cu-Cu bonds are observed. In particular, the fundamental effect of microstructural evolution of Cu grains towards the bonding process is systematically studied. A surface passivation method using self-assembled monolayer (SAM) is introduced to prevent Cu surface oxidation and particle contamination prior to bonding (courtesy of D. F. Lim). Hence, it facilitates low temperature bonding which is desired to minimize the thermal stress induced for 3-D ICs. On the other hand, the hermetic properties of seal ring formed by Cu-Cu bonding are studied with the aim to examine its effectiveness of environmental protection (courtesy of J. Fan). The passivation method and hermetic seal proposed are integrated into the fine-pitch Cu-Cu bonding process, which will be described in the following chapters.

### **3.2 Thermo-compression Bonding of Blanket Copper Wafers**

The fundamental analysis of Cu-Cu bonding formation is studied based on blanket Cu wafers, and using standard Cu damascene process. In the fabrication, we used 200 mm *p*-type Si-(100) test wafers as the starting substrate. Firstly, the wafers were deposited with 100 nm silicon dioxide (SiO<sub>2</sub>) and 100 nm silicon nitride (SiN) using a plasma-enhanced chemical vapor deposition (PECVD) process (Figure 3.1 (a)). After that, a physical vapor deposition (PVD) system was used to sputter ~25 nm of tantalum nitride (TaN) and ~150 nm of Cu seed layer on top of the SiN layer (Figure 3.1 (b)). TaN served as a barrier to prevent Cu diffusion into Si and at the same time, provided better adhesion between Cu and the dielectric layer. Following, the wafers were transferred for electro-chemical plating (ECP) to grow another ~1 μm of Cu layer. In order to stabilise the grain growth in the Cu layer, Cu-annealing furnace was used to anneal the wafers at 200°C in N<sub>2</sub> ambient for 30 minutes (Figure 3.1 (c)), before the Cu layer was thinned down to ~ 300 nm by chemical-mechanical polishing (CMP) (Figure 3.1(d)). A number of key parameters of the Cu wafer surface are vital prior to bonding, and they affect the final bonding quality. They are namely, wafer planarity, surface roughness and surface cleanliness.

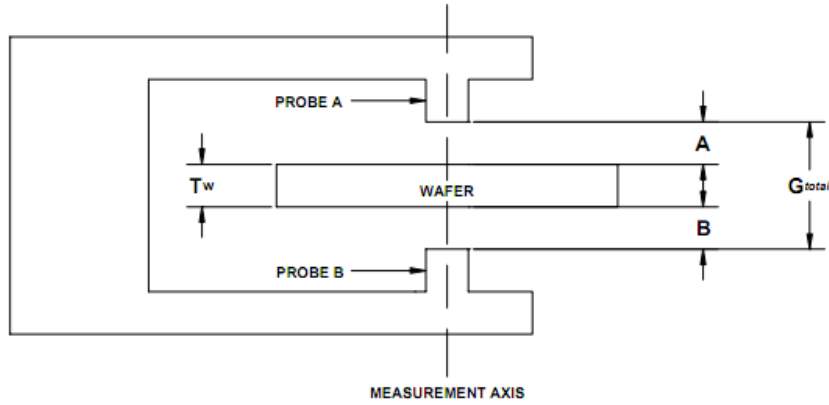


**Figure 3.1:** Process schematic of blanket Cu wafers prior to bonding. (a) Si substrate with the deposition of dielectric layers. (b) Deposition of the barrier layer and the Cu seed layer. (c) Cu ECP and Cu anneal. (d) Cu CMP.

### *3.2.1 Wafer planarity*

In a wafer-to-wafer bonding scheme, wafer planarity plays a critical role in forming reliable bonds in a wafer scale as it determines the initial contact uniformity of the wafer prior to thermo-compression bonding [3.1]. With a tight control of wafer planarity, the requirement of high temperature/ pressure process can be relaxed without necessary reinforcement to make an intimate contact between the pairing wafers. There are three important measures of wafer's flatness, including total thickness variation (TTV), wafer bow and warp. These can be used to gauge different perspectives of thickness deviation.

Total thickness variation (TTV) is a thickness measurement approach, examining the difference between the maximum and minimum thickness probed across the wafer prior to bonding. As shown in Figure 3.2, when the total gap ( $G_{total}$ ) and both air gaps ( $A$  and  $B$ ) between the probes and the wafer are acquired, the wafer thickness at the specific point is calculated as follows:



**Figure 3.2:** Measurement setup for calculation of total thickness variation (TTV) [3.2].

$$T_w = G_{total} - (A + B) \quad (3.1)$$

The measurement is taken at a number of points across the wafer. The accuracy of TTV significantly relies on the number of measurement locations. Based on the thickness data, TTV can be expressed as follows:

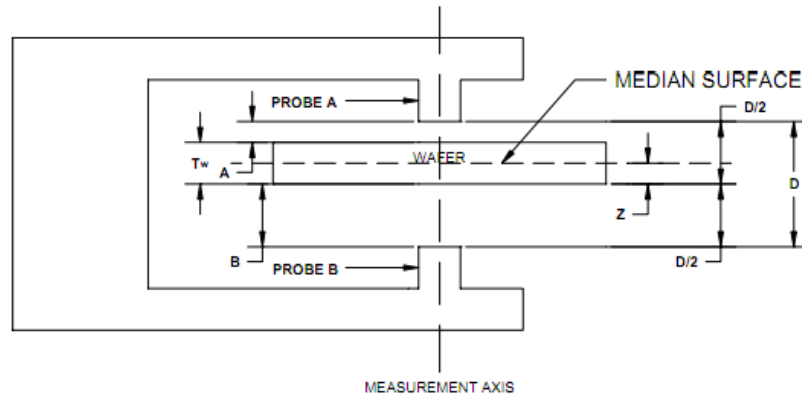
$$TTV = T_{max} - T_{min} \quad (3.2)$$

Wafer bow measurement determines the deviation of the center point of the median surface of a free, unclamped wafer from the median surface reference plane established by three points equally spaced on a circle with a diameter a specified amount less than the nominal diameter of the wafer. As shown in Figure 3.3, at any random point on the wafer,  $Z$  can be expressed in the following equations (3.3):

$$Z = D/2 - A - T/2 \text{ and } Z = -D/2 + B + T/2 \quad (3.3)$$

Based on equation (3.3), wafer bow ( $Z$ ) can be extracted as:

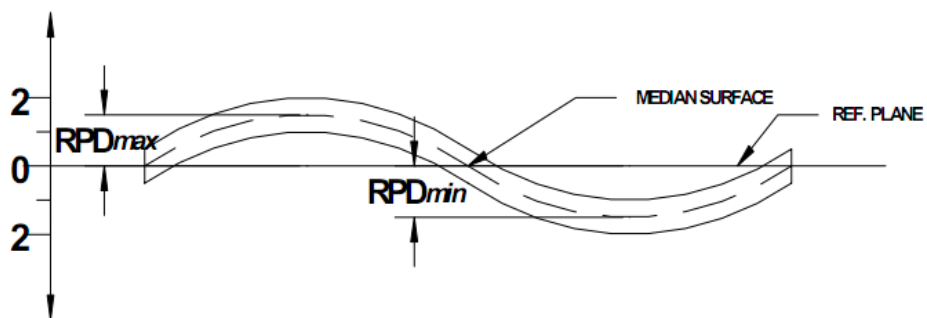
$$Z = (B - A)/2 \quad (3.4)$$



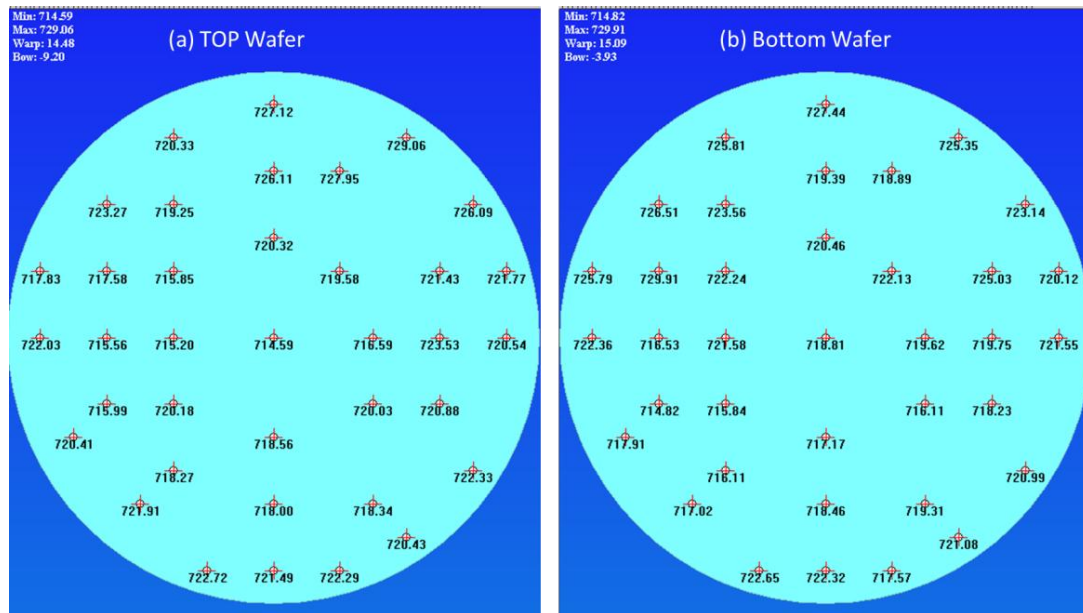
**Figure 3.3:** Measurement setup for calculation of wafer bow [3.3].

As shown in Figure 3.4, with respect to a reference plane, the differences between the positive and negative dislocations of the median surface represent wafer warp, which can be calculated by equation (3.5):

$$\text{Warp} = RPD_{max} - RPD_{min} \quad (3.5)$$



**Figure 3.4:** Schematic of wafer warp acquirement [3.4].



**Figure 3.5:** Wafer map of 37-point thickness measurement with the extraction of thickness deviation for both pairing wafers.

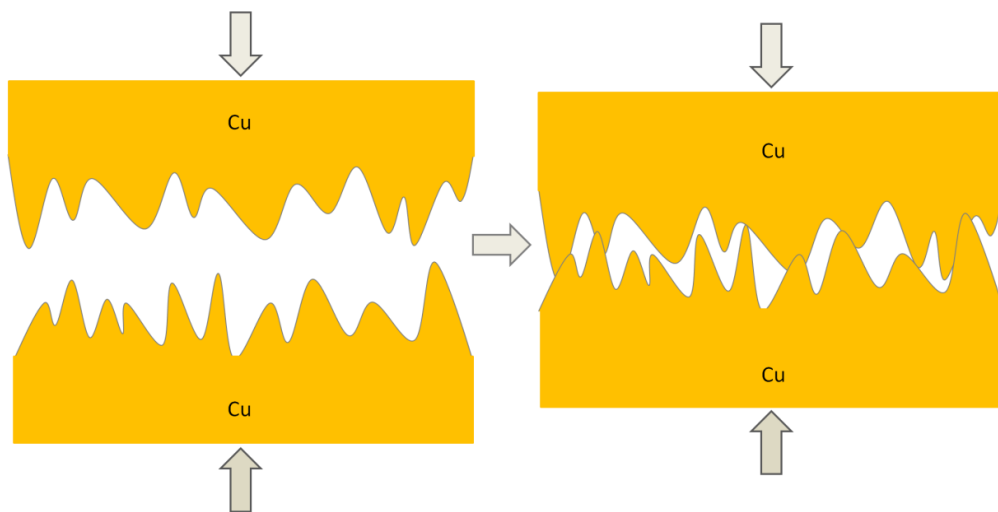
As the Cu layers to be bonded are in the range of a few micrometers, stringent requirement of wafer uniformity is needed for both pairing wafers prior to the bonding process. Figure 3.5 shows a 37-point thickness measurement in which TTV, wafer bow and wafer warp are extracted accordingly. All parameters need to be tightly controlled at  $\sim 10\mu\text{m}$  ( $< 3\%$  of the wafer thickness) to suppress the bonding issues induced by non-uniform wafers [3.5].

### 3.2.2 Surface roughness

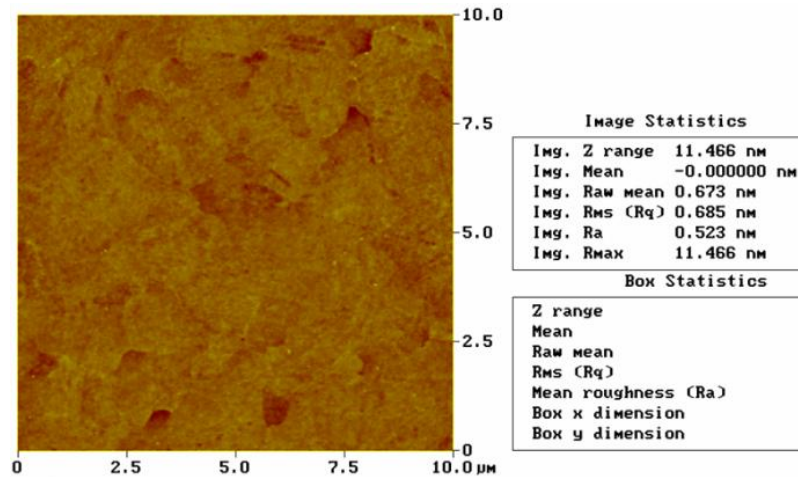
Microscopic roughness is always present on any “perfect” surface. During thermo-compression bonding, both surfaces of Cu wafers are in a direct contact. When modest conditions of bonding temperature and bonding pressure are applied, Cu films

with a high surface roughness are more difficult to fuse into each other, as shown in Figure 3.6, As a result, micro voids will be formed at the interface after the bonding process. Consequently, they will deteriorate the reliability of the bond for the stacked layers. Therefore, the degree of surface roughness significantly affects the bonding quality as it determines the total contact area which in turn limits the inter-diffusion of the Cu atoms.

Cu CMP is a main process that affects the surface roughness as it involves both mechanical thinning and chemical etching to the target layer. The guideline should be that the surface roughness be controlled below 1 nm, in order to provide for a successful bonding. The roughness analysis is performed using atomic force microscopy (AFM). Shown in Figure 3.7, the root-mean-square (rms) Cu surface roughness of the processed wafer is estimated to be 0.685 nm after Cu CMP.



**Figure 3.6:** Schematic of thermo-compression Cu-Cu bonding process. The quality of the bond is limited by surface roughness.



**Figure 3.7:** AFM scan of Cu with an area of  $10\ \mu\text{m} \times 10\ \mu\text{m}$ .

### 3.2.3 Surface cleanliness

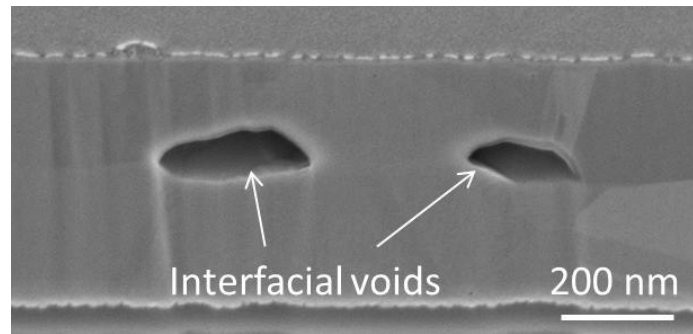
When a clean Cu film is exposed to ambient atmosphere, a native oxide can be readily formed on the Cu surface. Despite the Cu wafer being processed with tight control prior to bonding, a brief exposure in the ambient is all it needs to form a layer of oxide at the Cu-Cu interface; the presence of the oxide in turns, affect the bonding quality detrimentally. In addition, oxygen incorporated between the bonded layers will result in a higher resistance, which has an adverse effect on the electrical properties of the vertical interconnection. Therefore, a cleaning step is usually employed to remove the surface oxide prior to bonding. This can be done either using acid clean or forming gas anneal [3.6, 3.7]. Nonetheless, as there is no available *in-situ* cleaning process, surface oxide can still be re-grown during the subsequent alignment and transfer processes before bonding. Hence, a high bonding temperature is inevitably needed to make effective Cu inter-diffusion in order to overcome the barrier of surface oxide during Cu-Cu bonding process. On the other hand, reduction in the bonding temperature could be done if the Cu is oxide-free through some treatment without changing its surface properties.

### **3.3 Bonding Quality Study**

When the pre-bonding process was completed, the blanket Cu wafers were aligned face-to-face (F2F) and clamped together in a bond chuck, separated by three 30  $\mu\text{m}$ -thick metal flaps. The bond chuck was then transferred to a bonding chamber (EVG 520), in which a moderate pressure of  $\sim 1$  MPa was used and the bonding temperature was varied from 350  $^{\circ}\text{C}$  to 400  $^{\circ}\text{C}$  for several wafer pairs in order to observe different interfacial behaviors of bonded Cu layers. *Chen et al.* [3.8] indicated that different bonding observations may occur during thermo-compression Cu-Cu bonding. In the following, similar findings are presented after blanket wafer bonding.

#### *3.3.1 Interfacial void*

It is observed that at a high bonding temperature, large interfacial voids are usually present at the bonding interface, as shown in Figure. 3.8. This is in accordance with reported results from *Tan et al.* [3.9], suggesting that the formation of void comes from the thermal relaxation of Cu grain growth, when Cu atoms transferred in order to gain more stable phases. Therefore, localised voids are formed when the bonded wafer experience drastic change in the temperature from the high temperature bonding process to the room ambient when the process is completed. Though high temperature process improves the bondability of the system, accompanied voids generation may deteriorate the bonding reliability in the long term operation.

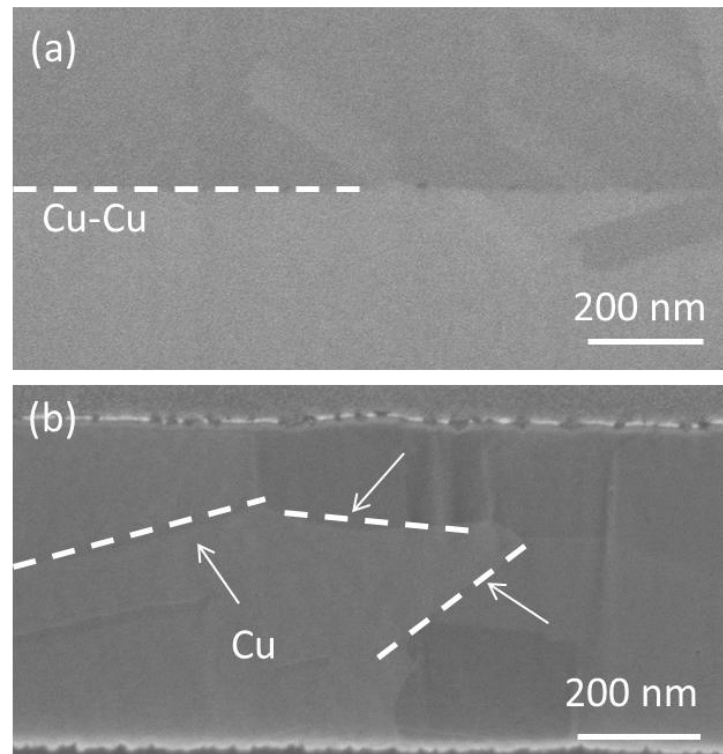


**Figure 3.8:** SEM image of bonded Cu layer with void formation at bonding interface.

### *3.3.2 Interface appearance*

As shown in Figure 3.9 (a), a clear Cu-Cu interface is observed when insufficient energy is obtained for Cu atoms to diffuse across the interface. Sometimes, it may also occur when there is either a high surface roughness or an oxide layer at the bonding interface, thus creating a barrier to prevent Cu grain growth to extend across the interface. The bonded layer is still less reliable as compared to a homogeneous Cu bond due to potentially a higher interface resistance and a weaker bonding strength.

Using high temperature or high pressure, we can maximize the total contact area with sufficient thermal energy to activate Cu atoms which substantial Cu inter-diffusion takes place between two wafers, and the Cu grains will extend to the other Cu film to form a seamless interface. Shown in Figure 3.9 (b), the original bonding interface of both Cu films is no longer seen and it suggests a successful Cu-Cu bonding process.



**Figure 3.9:** FIB images of two types of interface appearance: (a) Clear bonding interface; (b) Zigzag interface with substantial inter-diffusion across bonding interface.

### *3.3.3 Interface contamination*

When the oxidized Cu is present at the bonding interface, it potentially gives rise to mechanical issues as shown in Figure 3.10. An oxygen-rich bonding interface is clearly observed using electron energy loss spectroscopy (EELS), and the bonded layer splits into two layers along the interface oxide. The oxidized Cu ( $\text{Cu}_2\text{O}$  or  $\text{CuO}$ ) is more brittle and mechanically more unstable as compare to Cu. As a result, interfacial support is degraded for the stacked layers with the presence of surface oxide during the bonding process.

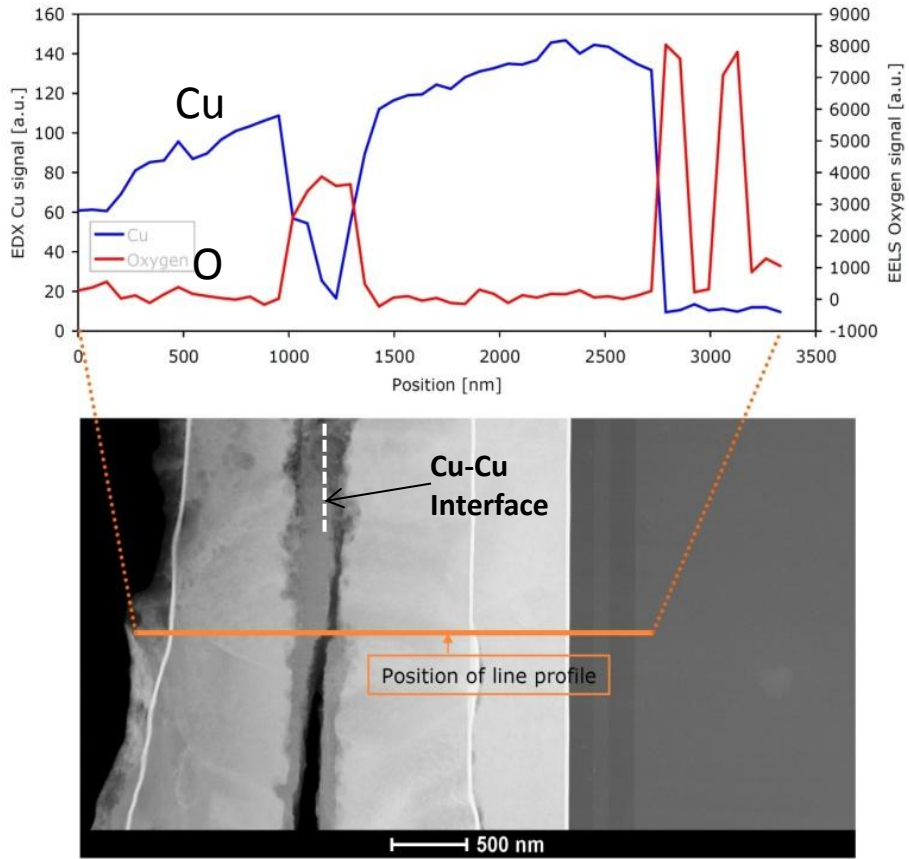


Figure 3.10: EELS analysis of composition of Cu and O across the bonded layer.

### **3.4 Micro-structural Evolution of Cu Grains**

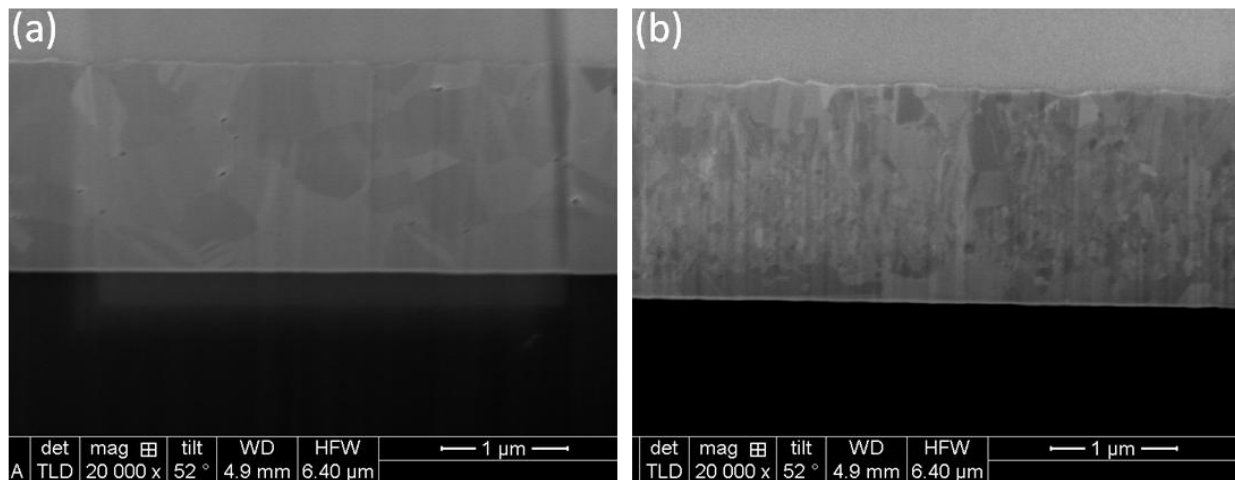
It is widely accepted that the mechanism behind thermo-compression bonding of two Cu films held in intimate contact is based on Cu inter-diffusion and grain growth across the bonding interface. In principle, it is energetically more favourable for smaller Cu grains to grow, coalesce and form larger grains. Therefore, it can be postulated that Cu film with a smaller initial grain size undergoes a higher rate of transformation to form larger grains across the interface during thermo-compression bonding. Hence, this can potentially result in a higher quality of the Cu-Cu bond. On the other hand, Cu film with a larger initial grain size experiences limited growth across the interface during thermo-compression bonding and one can expect a Cu-Cu bond with poorer quality. In the mainstream silicon back-end processes, Cu films are often annealed to stabilize the grain size, with an aim to improve the electrical properties. As a result, large Cu grains in these Cu films are expected to limit the grain growth during the bonding process.

When wafer level 3-D ICs are stacked during the back-end processes using bump-less Cu films, clear understanding of the effect of pre-bonding anneal and initial Cu grain size on the final Cu-Cu bond quality is essential for process optimization. While various reports on Cu-Cu bonding have been focused on the effectiveness of bonding temperature and post-bonding anneal [3.6, 3.10, 3.11], there has been a lack of systematic investigation on the effect of pre-bonding anneal. In this section, Cu grain morphology prior to bonding and its effect on the overall bonding quality are investigated.

*3.4.1 Experimental*

A batch of 200 mm *p*- type Si-(100) test wafers were used as the starting substrate in this experiment. Initially, the wafers were deposited with a 100 nm SiO<sub>2</sub> layer and a 100 nm SiN layer, respectively. Subsequently, PVD system was used to sputter a 25 nm TaN layer and a 300 nm Cu layer on top of the SiN layer. Thereafter, the wafers were separated into two groups: (1) the first group of wafers was subjected to a pre-bonding anneal process at 300 °C in nitrogen (N<sub>2</sub>) ambient for 1 h, and (2) the second group of wafers was used for bonding without additional processing. It is worthwhile to point out that in conventional silicon back-end processes, a post Cu-deposition anneal is often applied to enhance the grain growth which in turn improves the electrical properties of the Cu film.

The initial Cu grain morphology just before the bonding was analyzed using a combination of focus ion beam and scanning electron microscopy (FIB-SEM). When the Cu layer is subjected to the pre-bonding anneal, the Cu grains grow substantially and a grain size of > 0.3 μm is achieved as shown in Figure 3.11 (a). However, Figure 3.11 (b) shows that the fresh Cu layer without the pre-bonding anneal has a Cu grain size of < 0.3 μm. It can be expected that due to the smaller grain size, substantial inter-diffusion and higher growth rate of the Cu grains across the interface would occur during bonding.



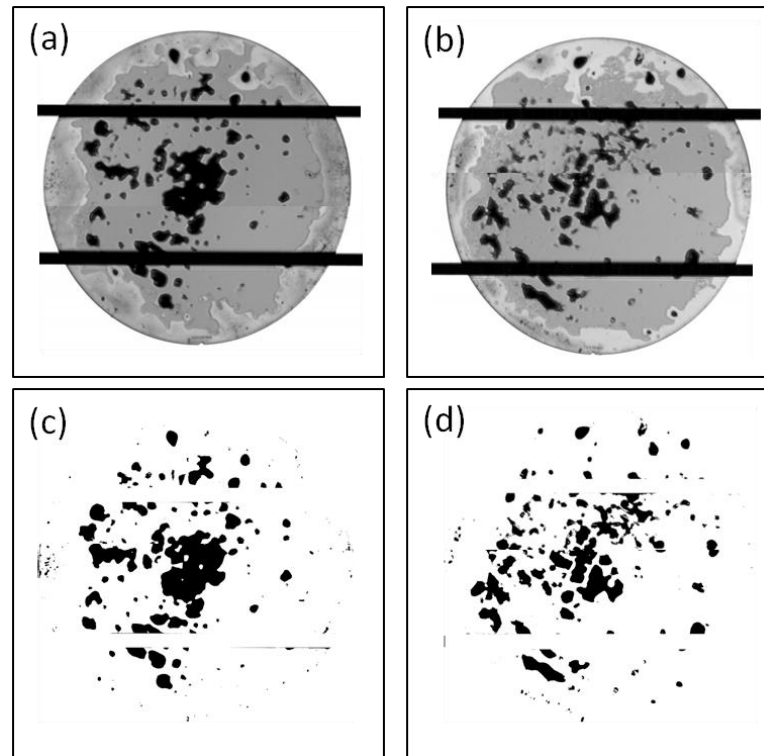
**Figure 3.11:** Cross-sectional FIB-SEM images of the Cu layer prior to bonding: (a) with a pre-bonding anneal, and (b) without a pre-bonding anneal.

The pairing wafers were then brought together into contact for thermo-compression bonding. The wafer pairs were bonded with a bonding pressure of ~300 kPa at 300 °C for 1 hr in vacuum (~1e-4 mbar). Following that, the wafers were sent for N<sub>2</sub> batch anneal at 350 °C for another 1 hr to enhance the Cu-Cu bond strength. Based on a previous study, a bonding temperature of 300 °C is the lowest threshold in order to obtain a well bonded Cu-Cu layer using thermo-compression bonding without any special surface treatment. Hence, this experiment is designed to aid the study on the effect of pre-bonding anneal on the Cu-Cu bond quality.

### *3.4.2 Results and discussion*

C-mode scanning acoustic microscopy (*c*-SAM) was used to estimate the effective Cu-Cu bonding area. Figure 3.12 (a) and (b) present the *c*-SAM images of the bonded wafer pairs with and without a pre-bonding anneal, respectively. The two

horizontal lines are artifacts originated from the two bars that were used to hold the wafers during imaging. Random patches with darker tone are found across the entire wafer with higher concentration near the center of the wafer. These patches indicate the possible locations of voids formation as a result of failure in the Cu-Cu bonding. The discolored grey regions at the wafer edge represent areas that are poorly bonded as compared to the grey color regions closer to the wafer center. The overall large void area reflects the fact that the two mating wafers are merely bonded at 300°C without special treatment. In order to compare the true bonding area more accurately, void area is isolated from the *c*-SAM images by GIMP software and followed by void area calculation by means of pixel counting using ImageJ software. Figure 3.12 (c) and (d) show the processed images of Figure 3.12 (a) and (b), respectively. Based on these images, the void area is estimated to be ~5,268.71 mm<sup>2</sup> and ~4,197.38 mm<sup>2</sup> respectively for both images. This analysis indicates that a ~20.3% reduction in void density is obtained when the pre-bonding anneal is not employed on the Cu films.

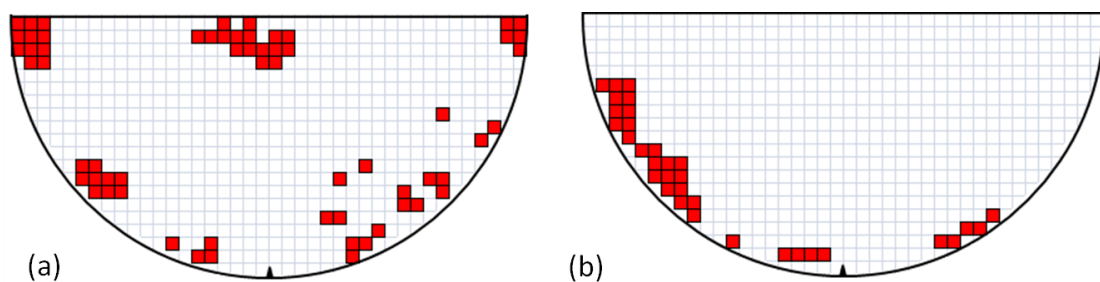


**Figure 3.12:** (a) *c*-SAM image of the bonded wafer with pre-bonding annealing. (b) *c*-SAM image of the bonded wafer without pre-bonding annealing. (c) and (d) are the corresponding interface void density quantification by void isolation and pixel counting.

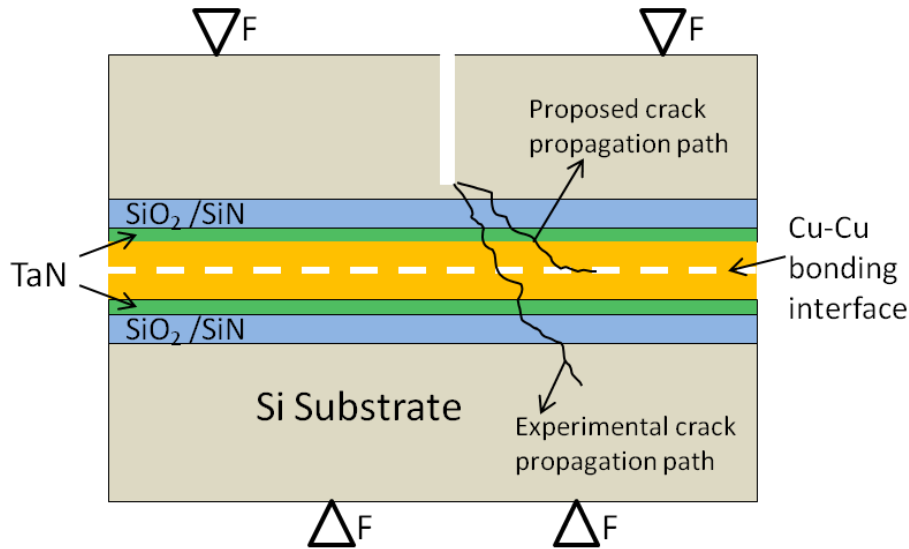
Subsequently, each of the bonding wafer pairs was diced into  $5 \text{ mm} \times 5 \text{ mm}$  samples to examine the dicing yield, as shown in Figure 3.13 (a) and (b). Since a high shear force is applied during wafer dicing, samples from poorly bonded area could potentially delaminate. In the region enclosed by a radius of 50 mm from the center origin of wafer, the dicing yield of the wafers with and without the pre-bonding anneal are 90% and 100% respectively. In the region outside the above wafer center, dicing yield decreases to ~75% and ~83% respectively. The wafer edge is particularly susceptible to contamination and damage during wafers handling, hence poorer Cu-Cu bond quality is expected. The results suggest that the pairing wafers without the

pre-bonding anneal have a higher proportion of regions that are better bonded as compared to the control wafers (with the pre-bonding anneal).

The remaining of the bonded samples are subjected to four-point bending test, which is used to measure the interface adhesion strength of the bonded Cu layers, as shown in Figure 3.14. The Cu thickness is intentionally kept low (300 nm) to minimize the effects of plastic energy dissipation that can affect the interpretation of the bonding results. A pre-machined notch serves as the stress concentration point for the origin of the crack. The crack propagates into the weak interface in the bonded stack and the steady-state value of the strain energy release rate will give the bond strength of the interface. However, the experimental crack propagates into the silicon substrate instead of the Cu-Cu bonding interface in most samples. Samples tested mainly breaks into half through the notch. The obtained bond toughness values are very high and this may due to the fact that the force measured has reached the silicon fracture limit. Therefore, results from four-point bending test do not accurately predict the real bonding strength, in this case.



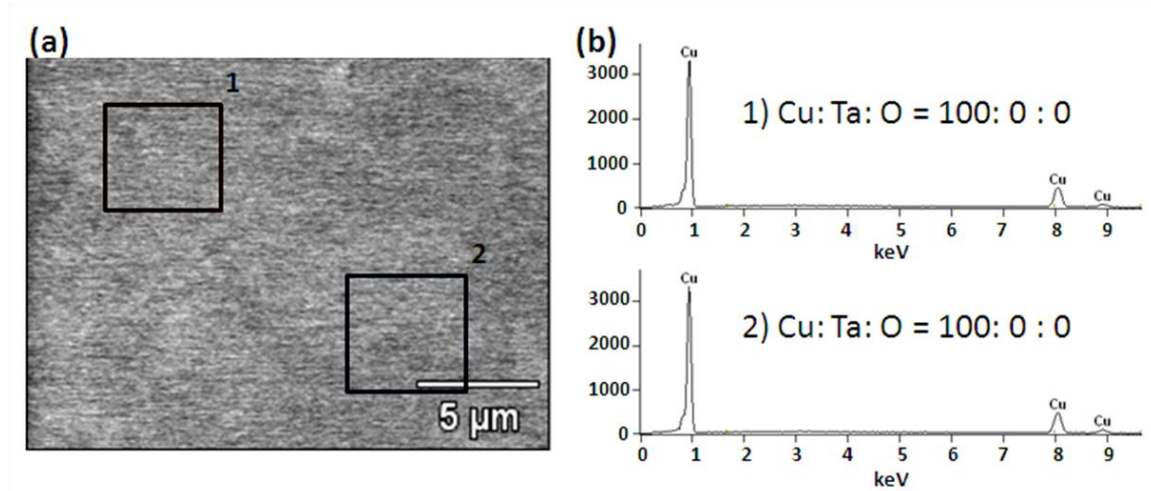
**Figure 3.13:** Dicing maps for (a) wafers with pre-bonding. (b) wafers without pre-bonding anneal.



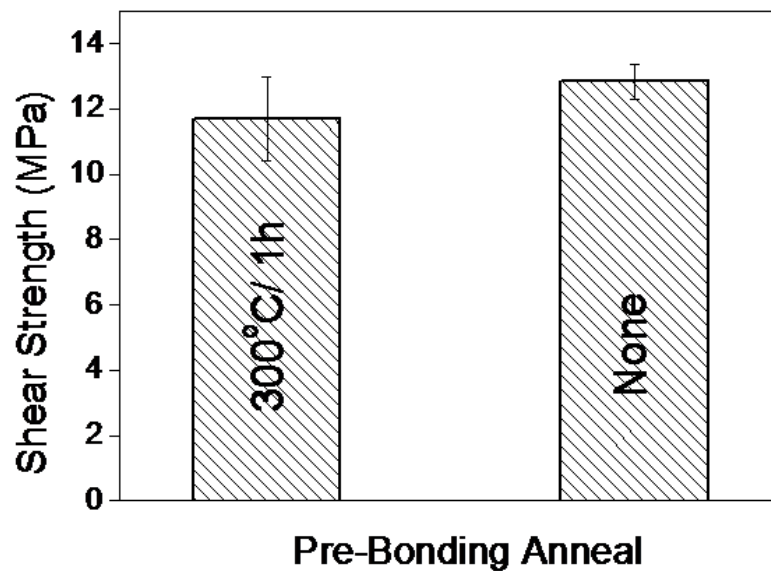
**Figure 3.14:** Schematic of the four-point bending test structure with the expected and actual crack propagation paths.

Since the results from *c*-SAM imaging and dicing only present qualitative view on the bond quality, the actual bond quality needs to be quantified against its actual mechanical strength. Hence, shear test was performed on the diced samples to determine the shear strength of the Cu-Cu bond. The test measured the maximum shear force that could be sustained by the bonded Cu-Cu layer before complete rupture. During the shear test, several failure modes could occur. These include Cu-Cu interface failure, Cu/TaN interface failure, and Si substrate failure. Therefore, energy dispersive X-ray spectroscopy (EDX) is used to identify the specific failure mode on each group of the samples. As shown in Figure 3.15 (a), the surface of the sample where the failure occurs is analyzed with EDX to identify the specific chemical composition on the surface to determine the respective failure mode. After that, the shear strength of the bonded samples that are solely due to Cu-Cu interface failure is compared for both groups (Figure 3.15 (b)). It is observed that there is ~8.9%

gain in the shear strength when the pre-bonding anneal is not applied as shown in Figure 3.16.

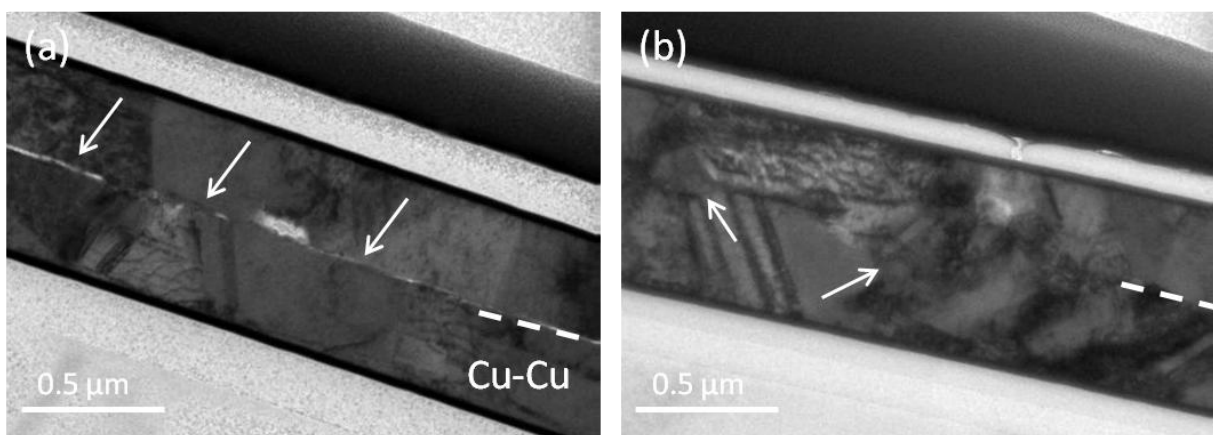


**Figure 3.15:** (a) Delaminated interface of the wafer pair after shear test. (b) EDX analysis of the surface composition.



**Figure 3.16:** Cu-Cu bond strength of both types of bonded wafer pairs with and without the pre-bonding anneal.

In order to explain the above observations, the bonded layers were examined using transmission electron microscopy (TEM). This analysis is essential to provide a close-up view on the Cu grain microstructure after bonding and this in turn, provides an explanation to the enhancement in the dicing yield and the shear strength when the pre-bonding anneal is not applied. TEM images in Figure 3.17 (a) and (b) are taken from wafers with and without the pre-bonding anneal respectively. In Figure 3.17 (a), a distinct Cu-Cu bonding interface (marked with arrow) is clearly observed when the Cu films are annealed prior to bonding. While there is substantial Cu grain growth (due to the heat treatment during pre-bonding anneal, bonding, and post-bonding anneal) in the in-plane direction, out-of-plane grain growth across the bonding interface is very limited. On the other hand, Figure 3.17 (b) shows that the Cu layers with no pre-bonding anneal fuses together to form a homogeneous final Cu layer. The bonded layer is seamless and the original bonding interface is distorted and a wiggling interface is vaguely seen. Substantial grain growth is observed in both in-plane and out-of-plane directions. This gives rise to a mechanically stronger Cu-Cu bond to withstand external force during the dicing and shear tests.



**Figure 3.17:** Cross-sectional TEM images of the bonded Cu layer: (a) with pre-bonding anneal (b) without pre-bonding anneal.

The microstructure of the bonded Cu layers observed from the above TEM analysis can be traced back to the initial Cu grain size prior to bonding on separate sets of un-bonded wafers as described above in Figure 3.11. Without the pre-bonding anneal, much smaller Cu grains tend to facilitate higher growth rate and stronger interaction of Cu atoms at the Cu-Cu contact area, resulting in a seamless bonding interface. It is also important to note that the in-plane Cu grain size after the bonding is comparable in both cases. During the bonding process, the initial smaller grain size (sample without pre-bonding anneal) has gone through a transformation into matured (i.e. larger) grains. Recent work has reported that the stress of the Cu film is the highest before any annealing process [3.12]. Owing to the stress relaxation of the initial Cu grains, they start to interact across the bonding interface as they grow, thus forming a seamless contact. As the Cu grains reach a certain stable size, stress relaxation is terminated and the grain interaction at the bonding interface is minimized. Hence, it is clear that a smaller initial Cu grains size is advantageous for the formation of better Cu-Cu contact as compared to the one with a larger initial Cu grain size. The change in the grain size, which in turn affects crystallographic texture, resistivity, hardness and stress, improves the final quality of the Cu-Cu bond [3.12, 3.13].

### *3.4.3 Conclusion*

The effect of the pre-bonding anneal on the Cu-Cu bond quality was investigated. Unlike the improvement seen with the post-bonding anneal, the pre-bonding anneal at 300 °C does not necessarily introduce better Cu-Cu bond. When the pre-bonding anneal is not employed, stronger growth and inter-diffusion of the small Cu grains takes place at the Cu-Cu interface during bonding, resulting in a seamlessly

### Chapter 3- Fundamental Study of Thermo-compression Cu-Cu Bonding

bonded Cu layer. This mechanism translates into ~8.0% higher dicing yield and ~8.9% bonding strength gain in the shear strength. In addition, the Cu-Cu bonding process as described in this work has a lower overall thermal budget, and therefore it is a more favorable option for future 3-D IC technology.

### **3.5 Self-Assembled Monolayer (SAM) Passivation**

#### *3.5.1 Introduction*

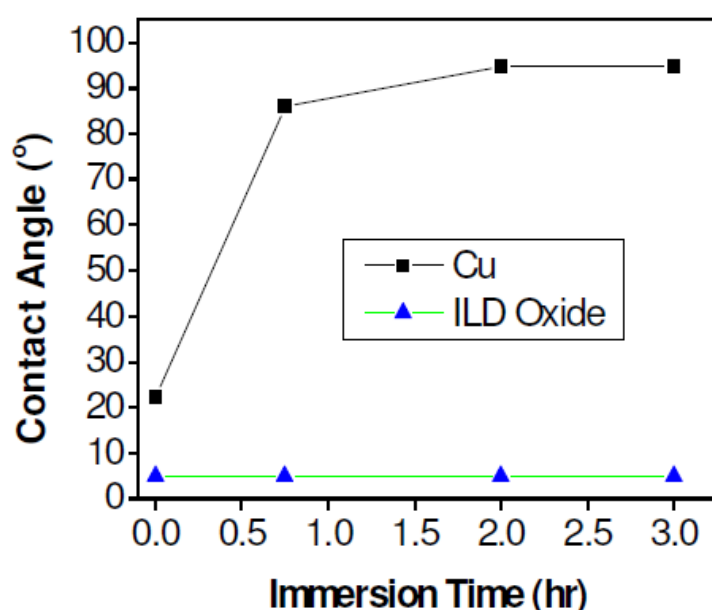
The limitation of obtaining a reliable low temperature Cu-Cu bonding primarily lies in the extent of Cu surface oxidation. Besides that, wafer level bonding requires more stringent process control as compared to that of chip-to-wafer or chip-to-chip bonding. One method is to remove the surface oxide with energetic ions and bond the Cu surfaces in ultra-high vacuum (UHV) ambient, but the manufacturing cost renders its application [3.14]. Oxide removal with wet cleaning such as acetic acid [3.14] has been used with some success. However, prolonged immersion in acetic acid results in the etching of the Cu layer, hence making process control challenging. Therefore, a non-UHV and non-corrosive method is desirable to accomplish thermo-compression bonding at low temperature. The feasibility of applying a self-assembled monolayer to passivate Cu surface for bonding enhancement at low temperature is examined by our research group. In the following, the fundamental study of the effect of SAM passivation on Cu-Cu bonding is presented based on 6 inch wafers with blanket Cu layers (Courtesy of D. F. Lim).

#### *3.5.2 Effect of SAM passivation on blanket Cu wafers*

Wafers used in this study are *p*-type 150 mm Si-(100) test wafers with resistivity in the range of 3-50  $\Omega\text{cm}$ . Wafers were first cleaned with standard RCA then followed by thermal oxidation to form 500 nm thick of silicon dioxide. Next, Piranha clean ( $\text{H}_2\text{O}_2:\text{H}_2\text{SO}_4 = 1:1$ ) was performed for pre-metal cleaning. Metal deposition was done successively for ~75 nm of Ti (as Cu diffusion barrier) and ~100 nm of Cu. As-

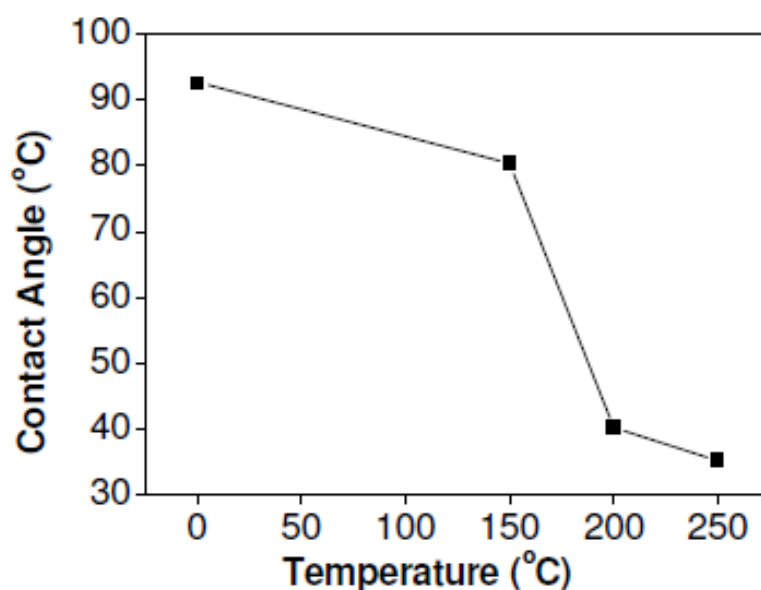
sputtered Cu wafers were immersed into alkane-thiol solution which contains 1mM of 1-hexanethiol with 95% that is diluted in ethanol and stored in nitrogen-purged dry box. The solution was maintained at room temperature during immersion. After a specific time interval, Cu wafers were taken out and rinsed with copious amount of ethanol to remove the unabsorbed molecules and blown dry with N<sub>2</sub> gas.

SAM formed by linear alkane-thiol molecules [CH<sub>3</sub>-(CH<sub>2</sub>)<sub>n-1</sub>-SH, n = number of carbon] are readily absorbed onto the Cu surface. The thiol (-SH) head groups bind to Cu and form a densely packed monolayer on the Cu surface. The methyl (-CH<sub>3</sub>) tail groups make the surface hydrophobic. SAM monolayer protects the Cu surface from surface contamination and oxidation resulting in better bonding uniformity. SAM formation is highly selective on Cu and it has no effect on ILD layer (Figure 3.18). The SAM formed are able to retard Cu surface from oxidation and protect Cu surface from contaminants, thus making it an excellent candidate to passivate the Cu surface prior to bonding.

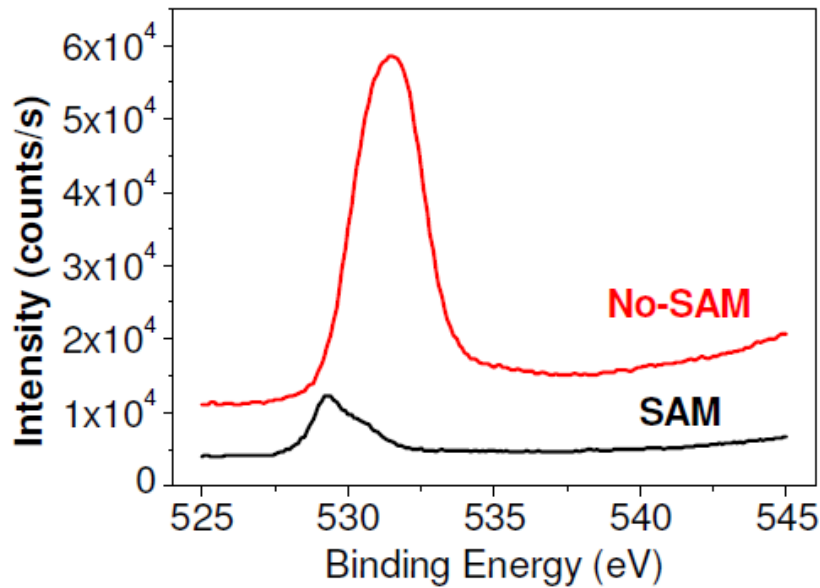


**Figure 3.18:** Cu surface is passivated by SAM and turns hydrophobic, while ILD oxide is not affected.

The pairing wafers were then aligned F2F and transferred into the bonding chamber. Prior to bonding, pre-bonding anneal of the wafers is carried out at different temperatures to evaluate the effectiveness of *in-situ* desorption of SAM. At 250 °C and above, the contact angle is significantly reduced as shown in Figure 3.19. Hence, a complete desorption of SAM provides a clean Cu surface for subsequent thermo-compression bonding. XPS surface analysis is performed to quantify the O content on Cu film and the result is shown in Figure 3.20. Cu wafer with SAM passivation shows lower O content after 12 days exposure in ambient hence confirming its ability to retard surface oxidation.



**Figure 3.19:** SAM can be thermally desorbed effectively with annealing at temperature > 200 °C. Annealing time is ~30 min.



**Figure 3.20:** XPS analysis on the oxygen content on Cu surface after 12 days of exposure in ambient (25 °C, ~50%RH). Blanket Cu with no SAM passivation shows significant presence of surface oxygen, and this is successfully suppressed with SAM passivation.

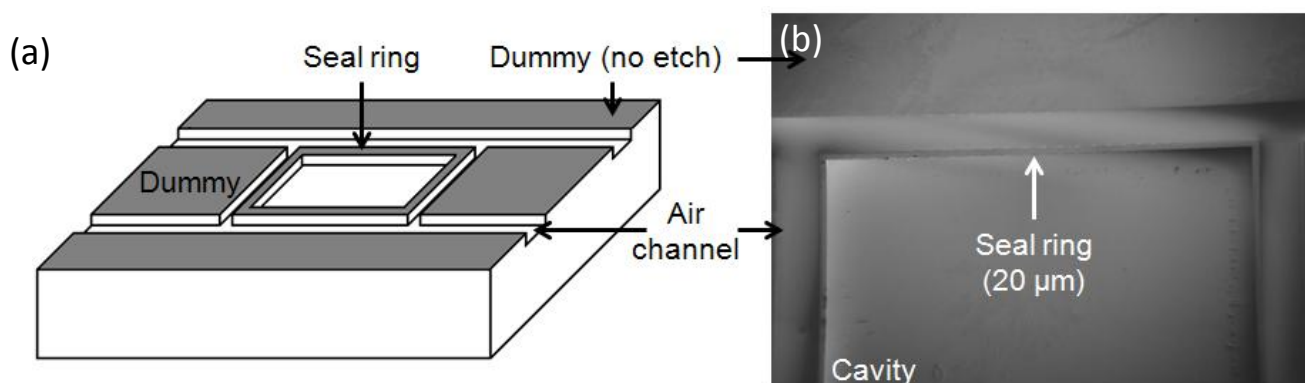
### *3.5.3 Application of SAM passivation into high density Cu-Cu bonding process*

The use of SAM passivation suppressed surface oxidation for blanket Cu wafers bonding. Therefore it is more interesting to explore the integration of this enhancement method into actual 3-D application where high density Cu-Cu bonds are implemented. Electrical performance and mechanical reliability are of greater focus for a potential technology development. In the following chapters, we will discuss the integration scheme in terms of characterizations of different test vehicles.

### **3.6 Hermeticity of Cu-Cu Bond**

It has become increasingly noticeable that the performance of micro- and nano-scale devices can be easily impeded and degraded by particles and impurities. Hence, it becomes critical that such systems, with long shelf lives of over 20 years, operate in a strict and controlled environment. Wafer level hermetic encapsulation for 3-D IC is important to provide the desired ambient for long term operation, and to protect these devices/structures against the harsh environment such as particle, moisture and acid/base corrosion. Though limited work has been reported using Cu-Cu bond as hermetic seal, the potential applications can be achieved through its robust bond quality after careful processing.

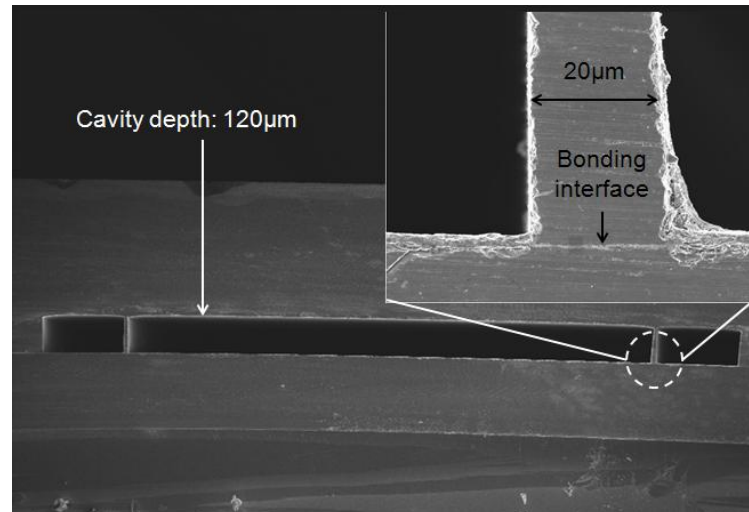
To quantify the hermeticity of Cu-Cu bond, a standalone and non-functional structure (sealed cavity) is designed and fabricated to characterize hermetic encapsulation using thermo-compression Cu-Cu bonding. Prior to bonding to a blanket Cu wafer, the cavity structure surrounded by a Cu seal ring is needed as shown in Figure 3.21 (a). The bonding medium consists of Cu (300 nm) bonding layer and Ti (50 nm) barrier layer. The width of the seal ring is 20  $\mu\text{m}$ . During bonding, the wafer pair was brought into contact under a contact force of 5500 N and held at 300  $^{\circ}\text{C}$  for 1 hour in vacuum ambient ( $\sim 2.5 \times 10^{-4}$  mbar). The sealed volume for helium bomb test based on MIL-STD-883E standard (method 1014.10) requires a volume larger than  $10^{-3} \text{ cm}^3$  as indicated by *Tao et al.* [3.15]. Therefore, all cavities were designed and etched to a volume of  $1.4 \times 10^{-3} \text{ cm}^3$  with a depth of 120  $\mu\text{m}$ . In the post-bonding process, the dummy area was diced, and the individual chip with sealed cavity is ready for hermetic testing.



**Figure 3.21:** (a) Schematic of the structure for hermetic encapsulation, (b) SEM image of the fabricated structure prior to bonding,

The cross-sectional SEM image of the sealing structure bonded with Cu is shown in Figure 3.22. A close-up view showing the bonding of the seal ring and the capping wafer is included in the SEM image on the upper right. This structure is used to study the properties of Cu-Cu hermetic seal ring. The bonding interface is clearly marked with an arrow and no void is observed. Helium leak rate measurement based on the specifications defined in MIL-STD-833E standard (method 1014.10) is employed for hermetic sealing test. The test begins by placing the samples in a chamber filled with helium gas at a pressure of 75 Psi (~0.52 MPa) for an exposure time of over 2 hr (“helium bombing”). Then, the samples are unloaded from the bombing chamber followed by helium leak test using a mass spectrometer. Table 3.1 lists the helium leak rates detected for the sealed cavities with a seal ring which has a width of 20 μm. The maximum helium leak rate detected is  $1.6 \times 10^{-9}$  atm.cm<sup>3</sup>/sec, which is ~30X smaller than the reject limit ( $5 \times 10^{-8}$  atm.cm<sup>3</sup>/sec) prescribed by the MIL-STD-883E standard [3.16]. Hence, this shows an excellent result for hermetic seal application. In real applications, the Cu seal ring will effectively shield the internal device and interconnect from environmental corrosion during the bonding

process. It is worth pointing out that having a Cu ring designed at the peripheral can also promote the overall mechanical robustness of the structure. Therefore, it is expected that the integration of Cu seal ring will enhance the overall reliability of Cu-Cu stacking in 3-D IC application.



**Figure 3.22:** Cross-sectional SEM image of cavity sealed with Cu-Cu bonding. (Upper right inset) SEM image shows the close-up view of the bonding ring and bonding interface.

**Table 3.1:** Results of helium leak rate for tested samples.

Samples	1	2	3	4	5
Helium leak rate ( $10^{-10}$ atm.cm <sup>3</sup> /sec)	5.5	5.8	7.6	13	16

### **3.7 Summary**

In this chapter, studies are associated with fundamental understandings of wafer level Cu-Cu bonding. Wafer planarity, surface roughness, surface cleanliness are the most critical factors to be controlled prior to wafer bonding. A zigzag Cu-Cu bonding interface is preferred among various interfacial behaviours of Cu-Cu bond, for the implication of substantial inter-diffusion taken place across the contact. The effects of micro-structural evolution of Cu grains on bonding quality are studied by comparing bonded wafers with and without pre-bonding anneal. It is found that stronger growth and inter-diffusion of the small Cu grains takes place at the Cu-Cu interface during bonding. Moreover, SAM passivation is examined with the ability to reduce surface oxidation based on the bonding results from 6 inch blanket Cu wafers. Lastly, Cu-Cu bonding exhibits excellent hermeticity using helium leak test on standalone cavity structures. The incorporation of both enhancement methods will be developed and discussed in later chapters.

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Chapter 3- Fundamental Study of Thermo-compression Cu-Cu Bonding

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## **Chapter 4**

# **Design and Fabrication of Wafer Level Fine Pitch Cu-Cu Bonding**

### **4.1 Introduction**

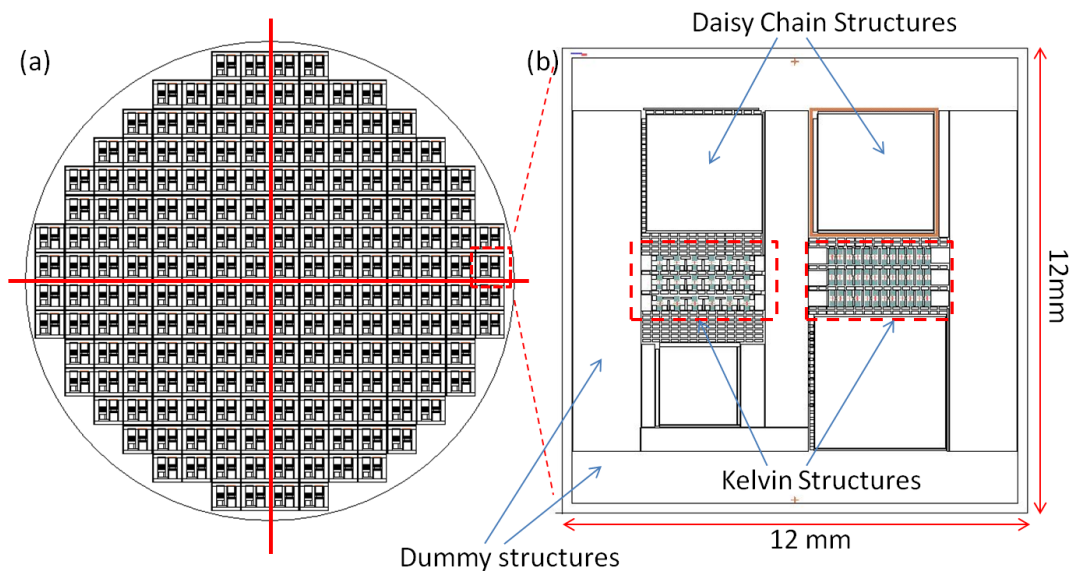
In this chapter, we introduce a wafer level design of a fine-pitch Cu-Cu bonding system which forms a continuous daisy chain based on thermo-compression bonding. Despite a number of demonstrations for high density Cu-Cu bonding at narrow pitch using C2W or C2C [4.1-4.3], W2W low temperature bonding demands more precise process control for forming robust fine pitch Cu-Cu bonds due to the susceptibility of bonding uniformity, W2W misalignment and surface properties.

A process flow is developed with the integration of self-assembled monolayer (SAM), which is used to provide temporary passivation to protect the Cu surface from contamination and oxidation prior to bonding. Following, process observations and optimizations are presented to tackle the challenges of the bonding process. Finally, we show that proper metallization and enhancement scheme can result in the formation of high quality Cu-Cu bonded interconnects in a CMOS compatible environment.

## **4.2 Wafer Level Design for Face-to-Face Bonding**

### *4.2.1 Wafer layout and mask design*

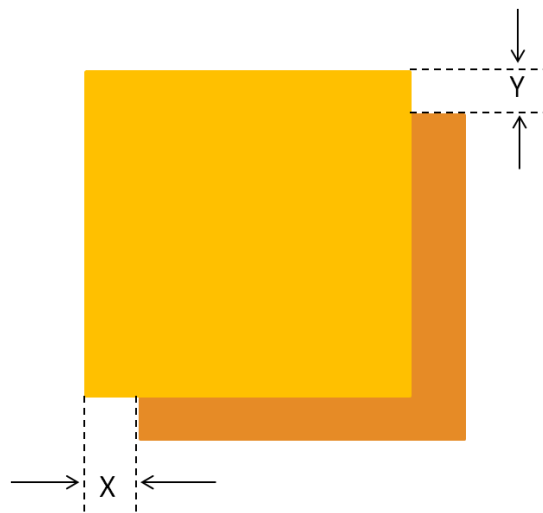
In this work, wafer stacking is achieved by bonding two wafers in a face-to-face (F2F) manner, in which temporary bonding and thin wafer handling processes are excluded. In this type of system, it is preferred to design pairing wafers with symmetric layout about the wafer center because each die will be face-to-face aligned and bonded exactly to the corresponding die from the pairing wafer, as shown in Figure 4.1 (a). Besides the layout design of the wafer map, a reticle containing four mask layers is designed to incorporate featured devices into Cu-Cu bonding process development. Figure 4.1 (b) shows a 12 mm × 12 mm mask design which consists of major components such as dummy structures, daisy chain structures and Kelvin structures.



**Figure 4.1:** Schematic wafer level design (a) symmetrical wafer map (b) die level mask design.

*4.2.2 Dummy structure*

In order to form a mechanically stable bonding system, it has to be ensured that the metal density for the bonding contact area is greater than 20%. Therefore copper dummy structures with dimension of  $50\ \mu\text{m} \times 50\ \mu\text{m}$  are used to increase the total bonding area across the wafer. In addition, after exposure of the test structures, W2W misalignment error can be extracted from the dummy structure using optic microscope, as shown in Figure 4.2.



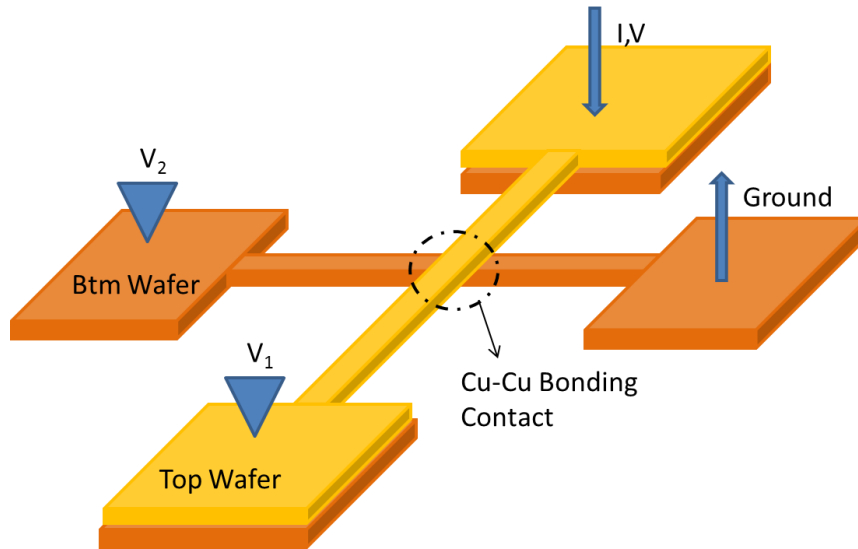
**Figure 4.2:** Schematic top view of copper dummy bonding structures, wafer-to-wafer misalignment error can be found in both X-axis and Y-axis.

*4.2.3 Kelvin structure*

Figure 4.3 shows a cross bar Kelvin structure design to characterize the bonding quality of Cu-Cu contacts. On each of both pairing wafers, the Cu line surface is exposed and bonded to each other. Both lines are intersected at a small bonding interface where the current is forced to flow through. The advantage of this structure is that the contact area is not affected by misalignment [4.4] and it only measures the resistance at the Cu-Cu bonding interface due to its insensitivity to the line resistance. The specific contact resistance ( $\rho_c$ ) can be calculated as:

$$\rho_c = R_c \cdot A_c \quad (4.1)$$

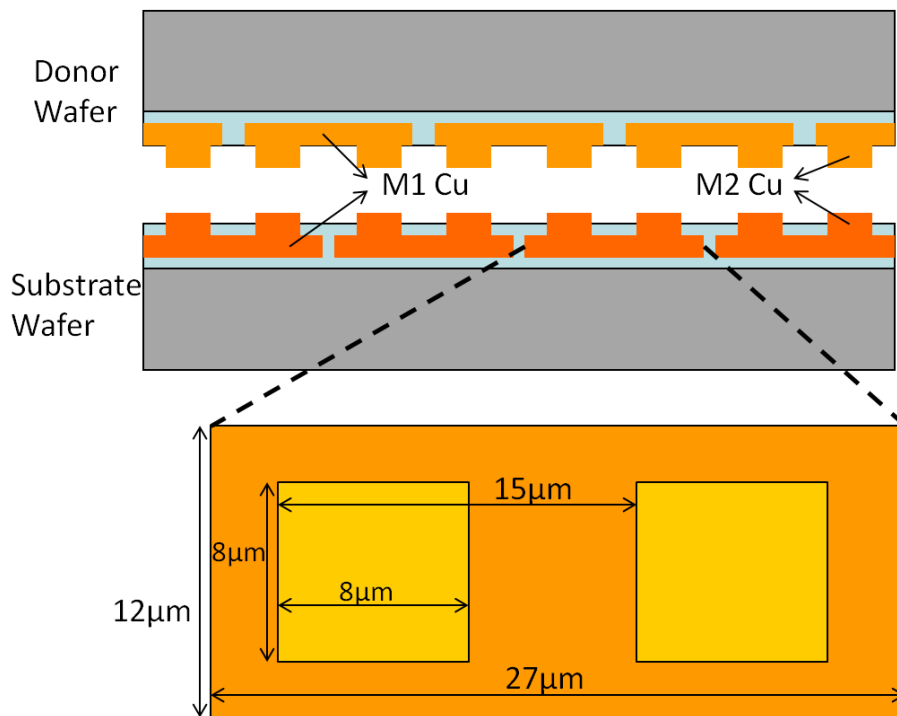
$$R_c = \frac{V_1 - V_2}{I} \text{ or } \frac{\Delta(V_1 - V_2)}{\Delta I} \quad (4.2)$$



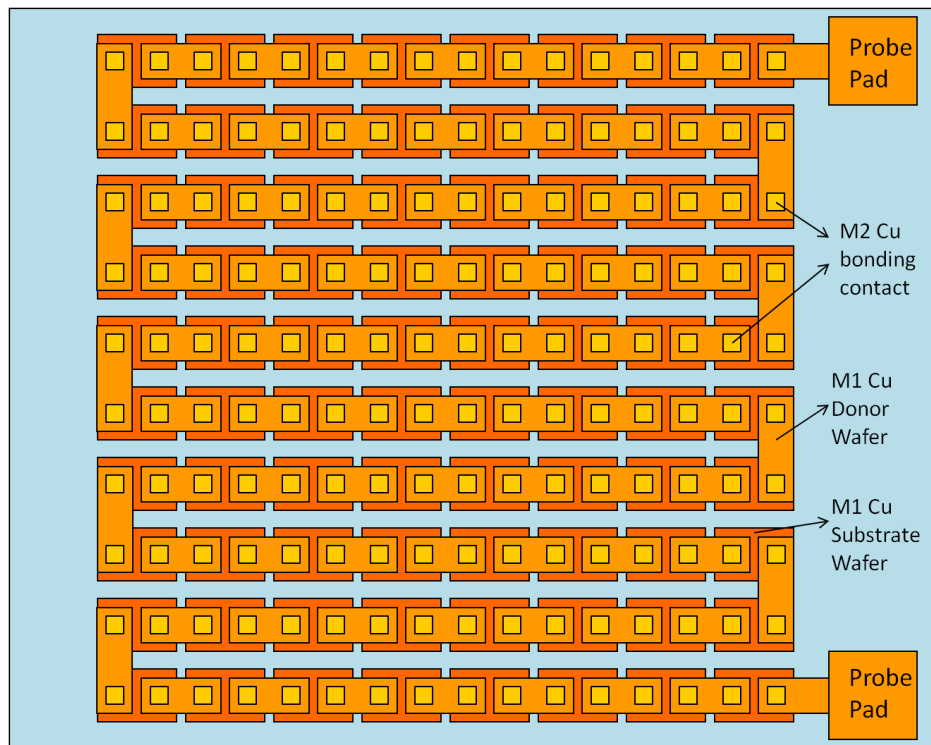
**Figure 4.3:** Schematic view of a cross bar Kelvin structure in which two Cu lines are bonded at a joint interface.

*4.2.4 Daisy chain structure*

High density Cu-Cu bonds is demonstrated by designing a fine pitch daisy chain circuit, with two layers of copper structures from both pairing wafers, as shown in Figure 4.4 (a). The size of contact copper pad is  $8\ \mu\text{m} \times 8\ \mu\text{m}$  with the pitch size of  $15\ \mu\text{m}$  (Figure 4.4 (b)). When wafer-to-wafer is precisely aligned and bonded, the bonding structure can conduct current in an inter-strata manner. After successful bonding, the final daisy chain structure can be tested across 220 rows of bonding nodes via extended probing pads, as shown in Figure 4.5.



**Figure 4.4:** (a) Cross-sectional schematic of bonding structures from the pairing wafers prior to bonding, (b) dimensions of M1 Cu pads and M2 Cu line.



**Figure 4.5:** Top-down view of bonded daisy chain circuit.

### **4.3 Fabrication of Fine Pitch Cu-Cu Bonding**

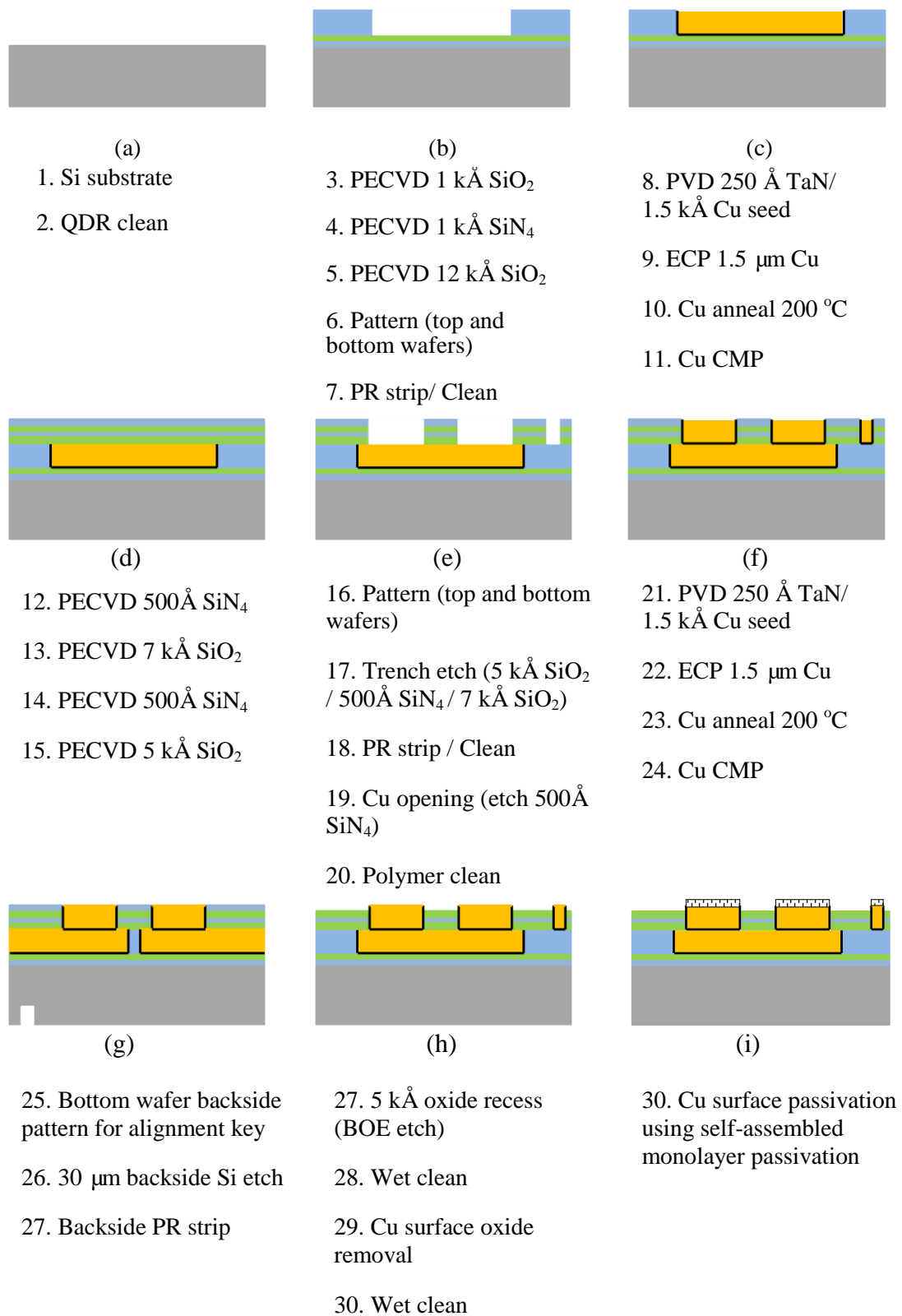
The schematic process flow for pre-bonding wafer fabrication is shown in Figure 4.6. A *p*-type 200mm Si substrate was used for pre-bonding development with QDR clean. (Figure 4.6 (a)) Then, three oxide/nitride layers were deposited on both pairing wafers, followed by lithography and dry etch steps to form the trenches for the first metal layers (M1), as shown in Figure 4.6 (b). After that, Cu film (M1) was formed through standard damascene process including barrier/Cu seed deposition, Cu ECP, Cu anneal and Cu CMP. (Figure 4.6 (c)) Subsequently, another four dielectric layers were deposited using PECVD. The top oxide recess layer is critical for a precise control on copper exposure, as shown in Figure 4.6 (d). Next, M2 metallization followed the same process sequence of M1 layer, except that the M2 trench formations requires two dry etch steps as to avoid Cu contamination in the non-metal chamber (Figure 4.6 (e)). After a successful M2 layer formation, M1 and M2 are connected and wafer front side alignment mark is formed, as illustrated in Figure 4.6 (f).

In order to perform face-to-face alignment, one of the pairing wafers needs to have wafer backside alignment mark. Therefore the bottom wafer was separated from the pairing group to carry out a wafer backside process to generate the alignment mark, as shown in Figure 4.6 (g). After that, the oxide layer from each wafer was removed after immersion in BOE for a few minutes to make M2 Cu layer protrusion, controlled by a thin nitride layer as the selective etch stop layer shown in Figure 4.6 (h).

Figure 4.6 (i) depicts self-assembled monolayer (SAM) passivation step on the clean Cu surface. This is a critical step to enable a good bonding process as it requires high surface cleanliness immediately before bonding. Therefore after Cu protrusion,

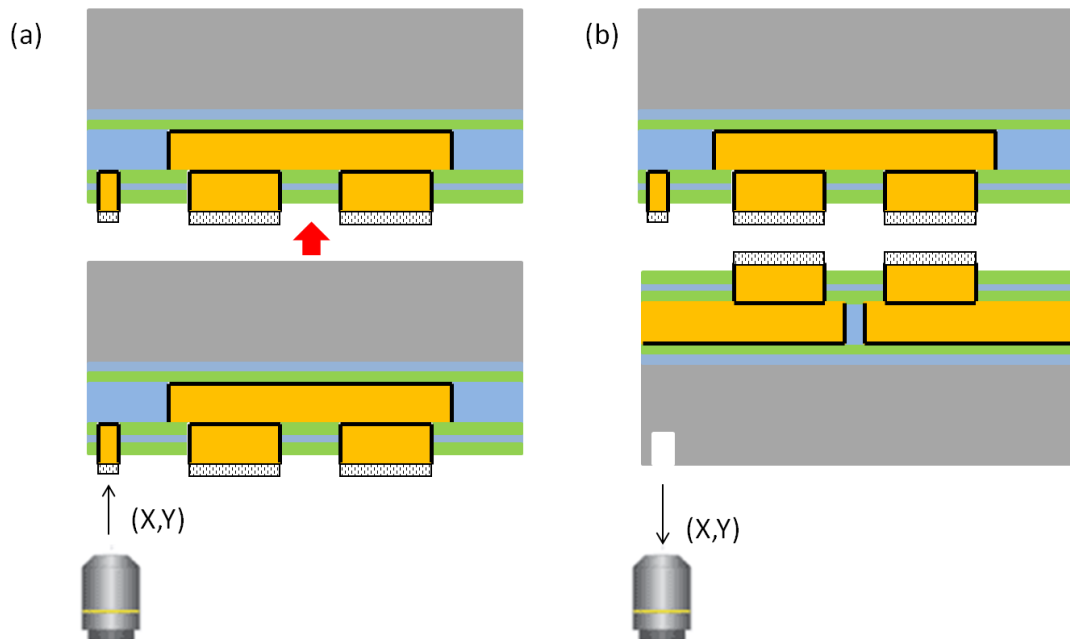
we used a cleaning step that is benign to the BEOL processes to completely remove surface oxide. Then, the Cu surface is passivated by immersing the wafer in the alkane-thiol solution. The alkane-thiol used in this work is 1-hexanethiol [ $\text{CH}_3\text{-(CH}_2\text{)}_4\text{-CH}_2\text{-SH}$ ]. The thiol (-SH) head groups bind to Cu and form a densely packed monolayer on the Cu surface. The methyl (-CH<sub>3</sub>) tail groups make the surface hydrophobic. As SAM protects the Cu surface from surface contamination and oxidation, better bonding quality is expected.

The pairing wafers are then aligned face-to-face. In the indirect-alignment methods, the two wafers are aligned by means of an external reference positioning system. For front-to-bottom side or backside alignment, the top wafer needs alignment keys on the active side (front side) and the bottom wafer needs them on the backside; thus, both alignment structures are faced downward in the microscope direction, as shown in Figure 4.7 (a). The alignment marks of the top wafer are imaged, the position is stored and the backside keys of the loaded bottom wafer are aligned to the stored images (Figure 4.7 (b)). The drawback of this method is that there are two alignment steps (formation of backside alignment key and front-to-bottom alignment) which make the W2W alignment error more severe. The counter measure is to use interface alignment, which is known as “front-to-front” alignment. It makes use of a dual-microscope system which provides two microscopes in between the wafer stack. During the alignment process, each microscope will observe the alignment key on the front side of each wafer. Therefore backside alignment key is not required and the new system allows for high alignment accuracy for wafer-bonding processes.

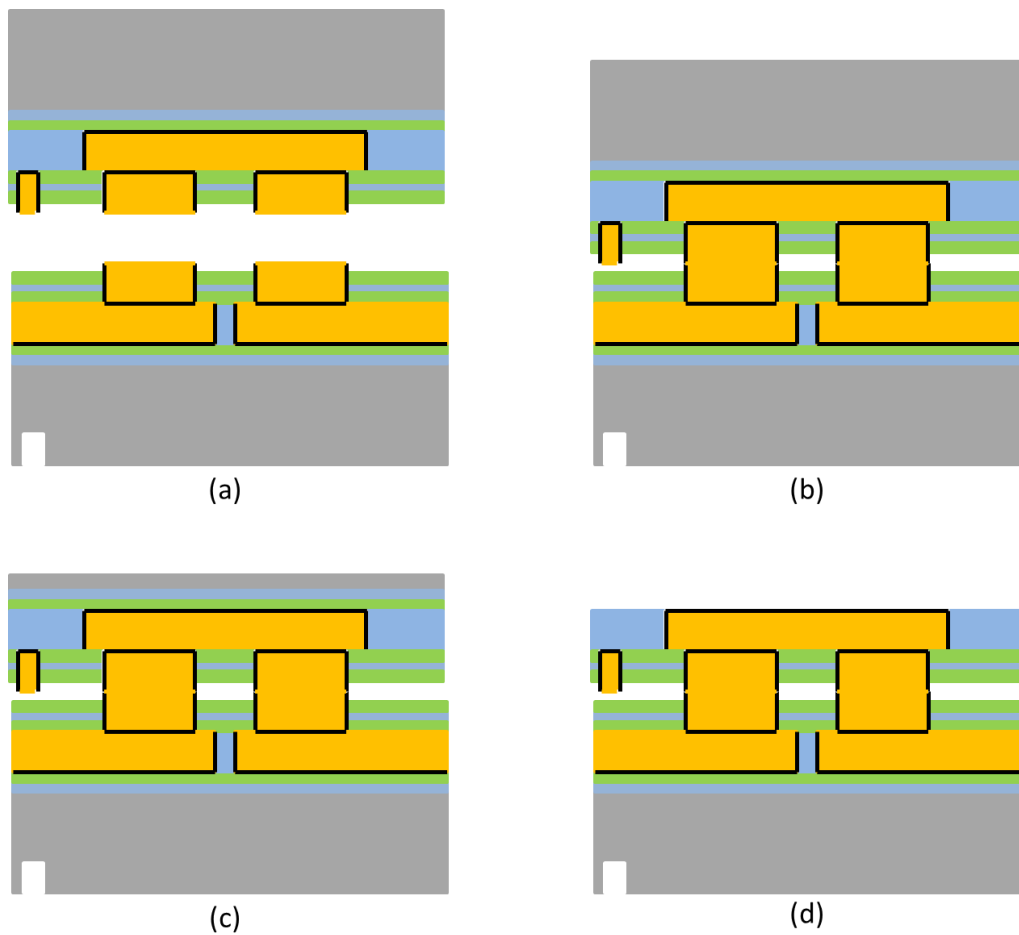


**Figure 4.6:** Schematic process flow of wafer fabrication prior to W2W alignment/bonding process.

After the W2W alignment, the pairing wafers protected by SAM were transferred into the bonding chamber. The chamber was subjected to a few N<sub>2</sub> pump-purge cycles to reduce the ambient oxygen content. Prior to bonding, *in-situ* desorption of SAM was carried out at 250 °C in the bonding chamber. This step uncovers the clean surface for Cu-Cu bonding at 350 °C for 1 hour in vacuum followed by N<sub>2</sub> batch annealing at 350 °C for 1 hour, shown in Figure 4.8 (a)-(b). The donor wafer was subsequently thinned back to the required thickness (Figure 4.8 (c)). Through silicon via (TSV) formation is excluded to simplify the process as we are mostly interested in the property of the Cu-Cu bond. Figure 4.8 (c)-(d) show that donor wafer is thinned down using a combination of grinding and selective etching. Finally, the bonded Cu structures can be probed directly through exposed Cu surface after donor wafer removal.



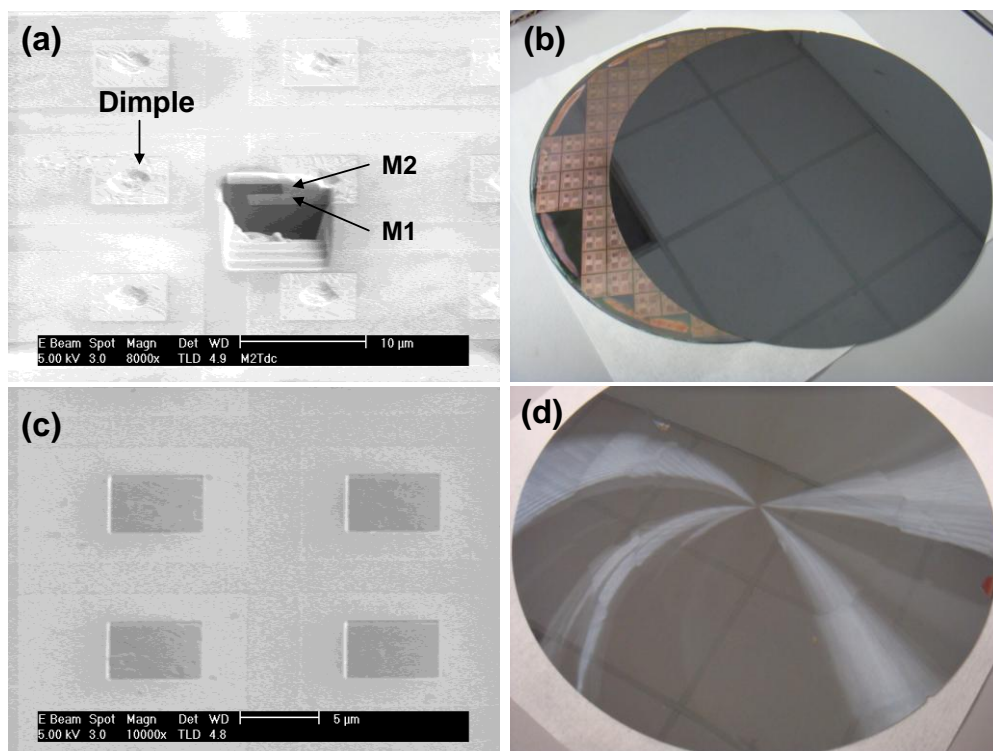
**Figure 4.7:** Face-to-face alignment mechanism: (a) Top wafer alignment mark positioning as reference and the wafer is then moved up. (b) Bottom wafer is loaded and aligned with reference to the stored coordinate.



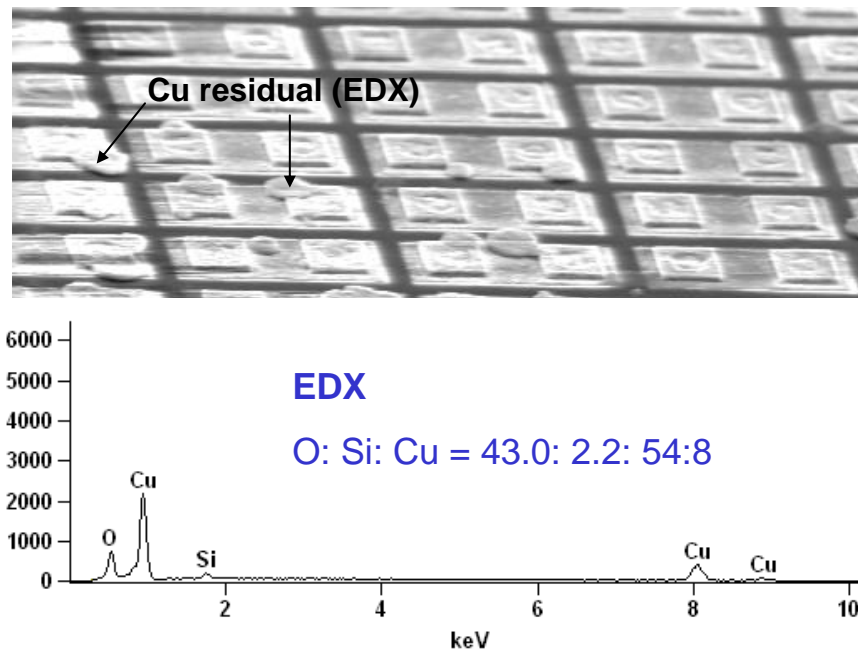
**Figure 4.8:** (a) SAM desorption in the chamber prior to bonding. (b) W2W bonding. (c) Wafer grinding to  $\sim 100 \mu\text{m}$ . (d) TMAH and BOE etch to expose Cu surface from the backside.

## 4.4 Observation and Process Optimization

In the early process development, the SAM passivation step was excluded to solely understand the challenges of each critical step. Figure 4.9 shows the effect of surface non-planarity as a result of poor process control during metallization and CMP. Cu surface dimple is initially observed and it reduces the amount of contact area for reliable bonding, as shown in Figure 4.9 (a). The bonding interface is unable to sustain shear force during grinding and wafers separate completely as shown in Figure 4.9 (b). When the metallization and CMP are fully optimized, the bonded Cu is able to withstand grinding down to  $\sim 100\ \mu\text{m}$  without failure as shown in Figure 4.9 (c)-(d). Furthermore, the same wafer pair survives subsequent selective etching as well.



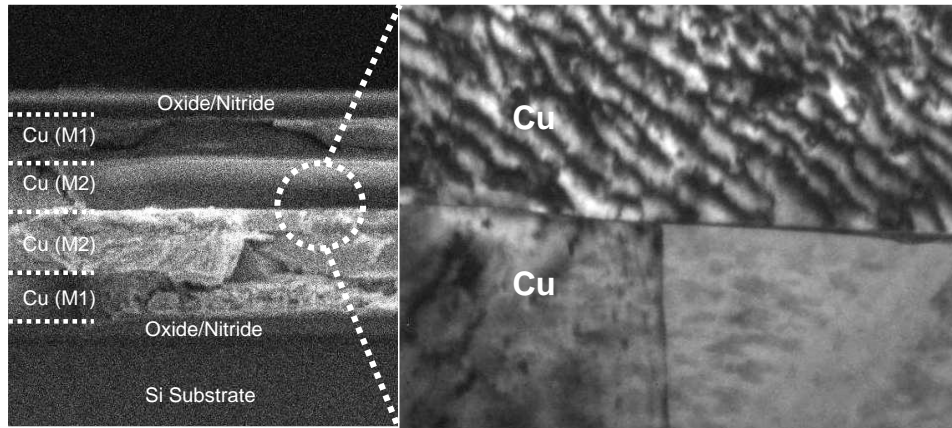
**Figure 4.9:** Cu surface topology and the mechanical bond strength of the bonded Cu-Cu structures. (a) Cu surface dimple due to poor process control. (b) Separation of the bonded wafer during wafer grinding. (c) Flat Cu surface after optimization. (d) Successful wafer thinning.



**Figure 4.10:** EDX analysis on the Cu surface of wafer pair that are separated during grinding.

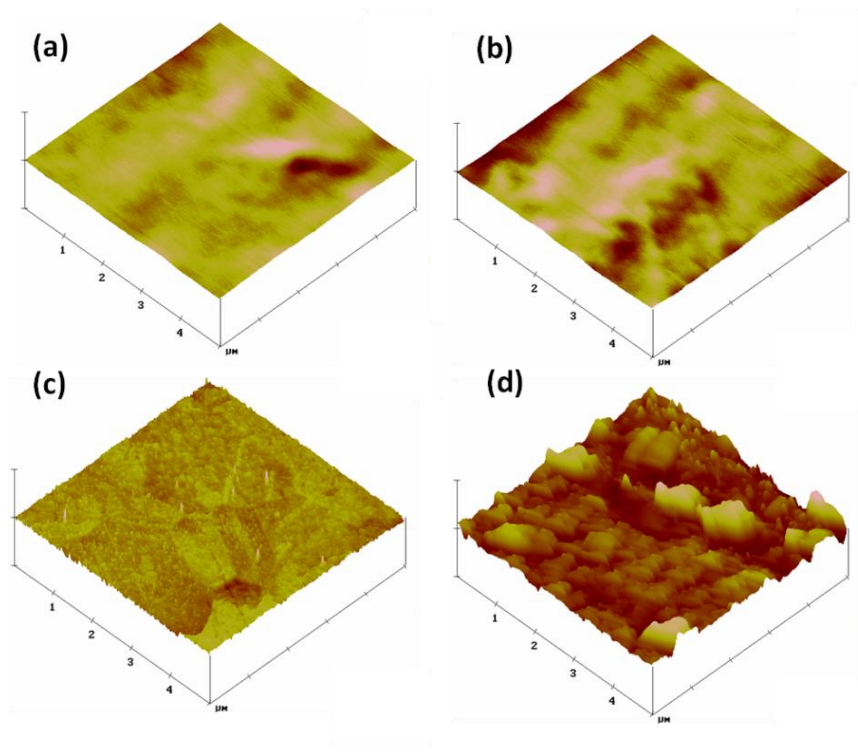
Figure 4.10 shows the surface of the Cu structure after failure (Figure 4.9 (b)) during grinding. Random Cu residual (as confirmed by EDX) is detached from the donor wafer due to partial/non-uniform bonding. However, majority of the bonded Cu-Cu peel off at the bonding interface due to poor bonding. Therefore, it is important to maintain the flatness of Cu surface in order to maximise the total contact area for a reliable mechanical support.

Figure 4.11 is a cross sectional view showing the bonded Cu-Cu structures when the patterned wafers are bonded at 350 °C, without SAM passivation. The right inset is a TEM image showing the bonded Cu-Cu interface and the grain structures. The bonding interface in between M2/M2 Cu layers can be clearly seen, indicating that no inter-diffusion has taken place.



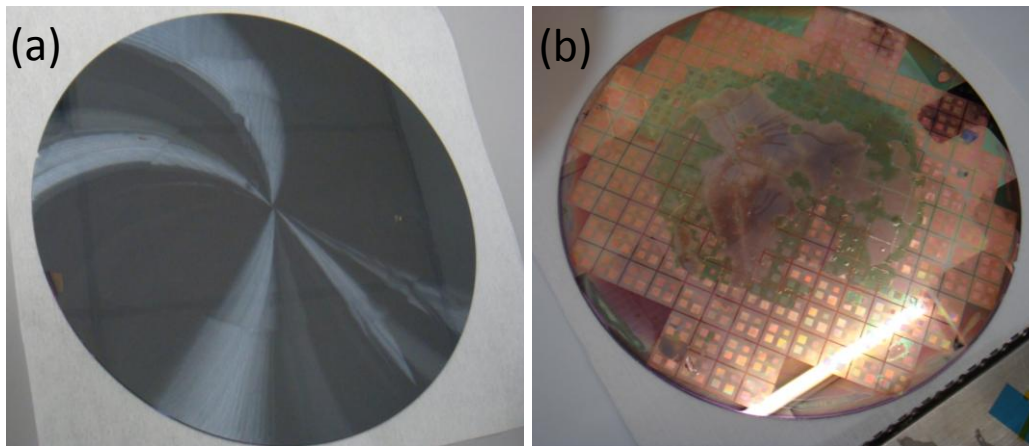
**Figure 4.11:** TEM image showing grain structure and morphology in bonded Cu-Cu layer.

Prior to bonding, it is important to ensure that the Cu surface is as clean as possible. Therefore, a proper cleaning method is required to remove the Cu surface oxide. Figure 4.12 (a) to (d) show the resulting Cu surfaces profile and surfaces roughness with different cleaning approaches. The Cu surface roughness after chemical mechanical polishing (CMP) is  $\sim 0.47$  nm as shown in Figure 4.12 (a). When acid clean is used, the surface roughness is strongly dependent on the concentration. Dilute acid clean results in an increment in the surface roughness to 0.52 nm (Figure 4.12 (b)) while regular acid clean results in a roughness of 1.20 nm (Figure 4.12 (c)), respectively. Dry etch with inert species results in the worst overall roughness of 11.90 nm as energetic ions are bombarded on the Cu surface as shown in Figure 4.12 (d). Higher surface roughness is not desirable for Cu-Cu bonding as Cu-Cu contact formation becomes more difficult due to the reduction of the contact area.



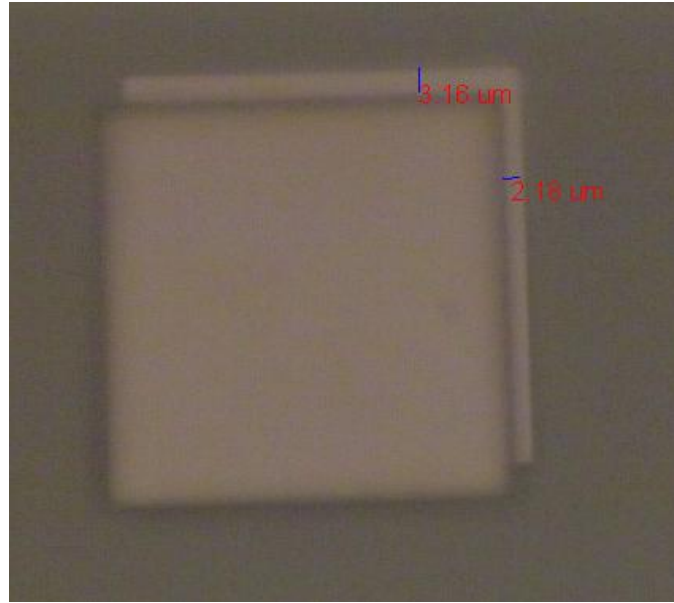
**Figure 4.12:** Cu surface profile and RMS roughness from atomic force microscopy (AFM) scanning after (a) Cu CMP (0.47 nm), (b) dilute acid clean (0.52 nm), (c) regular acid clean (1.20 nm), and (d) dry etch (11.90 nm).

Before pre-bonding fabrication, the total thickness variation (TTV) of each wafer is measured just after Cu CMP. It is vital that the TTV needs to be controlled below 3% of the total wafer thickness. Figure 4.13 shows an example of the bonding of two patterned wafers which exceeds the required control value of the TTV. As a result, cracks and non-uniform wafer surface are observed after thinning down the bonded wafer, as shown in Figure 4.13 (a). After further TMAH process for complete Si substrate removal, only the area on wafer center still remains bonded whereas the rest of bonded area is peeled off (Figure 4.13 (b)).



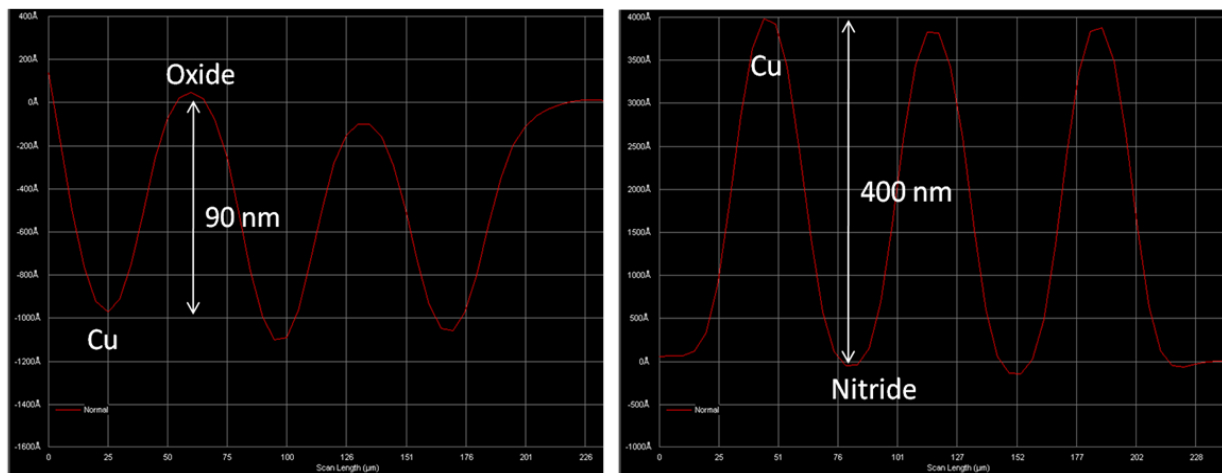
**Figure 4.13:** (a) Observation of surface non-uniformity after wafer thinning. (b) A large bonded area peeled off outside wafer center after TMAH process.

Moreover, the target alignment accuracy is another major decision criterion. The ITRS roadmap for high density TSV applications defines bonding overlay accuracy of  $0.5 \mu\text{m}$  in the near term. W2W alignment for fine pitch applications requires effort from the state-of-the-art aligner system and the robustness of the fabrication process. Figure 4.14 shows an example of revealed Cu-Cu bonded structures with  $\sim 3.16 \mu\text{m}$  on Y-axis and  $\sim 2.18 \mu\text{m}$  on X-axis, using front-to-back alignment method.

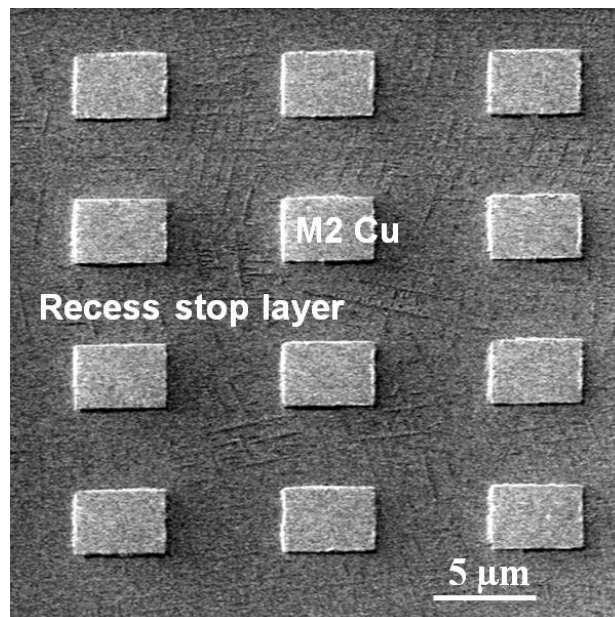


**Figure 4.14:** Microscopic image of Cu bonded structures with measured W2W alignment error.

Another critical step to Cu W2W bonding is oxide recess to expose the Cu bonding surface. This is necessary as oxide is more rigid as compared to Cu. The amount of oxide recess can be controlled precisely using a thin nitride layer as the selective etch stop layer. The general guideline is that the oxide recess must be at least equal to the amount of CMP dishing on the Cu structures. Soft polishing pad and strong removal rate slurry were applied during CMP. The load of polishing is 320-350g/cm<sup>2</sup>. The speed of pad and chuck are 90 rpm. Speed of slurry feeding is 170-200 cc/min. Figure 4.15 (a) shows the dishing effect after Cu CMP. There is a difference of ~90 nm in height between the top oxide layer and M2 Cu layer. Subsequently after oxide removal step, it is observed that a well-controlled recess has taken place when a 500 nm oxide layer is completely removed and etching stops on the nitride layer underneath, as shown in Figure 4.15 (b). Therefore, the Cu exposure will be controlled precisely at ~400 nm throughout the wafer, as shown in Figure 4.16.



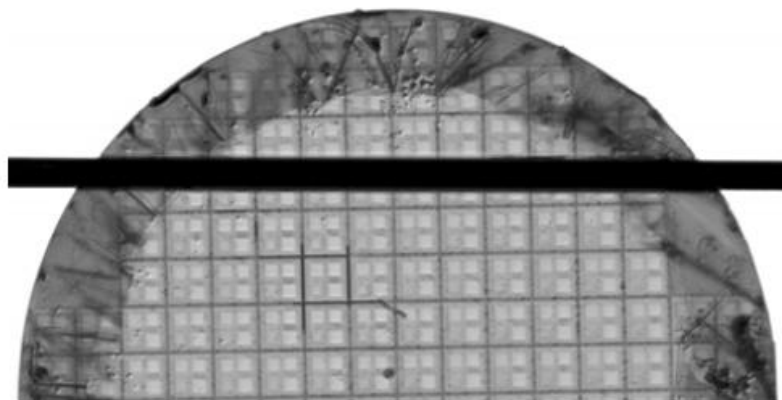
**Figure 4.15:** Surface profile characterization (a) After Cu CMP, (b) After oxide recess.



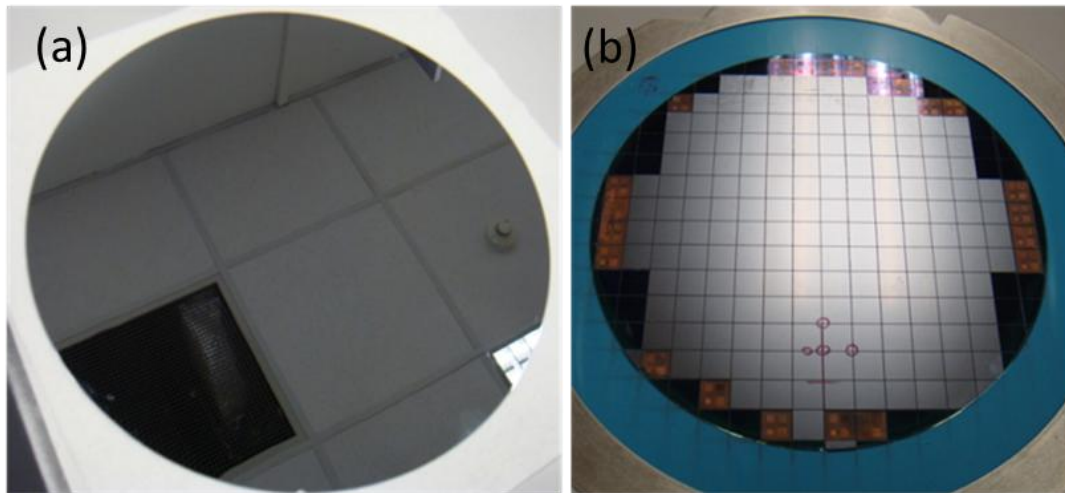
**Figure 4.16:** Uniform Cu exposure after ILD oxide recess step.

With the efforts to optimize the key process challenges, uniform bonding is achieved across the entire wafer as shown in the *c*-mode scanning acoustic microscopy (*c*-SAM) image in Figure 4.17. Figure 4.18 (a) shows a successful Cu-Cu bonded wafer after donor wafer grinding from  $\sim 720\ \mu\text{m}$  to  $\sim 100\ \mu\text{m}$ , without any surface defect and failure. The dicing test is also performed with  $\sim 90\%$  yield. A few failures are observed at wafer edge region, as shown in Figure 4.18 (b). Both tests suggest a reliable mechanical strength of Cu-Cu bonds with proper process control and optimizations have been obtained.

In addition to the abovementioned process controls, better surface finishing is expected for W2W bonding with the implementation of SAM passivation. The overall system reliability could be further enhanced if the surface oxidation can be substantially suppressed on small bonding contacts. The characterization of the enhancement scheme will be discussed in the next chapter.



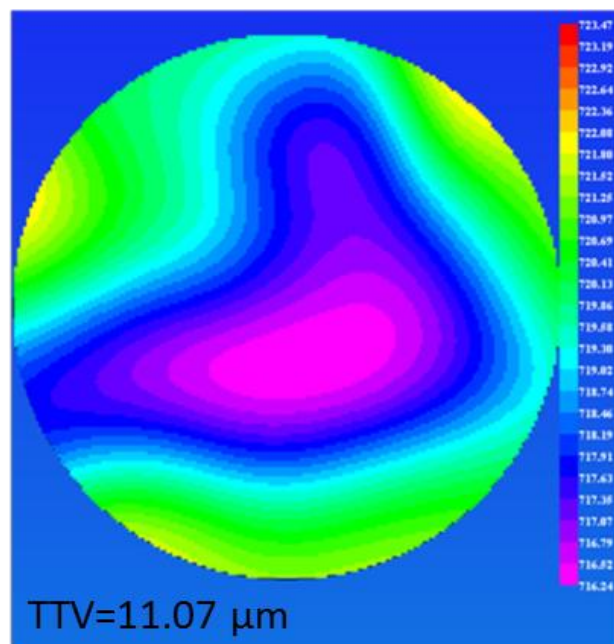
**Figure 4.17:** *C*-SAM view of the bonded wafers. The wafer edge is taped to prevent wafer infusion during scanning.



**Figure 4.18:** Post-bonding results including (a) Wafer grinding. (b) Wafer dicing.

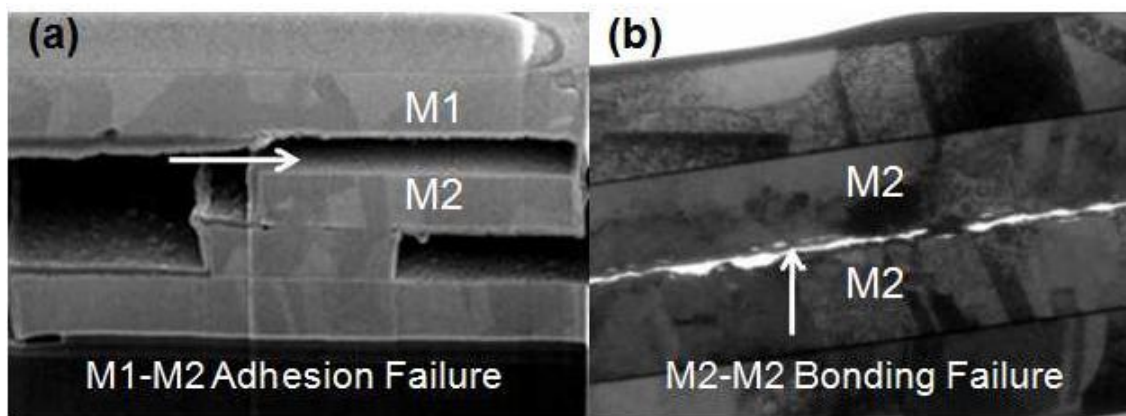
## **4.5 Mechanical Properties of Cu-Cu Bond**

In Figure 4.19, the wafer map shows a total thickness variation (TTV) value of 11.07  $\mu\text{m}$  prior to bonding. The wafer is concave with lower thickness at the center. This non-uniformity results in two possible types of failure during shear test on the bonded Cu structure described below. The bonded wafer pair is diced into dies of 12 mm  $\times$  12 mm. Two of such dies, one from the center and the other from the edge of the wafer, are subjected to shear test to delaminate the bonded die completely. An array of 8  $\times$  8 bonded Cu squares, each one with dimension of 50  $\mu\text{m}$   $\times$  50  $\mu\text{m}$  at a pitch of 100  $\mu\text{m}$ , are designed to examine the failure.

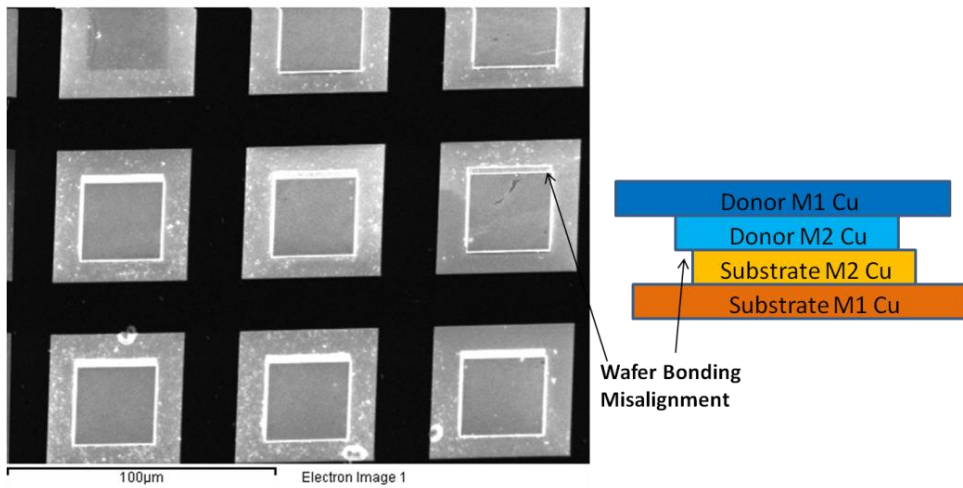


**Figure 4.19:** Wafer map showing the thickness across the wafer (200 mm). The total thickness variation (TTV) is 11.07  $\mu\text{m}$ .

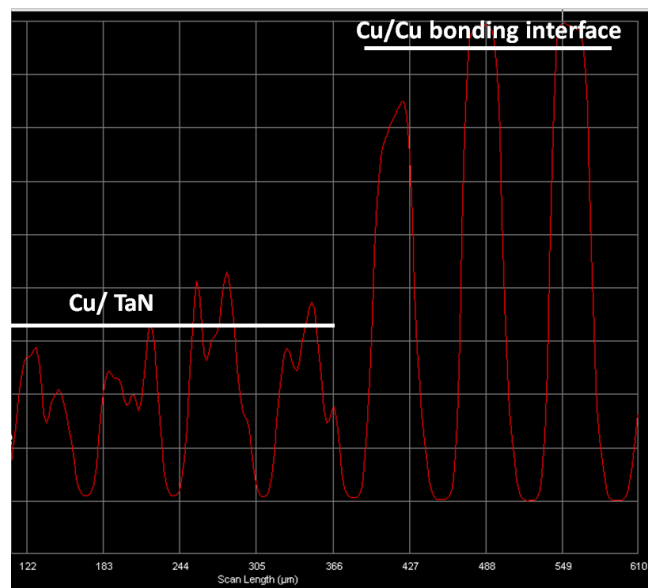
There are two possible types of failure during shear test, namely: (a) adhesion failure at the M1-M2 interface (between M2 TaN and M1 Cu) and (b) bonding failure at the M2-M2 interface (between M2 Cu and M2 Cu). These failures are shown in the TEM images in Figure 4.20. Identification of the failure interface can be done using a combination of surface profiler to measure the energy-dispersive X-ray spectroscopy (EDX) (Figure 4.21) and the step height (Figure 4.22). At the wafer edge, Cu-Cu is well bonded as this area is in intimate contact due to the wafer curvature. As a result, majority (58/64) of die failure is due to adhesion failure at the M1-M2 interface. This shows that well-bonded Cu-Cu layer is mechanically stronger than the adhesion between Cu and TaN. At the center of the wafer, Cu-Cu is not as well bonded (due to wafer curvature) and therefore 37/64 of die fail due to M2-M2 bonding failure. A summary of the failure analysis is summarized in Table 4.1.



**Figure 4.20:** Common modes of de-bonding: (a) Adhesion failure at the M1-M2 interface (between M2 TaN and M1 Cu). (b) Bonding failure at the M2-M2 interface (between M2 Cu and M2 Cu).



**Figure 4.21:** SEM image of bonding structure after shear test. Donor M1 Cu is detached but bonded layers (M2-M2) still present as misalignment mark is observed.



**Figure 4.22:** Step height measurement across bonding structures after shear test. Different step height values suggest respective the metal layers that remain undamaged after shear test.

**Table 4.1:** Summary of failure interface based on a group of  $8 \times 8$  bonded structures at the edge and center of wafer. Bond size is  $50 \mu\text{m} \times 50 \mu\text{m}$  at a pitch of  $100 \mu\text{m}$ .

<b>Failure</b>	<b>Edge</b>		<b>Center</b>	
	<b>M1-M2</b>	<b>M2-M2</b>	<b>M1-M2</b>	<b>M2-M2</b>
<b>Row 1</b>	6	2	2	6
<b>Row 2</b>	8	0	2	6
<b>Row 3</b>	8	0	5	3
<b>Row 4</b>	6	2	4	4
<b>Row 5</b>	7	1	2	6
<b>Row 6</b>	7	1	3	5
<b>Row 7</b>	8	0	3	4
<b>Row 8</b>	8	0	4	3
<b>Total</b>	58	6	27	37

## **4.6 Summary**

The wafer level design is discussed with the incorporation of the test vehicles. Process design, evaluation and optimization of a high density wafer level Cu-Cu bonding process are performed. Cu surface topology requires serious attention as it determines the total bonding area. Diluted acid clean is preferred to provide the desired surface roughness. In addition, wafer uniformity, W2W alignment accuracy and oxide recess need to be addressed for successful bonding. Mechanical properties are characterized based on optimized bonded wafer. It is found that failures at Cu-Cu bonding interface are largely attributed to wafer non-uniformity.

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## **Chapter 5**

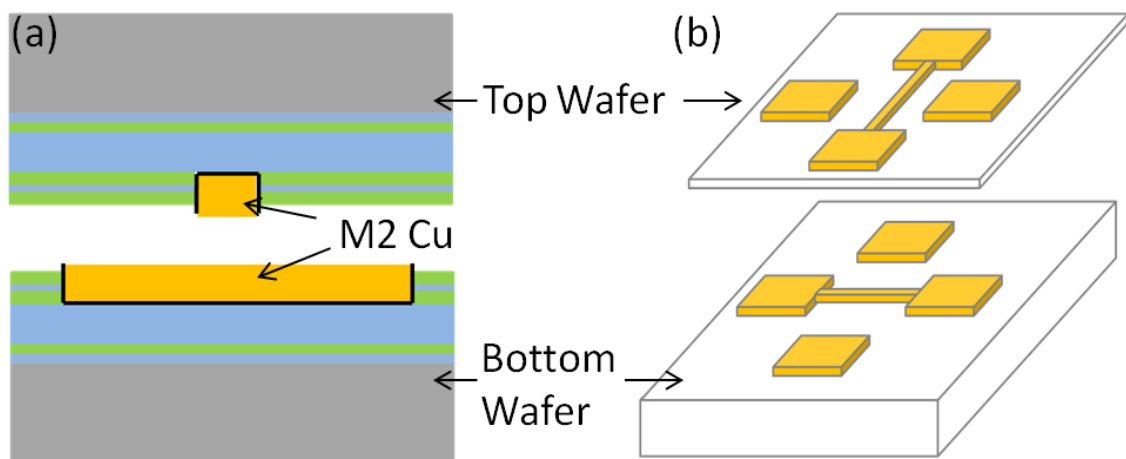
# **Characterization of Cu-Cu Bonding Contact**

### **5.1 Introduction**

The analysis of Cu-Cu bond is performed on Kelvin structures fabricated with different process conditions. The Kelvin structure serves as an effective way to extract the electrical properties of Cu-Cu bonding interface with various imperfections. In this chapter, the major interests of the characterization include the effect of enhanced bonding methods, bonding temperature, thermal reliability and the effect of Cu seal ring. Systematic investigations are carried out to understand the behavior of small bonding contact for the application of high density interconnects.

## 5.2 Fabrication and Characterization of Kelvin structure

The process flow of Cu-Cu bonding is described in Chapter 4. However, unlike the daisy chain structure which consists of M1 Cu lines and M2 Cu pads, the contact of Kelvin structure only makes use of M2 Cu lines from respective pairing wafers to be bonded as shown in Figure 5.1 (a). Oxide recess is needed to facilitate Cu exposure and Cu-Cu bonding. Figure 5.1 (b) shows the two probing pads from the top wafer requiring two landing pads for the mechanical support. The bonded wafer is completely thinned down from the top until the structure is exposed after sufficient etching. In the first reticle design, the contact dimension of Kelvin structure is  $8 \mu\text{m} \times 10 \mu\text{m}$ . This is in accordance with the equivalent fine pitch ( $15 \mu\text{m}$ ) bonding contact with the Cu pad dimension ranging from  $8 \mu\text{m}$  to  $10 \mu\text{m}$ .



**Figure 5.1:** (a) Cross sectional schematic of cross-over M2 Cu lines to be bonded. (b) Schematic of Kelvin structure prior to bonding.

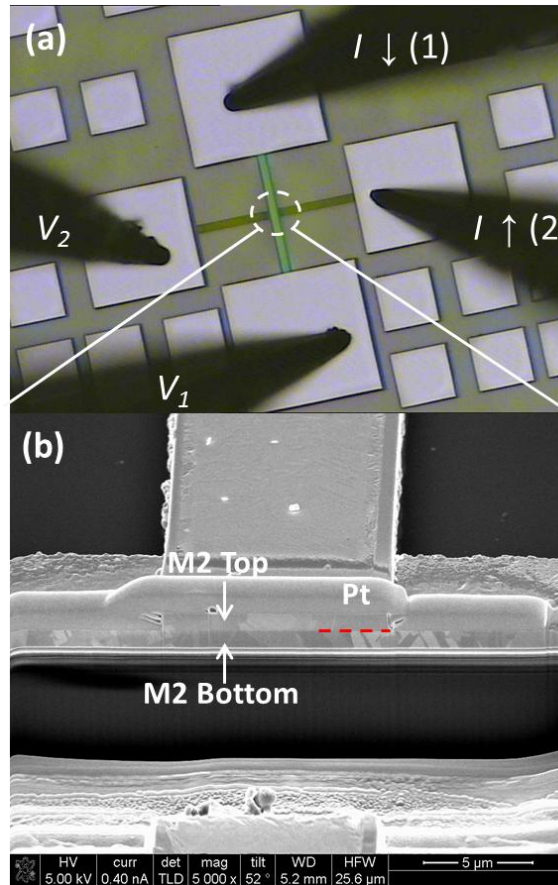
The quality of the Cu-Cu bond is gauged by measuring its contact resistance from the cross bar Kelvin structure as shown in Figure 5.2 (a). The extraction of both specific contact resistance ( $\rho_c$ ) and contact resistance ( $R_c$ ) described in Chapter 4 are as follows,

$$\rho_c = R_c \cdot A_c \quad (5.1)$$

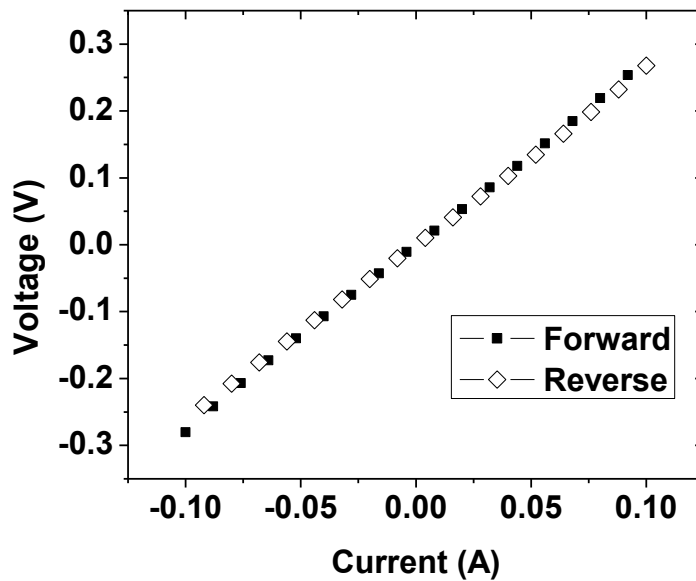
$$R_c = \frac{V_1 - V_2}{I} \text{ or } \frac{\Delta(V_1 - V_2)}{\Delta I} \quad (5.2)$$

In equation (5.1),  $R_c$  is the contact resistance and  $A_c$  is the contact area, while in equation (5.2),  $V_1$  and  $V_2$  are the measured voltages across the contact area and  $I$  is the sweeping current.

Figure 5.2 (b) shows the cross-sectional view of the Cu-Cu bonding interface. When current is swept in forward and reverse directions from across the bonded Cu-Cu structure, a repeatable ohmic behavior is clearly demonstrated and no hysteresis is observed. This suggests that an ohmic contact has been successfully formed as shown in Figure 5.3 that shows the measured voltage across terminals (1) and (2) as current ( $I$ ) changes.

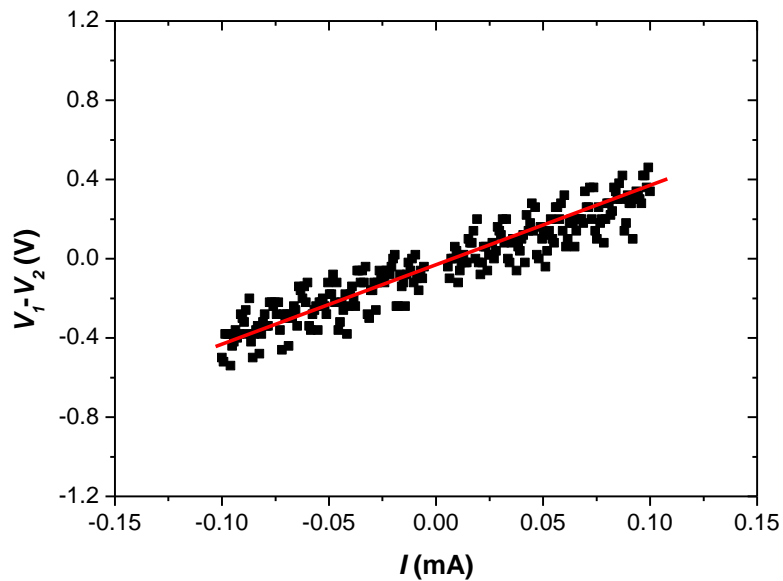


**Figure 5.2:** (a) Optical microscope image of Kelvin structure after bonding. (b) Interface of the bonding contact.

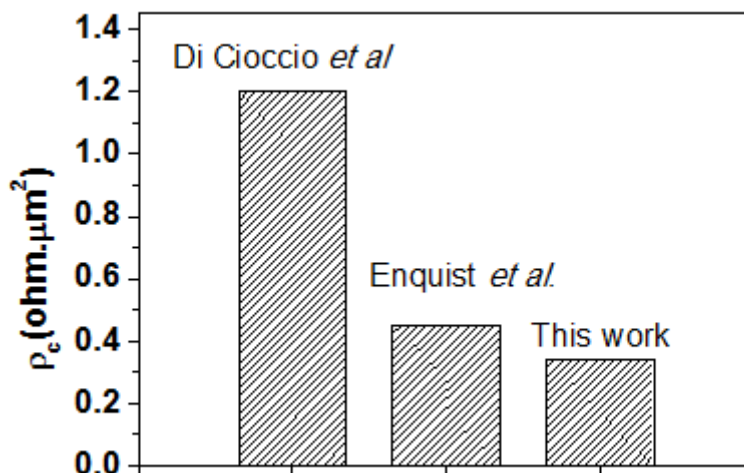


**Figure 5.3:**  $V$ - $I$  plot of the Cu-Cu contact in both forward and reverse sweeping current show an ohmic behavior with no hysteresis.

In Figure 5.4, the contact resistance of a  $10\ \mu\text{m} \times 8\ \mu\text{m}$  cross bar structure is measured and calculated. As current is swept from  $-100$  to  $+100$  mA, potential ( $V_1-V_2$ ) varies linearly and this again verifies the ohmic behavior of the Cu-Cu contact.  $R_c$  is estimated as  $\sim 4.2\ \text{m}\Omega$ . This translates into an excellent value of  $\rho_c$  of  $\sim 0.34\ \Omega\cdot\mu\text{m}^2$  which compares very favourably with reported values in the literatures [5.1, 5.2] (Figure 5.5).



**Figure 5.4:** Estimation of Cu-Cu contact resistance.

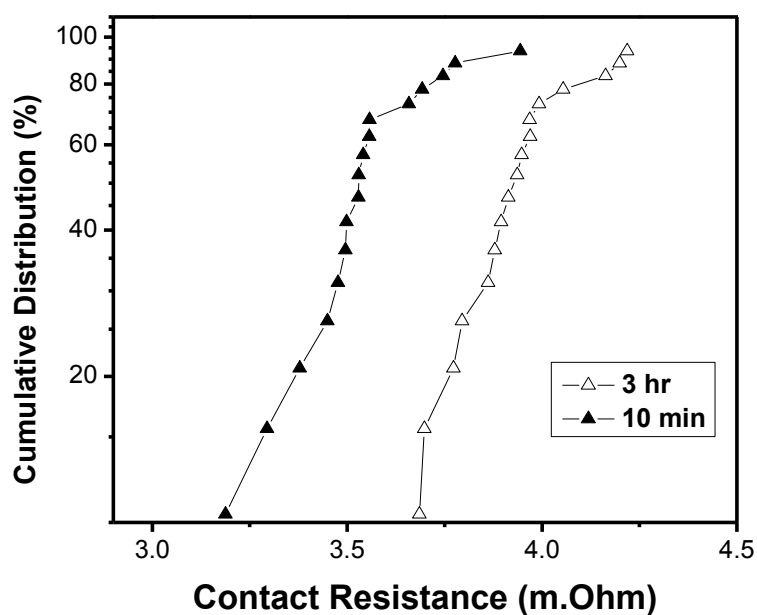


**Figure 5.5:** Reported Cu-Cu specific contact resistance values.

### **5.3 Bonding Contact due to Surface Imperfection**

Copper is a metal material which naturally reacts with atmospheric oxygen to form a copper oxide layer. However, in a Cu-Cu bonding system, the oxidized Cu surface impedes effective inter-diffusion of Cu atoms across the bonding interface. Hence, it is important to understand the effect of the barrier on the overall electrical performance of Cu-Cu bonds.

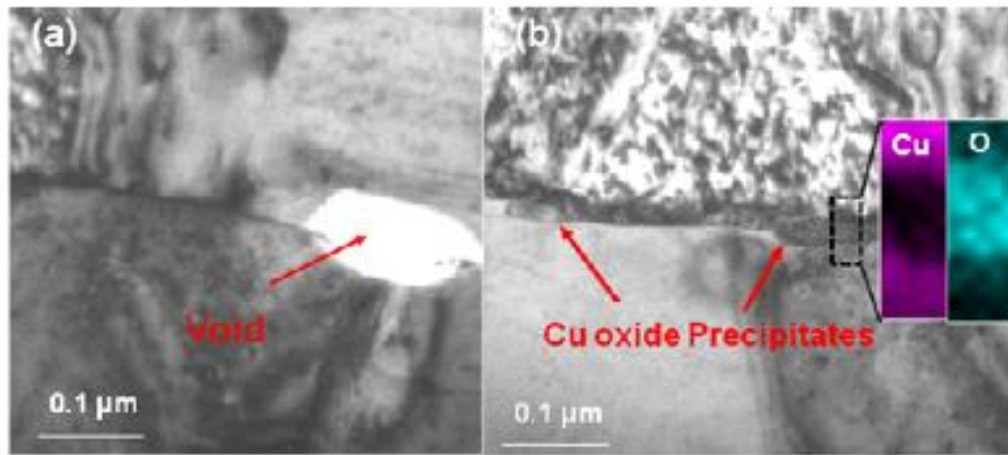
In Figure 5.6, contact resistance of a  $10\ \mu\text{m} \times 8\ \mu\text{m}$  cross bar structure is measured and presented in a cumulative plot. The contact resistance is sensitive to the amount of time lapse between cleaning and bonding. In the present set-up, there is a minimum unintentional time lapse of 10 min between cleaning and bonding for alignment and wafers transfer. The mid-distribution  $R_c$  value is 3.530 and 3.936 m $\Omega$  for 10 min and 3 hr time lapse, respectively. Therefore, cleaned wafers must be bonded as soon as possible as prolonged exposure is detrimental to the bonding quality. The values translate into an excellent  $\rho_c$  of  $\sim 0.282 - 0.315\ \Omega \cdot \mu\text{m}^2$ . However, these values are much higher than  $\rho_c$  value for Cu grain boundaries ( $< 0.0039\ \Omega \cdot \mu\text{m}^2$ ) [5.3]. Since homogeneously bonded Cu-Cu structure is a mono-metallic system, the measured contact resistance is mostly related to the imperfections at the bonding interface and must be carefully understood as they can have long term reliability concerns.



**Figure 5.6:** Contact resistance distribution of Cu-Cu bonds for two different waiting times between cleaning and bonding.

High resolution transmission electron microscopy (TEM) is used to investigate the Cu grain structures close to the original bonding interface. Two imperfections, a void and tiny precipitates are identified and shown in Figure 5.7 (a) and (b) respectively. The formation of void is related to the initial surface smoothness and planarity. Vacancies in the Cu layers can also coalesce and form micro voids during heat treatment. Void decreases the effective bonding area hence increasing the contact resistance. Tiny precipitates, which are believed to be copper oxide, are found at random places at the bonding interface. Despite pre-bonding cleaning, there is a brief exposure to the ambient during wafers alignment and transfer which allow for the formation of surface oxide. It is possible that this thin oxide layer forms precipitate during bonding and annealing. The presence of oxygen rich precipitates at the bonding interface is confirmed by EDX mapping as shown in the insets in Figure 5.7

(b). Based on the above findings, concerns of electrical reliability related surface imperfections need to be addressed.



**Figure 5.7:** Imperfections at the bonding interface which contribute to the measured contact resistance. (a) Presence of micro-void at bonding interface. (b) Possible copper oxide precipitates formation. (Inset) An oxygen rich area is detected at the bonding interface.

## **5.4 SAM Surface Passivation Method**

To address Cu surface issue that can potentially degrade the electrical performance of the Cu–Cu contacts, SAM is used to retard surface oxidation during exposure in the ambient. This method of passivation prevents both surface oxidation and contamination before thermo-compression bonding. Three sets of wafers were bonded and tested as shown in Table 5.1. In the first set, wafers were passivated with SAM immediately after recess with 3-h waiting time before bonding. The second set of control wafers (without SAM passivation) were aligned and transferred to the wafer bonder immediately with an unintentional  $\sim 0.2$  h of exposure time during wafers transfer. Another pair of control wafers (without SAM passivation) was exposed for  $\sim 3$ -h waiting time between cleaning and bonding, similar to wafer pair 1, which has shown SAM passivation. These experiments are designed to reflect actual situation in the manufacturing environment whereby wafers are placed in a queue since the wafer bonder can only accommodate one pair of wafers at any time. Figure 5.8 compares statistical value of  $R_c$  due to SAM passivation.

**Table 5.1:** Process comparison between wafers with SAM passivation and control groups. Though pre-anneal of SAM desorption is not required for the control groups, it is still needed to maintain the same thermal budget for a fair comparison.

	SAM	Control_1	Control_2
Cu CMP/Acid Clean	Yes	Yes	Yes
SAM Treatment	3 hours immersion	No	No
F2F Alignment & Transfer to bonder	~3 hours	~0.2 hour	~3 hours
SAM desorption	<i>in-situ</i> desorption of SAM at 250 °C	No	No
Bonding Process	350 °C for 1 hr followed by N <sub>2</sub> batch anneal at 350 °C for 1 hr	350 °C for 1 hr followed by N <sub>2</sub> batch anneal at 350 °C for 1 hr	350 °C for 1 hr followed by N <sub>2</sub> batch anneal at 350 °C for 1 hr

An overall improvement is shown with the use of SAM passivation. The contact resistances (at mid-distribution) are estimated as ~3.53 mΩ and ~3.92 mΩ in the second and third sets respectively. With the application of SAM (first set), the  $R_c$  is estimated as ~3.24 mΩ, which represents a reduction of 8.2% and 17.3%, as compared to the second and third sets, respectively. While this reduction is modest, it points to the potential of further improvement in contact resistance at low-temperature bonding (< 350 °C). The improvement may result from different bonding methodologies with optimized metallization and better oxidation control. Figure 5.9 shows different behavior of Cu grains growth for both cases, as explained in [5.4]. The presence of surface oxide presents a barrier for grain growth across the bonding interface when there is no surface treatment. Therefore, *in-plane* Cu grain growth is seen, and *out-of-plane* growth across the bonding interface is very limited. However, Cu surface passivated with SAM provides a cleaner surface to facilitate *out-of-plane*

grain growth across the bonding interface, and a wiggling bonding interface is obtained. Due to the reduction in surface oxide, diffusion of Cu atoms across the interface is promoted, and this results in higher degree of Cu grain growth across the bonding interface. Larger Cu grain size hence leads to an improvement in the contact resistance value when SAM passivation is applied.

In a work previously reported by *Shigetou et al.* [5.5] using surface activation bonding method in UHV ambient, low contact resistance of  $\sim 1$  m $\Omega$  for contact with 3  $\mu\text{m}$  in diameter is obtained. Therefore, perfectly clean Cu–Cu bonding interface maintained in the UHV ambient is advantageous in achieving low contact resistance. The value obtained in this work is higher because the SAM passivation method is performed in the clean-room ambient, and the Cu surface is not completely sealed from oxygen. Nevertheless, relative improvement in contact resistance is confirmed, as discussed above.

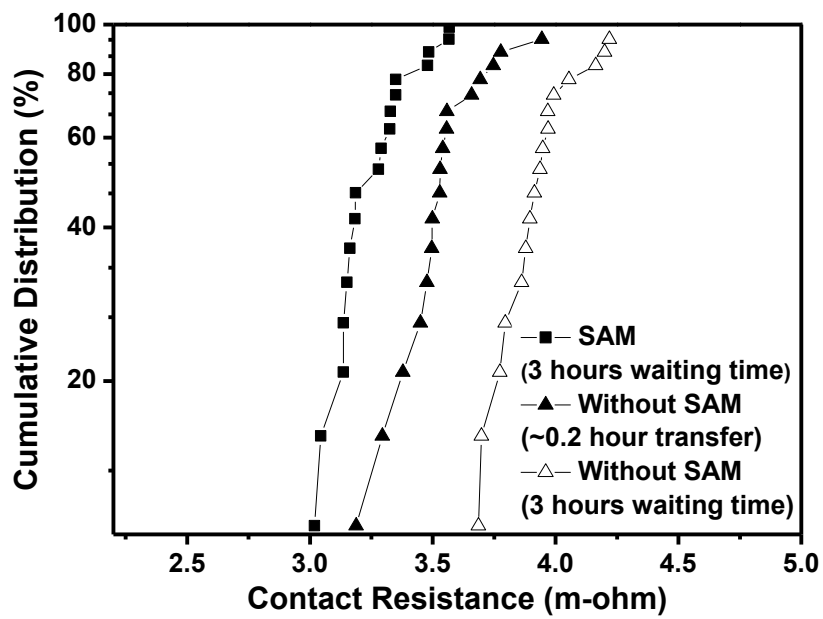


Figure 5.8: Comparison of the contact resistance of the bonded Cu-Cu structure with and without SAM passivation.

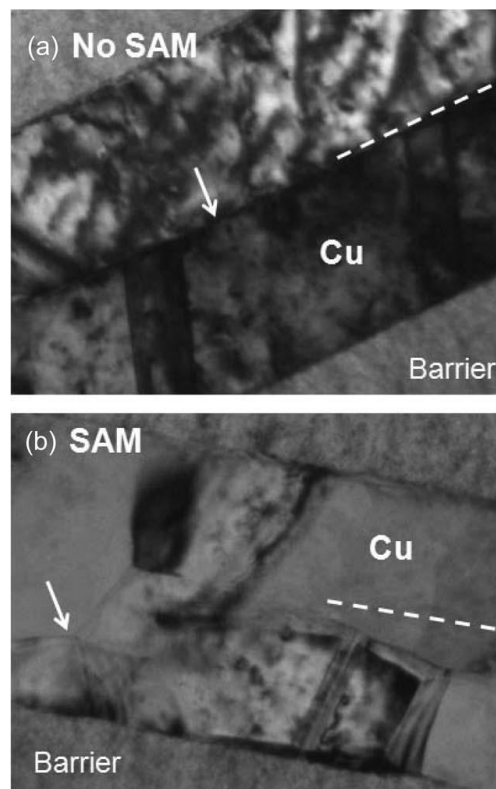
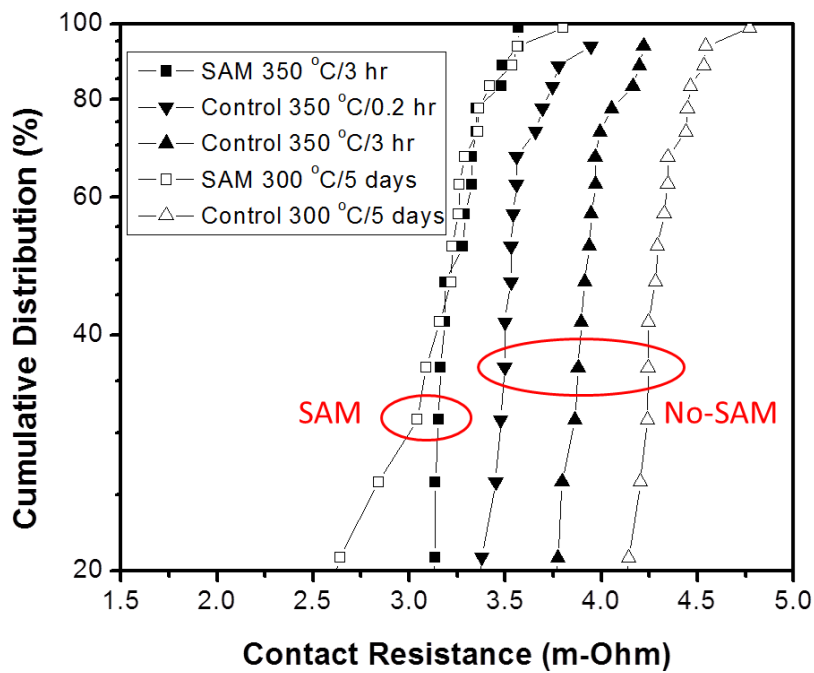


Figure 5.9: Transmission electron microscopy images of the respective Cu grain structures across the bonding interface, (a) without SAM treatment and (b) with SAM treatment.

Finally, the bonding temperature is lowered down to 300 °C and the delay of bonding is extended to 5 days. In Figure 5.10, contact resistances of 10 μm × 8 μm cross-bar structures are compared with respect to different bonding temperature and pre-bonding delay time in the ambient. With the application of SAM, the contact resistance is preserved even with pro-longed exposure in ambient and lower bonding temperature.



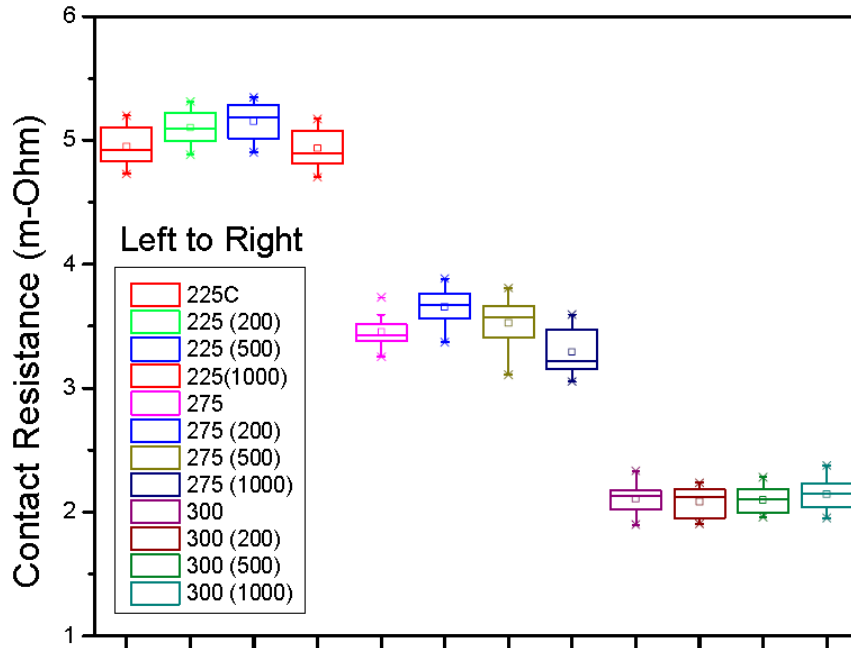
**Figure 5.10:** Summary of the contact resistance of the bonded Cu- Cu contacts at different bonding temperature and pre-bonding exposure time. Note that SAM passivation is effective in shielding the Cu surface from contamination and oxidation, hence preserving the contact resistance of the bonded Cu-Cu contact. The contact resistance of the control samples is sensitive to pre-bonding exposure and bonding temperature.

## **5.5 Thermal Reliability of SAM Passivated Kelvin Structures**

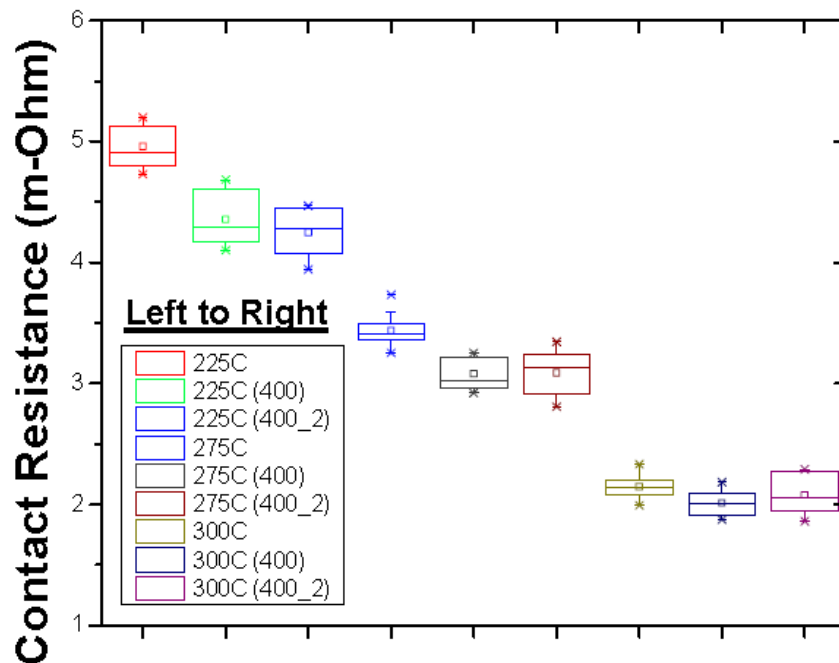
In order to further explore bonding contact behaviors, a second reticle is developed to include bonding contacts with different dimensions and designs. Thermal reliability of SAM passivated Cu-Cu bonds is also focused for the potential application of ultrahigh density interconnection. The wafers are bonded at different temperatures of 225 °C, 275 °C and 300 °C. The temperature of the post-bonding anneal is also lowered down from 350 °C to 300 °C. All bonded wafers were sustained from harsh post-bonding processes including wafer thinning, mechanical dicing and wet etching.

The contact resistance is measured from 20 samples of 5 μm × 5 μm Kelvin structures for each group with different bonding temperature. The evolution Cu-Cu contact during thermal cycling test (TCT, -40 °C to 125 °C) is summarized as a function of bonding temperature in Figure 5.11. At fresh condition, the average contact resistances are observed at ~4.9 mΩ, ~3.4 mΩ and ~2.2 mΩ, respectively. As seen, the bonding temperature has prominent effect on the bond quality for temperature below 300°C even with SAM passivation. However, no open failure is observed even after 1,000 cycles of TCT. It is also observed that Cu-Cu bonds remain thermally stable as there is minimum change in  $R_c$  from all groups of samples up to 1000 thermal cycles..

On the other hand, post-bonding anneal (400°C/30min) cycle improves the initial contact resistance (Figure 5.12) and this allows batch processing after preliminary bonding (single wafer process) hence higher overall throughput. Samples with 225°C bonding temperature are mostly reduced, indicating that the bonding interface is improved by more energetic atom inter-diffusion. After another 30 mins annealing at 400 °C, only samples with bonding temperature of 225°C continued to see a decrease in the mean value of contact resistance.



**Figure 5.11:** Evolution of Cu-Cu contact resistance as function of bonding temperature and thermal cycle. The electrical quality of Cu-Cu bond depends strongly on the bonding temperature. No failure is detected even with 1,000 cycles of TCT.



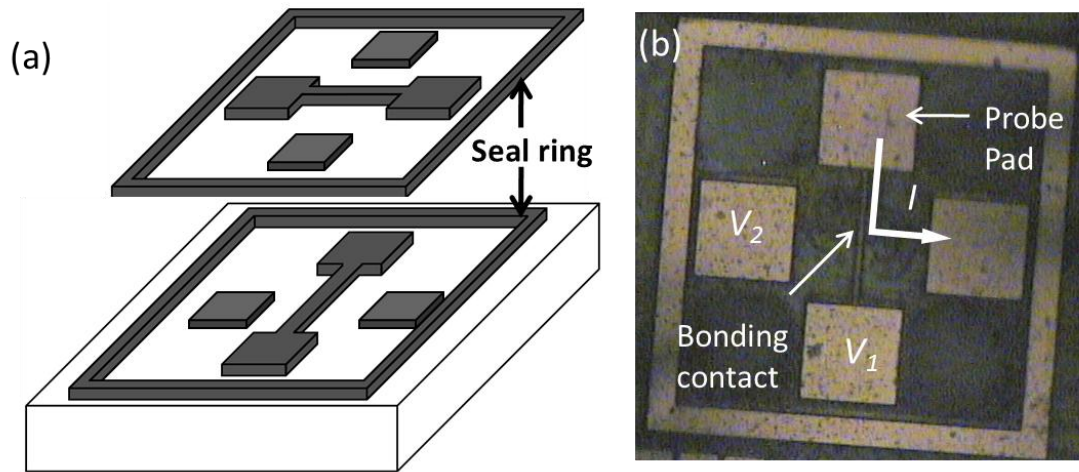
**Figure 5.12:** Evolution of Cu-Cu contact resistance as function of bonding temperature and the number of post-bonding anneal at 400°C/30min. The electrical quality of Cu-Cu bond improves clearly with post-bonding annealing.

## **5.6 Inclusion of Cu Seal Ring**

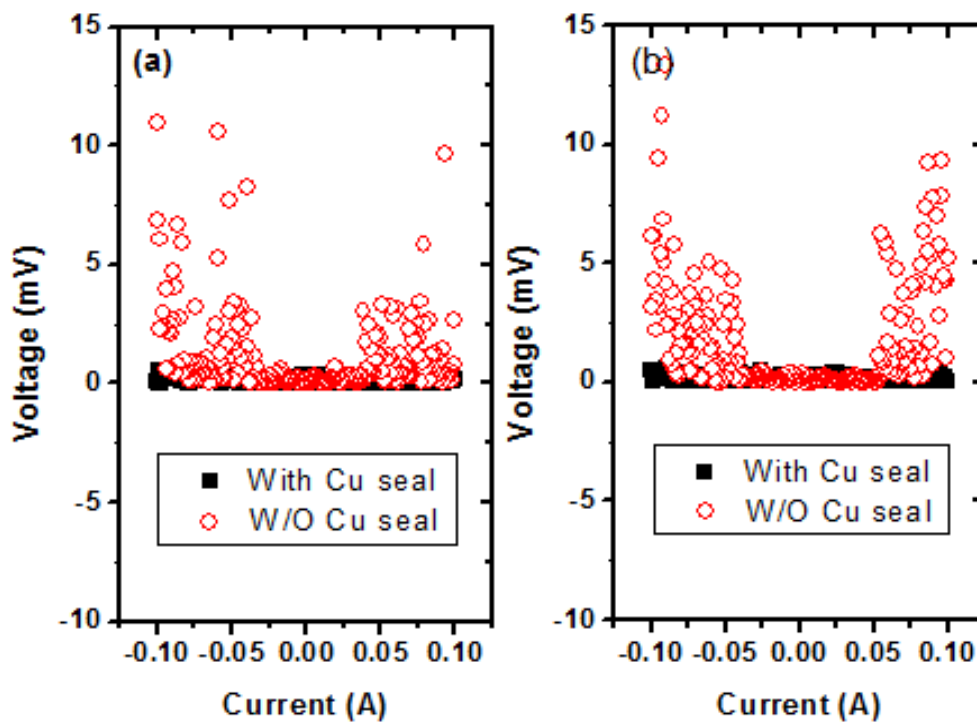
To potentially protect the device from contamination, a simultaneous inclusion of a Cu-Cu seal ring is used in the second reticle for a number of Kelvin structures. Electrical characterization is performed to identify its effectiveness. The structures are conventional cross bar design with/without a 20- $\mu\text{m}$ -width seal ring, as illustrated in Figure 5.13 (a).

Both types of Kelvin structures, with and without Cu seal ring, are adjacent to each other on the same die across the bonding wafer. There are three different contact sizes, 5  $\mu\text{m} \times 5 \mu\text{m}$ , 10  $\mu\text{m} \times 10 \mu\text{m}$  and 15  $\mu\text{m} \times 15 \mu\text{m}$ , respectively. The measurement is taken alternatively on different type of structures across the wafer (Figure 5.13 (b)). It is found that there is no significant difference observed from Kelvin structures with smaller contact sizes (5  $\mu\text{m} \times 5 \mu\text{m}$  and 10  $\mu\text{m} \times 10 \mu\text{m}$ ) with respect to the application of the seal ring.

However, out of the 50 structures tested for the device group containing 15  $\mu\text{m} \times 15 \mu\text{m}$  bonding contact, it is observed that 38% of samples without Cu seal ring start to deviate from an ohmic characteristic at high sweeping current as shown in Figure 5.14 (a). This implies that there is an existence of unstable or variable contact resistance, potentially caused by poor Cu-Cu bond quality. On the other hand, 100% of samples with Cu seal ring present perfect ohmic characteristic. Further, thermal cycling analysis is performed with temperature ranging from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . It is noted that even after 500 cycles, the Cu seal ring has proven to maintain a consistent electrical properties in the shielded devices, in contrast to non-sealed structures with unstable contact, as shown in Figure 5.14 (b).

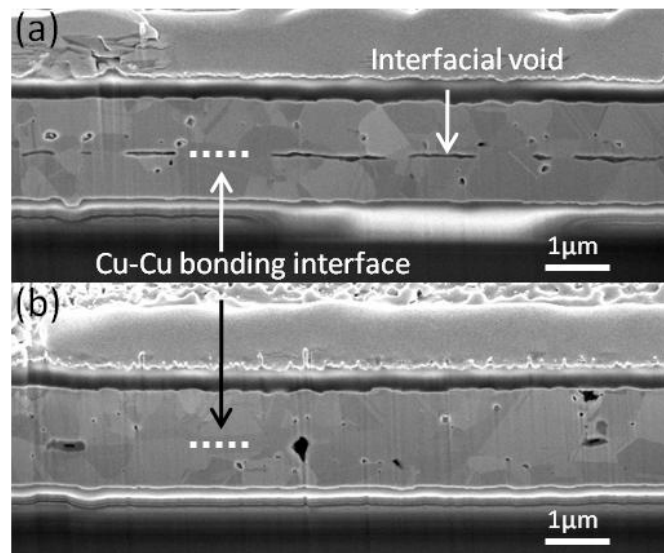


**Figure 5.13:** (a) Schematic of Kelvin structure prior to bonding and (b) Microscopic image of the bonded Kelvin structure for electrical probing.



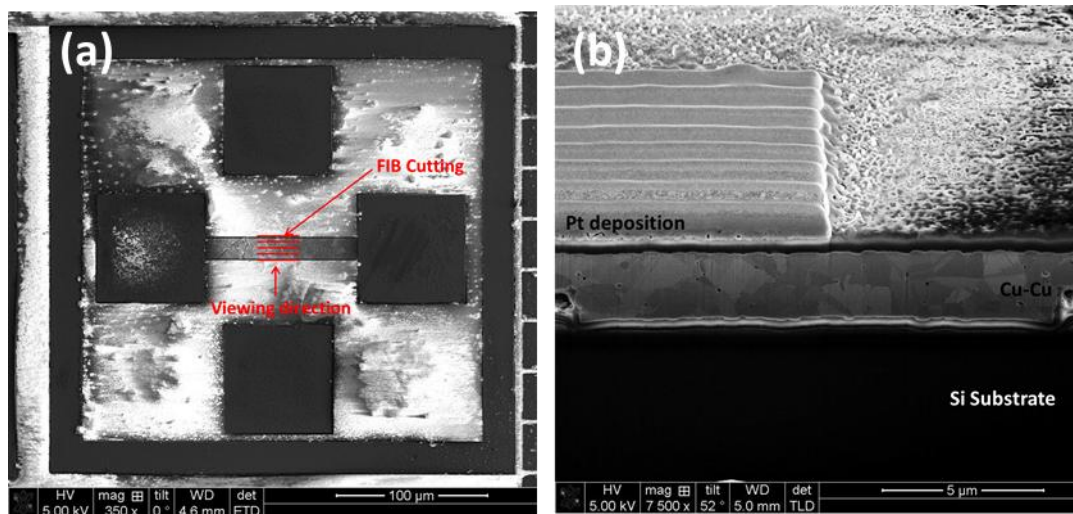
**Figure 5.14:** Relationship between differential voltages  $|V_1 - V_2|$  and the sweeping current  $I$  across the bonding contact for both types of Kelvin structures. (a) at fresh condition, (b) after 500 thermal cycles.

Focus ion beam (FIB) is then used to investigate the bond quality for both cases. Two distinct Cu-Cu bond behaviors can be observed in Figure 5.15. In Figure 5.15 (a) for sample without Cu-Cu seal, the bonding interface is not seamless and >50% of the interface is not contacted. Such non-contact area decreases the effective bonding area and results in an increase of the contact resistance. Under high current, it is suspected that the imperfect contact experiences Joule's heating and this causes instability in the electrical properties. On the contrary, in Figure 5.15 (b), the Cu seal ring has helped to maintain a mechanically uniform bonding condition to the enclosed structures. The inclusion of Cu-Cu seal frame at the periphery provides an extra adhesion force to promote intimate contact between the Cu layers. As a result, stable electrical property is achieved as shown in Figure 5.14 (b). Note that random voids are seen in the entire Cu layer and the origins are previously explained in [5.6].

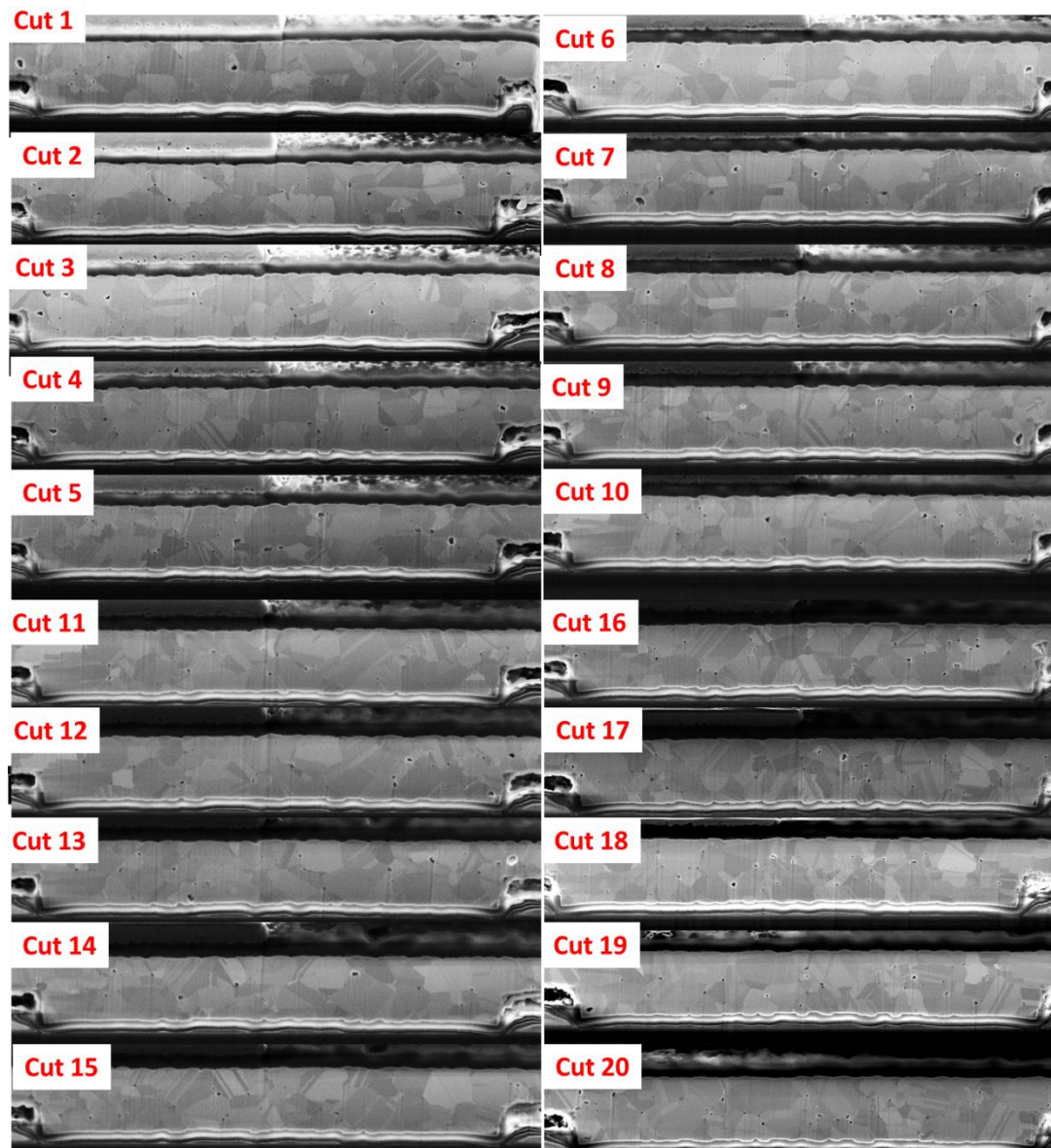


**Figure 5.15:** FIB images of Cu-Cu bond at adjacent Kelvin structures (a) without Cu seal ring, (b) with Cu seal ring.

A comprehensive FIB analysis is used on the sealed Kelvin structure with contact dimension of  $15\ \mu\text{m} \times 15\ \mu\text{m}$  in order to avoid random effect of FIB cut for the misinterpretation on Cu-Cu interface. A number of cuts are performed on the single bonding contact, as shown in Figure 5.16 (a)-(b). Figure 5.17 shows the results of the interfacial behaviors for all cuts. SAM passivation facilitates *out-of-plane* Cu grain growth across the bonding interface from all cross-sections. The bonding interface is uniform with the incorporation of Cu-Cu seal ring. There is no significant interfacial void seen as compared to Figure 5.15 (a). This suggests that the inclusion of the seal ring could potentially promote bonding adhesion on the enclosed Cu-Cu bond, which in turns improve the electrical performance of sealed device.



**Figure 5.16:** (a) SEM image of cutting locations on the Cu-Cu bonds at the intersection of bonded Cu lines. (b) A number of FIB cuts along the Cu-Cu bond of the Kelvin structure.



**Figure 5.17:** FIB-SEM images of the continuous cuts on the bonding contact of a  $15\ \mu\text{m} \times 15\ \mu\text{m}$  Kelvin structure that protected by Cu-Cu seal ring.

## **5.7 Summary**

Kelvin structures have been successfully fabricated and evaluated for measuring the contact resistance under various design and process conditions. The surface oxide and interfacial void are clearly the main contributions to contact resistance of Cu-Cu bond. The use of SAM passivation helps to inhibit surface oxide growth and hence effectively reduces the contact resistance. Low temperature bonding is therefore feasible with help of SAM. Thermal reliability of SAM passivated bonding contacts are proven through stringent thermal cycling test. Finally, the inclusion of a simultaneous Cu-Cu seal promotes overall bonding uniformity. The electrical characterization and qualitative analysis of sealed Kelvin structure prove the effectiveness of Cu seal ring.

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## **Chapter 6**

# **Fine Pitch Cu-Cu bonding system in 3-D wafer-on-wafer stacking**

### **6.1 Introduction**

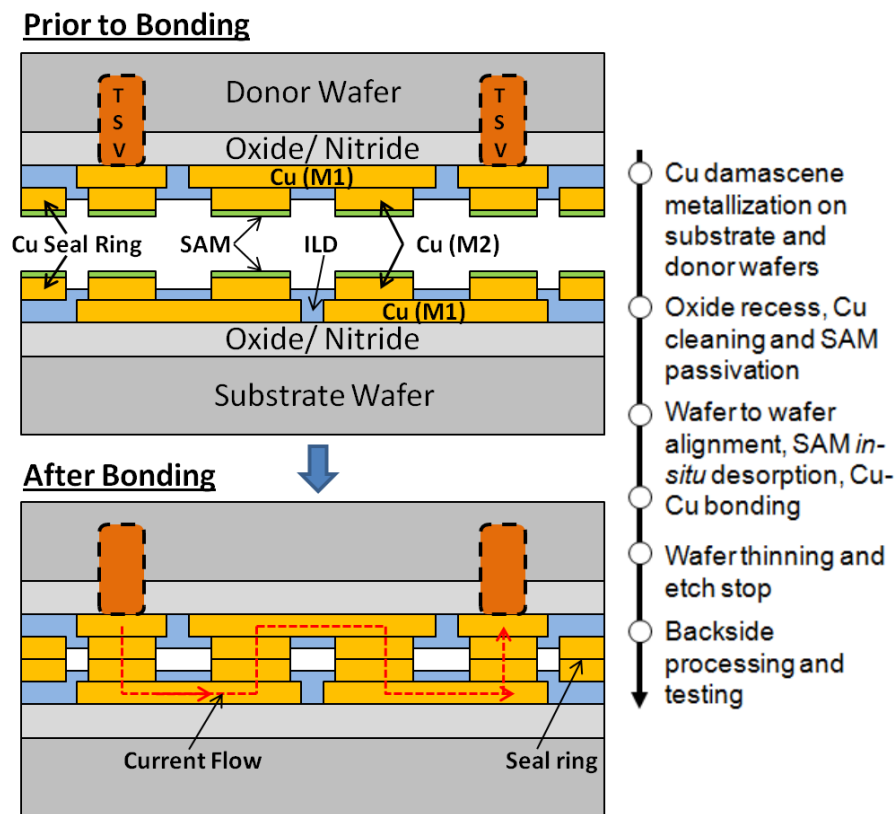
In previous chapters, we discussed the importance of process control, fundamental behavior, and enhancement technique for the formation of wafer level Cu-Cu bonds. All these studies learnt are meant to serve the purpose of this chapter, in which a fine pitch Cu-Cu bonding system needs to be developed to realize an actual demonstration of high density vertical interconnection in 3-D wafer-on-wafer stacking.

Firstly, we demonstrated the fabrication of a 15- $\mu\text{m}$  pitch daisy chain structure using SAM passivation (described in Chapter 4). Electrical and thermal results are then presented followed by mechanical shear test of fine pitch Cu-Cu bonds. Secondly, current stressing result on the fabricated samples is analyzed in details (courtesy of R. I. Made). Thirdly, the pitch size of Cu-Cu contacts is further scaled down to 6  $\mu\text{m}$ , incorporating both passivation method and hermetic seal ring. Finally, 3-D integration of TSV and Cu-Cu bonding is achieved with continued process development.

## **6.2 Daisy Chain of 15- $\mu\text{m}$ -pitch Cu-Cu Bonding**

### *6.2.1 Cu-Cu bonding procedures*

The challenge of wafer level fine-pitch Cu-Cu bonding is to form thousands of tiny bonds simultaneously with good bonding reliability and minimum misalignment error. Therefore, pre-bonding wafer preparation is critical in terms of comprehensive process development and control. In previous chapters, we presented the overview of wafer-to-wafer fine-pitch Cu-Cu bonding process in which fabrication flow, process challenges and optimizations are described. Enhancement methods are discussed and analyzed to further improve the reliability of the bonding system. In this chapter, we demonstrate a high density daisy chain structure based on aforementioned techniques. The fabrication process follows the previous description in Chapter 4. Figure 6.1 shows the process schematic of fine pitch Cu-Cu bonding process including: (1) Cu damascene process that consists of interlayer dielectric (ILD) and recess stop layers deposition, trench formation, TaN and Cu seed sputtering, Cu electroplating, and CMP, (2) Cu exposure with oxide recess followed by surface clean/SAM passivation, (3) Wafer-to-wafer (W2W) alignment, (3) *in-situ* SAM desorption and thermo-compression bonding.



**Figure 6.1:** Schematic illustration and process flow of fine pitch Cu-Cu interconnect formation using face-to-face stacking.

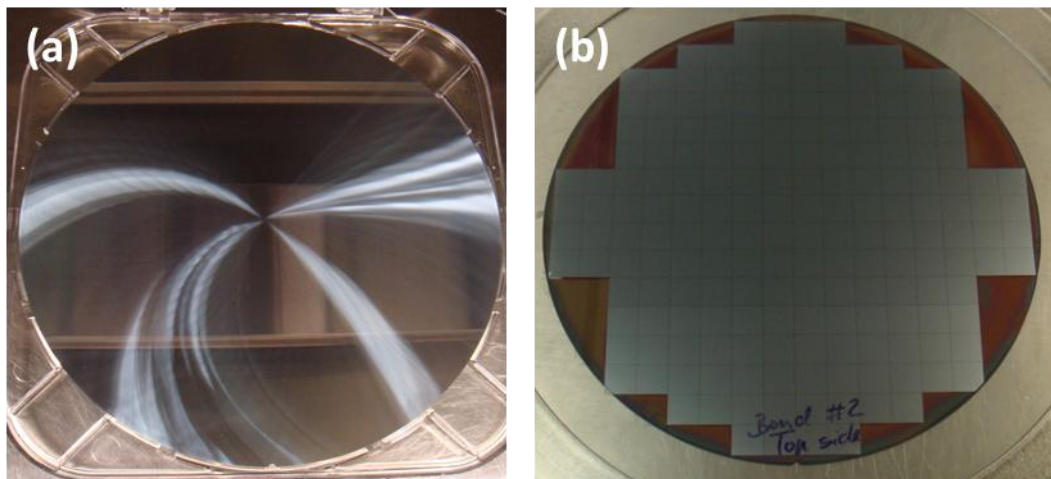
After bonding, the substrate of the donor wafer is thinned down using mechanical grinding. The bonded wafer is then diced into dies with size of 12 mm × 12 mm. The remaining thin Si layer was completely removed by tetra-methyl-ammonium-hydroxide (TMAH), and the dielectric layers underneath were etched by the buffered oxide etchant (BOE). The bonded Cu structures can then be probed directly through the oxide windows.

### 6.2.2 Results and discussion

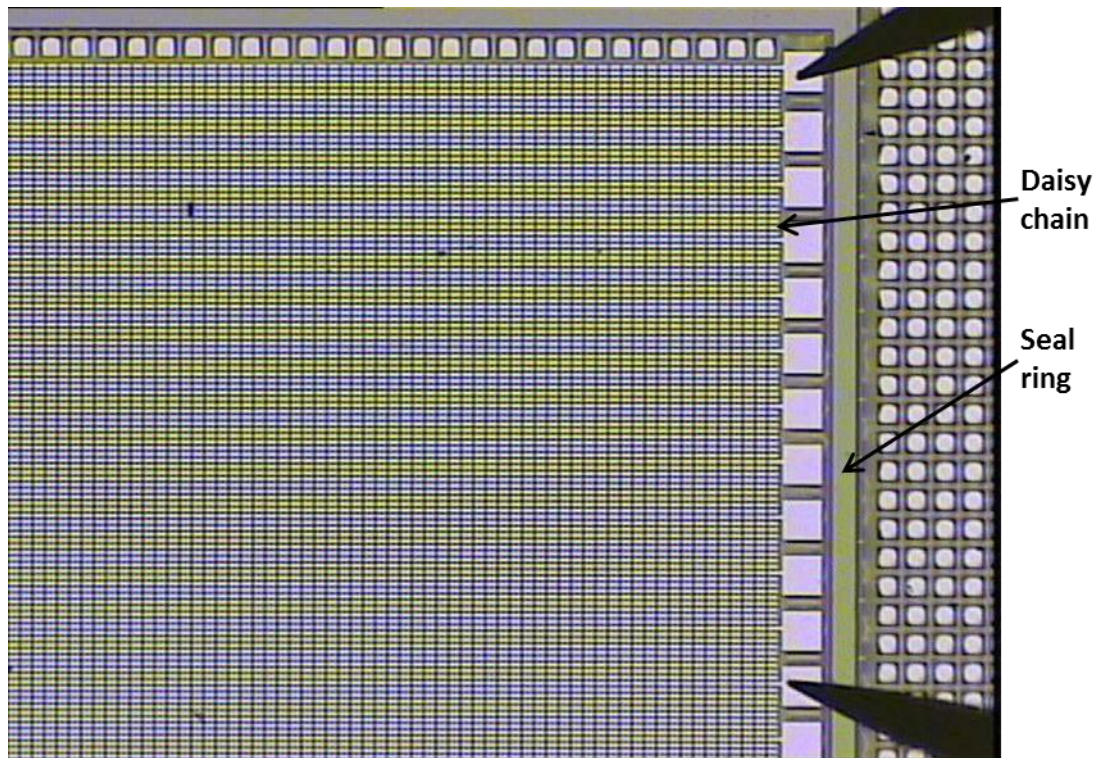
Figure 6.2 shows the post-bonding results. The donor wafer is successfully ground from ~720 μm to ~100 μm without any surface abnormality, suggesting the formation of a mechanically stable bonding interface (Figure 6.2 (a)). Excellent mechanical

bond is demonstrated during subsequent dicing test with 100% yield after wafer dicing into 12 mm × 12 mm dies as shown in Figure 6.2 (b).

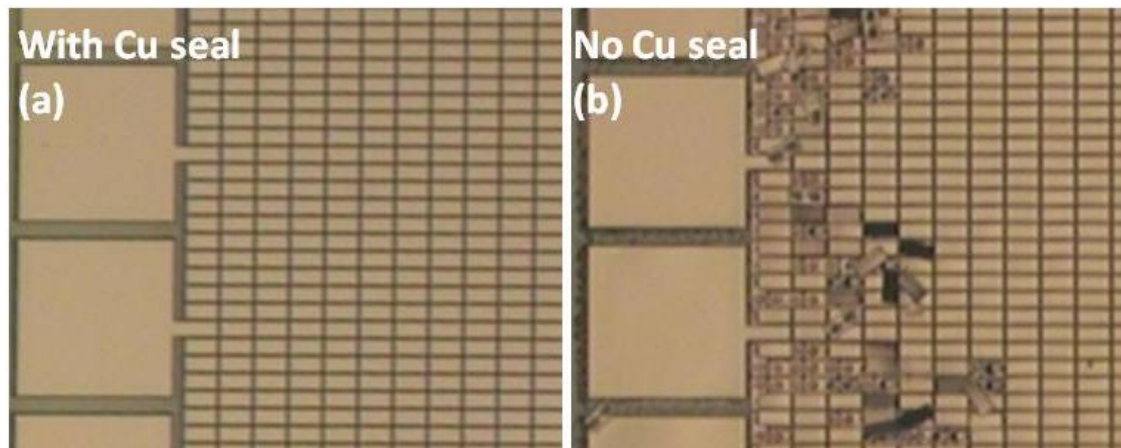
Figure 6.3 is a top-down view of the successful fabrication of the daisy chain. The robustness of Cu-Cu bonds is maintained by the application of Cu seal ring and SAM passivation. The Cu M1 layer of the donor wafer is completely revealed after a combination of wet processes including TMAH and BOE. Cu probing pads are finally exposed for electrical testing. The daisy chain contains a maximum number of 44000 Cu-Cu bonds with 15- $\mu$ m-pitch. A good bonding uniformity is observed across all fine pitch bonding contacts with the inclusion of the Cu-Cu seal ring as shown in Figure 6.4 (a). However, the bonding structure becomes less reliable without the seal ring due to possible exposure to the ambient and mechanical instability as no under-fill was applied in this case [6.1], as shown in Figure 6.4 (b). It can be seen that poorly bonded Cu segments are detached due to non-uniform bonding without the application of seal ring.



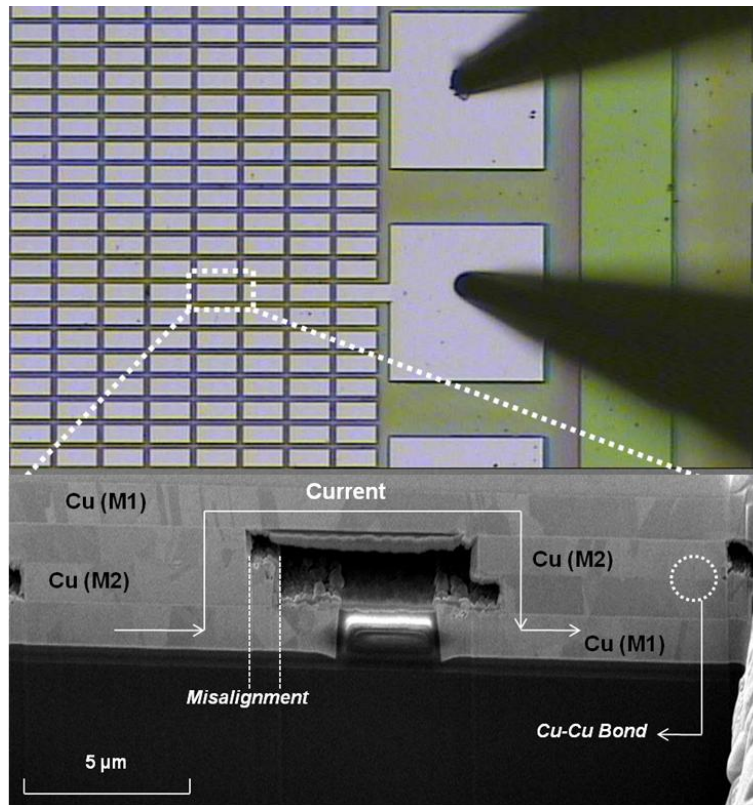
**Figure 6.2:** (a) Thinning of bonded wafer pair with Cu-Cu bonds which act as the mechanically supportive medium. (b) Wafer dicing with 100% yield after thinning process.



**Figure 6.3:** Microscopic image of a 15- $\mu\text{m}$  fine pitch Cu-Cu daisy chain under electrical probing.



**Figure 6.4:** (a) Uniformly revealed daisy chain with Cu seal ring after Si removal; (b) Detached Cu bonding structures without Cu seal ring.



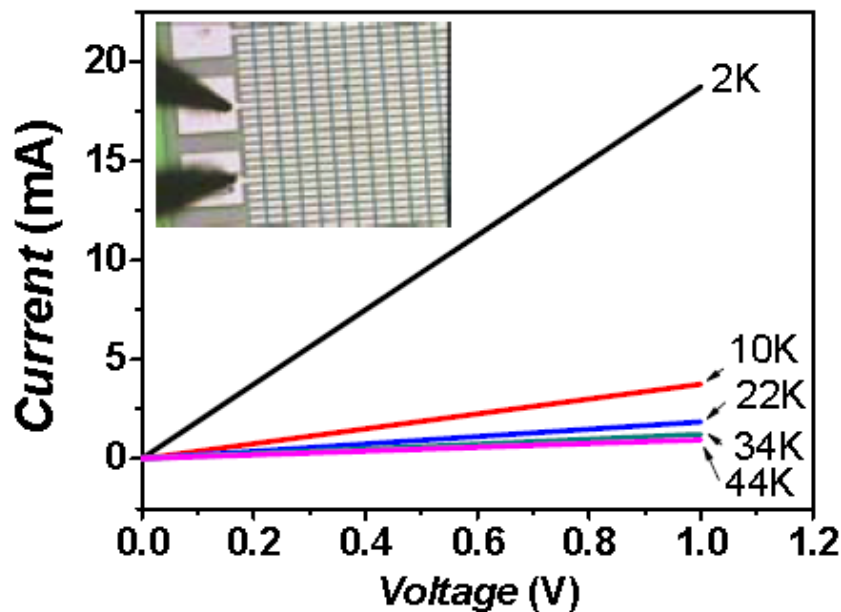
**Figure 6.5:** Daisy chain with a pitch of 15  $\mu\text{m}$  formed by Cu–Cu bonding used for bonding uniformity study. Each probing interval has 2000 contacts.

Figure 6.5 shows the FIB image of the final bonding structure on a randomly selected Cu wire with 15- $\mu\text{m}$ -pitch. Seamless Cu–Cu bond is formed such that current flows in an inter-strata manner.  $\sim 1\text{--}2\ \mu\text{m}$  misalignment and excessive etching of ILD are also observed.

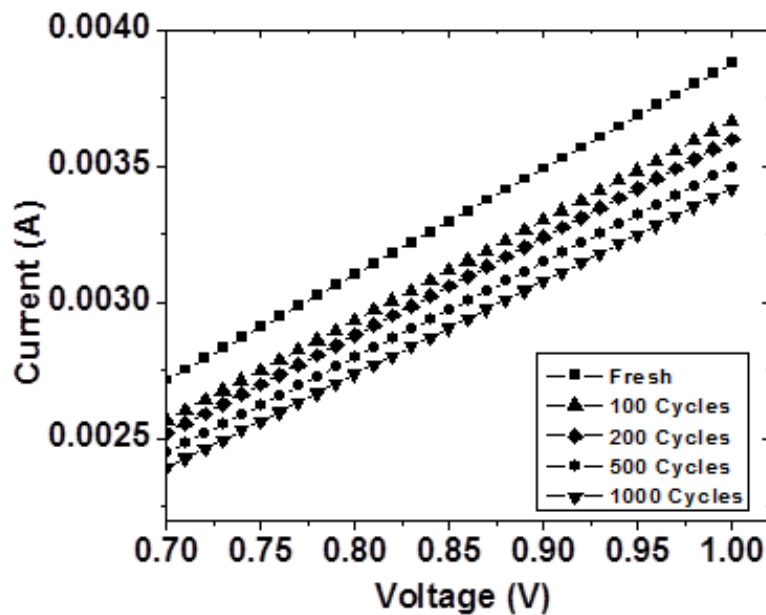
The fine pitch daisy chain is subsequently characterized with a successful and continuous connection. A linear increase in the total chain resistance with every 2000 nodes increment is presented in Figure 6.6. Each node consists of one Cu–Cu contact (M2-M2) and one Cu line (M1). A single failure of Cu–Cu bonding node would have resulted in an open circuit failure during electrical measurement. No open failure is detected during the electrical measurement. This represents a 100% bonding yield,

and an interlayer interconnect density of  $4.4 \times 10^5 \text{ cm}^{-2}$  is achieved. This verifies that SAM does not introduce any undesired artifact to the bonding process. In freshly bonded sample, the resistance of the daisy chain is estimated from  $I$ - $V$  plot, and each node (consists of Cu lines and contact) is estimated to have  $\sim 26.1 \text{ m}\Omega$  of resistance.

To verify the robustness of SAM assisted Cu-Cu bonding, the sample is subjected to TCT with temperature ranging from  $-40 \text{ }^\circ\text{C}$  to  $125 \text{ }^\circ\text{C}$ . Figure 6.7 shows the  $I$ - $V$  measurement of daisy chain with SAM passivated Cu-Cu contacts at  $15\text{-}\mu\text{m}$ -pitch with different thermal cycles. It is observed that the electrical continuity is maintained even after 1000 thermal cycles, suggesting that the robustness of the Cu-Cu bond is maintained, with the application of SAM.

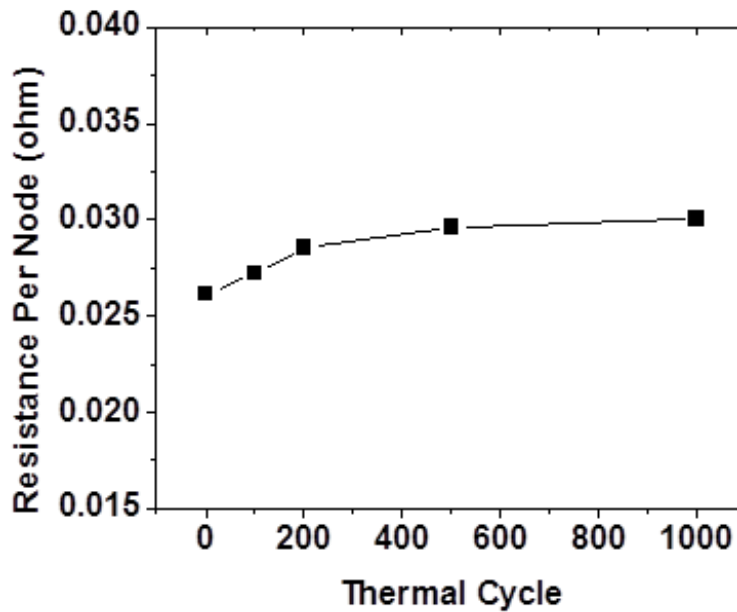


**Figure 6.6:**  $I$ - $V$  characteristic of the daisy chain measured from 2,000 to 44,000 contacts (each interval = 2,000 contacts). The contacts ( $15 \mu\text{m}$  pitch) are connected continuously and ohmic behavior is exhibited.



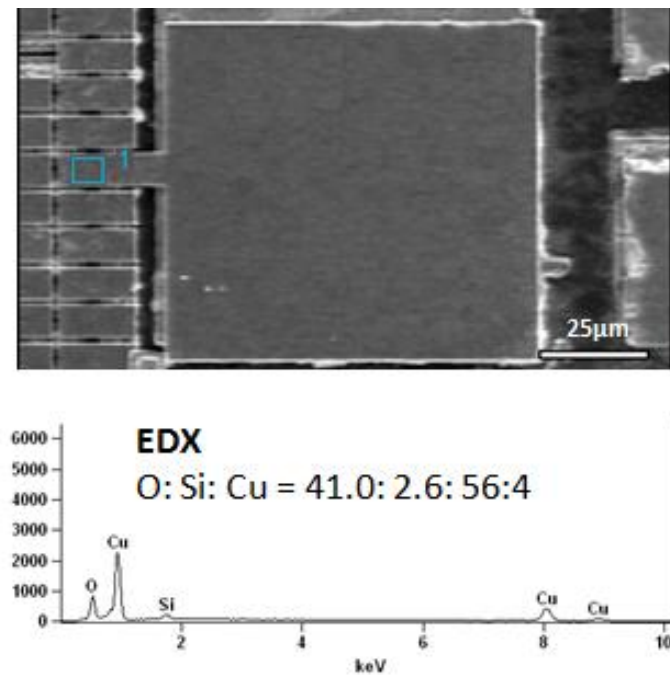
**Figure 6.7:** Daisy chain presents continuous  $I-V$  before and after thermal cycling. No open failure is detected.

Comparing the  $I-V$  characteristics of the fresh sample and thermally stressed sample, a reduction in current is measured after thermal cycling. However, the reduction rate becomes slower as the number of cycle increases, as shown in Figure 6.8. This results in a slight increment of the node resistance to  $\sim 29$  m $\Omega$  at 1000 thermal cycles. This degradation in line resistance saturates with further thermal cycling test. The degradation in the node resistance is due to the fact that the Cu structures are exposed to the ambient due to chemical etching during donor wafer thinning, which is not fully optimized. As a result, they are corroded during thermal cycling, and the Cu lines become more resistive. As the surface oxide layer grows thicker, it sets a barrier for subsequent oxygen to oxidize the Cu surface further; therefore, the oxidation rate slows down, and the increment in resistance per node saturates.

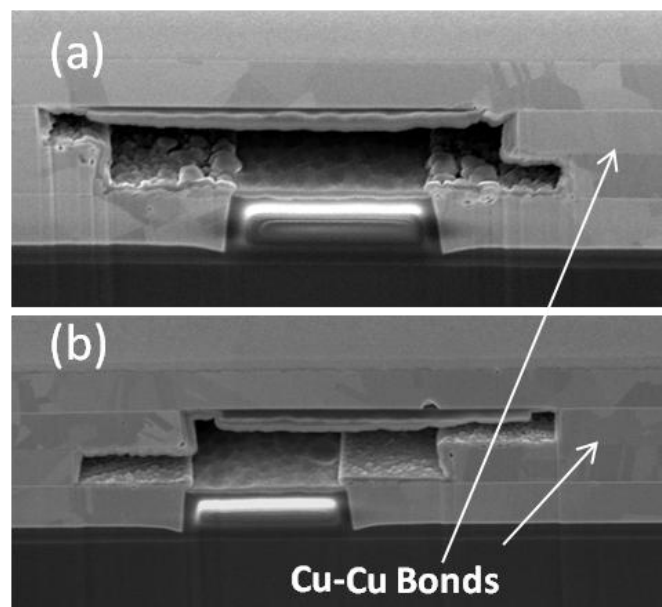


**Figure 6.8:** The node resistance degradation during thermal cycling.

EDX analysis in Figure 6.9 further shows that exposed Cu line surface gets oxidized during TCT. During oxidation, cuprous oxide ( $\text{Cu}_2\text{O}$ , also known as red oxide) initially forms, followed by cupric oxide ( $\text{CuO}$ , also known as black oxide) [6.2].  $\text{CuO}$  is the preferred form when the oxidation temperature is high. The oxide on the Cu line is mostly  $\text{CuO}$ , and this is reflected in the elemental composition obtained from EDX in Figure 6.9. We rule out failure at the Cu–Cu bonding interface as the Cu–Cu interface is intact after 500 thermal cycles based on the FIB image, as shown in Figure. 6.10 (b). A single failure of Cu–Cu bonding node will result in an open circuit during electrical measurement, but no such failure is detected after thermal cycling. The effect of increasing resistance is also reported by *Shigetou et al.* [6.3], suggesting that the prevention of Cu exposure would be highly desired in an optimally designed test structure. In actual 3-D IC flow, the Cu–Cu bonding interface can be electrically probed using TSV, without the need for extreme thinning and exposure to the ambient.



**Figure 6.9:** Since the Cu structures are exposed to the ambient due to chemical etching, they are oxidized, and this is confirmed by the EDX analysis.

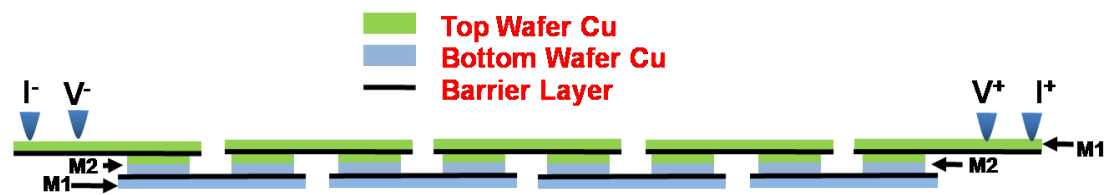


**Figure 6.10:** FIB SEM images of fine pitch Cu-Cu bond (a) At fresh condition. (b) after 500 thermal cycles. The Cu–Cu contact sustains 500 cycles of thermal stressing, and no defect is observed. The ILD is unintentionally removed during wafer thinning.

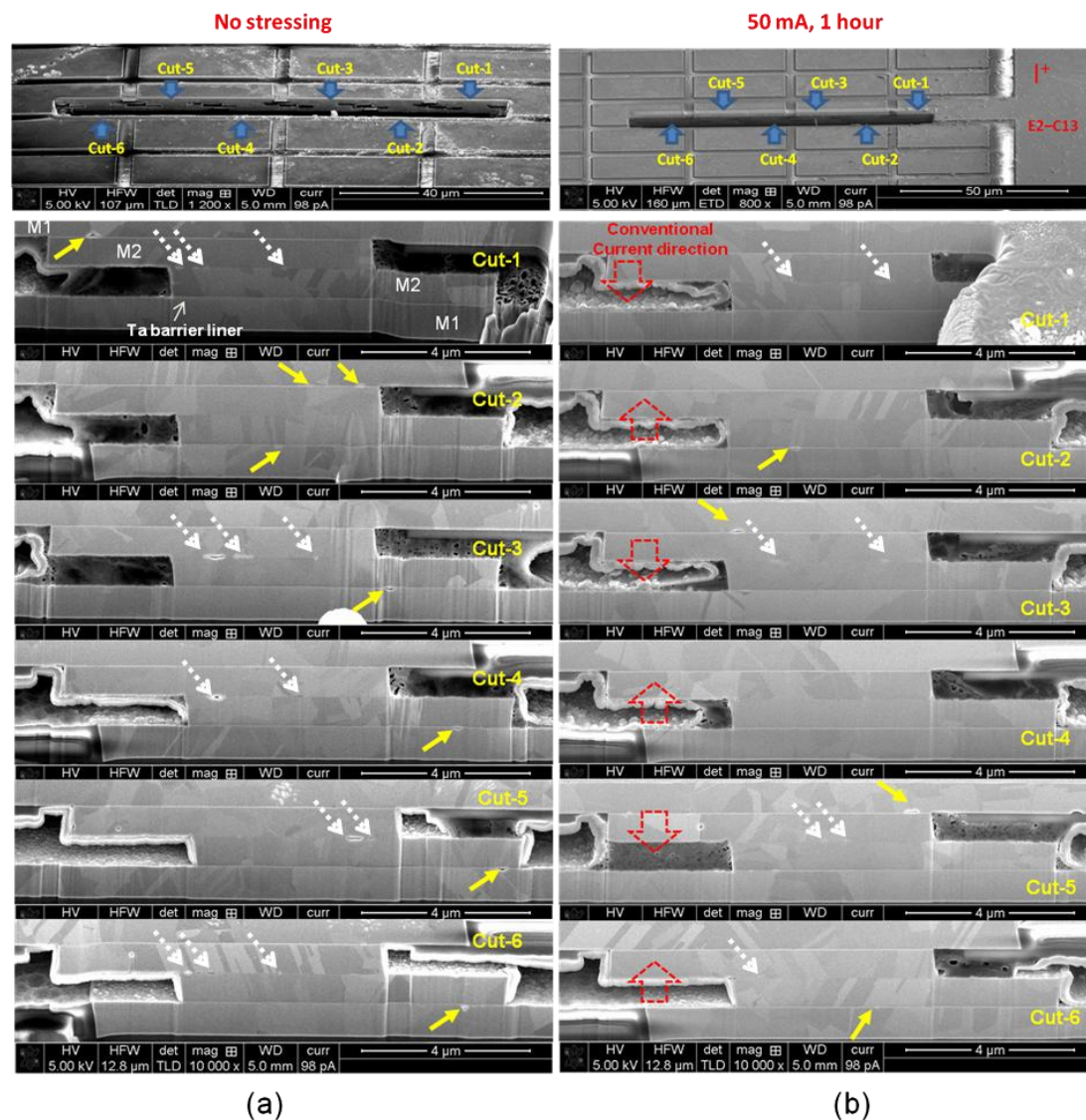
### 6.3 Current Stressing on Cu-Cu Daisy Chain

It is important to investigate the evolution of Cu-Cu bond interface under prolonged current stress by combining electrical current stressing and bond interface cross-sectional analysis. Voids at the bond interface were observed to be driven by electromigration (EM) to the adjoining interconnect line, leading to early failures of the line. This may have significant impact on the future of 3-D IC technology that utilizes Cu-Cu bonding, and it may be mitigated by inserting a barrier layer in between the bond interface and the interconnect line.

Electrical stressing was carried out on the daisy chain structures as illustrated in Figure 6.11. The implementations of Cu seal ring and SAM passivation are used in this case. The current source and ground terminal were placed in such a way that the stress current flowed through the bond interface. At the same time, the voltage drop across the interface was monitored from  $V^+$  and  $V^-$  terminals.



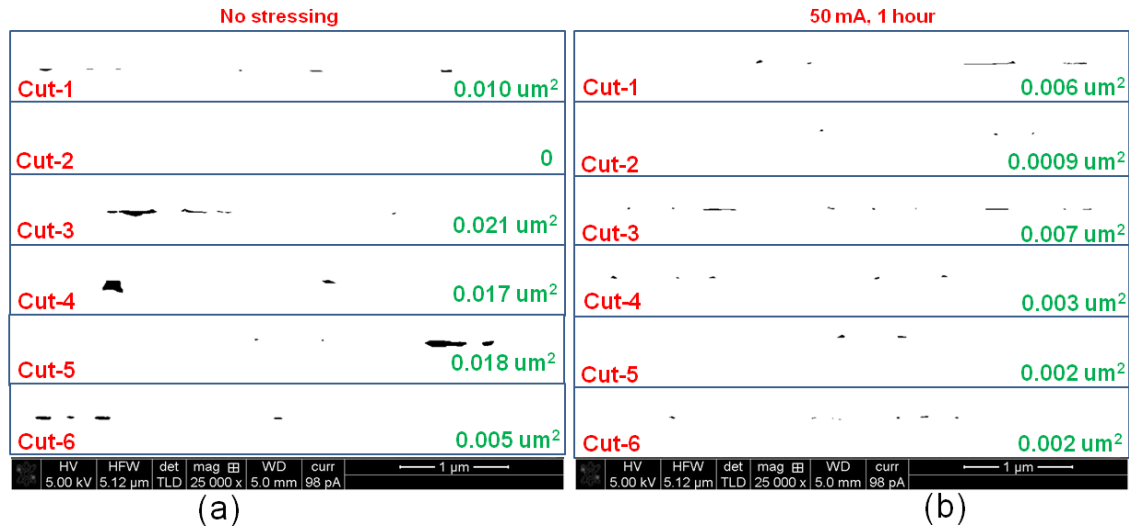
**Figure 6.11:** Current stressing on daisy chain structure.



**Figure 6.12:** FIB-SEM cross section comparison between daisy chain structures that were subjected to current stressing. Solid and dashed arrows and hollow dashed arrows point to voids found between barrier and M1- Cu interface, voids found on the bonding interface and current direction, respectively. (a) No current stressing, (b) 50 mA for 1 hour.

FIB-SEM was used to characterize the bond interface, and GIMP and ImageJ software were utilized to quantify the interface voids, as shown in Figure 6.12. It is observed from the daisy chain that had gone through 1 hr stressing with 50 mA shows

less voids at the bond interface as compared to non-stressed daisy chain structures. These observations have been confirmed by void quantity analysis, as shown in Figure 6.13. Another interesting observation is that, after current stressing, more voids were observed to accumulate at the barrier-Cu M1 interface, as pointed out by solid arrows in Figure 6.12. The presence of Ta between M1 and M2, could effectively block any materials transfer between the two metallization, which means that those voids can only originate from the interconnection lines instead of the bond interface. Therefore, usage of barrier layer between interconnection line and the bond interface could thus help to prevent the interconnection-bond interface coupling effect. However, by doing that, it also undesirably increases the total interconnection resistance.



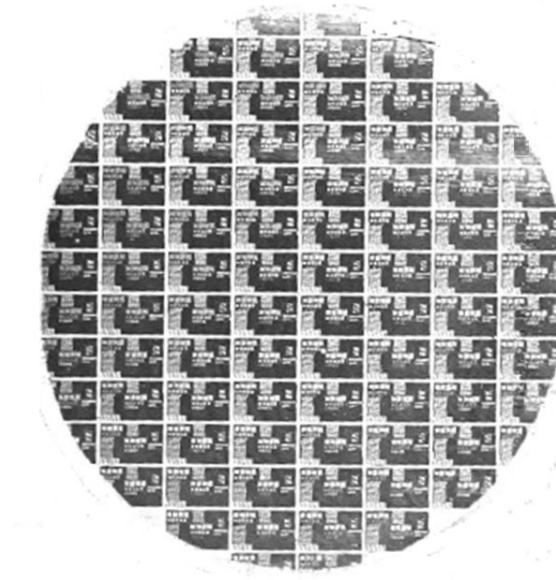
**Figure 6.13:** Voids quantification and comparison of stressed and non-stressed daisy chain from SEM-FIB cross section images by ImageJ, stressed structure has lower average void quantity. (a) non-stressed daisy chains, (b) stressed daisy chain with 50 mA current for 1 hour.

## **6.4 Ultrafine Pitch Evolution of Cu-Cu Bonded Interconnects**

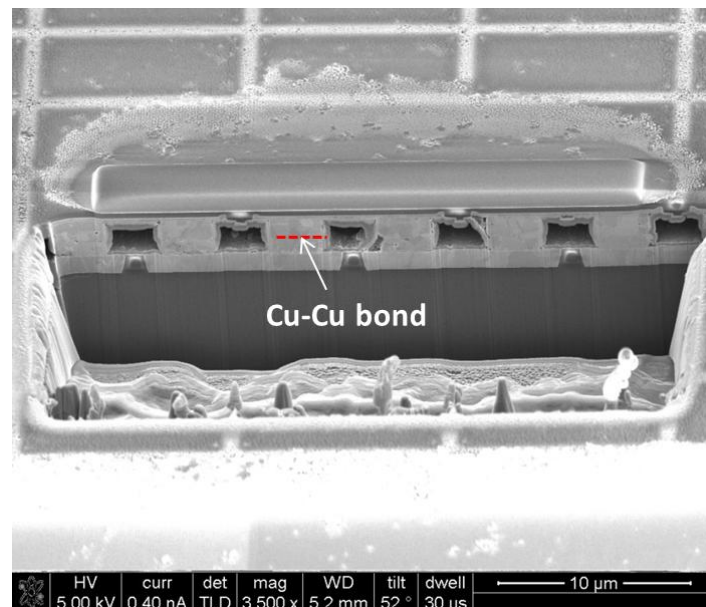
The continuous scaling of bonding pitch is inevitable due to Moore's law. Current state of art TSV has been demonstrated to reach a pitch of  $< 10 \mu\text{m}$  [6.4]. However, there is a huge challenge for Cu/Sn micro-bump in achieving such tight pitch [6.5]. Hence, the use of ultrafine pitch Cu-Cu bonding in conjunction with TSVs is much more feasible from a manufacturing perspective. If successful, it can bridge the gap to serve the future needs of high density 3-D applications. Based on the successful development of the  $15\text{-}\mu\text{m}$ -pitch of high density Cu-Cu bonds, Cu sealing frame is integrated with excellent helium leak rate to the bonded structures to promote the overall bond reliability. On top of that, temporary passivation of Cu surface using self-assembled monolayer (SAM) enhances the resistance against oxidation and particle contamination. Hence, it opens up new opportunity for wafer level integration of Cu-Cu bonding with state-of-the-art TSV technology, enabling future ultrahigh density 3-D IC applications.

With SAM passivation, low bonding temperature ( $300 \text{ }^\circ\text{C}$ ) was applied to bond the pairing wafers for 1 hr followed by a post bonding anneal at  $300 \text{ }^\circ\text{C}$  for 1 hr. Uniform Cu bonded structures are achieved at wafer level, as confirmed by the *c*-SAM image as shown in Figure 6.14. After further processing, the fine pitch daisy chain structure was revealed and analyzed using a combination of focus ion beam and scanning electron microscopy (FIB-SEM), as shown in Figure 6.15. Seamless Cu-Cu bonding interfaces are observed along the chain. For the case of W2W bonding with a smaller pitch size of  $6 \mu\text{m}$ , there was a misalignment of  $5 \mu\text{m}$  along the Y-axis during the bonding process. Hence, the final number of successful bonds is drastically reduced to 100 (one complete row along the x-axis). Should there be minimum misalignment, an ultrahigh IC-to-IC connection density of  $\sim 2.6 \times 10^6 \text{ cm}^{-2}$  can be

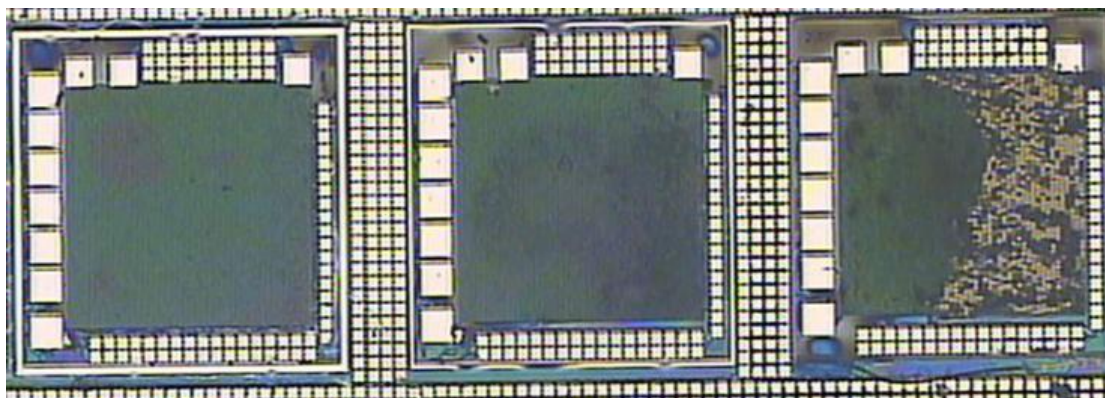
formed, which is a 6X increment in density from the previous achievement of  $\sim 4.4 \times 10^5 \text{ cm}^{-2}$  for 15  $\mu\text{m}$  pitch. Nevertheless, for this case, the 100 successful bonds are sufficient for us to adequately characterize the electrical characteristics of the chain.



**Figure 6.14:** *c*-SAM image of wafer level Cu-Cu bonding interface.



**Figure 6.15:** FIB-SEM image of continuous daisy chain structure with seamless Cu-Cu contact.

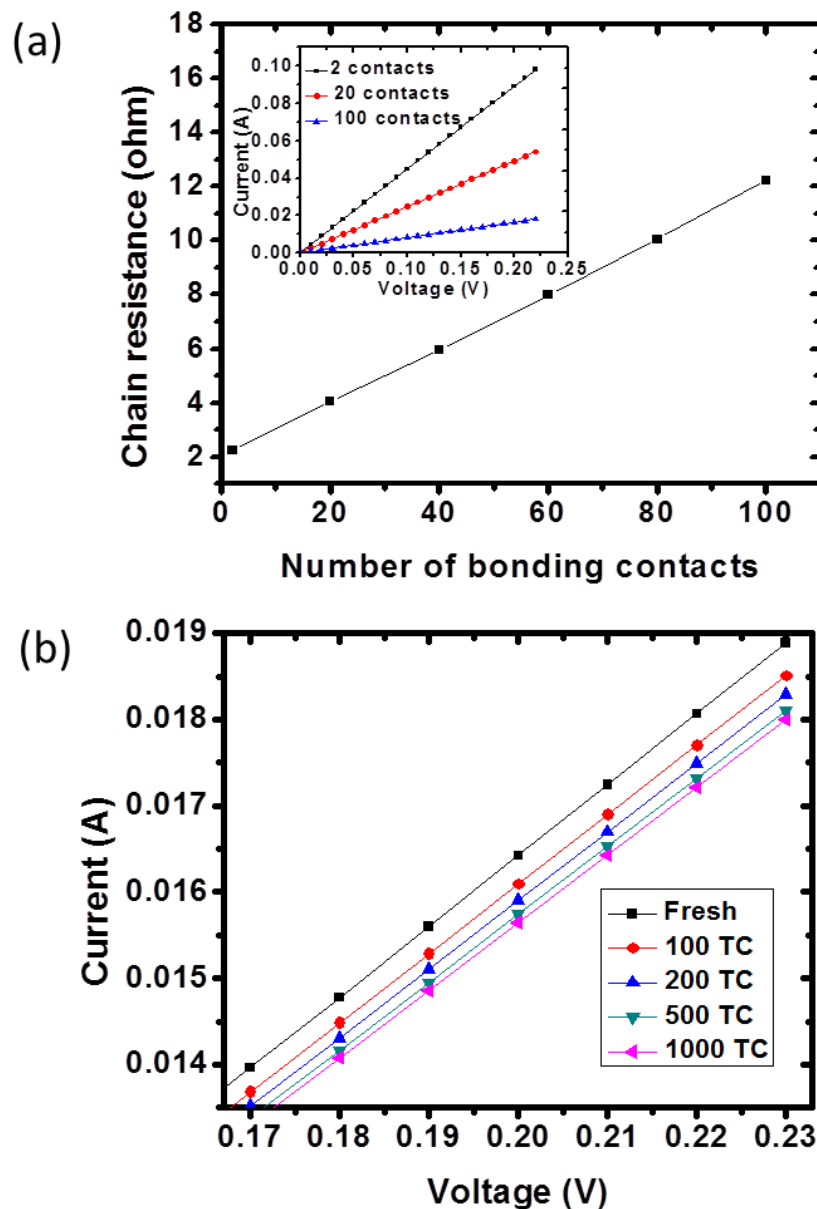


**Figure 6.16:** The robustness of Cu-Cu seal ring is ensured when the ring width is  $\geq 20\mu\text{m}$ . Below that, the ring collapses during wafer thinning.

The structure enclosed by the 20- $\mu\text{m}$  width Cu seal ring as described has clearly proven to enhance the robustness of the daisy chain structure. The ring is most reliable in undergoing harsh mechanical process steps when it is  $\geq 20\ \mu\text{m}$ , as shown in Figure 6.16. From left to right of the chain structures adjacent to each other, the widths of the seal rings are 20  $\mu\text{m}$ , 10  $\mu\text{m}$  and 5  $\mu\text{m}$ , respectively. For the daisy chain enclosed by a 5  $\mu\text{m}$  Cu-Cu seal ring, the protected fine pitch bonding structures collapse due to mechanical thinning and dicing process. It is also observed that the seal ring could not sustain by itself. With a 10  $\mu\text{m}$  Cu-Cu seal ring, the structures are better protected. However, minor failures still occur after magnified imaging. For 20  $\mu\text{m}$  structure, no single failure is observed and it suggests an excellent encapsulation.

During the electrical characterization of 20  $\mu\text{m}$  sealed structure, fine pitch (6- $\mu\text{m}$ ) daisy chain with 100 bonding nodes is successfully connected continuously as shown in Figure 6.17. The total chain resistance consists of Cu-Cu contacts and Cu lines (as illustrated by M2-M2 and M1 in Figure 6.17 (a)). The inset of Figure 6.17 (a) shows that linear  $I$ - $V$  behavior is observed from 2 to 100 contacts. TCT up to 1000

cycles again proves that the use of SAM passivation does not compromise pitch scaling and reliability of Cu-Cu bonding (Figure 6.17 (b)). The slight increase of the total resistance follows the same effect which is seen on 15  $\mu\text{m}$  daisy chain structure.



**Figure 6.17:** (a) Linear increment of total chain resistance with number of bonding contacts. (Inset) Linear  $I$ - $V$  characteristics from daisy chain containing 2 to 100 contacts. (b)  $I$ - $V$  characteristics of daisy chain containing 100 contacts with different number of thermal cycles.

## **6.5 3-D Stacking using TSV and Cu-Cu Bonding Integration**

### *6.5.1 Introduction*

In an actual 3-D integration, bonding technique has to be associated with Through-Silicon-Via (TSV) technology in order to form a complete inter-layer connection to serve functionalities such as signal transfer, power delivery, heat conduction and mechanical support [6.6]. Therefore, the integration of both is vitally important for the entire 3-D implementation process. In this chapter, we demonstrate the feasibility of integrating TSV and Cu-Cu bonding on wafer-to-wafer stacking, incorporating the enhancement schemes we have discussed in the previous chapters. Integration challenges and system reliabilities will be focused in this chapter.

### *6.5.2 TSV approaches*

TSV technology is an enabler of 3-D system integration in which two or more active layers are involved in the vertical direction [6.7]. It is typically demonstrated by using deep trench via etch up to the depth of a few hundreds of microns through the silicon substrate. The trench is then covered with dielectric layer for the isolation, followed by filling material such as poly-Si, copper or tungsten. After further 3-D processing, the adjacent active layers are communicated via the vertical path supported by TSV and conductive bonding material.

The implementation of TSV can be classified into three major categories namely, “via first”, “via middle” and “via last”. In the “via first” implementation, the TSV is always formed before any process steps for device fabrication. If the TSV is formed in between front end of line (FEOL) and back end of line (BEOL) processes, it is then called “via middle”. Accordingly, “via last” process indicates that the TSV is fabricated after all CMOS processes are completed. The selection of the

implementation approach depends on the actual requirement of the specific application.

On the other hand, when the TSV wafer is ready for stacking, there are two major options related to the stacking orientation. One is called face-to-face (F2F) stacking approach when both IC layers are facing each other. After alignment and bonding, the backside of the top wafer will be thinned down until the TSV are fully exposed. This method allows a high density layer to layer interconnection which is limited by the W2W alignment accuracy. No additional handle wafer is required in F2F stacking and this imposes more stringent requirement on the mechanical strength of the bonding interface in order to sustain shear force during wafer thinning. However, as the IC layers are close to each other and isolated by the ILD layers after bonding, heat dissipation becomes challenging. Back-to-face (B2F) stacking is the other implementation, in which both IC chips are stacked with the same facing. The IC layers are now separated by a thin substrate layer interconnected by TSV. This method makes use of a temporary handle and the layer to layer interconnection density is limited by the TSV pitch. When top device layer is bonded to a temporary handle, wafer thinning is required for backside TSV exposure which is similar to F2F approach. Therefore the temporary bond has to sufficiently strong to maintain the mechanical stability. Subsequently, the permanent bond is formed by bonding the exposed TSV to the pairing IC layer. Finally, the temporary bond can be released when the stacking is successful.

### *6.5.3 Integration process of TSV and Cu-Cu bonding*

In this demonstration, via first process is used in this integration scheme. The developed Cu-Cu bonding technique and a 30- $\mu\text{m}$ -depth TSV with an aspect ratio (AR) of 3 are integrated by F2F stacking. The process flow is as shown in Figure 6.18. In the first step, a TSV mask was used to define the TSV pattern with a diameter of 10  $\mu\text{m}$  using photo-resist (PR) (Figure 6.18 (a)). In order to achieve the targeted TSV trench depth during the deep reactive ion etch (DRIE) process, a thick layer of PR (1  $\mu\text{m}$ ) is used. Subsequently, DRIE is carried out to create the initial TSV trench, as shown in Figure 6.18 (b). The deep TSV silicon trench can be ranged from a few micro-meters to few hundred of micro-meters in depth. The deep silicon etch was done using the standard BOSCH processes carried out inside a multiple inductively coupled plasma etching system [6.8].  $\text{SF}_6$  and  $\text{O}_2$  were applied as gas source in the Si etching cycle while  $\text{C}_4\text{F}_8$  was applied during the sidewall passivation cycle. The alternate process of deposition and etch is repeated continuously until the required trench depth (30  $\mu\text{m}$ ) is achieved. Due to the strong isotropic nature of the  $\text{SF}_6/\text{O}_2$  etch chemistry, each etch cycle will form an unwanted sidewall recess known as a scallop, which needs to be suppressed as it potential creates voids during TSV refilling. The formation of this scallop will repeats with each etch cycle [6.9, 6.10], as shown in Figure 6.19.

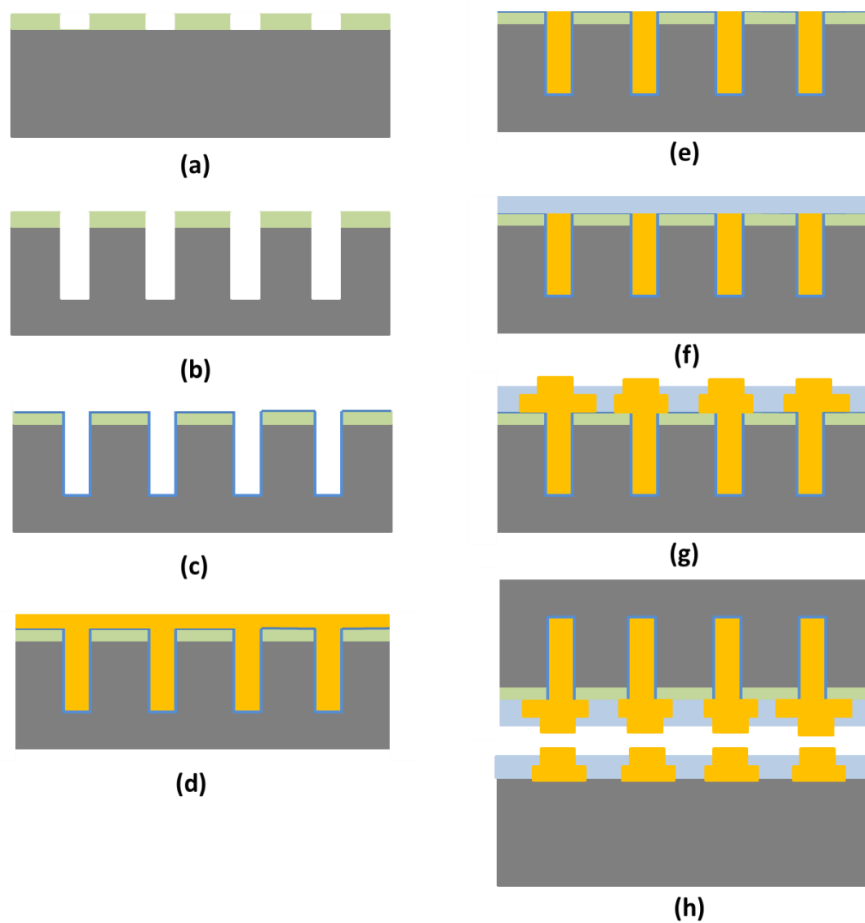


Figure 6.18: Schematic process flow of TSV and Cu-Cu bonding integration.

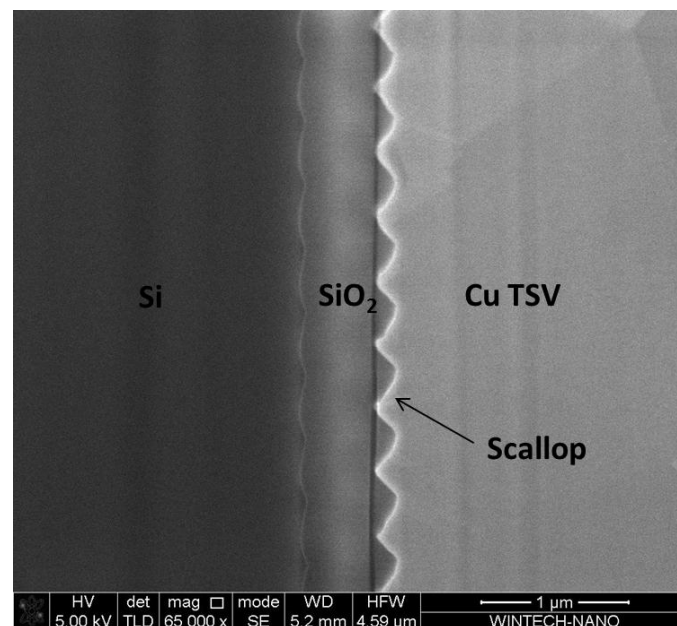
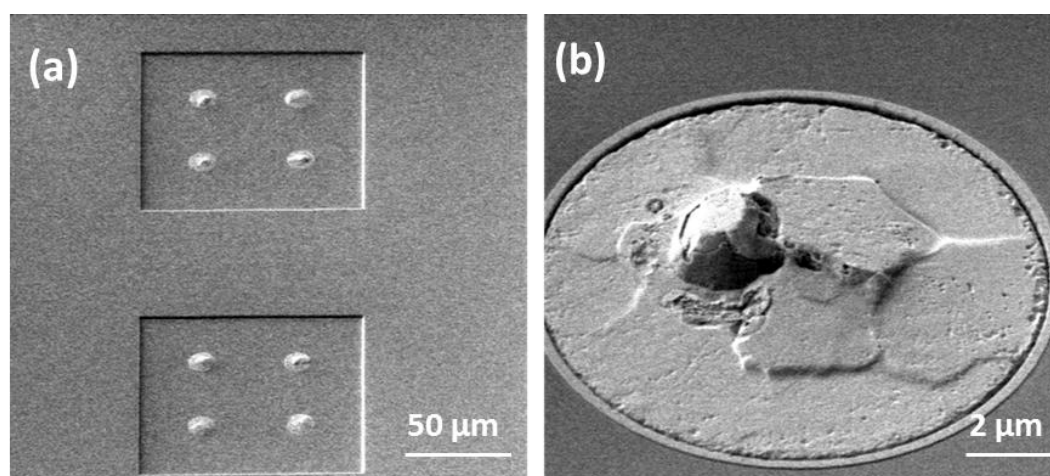


Figure 6.19: Scallop effect due to BOSCH process.

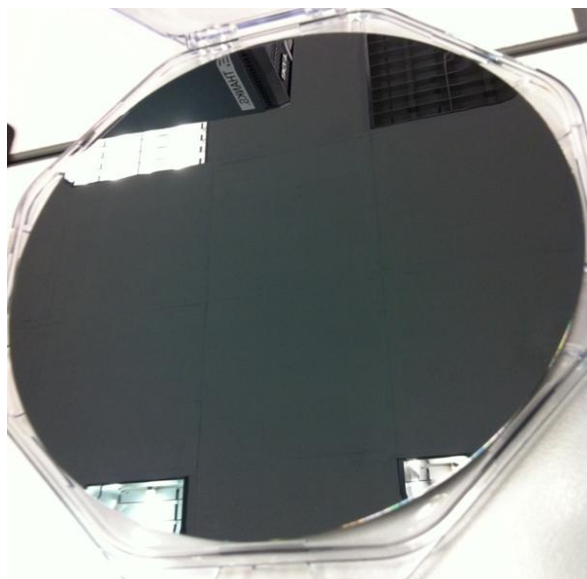
After that, TSV liner deposition with a layer of 3000 Å SiO<sub>2</sub> is done along the side-walls of the deep Si via and it is used as an electrical isolation for the TSV structure (Figure 6.18 (c)). It can be done either by using high temperature thermal oxide deposition or by plasma enhanced chemical vapor deposition (PECVD) with the use of silane or tetrathylorthosilicate (TEOS) as the pre-cursor in the PECVD process. Thermal oxide is used in the TSV via first approach because high temperature process will not have any effect on the active devices since the TSV is fabricated before the FEOL process. Moreover, good step coverage of the liner is critical for the TSV insulation from the Si substrate in order to minimise the current leakage during operation [6.11]. In our experiment, it is observed that the step coverage of the liner is continuous. Next, Figure 6.18 (d) shows that a 500 Å Ta barrier layer and a 3000 Å Cu seed layer are deposited using PVD, immediately followed by Cu ECP to grow a 6 µm of Cu to fill up the 30 µm depth of the trench. The Cu TSV wafer was then annealed at 300 °C to stabilize the grain growth. Cu CMP was performed to remove the overburden and the barrier layer (Figure 6.18 (e)). After TSV process, the wafer was deposited with ILD layer. (Figure 6.18 (f)). Subsequently, M1 trench was formed after defining the patterns with a contact etch. TSV is then revealed and is connected with M1/M2 Cu damascene layers as shown in Figure 6.18 (g). Similar Cu-Cu bonding enhancement approaches including SAM passivation and hermetic seal were introduced to make the conductive path between stacked wafers (Figure 6.18 (h)).

Cu TSV and Cu based bonding scheme seems to be a homogenous match as Cu is the only material involved in the integration process. What might be more important in this approach would be the thermo-mechanical stress induced in the system which needs to be more carefully examined to tackle the reliability concerns. It is understood that originally Cu filled TSV and Si are at equilibrium after post

deposition annealing stage [6.12]. However, the wafer cool-down creates a mismatch in thermal expansion coefficient (CTE) among the Si substrate, liner and Cu TSV. Therefore, a large compressive stress dominates Cu TSV which in turn tries to expand outwards. Cu protrusion from TSV top surface during thermal processing is a serious yield and reliability threat. Two undesirable effects due to this may be introduced: Firstly, the first effect is Cu extrusion around the center of the TSV which has an adverse impact for the following process integration. Secondly, there is the possibility of liner cracking which deteriorates the reliability of the electrical isolation. Therefore, another Cu CMP step is needed to further remove the protruded area after Cu annealing process. However, it is also important to ensure a low temperature process after that as the protrusion is still sensitive even after 2-step of Cu CMP. An example is as shown in Figure 6.20, TSV anneal is done at 300 °C, however we still observe Cu expansion due to subsequent SiN deposition at 400 °C. Therefore, low temperature process is detrimental to the reliability of 3-D integration when TSV is implemented by “via first” approach.



**Figure 6.20:** (a) TSV protrusion after ILD deposition and contact etch. (b) Enlarged view of Cu protrusion.



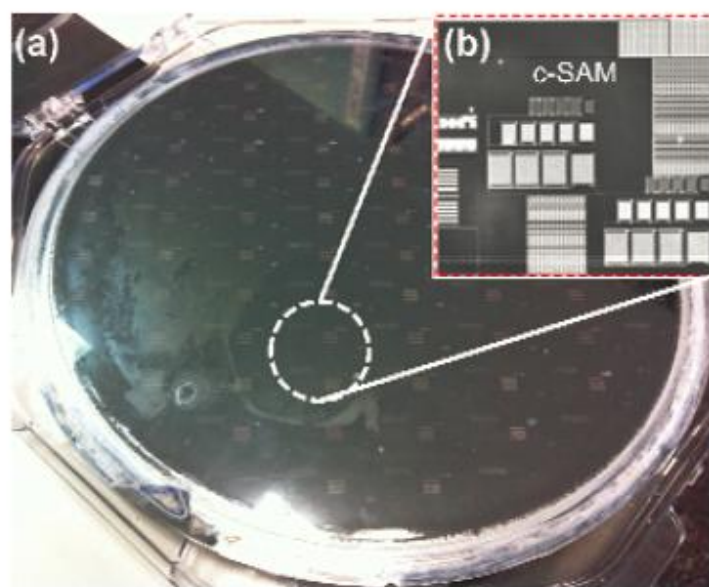
**Figure 6.21:** Defect-free surface after thinning down the TSV bonded wafer.

With the implementation of low temperature ILD deposition, Cu protrusion is largely suppressed. After careful preparation of the TSV wafer, both pairing wafers were SAM passivated for the subsequent alignment and transfer process. The bonding took place after SAM desorption at 250 °C followed by a number of cycles N<sub>2</sub> pump and purge in the bonding chamber. The bonding temperature was kept low at 300 °C for 1 hr and post annealed for another 1 hr. The bonded wafer was then thinned down to ~80 μm from the backside of the TSV wafer. Perfectly thinned wafer surface is observed in Figure 6.21. No surface defect is observed after polishing. This suggests that Cu-Cu bonds with integrated TSV can sustain from harsh mechanical process.

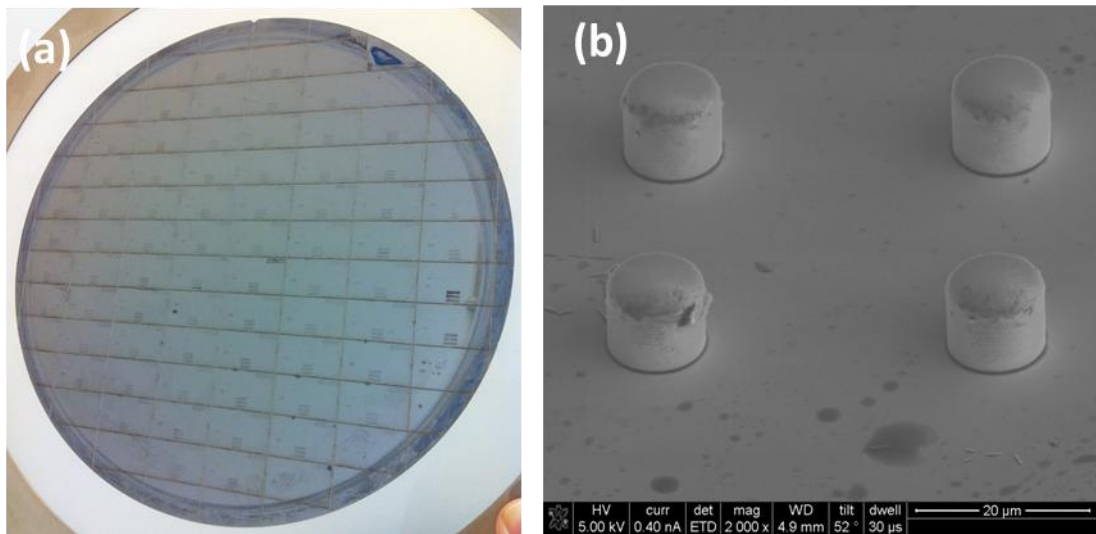
The bonded wafer was then immersed in potassium hydroxide (KOH) solution to carefully remove another ~50 μm Si substrate to reveal TSV. Figure 6.22 (a) shows that all TSV structures are revealed across the bonded wafer from the backside. It can be seen clearly that the high density Cu-Cu bonding patterns can be identified using c-SAM imaging tool, as shown in Figure 6.22 (b). It is also interesting to see that even

with ultrathin TSV layer, the bonded wafer can still survive the dicing process. The dicing yield is presented at 100%, as shown in Figure 6.23 (a). Uniform TSV exposure from wafer backside is observed in Figure 6.23 (b).

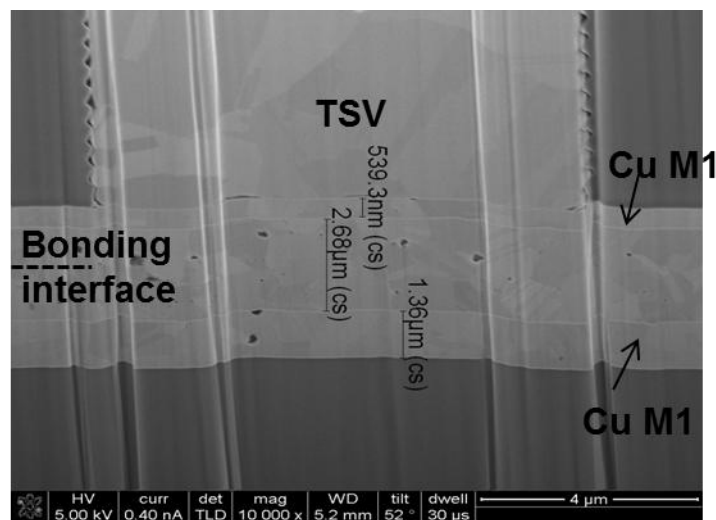
During the post bonding evaluation, there are two major interests to focus on: 1. TSV and M1-Cu layer contact after bonding and 2. Cu-Cu bonding interface behavior with introduction of TSV. Figure 6.24 shows the cross sectional image of the integrated structure. A full contact is made between TSV and M1-Cu layer. There is no Cu protrusion observed in further process after TSV formation. The bonding contact formed by both M2-Cu layers still maintains a seamless interface. Therefore, the integration scheme shows a promising result on the compatibility of both TSV and Cu-Cu bonding processes.



**Figure 6.22:** (a) Photo after top wafer thinning and TSV reveal; (b) C-SAM image of the bonding interface of a stacked chips.

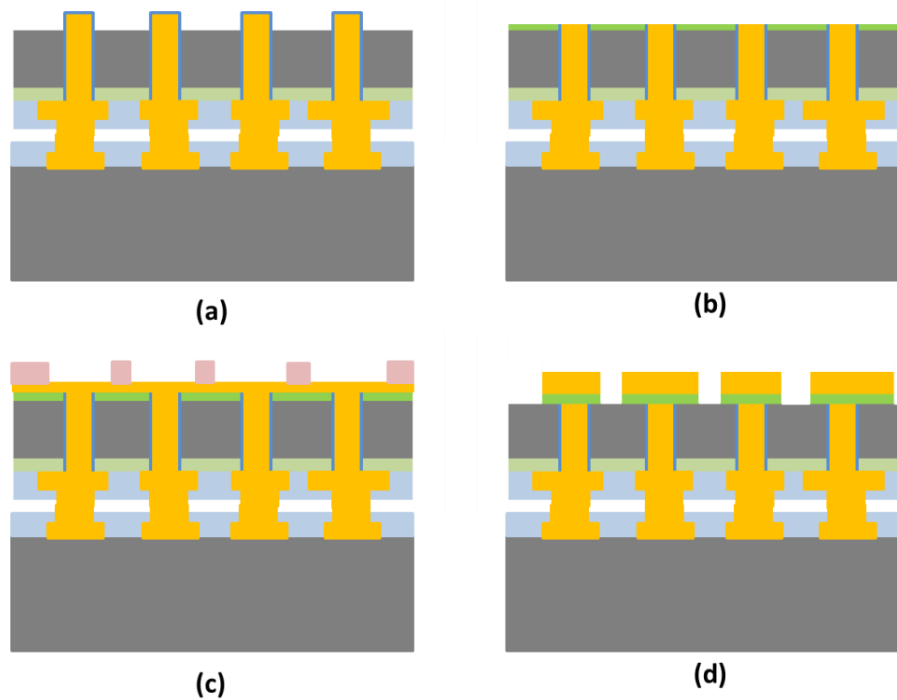


**Figure 6.23:** (a) 100% dicing yield with  $<30 \mu\text{m}$  TSV wafer bonded with bottom substrate. (b) SEM image on backside TSV exposure.



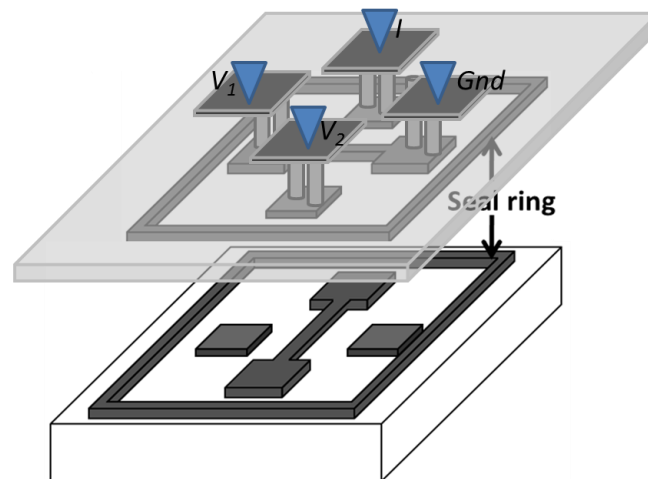
**Figure 6.24:** FIB-SEM image of TSV and Cu-Cu bonding integration.

Finally, a redistribution layer (RDL) process is implemented on the TSV exposed wafer side, as shown in Figure 6.25 (a). The wafer backside is then planarized (Figure 6.25 (b)) to carry out Cu seed deposition and backside metal patterning (Figure 6.25 (c)). Finally, the backside metal pads are formed through Cu plating, PR strip and Cu seed etch, as shown in Figure 6.25 (d).

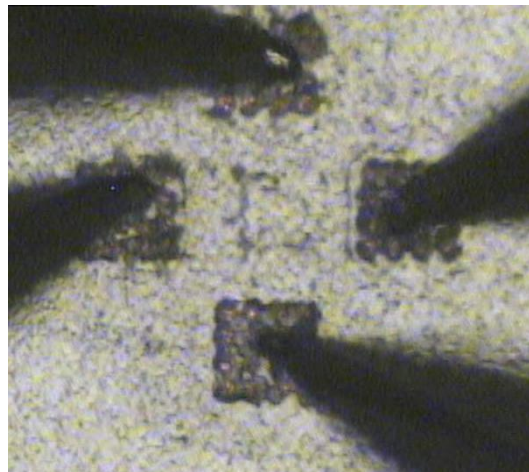


**Figure 6.25:** Backside metallization process: (a) Wet etch to expose TSV. (b) Oxide deposition/Oxide CMP/Cu CMP. (c) Cu seed deposition/Patterning. (d) Cu plating/PRS/Cu seed etch.

To characterize the electrical performance of the 3-D integration, a TSV integrated Kelvin structure is used as shown in Figure 6.26. Comparing to the conventional Kelvin structure, M1-Cu exposure is no longer required as TSV is integrated and outsourced through the thin substrate to the backside metal pads. Figure 6.26 (a) depicts the direct backside measurement of the Kelvin structure with the help of TSV. Figure 6.26 (b) shows the attempt to make probe tips directly contact with the exposed TSV to measure the contact resistance.



(a)

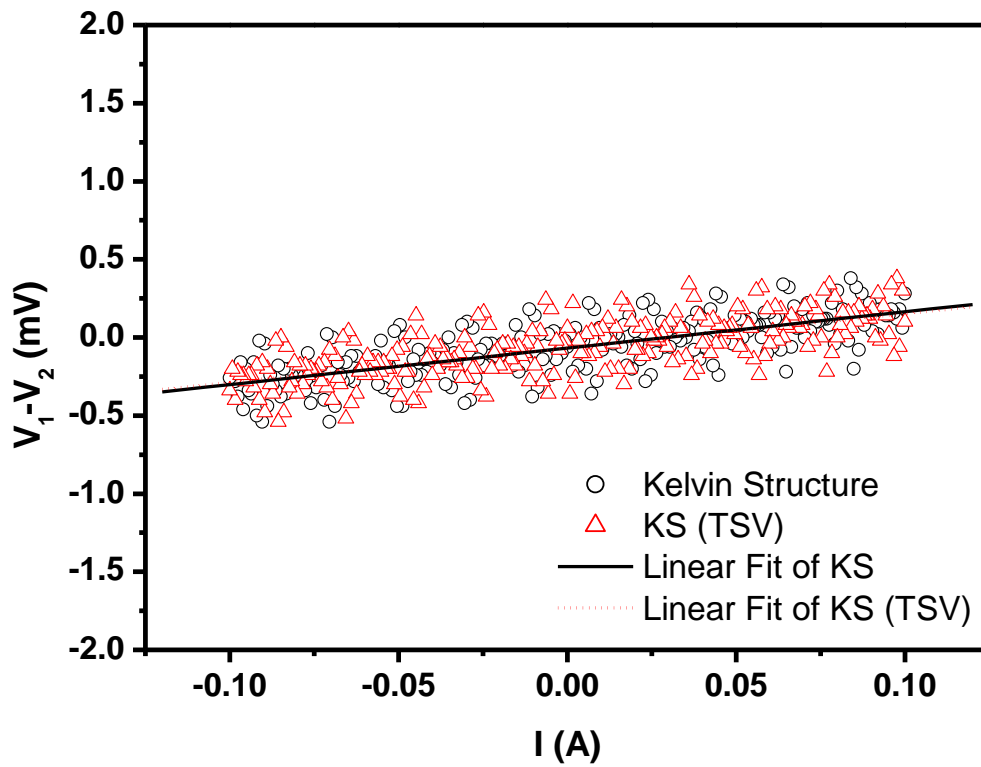


(b)

**Figure 6.26:** (a) Schematic of TSV integrated  $5\ \mu\text{m} \times 5\ \mu\text{m}$  Kelvin structure. (b) Microscopic image of 4-point probe measurement directly on backside exposed TSV.

After the electrical measurement was completed for the TSV integrated Kelvin structures, the sample was subjected to TMAH solution to expose conventional Kelvin structures on the same die. The results of both are shown in Figure 6.27. Comparing to the ordinary Kelvin structure with contact size of  $5\ \mu\text{m} \times 5\ \mu\text{m}$ , the contact resistance measured is extremely comparable with addition to TSV. The

integration scheme shows robust characteristics through excellent inter-layer and through-substrate electrical conduction.



**Figure 6.27:** Plot of  $V_1 - V_2$  vs  $I$  for the Kelvin structures with/ without TSV integration.

## **6.6 Summary**

Firstly, we have successfully demonstrated a 15- $\mu\text{m}$  fine pitch Cu-Cu interconnects using W2W thermo-compression bonding at 300 °C. Excellent electrical continuity (44000 nodes) and thermal reliability (1000 thermal cycles) of SAM passivated daisy chain are observed. Current stressing test is subjected to the daisy chain structures with reliable performance. Moreover, the evolution of ultrahigh density of 6- $\mu\text{m}$ -pitch Cu-Cu bonding is successful with comparable results from 15- $\mu\text{m}$  chain. Finally, we show that wafer level integration of TSV and low temperature Cu-Cu bonding is achievable using via-first approach. The process flow is introduced with challenges such as TSV protrusion and scallop effect. Excellent mechanical reliability of bonded wafer is observed with the optimized process. Successful TSV exposure is achieved across the wafer. The bonded structure shows a good contact between TSV and enhanced Cu-Cu bond. Finally, electrical characterizations of Kelvin structures with/without TSV integration suggest the prominent result of this integration scheme, which paves a way for the formation of high density IC-to-IC connections in the near future.

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# Chapter 7

## Summary and Conclusion

### 7.1 Thesis Summary

The main objective of this thesis is to develop a reliable fine pitch Cu-Cu bonding technology for future 3-D IC application. Wafer level face-to-face (F2F) thermo-compression bonding is successfully demonstrated at a low bonding temperature by incorporating enhancement techniques. High density Cu-Cu contacts with robust bonds are verified through the electrical performance, the mechanical strength and the thermal reliability. The bonding scheme shows excellent compatibility with TSV integration.

The major achievements are,

- 1) Successful mask design and wafer fabrication of fine pitch Cu-Cu bonding. Wafer planarity, surface roughness and surface cleanliness are addressed. Critical process steps are identified and optimized including ILD recess, surface topology and W2W alignment. Reliable mechanical support of Cu bonded wafer is achieved throughout harsh mechanical processes.
- 2) A maximum of 44,000 contacts with 15  $\mu\text{m}$  pitch is formed. EM test subjected to the daisy chain structures with reliable performance. Ultrafine pitch of 6- $\mu\text{m}$  is achieved with density of  $\geq 2 \times 10^6 \text{ cm}^{-2}$ , incorporating quality enhancement methods.

The research contributions are summarized as follows,

- 1) Investigation of the fundamental effects of microstructural evolution of Cu grains towards the bonding process. Improvement in Cu-Cu bond is achieved with smaller Cu grains, for providing stronger growth and inter-diffusion.
- 2) Cu surface cleanliness is preserved by SAM passivation. Successful implementation of SAM passivation into fine pitch Cu-Cu bonding, which is proven to reduce the contact resistance of Cu-Cu bonds due to higher degree of grain growth during bonding. Low temperature bonding is achieved  $\leq 300$  °C with reliable bonding contact.
- 3) Cu-Cu hermetic seal ring shows helium leak rate  $> 10X$  lower than the reject limit. Incorporation of hermetic seal ring is proven to promote the adhesion of Cu-Cu bond, through the characterizations of both Kelvin structures and fine pitch daisy chain. Electrical stability of the bonding contact is enhanced consequently. Hence, it provides an effective solution without additional application of under-fill.
- 4) 3-D integration scheme is developed utilizing TSV and Cu-Cu bonding. A successfully demonstration is achieved based on enhanced Cu-Cu bonding process and optimization of TSV formation. This study opens up new opportunity for wafer level integration of Cu-Cu bonding with state-of-the-art TSV technology, enabling future ultrahigh density 3-D IC applications.

## **7.2 Future Work**

This study has so far achieved a reliable low temperature bonding technique for wafer-to-wafer (W2W) fine pitch Cu-Cu bonding with face-to-face (F2F) stacking. It ensures reliable characteristics in mechanical, electrical and thermal properties. Building on the experimental work done, the following deserve further investigation:

(a) Wafer level Cu-Cu bonding and TSV integration is promising. However, the heat dissipation of this integration scheme needs to be understood for a part of important studies of forming ultrafine pitch interconnections.

(b) The enhancement bonding techniques implemented could be further applied to multi-level Cu-Cu bonding. Therefore, the exploration of this area should be carried out to identify new challenges for future heterogeneous 3-D integration.

(c) The demonstration of fine pitch Cu-Cu bonding in this work only makes use of BEOL process in which transistor fabrication is not involved. More comprehensive test structures could be included in the future study to evaluate the effect of SAM passivation process on transistor integration.

## List of Achievement and Publications

### Achievement:

1. Bronze prize winner at the 5th Taiwan Semiconductor Manufacturing Co (TSMC) Outstanding Student Research Awards in Hsinchu, Taiwan (2011).

### Journal Publications:

1. C. S. Tan, **L. Peng**, H. Y. Li, D. F. Lim, S. Gao, "Wafer-on-Wafer Stacking by Bump-less Cu-Cu Bonding and Its Electrical Characteristics", *IEEE Electron Device Letters*, vol. 32, pp. 943-945, 2011.
2. **L. Peng**, H. Y. Li, D. F. Lim, S. Gao, and C. S. Tan, "High Density 3D Interconnect of Cu-Cu Contacts with Enhanced Contact Resistance by Self-Assembled Monolayer (SAM) Passivation", *IEEE Transactions on Electron Devices*, vol. 58, pp. 2500-2506, 2011.
3. C. S. Tan, **L. Peng**, J. Fan, H. Y. Li, S. Gao, "3D Wafer Stacking Using Cu-Cu Bonding for Simultaneous Formation of Electrical, Mechanical and Hermetic Bonds", *IEEE Transactions on Device and Materials Reliability*, vol. 12, pp. 194-200, 2012.
4. J. Fan, D. F. Lim, **L. Peng**, K. H. Li, C. S. Tan, "Low Temperature Cu-to-Cu Bonding for Wafer-Level Hermetic Encapsulation of 3D Microsystems", *Electrochemical and Solid-State Letters*, vol. 14, pp. 470-4, 2011.
5. L. Zhang, **L. Peng**, H. Y. Li, G. Q. Lo, D. L. Kwong, C. S. Tan, "Operating TSV in Stable Accumulation Capacitance Region by Utilizing Al<sub>2</sub>O<sub>3</sub>-Induced Negative Fixed Charge", *IEEE Electron Device Letters*, vol. 33, pp. 875-877, 2012.
6. **L. Peng**, D. F. Lim, L. Zhang, H. Y. Li, and C. S. Tan, "Effect of pre-bonding anneal on the microstructure evolution and Cu-Cu diffusion bonding quality for three-dimensional integration application", *Journal of Electronic Materials*, vol. 41, pp. 2567-2572, 2012.
7. J. Fan, **L. Peng**, K. H. Li and C. S. Tan, "Wafer-Level Hermetic Packaging of 3D Microsystems with Low Temperature Cu-to-Cu Thermo-compression Bonding and Its Reliability", *Journal of Micromechanics and Microengineering*. (in press)
8. R. I. Made, **L. Peng**, H. Y. Li, C. L. Gan, and C. S. Tan, "Effect of Direct Current Stressing to Cu-Cu Bond Interface Imperfection for Three Dimensional Integrated Circuits", *Journal of Microelectronic Engineering*. (near acceptance)

## Conference Publications:

1. **L. Peng**, H. Y. Li, D. F. Lim, R. I. Made, G. Q. Lo, D. L. Kwong, and C. S. Tan, "Fine-Pitch Bump-less Cu-Cu Bonding for Wafer-on-Wafer Stacking and Its Quality Enhancement", *IEEE International 3D System Integration Conference (3DIC)*, Nov. 2010
2. **L. Peng**, H. Y. Li, D. F. Lim, G. Q. Lo, D. L. Kwong, and C. S. Tan, "Fabrication and Characterization of Bump-less Cu-Cu Bonding By Wafer-On-Wafer Stacking For 3D IC", *12th Electronics Packaging Technology Conference (EPTC 2010)*, Dec. 2010
3. R. I. Made, **L. Peng**, H. Y. Li, C. L. Gan, and C. S. Tan, "Study of the Possibility of Cu-Cu Bonding Interface Induced Interconnection Failure by Electromigration in Three Dimensional Integrated Circuits," *International Interconnect Technology Conference (IITC), Germany*, 2010
4. **L. Peng**, H. Y. Li, D. F. Lim, S. Gao, and C. S. Tan, "Thermal Reliability of Fine Pitch Cu-Cu Bonding with Self Assembled Monolayer (SAM) Passivation for Wafer-on-Wafer 3D-Stacking", *Electronic Components and Technology Conference (ECTC 2011)*, Jun. 2011.
5. **L. Peng**, H. Y. Li, D. F. Lim, G. Q. Lo, D. L. Kwong, and C. S. Tan, "High Density Bump-less Cu-Cu Bonding with Enhanced Quality Achieved by Pre-bonding Temporary Passivation for 3D Wafer Stacking", *International Symposium on VLSI Technology, Systems and Applications (2011 VLSI-TSA)*, Apr. 2011.
6. **L. Peng**, H. Y. Li, D. F. Lim, S. Gao, and C. S. Tan, "Analysis on Contact Resistance Behavior of Cu-Cu Bonding with Quality Enhancement Method", *International Conference on Materials for Advanced Technologies (ICMAT 2011)*, June. 2011.
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8. **L. Peng**, J. Fan, L. Zhang, H. Y. Li, D. F. Lim, and C. S. Tan, "Ultrafine pitch (6- $\mu$ m) evolution of Cu-Cu bonded interconnects in 3D wafer-on-wafer stacking", *IEEE International Interconnect Technology Conference (IITC)*, June. 2012.