A Fully Integrated Class-J GaN MMIC Power Amplifier for 5-GHz WLAN 802.11ax Application

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***Abstract*—This letter presents a fully integrated Class-J GaN MMIC power amplifier (PA), which is fabricated in Woolfspeed 0.25 um GaN-on-SiC technology. This PA is the first published design for the emerging IEEE 802.11ax application in literature. When tested with 80MHz 256-QAM 802.11ax signal with 11.25 dB peak-to-average power ratio (PAPR), the PA delivers average output power of 27.3 to 30.3 dBm from 4.9 to 5.9 GHz, with power-added efficiency (PAE) of 16.7% to 27.3%, while meeting the standard specification of error vector magnitude (EVM) below -32 dB.**

***Index Terms*—Monolithic microwave circuit (MMIC), 802.11ax, Class-J, GaN power amplifier.**

I. Introduction

RECENTLY, the accelerating growth of smartphones and mobile devices is propelling wireless communication to evolve towards higher data rate. As the successor of 802.11ac standard, 802.11ax introduces OFDMA and utilizes smaller sub-carrier spacing to improve overall spectrum efficiency, especially in high dense Wi-Fi deployment scenario. Besides, higher order 1024-QAM modulation is employed in 802.11ax to increase throughput. The data rate of 802.11ax is expected to be boosted up to 10 Gb/s, to meet the tremendous demand for high data rate application, such as interactive and high-definition video. However, wide bandwidth and complex modulation scheme of 802.11ax result in large PAPR, posing more stringent requirements of linearity and efficiency on power amplifier design than the earlier 802.11 standards. Consequently, design of a highly linear integrated PA with high efficiency remains a great challenge, especially in CMOS process. Since GaN HEMT device exhibits high breakdown voltage and high power density, GaN PA is a good candidate for 802.11ax application.

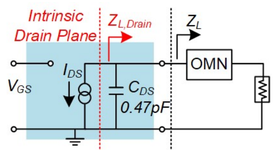

Fig.1. Simplified equivalent-circuit mode of the transistor in final stage

In recent years, Class-J mode of operation has drawn much attention to achieve high linearity, high efficiency and wide bandwidth simultaneously [1]-[5]. Class-J mode theoretically has the same efficiency and linearity as conventional Class-AB mode, but do not require open-circuit or short-circuit harmonic termination, which significantly simplifies the design of matching network such that high efficiency and wide bandwidth can be easily achieved. Therefore, Class-J mode is an appropriate choice for PA design to target high efficiency and high linearity over 5-GHz WLAN band.

In this letter, a novel fully integrated Class-J GaN PA for 802.11ax application is demonstrated. During the design, the fundamental and second harmonic termination is theoretically analyzed, providing objective for output matching network design. The proposed PA can deliver saturated output power over 37 dBm with PAE of 48.3%-54.6% across the whole 5-GHz WLAN band. Besides, the PA features excellent linearity that meets the requirements of 802.11ax standards, thus can be potentially used in 802.11ax access point with large coverage range.

II. Class-J PA Design

The Class-J mode requires complex fundamental load impedance and pure reactance second-harmonic load impedance [1]-[3], which are defined by

$$Z_{f_0} = \frac{2(V_{DD} - V_k)(1+j)}{I_{\max}} = R_{opt} + j \cdot R_{opt} \qquad (1)$$

$$Z_{2f_0} = \frac{-j \cdot 2(V_{DD} - V_k)}{\frac{2}{3\pi} I_{\max}} = -j\frac{3\pi}{8} R_{opt} \qquad (2)$$

in which, $R_{opt} = 2(V_{DD} - V_k)/I_{\max}$ is the optimum load of Class-B operation. In the design, the transistor's size in the final output stage is set at 1.6 mm, and this GaN transistor can

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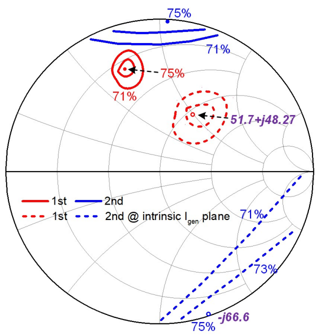


Fig.2. Drain efficiency contours for fundamental and second harmonic at 5.5 GHz

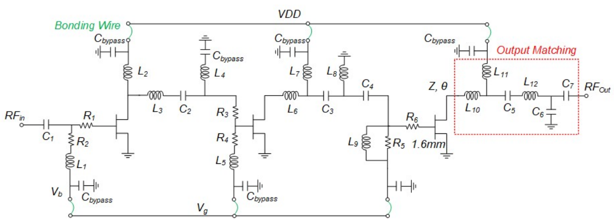


Fig.3. Schematic of the proposed PA

Table I
VALUES S OF THE COMPONENTS USED IN THE CLASS-J PA

Resistor (Ω)	Inductor (nH)	Capacitor (pF)
$R_1 = 5$	$L_1 = 0.61$, $L_2 = 9.04$	$C_1 = 2.11$, $C_2 = 0.84$
$R_2 = 10$	$L_3 = 2.66$, $L_4 = 1.30$	$C_3 = 1.29$, $C_4 = 1.40$
$R_3 = 9$	$L_5 = 1.71$, $L_6 = 3.07$	$C_5 = 2.04$, $C_6 = 0.54$
$R_4 = 100$	$L_7 = 1.29$, $L_8 = 0.58$	$C_7 = 2.38$
$R_5 = 6$	$L_9 = 1.40$, $L_{10} =0.56$	
$R_6 = 1.2$	$L_{11} = 0.5$, $L_{12} = 1.1$	

deliver maximum output power of 39.6 dBm at 5.5 GHz under a drain voltage of 28 V. The simplified equivalent circuit model of this transistor is depicted in Fig.1, showing the parasitic drain-source capacitance [6]. The knee voltage of this transistor is around 3 V and maximum drain current is 1.1 A, leading to the intrinsic optimum load R_{opt} of 45.4 Ω corresponding to a dc supply voltage of 28 V. According to the optimum fundamental and second harmonic load impedance in Class-J mode defined in Equations (1) and (2), the intrinsic load impedance Z_{f_0} = 45.4 + j45.4 and Z_{2f_0} = -j53.4.

To verify these theoretically determined intrinsic load impedances, load-pull simulation of the stabilized transistor is carried out up to second harmonic. Ideal Class-J mode assumes that there are no third harmonic and higher harmonic component, and hence the third harmonic impedance is assumed short in the load-pull simulation. The parasitic drain-source capacitance of 0.47 pF is de-embedded to obtain the intrinsic impedance at the intrinsic current generator plane. The simulated drain efficiency contours at 5.5 GHz are shown in Fig.2. From Fig.2, the intrinsic load impedance at the fundamental and second harmonic are 51.7 + j48.27 and –j66.6, respectively, which are in good agreement with the theoretical values. Therefore, in our design, it is reliable to use the theoretical values as the matching target when designing output matching network to achieve Class-J operation mode.

The schematic of the PA is shown in Fig.3, and the values of components utilized in the PA are listed in Table I. In order to

Table II
INTRINSIC FUNDAMENTAL AND SECOND-HARMONIC IMPEDANCE OF THE PROPOSED OUTPUT MATCHING NETWORK

	Theory	5.1GHz	5.5GHz	5.9GHz
Fundamental	45.4+j45.4	40.3+j45.9	45.2+j46.3	50.8+j50.4
2nd harmonic	-j53.4	5.1-j62.8	2.4-j49.5	1.2-j39.5

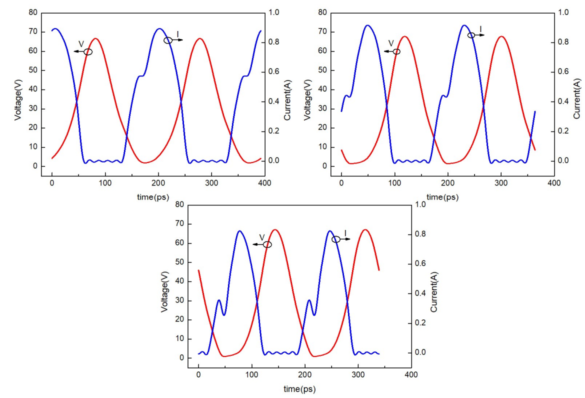


Fig.4. Simulated intrinsic drain voltage and current waveforms at different frequency

deliver at least 30 dB power gain, three-stage structure are employed in the PA. To ensure unconditional stability, stabilization circuits consisting of two resistors and one inductor are added to every stage, and the PA is unconditionally stable from DC to 20 GHz.

The practical intrinsic load impedances of the proposed output matching network are listed in Table II. As can be seen, the intrinsic load impedances match well with the theoretical impedances at the center frequency of 5.5 GHz. Although complete impedance matching cannot be realized by the proposed matching network in such a broadband, Class-J operation can still be approximately achieved with slight performance degradation. In order to further verify the Class-J operation of the proposed PA, the simulated drain voltage and current waveform at three frequencies of 5.1, 5.5 and 5.9 GHz at the device intrinsic drain plane are plotted in Fig.4. Compared with the waveform reported in [2], the simulated waveforms have the similar shapes, and a phase overlap exists between the drain and current waveform, which is a significant characteristic of the Class-J mode.

III. Implementation and Measurement

The PA was fabricated in Woolfspeed 0.25 um GaN on SiC technology and wire bonded to PCB implemented using RO4350 substrate with 20 mil thickness. Fig.5 depicts the photograph of fabricated die with dimension of 1.28×3.7 mm^2 and PCB. From the perspective of commercial application, all the gate bias in the three stage are connected together and fed by only one voltage. A gate voltage of -2.96 V and a drain voltage of 28 V were chosen for deep Class-AB bias condition, giving a quiescent current of 23.7 mA ($I_{dq} \approx 2\%$ of I_{max}). No external components including RF choke and DC blocking capacitor are required in this PA, thus facilitating full integration.

PA was tested with continuous wave (CW) signal over the

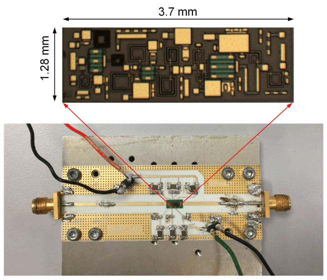
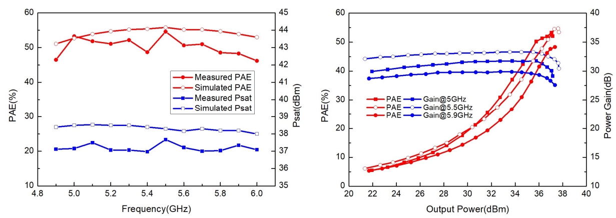
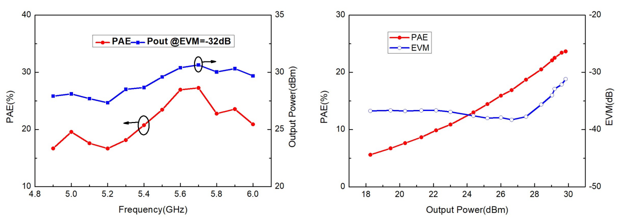


Fig.5. Photo of the fully integrated GaN die and testing board



(a) (b)

Fig.6. Measured performance of CW testing (a) PAE and Psat versus frequency (b) PAE and gain versus output power at different frequency



(a) (b)

Fig.7. Measured performance with 802.11ax signal (a) PAE and average output power (b) EVM and PAE in different power level at 5.5 GHz

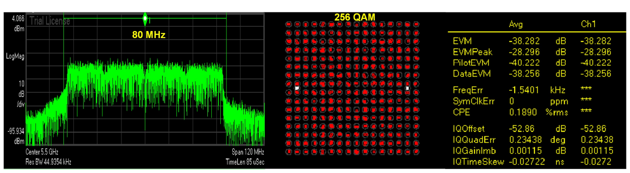


Fig. 8. Measured constellation, EVM and spectrum with 802.11ax signal

frequency range of 4.9-6 GHz, and the measured saturated output power and PAE are reported in Fig.6 (a). The measured maximum output power and efficiency are between 37-37.68 dBm and 48.3-54.6% from 4.9 GHz to 6 GHz, respectively. The measured power gain and efficiency versus output power at 5, 5.5 and 5.9 GHz are depicted in Fig.6 (b), showing the power gain is above 28.5 dB.

To evaluate the PA's practical performance for 802.11ax application, the PA was tested using 80MHz 802.11ax signal with 256-QAM modulation and 5/6 code rate without digital pre-distortion (DPD). The PAPR of this signal is as high as 11.25 dB. When satisfying the standard specification of EVM<-32 dB for 256-QAM modulation, PA delivers average output power of 27.3-30.6 dBm and achieves efficiency of 16.7-27.3%, as shown in Fig. 7 (a). The measured EVM in different output power level and the corresponding efficiency at 5.5 GHz are depicted in Fig.7 (b). The EVM floor of the test signal can only reach to -41 dB due to the imperfection of signal source, resulting in a little degradation in measured EVM performance. Consequently, the PA can only achieve -38.3 dB

TABLE III

PERFORMANCE COMPARISON BETWEEN THE PROPOSED PA AND OTHER INTEGRATED GAN PAS

Ref.	This work	[4]	[7]	[8]	[9]
Freq(GHz)	4.9-5.9	2.2-3.2	5-6	5.2-6.8	5.2-6.2
Psat(dBm)	37-37.68	24-27	47.7	46	42.1-43
PAE(%)	48.3-54.6	48-58	40-43	51.5-56.5	37-41
Gain(dB)	28.5-31.7	7-10	25	25.4-27.7	20
Size(mm^2)	1.28×3.7	2×2	3.2×5.3	3.2×5.3	4.5×3.5

EVM. In addition, the measured constellation, spectrum and EVM of -38.28 dB at 5.5 GHz are demonstrated in Fig. 7. Although EVM of signal with 1024-QAM modulation was not measured due to lack of analysis capacity, the PA is expected to satisfy -35 dB EVM specification for emerging 802.11ax standard with 1024-QAM. Finally, the PA's performance is summarized and compared with other published integrated GaN PAs [7]-[9], reported in Table III.

IV. CONCLUSION

This work introduces a fully integrated Class-J GaN power amplifier designed for 5GHz WLAN 802.11ax systems. To author's knowledge, this PA is the first published design for 802.11ax systems in literature. The measurement results demonstrate the promising performance, showing the PA is of great commercial value. If DPD is employed, PA's performance could be further enhanced. Besides of 802.11ax, the PA can also be used in current 802.11ac systems.

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