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Flicker Noise Fluctuations in Deep Submicron MOSFETs

Chew Kok Wai Johnny

School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University in fulfilment of the requirement for the degree of Doctor of Philosophy

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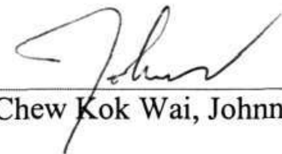

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ABSTRACT

This thesis investigates the effects of technology scaling on the flicker (or 1/*f*) noise performance of deep submicron complementary metal-oxide-semiconductor (CMOS) transistors. Two major effects have been investigated, namely the employment of different gate dielectric growth and subsequent nitridation conditions, and the effects of geometry scaling. The first part of this work focus on the study of these two effects within the 0.25μm technology node. Subsequently the scope of this study has been widened to examine the effects of scaling across a spectrum of technology nodes, namely 0.35μm, 0.25μm, 0.18μm and 0.13μm. Finally the scope is further extended to cover the offering of different process flavours, as well as geometry scaling for the 0.13μm technology node.

The 1/*f* noise performance of 0.25μm thin gate oxide transistors from the dual gate oxide thickness process and the single gate oxide thickness process have been evaluated and compared. A total of 20 transistors have been characterized. The results reveal that thin gate oxide transistors from the dual gate oxide thickness process show a maximum of an order reduction in the current noise spectra, as compared to their counterparts from the single gate oxide thickness process. This reduction can be attributed to the lower nitrogen concentration peak at the Si/SiO_2 interface. This lower nitrogen peak in turn correlates to a reduced oxide trap density at the interface, which has been verified via the charge-pumping technique. Hence the dual gate oxide thickness process will be the state-of-the-art for the implementation of low noise circuit designs. In general, the low frequency noise behaviour of the fabricated deep submicron metal-oxide-semiconductor field-effect transistors (MOSFETs) is best described by the correlated mobility fluctuation model.

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A thorough investigation of technology scaling on the 1/*f* noise characteristics of p-channel transistors from four advanced CMOS technologies with dual gate oxide thickness has been reported. The results show that the drain current noise spectral density S_{Id} of thin gate oxide transistors increases by approximately 2 orders of magnitude when scaling from 0.35μm to 0.13μm. This increase can be attributed to the changeover from thermal oxides to nitrided oxides from 0.25μm and below. The magnitude of increase is influenced by the degree of nitridation. In comparison with the thin gate oxide non-nitrided transistors from the 0.35μm node, nitridation has increased the S_{Id} of architecturally equivalent thick gate oxide transistors from the 0.25μm to 0.13μm nodes by a maximum of an order of magnitude. The experimentally observed 1/*f* noise trends correlate well with the Berkeley Short-Channel IGFET Model 3 version 3 (BSIM3v3) 1/*f* noise model.

We also investigate the composite effect of channel length and gate oxide thickness scaling, coupled with the effect of gate dielectric nitridation on the 1/*f* noise of minimum channel length n-channel MOS (NMOS) transistors. These transistors have been taken from four advanced CMOS technologies with dual gate oxide thickness. The results show that S_{Id} of thin gate oxide transistors increase by approximately 1.5 orders of magnitude when scaling from 0.35μm to 0.13μm. This increase is closely correlated to the changeover from thermal oxides to nitrided oxides from 0.25μm and below. This work also investigates the effect of nitridation on thick gate oxide transistors and compares them to their architecturally equivalent thin gate oxide non-nitrided counterpart from the 0.35μm technology. The comparison reveals that nitridation has increased the S_{Id} of architecturally equivalent thick gate oxide transistors from the 0.25μm to 0.13μm

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technologies by a maximum of 1.25 orders of magnitude. The experimental $1/f$ noise trends have been verified with simulations using the BSIM3v3 $1/f$ noise model.

Finally, we present the composite effects of technology and geometry scaling on the $1/f$ noise performance of deep submicron transistors taken from four advanced CMOS technologies with dual gate oxide thickness. For the 0.13μm technology node, three different process flavours, namely the generic process flow (G), the low voltage/high performance process flow (LV/HP) and the low standby power process flow (LSP) have been investigated. The higher degree of gate dielectric nitridation with technology downscaling from 0.35μm node to 0.13μm G node has resulted in a severe degradation of the $1/f$ noise performance by approximately 3 orders of magnitude. This work further demonstrates that the employment of LSP transistors in 0.13μm node will lower the $1/f$ noise spectra by approximately 2 orders of magnitude as compared to the 0.13μm LV/HP transistors, which gives the worst $1/f$ noise performance among the three different process flavours. The study of device geometry scaling on 0.13μm LSP transistors shows that in general the scaling trend follows the $S_{Id} \propto \frac{W}{L^3}$ rule, where W and L is the active gate width and length of the transistor respectively. For devices with gate area < 1 μm^2, a large dispersion in the $1/f$ noise level has been seen. This phenomenon has been correlated to the existence of Lorentzian-like spectra for small geometry transistors. The investigation of the effect of scaling the transistor's aspect ratio (W/L) reveals a $(S_{Id} \times WL) \propto \left(\frac{W}{L}\right)^2$ dependence.

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List of Symbols

α_H	Modified Hooge's constant
α_{H^*}	Original Hooge's constant
α_{sc}	Scattering parameter (Vs)
α_{latt}	Scattering due to lattice crystal only (Vs)
α_t	Tunneling parameter (m^{-1})
δN	Fluctuation in the charge density in the homogeneous channel (m^{-2})
ε_{si}	Permittivity of silicon (F/m)
ε_{ox}	Permittivity of silicon dioxide (F/m)
ϕ	Potential at gate oxide-silicon boundary (eV)
ϕ_B	Bulk potential (eV)
ϕ_F	Fermi potential (eV)
γ	Frequency exponent of $1/f$ noise
μ_0	Low field mobility (m^2/V-s)
μ, μ_n	Electron mobility (m^2/V-s)
μ_{eff}	Effective mobility (m^2/V-s)
μ_{ox}	Mobility due to oxide charge scattering (m^2/V-s)
μ_{latt}	Mobility due to lattice scattering (m^2/V-s)
μ_{ph}	Mobility due to phonon scattering (m^2/V-s)
μ_{peff}	Effective hole mobility (m^2/V-s)
τ_N	Lifetime or decay time constant of the free carrier (s)
ΔL_{clm}	Electrical channel length reduction due to channel length modulation (m)
ΔE	Energy element (J)
$\overline{\Delta N_t^2}$	Variance of the carrier number fluctuations
ΔV	Elemental volume (m^{-3})
AF, A_F	HSPICE level-3 noise model frequency exponent
A_{bulk}	Bulk charge coefficient
c	Electron capture coefficient
C_d, C_{dep}	Depletion layer capacitance (F/m^2)

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C_{inv}	Inversion layer capacitance (F/m^2)
C_{it}	Interface trap capacitance (F/m^2)
C_{ox}, C_{OX}	Gate oxide capacitance per unit area (F/m^2)
E_C	Conduction band energy at Si/SiO_2 interface (eV)
E_i	Intrinsic Fermi energy level (eV)
E_V	Valence band energy at Si/SiO_2 interface (eV)
EF	BSIM3v3 $1/f$ noise model frequency exponent
E_{Fn}, E_{fn}	Fermi energy level (eV)
E_{sat}	Critical electric field at which carrier reach saturation velocity (V/m)
E_t	Trap energy level (eV)
f	Frequency (Hz)
f_t	Fraction of filled traps under steady state conditions
F_n	Electrons quasi-Fermi level (eV)
F_t	Trap quasi-Fermi level (eV)
g_m	Transconductance (A/V or S)
g_{ds}	Output conductance (A/V or S)
I	Current (A)
I_d, I_{ds}	Drain current (A)
$I_{DS(ON)}$	Drain current in strong inversion (A)
k	Boltzmann's constant (eV/K)
KF, K_F	HSPICE level-3 noise parameter (V^2/F)
l_c	Characteristics length (m)
L	Device channel length (m)
L_{min}, $L_{g(min)}$	Device minimum drawn channel length (m)
L_{eff}	Device effective channel length (m)
N	Concentration of charge carriers in the channel (m^{-2})
N^*	Abbreviation introduced in equation (2.26a) (m^{-2})
N_0	Concentration of charge carriers at the source end of the channel (m^{-2})
NOIA or A	BSIM3v3 $1/f$ noise model fitting parameters (m^{-3} eV^{-1})
NOIB or B	BSIM3v3 $1/f$ noise model fitting parameters (m^{-1} eV^{-1})
NOIC or C	BSIM3v3 $1/f$ noise model fitting parameters (m eV^{-1})
N_L	Concentration of charge carriers at the drain end of the channel

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	(m^{-2})
N_f	Number of fingers of a multi-fingered transistor
n_i	Intrinsic carrier density (m^{-3})
n_s	Electron density at the interface (m^{-3})
$N_t(E_{Fn})$, $N_t(E_{fn})$	Extracted volume oxide trap density (N_t), in an energy interval of kT around the surface Fermi level (E_{fn}) (m^{-3} eV^{-1})
N_t	Oxide trap density (m^{-3} eV^{-1})
$\overline{N}$	Average number of free carriers, with the bar denoting time average
q	Electronic charge (C)
Q_N, Q_s, Q_{inv}	Inversion layer charge density (C/m^2)
R	Resistance (Ω)
Rd	Loading resistor (Ω)
R_F	Filter resistor (Ω)
$R_{S,D}$	Drain (source) resistance (Ω)
R_{sq}	Sheet resistance of drain-source diffusion (Ω/sq)
S_I	Noise current spectral density (A^2/Hz)
S_{Id}	Drain current noise spectral density (A^2/Hz)
S_N	Spectral density of the carrier number or free carriers in the channel (1/Hz)
$S_{\overline{\Delta N_t}}$	Spectral density of the trapped carriers in an elemental volume of the oxide (1/Hz)
S_R	Fluctuations due to resistance (Ω^2/Hz)
S_{Vg}	Input-referred gate voltage spectral density (V^2/Hz)
T	Temperature (K)
T_{OX}, t_{ox}	Gate oxide thickness (m)
V	Applied voltage (V)
V_a	Output voltage of the voltage supply (V)
V_{DD}	Drain supply voltage (V)
V_{DSAT}, V_{dsat}	Drain-source voltage at which velocity saturation occurred (V)
V_d, V_{ds}	Drain-source voltage (V)
V_g, V_{gs}	Gate-source voltage (V)
V_{SB}	Source-body voltage; Substrate bias voltage (V)
V_{th}, V_T	Threshold voltage (V)

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X_{dep}	Depletion layer thickness under the gate (m)
ϖ	Angular frequency (radians)
W	Device channel width (m)
W_{eff}	Effective channel width (m)
W_f	Length of the unit finger of a multi-fingered transistor (m)

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CHAPTER 1 INTRODUCTION

1.1 Motivation

Accelerated scaling of CMOS technology has led to the increasing ease of incorporating mixed-signal/radio-frequency (MS/RF) designs on-chip. This is due to the performance improvement and cost advantage derived from scaled CMOS technologies. However as the feature size of MOS devices is scaled down aggressively to achieve higher speed, greater packing density and to incorporate more functionalities per chip area, it has been reported that the flicker noise or $1/f$ noise spectra will increase with $1/L_{g(min)}^3$ [1], [2] where $L_{g(min)}$ is the minimum drawn gate length. This is one of the major reasons accounting for the study of $1/f$ noise for analog/RF mixed-mode applications gaining prominent attention in the recent years [3]-[9].

In the continual push to implement ultra-high frequency (UHF) transceivers using state-of-the-art scaled CMOS technologies [10], [11], $1/f$ noise appearing at the output of a downconversion mixer would degrade the signal-to-noise ratio (SNR). This is due to a two-pronged constraint of a reduction of the voltage headroom resulting from a lower supply voltage and a higher noise floor. This in turn reduces the usable dynamic range and consequently increase the overall noise figure (NF). More recently, with the emergence of zero-IF or direct-conversion transceiver architecture [12] as the best candidate to achieve fully integrated designs with few external components, $1/f$ noise has become even more important since the sensitivity of direct-conversion receivers are strongly affected by $1/f$ noise [12], [13]. In direct-conversion receiver, the signal goes through minimal amplification at RF and is thereafter directly downconverted to baseband. Hence the high

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$1/f$ noise situated before the corner frequency would interfere with the downconverted baseband signal. This is aggravated by the fact that with the scaling down of technology, the corner frequencies of $1/f$ noise tend to tread higher [14].

$1/f$ noise is the dominant phase noise source in silicon-based oscillator circuits. This noise gets up-converted into close-in phase noise of the oscillator circuits at high frequencies. A general theory of phase noise in linear oscillatory system proposed by Lee and Hajimiri [15] suggest that the phase noise spectrum consists of three regions, namely a $1/f^3$ region, a $1/f^2$ region and a flat region. It further illustrates that the $1/f^3$ sidebands around the carrier frequency is due to the device $1/f$ noise upconversion, whereas the $1/f^2$ portion is due to the white noise downconversion. Hence it is essential for designers to have a clear understanding of the device $1/f$ noise in order to be able to suppress the upconversion of $1/f$ noise into close-in phase noise. Furthermore in order to accurately predict the impact of $1/f$ noise on the circuit performance, thorough understanding of the effects of technology scaling on the $1/f$ noise behaviour of MOS transistors and accurate $1/f$ noise models are required.

For today's state-of-the-art technologies, gate dielectric nitridation using nitrogen sources such as N_2O or NO [16], [17] has become an integral part of advanced gate dielectrics to mitigate boron penetration problems, gate leakage issues, as well as to alter the equivalent oxide thickness (EOT). The presence of nitrogen in the oxide is known to control the transient enhanced diffusion of boron by modifying the population of interstitials in the Si/SiO_2 interface, given the fact that the diffusion of boron is mediated through interstitials [18]. Furthermore, nitrided oxides have a lower tunneling effective mass and barrier height as compared to SiO_2 oxides. This, in turn, produces a reduced decay constant [19]. For an equivalent capacitance, the reduction in decay constant is

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compensated for by using nitrided films with a physical thickness larger by a factor of $\varepsilon_{NO}/\varepsilon_{SiO2}$ compared with SiO_2. This, in turn, results in significant suppression of direct-tunneling gate current and thereby lowering power consumption [20]. Furthermore increasing the nitrogen concentration improves the reliability of pMOSFETs, resulting in a more hot-carrier injection (HCI) resistant interface [21]. With gate dielectric nitridation processes, higher doses of nitrogen will be incorporated at the Si/SiO_2 interface. It has been reported that there is a correlation between the nitrogen concentration at the Si/SiO_2 interface and the gate oxide interface state trap density [5]. The $1/f$ noise performance of oxynitride films is expected to degrade significantly as compared to the pure oxide films due to a higher interface state density [5], [22], [23]. In addition, with the introduction of advanced gate dielectric processing techniques and smaller geometries, the deep submicron devices $1/f$ noise behaviour, being technology dependent, is expected to deviate significantly from their long channel counterparts.

The motivations described above provided the basis to drive the author to perform a thorough investigation of the effects of process changes and technology scaling on the $1/f$ noise performance of deep submicron NMOS and PMOS transistors.

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1.2 Objectives

The objectives of this project are summarised as follows:

(i) To study and understand the effects of migrating from a single thickness gate oxide growth process to a dual thickness gate oxide growth process on the $1/f$ noise behaviours of deep submicron NMOS and PMOS transistors;

(ii) To study and understand the effects of technology downscaling, especially a higher degree of gate oxide nitridation, on the $1/f$ noise behaviours of deep submicron NMOS and PMOS transistors;

(iii) To compare and contrast the effects of gate oxide nitridation on the $1/f$ noise behaviours of input/output (I/O) thick gate oxide nitrided transistors from scaled technologies against the architecturally equivalent non-nitrided thin gate oxide transistors from the more mature technology;

(iv) To study and understand the effects of varying degree of gate oxide nitridation arising from different process flavours offered within a deep submicron technology, as well as scaling across technologies, on the $1/f$ noise behaviours of deep submicron thin gate oxide NMOS transistors;

(v) To investigate the effects of geometries, active gate areas and aspect ratios scaling on the $1/f$ noise behaviours of deep submicron thin gate oxide NMOS and PMOS transistors.

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1.3 Scope

The scope or coverage of this project is specified as follows:

(i) This work investigates the 1/*f* noise behaviours of transistors fabricated using deep submicron silicon-based conventional CMOS technologies;

(ii) The 1/*f* noise measurements have been conducted at room temperature (25°C);

(iii) During 1/*f* noise measurements and analysis, emphasis has been placed on the transistor types and the regions of operation employed in analog/RF applications.

1.4 Major Contributions of the Thesis

The major contributions of this thesis are presented as follows:

(i) The author has investigated and demonstrated for the first time, the improvement in thin gate oxide transistors' 1/*f* noise performance when migrating from a single thickness gate oxide technology to a dual thickness gate oxide technology. This finding has profound implications for analog/RF circuit designers. This can be explained by correlating the following two factors. First, as nitrided oxides become integral part of advanced gate dielectrics to enhance gate oxide

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reliability, minimize gate leakages and to mitigate boron penetration issues, it is inevitable that the 1/*f* noise in CMOS transistors increase significantly. This can be attributed to the introduction of oxide charges and traps during gate dielectric nitridation [5], [22], [23]. Second, with the dual thickness gate oxide technology, which offers additional high-voltage thick gate oxide transistors for designs requiring large voltage swings, such as the I/O stages, high gain amplifiers and so on, gaining dominance for deep submicron processes, this finding offers analog/RF circuit designers a cost-effective solution to moderate the rapid increase of low-frequency noise resulting from the miniaturization of CMOS devices.

(ii) The 1999 ITRS roadmap [24] calls for the reduction of the normalized input-referred voltage noise spectral density, S_{Vg} with technology generation scaling. The simulations presented in reference [25] showed that this requirement can be met if one considers the predominant scaling of the oxide thickness, T_{OX}, without accounting for the changeover to nitrided oxides from 0.25μm generation and below. In this work, the author has presented a more realistic and accurate 1/*f* noise scaling trend with technology downscaling, which takes into account not only the key device parameters, such as the supply voltage, gate dielectric thickness, threshold voltage and so on, but most importantly the direct impact of gate oxide nitridation.

(iii) With the dominance of the dual thickness gate oxide technology, the author has demonstrated conclusively that the high-voltage thick gate oxide transistors do

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not offer relief for the degradation of the $1/f$ noise performance. This is due to the fact that the thick gate oxide areas get nitrided as well during nitridation of the thin gate oxide regions.

(iv) To provide designers with the appropriate performance-leakage design coverage and flexibility, and for systems-on-chip (SOC) solutions, foundries have begun offering different process flavours within a single node from 0.13μm technology node and below. The author has performed a comprehensive comparison of the $1/f$ noise behaviours of deep submicron thin gate oxide NMOS transistors from different process flavours offered within the 0.13μm technology, as well as across different technologies. The finding that the use of 0.13μm low standby power transistors helps to moderate the increase of the $1/f$ noise down to a level comparable to that of a more mature technology serves as a highly valuable process selection guideline to analog/RF circuit designers. Thereafter, the author performed a detailed analysis of the impact of geometries, active gate areas and aspect ratios scaling on the $1/f$ noise behaviours of 0.13μm low standby power thin gate oxide NMOS and PMOS transistors. The results presented provide a practical design guideline for analog/RF circuit designers when they need to tradeoff between speed, power consumption and area coverage with low-frequency noise.

(v) This work has generated three full journal papers with another journal submission currently under review, and one international conference paper. In addition, the author's published work has been cited by numerous other authors,

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reflecting the significance of the work done (refer to the author's publication and citation list on page 134).

1.5 Organization of the Thesis

This thesis is organised into 8 chapters. Chapter 1 presents the motivation of this research work. It also defines the objectives and scope of the project and highlights the major contributions of the thesis.

Chapter 2 provides a comprehensive literature review of $1/f$ noise theories, the analytical formulations leading to the formation of $1/f$ noise compact models. It also provides a critical review of the impact of advanced processing techniques on the $1/f$ noise behaviours of CMOS transistors.

Chapter 3 discusses in depth the $1/f$ noise measurement system setup, the pros and cons between the different measurement techniques, and the theories behind the measurement technique employed for this work.

Chapter 4 discusses the impact of migrating from a single thickness gate oxide growth process to a dual thickness gate oxide growth process on the $1/f$ noise behaviours of 0.25μm technology NMOS and PMOS transistors. The main drive to effect this migration is the ability to provide thick gate oxide transistors for I/O applications, and thin gate oxide transistors for core applications within a single processing technology. This chapter will set the stage for the subsequent chapters, whereby the silicon wafers under investigation has been fabricated using primarily the dual thickness gate oxide growth process.

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Chapter 5 investigates the composite effect of channel length and gate oxide thickness scaling, coupled with an increasing nitridation dosage, resulting from a consequence of gate dielectric scaling, on the 1/*f* noise of deep submicron minimum gate length PMOS transistors. Another key highlight of this chapter is the investigation and comparison of the effect of nitridation on thick gate oxide I/O transistors taken from the advanced 0.13μm, 0.18μm and 0.25μm technologies, with their architecturally equivalent thin gate oxide counterpart from the more mature 0.35μm technology.

Chapter 6 continues to investigate the effects of technology scaling on the 1/*f* noise behaviour of deep submicron NMOS transistors fabricated using the dual gate oxide thickness process. It examines the composite effect of channel length and gate oxide thickness scaling, coupled with the effect of gate dielectric nitridation on the 1/*f* noise performance of minimum gate length NMOS transistors taken from the four advanced CMOS technologies previously mentioned. It further examines the effects of a higher degree of gate oxide nitridation, resulting from a consequence of technology downscaling, on the 1/*f* noise performance of deep submicron thin and thick gate oxide NMOS transistors. This is followed by the identification of the mechanisms responsible for the 1/*f* noise of deep submicron thin gate oxide NMOS transistors.

Chapter 7 focuses on the 1/*f* noise of 0.13μm low standby power (LSP) transistors for mixed-mode and RF applications. A key highlight of this chapter is the comparison of the 1/*f* noise performance of the LSP transistors against the 0.13μm low voltage/high performance (LV/HP) and generic (G) options, as well as against the more mature nodes, namely 0.18μm, 0.25μm and 0.35μm respectively. Another major topic discussed in this chapter is the detailed investigation of the effects of geometry scaling on the 1/*f* noise of 0.13μm LSP transistors. Two important highlights of this topic is the discussion of the

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effects of aspect ratio (*W/L*) scaling and the demonstration that the 1/*f* noise of modern small area CMOS devices is dominated by Lorentzian-like spectra.

Finally, Chapter 8 summarizes the results of this research work and recommends a few key areas for future research on this topic.

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CHAPTER 2
LITERATURE REVIEW OF TRANSISTOR 1/f NOISE

2.1 Review of 1/f Noise Models

The spatially inhomogeneous fluctuations of electron density in a semiconductor system result in macroscopic current density fluctuations creating noise. When these excitations are investigated statistically in the frequency domain, the mean-square value of current fluctuation per frequency bandwidth or the current noise power spectral density provides an indication of the strength of the noise source. There are four major sources of noise in a MOSFET [26].

The first dominant noise source is thermal noise, also known as Johnson noise. Thermal noise is generated in a MOSFET by the random motion of carriers in the channel of the device at temperatures above absolute zero Kelvin. In turn the device produces current fluctuations, and consequently induced gate voltage fluctuations. The current noise power spectral density of thermal noise is given by [27]:

$$S_{Id} = \frac{4kT\mu_{eff}}{L_{eff}^{2}}|Q_{inv}| \tag{2.1}$$

Secondly, current passing through a semiconductor potential barrier, such as the p-n junction of a transistor, will produce shot noise, which is caused by the quantized and random carrier flow through the junction. Random generation leads to fluctuations around the average current I_{ds}. The current noise power spectral density of shot noise is defined as [26]:

$$S_{Id} = 2qI_{ds} \tag{2.2}$$

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Thirdly, in a semiconductor system with considerable number of traps, the continuous trapping and de-trapping processes between donors, acceptors, traps and recombination centers cause carrier number fluctuations in the conduction and valence bands. This in turn creates generation-recombination or g-r noise. The spectrum of the fluctuations of g-r noise is of Lorentzian type characterized by two parameters, the relative variance of number fluctuations and a corner frequency determined by the lifetime of the charge fluctuations in traps located at distance z from the Si/SiO_2 interface. The current noise power spectral density of g-r noise can be described as [28]:

$$S_{Id} = I_{ds}^{\ 2} \frac{S_N}{\overline{N}^2} \qquad (2.3a)$$

$$where \ \frac{S_N}{\overline{N}^2} = \frac{\overline{\Delta N_t}^2}{\overline{N}^2} \frac{4\tau_N}{1+(2\pi f \tau_N)^2} \qquad (2.3b)$$

The last type of noise source in a MOSFET, which is also the focus of research in this work, is the low-frequency, bias-dependent noise effect typically attributed to traps associated with contamination and crystal defects in the silicon/silicon dioxide (Si/SiO_2) interface. This type of noise is termed as $1/f$ noise due to the fact that its power spectral density is proportional to f^{γ}, where $\gamma = 1.0 \pm 0.3$. $1/f$ noise dominates in the lower frequencies, typically in the range of 1 Hz to 1 KHz. Unlike the first three noise sources mentioned above, which are well understood, the origin of the $1/f$ noise in MOSFET is still open to debate despite more than 10 years of research [29-31]. Especially the research of $1/f$ noise behaviour of ultra-deep submicron MOSFETs in the state-of-the-art CMOS technologies has received growing interest from the RFCMOS engineering community lately [11-13], [15]. This is because $1/f$ noise has a major impact on the phase noise and noise figure performance of nonlinear circuits and devices in the GHz regime.

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Phase noise is caused by rapid, short-term, random fluctuations in the phase of a wave due to time domain instabilities in an oscillator. It is typically expressed in units of dBc/Hz at various offsets from the carrier frequency. As discussed earlier on page 2, lines 4 to 15, the dominant phase noise source in silicon-based oscillator circuits originates from device's $1/f$ noise characteristics. This type of noise gets up-converted into close-in phase noise of the oscillator circuits at high frequencies.

The noise factor (F) of a device relates how much additional noise the device will contribute at the output to the noise already from the source at the input. The noise figure (NF) is the conversion of the noise factor to decibels (dB). Higher $1/f$ noise levels will result in greater additional noise contribution from the device itself hence increasing its overall NF.

There are three well-known theories to explain the origin of $1/f$ noise in MOSFETs: the number fluctuation or Δn theory proposed by A. L. McWhorter [32], the mobility fluctuation or $\Delta\mu$ theory proposed by F. N. Hooge [33] and the correlated mobility fluctuation model or Δn-$\Delta\mu$ model proposed by K. K. Hung et al. [34]. The three noise models and their formulation will be discussed in more details in the next four sub-sections.

2.1.1 Number Fluctuation 1/f Noise Model

McWhorter working with germanium filaments at the Massachusetts Institute of Technology (MIT) Lincoln Laboratory in 1957 found that $1/f$ noise in germanium is closely dependent on the ambient atmosphere of the filament. After a series of experiments, he concluded that the $1/f$ noise is predominantly a surface phenomenon.

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McWhorter number fluctuation (Δn) theory originally proposed for 1/*f* noise in germanium states that the origin of number fluctuations is due to the tunneling of charge carriers to and from traps located in the oxide close to the interface [32]. Each trap generates a Lorentzian-type g-r spectrum characterized by its amplitude and a tunneling time constant, which varies with distance from the interface. Christensson et al. [35] were the first to apply the McWhorter theory to MOSFETs, using the assumption that the necessary time constants are caused by the tunneling of carriers from the channel into traps located within the gate oxide. A uniform spatial distribution of oxide traps near the interface will give rise to a distribution of time constants which add up to yield the 1/*f* noise spectrum, i.e. the superposition of a series of Lorentzian-type spectra leads to the resultant 1/*f* noise spectrum. Fig. 2.1 shows pictorially the location of the interfacial traps.

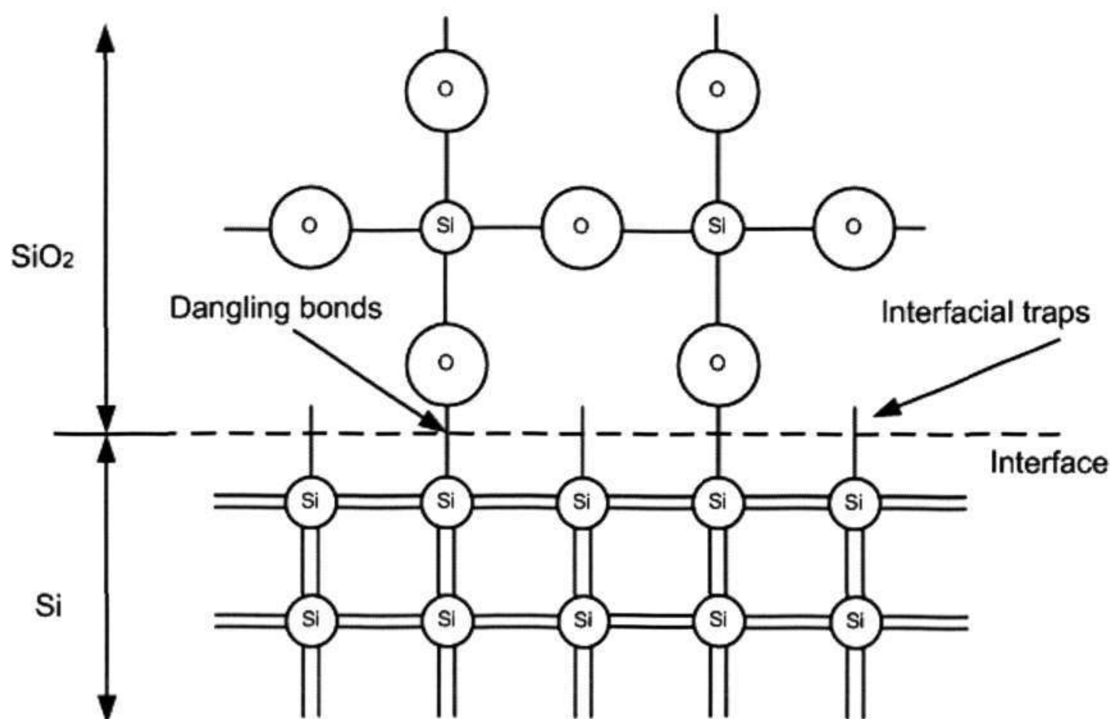

Fig. 2.1: Pictorial depiction of the traps located in the Si/SiO2 interface [36].

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Dangling bonds occur when the silicon lattice is abruptly terminated along a given plane to form a surface. After post-oxidation process, the number of dangling bonds is greatly exaggerated, giving rise to extra energy states that become the interfacial traps [36]. These traps communicate randomly with the charge carriers in the channel via a series of trapping and de-trapping processes.

In order to derive the formulation of the number fluctuation 1/*f* noise model, we will define a typical transistor channel region with channel length, L, width, W and gate oxide thickness, T_{OX} as illustrated in Fig. 2.2. Further to that, let us represent a localized section of the SiO_2 region near the Si/SiO_2 interface with a cube having an elemental volume of ΔV, where $\Delta V = \Delta x \times \Delta y \times \Delta z$ as indicated in Fig. 2.2.

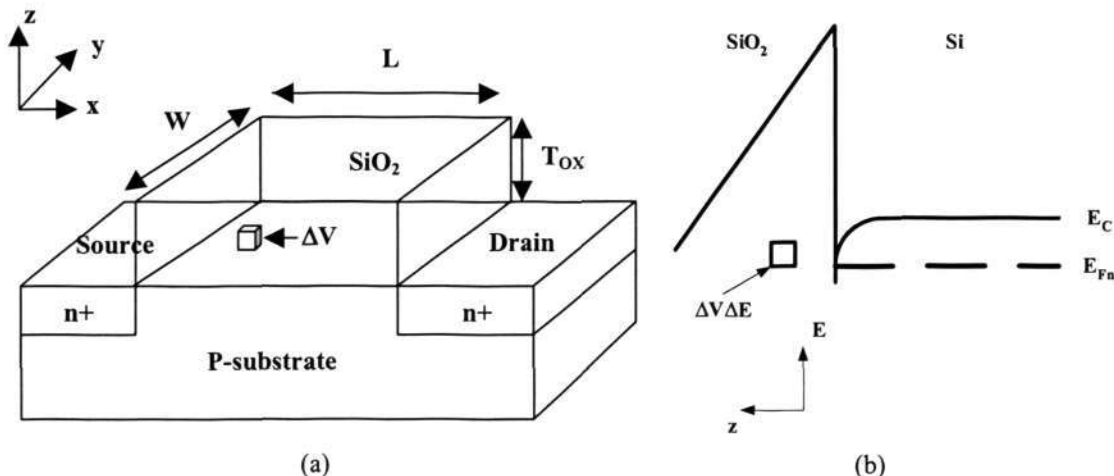

Fig. 2.2: The (a) real space (x, y, z) and (b) energy space (E) coordinate systems of an elemental volume ΔV in a n-channel MOSFET [37].

Several assumptions have been made prior to the formulation of the number fluctuation model [37]:

1. The transistor is biased in the strong inversion region so that the carriers in the conduction band tunnel directly into and out of oxide traps at the same energy level.

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Inelastic tunnelling involving tunnelling of traps at different energy levels is neglected.

2. The transistor is biased in the linear region ($V_{ds} \leq V_{gs} - V_T$) consequently resulting in a nearly constant band bending along the channel from the source to the drain. In addition, it is assumed that the inversion charge, carrier mobility and the electric field are all relatively constant along the channel. Hence the drain current can be expressed as:

$$I_{ds} = \frac{W}{L} \mu_N Q_N V_{ds} \tag{2.4}$$

$$where \;\; Q_N = qN = C_{OX} \cdot \left(V_{gs} - V_T\right) \tag{2.4a}$$

$$g_m = \frac{W}{L} \mu_N C_{OX} V_{ds} \tag{2.4b}$$

3. The trapping of a carrier from the inversion layer by an interface trap is assumed to induce a carrier density fluctuation in the channel only, i.e. any mobility fluctuations due to trapping of the free carriers are considered highly unlikely.

4. The oxide tunnel barrier seen by the inversion layer charge is a rectangular barrier of height Φ_B, which is the height of the oxide conduction band edge from the Si conduction band edge.

The mean square fluctuation, $\overline{\Delta N_t}$ of the number of trapped carriers in the elemental volume at a specific position in real and energy space can be described as [26]:

$$\overline{\Delta N_t} = N_t \cdot f_t \cdot \Delta V \cdot \Delta E \tag{2.5}$$

According to Wiener-Khintchine Theorem [38], [39], the frequency spectrum of the mean square fluctuation of the number of trapped carriers in an elemental volume ΔV in real and energy space is given by:

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$$S_{\overline{\Delta N_t}}(f) = \frac{4\tau_N}{1+(2\pi f\tau_N)^2} \cdot N_t \cdot f_t \cdot (1-f_t) \cdot \Delta V \cdot \Delta E \tag{2.6}$$

$$where\ \ f_t = \frac{1}{1+e^{\frac{E_t - F_t}{kT}}} \tag{2.6a}$$

In strong inversion, the fluctuation in the number of trapped carriers will in turn cause fluctuations in the free carriers in the channel. This consequently leads to fluctuations in the drain current. Thus we have the following relationship [40]:

$$S_{\overline{\Delta N_t}}(f) = S_N(f) \tag{2.7}$$

The frequency spectrum of the mean square fluctuation in the drain current due to fluctuations in the number of carriers trapped in the elemental volume is given by [41]:

$$\Delta S_{Id}(f) = \left(\frac{\Delta I_{ds}}{\Delta N}\right)^2 \cdot S_N(f) \tag{2.8}$$

The drain current fluctuations in an elemental area $\Delta y \Delta x$ at the Si-SiO_2 interface directly beneath the elemental volume ΔV can be derived as follows [2]:

$$I_{ds} = \frac{W}{L}\mu_N Q_N V_{ds} \tag{2.9a}$$

$$where\ \ Q_N = q \cdot N \tag{2.9b}$$

Hence the drain current fluctuations in an elemental area $\Delta y \Delta x$ can be given by:

$$\Delta I_{ds} = \frac{W}{L}\mu_N V_{ds}\ \Delta Q_N \tag{2.9c}$$

$$where\ \ \Delta Q_N = q \cdot \Delta N = \frac{q\delta N \Delta y \Delta x}{WL} \tag{2.9d}$$

$$\Delta I_{ds} = \frac{W\mu_N V_{ds}}{L} \cdot \frac{q\delta N \Delta y \Delta x}{WL} \tag{2.9e}$$

Substituting equation (2.9e) into equation (2.8) and simplifying gives:

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$$\Delta S_{Id} = \left(\frac{W\mu_N V_{ds}}{L} \cdot \frac{q\delta N \Delta y \Delta x}{WL} \right)^2 \cdot \left(\frac{S_N(f)}{\Delta N^2} \right) \tag{2.10a}$$

$$= \left(\frac{W\mu_N q\delta N \Delta y \Delta x V_{ds}}{L} \right)^2 \cdot \left(\frac{S_N(f)}{(WL\Delta N)^2} \right) \tag{2.10b}$$

$$\Delta S_{Id} = \frac{\Delta I_{ds}^{\;2}}{W^2 L^2 \Delta Q_N^{\;2}} \cdot q^2 \cdot S_N(f) \tag{2.10c}$$

The equivalent input-referred gate voltage noise spectrum can be derived as follows:

$$\Delta S_{Vg} = \frac{\Delta S_{Id}}{g_m^{\;2}} = \frac{\Delta I_{ds}^{\;2}}{W^2 L^2 \Delta Q_N^{\;2}} \cdot q^2 \cdot S_N(f) \cdot \frac{L^2}{(\mu_N W C_{OX} V_{ds})^2} \tag{2.11a}$$

$$where \;\; g_m = \frac{\mu_N W C_{OX} V_{ds}}{L} \tag{2.11b}$$

$$= \frac{\Delta I_{ds}^{\;2} \cdot L^2}{W^2 \mu_N^{\;2} \Delta Q_N^{\;2} V_{ds}^{\;2}} \cdot \frac{q^2 \cdot S_N(f)}{W^2 L^2 C_{OX}^{\;2}} \tag{2.11c}$$

$$= \frac{q^2 \cdot S_N(f)}{W^2 L^2 C_{OX}^{\;2}} \tag{2.11d}$$

To calculate the effective voltage noise spectrum for the transistor, we need to integrate equation (2.11) over x, y, z and E as follows:

$$S_{Vg} = \int_0^L \int_0^W \int_0^{d_t} \int_{E_V}^{E_C} \frac{q^2}{W^2 L^2 C_{OX}^{\;2}} \cdot \frac{4\tau_N(z,E)}{1 + (2\pi f \tau_N(z,E))^2} \cdot N_t(z,E) \cdot f_t(E) \cdot (1 - f_t(E))\, dE\, dz\, dy\, dx \tag{2.12}$$

It is assumed that majority of the traps that contribute to the transistor 1/*f* noise are located within the gate oxide from the interface (z=0) to the distance z=d_t, where $d_t \ll T_{OX}$. Solving the outermost two integrals gives the following:

$$S_{Vg} = \frac{4q^2}{WLC_{OX}^{\;2}} \int_0^{d_t} \int_{E_V}^{E_C} \frac{\tau_N(z,E)}{1 + (2\pi f \tau_N(z,E))^2} \cdot N_t(z,E) \cdot f_t(E) \cdot (1 - f_t(E))\, dE\, dz \tag{2.13}$$

To evaluate the integrals of equation (2.13), two additional assumptions have to be made:

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5. A homogeneous oxide trap density, N_t with depth is assumed, i.e. the oxide traps have a uniform spatial distribution in the energy interval involved, independent of the gate voltage [40]. Hence it can be approximated that $N_t(z,E) \approx N_t(E_{Fn})$.

6. The free carriers tunnel to the traps with a tunneling time constant, τ_N, such that the probability of an electron penetrating into the oxide decreases exponentially with distance from the interface [37].

The Shockley-Read-Hall (SRH) statistics for the fluctuation of the charge states or trapped carriers on the SRH centers in a semiconductor are given by [35], [42]:

$$\tau_N(z,E) = \tau_0 e^{(\alpha_t z)} \tag{2.14}$$

$$where\ \alpha_t \approx 10^8\ cm^{-1} \tag{2.14a}$$

$$\tau_0 = \frac{1}{c(n_s + n_1)} \tag{2.14b}$$

$$n_s = n_i e^{\frac{F_n - E_i}{kT}} \tag{2.14c}$$

$$n_1 = n_i e^{\frac{F_t - E_i}{kT}} \tag{2.14d}$$

$$c \approx 10^{-8}\ cm^3/s \tag{2.14e}$$

Using the SRH statistics shown in equation (2.14) above, taking into account assumptions 5 and 6, and approximating the solution to the frequency region where the noise spectrum is given by $1/2\pi f$, the integral of the first term of equation (2.13) can be evaluated as follows [35], [40]:

$$\int_0^{d_t} \frac{\tau_N}{1+(2\pi f \tau_N)^2} dz = \frac{1}{2\pi f \alpha_t}\left(\tan^{-1}\varpi\tau_{\max(d_t)} - \tan^{-1}\varpi\tau_0\right) \tag{2.15}$$

$$\approx \frac{1}{2\pi f \alpha_t}\left(\frac{\pi}{2}\right) \tag{2.15a}$$

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The second term of equation (2.13), $f_t(E)\cdot(1-f_t(E))$ behaves like a delta function around the electron quasi-Fermi level. Since the trap levels around the quasi-Femi level contribute mainly to the integral, it can be evaluated as [35], [43]:

$$\int_{E_V}^{E_C} N_t(E)\cdot f_t(E)\cdot(1-f_t(E))\,dE \approx 4kT\cdot N_t(E_{Fn})\cdot f_t(E_{Fn})\cdot(1-f_t(E_{Fn})) \qquad (2.16)$$

$$\approx 4kTN_t(E_{Fn}) \qquad (2.16a)$$

Finally substituting equations (2.15a) and (2.16a) into (2.13) yields:

$$S_{Vg} = \frac{4kTq^2 N_t(E_{Fn})}{\alpha_t WLfC_{OX}{}^2} \qquad (2.17)$$

2.1.2 Mobility Fluctuation 1/f Noise Model

The Δμ $1/f$ noise model is essentially empirical in nature. It was first proposed by Hooge [33] to explain the $1/f$ noise phenomenon in homogeneous semiconductors, namely in resistors with ideal ohmic contacts.

The current noise of a homogeneous resistor is governed by the following relationships [41]:

$$V = I(t)R(t) = const. \qquad (2.18a)$$

$$\frac{\delta I}{I} = -\frac{\delta R}{R} \qquad (2.18b)$$

$$\frac{S_I(f)}{I^2} = \frac{S_R(f)}{R^2} \qquad (2.18c)$$

Hooge observed that the normalized current noise spectral density for a wide range of materials has the following relationship:

$$\frac{S_I(f)}{I^2} = \frac{const.}{f} \qquad (2.19)$$

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He later proposed the following empirical equation for a homogeneous semiconductor material:

$$\frac{S_I(f)}{I^2} = \frac{S_R(f)}{R^2} = \frac{\alpha_H}{Nf} \tag{2.20}$$

where α_H is known as the Hooge's constant. For the numerous semiconductor samples that Hooge characterized, he concluded that α_H had a constant value of approximately 10^{-3}, nearly independent of the material. However nowadays, and also demonstrated later in chapters 4, 5 and 6 of this work, it is known that α_H varies according to the quality of the semiconductor material and is also gate voltage dependent. Its magnitude can in fact vary over several decades. This later led to the refinement of the original Hooge's constant as follows [2]:

$$\alpha_H = \alpha_{H^*}\left(\frac{\mu_{eff}}{\mu_{latt}}\right) \tag{2.21}$$

The formulation in equation (2.21) assumed that the lattice or phonon scattering is the dominant 1/*f* noise generating mechanism, although other types of scattering mechanisms, such as Coulombic scattering, are also present. The effective mobility of the device μ_{eff} can be obtained according to Matthiessen's theorem [55], [56]:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{latt}} + \sum_i^n \frac{1}{\mu_i} \tag{2.22}$$

In equation (2.22), *n* is the total number of different scattering processes denoted by *i*.

Adapting Hooge's model to the case of a typical transistor in the linear region using equations (2.4a) and (2.20) gives the following [44]:

$$S_{I_d} = \frac{q\alpha_H}{WLfQ_N} \cdot I_{ds}^{\ 2} \tag{2.23a}$$

$$S_{Vg} = \frac{q\alpha_H}{WLfC_{OX}}\left(V_{gs} - V_T\right) \tag{2.23b}$$

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2.1.3 Comparison between Number Fluctuation and Mobility Fluctuation 1/f Noise Models

There is still much controversy surrounding the argument of whether the origin of $1/f$ noise in MOSFETs is due to Δn fluctuations or $\Delta \mu$ fluctuations [30]. One way to discriminate between the two mechanisms is to highlight the differences between the two mechanisms.

From equations (2.17) and (2.23b), firstly it can be observed that in the Δn fluctuation model, the noise spectral density is independent of any dc bias condition, whereas the $\Delta \mu$ fluctuation model predicts that $1/f$ noise is linear with increasing gate overdrive voltage. Secondly both models predict an improvement of $1/f$ noise with the scaling of oxide thickness. The Δn fluctuation model predicts that $1/f$ noise decreases with increasing C_{ox}^2, whereas the $\Delta \mu$ mobility fluctuation model predicts that $1/f$ noise decreases with increasing C_{ox}. Both models predict that $1/f$ noise decreases with increasing device area WL.

The availability of submicrometer-size small channel area (< 1 μm^2) MOSFETs for random telegraph signal (RTS) studies and $1/f$ noise measurements [45-47], has recently led to another school of thought with regard to the origin of $1/f$ noise in MOSFETs. Based on RTS studies of small area devices, several researchers [34] proposed that the above-mentioned two noise mechanisms are actually not independent from each other but are correlated, since they originate from the same noise fluctuation source, i.e. the fluctuation in the occupancy of the oxide traps. The next sub-section examines this correlated noise theory in details.

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2.1.4 Correlated Mobility Fluctuation 1/f Noise Model

One of the earliest attempts to combine the Δn and Δμ fluctuation phenomena to explain the origin of 1/*f* noise in MOSFET is by Mikoshiba et al. [48], [49]. Subsequently the availability of small area MOSFETs for RTS study by other researchers resulted in the development of the correlated mobility fluctuation model [34], [37], [50-52]. This model essentially states that both the carrier number fluctuations and the surface mobility fluctuations give rise to transistor drain current fluctuations. This is because besides causing carrier number fluctuations in the channel, charge oxide traps can in parallel scatter or disturb the flow of carriers in the channel leading to surface carrier mobility fluctuations. Hence these two phenomena are actually correlated to each other.

With reference to the coordinate system illustrated in Fig. 2.2, the equations shown in (2.4) and (2.4a), and the fact that fluctuations in the occupancy of the oxide traps will induce correlated fluctuations in both the channel carrier number and surface mobility, one can expressed the resultant fractional change of the local drain current in the elemental volume ΔV by re-writing equation (2.9) as follows [37]:

$$\delta I_{ds} = \frac{WV_{ds}}{L}\cdot\left(\mu_N \frac{q\delta N\Delta y\Delta x}{WL} \pm Q_N \delta\mu_N\right) \tag{2.24a}$$

$$= \left(\frac{W}{L}\mu_N Q_N V_{ds}\right)\cdot\left(\frac{1}{Q_N}\cdot\frac{q\delta N\Delta y\Delta x}{WL} \pm \frac{1}{\mu_N}\cdot\delta\mu_N\right) \tag{2.24b}$$

$$= I_{ds}\cdot\left(\frac{1}{\Delta N}\cdot\delta\Delta N \pm \frac{1}{\mu_N}\cdot\delta\mu_N\right) \tag{2.24c}$$

$$\frac{\delta I_{ds}}{I_{ds}} = \left(\frac{1}{\Delta N}\cdot\frac{\delta\Delta N}{\delta\Delta N_t} \pm \frac{1}{\mu_N}\cdot\frac{\delta\mu_N}{\delta\Delta N_t}\right)\cdot\delta\Delta N_t \tag{2.24d}$$

$$where\ \ \Delta N = NW\Delta x \tag{2.24e}$$

$$\Delta N_t = N_t W\Delta x \tag{2.24f}$$

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Note that N and N_t are the number of channel carriers and the occupied traps per unit area respectively. The sign of the mobility term in equation (2.24d) is chosen according to whether the trap is neutral or charged when filled, i.e. the sign will be chosen either negative for acceptor-like traps or positive for donor-like traps.

The ratio of the fluctuations in the channel carriers to the fluctuations in the occupied traps $\frac{\delta\Delta N}{\delta\Delta N_t}$ can be approximated to unity at strong inversion but assumes a smaller value at other bias conditions [53], [54]. The ratio $\frac{\delta\Delta N}{\delta\Delta N_t}$ has been generalized in [51] as follows:

$$R = \frac{\delta\Delta N}{\delta\Delta N_t} = -\frac{C_{inv}}{C_{OX} + C_{inv} + C_{dep} + C_{it}} \tag{2.25}$$

$$where\ C_{inv} \approx \frac{q^2 N}{kT} \tag{2.25a}$$

Equation (2.25) can be re-written as [51]:

$$R = -\frac{N}{N + N^*} \tag{2.26}$$

$$where\ N^* = \frac{kT}{q^2}\cdot\left(C_{OX} + C_{dep} + C_{it}\right) \tag{2.26a}$$

To evaluate the ratio $\frac{\delta\mu_N}{\delta\Delta N_t}$, one needs to correlate fluctuations in the channel carrier mobility to fluctuations of the oxide trap density. This relationship can be realized via the use of the Matthiessen's rule [55], [56]:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_n} + \frac{1}{\mu_{ox}} = \frac{1}{\mu_n} + \alpha_{sc} N_t \tag{2.27}$$

The ratio of the fluctuations in the channel carrier mobility to the fluctuations in the oxide charge density has been solved in [34] as follows:

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$$\frac{\delta\mu_{eff}}{\delta\Delta N_t} = -\frac{\alpha_{sc}\mu_{eff}^{\ 2}}{W\Delta x} \tag{2.28}$$

Note that the term μ_{eff} is equivalent to the term μ_N used in all previous equations. Hence these two terms can be used interchangeably. Substituting equations (2.25) and (2.28) into equation (2.24d) and simplifying yields:

$$\frac{\delta I_{ds}}{I_{ds}} = -\left(\frac{R}{N} \pm \alpha_{sc}\mu_{eff}\right)\cdot\frac{\delta\Delta N_t}{W\Delta x} \tag{2.29}$$

Substituting equation (2.29) into (2.8) and simplifying, the power spectrum density of the local current fluctuations is given by:

$$\Delta S_{Id} = \left(\frac{I_{ds}}{W\Delta x}\right)^2\cdot\left(\frac{R}{N} \pm \alpha_{sc}\mu_{eff}\right)^2\cdot S_N \tag{2.30}$$

Invoking the number fluctuation theory, similar to that employed for equation (2.12) earlier, one can express the effective drain current noise spectral density for the transistor as:

$$S_{Id} = \int_0^L\int_0^W\int_0^{d_t}\int_{E_V}^{E_C}\left(\frac{I_{ds}}{W\Delta x}\right)^2\cdot\left(\frac{R}{N(x)} \pm \alpha_{sc}\mu_{eff}\right)^2\cdot\frac{4\tau_N(z,E)}{1+(2\pi f\tau_N(z,E))^2}\cdot$$
$$N_t(z,E)\cdot\Delta x\cdot f_t(E)\cdot(1-f_t(E))\,dE\,dz\,dy\,dx \tag{2.31}$$

Using equations (2.15a) and (2.16a) stated previously, the innermost three integrals for the following terms in equation (2.31) can be evaluated as:

$$\int_0^W\int_0^{d_t}\int_{E_V}^{E_C}\frac{4\tau_N(z,E)}{1+(2\pi f\tau_N(z,E))^2}\cdot N_t(z,E)\cdot\Delta x\cdot f_t(E)\cdot(1-f_t(E))\,dE\,dz\,dy \tag{2.32}$$

$$= \frac{\pi}{4\pi f\alpha_t}\cdot 4kTN_t(E_{Fn})\cdot W\Delta x \tag{2.32a}$$

$$= \frac{kTW\Delta x}{\alpha_t f}\cdot N_t(E_{Fn}) \tag{2.32b}$$

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Substituting equation (2.32b) into equation (2.31), the outermost integral in equation (2.31) is given by [41]:

$$S_{Id} = \frac{1}{L^2}\int_0^L \left(\frac{I_{ds}}{W\Delta x}\right)^2 \cdot \left(\frac{R}{N(x)} \pm \alpha_{sc}\mu_{eff}\right)^2 \cdot \frac{kTW\Delta x}{\alpha_t f} \cdot N_t(E_{Fn}) \cdot \Delta x \, dx \tag{2.33}$$

$$= \frac{kTI_{ds}^2}{\alpha_t fWL^2} \cdot \int_0^L N_t(E_{Fn}) \cdot \left(\frac{R}{N(x)} \pm \alpha_{sc}\mu_{eff}\right)^2 dx \tag{2.33a}$$

At strong inversion and in the linear region, $R = \frac{\delta \Delta N}{\delta \Delta N_t}$ can be approximated to unity, thus equation (2.33a) can be simplified as:

$$S_{Id} = \frac{kTI_{ds}^2}{\alpha_t fWL} \cdot \left(\frac{1}{N} \pm \alpha_{sc}\mu_{eff}\right)^2 \cdot N_t(E_{Fn}) \tag{2.34a}$$

$$S_{Vg} = \frac{kTq^2}{\alpha_t fWLC_{OX}^2} \cdot (1 \pm \alpha_{sc}\mu_{eff}N)^2 \cdot N_t(E_{Fn}) \tag{2.34b}$$

In the general case, to solve the integral of equation (2.33a), reference [51] proposed to analyze the bias dependencies of the terms within the integral. Using equations (2.4) and (2.4a), equation (2.33a) can be expressed as follows:

$$S_{Id} = \frac{kTI_{ds}^2}{\alpha_t fWL^2} \cdot \int_0^L N_t(E_{Fn}) \cdot \left(1 \pm \alpha_{sc}\mu_{eff}\frac{N(x)}{R}\right)^2 \cdot \left(\frac{R}{N(x)}\right)^2 dx \tag{2.35a}$$

$$= \frac{kTI_{ds}^2}{\alpha_t fWL^2} \cdot \int_0^L N_t(E_{Fn}) \cdot \left(1 \pm \alpha_{sc}\mu_{eff}\frac{N(x)}{R}\right)^2 \cdot \left(\frac{R^2}{N(x)}\right) \cdot \left(\frac{q}{Q_N}\right) dx \tag{2.35b}$$

$$= \frac{kTI_{ds}W\mu_{eff}Q_N V_{ds}}{\alpha_t fWL^3} \cdot \int_0^L N_t(E_{Fn}) \cdot \left(1 \pm \alpha_{sc}\mu_{eff}\frac{N(x)}{R}\right)^2 \cdot \left(\frac{R^2}{N(x)}\right) \cdot \left(\frac{q}{Q_N}\right) dx \tag{2.35c}$$

$$= \frac{kTqI_{ds}\mu_{eff}V_{ds}}{\alpha_t fL^3} \cdot \int_0^L N_t(E_{Fn}) \cdot \left(1 \pm \alpha_{sc}\mu_{eff}\frac{N(x)}{R}\right)^2 \cdot \left(\frac{R^2}{N(x)}\right) dx \tag{2.35d}$$

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$$= \frac{kTqI_{ds}\mu_{eff}V_{ds}}{\alpha_t fL^2} \cdot N_t(E_{Fn}) \cdot \left(1 \pm \alpha_{sc}\mu_{eff}\frac{N}{R}\right)^2 \cdot \left(\frac{R^2}{N}\right) \quad (2.35e)$$

$$= \frac{kTqI_{ds}\mu_{eff}}{\alpha_t fL^2} \cdot \int_0^{V_{ds}} N_t(E_{Fn}) \cdot \left(1 \pm \alpha_{sc}\mu_{eff}\frac{N}{R}\right)^2 \cdot \left(\frac{R^2}{N}\right) dV \quad (2.35f)$$

$$= \frac{kTqI_{ds}\mu_{eff}}{\alpha_t fL^2} \cdot \int_0^{V_{ds}} N_t^*(E_{Fn}) \cdot \left(\frac{R^2}{N}\right) dV \quad (2.35g)$$

$$where\ N_t^*(E_{Fn}) = N_t(E_{Fn}) \cdot \left(1 \pm \alpha_{sc}\mu_{eff}\frac{N}{R}\right)^2 \quad (2.35h)$$

For ease of implementation of the noise model into a spice simulator, the term $N_t^*(E_{Fn})$ has been approximated as follows [51]:

$$N_t^*(E_{Fn}) = A + BN + CN^2 \quad (2.36)$$

where A, B and C are technology-dependent model parameters. They correspond to the noise parameters NOIA, NOIB and NOIC implemented in BSIM3v3 $1/f$ noise model [57].

The evaluation of the integral of equation (2.35g) can be achieved by examining the solutions at three different operating regions of the transistor and then summing up the solution for each region via superposition.

1) Linear region in strong inversion ($V_{gs} > V_T$ and $V_{ds} < V_{dsat}$)

In the strong inversion region, the channel carrier charge density is given by:

$$qN(x) = C_{OX}\left(V_{gs} - V_T - A_{bulk}V(x)\right) \quad (2.37)$$

Consequently the carrier densities at the source and drain ends can be expressed as:

$$qN_0 = qN(0) = C_{OX}\left(V_{gs} - V_T\right) \quad (2.38a)$$

$$qN_L = qN(L) = C_{OX}\left(V_{gs} - V_T - A_{bulk}V_{ds}\right) \quad (2.38b)$$

$$q\Delta N = q\left(N_0 - N_L\right) = C_{OX}\left(A_{bulk}V_{ds}\right) \quad (2.38c)$$

$$V_{ds} = \frac{q\Delta N}{A_{bulk}C_{OX}} \quad (2.38d)$$

Substituting equation (2.38d) into equation (2.35e) and re-arranging gives:

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$$S_{Id} = \frac{kTq^2 I_{ds}\mu_{eff}}{A_{bulk}\alpha_t f L^2 C_{OX}} \int_{N_L}^{N_0} N_t^*(E_{Fn}) \cdot \left(\frac{R^2}{N}\right) dN \qquad (2.39)$$

Using equations (2.26) and (2.36), the integral of equation (2.39) can be evaluated as [51]:

$$S_{Id} = \frac{kTq^2 I_{ds}\mu_{eff}}{A_{bulk}\alpha_t f L^2 C_{OX}} \cdot \left[A \cdot \ln\frac{N_0 + N^*}{N_L + N^*} + B \cdot (N_0 - N_L) + \frac{C}{2} \cdot \left(N_0^2 - N_L^2\right) \right] \qquad (2.40)$$

2) Saturation region in strong inversion ($V_{gs} > V_T$ and $V_{ds} \geq V_{dsat}$)

The channel in this region can be partitioned into two parts, namely the triode channel region from L=0 to $L=L_s$ and the pinch-off region from $L=L_s$ to L_{eff}. Using equation (2.35a), the drain current spectral density for these two sections can be written as [51]:

$$S_{Id} = \frac{kT I_{ds}^2}{\alpha_t f W L^2} \cdot \int_0^{L_s} N_t^*(E_{Fn}) \cdot \left(\frac{R}{N(x)}\right)^2 dx + \frac{kT I_{ds}^2}{\alpha_t f W L^2} \cdot \int_{L_s}^{L_{eff}} N_t^*(E_{Fn}) \cdot \left(\frac{R}{N(x)}\right)^2 dx \qquad (2.41)$$

The expression for the first term in the integral is similar to equation (2.40) with V_{ds} replaced by V_{dsat} in the expression for N_L. An assumption made to evaluate the second term in the integral is that both the electron quasi-Fermi level and carrier density are uniform in the pinch-off region and is equal to the channel potential at the boundary of the pinch-off point. Thereafter, it can be shown that the integral in equation (2.41) can be evaluated as [51]:

$$\begin{aligned} S_{Id} = {} & \frac{kTq^2 I_{ds}\mu_{eff}}{A_{bulk}\alpha_t f L^2 C_{OX}} \cdot \left[A \cdot \ln\frac{N_0 + N^*}{N_L + N^*} + B \cdot (N_0 - N_L) + \frac{C}{2} \cdot \left(N_0^2 - N_L^2\right) \right] + \\ & \Delta L_{clm} \cdot \frac{kT I_{ds}^2}{\alpha_t f W L^2} \frac{A + BN_L + CN_L^2}{\left(N_L + N^*\right)^2} \end{aligned} \qquad (2.42)$$

$$where\ \Delta L_{clm} = l_c \sinh^{-1}\left(\frac{V_{ds} - V_{dsat}}{l_c E_{sat}}\right) \qquad (2.42a)$$

$$l_c = \sqrt{\frac{\varepsilon_{si} T_{OX} X_{dep}}{\varepsilon_{OX}}} \qquad (2.42b)$$

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3) Subthreshold region ($V_{gs} < V_T$)

In this region, the channel charge density can be expressed as [58]:

$$qN = \frac{C_{dep}^{*}kT}{q} \cdot \exp\left[\frac{q(V_{gs}-V_{gc})}{nkT} - \frac{q\phi_F}{2kT} - \frac{qV}{kT}\right] \quad (2.43)$$

$$where\ n = \frac{\left(C_{OX} + C_{dep}^{*} + C_{it}^{*}\right)}{C_{OX}} \quad (2.43a)$$

where C_{dep}^{*}, C_{it}^{*} and V_{gc} are the depletion capacitance, interface trap capacitance and the gate voltage when the surface potential is equal to $1.5\phi_F$ respectively.

Substituting equation (2.43) into equation (2.35f) yields [51]:

$$S_{Id} = \frac{k^2T^2 I_{ds}\mu_0}{\alpha_t f L^2} \int_{N_L}^{N_0} \frac{N_t^{*}(E_{Fn})}{\left(N^{*}+N\right)^2} dN \quad (2.44)$$

$$where\ qN_0 = \frac{qK_s}{kT} \cdot \exp\left[\frac{q}{nkT} \cdot \left(V_{gs}-V_T\right)\right] \quad (2.44a)$$

$$qN_L = qN_0 \cdot \left[1-\exp\left(-\frac{qV_{ds}}{kT}\right)\right] \quad (2.44b)$$

$$K_s = \left(\frac{kT}{q}\right)^2 \cdot C_{dep}^{*} \cdot \exp\left[\frac{q}{nkT}\left(V_T - V_{gc}\right) - \frac{1}{2}\frac{q\phi_F}{kT}\right] \quad (2.44c)$$

With the assumptions that $N << N^{*}$ and $N_t^{*}(E_{Fn}) = A + BN + CN^2 \approx A$, the integral in equation (2.44) can be evaluated as [51]:

$$S_{Id} = \frac{AkTI_{ds}^{2}}{\alpha_t f WLN^{*2}} \quad (2.45)$$

By summing the drain current noise spectral densities given by equations (2.40), (2.42) and (2.45), one can compute the resultant noise power at any given bias condition. Furthermore these three equations have implemented in the BSIM3v3 $1/f$ noise compact model [57].

With the aid of equation (2.4a), the analysis of equation (2.34b) shows that the

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input-referred gate noise power S_{Vg} has one term proportional to $\frac{1}{C_{OX}{}^{2}}$ (similar to the S_{Vg} dependency of the carrier number fluctuation model), and another term proportional to $\frac{(V_{gs}-V_T)}{C_{Ox}}$ (similar to the S_{Vg} dependency of the carrier mobility fluctuation model). Furthermore at low gate bias, the term $\frac{1}{N}$ will be much bigger than $\alpha_{sc}\mu_{eff}$ since the channel carrier density diminishes. Subsequently from equation (2.34a), the model reduces to the carrier number fluctuation model. At high gate bias, the reverse trend is true and the model then reduces to the carrier mobility fluctuation model.

2.2 *Impact of Processing Technologies on the 1/f Noise Performance of Deep Submicron Transistors*

2.2.1 *Overview of CMOS Transistor Process Flow*

This section provides a general overview of a baseline deep submicron CMOS process flow. However the detailed processing conditions have not been listed due to confidentiality agreements with the foundry providing the silicon hardwares across multiple technology nodes.

A typical deep submicron CMOS processing technology begins with the growth of a thin layer of pad oxide on the p-type semiconductor bulk substrate with crystal orientation of <100> and substrate resistivity of 6-9 ohm-cm. This layer of initial pad oxide serves to cleanse the surface of the substrate of impurities and it will be stripped away before the next step. Subsequently another thin layer of pad oxide and a layer of nitride are deposited across the wafer. Following that nitride etch is performed using the active layer mask to

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define the regions needed for isolation formation. For deep submicron technologies, the shallow trench isolation (STI) scheme is employed. Once the trenches are formed, they are filled with oxide and then planarized using chemical mechanical polishing (CMP). Following that the layer of nitride is removed.

Retrograde well formation encompassing well, threshold voltage adjust and punchthrough implants, takes place. Thereafter an anneal step involving high temperature thermal cycle is performed to alleviate some of the implant damages or defects due to well formation. This is followed next by the dual thickness gate oxide deposition process. First a pre-gate clean step is performed; this is followed by the growth of the thick gate oxide across the wafer. Then the thick gate oxide is etched away in areas where it is not required. Then a second pre-gate clean step takes place; this is followed by the growth of the thin gate oxide. During the growth of the thin gate oxide, nitridation occurs across the wafer thereby resulting in both the thick and thin gate oxide areas being nitrided. The deposition, definition and subsequent re-oxidation of the gate polysilicon follow next.

The self-aligned source and drain lightly-doped drain (LDD) implants take place with the gate polysilicon acting as the self-aligned hard mask. Following this is the deposition of a layer of nitride and etching to form the gate polysilicon spacer. Subsequently source and drain implants occur, coupled with an anneal step at the end. Next salicidation of the source, drain and gate polysilicon areas takes place. At this juncture, the front-end-of-line (FEOL) processing has been completed.

The back-end-of-line (BEOL) processing starts with the deposition of a layer of inter-layer dielectric (ILD) across the wafer. This is followed by contact etch and tungsten plug formation for the 0.35μm, 0.25μm and 0.18μm technology nodes and copper via formation for the 0.13μm technology node. The steps subsequent to this is a series of

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metallization and via formation till the top metal is defined, which for an *N*-level CMOS process will be metal-*N*. The BEOL processing finishes with the passivation and bondpad masking and definition processes.

2.2.2 Impact of FEOL Process Modules on Transistor 1/f Noise Performance

One of the most important FEOL process modules that have a major impact on the transistor 1/*f* noise performance is the gate oxidation conditions. This topic is also the focus of this research work. The use of nitrided gate oxide as an alternative to pure SiO_2 gate oxide in scaled technologies is necessary for several reasons. This has been discussed in details in section 1.1 of chapter 1 earlier.

There have been numerous studies published with regard to the 1/*f* noise performance of nitrided oxides fabricated using different nitridation recipes, namely NH_3 annealed thermal oxides (NO) which are subsequently reoxidized (RNO) [59], N_2O annealed oxides [60] and rapid thermal (RT) CVD oxynitrides [22]. Comparison between the interface state densities and noise levels for the different types of nitrided oxide under similar bias condition has been performed in [61] and the results are illustrated in Fig. 2.3. It can be concluded that gate oxide nitridation results in severe degradation of the transistor 1/*f* noise performance and this can be attributed to the higher oxide interface state density.

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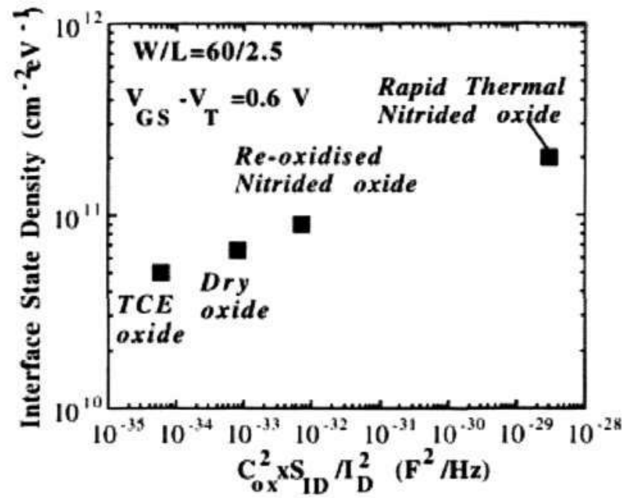

Fig. 2.3: Comparison of the interface state density and the normalized noise levels under similar bias conditions [61].

Morfouli et al. [22] demonstrated that a higher degree of nitridation result in higher $1/f$ voltage noise levels for both n- and p-MOSFETs. This is illustrated in Figs. 2.4(a) and (b).

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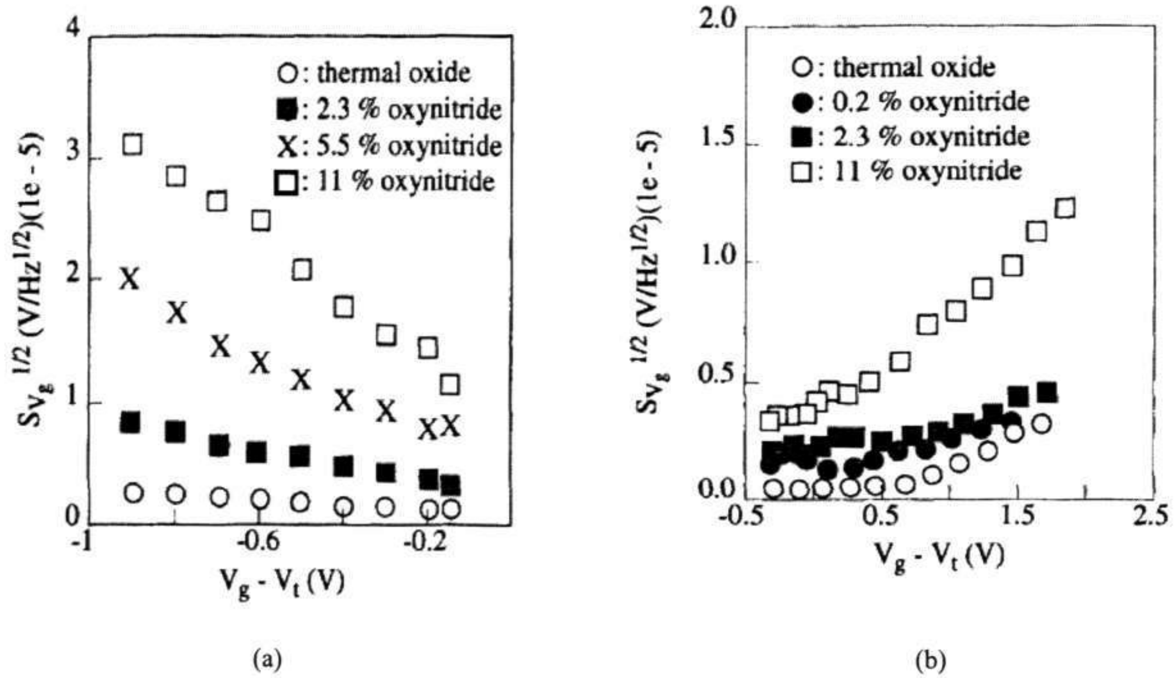

Fig. 2.4: Effect of gate overdrive voltage and percentage of nitrogen incorporation into the gate oxide on the input-referred gate voltage noise $S_{V_g}^{1/2}$ for (a) p-channel and (b) n-channel MOSFETs. Transistor aspect ratio W/L = 10/3; frequency for comparison = 10Hz and V_{ds} = 0.05V [22].

Morfouli et al. [22] has correlated the trend seen in Figs. 2.4(a) and (b) to the finding that the oxide trap density varies almost exponentially with the nitrogen concentration within the film for both n- and p-MOSFETs. This is shown in Fig. 2.5.

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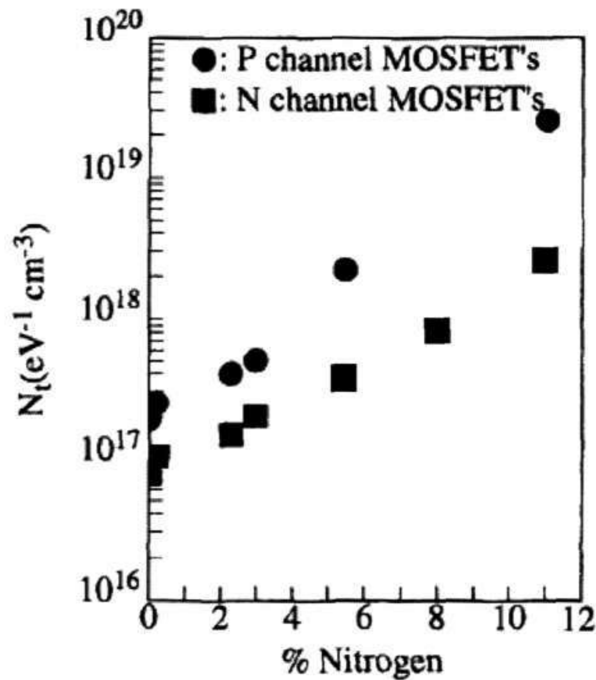

Fig. 2.5: Oxide trap density variation with percentage of nitrogen incorporated into the gate dielectric for n- and p-MOSFETs. The oxide trap density values have been derived from $1/f$ noise measurements [22].

Ohguro et al. [23] studied the analog characteristics of MOSFETs with heavily nitrided NO oxynitrides and also found that transistor with oxynitride gate oxide has higher interface state density as compared to its pure oxide counterpart. This is shown in Figs. 2.6(a) and (b). This in turn brings about a degradation of the transistor $1/f$ noise performance as shown in Fig. 2.6(c).

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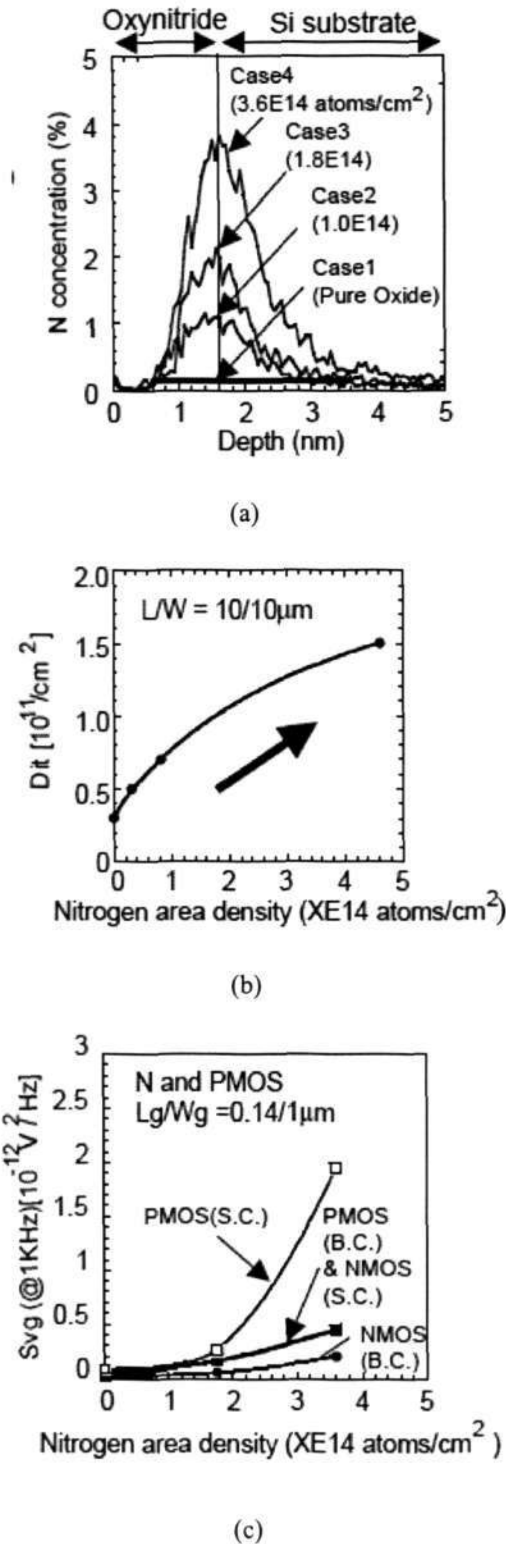

Fig. 2.6: (a) Nitrogen profile in the oxynitride films for the various nitrogen concentration investigated; (b) Effect of nitrogen area density on the interface state density of the transistors with nitrided NO oxynitrides and (c) Dependence of S_{Vg} on nitrogen area density for n- and p-channel transistors [23] B.C stands for buried channel and S.C. stands for surface channel.

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In the published works mentioned earlier in pages 32-36, the investigation of the effect of nitridation on transistor 1/*f* noise performance has been performed within a single technology node. The investigation of the effect of nitridation on transistor 1/*f* noise performance across multiple technology nodes is still lacking. Hence this research work aims to fulfill this gap of providing results on the effect of technology downscaling on transistor 1/*f* noise performance. One of the consequences of technology downscaling is the need for a higher degree of gate dielectric nitridation to achieve acceptable static performance for both n-channel and p-channel transistors.

Another area that is related to the gate oxidation condition that has been reported in literature is the pre-gate clean process module. Toita et al. [62] reported that the 1/*f* noise magnitude in p-MOSFET could be reduced by adding an additional pre-oxidation cleaning step using an ammonia hydrogen peroxide mixture (APM) prior to oxide growth. The results illustrated in Fig. 2.7 shows that the voltage noise level has been reduced by a maximum of 14 dBV^2/Hz at 2 Hz. This has been attributed to the lower interface state density with the additional APM preoxidation cleaning step. However additional cost is associated with this proposed cleaning step.

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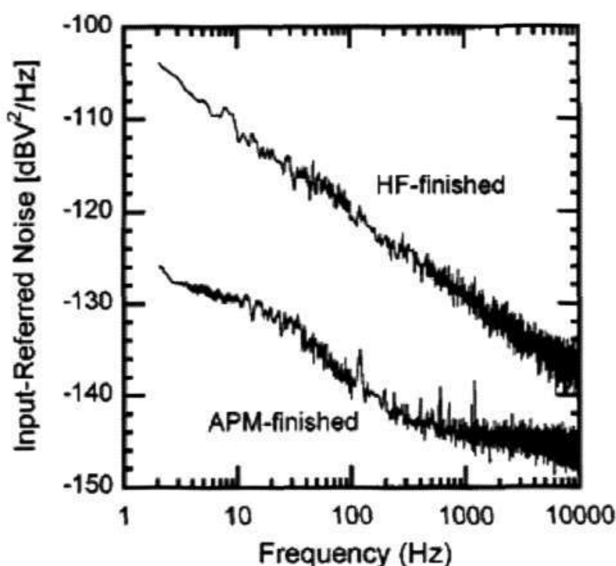

Fig. 2.7: Input-referred gate voltage noise spectra for PMOSFETs with W/L = 15/0.5, V_{ds} = -1V and V_{gs}-V_T = -0.11V. HF-finished refers to the control device with hydro-fluoride (HF) clean treatment. It can be observed that significantly lower noise power resulted due to the additional APM treatment [62].

Research work has been done to study the effect of the Local Oxidation of Silicon (LOCOS) isolation scheme on the noise performance of the transistor measured in the gated source or drain diode configuration [63]. The results showed that RTS noise is generated, which has been attributed to the fact that the stressed edges of the LOCOS structure or the bird's beak regions are prone to the generation of interface traps. In deep submicron technologies, the LOCOS isolation scheme has been replaced by the STI isolation scheme. It has been reported by Ohguro et al. [64] that mechanical stress induced by STI, which is compressive in nature, degrades both n- and p-channel transistors $1/f$ noise performance. However the degradation is more severe in p-MOSFET as compared to n-MOSFET, as illustrated in Figs. 2.8(b) and (c). This can be attributed to the fact that compressive stress improves p-MOSFET but degrades n-MOSFET static characteristics. Ohguro et al. then proposed that the compressive mechanical stress due to STI induces

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greater mobility fluctuations (but not increasing oxide trap density), thereby resulting in the transistor 1/*f* noise degradation. This is illustrated in Fig. 2.8(d).

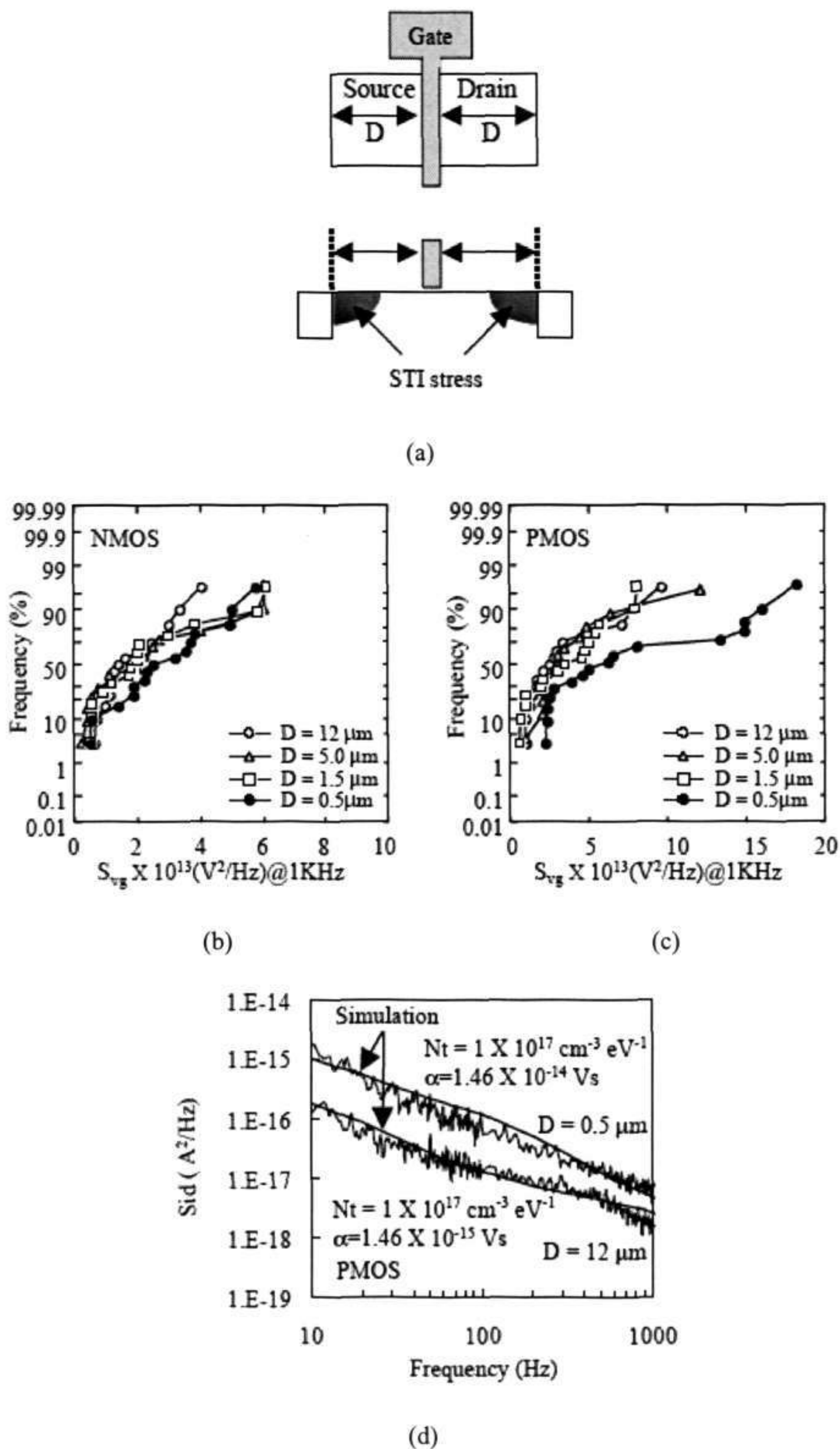

Fig. 2.8: (a) Effect of the variation of the STI edge distance from the gate electrode (D) on S_{V_g} of (b) n-MOSFETs and (c) p-MOSFETs with W/L = 5/0.11. Fig. (d) illustrates the simulation versus measurement

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results for p-MOSFETs with D = 0.5 and 12 μm respectively. The results showed that the scattering parameter α is one order larger for the device with D = 0.5μm as compared to its counterpart with D = 12μm [64].

On the source/drain engineering front, Wu et al. [65], investigated the effect of pocket implantation on the n-channel transistor *1/f* noise performance. Pocket implantation is necessary in deep submicron processes to reduce the subthreshold leakage currents in MOSFETs. Wu et al. demonstrated that a higher pocket implant dosage will degrade n-channel transistors *1/f* noise performance across the entire range of gate overdrive voltage measured, as shown in Figs. 2.9(a) and (b). The researchers attributed the increase in the *1/f* noise to the non-uniform threshold voltage distribution along the channel due to the presence of the high dose pocket implants. This is illustrated in Fig. 2.9(c). The degradation is more severe for shorter channel length devices since the pocket implant regions occupy a significant portion of the channel region.

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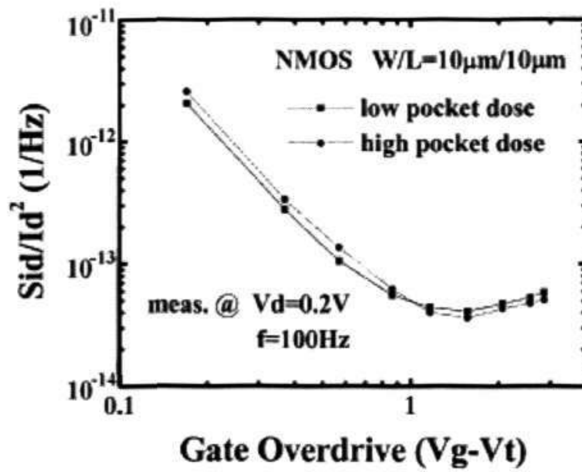
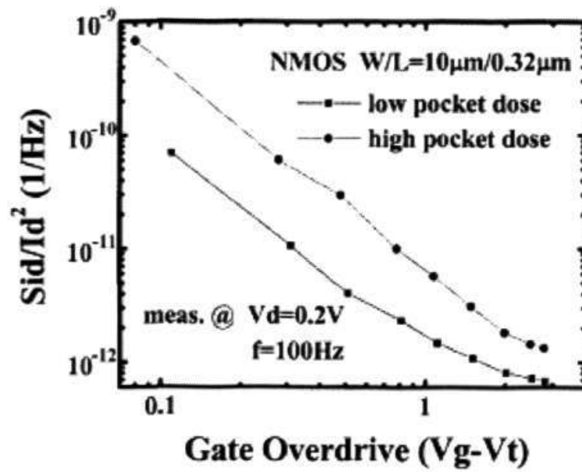


(a)



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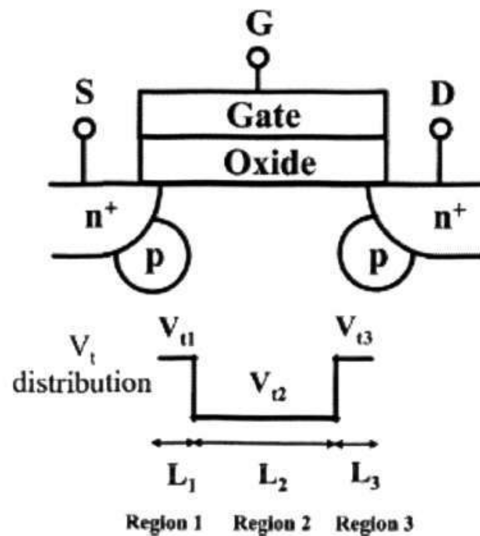

(c)

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Fig. 2.9: Effect of varying the pocket implant dose on the normalized drain current noise spectral density versus the gate overdrive voltage (V_{gs}-V_T) for (a) n-MOSFETs with W/L = 10/10 and (b) n-MOSFETs with W/L = 10/0.32. Fig. (c) illustrates the non-uniform threshold voltage distribution along the channel due to the presence of the pocket implants. Regions 1 and 3 represent the pocket-implanted areas that possess a higher threshold voltage. Region 2 represents the remaining channel region [65].

The effect of the parasitic series resistance of LDD MOSFETS on transistor 1/*f* noise performance has been studied by several researchers [66-68] in the past. Fig. 2.10(a) and 2.10(b) show the plots of the normalized current noise versus the gate overdrive voltage for a set of different channel length n-channel and p-channel devices fabricated in the 0.35μm CMOS technology [2]. It can be observed that for gate overdrive voltages below and around the threshold level, the normalized current noise magnitude scales with 1/L. However for higher gate overdrive voltages, the noise power saturates at a constant value, indicating the dominance of the 1/*f* noise generated in the series resistance portions of the source/drain LDD regions. It can be further observed that the effect of the parasitic series resistance noise is more pronounced for the longer channel length devices. In current deep submicron technologies, the effect of the LDD series resistance on transistor 1/*f* noise performance has been drastically reduced due to the employment of the salicidation scheme for the source, drain and gate contact areas.

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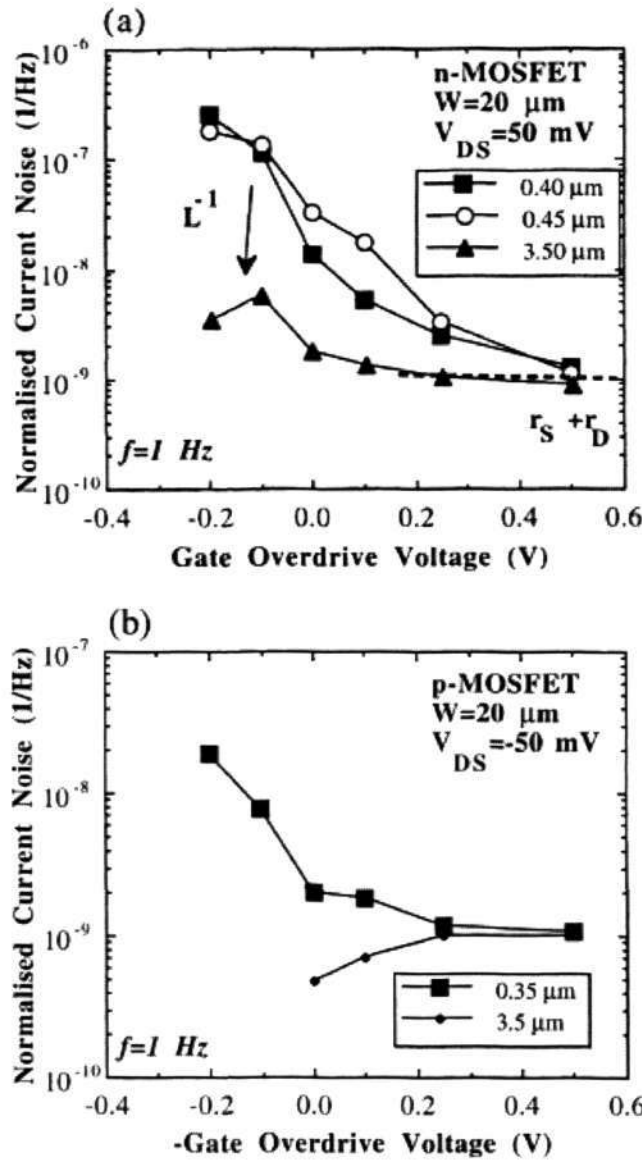

Fig. 2.10: Plot of normalized drain current noise spectral density in the linear region versus the gate overdrive voltage for (a) n-MOSFETs and (b) p-MOSFETs with different channel lengths fabricated in a 0.35μm CMOS technology at 1 Hz. Below threshold, the noise power scales approximately with 1/L. At high gate overdrive regions, the noise power reaches a constant level and this is indicative of the existence of series resistance dominated 1/*f* noise [2].

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2.2.3 Impact of BEOL Process Modules on Transistor 1/f Noise Performance

One of the most important BEOL processing effects that have a major impact on the transistor 1/*f* noise performance is that due to plasma charging damage resulting from MOSFETs experiencing antenna effects. The patterning of the metallization in advanced CMOS technologies involves the use of reactive ion etching processes and/or electro-chemical plating technologies. These processes employ reactive plasma ion cloud for the micropatterning step, thereby leading to antenna effects. The severity of the antenna effect is directly correlated to the length of the metal interconnects on top of the oxide. The antenna effect in turn causes plasma-induced gate-oxide damage resulting in transistor threshold voltage, subthreshold swing, input offset voltage and 1/*f* noise performance degradation. The relationship between the MOSFETs with different antenna areas and the degradation of the 1/*f* noise performance is shown in Fig. 2.11 [69].

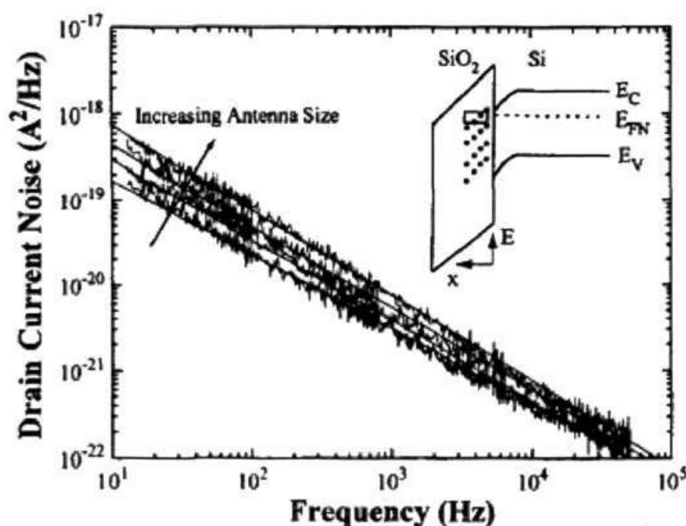

Fig. 2.11: Drain current noise spectra of the plasma-damaged oxide MOSFETs with varying antenna areas, namely 80×80, 160×160, 320×320 and 640×640 μm^2 respectively in ascending order. The devices aspect ratio is W/L = 49.5/0.9, V_{gs}-V_T = 0.35V and V_{ds} = 2.5V. Shown in the insert is a schematic drawing of the x

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and E space accessed by the 1/*f* noise measurements. It can be observed that plasma ashing damage significantly increases the 1/*f* noise mainly in the lower frequency range regime. This damage has been demonstrated to be directly correlated to the antenna area coverage [69].

Other aspects of BEOL processing that can contribute to the degradation of transistor 1/*f* noise include the mechanical stress and electromigration phenomena associated with the metal interconnects, the use of different types of metal barrier layer, and the employment of different materials, for instance TEOS oxide versus HDP oxide, for the passivation scheme. However there is relatively fewer or no research work done to date on these areas.

The advancement in the continuous down scaling of transistor geometries has also led to the reduction of the minimum feature size of the interconnects. For example in a typical foundry-based 0.25μm technology, the minimum width for the first level metal and the subsequent levels above that are 0.32μm and 0.36μm. Scaling to the 0.13μm technology, the minimum width for the first level metal and the subsequent levels above have been reduced to 0.16μm and 0.20μm respectively. The main concerns with the interconnect scaling are electromigration failures and mechanical stress induced voids affecting the reliability of very large-scale integration (VLSI) circuitries with small feature sizes. This in turn has led to the requirement of a sensitive, quick turnaround time and non-destructive wafer-level reliability testing method. Research studies [70-73] have shown that the 1/*f* noise measurement is a sensitive and reliable method to analyze electromigration parameters of thin film interconnects. As compared to the conventional mean-time-to-failure (MTF) method, this technique requires less time and is non-destructive in nature. Fig. 2.12 shows the correlation the normalized change in the

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resistance of the thin film Al interconnect and the 1/*f* noise of the interconnect versus the stress time.

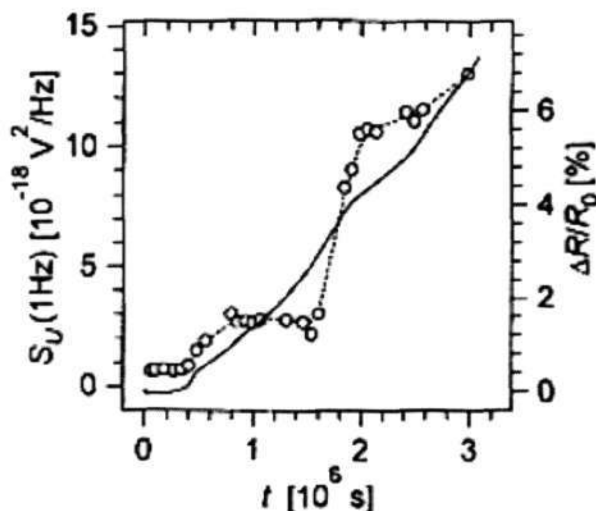

Fig. 2.12: Comparison of the normalized resistance change ($\Delta R/R_0$ – solid line) and the 1/*f* noise spectral density at 1 Hz (open symbols with dotted line) of an Al (1% Si, 0.5% Cu) interconnect under electromigration test (current density 2×10^6 A cm^{-2} and T = 303 K) [73].

It can be observed that there is a strong correlation between the change in the film resistance, symbolizing the extent of the electromigration phenomenon, and the measured 1/*f* noise data. Researchers attribute the 1/*f* noise spectra of thin film interconnects of CMOS transistors to the grain boundary movements and/or the vacancy creation and the subsequent rate of fluctuations of the vacancy diffusion around the grain boundaries [74]. This 1/*f* noise contribution from the interconnect film due to the electromigration and mechanical stress induced voids phenomena will subsequently add on to the main noise contribution from the Si-SiO_2 interface of the transistor.

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2.2.4 Impact of SOI and FinFET Technologies on Transistor 1/f Noise Performance

An overview of the 1/*f* noise characteristics in both partially- and fully-depleted silicon-on-insulator (SOI) CMOS technologies has been reported recently by Jomaah et al. [75], [76]. For the floating-body (FB) partially-depleted (PD) devices, a kink-related excess noise has been observed in the saturation region. This is due to the floating body effect inducing a Lorentzian-like noise component that superimposes onto the conventional 1/*f* noise spectrum. The Lorentzian spectrum is characterized by a corner frequency f_c and a plateau noise level, both of which are dependent on the drain bias. Several mechanisms have been proposed to explain this excess noise, which includes trap assisted generation-recombination noise [77] or shot noise amplified by the floating body effect [78]. However the kink-related excess noise disappears when the SOI transistor's body is contacted to ground (BC). The above-mentioned phenomena are illustrated in Figs. 2.13(a) and 2.13(b).

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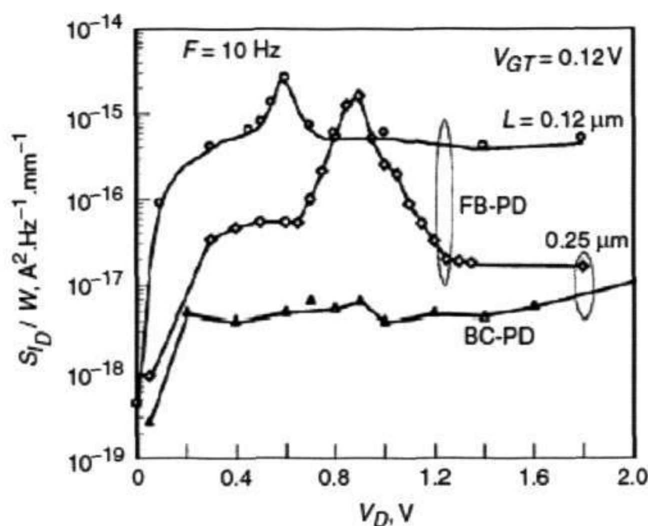

Fig. 2.13(a): Drain current power spectral density normalized by the width W, for FB-PD devices with two gate lengths (L=0.25µm and 0.12µm) and for BC-PD devices with L=0.25µm versus the drain voltage at f=10Hz [76].

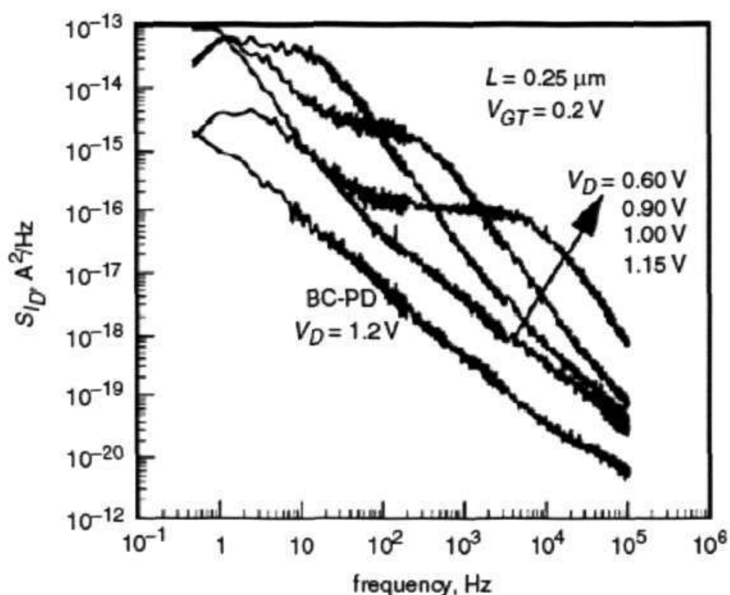

Fig. 2.13(b): Drain current power spectral density versus frequency for 0.25µm FB and BC partially depleted devices at different drain voltages [76].

Fully depleted (FD) SOI devices exhibit floating body effects only when the back interface is biased in the accumulation mode [79]. Fully depleted MOSFETs are in theory

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dual-gate devices, the inversion channel can be controlled by both the front and back gate voltages. Since the buried oxide on a standard SOI wafer is usually much thicker than the front gate oxide, hence to obtain a symmetric behaviour, the back gate voltage must be much larger than the front gate voltage. This coupling between the front and back gate leads to increased $1/f$ noise levels as the noise generated from traps at the back interface then couples out to the output and adds to the drain current noise generated from the front gate [75].

For the PD devices, interface state density values of $2\text{–}7\times10^{17}$ cm^{-3} eV^{-1} have been calculated. For the FD devices, for transistors with a channel length of 1 and 0.12μm, the extracted oxide trap density values are in the range of 10^{18} cm^{-3} eV^{-1} [75]. These large values have been attributed to the influence of the back interface. In general the $1/f$ noise characteristics of the PD and FD devices correlates well with the carrier number fluctuation with correlated mobility fluctuation model [76].

Lee et al. [80] reported the $1/f$ noise characterization of a FD double-gated p-channel FinFET. The researchers found that the noise spectra follows a $1/f$ dependence and can be described by the carrier number fluctuation with correlated mobility fluctuation model. The extracted oxide trap density for the p-FinFET with poly-Si-gate is approximately 1.5×10^{17} cm^{-3} eV^{-1}. This value is comparable to the oxide trap densities of bulk-Si thin gate oxide p-MOSFETs illustrated in chapter 5, table 5.2 on page 85 of the revised thesis.

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CHAPTER 3
1/f NOISE MEASUREMENT SYSTEM AND SETUP

3.1 1/f Noise Measurement System and Setup

On-wafer $1/f$ noise measurements have been performed using Cadence 9812B noise analyzer system connected to a HP35670A dynamic spectrum analyzer in an electromagnetic and light shielded CASCADE™ probe station. The schematic diagram of the Cadence $1/f$ noise measurement system is shown in Fig. 3.1 [81]. The system consists of a controller unit and an amplifiers/filters unit joint together via connectors A and B. The terminals of the device under test (DUT) are connected to the BNC receptacles located on the front panel of the amplifiers/filters unit using coaxial cables. The two-piece design of the noise system allows the noise amplifiers to be placed close to the DUT and away from any other noisy equipment in the laboratory. By placing the noise amplifiers in close proximity to the DUT, only short length of coaxial cables need to be used thereby minimizing stray ambience noise pickup. The amplifiers unit consists of the voltage and current preamplifiers. The selection of the appropriate amplifier depends on the output impedance of the DUT and this discussion will be covered in section 3.1.2. The user has a choice to choose either type of amplifier via the 'Noise Analyzer' setup window of the controller software, NoisePro™. The amplifiers unit is constructed with discrete components and is powered by rechargeable batteries.

The hardware system is controlled by Cadence NoisePro™ software residing on a Windows™ PC. The computer running NoisePro™ controls the measurement instruments, I-V and $1/f$ noise measurements via the IEEE-488 (GPIB) bus. Besides controlling the I-V

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and 1/*f* noise measurements, NoisePro™ also allows the user to perform data analysis, 1/*f* noise compact model parameter extraction and simulation.

HP4156C parametric analyzer has been used to provide the biasing voltages at the device's gate, source, drain and bulk terminals, as well as to provide a constant current source at the device's drain terminal for several experiments in chapters 5, 6 and 7. Static parameter measurements, namely V_{gs}, V_{ds}, I_{ds}, transconductance g_m and output conductance g_{ds}, have been performed prior to the 1/*f* noise measurements.

The current noise at the drain (S_{Id}) is fed to a low-noise voltage or current amplifier, and the amplified signal is then output to the HP35670A dynamic signal analyzer. Agilent's HP35670A dynamic signal analyzer has a spurious free dynamic range of typically 90 dB and a maximum real-time bandwidth of 25.6 kHz in a 1 channel mode [82]. The background noise level has been corrected for by performing 1/*f* noise measurements at a low drain bias of 500μV. For subsequent measurements, this background noise level will be subtracted away from the measured data of the DUT. Drain current noise spectra have been measured within the frequency range of 1Hz to 1KHz. This frequency range has been chosen to reflect the region where 1/*f* noise of CMOS devices is most dominant. An average of 100 spectra has been taken for each biasing condition via NoisePro™. These spectra are subsequently averaged by NoisePro™ to produce a single spectrum for each biasing condition. All the measurements have been carried out at room temperature.

In wafer-level 1/*f* noise testing, contact probes are used to make electrical connections between the test sample and the measurement system via contact pads. Further to that, metal interconnects are used to connect the device under test to the contact pads. Beryllium-copper (Be-Cu) probes from CASCADE™ have been employed in the 1/*f* noise

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measurements, as it is well known that Be-Cu probes exhibit the lowest contact resistance. These probes typically have a contact resistance of approximately 0.4Ω. This corresponds to the measured voltage noise spectral density, S_{Vc} at 10Hz of the order of 10^{-18} V^2/Hz. This order is far smaller than the typical input-referred gate voltage noise spectral density, S_{Vg} of CMOS transistors, which ranges from 10^{-13} to 10^{-11} V^2/Hz. In order to minimize 1/*f* noise contributions by the metal interconnects, the terminals of the device under test are connected to the contact pads using metal traces with wide line-widths (typically about 4 to 6 μm wide). This design, coupled with the fact that the highest current density seen by the transistors with the strongest current drive is in the order of 10^5 A/cm^2, it has been found that voltage noise spectral density, S_{Vi} at 10Hz is less than 10^{-17} V^2/Hz.

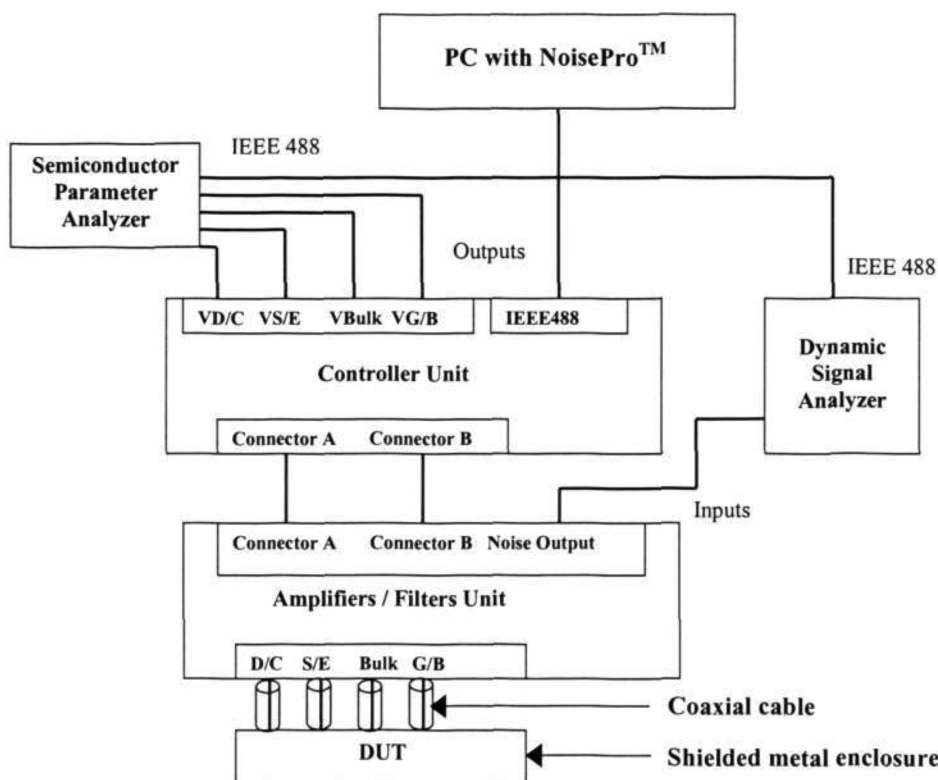

Fig. 3.1: Cadence 9812B 1/*f* noise measurement system with built-in noise amplifiers [81].

3.1.1 BTA 9812B 1/f Noise System Measurement Modes

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The BTA 9812B 1/*f* noise system has two measurement modes: (a) Measure I-V mode and (b) Measure Noise mode.

Fig. 3.2 shows the connections between the semiconductor parametric analyzer, the noise system and the DUT when operated in the Measure I-V mode. The source monitor unit (SMU) bias inputs (VD/C, VG/B, Vbulk, and VS/E) are directly connected to the DUT terminals (Drain/Collector, Gate/Base, Bulk, and Source/Emitter). Thereafter the I-V characteristics of the DUT will be captured.

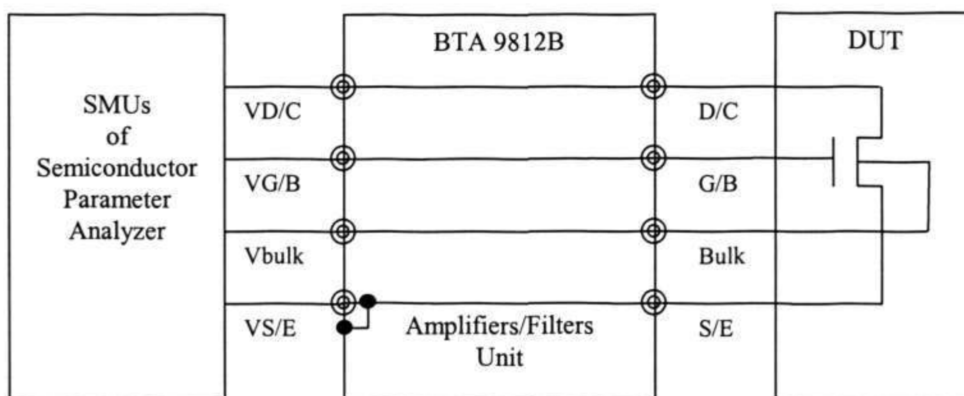

Fig. 3.2: Measure I-V mode configuration for BTA9812B [83].

Fig. 3.3 shows the connections between the semiconductor parametric analyzer, the noise system, the dynamic signal analyzer and the DUT when operated in the Measure Noise mode. Three RC filters have been employed to reduce the residual noise in the bias voltages generated by the SMUs before the voltages are applied to the DUT. The user can change the time constant or cut-off frequency of the filters by changing the value of resistor in each filter. The general guideline is that the time constant should be chosen according to the estimated magnitude and frequency range of the noise to be measured. The user needs to tradeoff between the long filter time-constant, which would result in

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more accurate noise measurement, and the long filter response time. Upon changes made to the DUT bias voltage, it is essential to provide sufficient settling time for the voltage at the filter output before conducting further I-V or noise measurement. The settling time is about several times of the filter time constant. Due to the employment of high quality non-electrolytic capacitors, the filter's leakage current is almost zero, measured upon settling down of the charging current.

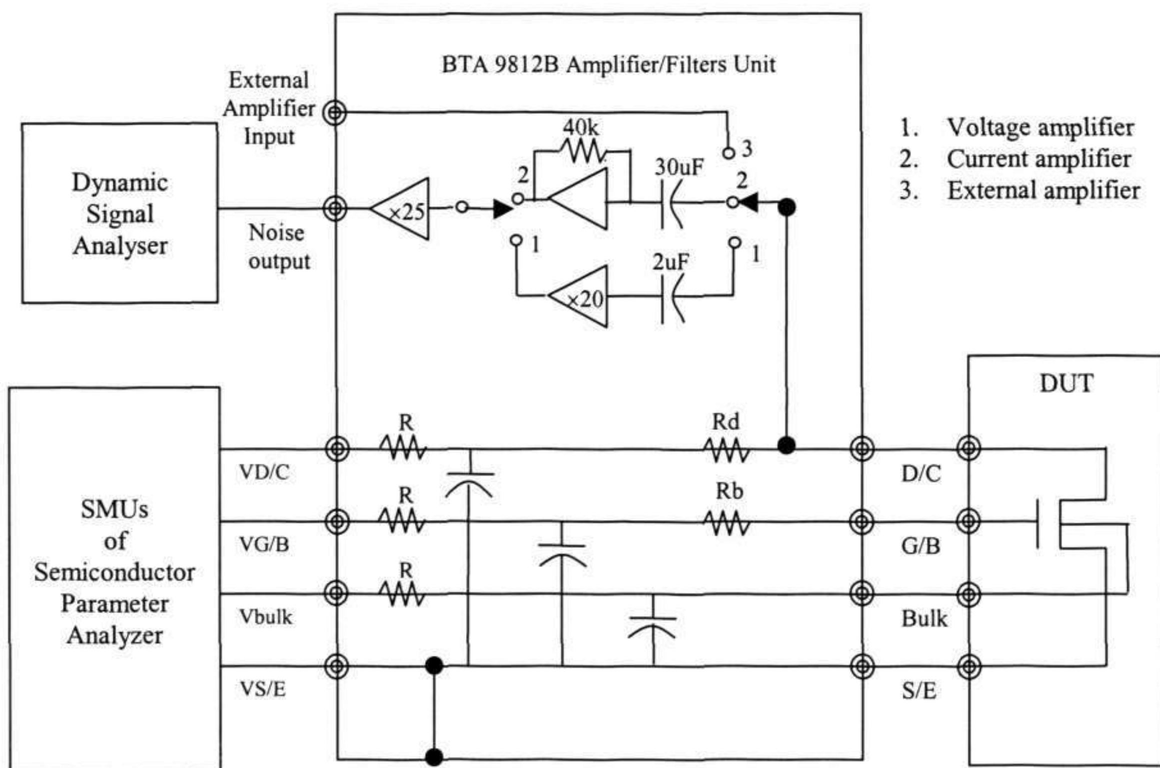

Fig. 3.3: Measure Noise mode configuration for BTA9812B [83].

3.1.2 Criteria for Selection of Noise Pre-Amplifier

As mentioned earlier in section 3.1, there are two types of built-in noise pre-amplifiers included in BTA9812B. The built-in current amplifier has a feedback resistor (R_f) of

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40Kohm and an input coupling capacitor of 30μF. The coupling capacitor will attenuate the gain of the current amplifier at very low frequency, and the amount of attenuation will depend on the g_{ds} of the DUT. The floor noise for the current amplifier is 0.5pA/√Hz [84].

On the other hand, the voltage amplifier consists of an input coupling capacitor of 2μF. Due to the high input impedance of the voltage amplifier (more than 1Mohm), the input capacitor has minimal effect on the frequency response of the amplifier for most practical frequency ranges. The voltage amplifier has a voltage gain of 20 and a noise floor of 1.4nV/√Hz. Both amplifiers have a working bandwidth of 0.5Hz-1MHz [84].

The selection of the appropriate pre-amplifier depends on the nature of the output impedance of the DUT. A voltage amplifier is best used for the measurement of DUTs with relatively low output impedance R_{out} ($1/g_{ds}$) such as MOSFETs, while a current amplifier is most suitable for measuring DUTs with relatively high output impedance such as BJTs. Another advantage of using a voltage pre-amplifier is its insensitivity to chuck noise when doing wafer level measurement. For this research work, which focuses on deep submicron MOSFETs, the voltage pre-amplifier has been chosen for the $1/f$ noise measurements.

3.1.3 Criteria for Selection of Output Load Resistor

To measure the $1/f$ noise of MOSFETs, an internal load resistor needs to be connected at the 'output' terminal of the DUT. This is illustrated in Fig. 3.3 by resistor Rd. The purpose of this load resistor is to prevent the low output resistance of the bias voltage from shunting the DUT noise current to ground. The value of this load resistor will have an impact on the lowest noise level measurable, the DUT dc operation point settling time

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and the measurement bandwidth of the system. Fig. 3.3 shows that there is an internal resistor Rb connected to the 'input' terminal of the DUT. For MOSFETs, Rb should be set to zero, whereas a suitable value should be chosen for low input impedance DUT such as the BJT.

Fig. 3.4 shows a simplified schematic of the BTA9812B dc biasing and filter circuitries, as compared to the detailed drawing illustrated previously in Fig. 3.3.

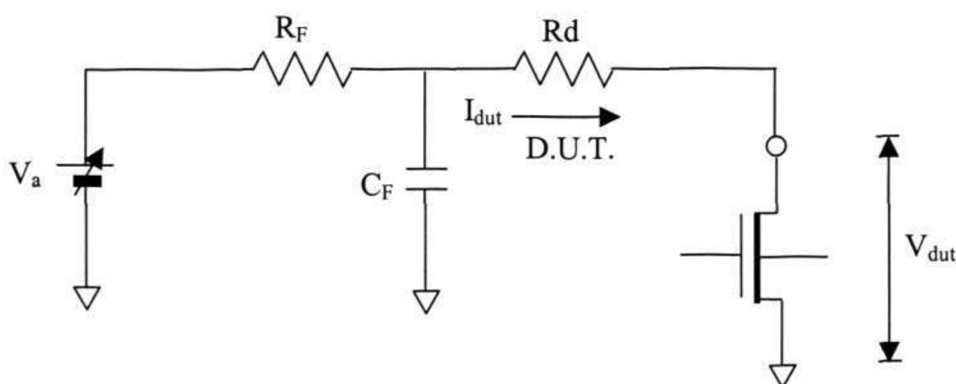

Fig. 3.4: Simplified schematic of the dc biasing and filter circuitries for BTA9812B [84].

With the assumption that the leakage current of the filter capacitor C_F is negligible, the DUT bias voltage (V_{dut}) can be written as:

$$V_{dut} = V_a - I_{dut}\left(R_F + Rd\right) \tag{3.1}$$

NoisePro™ offers a choice of selecting Rd based on (a) a fixed user-input value, (b) the static R_{out} and (c) the dynamic R_{out}. For option (a), the user can set Rd to one of the following value: 100, 333, 1K, 3.3K, 10 K, 100 K, or 1Mohms. The optimal value of Rd is chosen according to the type of noise amplifier being used and the biasing conditions of the DUT. As a general rule of thumb, if the voltage amplifier is used, then a lower value of Rd is recommended to ensure that the voltage noise contributed by Rd will not be excessive. On the other hand when the current amplifier is employed, the largest possible

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value of Rd allowable by the maximum bias voltage should be chosen. In doing so, the noise current contributed by Rd can be minimized. The selection of Rd based on option (b) will select the largest possible Rd value, which satisfy the following condition: $I_{dut}(R_F + Rd) \leq V_{\max} - V_{ds}$. V_{max} denotes the minimum of the maximum output voltage of the power supply and 100V. For the case of selecting Rd based on option (c), NoisePro™ will automatically calculate and select the appropriate resistor value based on the bias condition and R_{out} of the DUT. Rd is decided based on Rd >> R_{out} in the case of the current amplifier and Rd << R_{out} in the case of the voltage amplifier. For most noise measurements, unless the high voltage drop crossing the filtering and loading resistors is a concern, choosing Rd based on static R_{out} will generally give the best results. This option has been employed in this research work.

3.2 Best Practices for Reliable 1/f Noise Measurements

Listed below are the best practises adopted during the 1/f noise measurements:

1. The automatic movement feature of the semi-automatic probe station is disabled during 1/*f* noise measurements. This will subsequently power down the relevant controllers within the probe station, thereby minimizing noise interference.
2. The chassis of the controller unit is connected to the ground of the AC supply, whereas the chassis of the amplifiers/filters unit has been hardwired to the VS/E input. This arrangement is intended to eliminate any potential ground loops from forming.
3. The power cords of all the equipment in the system are connected to the same power outlet to minimize noise interference through the AC ground loop.

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4. The amplifiers/filters unit is positioned as close to the DUT as possible so as to minimize the length of coaxial cables used, thereby reducing stray noise pickup.
5. All cables of the measurement system are kept away from potential noise generators, such as computer monitors, monitors of test equipment, test equipment with rotating motors etc.
6. Upon completion of $1/f$ noise measurements for more than 24 hours, the system is left in the idle mode with the power supply switched on. This will subsequently charged the batteries for use in the next measurement cycle.
7. After switching on the bias voltages, some settling time, typically about 5-10 minutes, is required for the amplifier output voltage and the DUT current to become stable. When the measured noise spectrum appears abnormal, it is usually due to oscillation, i.e. the measurements have begun before the amplifier's output or the DUT current has completely settled down.
8. The $1/f$ noise measurements typically spans across several orders of frequencies. In order to increase the frequency resolution during the measurements, the entire frequency range is broken down into multiple smaller frequency bands. The selection of the frequency bands is done through the 'Spectrum Analyzer' setup in NoisePro™. The user needs to tradeoff the higher frequency resolution with the measurement time required. Typically for measurements of frequency range above 50Hz, selecting a frequency band of 0 to 200Hz is recommended [85]. This frequency band has been adopted in this research work.
9. The averaging number setup in the "Spectrum Analyzer' window of NoisePro™ allows the user to use different average numbers for different measurements. In this research work, the averaging number used is 100.

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CHAPTER 4

IMPACT OF 0.25μm DUAL GATE OXIDE THICKNESS CMOS PROCESS ON 1/f NOISE PERFORMANCE OF MULTI-FINGERED DEEP SUBMICRON MOS TRANSISTORS

4.1 Introduction

To enable System-on-Chip (SoC) design to be implemented in CMOS technology, it is necessary to provide multiple supply voltages on the same wafer. This requires the ability to grow multiple gate oxide thicknesses simultaneously. Dual thickness gate oxide technology offers the nominal supply voltage thin gate oxide MOSFETs for high-speed applications, and the higher supply voltage thick gate oxide MOSFETs for circuits requiring a large signal swing such as the I/O stages and the high gain amplifiers. This arrangement offers definitive advantages for SoC design integrating radio-frequency (RF), analog and digital circuitries together.

Worldwide foundries have begun offering the dual thickness gate oxide process (henceforth called the dual gate oxide or DG process) starting from the 0.25μm technology and below. This work focus on the 0.25μm DG technology, which features the 2.5V, 4.3nm thin gate oxide devices that have been developed for the core chip area and the 3.3V, 6.2nm thick gate oxide devices that have been developed for the I/O area. However due to the additional processing steps required to incorporate the two different gate oxide thicknesses together, the $1/f$ noise performance of devices fabricated using the DG process needs to be investigated. This motivates the author to study and compare the $1/f$ noise performance of 0.25μm multi-fingered devices fabricated using both the DG

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process and the standard thickness gate oxide process (henceforth called the single gate oxide or SG process) in this chapter.

Section 4.2 of this chapter compares the flow between the SG and the DG processes, highlighting the main differences between them. It also provides a brief description of the test structure used and the measurement setup employed. Section 4.3 compares the 1/*f* noise characteristics between the SG and DG MOSFETs. The comparison further involves the generation of HSPICE level-3 1/*f* noise models to accurately simulate the 1/*f* noise characteristics of these devices. Thereafter, the author will proceed to identify the dominant noise mechanism at the different biasing condition for each transistor type using several analytical techniques. Lastly, section 4.4 summarizes this chapter.

4.2 Device Fabrication, Test Structure Description and Measurement Setup

Fig. 4.1 shows a block diagram of a portion of Chartered Semiconductor's 0.25μm CMOS baseline SG process flow and the necessary plug-in modules to achieve the DG process flow. The SG process flow starts with the shallow trench isolation (STI) scheme; 10nm sacrificial oxide growth; followed by well and channel dopants implantation; sacrificial oxide removal; 4.3nm oxynitride (N_2O) gate oxide growth; polysilicon gate patterning; lightly-doped drain (LDD) implantation; nitride spacers formation; source and drain regions implantation; silicidation; contact formation; metallization and finally passivation.

For the DG process, prior to the 4.3nm oxynitride (N_2O) gate oxide growth, a 5.0nm thick gate oxide is grown. This gate oxide functions as the gate dielectric for the thick gate transistor area, and acts as a sacrificial oxide layer for the thin gate transistor area. In

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the latter area, this oxide layer is subsequently etched away using an additional mask. Next a hydrofluoric (HF) acid clean is carried out before proceeding back to grow the 4.3nm of oxynitride (N_2O) gate oxide for the thin gate transistor area. Note that the gate oxide on the thick gate transistor area will subsequently be re-grown to a final thickness of 6.2nm. The remaining processing steps for the DG process are similar to that of the SG process.

In retrospect, the thin gate oxide transistor areas of the DG process effectively undergo two cleaning cycles since as mentioned earlier, the gate dielectric of the thick gate area further acts as a sacrificial oxide for the thin gate area. In contrast the thin gate oxide transistor areas of the SG process undergo only one cleaning cycle.

The test structures available for measurements are all minimum channel length multi-fingered devices. Multi-fingered transistor layout ensures sufficient current drive for wireless applications and to facilitate accurate RF measurements using the 50 ohms impedance-based network analyzer. The devices have been layout as an array of polysilicon fingers connected in parallel with shared source/drain diffusion regions. The devices are identified by the number of fingers (N_f), the length of each finger (W_f) and the width of each finger (L). The total width of a device W_{total} is given by $N_f \times W_f$. As all the devices characterized in this work have even number of fingers, there would always be one more source diffusion region than the drain diffusion region for each transistor type.

On-wafer measurements have been performed using Cadence 9812B flicker noise system connected to a HP35670A dynamic spectrum analyzer in a shielded CASCADE™ probe station. A HP4156 parametric analyzer has been used to provide the biasing voltages at the device's source, gate and bulk, and to provide a constant current source at the device's drain. The voltage noise at the drain is fed to a low-noise voltage amplifier

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and the amplified signal is output to the HP35670A dynamic signal analyzer. The background noise level has been corrected for by performing noise measurements at the drain bias of 500μV. For subsequent measurements, this background noise level has been subtracted away from the measured data. More in-depth discussions on the measurement setup and the measurement procedures can be found in Chapter 3.

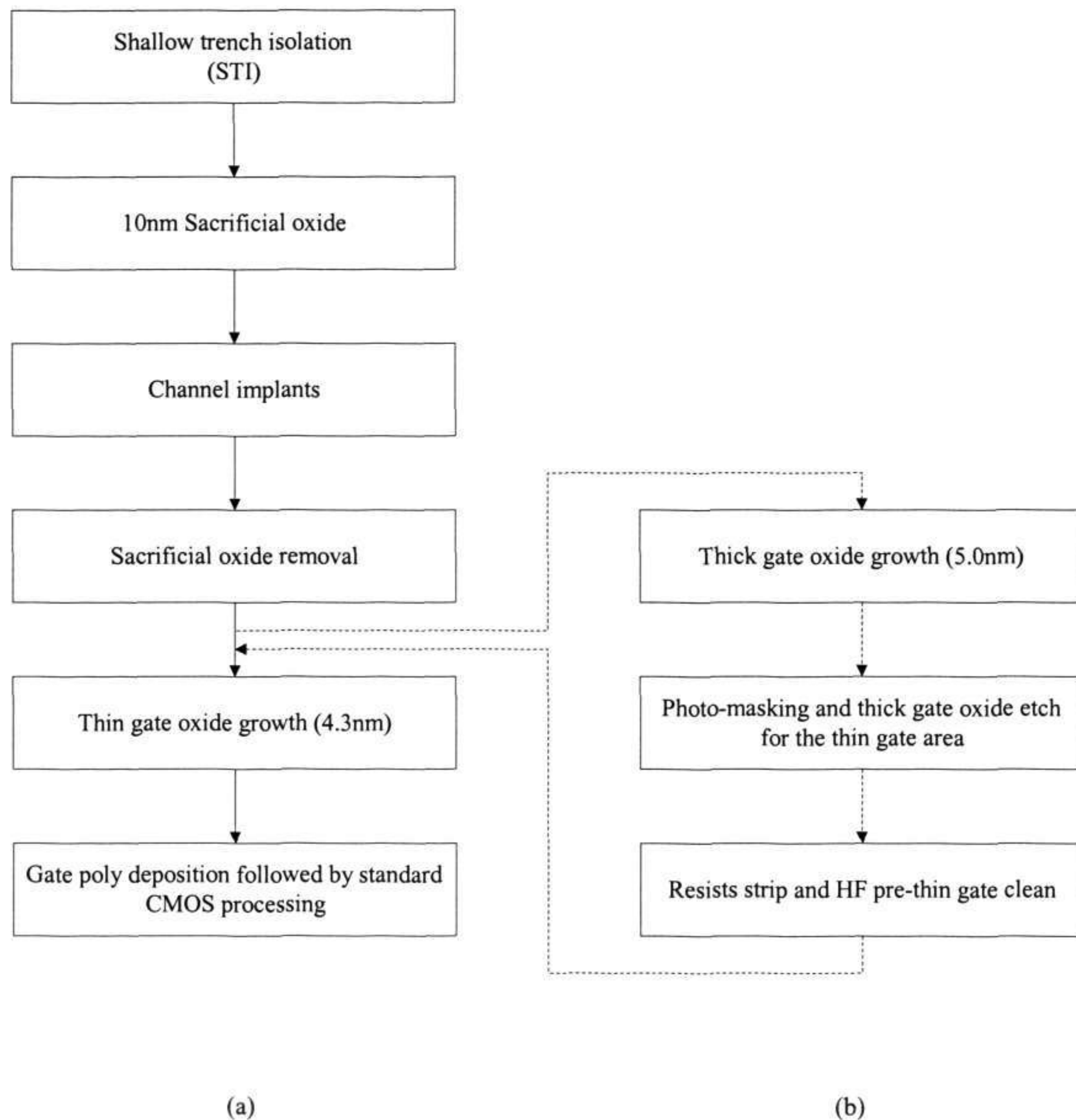

Fig. 4.1: Block diagram highlighting Chartered Semiconductor's 0.25μm (a) baseline analog CMOS single gate oxide (SG) process flow and (b) the plug-in modules required for the dual gate oxide (DG) process flow.

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4.3 Comparison of SG and DG Multi-fingered Transistors' 1/f Noise Characteristics and Identification of Dominant Noise Mechanism

Fig. 4.2 shows the drain current noise spectral density versus varying frequency for SG and DG nMOSFETs and pMOSFETs corresponding to $N_f = 28$, $W_f = 2.38\mu m$ and $L = 0.24\mu m$. The solid lines show the simulation results using the HSPICE level-3 1/*f* noise model, which is given by [86]:

$$S_{Id} = \frac{KFg_m^{\ 2}}{C_{OX}W_{eff}L_{eff}f^{AF}} \tag{4.1}$$

where KF is a technology and bias dependent noise parameter and AF is the frequency exponent that can vary from 0.7 to 1.3 [2]. For an ideal flicker noise spectrum, AF is equal to 1.

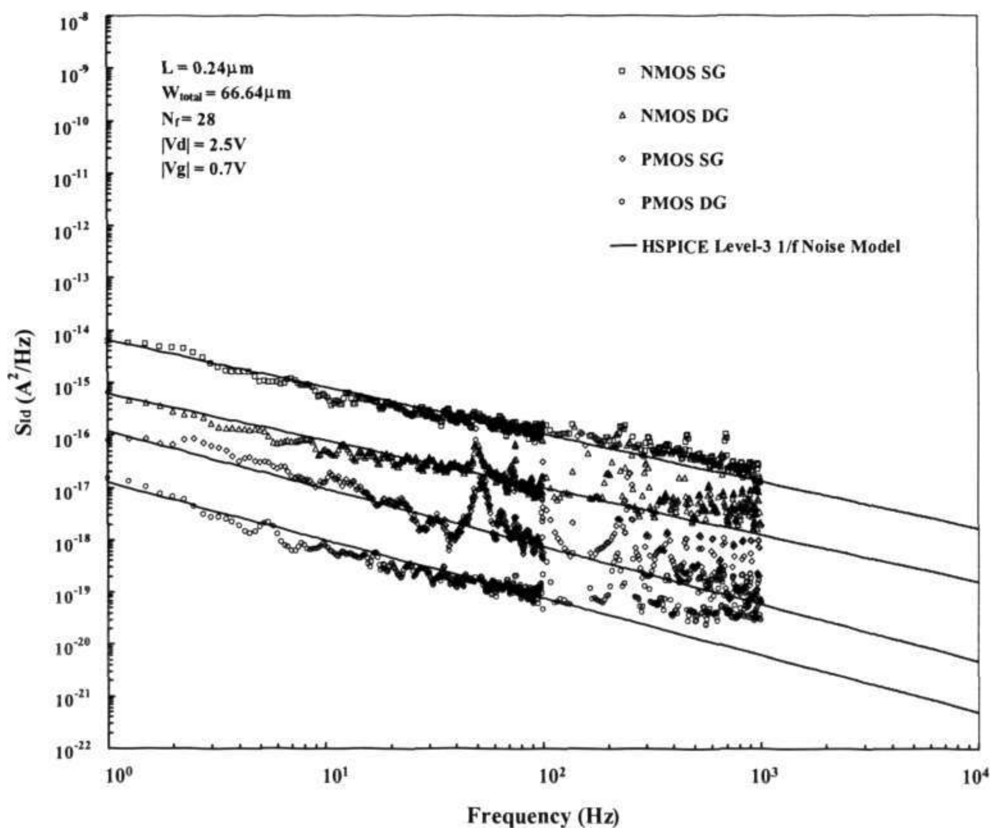

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Fig. 4.2: Comparison of drain current noise power spectra for SG and DG NMOSFETs and PMOSFETs with number of fingers, $N_f = 28$, length of each finger, $W_f = 2.38\mu m$ and width of each finger, $L = 0.24\mu m$. Solid lines represent the fitting by the HSPICE level-3 $1/f$ noise model.

An important observation from Fig. 4.2 is that in the saturation regime with weak inversion, the NMOSFETs are noisier than the PMOSFETs. Intuitively electrons have higher mobilities than holes. Invoking Hooge's $1/f$ noise model for MOSFETs, the normalized drain current spectral density is given by [50]:

$$\frac{S_{Id}}{I_d^{\,2}} = \frac{q\alpha_H}{fWLQ_N} \tag{4.2}$$

and the input-referred gate voltage noise spectral density can be written as [2]:

$$S_{Vg} = \frac{q\alpha_H (V_g - V_T)}{C_{OX}WLf} \tag{4.3}$$

where the Hooge's parameter is specified as [87]:

$$\alpha_H = \alpha_{latt}\left(\frac{\mu_{eff}}{\mu_{latt}}\right)^2 \tag{4.4}$$

From equations (4.2) to (4.4), it can be seen that that a higher effective mobility would lead to a higher value of the Hooge's parameter, and hence more pronounced $1/f$ noise spectra.

Another important observation from Fig. 4.2 is that regardless of whether it is an nMOSFET or a pMOSFET, the DG devices always have lower $1/f$ noise levels than the SG devices. To further substantiate this observation, a total of 20 devices, corresponding to five different device configurations and four different device types have been characterized and modelled. The most effective method of making comparison among the 20 devices to support the above observation and yet not confused the reader with "over-

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cluttered" plots is to compare the HSPICE level-3 $1/f$ noise model KF and AF parameters for the 20 different multi-fingered SG and DG devices as illustrated in Table 4.1. It can be clearly seen that all DG devices have lower KF values as compared to SG devices. The AF values for both SG and DG devices are similar for each transistor type. This is understandable, as the slope for SG and DG devices of a particular transistor type should remain close to the ideality factor of 1.

Table 4.1: Comparison of the HSPICE level-3 flicker noise model KF and AF noise coefficients for 5 NMOS SG transistors, 5 NMOS DG transistors, 5 PMOS SG transistors and 5 PMOS DG transistors for the different dimensions specified.

$N_f \times W_f \times L$ Dimensions (μm^2)	Type of MOSFET	KF (V^2F)	AF
8×9.58×0.24	NMOS SG	1.5×10^{-24}	0.9
8×9.58×0.24	NMOS DG	5.5×10^{-25}	0.9
8×9.58×0.24	PMOS SG	1.3×10^{-24}	1.2
8×9.58×0.24	PMOS DG	4.9×10^{-25}	1.2
12×4.78×0.24	NMOS SG	7.5×10^{-24}	1.1
12×4.78×0.24	NMOS DG	1.8×10^{-24}	1.1
12×4.78×0.24	PMOS SG	5.0×10^{-24}	1.1
12×4.78×0.24	PMOS DG	7.0×10^{-25}	1.1
28×2.38×0.24	NMOS SG	4.8×10^{-24}	0.9
28×2.38×0.24	NMOS DG	7.5×10^{-25}	0.9
28×2.38×0.24	PMOS SG	1.5×10^{-24}	1.1
28×2.38×0.24	PMOS DG	3.6×10^{-25}	1.1
56×1.18×0.24	NMOS SG	6.0×10^{-24}	1.1
56×1.18×0.24	NMOS DG	1.2×10^{-24}	1.1
56×1.18×0.24	PMOS SG	3.5×10^{-24}	1.1
56×1.18×0.24	PMOS DG	6.0×10^{-25}	1.1
116×0.58×0.24	NMOS SG	9.8×10^{-25}	1.0
116×0.58×0.24	NMOS DG	3.5×10^{-25}	1.0
116×0.58×0.24	PMOS SG	3.8×10^{-25}	1.1
116×0.58×0.24	PMOS DG	1.5×10^{-25}	1.1

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Fig. 4.3 shows a comparison of the extracted Hooge's parameter for each transistor type. Reference data taken from the literature [34], [66] has also been included for comparison. It can be observed that the extracted Hooge's parameter values are at least 1 order lower than those reported from the literature at |Vg|=1.5V, thus reflecting the state-of–the-art processes employed. Furthermore the Hooge's parameter values for the DG transistors are consistently lower than those for the SG transistors. This reinforce the observation from Fig. 4.2 that the DG process results in thin gate oxide transistors with better 1/*f* noise performance than their counterparts from the SG process. This is consistent with the earlier description that the thin gate oxide transistors from the DG process experience an additional cleaning cycle as compared to the thin gate oxide transistors from the SG process. To further support this observation, conventional base-level charge-pumping measurements have been carried out and the results for a NMOSFET are shown in Fig. 4.4. It can be seen that indeed the charge-pumping current level for the DG transistor is lower than that of the SG transistor. To locate the root cause of this decrease in the charge-pumping current level for the DG transistor, secondary ion mass spectroscopy (SIMS) analysis has been performed on both the SG and DG transistors. The results are illustrated in Fig. 4.5. It can be concluded that the 1/*f* noise improvement is mostly likely caused by the lowering of the peak nitrogen concentration at the interface between the gate insulator and the silicon for the DG transistors. It has been reported in the literature that a higher peak nitrogen concentration at the Si/SiO_2 interface correlates to higher interface state density, hence resulting in enhanced 1/*f* noise levels [5]. However gate nitridation is not the only cause of higher 1/*f* noise levels for the SG transistors. Another possible cause would be Si-O bond length and angle distortions due to lattice mismatch of the Si-SiO_2 structure leading to more interface states formation.

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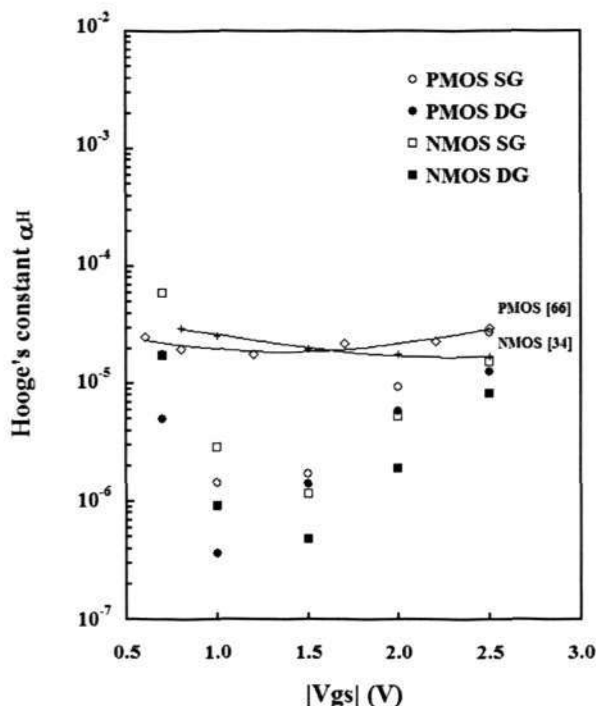

Fig. 4.3: Comparison of extracted Hooge's parameter values for SG and DG NMOSFETs and PMOSFETs with published data [34], [66]. Published data is denoted by symbols with solid lines.

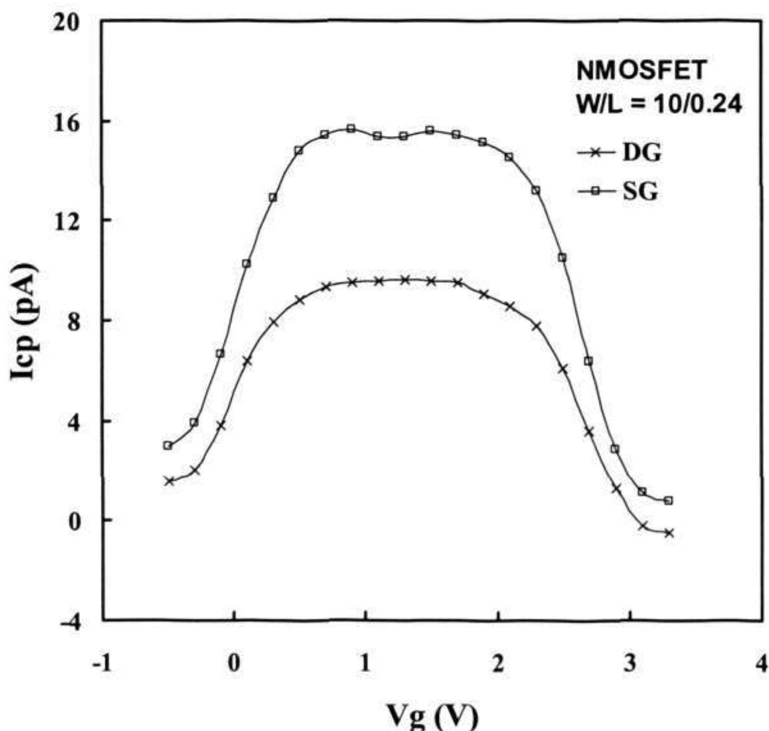

Fig. 4.4: Verification of observed 1/*f* noise improvement using the base-level charge-pumping technique. A trapezoidal gate pulse with a period of 5μsec, rise/fall gradient of 50ns/V and a pulse height of 3V has been used. The start base voltage is –3.5V and the stop base voltage is 0.5V in steps of 0.2V.

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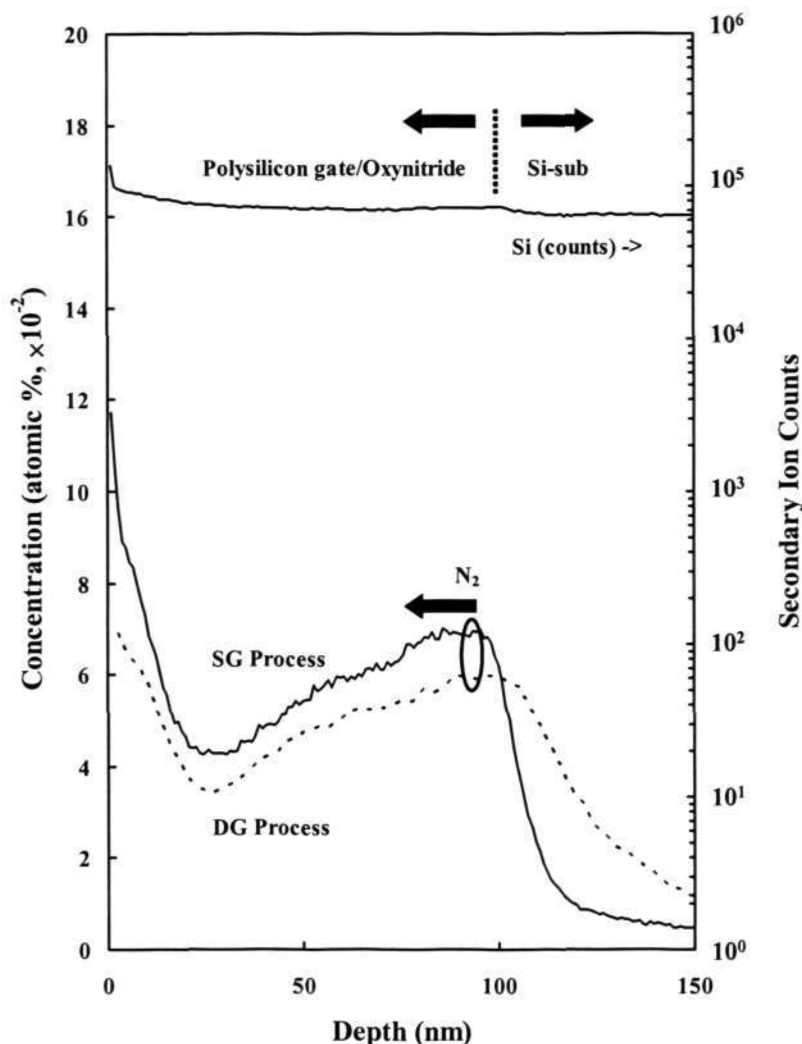

Fig. 4.5: Comparison of SIMS analysis performed using polysilicon-oxide-silicon capacitor structure, with an area of 47,7378 μm^2, for both the SG and DG processes.

Fig. 4.6 shows the DG and SG NMOSFETs' S_{Vg} versus the gate overdrive voltage. For V_{ds}=1.0V, a quadratic increase of S_{Vg} with the gate overdrive in strong inversion is observed for both the SG and DG transistors, while there is a slight rise of S_{Vg} in the weak inversion region. This trend suggests that carrier number with correlated mobility fluctuation dominates. The carrier number fluctuation model can account for the slight variation of S_{Vg} in the weak inversion region if different types of traps (donors and acceptors) are considered [50]. When V_{ds} is increased to 2.5V, the DG NMOSFET shows

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a relatively constant noise level suggesting that the carrier number fluctuations dominate. For the SG NMOSFET, there is a strong increase of S_{Vg} in the weak inversion region. The mobility fluctuation model can explain this phenomenon. The gate voltage spectral density of the mobility fluctuation model in weak inversion can be written as:

$$S_{Vg} = \frac{S_{Id}}{I_d^{\,2}} \times \frac{I_d^{\,2}}{g_m^{\,2}} = \frac{q\alpha_H}{fWLQ_N} \times \frac{I_d^{\,2}}{g_m^{\,2}} \tag{4.5}$$

Equation (4.5) illustrates that there are two I_d dependencies of S_{Vg}. The first term of equation (4.5) gives a $1/I_d$ (or $1/Q_N$) dependence whereas the second term shows a I_d^2 dependence. In weak inversion ($V_{gs} - V_{th} < 1.0V$) and at $V_{ds} = 2.5V$, the ratio I_d/g_m remains relatively constant and equates to the subthreshold swing [2], [50]. This effectively removes the second dependency, resulting in S_{Vg} being proportional to $1/I_d$ (or $1/Q_N$). Hence the increase of S_{Vg} for the SG NMOSFET biased in weak inversion ($V_{gs} - V_{th} < 1.0V$) and at $V_{ds} = 2.5V$ can be attributed to the $1/I_d$ (or $1/Q_N$) variation of S_{Vg} with V_g.

Figs. 4.7 and 4.8 show the normalized drain current noise, $(g_m/I_d)^2$ and the $1/I_d$ ratios versus the drain current in a log-log plot at Vds=1.0V and 2.5V respectively. Fig. 4.7 shows that the normalized current noise curves for both the SG and DG NMOS transistors at V_{ds}=1.0V do not follow the $(g_m/I_d)^2$ or the $1/I_d$ variations. Fig. 4.8 reveals that at V_{ds}=2.5V, the normalized current noise curves for the DG transistor run approximately parallel to the $(g_m/I_d)^2$ plots, reiterating that the carrier number fluctuation dominates. Furthermore it can be seen in Fig. 4.8 that there is a strong exponential increase ($\sim 1/I_d^2$) of the normalized drain current noise for the SG transistor in weak inversion. This again suggests that mobility fluctuations may be dominant in that region.

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Figs. 4.9, 4.10 and 4.11 show similar plots for the PMOSFETs with identical layout and dimensions. Fig. 4.9 shows that for V_{sd}=1.0V, a stronger quadratic increase of S_{Vg} than the NMOS transistors is observed. Fig. 4.10 shows a significant departure of the normalized current noise from the $(g_m/I_d)^2$ variation at strong inversion for both the SG and DG transistors. This phenomenon can be attributed to the extra correlated mobility fluctuations model [50]. Fig. 4.11 shows a strong exponential increase ($\sim 1/I_d^2$) of the normalized current noise at weak inversion for both the SG and DG transistors suggesting that mobility fluctuations dominate in that region. In general, it has been observed from Figs. 4.6 to 4.11 that the normalized drain current noise levels or the input-referred gate voltage noise levels of SG NMOSFETs and PMOSFETs are higher than their DG counterparts.

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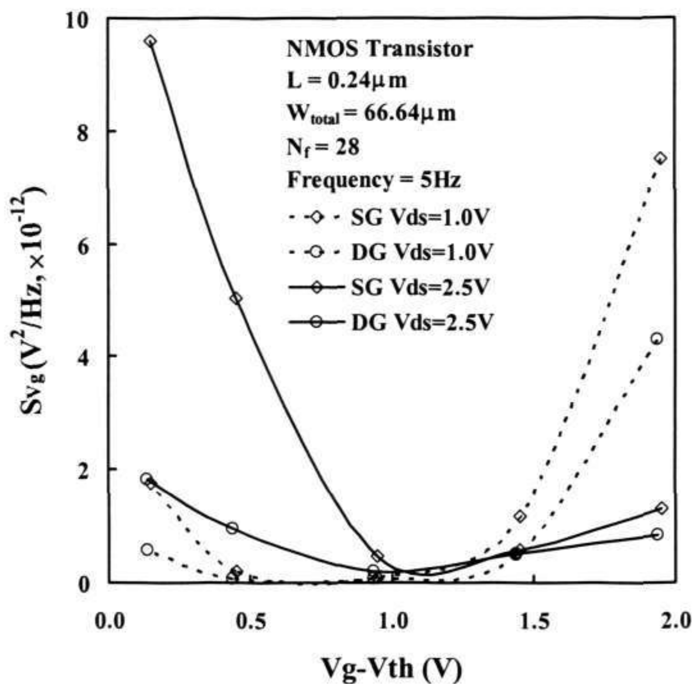

Fig. 4.6: NMOS SG and DG transistors' input-referred gate voltage spectral density versus the gate overdrive voltage at Vds = 1.0V and 2.5V.

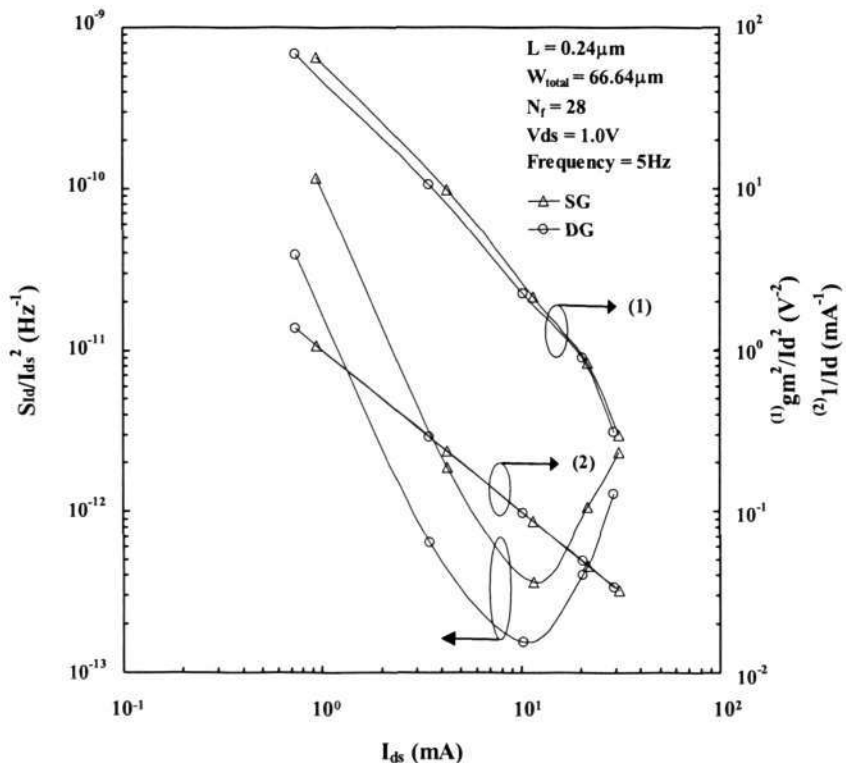

Fig. 4.7: NMOS SG and DG transistors' normalized drain current noise, $(gm/Id)^2$ and 1/Id ratios versus the drain current at Vds = 1.0V.

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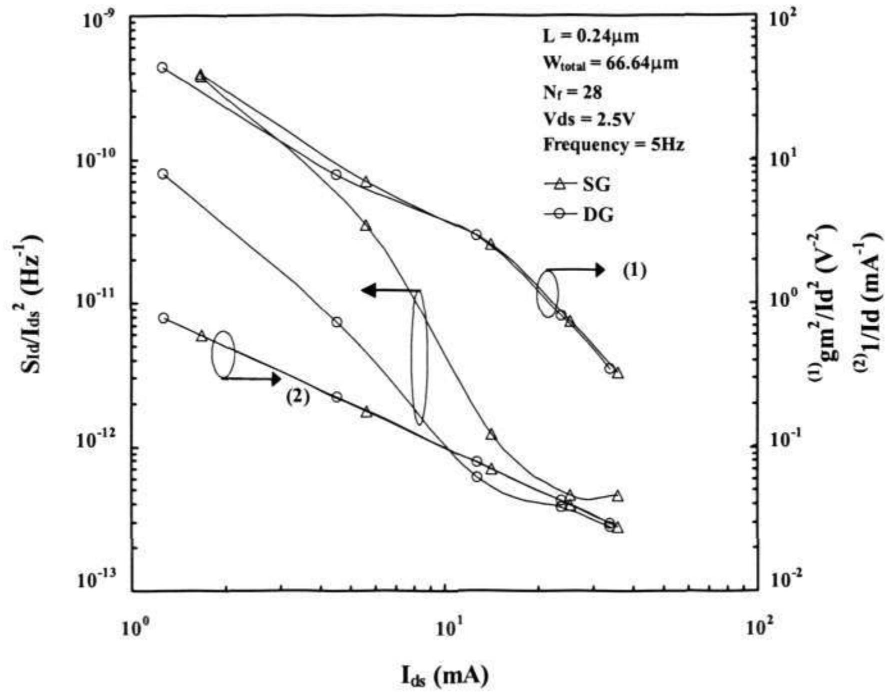

Fig. 4.8: NMOS SG and DG transistors' normalized drain current noise, $(gm/Id)^2$ and 1/Id ratios versus the drain current at Vds = 2.5V.

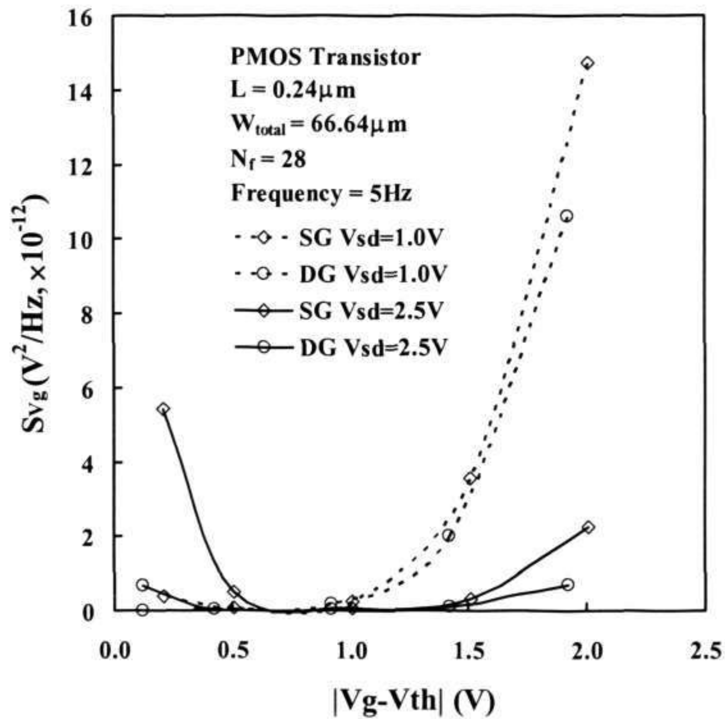

Fig. 4.9: PMOS SG and DG transistors' input-referred gate voltage spectral density versus the gate overdrive voltage at Vsd = 1.0V and 2.5V.

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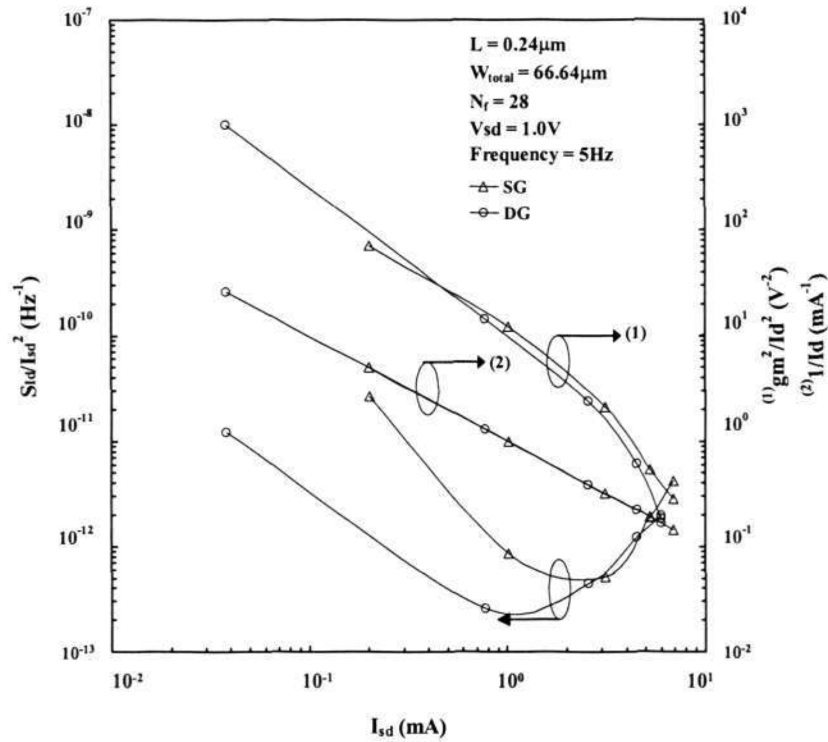

Fig. 4.10: PMOS SG and DG transistors' normalized drain current noise, $(gm/Id)^2$ and 1/Id ratios versus the drain current at Vsd = 1.0V.

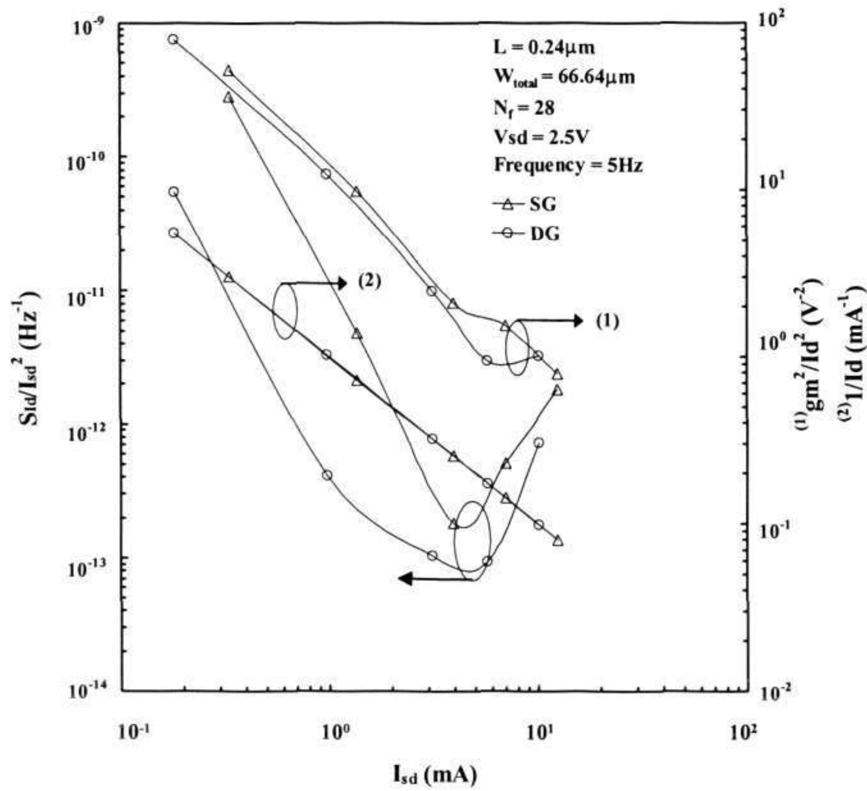

Fig. 4.11: PMOS SG and DG transistors' normalized drain current noise, $(gm/Id)^2$ and 1/Id ratios versus the drain current at Vsd = 2.5V.

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4.4 Conclusion

The author has shown that the dual gate oxide process, which provides both thin and thick gate oxide transistors in a single process technology, produces thin gate oxide transistors with better 1/*f* noise performance than their counterparts from the single gate oxide process. The results show a maximum reduction of approximately an order of magnitude in the current noise spectra. This is mostly likely due to the lowering of the peak nitrogen concentration at the Si/SiO_2 interface causing 1/*f* noise spectra improvement. Dual gate oxide process will therefore be state-of-the-art for the implementation of SoC designs. The author has applied the classical 1/*f* noise theories to explain the experimental findings. The results show that the number with correlated mobility fluctuation model seems to be the most appropriate to describe the low frequency noise behaviour of the investigated MOSFETs.

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CHAPTER 5
EFFECT OF TECHNOLOGY SCALING ON THE 1/f NOISE OF DEEP SUBMICRON PMOS TRANSISTORS

5.1 Introduction

In the previous chapter, we have examined the impact of single thickness versus dual thickness gate oxide processes on the 1/*f* noise performance of NMOS and PMOS transistors. The main conclusion was that using the dual thickness gate oxide process results in a maximum reduction of approximately an order of magnitude in the current noise spectra as compared to the single gate oxide process. This is mostly likely due to the lowering of the peak nitrogen concentration at the Si/SiO_2 interface causing 1/*f* noise spectra improvement. Dual gate oxide process will therefore be state-of-the-art for the implementation of SoC designs. In this chapter, we continue to focus on PMOS transistors fabricated using dual thickness gate oxide processes from four advanced CMOS technologies, and perform a thorough investigation of the effects of technology scaling on the 1/*f* noise characteristics of these transistors. This work examines the composite effect of channel length and gate oxide thickness scaling, coupled with an increasing nitridation dosage, resulting from a consequence of gate dielectric scaling, on the 1/*f* noise of nominal gate length PMOS transistors.

Section 5.2 of this chapter describes the device fabrication process, the measurement setup and the effect of technology scaling on key device parameters. Section 5.3 examines the effects of gate dielectric nitridation on the 1/*f* noise of thin and thick gate oxide PMOS transistors. One of the key highlight of this section is the investigation and comparison of the effect of nitridation on thick gate oxide I/O transistors taken from the advanced

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0.13μm, 0.18μm and 0.25μm technologies, with their architecturally equivalent thin gate oxide counterpart from the more mature 0.35μm technology. The author then attempts to establish the mechanisms responsible for the 1/*f* noise of deep submicron thin gate oxide PMOS transistors. In section 5.4, accurate 1/*f* noise models have been derived to allow circuit designers to evaluate the impact of the 1/*f* noise behaviour of the deep submicron PMOS transistors on their analog/RF circuit performance. Lastly, section 5.5 summarizes this chapter.

5.2 Device Fabrication, Measurement Setup and Process-Related Discussion

P-channel transistors have been fabricated on p-type silicon wafers with a resistivity of 6-9 Ω-cm. The PMOS transistors are surface channel devices with p^+ polysilicon gate. For each technology, both the thin gate oxide transistors (for high speed core circuitries) and the thick gate oxide transistors (for high voltage I/O circuitries) with minimum gate lengths have been characterized. The channel width for all transistors is kept at 20μm.

On-wafer measurements have been performed using Cadence 9812B flicker noise system connected to a HP35670A dynamic spectrum analyzer in a shielded CASCADE™ probe station. DC measurements have been performed prior to flicker noise measurements. S_{Id} spectra have been measured in the 1Hz to 100Hz frequency range. All measurements have been performed at room temperature. Comparisons of 1/*f* noise from the various technologies have been made at a specific drain current value of 5mA. More in-depth discussions on the measurement setup and the measurement procedures can be found in Chapter 3.

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Fig. 5.1 illustrates the key device parameters as a function of technology scaling. It shows that the supply voltage (V_{DD}) and gate dielectric thickness (T_{OX}) scale down linearly with technology. However the threshold voltage (V_{th}) clearly does not scale linearly with technology. It tends towards 300mV at smaller technologies. Table 5.1 highlights the gate oxide growth sequence used for each technology.

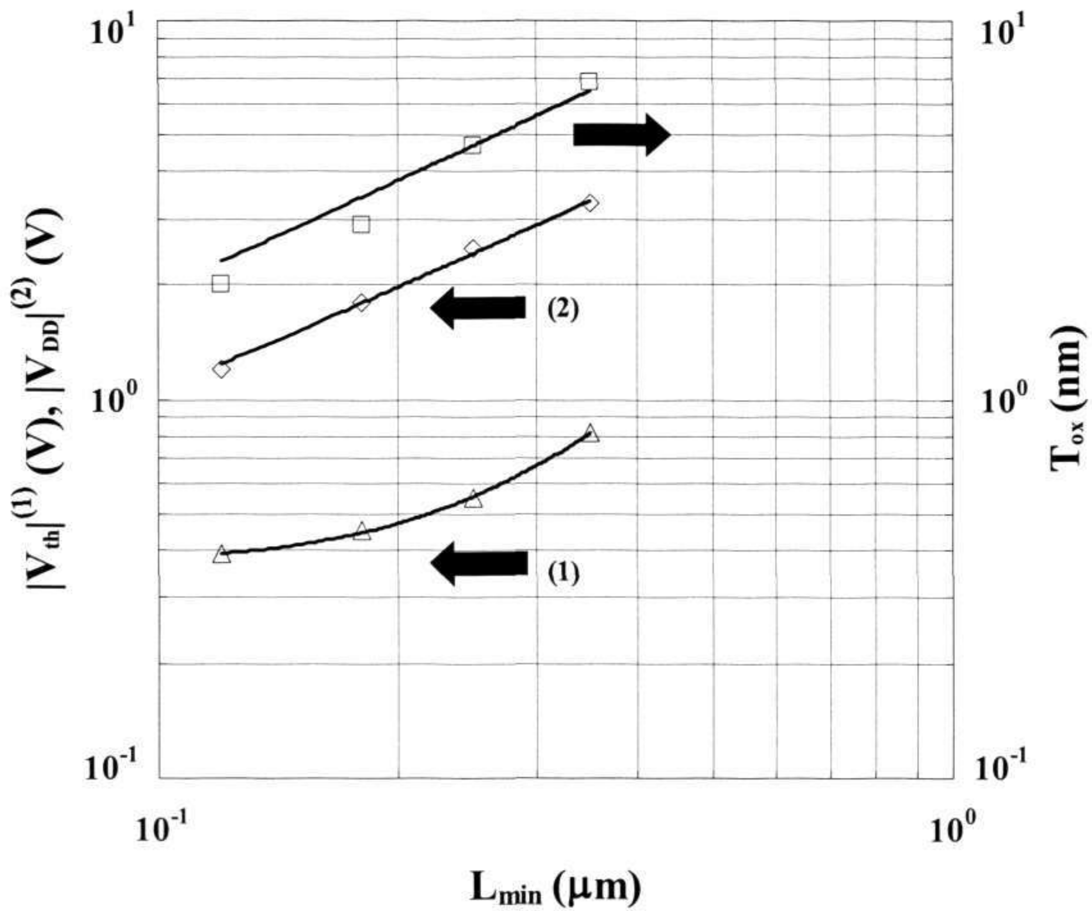

Fig. 5.1: Effect of technology scaling on three key device parameters. Note that L_{min} refers to the nominal gate length transistor from each of the four technologies. The gate width is kept at 20μm.

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Table 5.1: Comparison of the gate oxide growth sequence for the four CMOS technologies.

Gate Oxidation Sequence	0.13μm Technology	0.18μm Technology	0.25μm Technology	0.35μm Technology
Oxidation	18 sec. at 950°C (dry)	28 sec. at 1000°C (dry)	2 min. at 800°C (wet)	12 min. at 800°C (wet)
Nitridation	NO (60 sec. at 950°C)	N_2O (73 sec. at 1000°C)	N_2O (30 min. at 850°C)	-
Anneal	N_2O (120 sec. at 1050°C)	N_2 (30 sec. at 1000°C)	N_2 (15 min. at 850°C)	

Fig. 5.2 illustrates the secondary ion mass spectroscopy (SIMS) profiles of nitrogen in the oxynitride films for the three technologies that employed nitrided gate dielectrics. It can be seen that the concentration of nitrogen near the interface increases with more advanced technology. For the 0.13μm node, by nitriding the thermally grown gate oxide with pure NO ambient and subsequently annealing it in N_2O ambient, a peak nitrogen concentration of 1.8% near the interface has been obtained. Heavier nitridation of the gate dielectric in the more advanced technologies is essential to suppress impurity diffusion into the gate dielectric and to provide increased gate dielectric capacitance density without compromising the gate leakage current [24].

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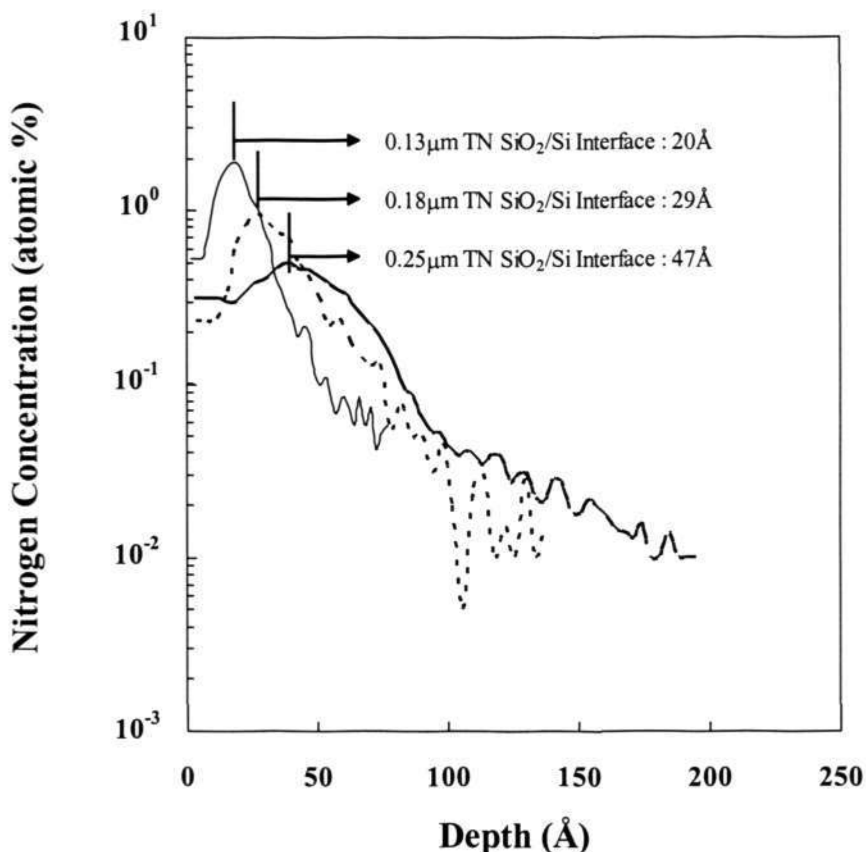

Fig. 5.2: Comparison of the nitrogen SIMS profile in the oxynitride film for the three technologies that employed nitrided gate oxide. Indicated in the figure is the approximated physical gate oxide thickness for each node.

5.3 Thin and Thick Gate Oxide PMOS 1/f Noise Scaling Trends and 1/f Noise Mechanisms

Figs. 5.3(a) and 5.3(b) show the comparison of the drain current noise spectra for the thin gate oxide (TN) transistors, and that of the thin gate oxide non-nitrided transistor from the 0.35μm node with its thick gate oxide (TK) I/O counterparts from the other three technologies respectively. It can be observed from Fig. 5.3(a) that with technology scaling from 0.35μm to 0.13μm, the drain current noise spectrum has increased by about two orders of magnitude. It can be further deduced from the insert in Fig. 5.3(a) that the

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normalized S_{Id} scales with approximately $L^{-3.5}$ at 1Hz. These trends agree with the published data [1], [2], [88]. Fig. 5.3(b) illustrates the impact of incorporating nitrided oxides in advanced CMOS TK technologies. Note that the TK transistors from 0.13μm, 0.18μm and 0.25μm technologies, and the 0.35μm TN transistor have similar dimensions (channel width, W=20μm and gate length, L=0.35μm), approximately equivalent amount of channel and source/drain dopants, and oxide thickness of about 7nm. This eliminates the effects of geometry, oxide thickness and voltage scaling during the comparison. Fig. 5.3(b) shows that nitridation (comparing the non-nitrided 0.35μm TN transistor with the nitrided 0.18μm TK transistor) has resulted in an order increase in S_{Id} at 1Hz. This agrees with published literature [89]. However the S_{Id} of the 0.13μm TK transistor is comparable to that of the 0.18μm TK transistor at ≤ 2Hz, but drops lower for > 2Hz. This could be due to the fact that for the 0.13μm TK transistor, the N_2O annealing removes preferentially oxide traps at higher energies [2]. This is confirmed by the data shown in the insert in Fig. 5.3(b).

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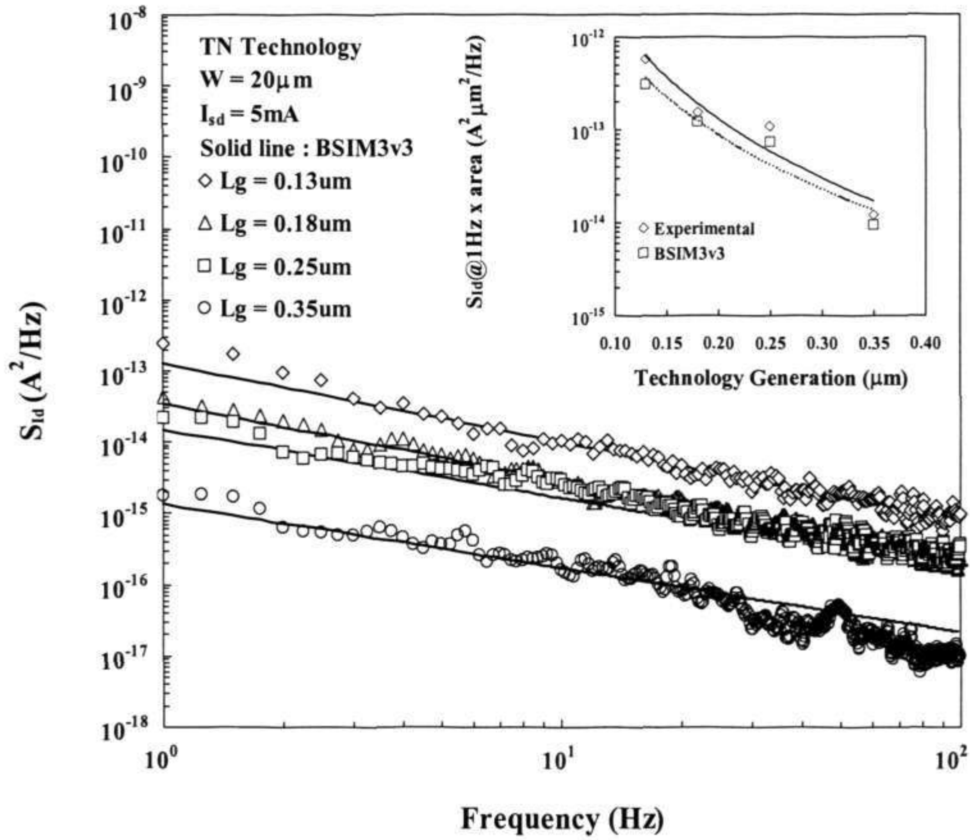
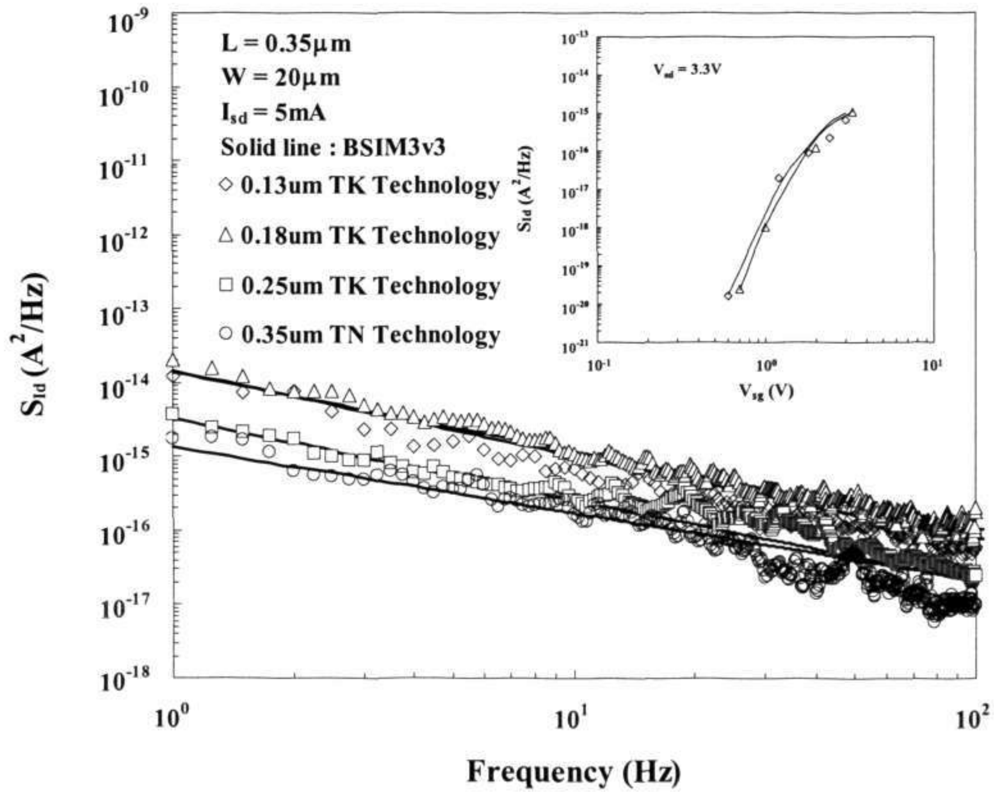


(a)



(b)

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Fig. 5.3(a): Effect of technology scaling on the drain current noise spectra of thin gate oxide transistors. The insert compares the drain current noise spectral density value at 1Hz, normalized to an active area of 1μm^2, for the four thin gate oxide technologies. The solid line and the dotted line in the insert are the least square fit trend line for the experimental and the BSIM3v3 simulation data respectively. (b): Effect of nitridation on the drain current noise spectra of thick gate oxide transistors from the 0.13μm, 0.18μm and 0.25μm technologies, compared with that of the thin gate oxide transistor from the 0.35μm technology. The insert shows the drain current noise spectral density versus the gate voltage at 10Hz for thick gate oxide transistors from the 0.13μm (◊) and 0.18μm (Δ) technologies respectively. The solid line in the insert represents the BSIM3v3 simulation results.

Figs. 5.4(a) and 5.4(b) show the respective input-referred voltage noise spectra and the device transconductance corresponding to current noise spectra shown in Figs. 5.3(a) and 5.3(b). Contrary to what have been reported in the literature previously [23], [25], the results in Fig. 5.4(a) show that the normalized S_{Vg} increases with technology scaling initially before tapering to a "plateau" with further scaling, as indicated by the least square fit solid trend line in Fig. 5.4(a). This trend is observed when one takes into consideration the changeover to nitrided gate oxide from the 0.25μm node and below. Fig. 5.4(a) also illustrates the effect of technology scaling on g_m. It can be seen that g_m scales with approximately $L^{-1.2}$. Since the higher rate of increase of the normalized S_{Id} with technology scaling is being moderated by a lower rate of increase of g_m, this could have resulted in the "plateau" seen between the 0.13μm node and the 0.25μm node. Included in Fig. 5.4(a) is data taken from published literature [2], [90], [91] for 0.18μm, 0.25μm and 0.35μm technologies respectively. Good agreement between the published data and the experimental data can be seen. Fig. 5.4(b) demonstrates that the increase of the

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normalized S_{Vg} for the TK and TN transistors comparison is predominantly due to the increase of S_{Id} (as shown earlier in Fig. 5.3(b)), since the g_m remains fairly constant.

Table 5.2 illustrates the extracted oxide trap density (N_t), in an energy interval of kT around the surface Fermi level (E_{fn}), as a function of the oxide thickness at 10Hz. N_t (E_{fn}) has been extracted using the correlated mobility fluctuations model [34], [51], [52]. The drain current noise spectral density in this concept is given by:

$$S_{Id} = \frac{kTI_d^{\ 2}}{\alpha_t fWL}\left(\frac{1}{N} \pm \alpha_{sc}\mu_{peff}\right)^2 N_t(E_{fn}) \qquad (5.1)$$

where α_t is in the order of 10^8 cm^{-1} and α_{sc} is in the range of 2×10^{-15} Vs. For the majority of the samples characterized, the positive sign before the mobility term has been used. Table 5.2 shows that the oxide trap density ranges from 10^{16} to 10^{17} cm^{-3} eV^{-1}. Included in row two of Table 5.2 in parenthesis is data taken from other reports [22], [92] for 0.18μm and 0.25μm technologies respectively. Close agreement between the published data and the experimental data can be seen. The extracted oxide trap density correlates well with the earlier S_{Id} trends seen in Figs. 5.3(a) and 5.3(b). It substantiate the proposition that the S_{Id} of the 0.13μm TK transistor is slightly lower than that of the 180 nm TK transistor due to partial annealing of the oxide traps located at higher energy level with N_2O treatment after NO nitridation.

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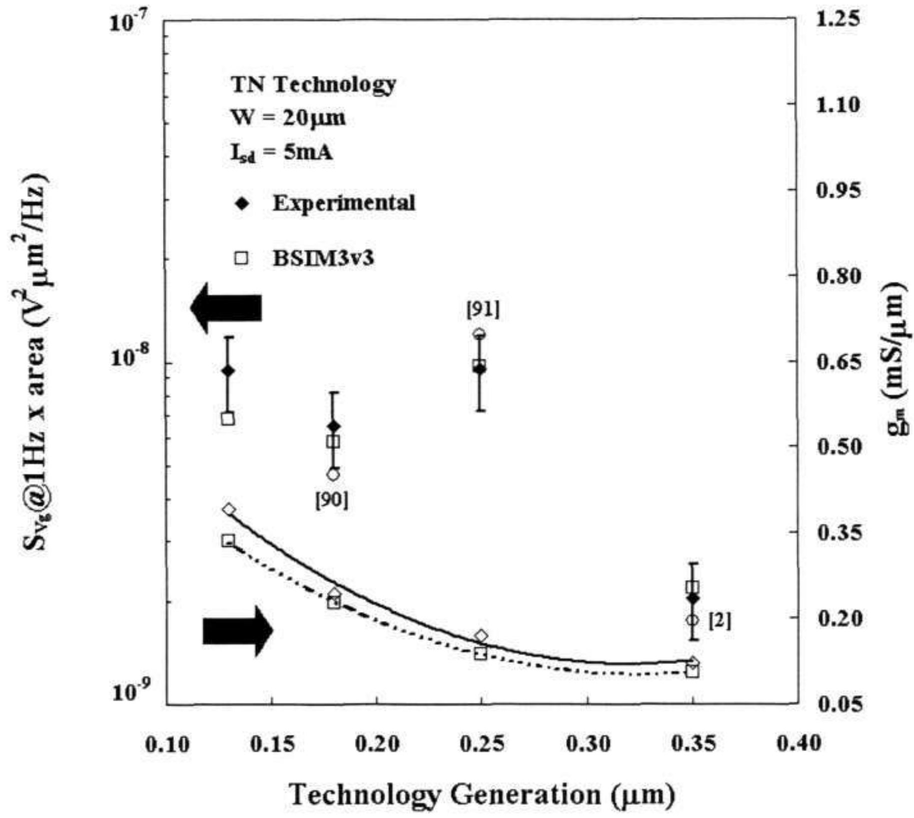

(a)

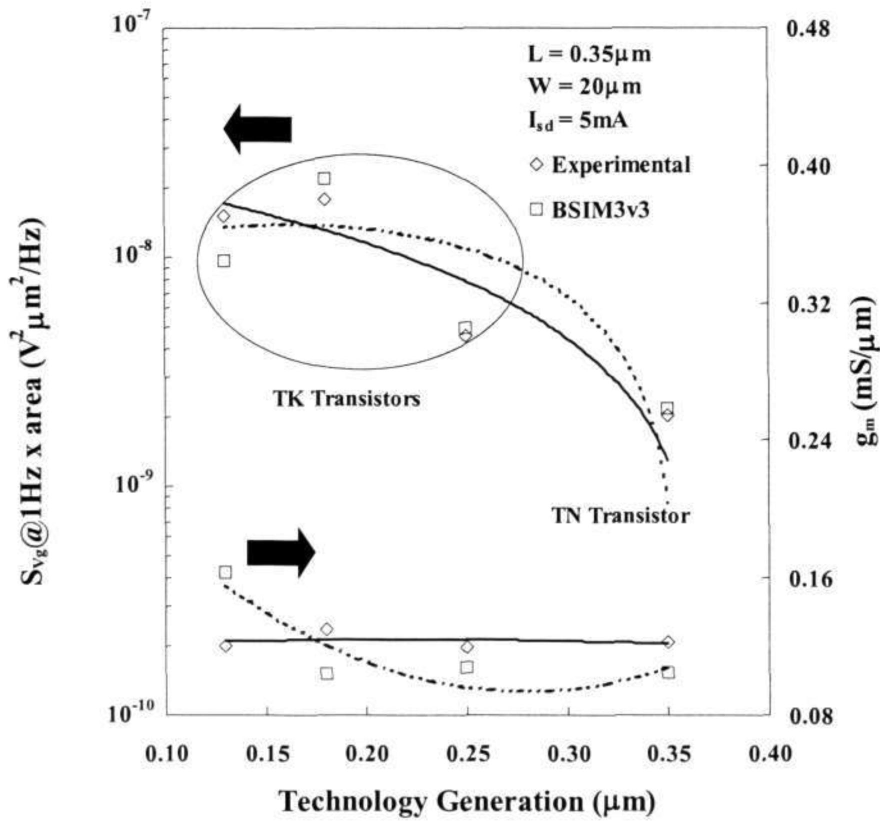

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Fig. 5.4(a): Effect of technology scaling on the input-referred voltage noise spectral density at 1Hz, normalized to an active area of 1μm², and the transconductance of thin gate oxide transistors. Included in this figure is S_{Vg} data taken from references [2], [90] and [91] for benchmarking. The solid line and the dotted line are least square fit trend lines for the experimental data and the BSIM3v3 simulation data respectively. (b): Effect of technology scaling on the input-referred voltage noise spectral density at 1Hz, normalized to an active area of 1μm², and the transconductance of thick gate oxide transistors from the 0.13μm, 0.18μm and 0.25μm technologies, compared with that of the thin gate oxide transistor from the 0.35μm technology. The solid line and the dotted line are least square fit trend lines for the experimental data and the BSIM3v3 simulation data respectively.

Table 5.2: List of oxide trap density N_t (E_{fn}), Hooge's constant α_H, and the HSPICE level 3 flicker noise model parameters K_F and A_F, for each TN and TK technology. The conditions used for the extraction of N_t (E_{fn}) and α_H are Ids = 5mA, f = 10Hz and V_{ds} is the V_{DD} of the particular technology. Included in this table is N_t (E_{fn}) data taken from references [22] and [92] for benchmarking.

Parameter \ Technology	0.13μm TN	0.18μm TN	0.25μm TN	0.35μm TN	0.13μm TK	0.18μm TK	0.25μm TK
N_t (E_{fn}) ($cm^{-3}\,eV^{-1}$)	4.96×10^{17}	2.20×10^{17} (4.31×10^{17} [92])	2.39×10^{17} (1.70×10^{17} [22])	2.01×10^{16}	7.81×10^{16}	1.27×10^{17}	3.33×10^{16}
α_H	9.09×10^{-4}	4.48×10^{-4}	4.46×10^{-4}	3.38×10^{-5}	1.83×10^{-4}	2.18×10^{-4}	5.46×10^{-5}
K_F (V^2F)	3.50×10^{-23}	5.50×10^{-23}	4.00×10^{-23}	7.00×10^{-24}	5.00×10^{-23}	8.00×10^{-23}	1.72×10^{-23}
A_F	1.15	1.15	0.95	0.90	1.12	1.15	0.95

According to Hooge's bulk mobility fluctuation model [33], [50] the drain current noise spectra can be given by:

$$\frac{S_{Id}}{I_d^{\,2}} = \frac{q\alpha_H}{fWLQ_N} \tag{5.2}$$

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α_H was found to have a universal value of 2×10^{-3} when the expression was applied to homogeneous samples. However it is known that for modern MOS transistors, the values are typically several orders of magnitude smaller than 2×10^{-3} [34], [66], [93]. This agrees with the data shown in Table 5.2. A considerable dependence of α_H on the gate bias and oxide thickness has been observed by other researchers [94], [95], which contradicts Hooge's theory. Hence in order to account for the discrepancy between the expected and measured values of α_H, Hooge and Vandamme proposed that only phonon scattering contributes to flicker noise, while other types of scattering suppress the flicker noise at low frequencies [87]. This semi-empirical refinement of the original Hooge's parameter is described as follows:

$$\alpha_H = \alpha_{H*}\left(\frac{\mu_{peff}}{\mu_{ph}}\right)^2 \tag{5.3}$$

where α_{H*} is the true Hooge parameter of approximately 2×10^{-3}.

Table 5.2 indicates that nitridation has increased the Hooge's parameter by a maximum of an order of magnitude (comparing the 0.35μm TN non-nitrided transistor with the 0.13μm TN nitrided transistor). It is known that nitridation enhances the effective hole mobility degradation at high transverse fields [96]. Hence this explains the order increase in α_H with nitridation.

Fig. 5.5 illustrates the dependence of TN transistors S_{Id} on the effective gate voltage ($|V_{gs}-V_{th}|$) for two different V_{sd} values. The plot shows that the S_{Id} of the 0.18μm, 0.25μm and 0.35μm transistors vary with approximately $|V_{gs}-V_{th}|^2$ for V_{sd} of 1.0V and $|V_{gs}-V_{th}|^{1.5}$ for V_{sd} of 0.3V. The former trend can be explained by the correlated mobility fluctuation model [34] and the latter trend can be attributed to the mobility fluctuation model [2]. The

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stronger effective gate voltage dependence (power of 1.5 versus 1) for the latter trend could be due to the close proximity of the inversion layer from the interface and the oxide traps for surface channel pMOSFETs. For the 0.13μm transistors, the S_{Id} trends show little dependence on V_{sd}, and they vary with approximately $|V_{gs}-V_{th}|^2$. This means that correlated mobility fluctuations dominate.

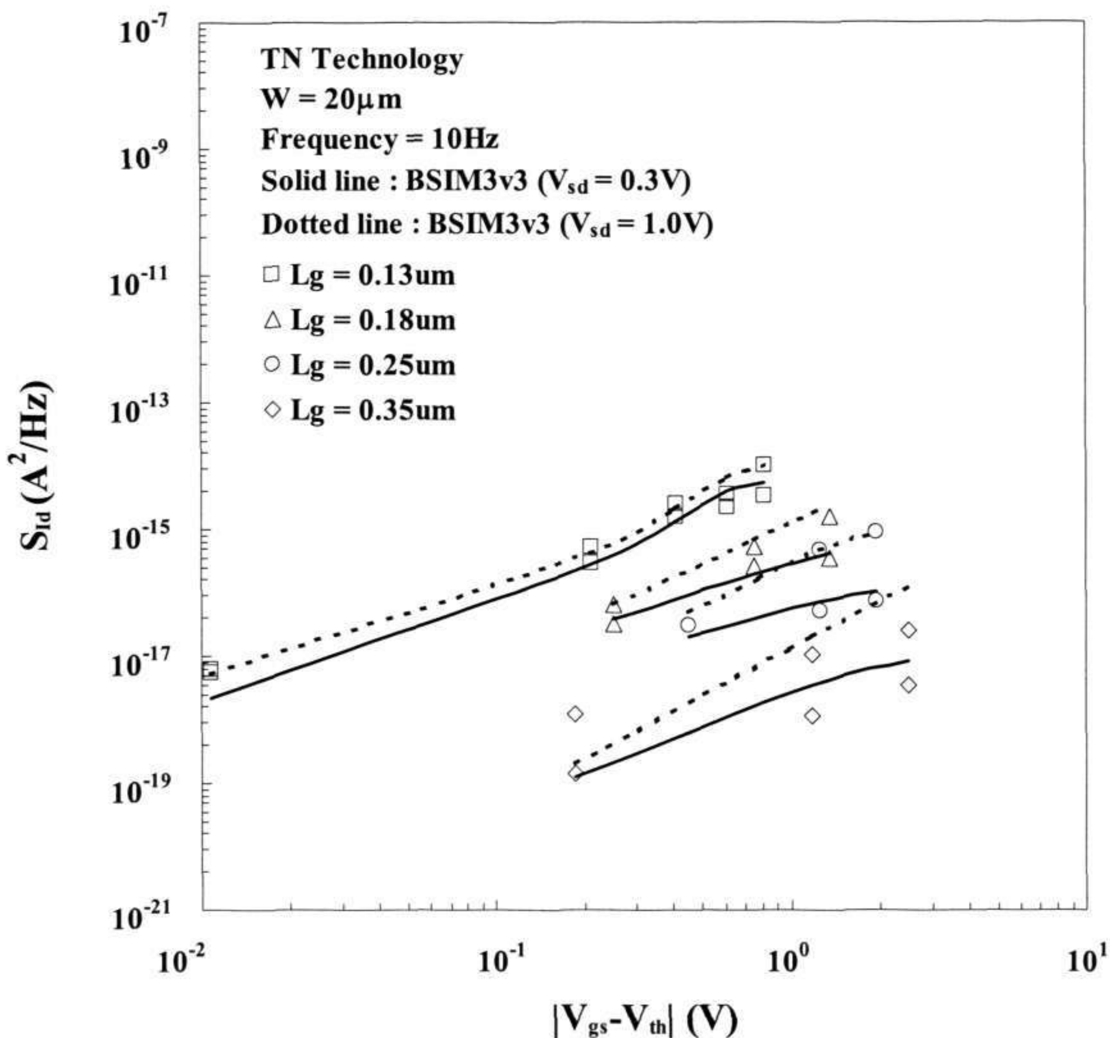

Fig. 5.5: Drain current noise spectral density versus the effective gate voltage at V_{sd} = 0.3V and V_{sd} = 1.0V for thin gate oxide transistors at 10Hz.

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5.4 Correlation of Scaling Trends to 1/f Noise Compact Models

Comparison of the experimental data with an existing $1/f$ noise model has been performed. The BSIM3v3 flicker noise model [57] has been chosen, as it is a physics-based model that incorporates both the carrier number and surface mobility fluctuations. Furthermore, it is able to model the $1/f$ noise in all operating regimes of the MOSFET and is widely available in major circuit simulators. The BSIM3v3 noise simulations have been performed using Cadence Noisepro™.

In the saturation region with strong inversion, the BSIM3v3 $1/f$ noise model drain current noise spectral density is given by [51], [57]:

$$S_{Id} = \frac{kTq^2|I_d|\mu_{eff}}{\alpha_t f^{EF} L_{eff}^{\ 2} C_{OX}}\left[NOIA\ln\frac{N_0+N^*}{N_L+N^*} + NOIB(N_0-N_L) + \frac{NOIC}{2}\left(N_0^{\ 2}-N_L^{\ 2}\right)\right] + \Delta L_{clm}\frac{kTI_d^{\ 2}}{\alpha_t f^{EF} W_{eff} L_{eff}^{\ 2}}\frac{NOIA+NOIBN_L+NOICN_L^{\ 2}}{(N_L+N^*)^2} \tag{5.4}$$

with

$$qN_0 = C_{OX}\left(|V_{gs}-V_{th}|\right) \tag{5.4a}$$

$$qN_L = C_{OX}\left(|V_{gs}-V_{th}-V_{ds}|\right) \tag{5.4b}$$

$$N^* = \frac{kT(C_{OX}+C_d+C_{it})}{q^2} \tag{5.4c}$$

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Table 5.3 lists the key 1/*f* noise model parameter values used to generate the models for each respective technology.

Table 5.3: List of BSIM3v3 model parameters for each TN and TK technology.

Technology / Parameter	0.13μm TN	0.18μm TN	0.25μm TN	0.35μm TN	0.13μm TK	0.18μm TK	0.25μm TK
$\|V_{DD}\|$ (V)	1.2	1.8	2.5	3.3	3.3	3.3	3.3
$\|V_{th}\|$ (V)	0.36	0.45	0.59	0.76	0.61	0.60	0.64
T_{OX} (m)	2.57×10^{-9}	3.70×10^{-9}	5.90×10^{-9}	8.69×10^{-9}	7.40×10^{-9}	7.15×10^{-9}	7.62×10^{-9}
E_{sat} (V/m)	1.91×10^{7}	4.43×10^{7}	3.99×10^{7}	4.36×10^{7}	2.13×10^{7}	2.27×10^{7}	2.65×10^{7}
l_c (m)	2.78×10^{-8}	3.34×10^{-8}	4.22×10^{-8}	5.12×10^{-8}	4.72×10^{-8}	4.64×10^{-8}	4.79×10^{-8}
NOIA	9.77×10^{19}	1.40×10^{18}	1.07×10^{18}	1.04×10^{18}	1.39×10^{18}	9.90×10^{16}	8.00×10^{16}
NOIB	5.50×10^{5}	5.61×10^{4}	1.14×10^{5}	4.60×10^{3}	1.85×10^{3}	1.00×10^{3}	1.00×10^{5}
NOIC	1.84×10^{-11}	6.88×10^{-12}	1.85×10^{-12}	1.40×10^{-12}	1.20×10^{-11}	1.00×10^{-11}	1.00×10^{-13}

Fig. 5.3(a) shows that there is a pronounced increase of S_{Id} with technology scaling. This can be attributed to a couple of competing scaling factors. The reduction of the oxide thickness and the effective gate voltage with technology scaling tend to decrease the current noise spectra, whereas the reduction of the active device area and the increase of the oxide trap density, due to a higher degree of nitridation, tend to increase the current noise spectra. For the correlated mobility fluctuation model, it is known that $S_{Id} \propto T_{OX}$ and $S_{Id} \propto |V_{gs}-V_{th}|^2$. Fig. 5.1 shows that both V_{DD} and T_{OX} scale linearly with technology, whereas V_{th} scales approximately as a square root of technology. It has been observed that the effective gate voltage ($|V_{gs}$ ($=V_{DD}$) $-V_{th}|$) continues to scale linearly with technology. On the other hand, the insert in Fig. 5.3(a) shows that the normalized S_{Id} scales with approximately $L^{-3.5}$ at 1Hz. In retrospect, it is clear that the reduction of the active device area and the increase of the oxide trap density dominate over the reduction of the oxide

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thickness and the effective gate voltage, hence resulting in an overall rise of the current noise spectra, as shown in Fig. 5.3(a). These competing factors are included in the BSIM3v3 1/*f* noise model (refer to equation 5.4). Figs. 5.3(a), 5.3(b), 5.4(a), 5.4(b) and 5.5 illustrate that the simulation results correlate well with the experimental trends.

Alternatively the device 1/*f* noise can be described by the level-3 HSPICE flicker noise model. This is given by [86]:

$$S_{Id} = \frac{KFg_m^{\ 2}}{C_{OX} W_{eff} L_{eff} f^{AF}} \tag{5.5}$$

Shown earlier in Table 5.2 is the extracted AF values for the TN and TK technology transistors respectively. It can be observed that the AF values for the TN and TK transistors vary from a minimum of –10% to a maximum of +15% from the expected ideal frequency exponent value of 1. This indicates that the noise data are predominantly $1/f^{\gamma}$-like, with $0.9 < \gamma < 1.15$ and a mean of 1.05. This variation in the frequency exponent about the mean value is due to the non-uniform spatial distribution of the oxide trap density near the Si/SiO_2 interface [37].

5.5 Conclusion

In this study the competing scaling effects of gate length, gate dielectric thickness, device threshold voltage, effective gate voltage and oxide trap density, due to the varying degree of nitridation, on the 1/*f* noise of nominal channel length, surface-type pMOSFETs have been investigated. The pMOSFETs have been processed in four advanced CMOS technologies. In the saturation region with strong inversion, it has been found that with technology scaling from 0.35μm to 0.13μm, the drain current noise spectra increase by approximately two orders of magnitude. This has been explained by analyzing the scaling

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trends of the abovementioned parameters and their effects on the current noise spectra. It can be concluded that the reduction of the active device area and the increase of the oxide trap density dominate over the reduction of the oxide thickness and the effective gate voltage, resulting in an increase of the current noise spectra. The effect of nitridation on thick gate oxide I/O transistors from the 0.13μm, 0.18μm and 0.25μm technologies, compared to their architecturally equivalent thin gate oxide transistor from the 0.35μm technology has been performed. The results show that nitridation has resulted in an order increase in S_{Id} at 1Hz. Correlation of the experimental data with the BSIM3v3 1/*f* noise model has been carried out. A good agreement between the measurements and the simulation has been achieved.

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CHAPTER 6
IMPACT OF TECHNOLOGY SCALING ON THE 1/f NOISE OF THIN AND THICK GATE OXIDE DEEP SUBMICRON NMOS TRANSISTORS

6.1 Introduction

In the previous chapter, we have examined the effects of technology scaling on the 1/*f* noise characteristics of PMOS transistors taken from four advanced CMOS technologies with dual gate oxide thicknesses. The results show that the S_{Id} of thin gate oxide PMOS transistors increase by approximately two orders of magnitude when scaling from 0.35μm to 0.13μm technology. Furthermore, the comparison of thin gate oxide non-nitrided PMOS transistor from the 0.35μm node with its architecturally equivalent thick gate oxide PMOS I/O transistors from the 0.13μm, 0.18μm and 0.25μm nodes reveals a maximum of an order increase in S_{Id} at 1Hz.

This work continues to investigate the effects of technology scaling on the 1/*f* noise behaviour of deep submicron NMOS transistors fabricated using dual gate oxide thicknesses. It examines the composite effect of channel length and gate oxide thickness scaling, coupled with the effect of gate dielectric nitridation on the 1/*f* noise performance of minimum gate length NMOS transistors taken from the four advanced CMOS technologies previously mentioned.

Section 6.2 of this chapter describes the device fabrication process, the characterization setup employed and the biasing condition used for the comparisons. Section 6.3 examines the effects of a higher degree of gate oxide nitridation, resulting from a consequence of technology downscaling, on the 1/*f* noise performance of deep

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submicron thin and thick gate oxide NMOS transistors. This is followed by the identification of the mechanisms responsible for the 1/*f* noise of deep submicron thin gate oxide NMOS transistors. Section 6.4 discusses the 1/*f* noise compact models generated to simulate these NMOS devices. Lastly, section 6.5 summarizes this chapter.

6.2 Device Fabrication and 1/f Noise Characterization

The CMOS transistor process flow starts with the field oxide isolation scheme; sacrificial oxide growth; followed by twin well and channel dopants implantation; sacrificial oxide removal; gate oxide growth; polysilicon gate patterning; lightly-doped drain (LDD) implantation; nitride spacers formation; source and drain regions implantation; salicidation; contact formation; metallization and finally passivation. NMOS transistors fabricated on p-type silicon wafers with a resistivity of 6-9 Ω-cm has been used for this study. For each technology, both the thin gate oxide transistors (for high speed core circuitries) and the thick gate oxide transistors (for high voltage I/O circuitries) with minimum gate lengths have been characterized. The physical thickness of the thin gate dielectrics varies from 2nm to 7nm, whereas that for the thick gate dielectrics is approximately 7nm. The channel width for all transistors is 20μm.

On-wafer flicker noise measurements have been performed using Cadence 9812B 1/*f* noise system connected to a HP35670A dynamic spectrum analyzer in a shielded CASCADE™ probe station. The hardware system is controlled by Cadence NoisePro™ software residing on a Windows™ PC. HP4156 parametric analyzer has been used to provide the biasing voltages at the device's source, gate and bulk terminals, and to provide a constant current source at the device's drain terminal. Static parameter measurements have been performed prior to the 1/*f* noise measurements. The current

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noise at the drain (S_{Id}) is fed to a low-noise voltage amplifier and the amplified signal is output to the HP35670A dynamic signal analyzer. The background noise level has been corrected for by performing noise measurements at the drain bias of 500μV. For subsequent measurements, this background noise level is subtracted away from the measured data. Drain current noise spectra have been measured in the frequency range of 1Hz to 100Hz. An average of 100 spectra has been taken for each biasing condition via NoisePro™. These spectra are subsequently averaged by NoisePro™ to produce a single spectrum for each biasing condition. All the measurements have been carried out at room temperature. More in-depth discussions on the measurement setup and the measurement procedures can be found in Chapter 3. Comparisons of 1/*f* noise from the various technologies have been made at a specific drain current I_{ds} of 10mA.

6.3 Thin and Thick Gate Oxide NMOS 1/f Noise Scaling Trends and 1/f Noise Mechanisms

Table 6.1 illustrates the gate oxide growth sequence and conditions used for each technology. Shown in the last row of Table 6.1 is the peak nitrogen concentration obtained from Secondary Ion Mass Spectroscopy (SIMS) for each technology node. Note that the 0.35μm node uses pure thermal oxide gate dielectric. It can be seen that the peak nitrogen concentration near the Si/SiO_2 interface increases with technology downscaling. For the 0.13μm node, by nitriding the thermally grown gate oxide in pure NO ambient and subsequently annealing it in N_2O ambient, a peak nitrogen concentration of approximately 1.9% near the interface has been obtained. Heavier nitridation of gate dielectrics in the more advanced technologies is essential to suppress impurity diffusion

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into the gate oxide and to provide increased gate dielectric capacitance density without compromising the gate leakage current [24].

In subsequent sections and figures, the nomenclature TN refers to thin gate oxide and TK refers to thick gate oxide. Also note that all comparative ratios presented in the subsequent paragraphs have been derived with reference to the measured data.

Table 6.1: Comparison of the gate oxide growth sequence for the four advanced CMOS technologies. Indicated in the last row of the table is the peak nitrogen concentration obtained from SIMS analysis.

Gate Oxidation Sequence	**0.13μm Technology**	**0.18μm Technology**	**0.25μm Technology**	**0.35μm Technology**
Oxidation	18 sec. at 950°C (dry)	28 sec. at 1000°C (dry)	2 min. at 800°C (wet)	12 min. at 800°C (wet)
Nitridation	NO (60 sec. at 950°C)	N_2O (73 sec. at 1000°C)	N_2O (30 min. at 850°C)	—
Anneal	N_2O (120 sec. at 1050°C)	N_2 (30 sec. at 1000°C)	N_2 (15 min. at 850°C)	—
Peak Nitrogen Concentration from SIMS (atomic %)	1.90	0.96	0.50	—

Fig. 6.1(a) shows the comparison of the drain current noise spectra S_{Id} of TN transistors. It shows that S_{Id} increases by 30 times or 1.5 orders with technology scaling from 0.35μm to 0.13μm at 1 Hz. This can be explained by the transition from pure gate oxide to oxynitride gate dielectric with heavier amount of nitridation (refer to Table 6.1 above). Several studies have shown that the use of nitrided oxides significantly increases the 1/*f* noise in MOSFETs through an introduction of interface traps [5], [37], [60]. This phenomenon can be related to the bonding coordination at the interface of two materials [97], [98]. The average bonding coordination per atom of SiO_2-Si interface is 2.9. This is sufficiently low and promotes the formation of low defect density interfaces. On the other

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hand, the average bonding coordination per atom at the Si_xN_y-Si interface has been calculated to be approximately 3.5. This over-coordination of the Si_xN_y-Si, as compared to the SiO_2-Si interface, will promote further interface trap formation.

Fig. 6.1(b) illustrates the S_{Id} comparison of the 0.35μm non-nitrided TN transistor with its nitrided TK I/O counterparts from the other three technologies. It is important to mention that all the non-nitrided and nitrided TK transistors have similar W/L ratios of 20/0.35. They also have approximately equivalent amount of channel and source/drain dopants, and their physical oxide thickness is about 7nm. This eliminates the effects of geometry, threshold voltage and gate oxide thickness scaling from the comparison. Fig. 6.1(b) shows that nitridation has resulted in a maximum of 20 times increment in S_{Id} when the technology is reduced from 0.35μm to 0.25μm at 1Hz. This agrees with our earlier published work [89], [99]. The S_{Id} of the 0.18μm TK transistor is approximately 0.25 times lower than that of the 0.25μm TK transistor at 1Hz. This is most probably due to the differences in the gate oxidation conditions. With reference to Table 6.1, the gate oxide for the 0.18μm TK transistor is grown at a higher temperature, for a shorter period of time and in a different oxidizing ambient, but nitrided and annealed using the same chemical source employed for the 0.25μm node. It is known that gate oxide grown in dry oxygen using rapid thermal oxidation (RTO), followed by rapid thermal anneal (RTA) is dense, and has a relatively low concentration of traps and interface states [100], [101]. This would explain the lower S_{Id} of the 0.18μm TK transistor. The S_{Id} of the 0.13μm TK transistor is approximately 0.4 times lower than that of the 0.18μm TK transistor at 1Hz. This could be due to the fact that for the 0.13μm TK transistor, the N_2O annealing removes preferentially oxide traps from the interface [2].

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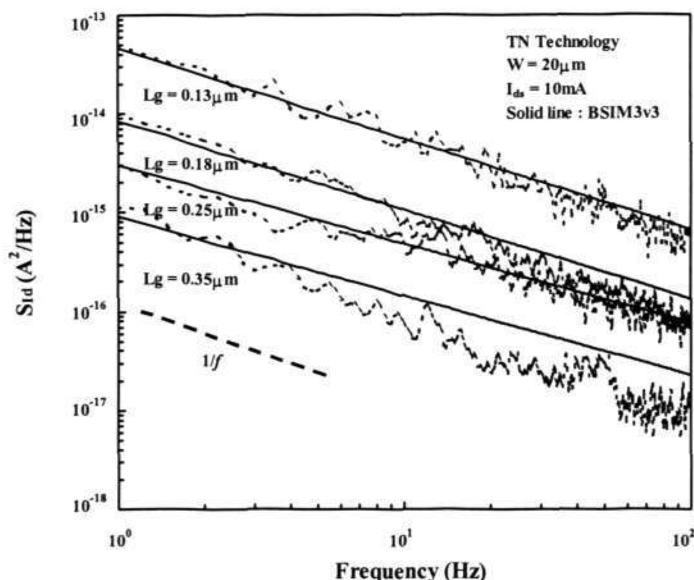

Fig. 6.1(a): Effect of technology scaling on the drain current noise spectra of thin gate oxide, minimum channel length n-MOSFETs. V_{ds} for each technology node corresponds to its respective V_{DD}. The solid lines represent the BSIM3v3 simulation data and the dotted lines represent the experimental data.

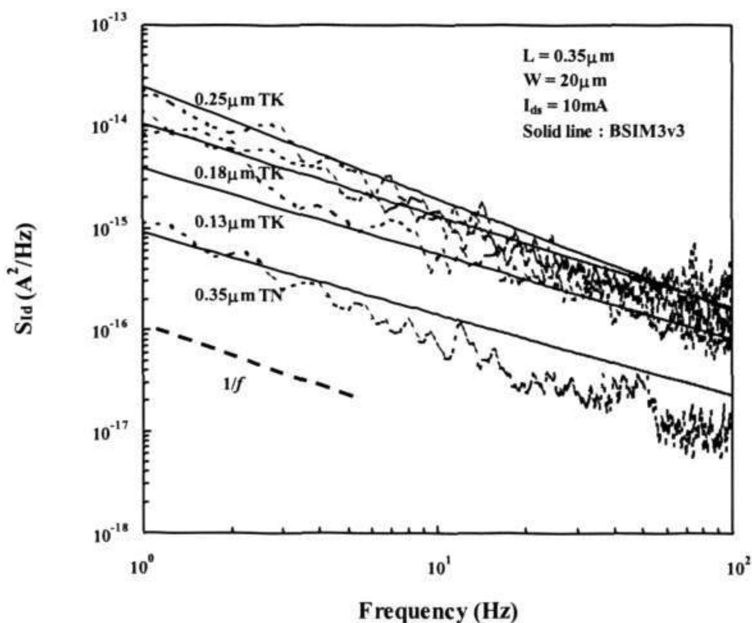

Fig. 6.1(b): Comparison of the drain current noise spectra of nitrided thick gate oxide I/O n-MOSFETs from 0.13μm, 0.18μm and 0.25μm technologies respectively with the non-nitrided thin gate oxide n-MOSFET from 0.35μm technology. All transistors have the same W/L ratio. V_{ds} used for comparison corresponds to the V_{DD} of the 0.35μm node. The solid lines represent the BSIM3v3 simulation data and the dotted lines represent the experimental data.

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Fig. 6.2(a) shows the normalized input-referred voltage noise spectra S_{Vg} at 1Hz versus the effect of minimum channel length scaling across various deep submicron technologies. S_{Vg} is defined as:

$$S_{Vg} = \frac{S_{Id}}{{g_m}^2} \tag{6.1}$$

Shown in the insert is the effect of technology scaling on the normalized S_{Id} and the device transconductance g_m respectively. Several observations can be made from the insert of Fig. 6.2(a). Firstly the normalized S_{Id} for TN transistors scales with approximately $1/{L_{g(min)}}^3$ at 1Hz in saturation. This trend agrees with other published data [1], [2], [88], [92], [102] although their comparisons have been done at low drain bias and constant V_{ds}. These authors explained the $1/L^3$ dependence by using the drain current noise spectral density of the correlated mobility fluctuation model [2]:

$$S_{Id} = \frac{kT{I_{ds}}^2}{\alpha_t f^\gamma WL}\left(\frac{1}{N} \pm \alpha_{sc}\mu_{eff}\right)^2 N_t(E_{fn}) \tag{6.2}$$

The sign of the second term in the parenthesis is chosen either negative for acceptor-like traps or positive for donor-like traps. In this work, for the majority of the samples characterized, the positive sign before the mobility term has been used for subsequent analysis. By substituting the drain current expression, equation (6.2) can be rewritten as [1]:

$$S_{Id} = \frac{kTW}{\alpha_t f^\gamma L^3}\left(\mu_{eff}{V_d}^2\right)\left(q \pm \alpha_{sc}\mu_{eff}Q_s\right)^2 N_t(E_{fn}) \tag{6.3}$$

Equation (6.3) shows that the noise power density of the drain current is proportional to $1/L^3$ at low drain bias and constant V_{ds}. In this work, the observation of a similar L dependence for S_{Id} in saturation and at constant I_{ds} can be explained by using equation

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(6.9), which gives the expression of 1/*f* noise in the saturation region. It can be seen that the equation predicts that with everything else, inclusive of I_{ds}, kept constant, S_{Id} has $1/L^2$ dependence. However, the results in this work showed a much stronger dependence of $\sim 1/L^3$. This is most probably due to the fact that in this work the authors have been investigating the scaling of 1/*f* noise across different technology nodes, thus the assumption of "everything else being kept constant", excluding I_{ds}, would not hold true.

Secondly the increasing S_{Id} with technology scaling seen in the insert of Fig. 6.2(a) can be explained when one takes into consideration the changeover to nitrided gate oxide from 0.25μm and below. Contrary to what have been reported in [23], [25], Fig. 6.2(a) shows that S_{Vg} does not decrease with technology scaling. It is evident that S_{Vg} increases with technology scaling initially before decreasing slightly with further scaling to 0.13μm and below. The decrease in S_{Vg} for 0.13μm and below is because g_m^2 in the denominator of equation (6.1) increases at a faster rate than the increment of S_{Id} in the numerator. With reference to the experimental data shown in Fig. 6.2(a), when scaling from 0.18μm to 0.13μm, g_m^2 increases by four times as compared to the three times increase in S_{Id}. This resulted in approximately 0.2 times decrease in S_{Vg}. Fig. 6.2(b) demonstrates that the trend of the normalized S_{Vg} for the TK and TN transistors comparison is determined predominantly by their respective S_{Id}, since their g_m remains fairly constant. Hence the trend of S_{Vg} mirrors that of S_{Id} closely.

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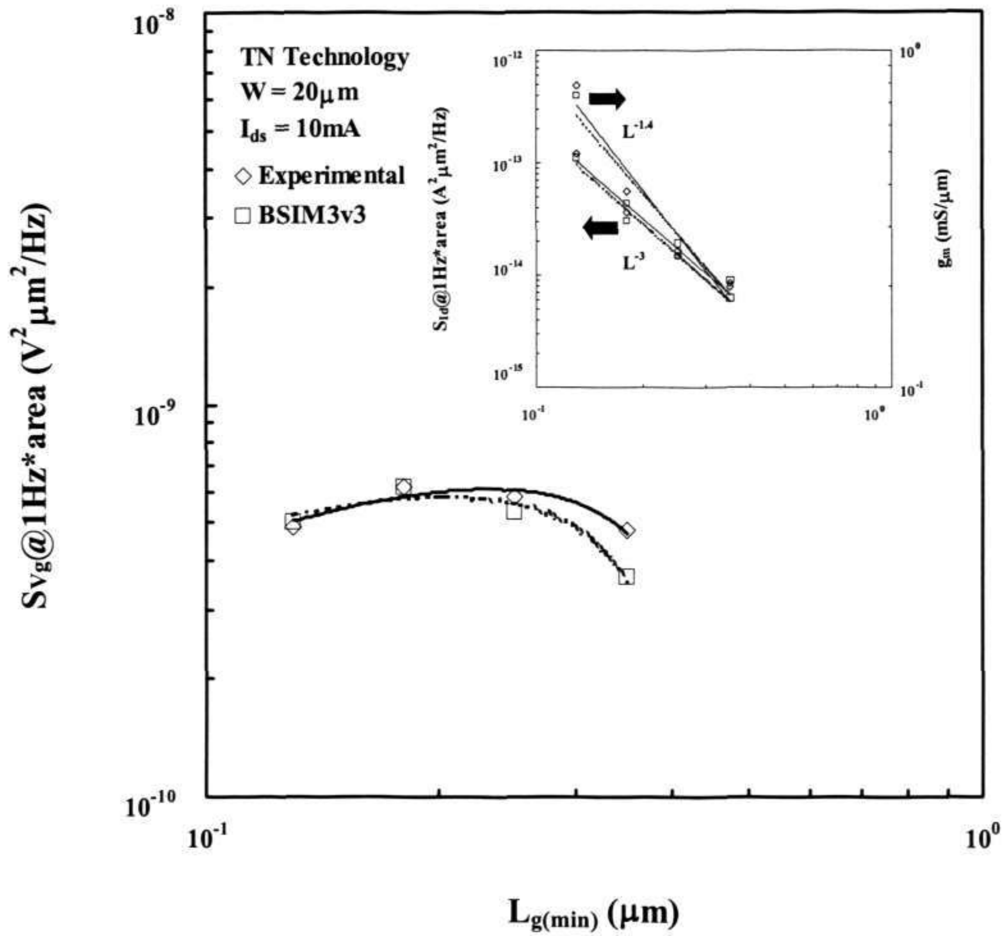

Fig. 6.2(a): Effect of minimum channel length scaling across various deep submicron technologies on the normalized S_{Vg} at 1Hz of thin gate oxide n-MOSFETs. V_{ds} for each technology node corresponds to its respective V_{DD}. Shown in the insert is a log-log plot of the effect of minimum channel length scaling across various deep submicron technologies on the normalized S_{Id} (primary y-axis) and the transconductance, g_m (secondary y-axis) at 1Hz. The solid lines and the dotted lines are the least square fit trend lines for the experimental data and the BSIM3v3 simulation data respectively.

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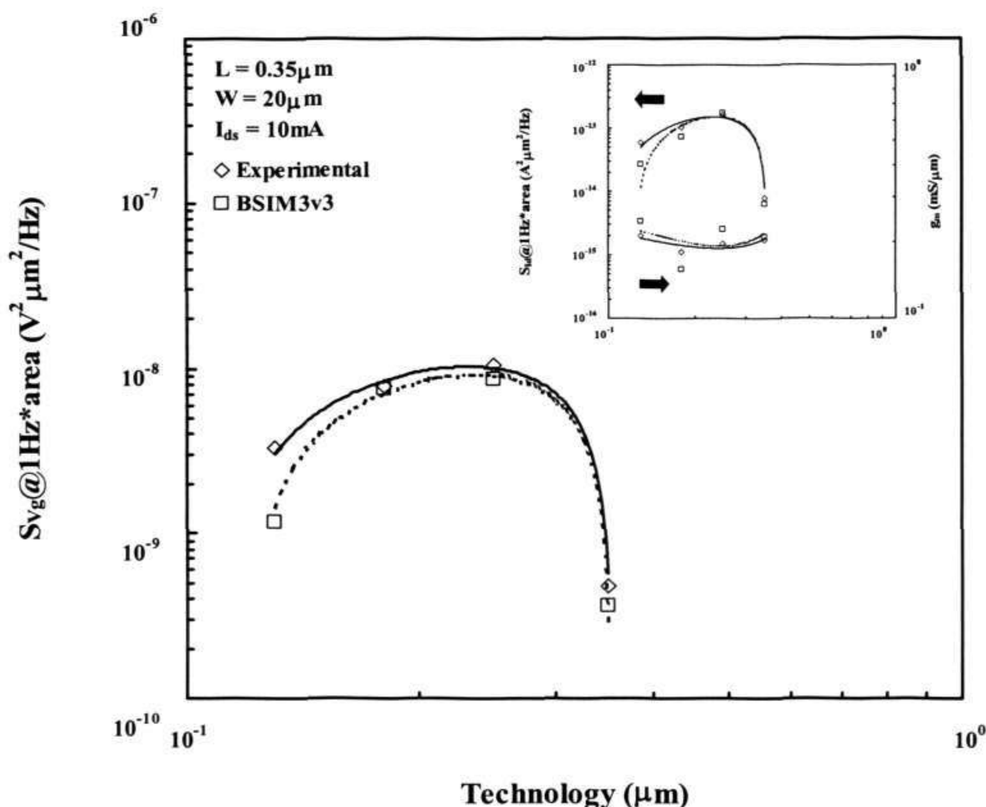

Fig. 6.2(b): Effect of process/technology scaling at constant W/L dimension on the normalized S_{Vg} at 1Hz of nitrided thick gate oxide transistors from 0.13μm, 0.18μm and 0.25μm technologies respectively, compared with the non-nitrided thin gate oxide transistor from the 0.35μm technology. V_{ds} used for comparison corresponds to the V_{DD} of the 0.35μm node. Shown in the insert is a log-log plot of the effect of process/technology scaling at constant W/L dimension on the normalized S_{Id} (primary y-axis) and the transconductance, g_m (secondary y-axis) at 1Hz. The solid lines and the dotted lines are the least square fit trend lines for the experimental data and the BSIM3v3 simulation data respectively.

Fig. 6.3 shows the normalized drain current noise plotted versus the drain current in a log-log scale, and compared with the $(g_m/I_{ds})^2$ ratio. This plot provides a practical identification of the origin of the low frequency noise source in a MOS device. It has been found that when the normalized drain current noise S_{Id}/I_{ds}^2 is closely correlated to the

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$(g_m/I_{ds})^2$ ratio, the number fluctuations dominate the flicker noise behaviour [2], [50]. In the carrier number fluctuation model, the normalized drain current noise is given by [50]:

$$\frac{S_{Id}}{I_{ds}^2} = \left(\frac{g_m}{I_{ds}}\right)^2 S_{Vg} \tag{6.4}$$

Therefore if S_{Vg} is weakly bias dependent, S_{Id}/I_{ds}^2 will vary with $(g_m/I_{ds})^2$. S_{Vg} is actually related to the flatband voltage spectral density associated with the interface charge fluctuations S_{VFB} and correlated mobility fluctuations as [34], [50], [51]:

$$S_{Vg} = S_{VFB}\left(1 \pm \alpha_{sc}\mu_0 C_{OX}\{V_{gs} - V_{th}\}\right)^2 \tag{6.5}$$

S_{VFB} is defined as [90]:

$$S_{VFB} = \frac{q^2 kTN_t(E_{fn})}{\alpha_t WLC_{OX}^2 f^{\gamma}} \tag{6.6}$$

By taking a square root on both sides of equation (6.5), one could extract the values of S_{VFB} and α_{sc}. The variations of $S_{Vg}^{0.5}$ versus V_{gs}-V_{th} have been plotted as shown in Fig. 6.4(b) and the extracted values of S_{VFB} and α_{sc} tabulated in the insert of Fig. 6.4(b). The values of S_{VFB} and α_{sc} are comparable or lower than those found in the literature [90]. This implicitly implies that S_{Vg} is not strongly bias dependent, and from equation (6.4), it follows that S_{Id}/I_{ds}^2 essentially varies with $(g_m/I_{ds})^2$. This is further substantiated by the data shown in Fig. 6.3, which illustrates that there is a good correlation between the two ratios. This suggests that carrier number fluctuations dominate.

Fig. 6.4(a) shows the plot of S_{Vg} versus the gate overdrive voltage (V_{gs}-V_{th}) in the linear operation. It can be observed that there is a relatively flat region in the weak inversion regime for each technology node. This trend is in line with the number fluctuation model, which predicts no explicit gate bias dependence of the flicker noise in linear operation [2]. With a stronger level of inversion, a pronounced parabolic increase in

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S_{Vg} is seen for each technology node. However the number fluctuation model cannot explain this increase in strong inversion. Only number fluctuation with correlated mobility fluctuations can correctly account for the observed phenomena [90]. The input-referred voltage noise spectral density for this model is given by equation (6.5). The sign of the second term in the parenthesis is chosen either negative for acceptor-like traps or positive for donor-like traps. For the majority of the samples characterized, the positive sign before the second term has been used. Based on equation (6.5), a quadratic dependence of S_{Vg} on (V_{gs}-V_{th}) is expected for trapping noise with correlated mobility fluctuations. This is consistent with the results shown in Fig. 6.4(a).

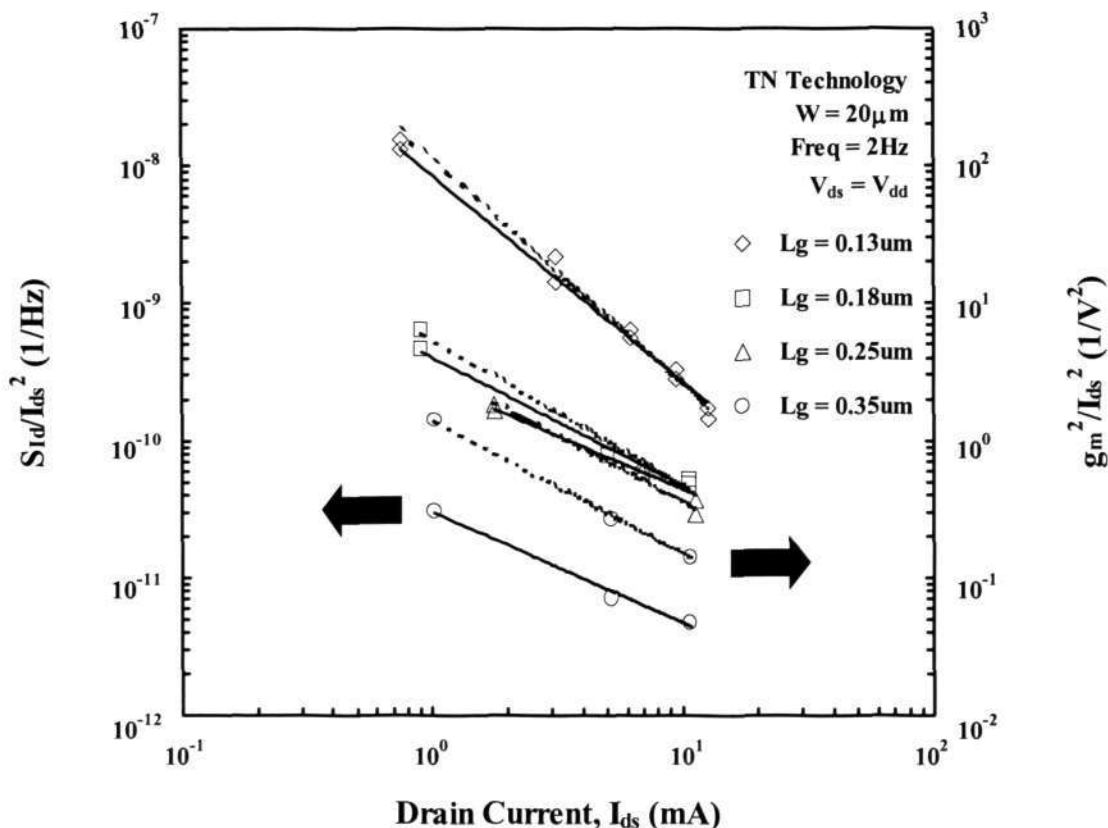

Fig. 6.3: Ratios of S_{Id}/I_d^2 and $(g_m/I_d)^2$ versus the drain current in a log-log scale for thin gate oxide, minimum channel length n-MOSFETs at 2Hz. The solid lines and the dotted lines represent the trend lines for S_{Id}/I_d^2 and $(g_m/I_d)^2$ data respectively.

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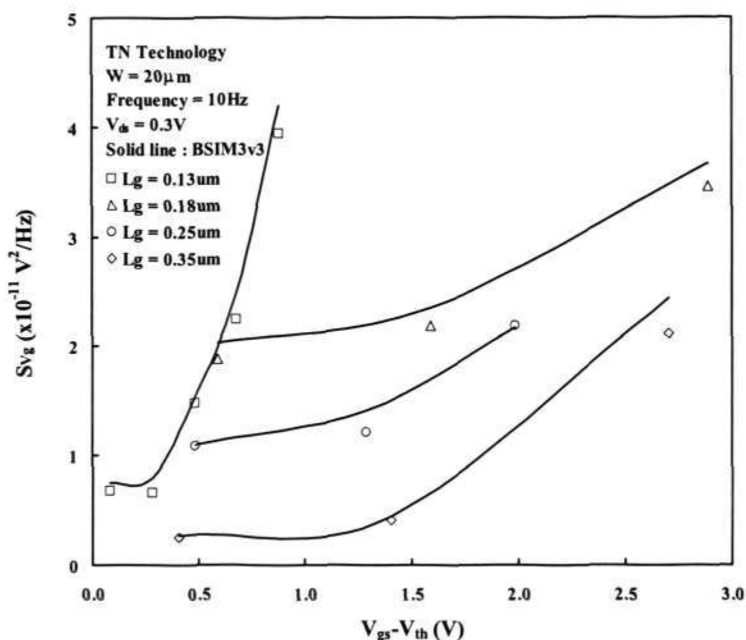
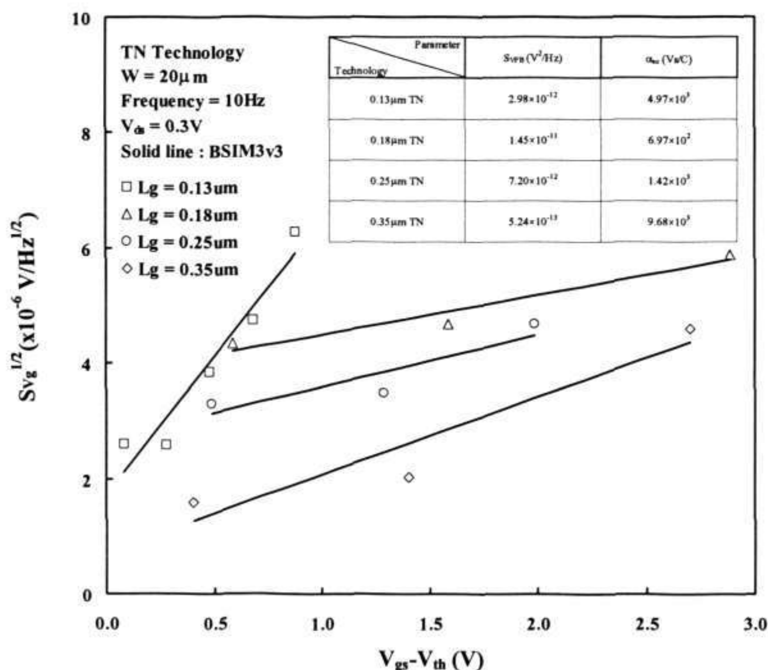


Fig. 6.4(a): S_{Vg} versus the gate overdrive voltage (V_{gs}-V_{th}) for thin gate oxide, minimum channel length n-MOSFETs in linear operation at 10Hz. The solid lines represent the BSIM3v3 simulation data and the symbols represent the experimental data.



Technology \ Parameter	S_{VFB} (V^2/Hz)	α_{sc} (Vs/C)
0.13μm TN	2.98×10^{-12}	4.97×10^{3}
0.18μm TN	1.45×10^{-11}	6.97×10^{2}
0.25μm TN	7.20×10^{-12}	1.42×10^{3}
0.35μm TN	5.24×10^{-13}	9.68×10^{3}

Fig. 6.4(b): $S_{Vg}^{0.5}$ versus the gate overdrive voltage (V_{gs}-V_{th}) for thin gate oxide, minimum channel length n-MOSFETs in linear operation at 10Hz. The solid lines represent the linear fits of the experimental data and the symbols represent the experimental data. Shown in the insert is a table listing the extracted flat band spectral density, S_{VFB} and the scattering parameter, α_{sc} for each technology node.

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Tabulated in the second row of Table 6.2 is the extracted oxide trap density $N_t(E_{fn})$ in an energy interval of kT around the surface Fermi level, as a function of the oxide thickness at 10Hz. $N_t(E_{fn})$ has been extracted using the correlated mobility fluctuation model as specified in equation (6.2). The presented data shows that the oxide trap density for the nitrided devices is in the order of 10^{16} cm^{-3} eV^{-1}, whereas that of the non-nitrided device is in the order of 10^{15} cm^{-3} eV^{-1}. This is in good agreement with the results published by other researchers [22], [34].

Tabulated in the third row of Table 6.2 is the Hooge's constant α_H at 10Hz. In Hooge's mobility fluctuation model [33], [50] the normalized drain current noise spectrum is given by:

$$\frac{S_{Id}}{I_{ds}^{\ 2}} = \frac{q\alpha_H}{f^{\gamma} WLQ_N} \tag{6.7}$$

Originally it was thought that α_H was a fundamental constant for all materials in the range of 10^{-3} when the expression was applied to homogeneous samples [33]. Nowadays, this parameter is often used as a figure-of-merit to gauge the quality of the material, and it is known that for modern MOS transistors, the values of α_H are typically several orders of magnitude smaller than 10^{-3} [34], [66], [93]. This agrees with the data shown in Table 6.2. Furthermore it can be observed that nitridation has increased the Hooge's parameter by a maximum of 21 times comparing the 0.35μm non-nitrided TN transistor with the 0.13μm nitrided TN transistor.

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Table 6.2: List of oxide trap density N_t (E_{fn}), Hooge's constant α_H, and the HSPICE level 3 flicker noise model parameters K_F and A_F, for each TN and TK technology. The conditions used for the extraction of N_t (E_{fn}) and α_H are Ids = 10mA, f = 10Hz and V_{ds} is the V_{DD} of the particular technology.

Technology / Parameter	0.13μm TN	0.18μm TN	0.25μm TN	0.35μm TN	0.13μm TK	0.18μm TK	0.25μm TK
N_t (E_{fn}) (cm^{-3} eV^{-1})	8.25×10^{16}	7.91×10^{16}	1.84×10^{16}	8.41×10^{15}	2.11×10^{16}	6.36×10^{16}	5.82×10^{16}
α_H	7.22×10^{-5}	4.06×10^{-5}	1.70×10^{-5}	3.41×10^{-6}	2.40×10^{-5}	7.59×10^{-5}	6.45×10^{-5}
K_F (V^2F)	4.50×10^{-24}	5.00×10^{-24}	3.10×10^{-24}	2.80×10^{-24}	1.20×10^{-23}	3.50×10^{-23}	3.50×10^{-23}
A_F	1.05	1.10	1.00	1.15	1.00	1.08	1.10

6.4 Correlation of Scaling Trends to 1/f Noise Compact Models

The MOS transistor 1/*f* noise can be described by the HSPICE level 3 flicker noise model. This is given by [86]:

$$S_{Id} = \frac{K_F g_m^{\;2}}{C_{OX} W_{eff} L_{eff} f^{A_F}} \tag{6.8}$$

Tabulated in the fourth and fifth rows of Table 6.2 shown earlier are the extracted K_F and A_F values for TN and TK technology transistors respectively. It can be seen that the A_F values are ≥ 1. This implies that the oxide trap density decreases towards the interface [2]. Since majority of the oxide traps are located further away from the interface, this resulted in an increased of the tunneling time. Consequently this emphasizes the low frequency transitions. Although existent models often apply a pure 1/*f* law [32], [34], [103] with the assumption of an uniform spatial distribution of the oxide traps near the interface [51], in reality the spectra dependence of the measured 1/*f* noise actually is $1/f^{\gamma}$, where $1.5 < \gamma < 0.5$ is the slope of the log-log noise spectrum [104]. The argument is that

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trap density across the band gap varies with energy, and even though there may not be intrinsic spatial non-uniformity of the traps, it is possible that band bending with increasing gate voltage will "pull down" the traps, effectively causing a non-uniform distribution. This phenomenon tends to manifest for ultra-thin gate dielectrics, such as the transistors from advanced technologies that have been presented in this work. It has been reported in [22] that the frequency exponent is found close to 1 ± 0.1 at 10Hz for ultra-thin (5 to 8.5 nm) silicon oxynitride gate dielectrics.

In retrospect, comparison of the experimental data with the widely adopted BSIM3v3 flicker noise model [57] has been demonstrated in Figs. 6.1(a), 6.1(b), 6.2(a), 6.2(b), 6.4(a) and 6.4(b). The BSIM3v3 flicker noise model is a unified flicker noise model. The unified model is not, as one may think, a combination of the number fluctuation theory and the Hooge's mobility fluctuation theory, that describes carrier mobility fluctuations. Rather it extends the carrier number fluctuation theory to include the Coulomb scattering of free charge carriers by trapped oxide charges. As a consequence, not only the number of charge carriers in the channel, but also their mobility fluctuates. Since these mobility fluctuations have the same origin as the number fluctuations, they are correlated. Furthermore, this model provides a complete *1/f* noise modeling in all operating regions of the MOSFET and is widely available in major circuit simulators. The BSIM3v3 noise simulations have been performed using Cadence NoisePro™ software.

In strong inversion, the drain current noise power is given by [51], [57]:

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$$S_{Id} = \frac{kTq^2 I_{ds}\mu_{eff}}{10^8 f^{EF} L_{eff}^{\ 2} C_{OX}}\left[NOIA \ln\frac{N_0 + N^*}{N_L + N^*} + NOIB(N_0 - N_L) + \frac{NOIC}{2}\left(N_0^{\ 2} - N_L^{\ 2}\right)\right] + \Delta L_{clm}\frac{kTI_{ds}^{\ 2}}{10^8 f^{EF} W_{eff} L_{eff}^{\ 2}}\frac{NOIA + NOIB * N_L + NOIC * N_L^{\ 2}}{\left(N_L + N^*\right)^2} \quad (6.9)$$

where

$$qN_0 = C_{OX}\left(V_{gs} - V_{th}\right) \quad (6.9a)$$

$$qN_L = C_{OX}\left(V_{gs} - V_{th} - V_{ds}\right) \quad (6.9b)$$

$$N^* = \frac{kT\left(C_{OX} + C_d + C_{it}\right)}{q^2} \quad (6.9c)$$

$$\Delta L_{clm} = l_c \sinh^{-1}\left(\frac{V_d - V_{dsat}}{l_c E_{sat}}\right) \quad (6.9d)$$

$$l_c = \sqrt{\frac{\varepsilon_{si} T_{OX} X_{dep}}{\varepsilon_{ox}}} \quad (6.9e)$$

Listed in Table 6.3 are the key model parameter values. NOIA, NOIB and NOIC are the 3 BSIM3v3 fitting noise parameters [57]. Noise data has been sampled at low frequencies where the flicker noise dominates. NOIA has been extracted from several data points located in the sub-threshold region. There are several data points measured from the ohmic region (at low V_{ds}), both with low V_{gs} and high V_{gs}. NOIB has been extracted by using the data of low V_{gs} in this region, and NOIC has been extracted by using high V_{gs} data in this region. After obtaining initial values of the noise parameters by noise extraction, the final noise parameters have been obtained via noise optimization. Figs. 6.1(a), 6.1(b), 6.2(a), 6.2(b), 6.4(a) and 6.4(b) show that good agreement between the measured data and the simulation results have been achieved.

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Table 6.3: List of BSIM3v3 model parameters for each TN and TK technology.

Parameter \ Technology	0.13μm TN	0.18μm TN	0.25μm TN	0.35μm TN	0.13μm TK	0.18μm TK	0.25μm TK
V_{DD} (V)	1.2	1.8	2.5	3.3	3.3	3.3	3.3
V_{th} (V)	0.35	0.50	0.59	0.65	0.60	0.61	0.62
T_{OX} (m)	2.82×10^{-9}	3.90×10^{-9}	6.10×10^{-9}	7.65×10^{-9}	7.08×10^{-9}	7.40×10^{-9}	7.90×10^{-9}
E_{sat} (V/m)	6.29×10^{6}	1.20×10^{7}	6.10×10^{6}	7.04×10^{6}	1.10×10^{7}	6.73×10^{6}	5.66×10^{6}
l_c (m)	2.91×10^{-8}	3.43×10^{-8}	4.29×10^{-8}	4.80×10^{-8}	4.62×10^{-8}	4.72×10^{-8}	4.88×10^{-8}
NOIA	5.40×10^{20}	1.00×10^{18}	5.00×10^{20}	3.00×10^{19}	4.00×10^{20}	4.90×10^{21}	7.00×10^{21}
NOIB	6.50×10^{4}	3.00×10^{3}	2.00×10^{3}	4.00×10^{3}	1.05×10^{4}	2.00×10^{3}	2.00×10^{2}
NOIC	1.00×10^{-16}	8.00×10^{-15}	8.00×10^{-15}	8.00×10^{-16}	8.00×10^{-14}	8.00×10^{-15}	8.00×10^{-15}

6.5 Conclusion

In this work, the effects of scaling the channel length and gate dielectric thickness, coupled with increasing degree of nitridation on the 1/*f* noise of minimum gate length n-MOSFETs have been investigated. Both TN and TK transistors processed in four advanced CMOS technologies have been characterized.

It has been found that with technology scaling from 0.35μm to 0.13μm at a constant drain current of 10mA, the drain current noise spectrum of TN technology increases by approximately 1.5 orders of magnitude at 1Hz. This increase is correlated to the scaling trends of the above-mentioned technology parameters. It can be concluded that the reduction of the active gate area and the increase of the oxide trap density with technology scaling dominate over the reduction of the gate dielectric thickness and the effective gate voltage, resulting in an overall increase of the current noise spectra. The effect of incorporating nitrided gate dielectrics in advanced CMOS TK technologies, namely the

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0.13μm, 0.18μm and 0.25μm nodes, has been investigated. Comparison of these TK transistors with the architecturally equivalent furnace gate oxide TN transistor from the 0.35μm technology node has been made. The data shows that nitridation has resulted in approximately 1.25 orders increase in S_{Id} at 1Hz. Investigation of the physical origins of NMOS transistors' flicker noise has been carried out. It can be concluded that for deep submicron NMOS transistors with ultra-thin gate dielectrics, the number fluctuation with correlated mobility fluctuations dominate. Verification and comparison of the experimental data with the BSIM3v3 flicker noise model have been performed. A good agreement between the measurements and the simulation has been achieved.

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CHAPTER 7
IMPACT OF DEVICE SCALING ON THE 1/f NOISE PERFORMANCE OF DEEP SUBMICRON THIN GATE OXIDE CMOS TRANSISTORS

7.1 Introduction

The need for silicon foundries to provide various process flavours to cater for different application segments has led to the proliferation of process options such as low standby power (LSP) transistors for wireless, handheld consumer applications and low voltage (LV) and high performance (HP) transistors for high speed analog, graphics, and microprocessor designs. To provide designers with the appropriate performance-leakage design coverage and flexibility, and for systems-on-chip (SOC) solutions, these different process flavours have been offered by foundries beginning from 0.13μm technology node and below.

Foundries offer the LSP transistors as a standalone process option, whereas the LV and HP options have been made available within a single process offering termed LV/HP, as the two options share the same design rules. The LSP transistor gate length typically lags that of the LV/HP option by at least two generations, and it has a thicker gate oxide to achieve the ultra-low leakage current requirement. On the contrary, the LV/HP transistors have both the highest performance and the highest leakage current. However the LV/HP transistors have the most aggressively scaled gate length to enhance performance.

This work focuses on the 1/*f* noise of 0.13μm LSP transistors for mixed-mode and RF applications. Section 7.2 of this chapter compares the 1/*f* noise performance of the LSP transistors against the 0.13μm LV/HP and generic (G) options, as well as against the more

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mature nodes, namely 0.18μm, 0.25μm and 0.35μm respectively. Section 7.3 examines the effects of geometry scaling on the 1/*f* noise of 0.13μm LSP transistors. One important highlight of this section is the discussion of the effects of *W/L* ratio scaling. Another key topic reviewed in this section is the demonstration that the 1/*f* noise of modern small area CMOS devices is dominated by Lorentzian-like spectra. This behaviour poses great challenges to obtaining reasonable yields when minimal area low noise analog and RF circuits are employed in advanced CMOS technologies. Lastly, section 7.4 summarizes this chapter.

7.2 Comparison of 1/f Noise for Different Technologies

Fig. 7.1 shows the secondary ion mass spectroscopy (SIMS) profiles of nitrogen in the oxynitride films for 0.13μm, 0.18μm and 0.25μm nodes respectively. Note that the 0.13μm LSP variant and the 0.35μm node have been excluded from this plot because they employed furnace gate oxide without nitridation. It is evident that the peak nitrogen concentration near the Si/SiO_2 interface increases with technology downscaling. For 0.13μm LV/HP node, by nitriding the thermally grown gate oxide in pure NO ambient and subsequently annealing it in N_2O ambient, a peak nitrogen concentration of 4.3% near the interface has been obtained. Heavier nitridation of gate dielectrics in the more advanced technologies is essential to suppress impurity diffusion into the gate oxide and to provide increased gate dielectric capacitance density without compromising the gate leakage current [105].

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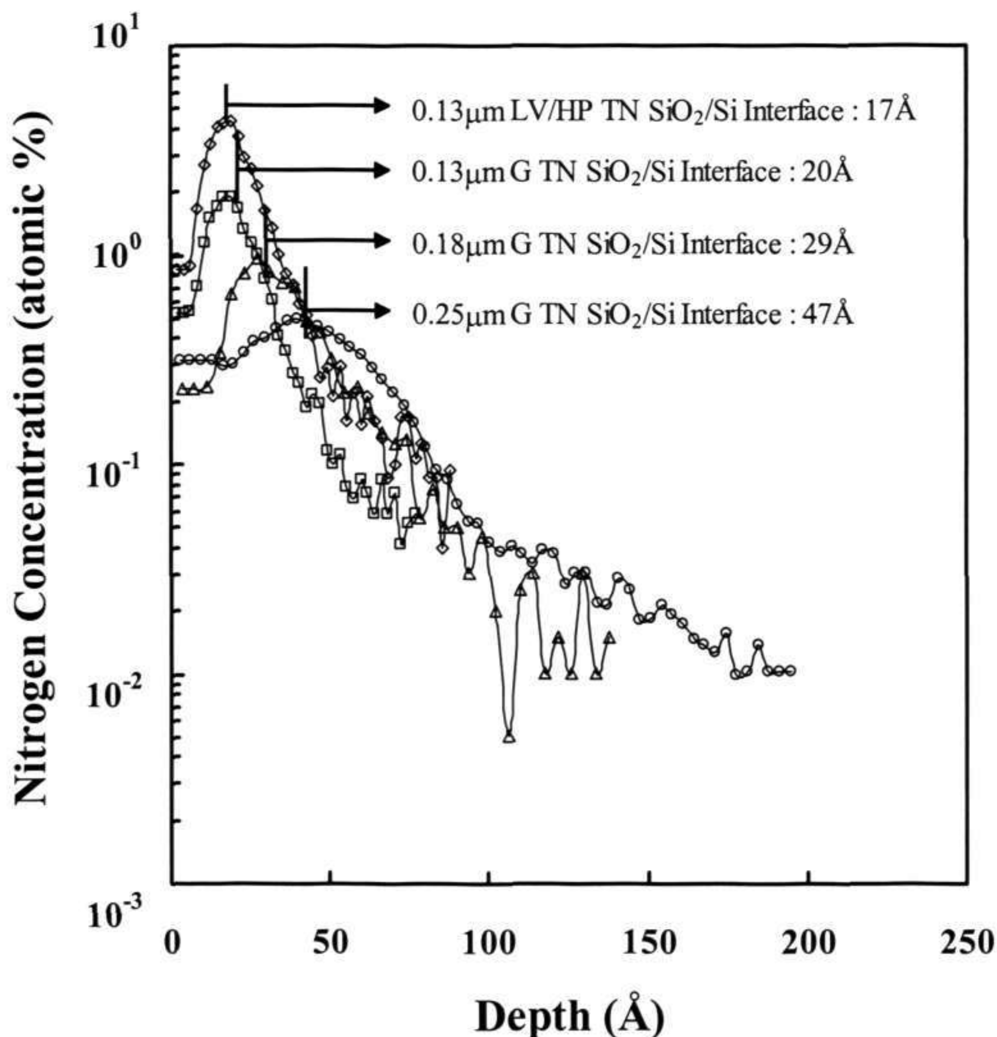

Fig. 7.1: Comparison of the nitrogen SIMS profile in the oxynitride film for the four technologies that employed nitrided gate oxide. Indicated in the figure is the approximated physical gate oxide thickness for each node.

Fig. 7.2 shows the extracted oxide trap density $N_t(E_{fn})$ in an energy interval of kT around the surface Fermi level, versus the peak nitrogen concentration in % at 10 Hz for the technology nodes demonstrated in Fig. 7.1. $N_t(E_{fn})$ has been extracted using the correlated mobility fluctuation model specified as follows [34]:

$$S_{Id} = \frac{kTI_{ds}^{2}}{\alpha_t f^{\gamma} WL}\left(\frac{1}{N} \pm \alpha_{sc}\mu_{eff}\right)^2 N_t\left(E_{fn}\right) \qquad (7.1)$$

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A clear correlation between the oxide trap density and the peak nitrogen concentration in the oxynitride films can be observed from Fig. 7.2. This agrees very well with published literature [22].

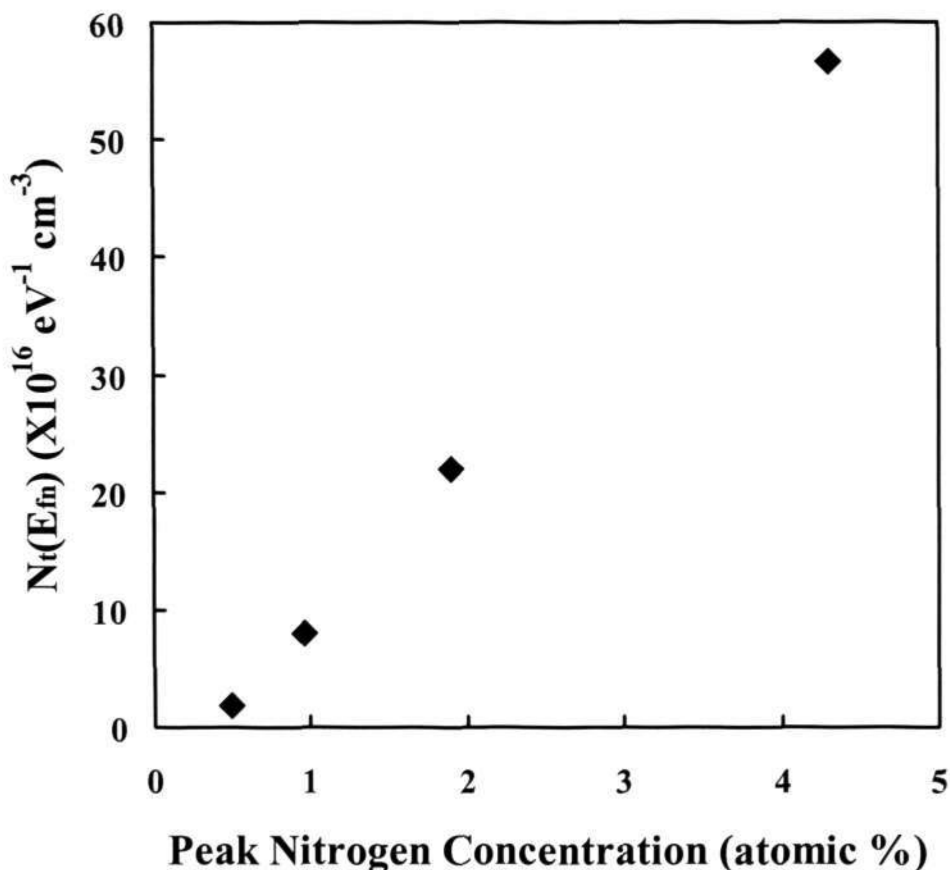

Fig. 7.2: Impact of increasing peak nitrogen concentration on the extracted oxide trap density $N_t(E_{fn})$, in an energy interval of kT around the surface Fermi level, versus the peak nitrogen concentration in % at 10Hz. The data points in this plot correspond to the technology nodes demonstrated earlier in Fig. 7.1.

Fig. 7.3 shows the comparison of the normalized NFET drain current noise versus the active gate area for 6 different technologies. It can be observed that in general as the active gate area increases, the noise level decreases. This trend agrees with literature that the noise level is inversely proportional to $1/WL$ [37]. Next it can be seen that the noise level increases with technology scaling from 0.35μm G to 0.13μm G. This trend is evident when one takes into consideration the changeover to nitrided gate oxide from 0.25μm

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technology and below. As illustrated in Fig. 7.2, increasing nitrogen incorporation near the Si/SiO_2 interface with technology scaling resulted in enhanced oxide trap density. These traps, in turn, cause the transistor to produce higher $1/f$ noise. Hence designing analog and RF circuits with deep submicron technologies would become more challenging due to a two-pronged constraint, i.e. the reduction of the voltage headroom due to a lower supply voltage and a higher floor noise, which reduces the usable dynamic range. Comparing the three different 0.13μm variants, it can be observed that the LV/HP option causes the $1/f$ noise level to be even more pronounced as compared to the G option. This is due to a higher level of gate dielectric nitridation associated with a thinner physical oxide thickness. Fig. 7.3 further illustrates that the LSP option help to moderate the escalating $1/f$ noise down to a magnitude close to that exhibited by the 0.18μm node. This has been achieved by the use of furnace gate oxide with physical oxide thickness slightly less than that of the 0.18μm node.

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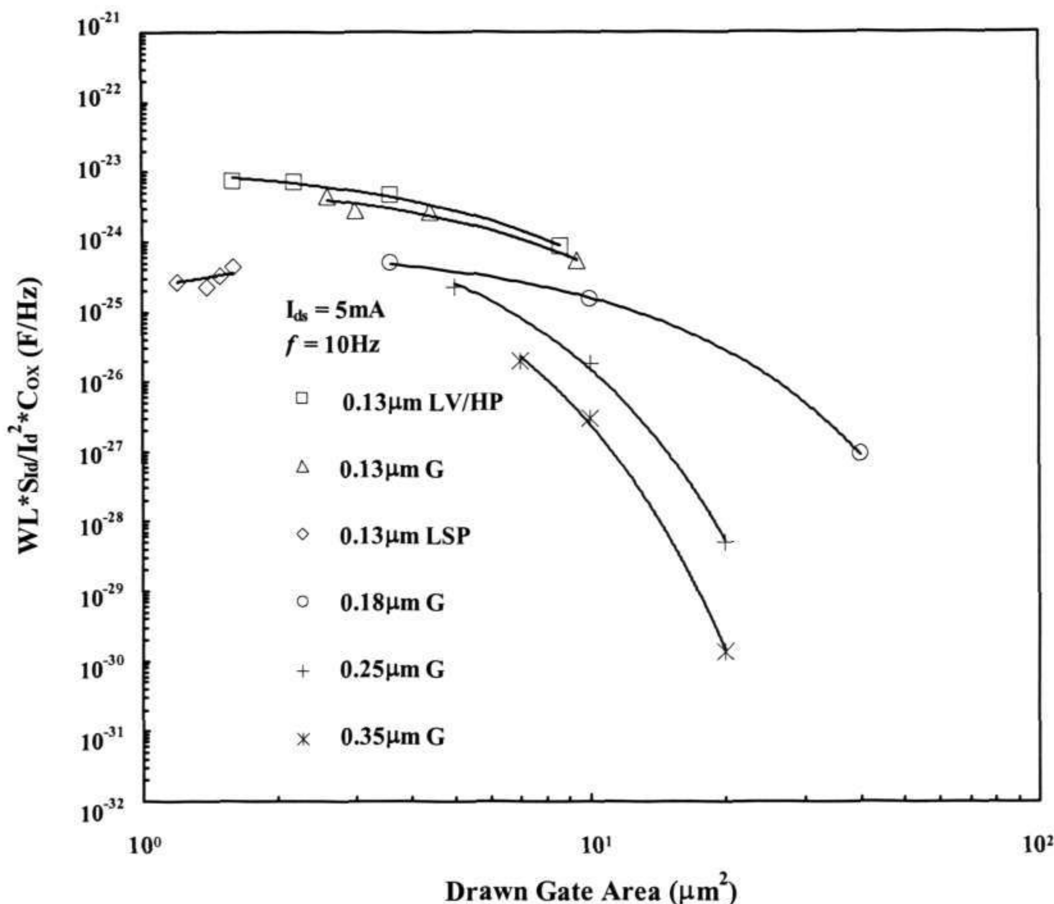

Fig. 7.3: Effect of gate geometry and technology scaling on the normalized drain current noise of NFETs. The symbols represent the measured data and the solid lines are obtained using least square fit.

7.3 *Impact of Geometry Scaling on the 1/f Noise of 0.13μm LSP Transistors*

Fig. 7.3 earlier has demonstrated the superiority of 0.13μm LSP transistors in terms of $1/f$ noise performance. In this section, we would investigate on how does device geometry scaling impacts the LSP transistors' $1/f$ noise.

By substituting the drain current expression, equation (7.1) can be rewritten as [1]:

$$S_{Id} = \frac{kTW}{\alpha_t f^{\gamma} L^3}\left(\mu_{eff} V_d^{\,2}\right)\left(q \pm \alpha_{sc}\mu_{eff}Q_s\right)^2 N_t\left(E_{fn}\right) \tag{7.2}$$

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Equation (7.2) shows that the drain current noise power density is proportional to W/L^3. From equation (7.2), it can be deduced that even if one scales down W and L by the same proportion such that the W/L ratio remains constant, the drain current noise would still increase by $1/L^2$ with technology downscaling. Similar finding has been published in our earlier work [99], [106]. This raises a concern about the $1/f$ noise performance of future generations of ultra-deep submicron MOSFET's, where low drain current noise is desired.

Figs. 7.4(a) and 7.4(b) show the effect of gate width scaling on the $1/f$ noise of LSP NFETs and PFETs with three different gate lengths, namely L = 0.15μm, 0.50μm and 10μm, at 10Hz respectively. The gate width has been varied from 0.15μm up to 100μm. Figs. 7.4(c) and 7.4(d) show the effect of gate length scaling with three different gate widths, namely W = 0.15μm, 0.60μm and 10μm, at 10Hz respectively. The gate length has been varied from 0.12μm up to 20μm. For both experiments, the drain voltage is biased at V_{DD} and the gate overdrive voltage ($|V_g - V_t|$) is maintained at 0.95V. The solid lines in Figs. 7.4(a) to 7.4(d) can be described by a power law relation of the form: $S_{Id} = Coefficient \times X^{Index}$, where X refers to the parameter plotted on the x-axis. Table 7.1 tabulates the values of the coefficient and the index for NFETs and PFETs respectively. It can be seen that the value of the coefficient increases with smaller L but decreases with smaller W. This is in agreement with equation (7.2), which specifies that $S_{Id} \propto \frac{W}{L^3}$. For a 98.5% reduction in L, an approximately six orders of magnitude increase in the NFET's coefficient and five orders of magnitude increase in the PFET's coefficient are observed. For the same percentage reduction in W, the NFET's coefficient decreases by two orders of magnitude and the PFET's coefficient decreases by approximately one order of magnitude. A possible explanation for the larger delta for the NFETs as compared to the

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PFETs can be attributed to the smaller tunneling barrier (3.1eV) experienced by electrons across the Si-SiO_2 interface relative to holes (4.5eV), the different oxide trap densities near the conduction and valence band edges and the different electron and hole mobilities. Table 7.1 further illustrates that the NFET's width dependence index values are slightly > 1, whereas those for the PFETs are slightly < 1. For the length dependence index values, both NFETs and PFETs show a dependence of close to L^{-3}. These deviations from the predictions of equation (7.2) can be attributed to errors in estimating the effective channel lengths and widths, as well as due to the non-uniform area distribution of the interfacial defects throughout the gate area.

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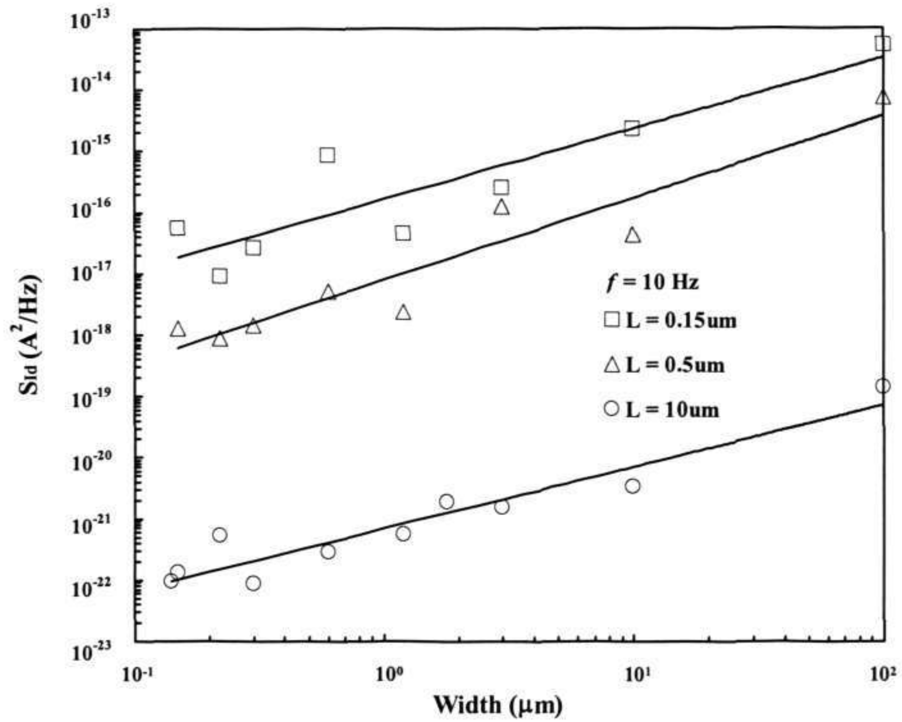

Fig. 7.4(a): Effect of gate width scaling on the drain current noise of NFETs for L = 0.15μm, 0.50μm and 10μm. The symbols represent the measured data and the solid lines are obtained using least square fit.

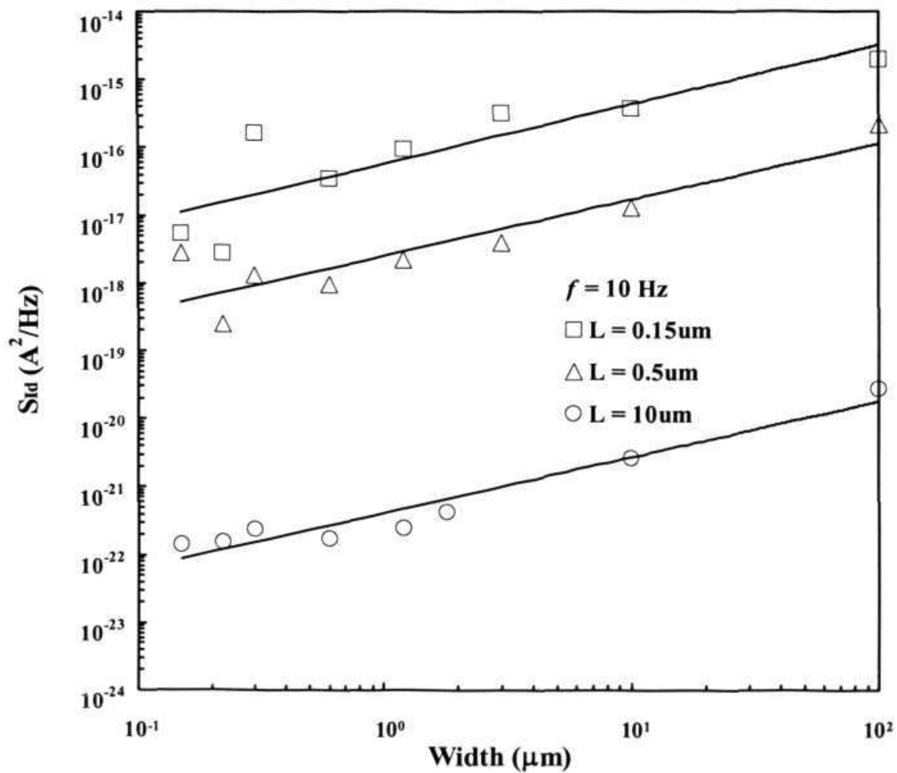

Fig. 7.4(b): Effect of gate width scaling on the drain current noise of PFETs for L = 0.15μm, 0.50μm and 10μm. The symbols represent the measured data and the solid lines are obtained using least square fit.

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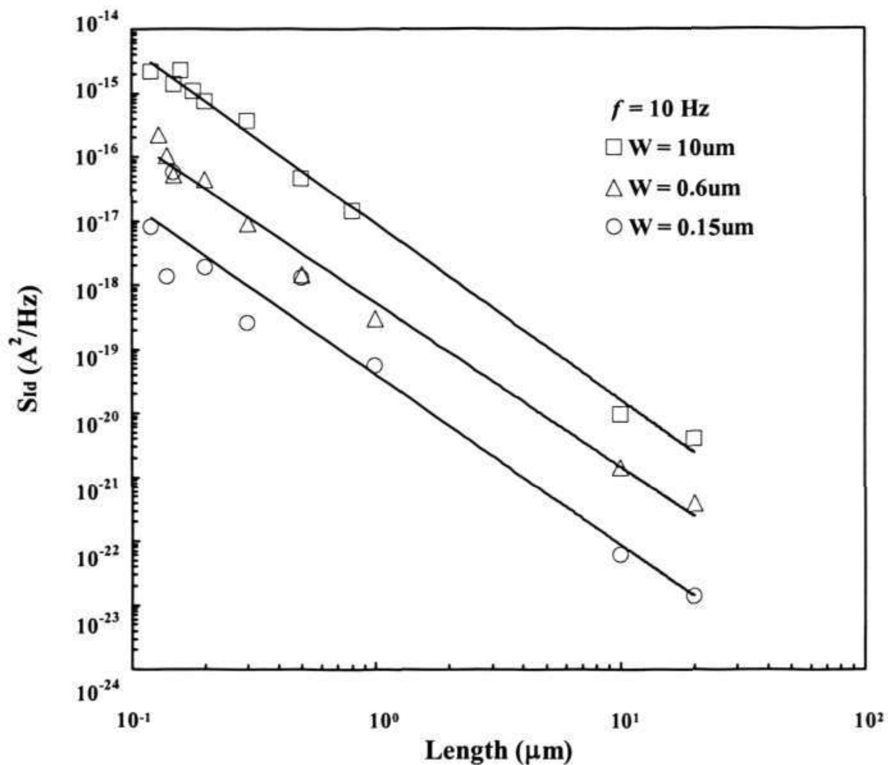

Fig. 7.4(c): Effect of gate length scaling on the drain current noise of NFETs for W = 0.15μm, 0.60μm and 10μm. The symbols represent the measured data and the solid lines are obtained using least square fit.

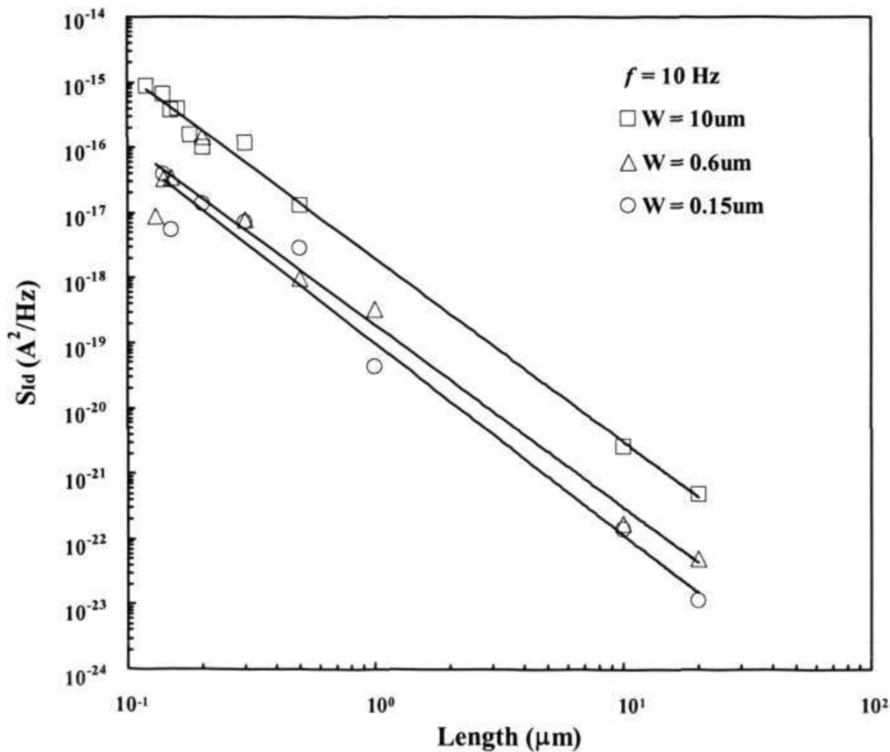

Fig. 7.4(d): Effect of gate length scaling on the drain current noise of PFETs for W = 0.15μm, 0.60μm and 10μm. The symbols represent the measured data and the solid lines are obtained using least square fit.

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Table 7.1: List of coefficients and indices for the least square fit lines included in Figs. 7.4(a)-7.4(d).

Device	NFET		PFET	
Length (μm)	**Coefficient (A^2/Hz-μm)**	**Index (Width Dependence)**	**Coefficient (A^2/Hz-μm)**	**Index (Width Dependence)**
0.15	2×10^{-16}	1.1567	6×10^{-17}	0.8710
0.50	8×10^{-18}	1.3402	3×10^{-18}	0.8264
10.0	7×10^{-22}	1.0090	4×10^{-22}	0.8179
Width (μm)	**Coefficient (A^2/Hz-μm)**	**Index (Length Dependence)**	**Coefficient (A^2/Hz-μm)**	**Index (Length Dependence)**
0.15	4×10^{-20}	-2.6526	1×10^{-19}	-2.9325
0.60	5×10^{-19}	-2.5554	2×10^{-19}	-2.7901
10.0	9×10^{-18}	-2.7381	2×10^{-18}	-2.8075

Fig. 7.5 shows the plot of the input referred gate noise voltage spectral density S_{Vg} versus the inverse of the gate geometry for both NFETs and PFETs at 10Hz respectively. S_{Vg} is defined as:

$$S_{Vg} = \frac{S_{Id}}{g_m^{\ 2}} \tag{7.3}$$

The solid lines in Fig. 7.5 can be described by a power law relation of the form: $S_{Vg} = Coefficient \times X^{Index}$, where X refers to the parameter plotted on the x-axis. Table 7.2 tabulates the values of the coefficient and the index for NFETs and PFETs respectively. Fig. 7.5 illustrates that S_{Vg} varies linearly with the inverse of the gate geometry with a slope of approximately 1 for the PFETs and 0.8 for the NFETs. The higher coefficient and slope for S_{Vg} of PFETs, as shown in Table 7.2, can be explained by examining the barrier energies experienced by holes and electrons across the Si/SiO_2 interface. The barrier heights in the valence and conduction bands of MOS transistor with thermal oxide are 4.5eV and 3.1eV respectively. After nitridation of the gate dielectric, the valence band barrier height will decrease rapidly from 4.5eV to 1.9eV, whereas that of the conduction

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band will lower slightly from 3.1eV to 2.1eV [107]. The significant lowering of the valence band barrier height will make it easier for the PFET's channel to exchange charges with the interfacial oxide traps through tunneling. Fig. 7.5 indicates that in order to minimize S_{Vg}, designers need to use very large gate geometries. For a five orders increase in the active gate area, S_{Vg} of PFETs decreases by approximately seven orders, whereas that for NFETs decreases by approximately five orders. This delta difference between PFETs and NFETs can be attributed to the different oxide trap densities near the valence and conduction band edges, as well as the different hole and electron mobilities, resulting in different degrees of correlated surface mobility fluctuations. Another observation from Fig. 7.5 is the large dispersion in noise level for devices with gate area < 1 μm^2, which can be as much as two orders of magnitude for devices with the smallest gate area. Explanations for this observation will be given in the following two paragraphs.

The availability of deep submicron MOSFET's has given researchers the opportunity to examine the noise generated by individual oxide traps. For small area devices (< 1 μm^2), it has been reported that the trapping and detrapping process of a carrier by a trap in the vicinity of the surface Fermi level over the entire channel creates discrete switching phenomena resembling a random telegraph signal (RTS) [108-110]. In frequency domain, this noise with two-level RTS switching power spectrum translates to Lorentzian-like spectrum with two distinct slopes demarcated by a corner frequency f_c. The superposition of numerous Lorentzian spectra from several small area devices will constitute the commonly observed $1/f$ noise spectrum of an equivalent large area device. Shown in Fig. 7.6(a) are the Lorentzian spectra of four NFETs, with a W/L ratio of 0.15/0.14, located on different sites in the same wafer. A Lorentzian spectrum is typically characterized by a plateau at low frequencies, followed by a sharp roll-off with a slope of $1/f^2$ above f_c. The

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corner frequencies for the 4 samples are denoted by the dotted arrows in Fig. 7.6(a), and are given by f_{c1}, f_{c2}, f_{c3} and f_{c4} respectively. It can be observed that each corner frequency is approximately 2.4 times higher than the previous one. Furthermore, as the corner frequency of each spectrum pushes towards a higher value, the magnitude of the S_{Id} at 1 Hz lowers by a maximum of one order of magnitude. The uppermost spectrum in Fig. 7.6(a) illustrates the resultant summation of the four Lorentzian spectra. The superposition of the Lorentzians produces a nearly $1/f$ noise spectrum in the low frequencies before degrading into a $1/f^2$ spectrum at high frequencies. Similar phenomena have been observed for the four PFET samples with an aspect ratio of 0.15/0.14. As illustrated in Fig. 7.6(b), each corner frequency is approximately 1.8 times higher than the previous one. As the corner frequency of each spectrum pushes towards a higher value, the magnitude of the S_{Id} at 1 Hz similarly lowers by a maximum of one order of magnitude. It can be observed that for the PFET, the onset of the degradation of the resultant spectrum into a $1/f^2$ slope starts at a much higher frequency than the NFET.

The demonstration of the existence of Lorentzian-like spectra in Figs. 7.6(a) and 7.6(b) for small size devices will help to explain the large noise dispersion seen earlier in Fig. 7.5 for this group of transistors. As mentioned earlier, the noise spectra of today's small size devices are believed to be dominated, for certain frequency band, by RTS from single-trap states. The random placement of these defects within the Si/SiO_2 energy gap leads to the formation of Lorentzian components in frequency domain. This, in turn, constitutes the large scattering of noise data observed in Fig. 7.5. Similar results have been published by other researchers [1], [111].

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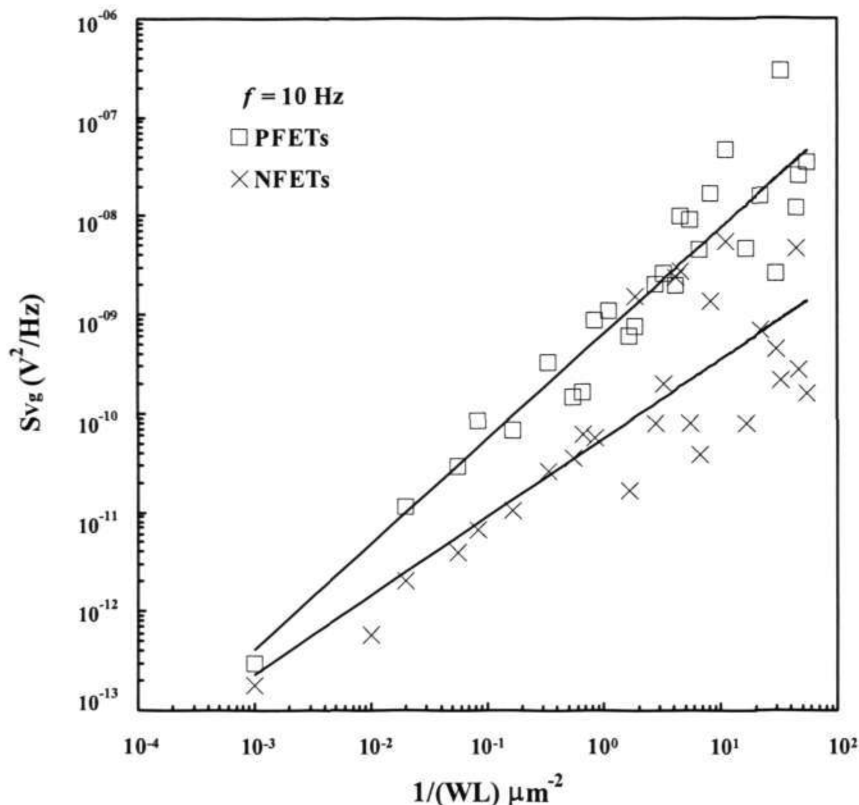

Fig. 7.5: Effect of the inverse of gate geometry scaling on the input referred gate voltage noise of NFETs and PFETs. The symbols represent the measured data and the solid lines are obtained using least square fit.

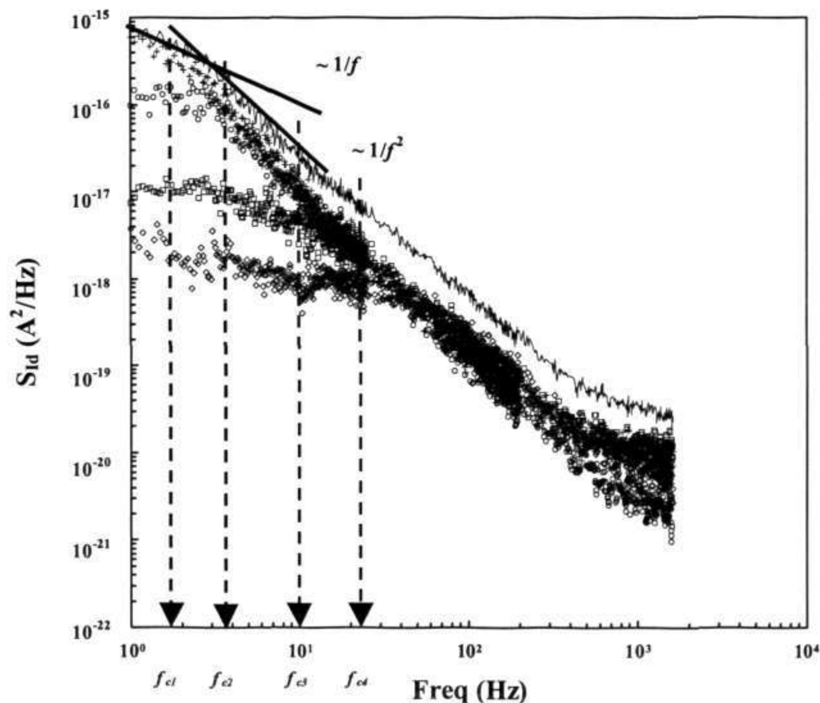

Fig. 7.6(a): Lorentzian spectra for 4 samples of W/L = 0.15/0.14 NFETs. The symbols (+ o □ ◊) refer to sample1, sample2, sample3 and sample4 respectively. f_{c1}, f_{c2}, f_{c3} and f_{c4} refer to the corner frequencies for the 4 samples respectively. The uppermost spectrum (solid line) is the resultant summation of the 4 Lorentzian spectra. The behaviors $1/f$ and $1/f^2$ are shown by bold solid lines as guides to the eye.

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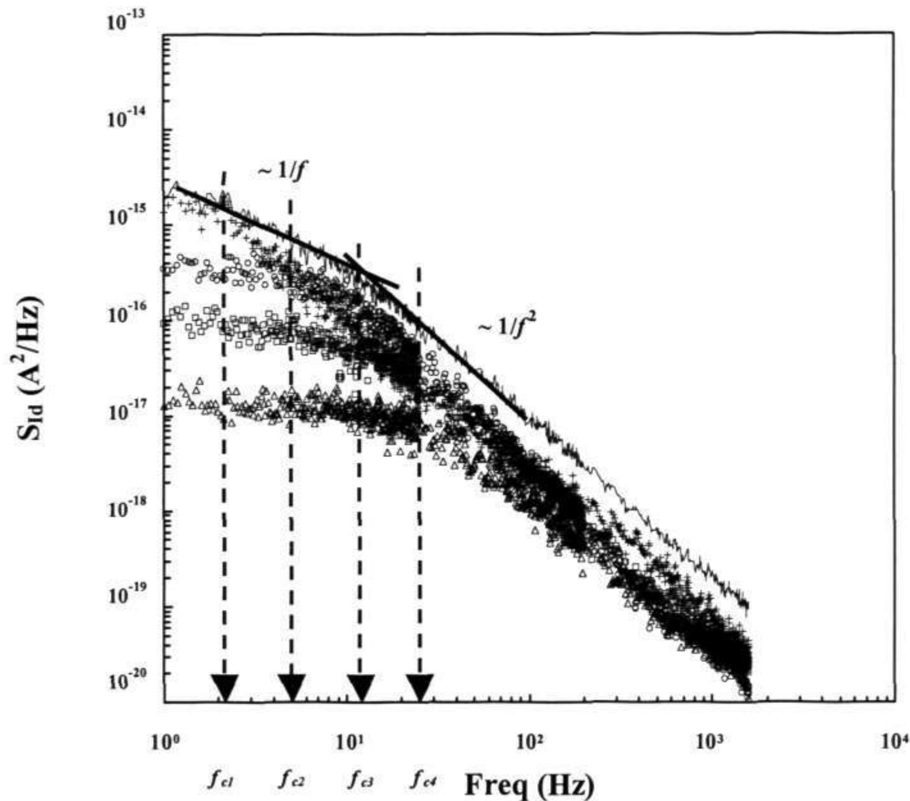

Fig. 7.6(b): Lorentzian spectra for 4 samples of W/L = 0.15/0.14 PFETs. The symbols (+ o □ ◊) refer to sample1, sample2, sample3 and sample4 respectively. f_{c1}, f_{c2}, f_{c3} and f_{c4} refer to the corner frequencies for the 4 samples respectively. The uppermost spectrum (solid line) is the resultant summation of the 4 Lorentzian spectra. The behaviors $1/f$ and $1/f^2$ are shown by bold solid lines as guides to the eye.

Table 7.2: List of coefficients and indices for the least square fit lines included in Fig. 7.5.

Device	**NFET**		**PFET**	
	Coefficient (V^2-μm^2/Hz)	**Index (Area Dependence)**	**Coefficient (V^2-μm^2/Hz)**	**Index (Area Dependence)**
	6×10^{-11}	0.7953	6×10^{-10}	1.0636

Figs. 7.7(a) and 7.7(b) show the plots of the normalized S_{Id} versus varying W/L ratio. The transistor W/L ratio varies from 0.015 to 83 and 0.015 to 200 for NFETs and PFETs respectively. The drain voltage is biased at V_{DD} and the gate overdrive voltage ($|V_g - V_t|$) is maintained at 0.95V. The solid lines in Figs. 7.7(a) and 7.7(b) can be described by a power law relation of the form: $S_{Id} \times Area = Coefficient \times X^{Index}$, where X refers to the parameter plotted on the x-axis. Table 7.3 tabulates the values of the coefficient and the

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index for NFETs and PFETs respectively. By multiplying both sides of equation (7.2) with *WL* to obtain the normalized S_{Id}, and then simplifying the right-hand side of the equation, one would arrive at $\left(S_{Id} \times WL\right) \propto \left(\frac{W}{L}\right)^2$. Table 7.3 indicates that the slopes of NFETs and PFETs are approximately 2.1 and 1.9 respectively. These indices agree closely with the theoretical prediction shown above. Figs. 7.7(a) and 7.7(b) further illustrate that the normalized S_{Id} increases as the *W/L* ratio increases. Having a larger *W/L* ratio would imply employing larger widths and/or using smaller channel lengths. Conversely, the plots show that in order to reduce the magnitude of the normalized S_{Id}, one needs to use smaller widths and/or longer channel lengths. The relation between the sizing of the gate geometry and the resulting normalized S_{Id} is illustrated pictorally in Fig. 7.7(a). Similar conclusion can be derived for the PFETs as shown in Fig. 7.7(b).

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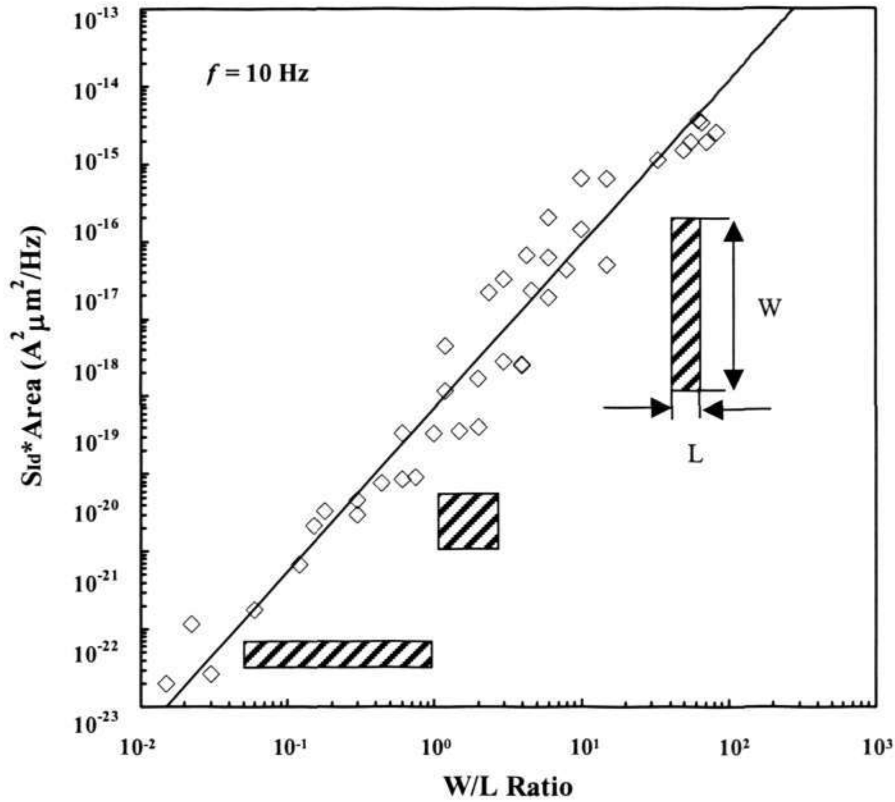

Fig. 7.7(a): Effect of aspect ratio dependence on the normalized drain current noise of NFETs. The symbols represent the measured data and the solid line is obtained using least square fit.

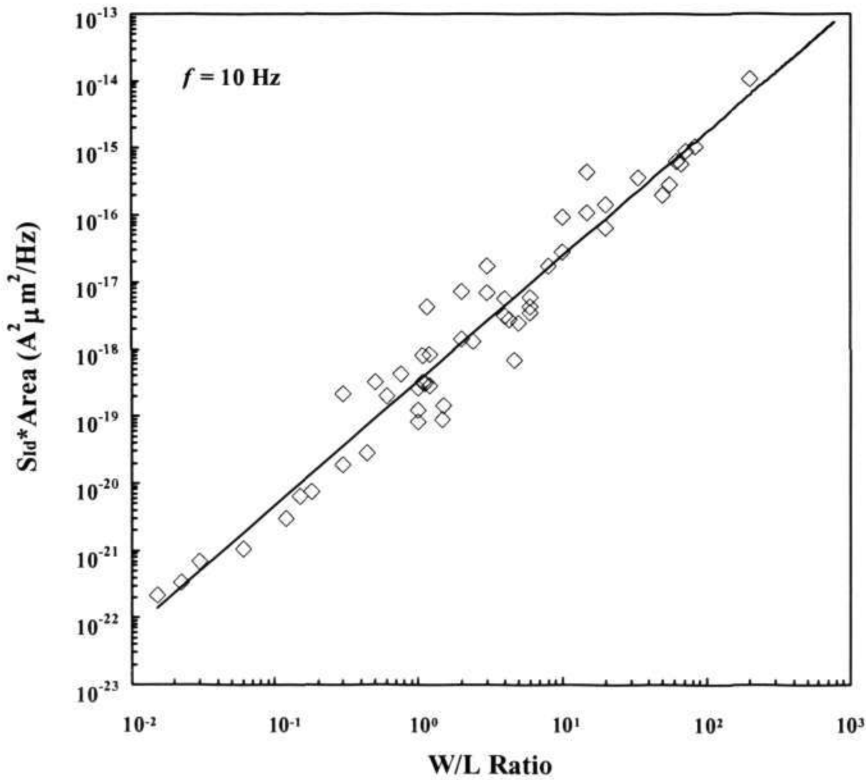

Fig. 7.7(b): Effect of aspect ratio dependence on the normalized drain current noise of PFETs. The symbols represent the measured data and the solid line is obtained using least square fit.

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Table 7.3: List of coefficients and indices for the least square fit lines included in Figs. 7.7(a) and 7.7(b).

Device	NFET		PFET	
	Coefficient (A^2-μm^2/Hz)	Index (Aspect Ratio Dependence)	Coefficient (A^2-μm^2/Hz)	Index (Aspect Ratio Dependence)
	7×10^{-19}	2.1066	3×10^{-19}	1.8566

7.4 Conclusion

In the first part of this chapter, the authors showed that the normalized S_{Id} increases with technology downscaling from 0.35µm G to 0.13µm G due to a higher degree of gate dielectric nitridation. The employment of 0.13µm LV/HP transistors aggravates this increase further. However, the use of 0.13µm LSP transistors helps to moderate this increase down to a level similar to that of the 0.18µm node. This has been achieved by the use of furnace gate dielectric with physical dielectric thickness slightly less than that of the 0.18µm node.

In the second part of this chapter, the authors investigated the effects of geometry scaling on the $1/f$ noise of 0.13µm LSP transistors. The relationships between S_{Id} and width and length scaling have been studied. In general the scaling trend follows the $S_{Id} \propto \frac{W}{L^3}$ rule. From the plot of S_{Vg} versus $1/WL$, a large dispersion in noise level for devices with gate area < 1 µm^2 has been observed. This scattering can be as much as 2 orders of magnitude for devices with the smallest gate area. The phenomenon has been attributed to the existence of Lorentzian-like spectra for small area transistors.

Finally, the authors investigated the effects of varying W/L ratio on the normalized S_{Id}. It has been demonstrated that $(S_{Id} \times WL) \propto \left(\frac{W}{L}\right)^2$ holds true for deep submicron devices.

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CHAPTER 8
CONCLUSIONS AND RECOMMENDATIONS

8.1 Conclusions

The main thrust of this thesis is to study the effects of technology scaling on the 1/*f* noise performance of deep submicron CMOS transistors. The study has been performed on conventional oxide transistors for the mature technology, namely the 0.35μm node, and nitrided oxide transistors for the more advanced technologies, which include the 0.25μm, 0.18μm and 0.13μm nodes.

The first part of this work focus on the effects of migrating from a single thickness gate oxide growth process to a dual thickness gate oxide growth process on the 1/*f* noise behaviour of deep submicron NMOS and PMOS transistors. The study has been carried out using multi-finger NMOS and PMOS thin gate oxide transistors optimized for high frequency wireless applications. The results reveal that both thin gate oxide NMOS and PMOS transistors from the dual gate oxide thickness process show a maximum of an order reduction in the current noise spectra, as compared to their counterparts from the single gate oxide thickness process respectively. This reduction has been attributed to the fact that thin gate oxide transistors from the dual thickness gate oxide process undergo an additional cleaning cycle thereby leading to lower interface trap densities. The verification for this phenomenon has been achieved via the extraction of the Hooge's parameter, comparing the charge-pumping current levels and the nitrogen profiles for thin gate oxide transistors derived from the single thickness and the dual thickness gate oxide processes respectively. Hence the dual gate oxide thickness process will be the state-of-the-art for the implementation of low noise circuit designs and it forms the baseline process for

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subsequent work in the later chapters. Furthermore, the study also reveals that the number fluctuation with correlated mobility fluctuation model seems to best describe the $1/f$ noise performance of the transistors being investigated.

The second part of this work focus on the effects of technology downscaling, especially a higher degree of gate oxide nitridation, on the $1/f$ noise behaviours of deep submicron NMOS and PMOS transistors. Thorough studies of technology scaling on the $1/f$ noise characteristics of p- and n-channel transistors from four advanced CMOS technologies with dual gate oxide thickness have been reported. The results show that the thin gate oxide p- and n-channel transistors' S_{Id} increase by approximately 2 and 1.5 orders of magnitude respectively when scaling from 0.35μm to 0.13μm technologies. This increase has been attributed to the changeover from thermal oxides to nitrided oxides from 0.25μm and below. The magnitude of increase is influenced by the degree of nitridation. P-channel transistors are more susceptible to the interface traps introduced by the nitridation process because the oxide traps tends to pile up near the valence band [23], [112], thereby facilitating an easier exchange of carriers between the channel region and the trap states for the PMOS transistors. Furthermore, the experimentally observed $1/f$ noise trends for both the p- and n-channel transistors correlate well with the BSIM3v3 $1/f$ noise model, which has been developed based on the number fluctuation with correlated mobility fluctuation model.

The third part of this work attempts to compare and contrast the effects of gate oxide nitridation on the $1/f$ noise behaviours of thick gate oxide nitrided I/O p- and n-channel transistors from scaled technologies against the architecturally equivalent non-nitrided thin gate oxide p- and n-channel transistors from the mature 0.35μm technology. The term "architecturally equivalent" here implies that the I/O transistors have the same aspect ratio

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(W/L = 20/0.35), approximately equivalent amount of channel and source/drain dopants, and an oxide thickness of about 7nm. The results show that the I/O p- and n-channel transistors' S_{Id} increase by a maximum of approximately 1.25 orders of magnitude. This increase in S_{Id} has been attributed to the thin gate oxide nitridation process, since this processing step takes place after the completion of the thick gate oxide growth module. Again the experimental $1/f$ noise trends have been verified with simulations using the BSIM3v3 $1/f$ noise model.

The fourth part of this work aims to study the effects of varying degree of gate oxide nitridation arising from scaling across technologies, as well as different process flavours offered within the 0.13μm technology, on the $1/f$ noise behaviours of deep submicron thin gate oxide NMOS transistors. The results show that a higher degree of gate dielectric nitridation with technology downscaling from 0.35μm node to 0.13μm G node has resulted in a severe degradation of the $1/f$ noise performance of thin gate oxide n-channel transistors by approximately 3 orders of magnitude. For the 0.13μm technology node, three different process flavours, namely the G process flow, the LV/HP process flow and the LSP process flow, have been investigated. The findings show that the employment of LSP transistors in 0.13μm node will lower the $1/f$ noise spectra by approximately 2 orders of magnitude as compared to the 0.13μm LV/HP transistors, which gives the worst $1/f$ noise performance among the three different process flavours. This has been achieved by the use of furnace gate oxide with physical oxide thickness slightly less than that of the 0.18μm node. This finding provides a significant respite for circuit designers with noise sensitive designs, as it has been demonstrated in our work [99], [106] that technology downscaling aggravates the $1/f$ noise performance of CMOS transistors.

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Finally the last part of this thesis examines the effects of channel widths, channel lengths, active gate areas and aspect ratios scaling on the 1/*f* noise behaviours of 0.13μm thin gate oxide LSP n- and p-channel transistors. The results show that in general the scaling trend follows the $S_{Id} \propto \frac{W}{L^3}$ rule. For devices with gate area < 1 μm^2, a large dispersion in the 1/*f* noise level has been observed. This phenomenon has been correlated to the existence of Lorentzian-like spectra for small geometry transistors. The investigation of the effect of scaling the transistor's aspect ratio reveals a $(S_{Id} \times WL) \propto \left(\frac{W}{L}\right)^2$ dependence.

8.2 Recommendations for Future Research

Three main suggestions for further research are presented here:

Firstly the aggressive scaling of CMOS technology has led to the thinning of the SiO_xN_y gate dielectric to thickness of 16Å and below. One of the major concerns associated with the dielectric scaling is the increasingly significant gate leakage current levels leading to substantial stand-by power consumption. Hence there is immense interest in the search for alternative gate dielectric materials with higher relative permittivities (κ). The potential materials under consideration include zirconium oxide (ZrO_2), hafnium oxide (HfO_2), lanthalum oxide (La_2O_3) and aluminium oxide (Al_2O_3). Hence this current work can be extended to study the 1/*f* noise behaviours of transistors fabricated using high-κ gate dielectric materials.

Secondly as mentioned in the paragraph above that gate leakages will dominate for dielectric thickness of 16Å and below, hence it is imperative to modify the existing

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compact $1/f$ noise models to account for the gate leakage current noise manifested by ultra-thin gate oxide CMOS transistors. However in order to ensure that the modified noise models are still suitable for implementation in circuit simulators, a sub-circuit implementation involving the addition of a gate leakage related noise source to the existing BSIM model is recommended as the initial approach.

Thirdly due to the aggressive downscaling of technology, the analysis and modelling of RTS in small area sub-micron MOSFETs is gaining importance. The current $1/f$ noise compact models do not account for this phenomenon. Hence this area is an important topic for future research.

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2.	K. W. Chew, K. S. Yeo, S. –F. Chu and Y. M. Wang, "Impact of 0.25 μm Dual Gate Oxide Thickness CMOS Process on Flicker Noise Performance of Multifingered Deep-Submicron MOS Devices," *IEE Proceedings – Circuits, Devices and Systems*, vol. 148, no. 6, pp. 312-317, Dec. 2001.	4
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