Equivalent Circuit Model of High Power Density SiC Converter for Common-Mode Conducted Emission Prediction and Analysis

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***Abstract*—High power density is the primary design consideration for power converters in more electric aircraft (MEA) to meet both space and weight requirements. Therefore, wide bandgap (WBG) semiconductor switching devices, such as SiC, have been chosen to push the switching frequency of the power converter further for size and weight reduction. To meet power quality and conducted emission requirements, a LCL filter is necessary between the converter output and the power grid. With the power switching devices operate at higher frequency, the parasitic effects of various key circuits of the converter cannot be ignored and must be accounted for in the simulation model. This paper describes a complete equivalent circuit model that includes these effects of DC bus-bar, power semiconductor device, gate driver and LCL filter. With the comprehensive model, common-mode (CM) conducted emissions can be predicted and evaluated during the design phase for performance optimization purpose.**

***Index Terms*—High power density converter, LCL filter, CM emissions, high frequency equivalent circuit model.**

I. INTRODUCTION

To be less reliant on fuel and to reduce carbon footprint, adopting more efficient electric technologies in the aerospace industry has been gaining much attention. The backbones of these electric technologies are power converters that connect between loads and power grids. For aerospace applications, high power density converters (HPDCs) are the only solutions for obvious reasons [1]. The pre-requisite for HPDC design is to operate at high switching frequency for power conversion so that sizes of magnetic components that form the bulk of the of the converter, can be reduced. In addition, for standard low temperature applications, it is usual to position the converter close to the machine to reduce EMI. Due to space constraints and high temperature applications, the use of high temperature capable devices forces that the electric starter/generator (ESG) is mounted directly with the power converter on the shaft of the gas turbine engine [2].

With ever-increasing switching frequencies in HPDC design, silicon carbide (SiC) is regarded as the emerging wide bandgap power devices intended for high power density and high temperature applications, such as electric vehicle (EV) and more electric aircraft (MEA) [3]. The ability of SiC devices to switch at high frequency paves the way for SiC power converters in HPDC designs [4, 5] but also generates higher electromagnetic interference (EMI) [6]. During the turn-off transition, the high di/dt leads to a voltage overshoots due to the stray inductance. While in the half bridge circuit, the high dv/dt during the turn-on transition of one transistor affects the complimentary transistor via the Miller capacitance, which may lead to a momentary arm shoot through or crosstalk [4].

Therefore, to model and predict EMI emissions of a SiC power converter is important for EMI mitigation. The common-mode (CM) EMI noise modeling with Si IGBT T-type device noise source and LCL filter propagation path has been developed [7]. An experimental case study on the switching characteristics and CM noise generation of Si and GaN based half-bridge configuration operating in synchronous boost mode has also been studied [8]. Modeling and reduction of conducted EMI of discrete SiC JFETs inverters on insulated metal substrate for motor drive are reported [9]. In addition, a fair amount of EMI modeling work has been carried out [10-12] but there is very little research work focused on a comprehensive high frequency equivalent circuit model of integrated SiC MOSFET converter for EMI analysis, including gate driver, DC bus bar, power semiconductor device and LCL filter. This paper aims to develop this comprehensive model for conducted emission prediction and analysis.

II. HIGH FREQUENCY MODELLING OF SIC HPDC

There are four main circuit blocks in a HPDC, namely gate driver, DC bus bar, power semiconductor device and LCL filter. Fig. 1 shows the high frequency equivalent circuit of the complete HPDC with the above-mentioned circuit blocks.

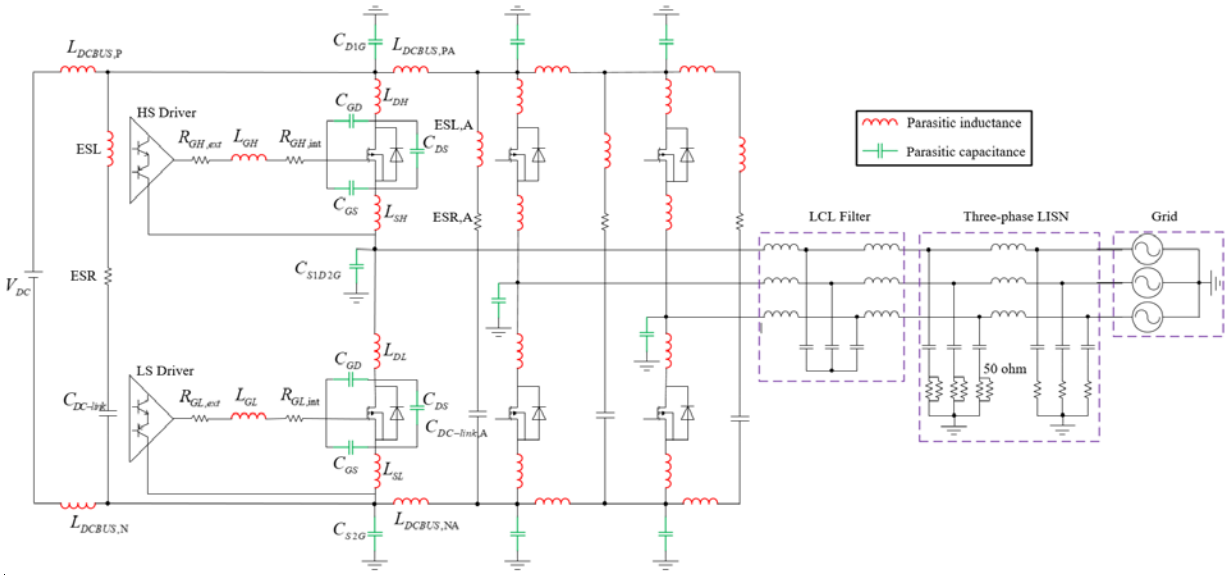

Fig. 1 High frequency equivalent circuit of a HPDC system.

To predict the conducted emission from the HPDC, a three-phase line impedance stabilization network (LISN) is also modelled between the HPDC and the power grid. Fig. 2 shows an in-house designed 50-kW HPDC. It will be used as a design example for the modeling and simulation to be presented in this paper.

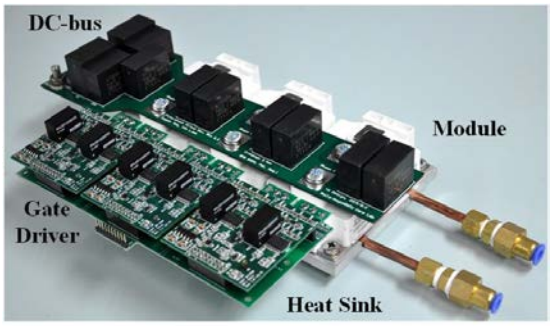

Fig. 2. Prototype of the in-house designed 50-kW HPDC.

The equivalent circuit model of each of the four main circuit blocks will be briefly described in this section.

A. Gate driver

The parasitic element of the gate driver is mainly contributed by the inductance L_G that consists of parasitic inductances of driver chip, layout and module. Besides the gate inductance, the gate resistance R_G also has an influence on the switching characteristics of SiC power module. Both parameters have to be optimized as a trade-off between switching loss and EMI [4].

B. DC bus bar

A typical equivalent circuit of a DC bus bar is shown in Fig. 3, which includes the conductor's resistance and inductance, as well as the stray capacitance between conductors [13]. The stray capacitance is usually very small and its effect can only be felt at very high frequency [14]. Usually, the DC bus bar structure is designed such that it has low inductance in the range of several to tens of nH. This is to minimize the voltage spike during the turn-off transition of the switching devices [13, 15].

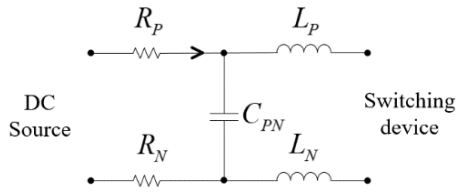

Fig. 3 DC bus bar model.

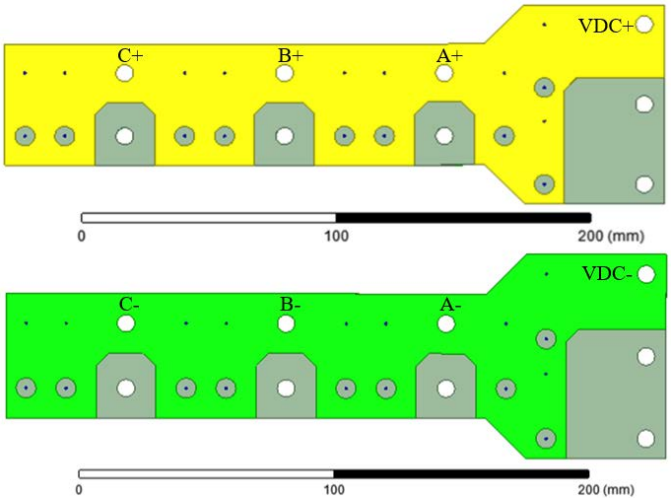

Fig. 4 DC bus bar structures.

Table I Extracted inductances of the DC bus bar.

Parameters	Value
L_{A+A-}	4.70 nH
L_{B+B-}	4.72 nH
L_{C+C-}	4.80 nH
L_{DC+DC-}	34.97 nH

Fig. 4 shows the actual design of the DC bus bar of the HPDC shown in Fig.2. Both the thickness of positive and negative PCB copper thickness are 0.8 mm and the thickness of the substrate is 1.6 mm with a creepage of 2.4 mm. The inductances of various parts of the DC bus bar are extracted using ANSYS Q3D [16] with their respective values presented in Table I.

ANSYS Q3D is a 3-D quasi-static electromagnetic field solver to extract the resistance, inductance, capacitance and conductance of an interconnect structure.

C. Power semiconductor device

The SiC power module (Wolfspeed CAS120M12BM2) is chosen for the HPDC design. The device's terminal capacitances are taken from the datasheet at 750V with C_{GS} = 6.26 nF, C_{GD} = 37 pF and C_{DS} = 900 pF. The trans-conductance g_m = 53.8 S at 120 A and the on-resistance R_D = 13 mΩ [4]. The drain inductance (or converter loop inductance) L_D, consists of inductances of DC-link capacitor, layout and module. This inductance has a direct impact on voltage overshoot due to *di/dt*. It also determines the ringing frequency of the gate voltage spike. The common source inductance L_S, is the trace between external source terminal and source pad of die. In addition, the parasitic capacitances from drain and source sides of the switching device to ground have to be extracted for CM emission analysis. For each SiC MOSFET module, there are three major parasitic capacitances C_{D1G}, C_{S1D2G}, and C_{S2G}, which contribute to the path for the circulation of CM conducted emission. These capacitances can be measured with an impedance analyzer. With the actual module package shown in Fig. 5, they can be modeled and extracted by using Ansys Maxwell [17] as shown in Fig. 6, and ANSYS Maxwell is an electromagnetic solver that uses finite element analysis (FEA) to extract parasitic elements of a device packaging.

The capacitances of C_{D1G}, C_{S1D2G}, and C_{S2G} extracted based on measurement and simulation are given in Table II. The simulated and measured capacitances are in close agreement with slight discrepancy.

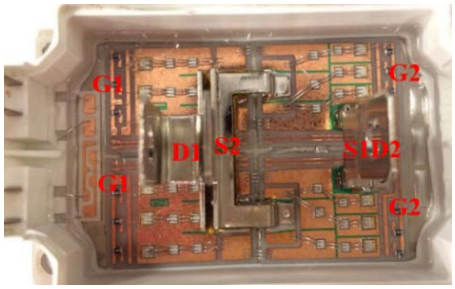

Fig.5 SiC half-bridge module CAS120M12BM2 with its packaging opened.

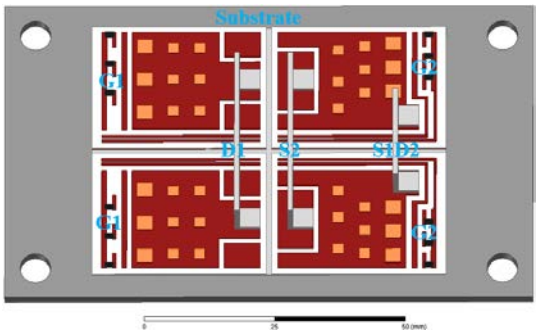

Fig. 6 Extraction of stray capacitance of drain and source to substrate using Ansys Maxwell.

Table II Comparison of simulated and measured parasitic capacitances of switching device.

Parameters	Simulated	Measured
C_{D1G}	220.0 pF	218.1 pF
C_{S1D2G}	240.7 pF	238.7 pF
C_{S2G}	93.2 pF	92.2 pF

D. LCL filter

The LCL filter is needed for power quality and conducted emission compliance. The equivalent circuit of the LCL filter for each phase can be modelled as several cascaded RLC parallel circuits [7], as shown in Fig. 7. The number *n* denotes the number of stages needed to resemble the filter's measured impedance frequency response with resonances and anti-resonances for a given frequency range of interest. With *n* = 3, the modeled impedance response matches well with the measured impedance response for each phase of the LCL filter, as shown in Fig. 8. The resonant (peak) and anti-resonant (valley) frequencies are determined as follows:

$$f_{res1} = \frac{1}{2\pi\sqrt{L_1 C_1}} \quad (1)$$

$$f_{anti-res1} = \frac{1}{2\pi\sqrt{L_2(C_1+C_2)}} \quad (2)$$

$$f_{res2} = \frac{1}{2\pi\sqrt{L_2 C_2}} \quad (3)$$

$$f_{anti-res2} = \frac{1}{2\pi\sqrt{L_3(C_1+C_2+C_3)}} \quad (4)$$

$$f_{res3} = \frac{1}{2\pi\sqrt{L_3 C_3}} \quad (5)$$

where, L_1 = 63.25 µH, R_1=2535.3 Ω, C_1=160 pF; L_2=0.5 µH, R_2=180.0 Ω, C_2=453 pF; and L_3=0.08 µH, R_3=130.0 Ω, C_3=440 pF.

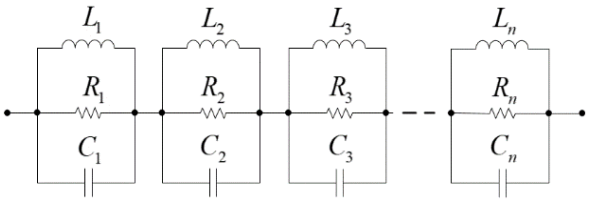

Fig. 7 Equivalent circuit model of the LCL filter.

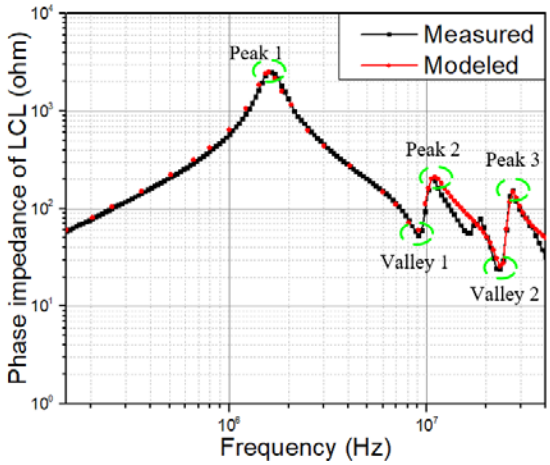

Fig. 8 Comparison of measured and modelled impedance frequency responses of the LCL filter.

III. CM EMISSIONS PREDICTION

Table III lists the parameters of the two-level three-phase SiC

HPDC converter shown in Fig. 2. With these parameters and the extracted parasitic elements described earlier, the full HPDC equivalent circuit is modeled and simulated for the prediction of CM conducted emissions, as shown in Fig. 9. The CM conducted emission is determined by calculating the average value of the noise currents in the 50 Ω terminations of the three-phase LISN. For the simulation, the frequency range of interest is from 150 kHz to 152 MHz, as required by aerospace EMC standard RTCA DO-160 [18]. The first peak (peak #1) in the CM emission can be estimated by the total CM inductance of LCL filter and the total CM capacitance of the switching devices to ground, as given in (6):

$$f_{peak1,CM} = \frac{1}{2\pi\sqrt{(L_1+L_2+L_3)(C_{D1G}+C_{S1D2G}+C_{S2G})}} \quad (6)$$

The valleys (valleys #1 and #2) and peak (peak #2) in CM emissions correlate well with the LCL filter impedance response, as shown in Fig. 8.

Table III Parameters used for the high frequency equivalent circuit model of the HPDC

Parameters	Value
DC bus bar inductance between two adjacent phases	9.4 nH
Drain inductance	7 nH
Common source inductance	0.8 nH
Gate inductance	10 nH
Gate external resistor	10 Ω
DC input voltage	750 V
Switching frequency	100 kHz

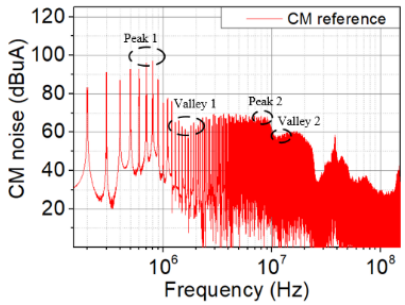

Fig. 9 Simulated CM conducted emissions.

A. Impact of gate driver inductance and resistance

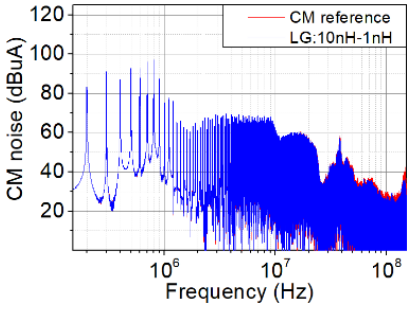

Fig. 10 Simulated CM conducted emissions (gate inductance reduces from 10 nH to 1 nH).

To evaluate the impact of the gate inductance, Fig. 10 shows the simulated CM emissions when the gate inductance reduces from 10 nH to 1 nH with the external gate resistance remained at 10 Ω. It indicates that CM emission has reduced slightly marginally above 30 MHz with reduced gate inductance, since the gate inductance is directly related to the voltage overshoot [4], which can be explained by the switching waveforms as shown in Fig. 11. The drain-source voltage and the drain current are varied slightly with the reduction of the gate inductance.

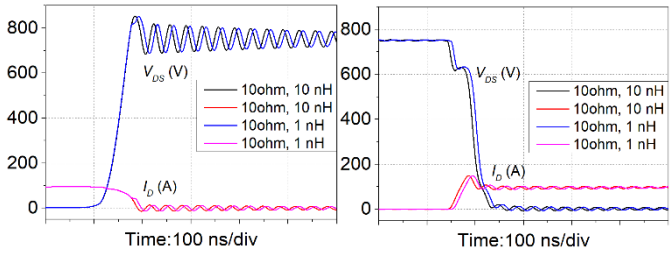

Fig. 11 Simulated switching waveforms with different gate inductances: turn-off (left) and turn-on (right).

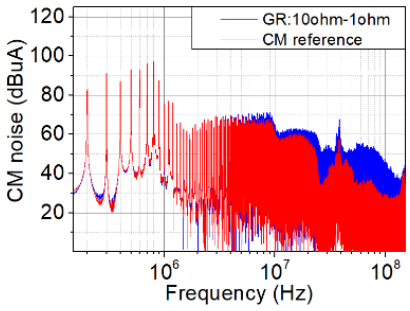

Fig. 12 Simulated CM conducted emissions (gate external resistance reduces from 10 Ω to 1 Ω).

To evaluate the impact of external gate resistance, it is reduced from 10 Ω to 1 Ω with the gate inductance remaining at 10 nH. Fig. 12 shows that the simulated CM conducted emissions have increased significantly above 10 MHz, since a smaller gate resistance provides a low impedance path for C*dv/dt* during the turn-off transition, and also shortens the transition times of the switching waveforms, as illustrated in Fig. 13. Although higher gate resistance is more favorable for reduction of conducted emission, it also incurred higher losses in the switching devices. Therefore, the selection of the gate resistor value should be optimized between converter efficiency and EMI compliance.

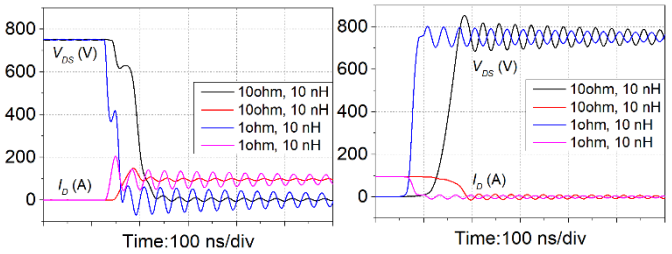

Fig. 13 Simulated switching waveforms with different gate resistors: turn-off (left) and turn-on (right).

B. Impact of DC bus bar inductance

The DC bus bar with higher parasitic inductance increases the loop inductance of the switching device, which will have an impact on conducted emission. The CM conducted emissions, as presented in Fig. 14, are slightly lower with smaller DC bus inductance, especially above 100 MHz. Therefore, a control of the parasitic inductance of DC bus bar is important if EMI of HPDC at very high frequency with higher switching frequency is of interest.

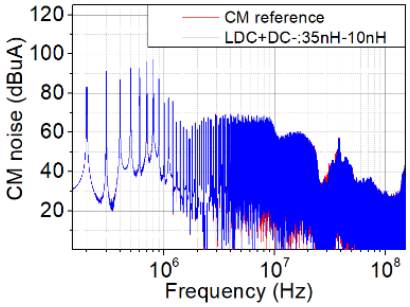

Fig. 14 Simulated CM conducted emissions (DC bus inductance of two adjacent phases reduces from 9.4 nH to 4 nH).

C. Impact of parasitic inductance and capacitance of power semiconductor device

The parasitic parameters of power semiconductor, such as drain inductance, common source inductance, drain-to-gate capacitance, gate-to-source capacitance, and drain-to-source capacitance also have some impacts on conducted emission.

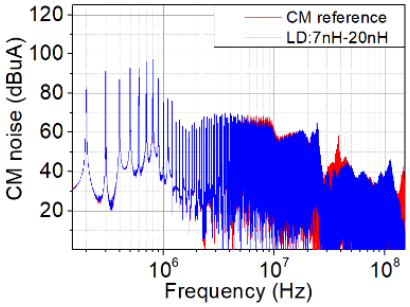

Fig. 15 Simulated CM conducted emissions (drain inductance from 7 nH to 20 nH).

Higher drain inductance increases conducted emission at around 20 MHz, as shown in Fig. 15. This is expected as higher drain inductance produces larger voltage overshoot. The change of the drain inductance from 7 nH to 20 nH also shifted the resonant frequency of the conducted emission spectrum.

Fig. 16 presents the simulated conducted emission with the increase of source inductance. The common source inductance with the other parasitic parameters also shifted the resonant frequency of the conducted emission spectrum.

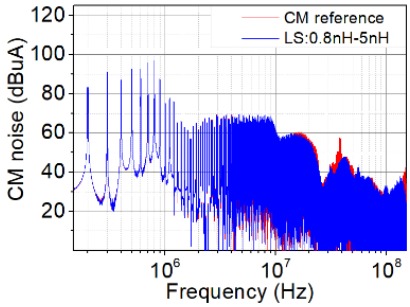

Fig. 16 Simulated CM conducted emissions (common source inductance increases from 0.8 nH to 5 nH).

To investigate the effects of parasitic capacitance on conducted emissions, the device's parasitic capacitances are changed with C_{GS} = 20 nF, C_{GD} = 0.1 nF and C_{DS} = 2 nF at 750V.

Figures 17, 18, 19 show that CM emissions have reduced visibly after several MHz with the increases of C_{gd}, C_{gs}, and C_{ds}. Higher C_{gd} decreases the *dv/dt* at both turn-on and turn-off transitions, higher C_{gs} decreases the *di/dt* at both turn-on and turn-off transitions, and higher C_{ds} decreases the *dv/dt* at turn-off transition. Therefore, these high frequency conducted emissions can be reduced by the snubbers such as RC, RCD, and so on, which are parallel with C_{gd}, C_{gs}, and C_{ds}. On the other hand, the switching losses are expected to increase with higher device capacitances, which again is a trade-off between device losses and EMI compliance.

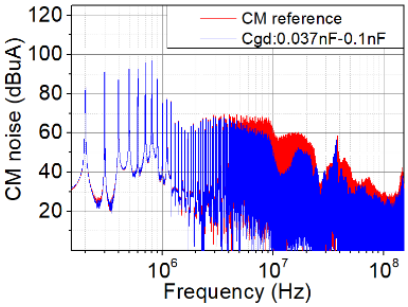

Fig. 17 Simulated CM conducted emissions (drain-to-gate capacitance *Cgd* increases from 0.037 nF to 0.1 nF).

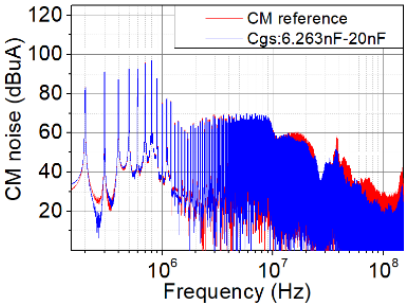

Fig. 18 Simulated CM conducted emissions (gate-to-source capacitance *Cgs* increases from 6.263 nF to 20 nF).

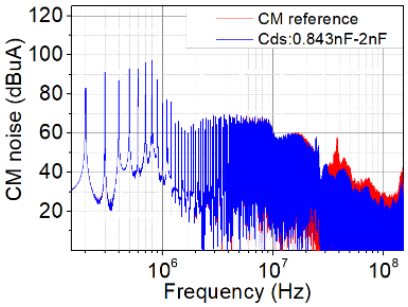

Fig. 19 Simulated CM conducted emission (drain-to-source capacitance *Cds* increases from 0.843 nF to 2 nF).

D. Impact of switching frequency

Besides the impact of parasitic effects of all the key circuits on conducted emission, switching frequency of the HPDC also have some impact on conducted emission. Fig. 20 show the impacts of the switching frequency. As expected, lower switching frequency leads to lower conducted emission. However, the switching frequency can be optimized between the size and weight of LCL filter and the efficiency of the whole converter system.

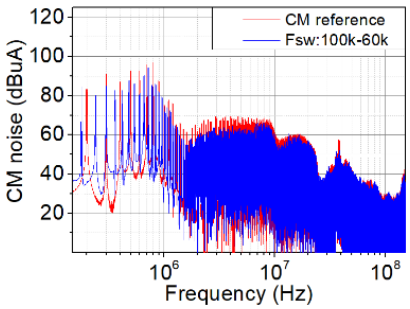

Fig. 20 Simulated CM conducted emissions (switching frequency reduces from 100 kHz to 60 kHz).

IV. Conclusions

A comprehensive equivalent circuit of a HPDC for DC to three-phase AC conversion has been developed. With all the parasitic elements of the major circuit blocks included in the equivalent circuit model, the impacts of these elements on both CM conducted emissions can be systematically evaluated during the design phase. Such an evaluation through simulations allows the designers to gain insights on how each of these parameters can affect conducted emission of the HPDC so that early design measures can be taken into account before the prototype is constructed, which will reduce the product design time and cost.

Acknowledgements

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