NANYANG TECHNOLOGICAL UNIVERSITY

Analysis and Design of Analogue Class D Amplifier Output Stages

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ABSTRACT

It is well established that Class D audio amplifiers have higher power efficiency compared to classical linear amplifiers (Class A, Class B and Class AB) due to the fact that the transistors in their output stage operate either in the cut-off region or in the triode region. As the output stage typically dissipates the highest power of all circuit blocks in audio amplifiers, the overall power efficiency of amplifiers largely depends on the design of the output stage.

The optimization of the output stage based on CMOS (embodying the *p*-channel-cum-*n*-channel inverter) has been reported in literature. These output stages are limited only to low voltage (~5V) applications due to the low breakdown voltage of CMOS. In this dissertation, we investigate the power dissipation mechanisms of the High Voltage MOS (HVMOS) output stage in half bridge configuration (the half bridge can be easily extended to the full bridge) and the Double-diffused MOS (DMOS) output stage in full bridge configuration, and apply protection circuits to the output stages for higher voltage (~20V) applications. We derive analytical expressions to determine their power efficiencies and establish a methodology to optimize the channel width of the output stages for optimum power efficiency. We also propose a small non-overlapping logic circuit to reduce the possibility of short-circuit current.

The derived expressions depict the parameters that affect power efficiency, and are insightful to designers to design the output stage for optimum power efficiency in view of IC area. The analytical results are verified against Cadence (Spectre) computer simulations for both DMOS and HVMOS, and on the basis of measurements on an IC for DMOS. The DMOS output stage is shown to offer higher power efficiency than the HVMOS output stage due to its lower on-resistance and lower capacitance.

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List of Abbreviations and Symbols

$\sum\Delta$	Sigma-Delta
α	$W_P/W_{n.}$
β	Gain factor of MOS Transistor
η	Power efficiency
BCCD	Bang-bang Control Class D
CDA	Class D Amplifier
CMOS	Complementary MOS
C_d	Lumped drain capacitance
C_g	Lumped gate capacitance
C_{gd}	Gate-drain overlap of drift region in DMOST/HVMOST
C_{gdo}	Gate-to-drain capacitance per unit gate width
C_{gso}	Gate-to-source capacitance per unit gate width
C_j	Zero-biased p-n junction area capacitance
C_{jsw}	Zero-biased p-n junction periphery capacitance
C_{OUT}	Total output capacitance
C_{OX}	Oxide capacitance per unit gate area
C_P	Parasitic capacitance
C_{pad}	Bond pad capacitance
C_s	Source capacitance
D	Duty Cycle
DMOS	Double-diffused MOS
EMI	Electro-Magnetic Interference
ε_{OX}	Permittivity of gate oxide
FBD	Fold-Back Distortion
f_c	Carrier frequency
f_s	Input signal frequency
HVMOS	High-Voltage MOS
IC	Integrated Circuit
I_{DS}	Drain-to-source current
I_{LIM}	Over-current limit
I_{mean}	Mean value of short circuit current
I_o	Maximum output current (V_{DD}/R_L)
i_o	Output load current
L	Channel length
L_n	Channel length of the nMOST
L_p	Channel length of the pMOST
L_{DS}	Length of the source or drain area
LDMOS	Lateral DMOS
MOS	Metal-Oxide Semiconductor
MOST	MOS Transistor
M	Modulation Index
PDM	Pulse Density Modulation

PSRR	Power Supply Rejection Ratio
PWM	Pulse Width Modulation
P_C	Power dissipation due to parasitic capacitance
P_{DISS}	Total power dissipation
P_{OUT}	Output power
P_{pkg}	Power loss due to package resistance
P_r	Power dissipation due to on-resistance
P_S	Power dissipation due to short circuit current
P_{tot}	Total power dissipation in terms of width, W
R_L	Load resistance
R_{ctn}	n-type contact resistance per contact
R_{ctp}	p-type contact resistance per contact
R_n	Source and drain area resistance per square of an nMOST
R_{on}	On-resistance
R_p	Source and drain area resistance per square of a pMOST
R_{pkg}	Package resistance
r_b	Body resistance
r_c	Contact resistance
r_{ch}	Channel resistance
r_d	Drain resistance
r_{epi}	Drift region epitaxial resistance in DMOST/HVMOST
r_s	Sheet resistance
r_{so}	Source resistance
s	Skew factor
τ	Rise or fall time of a PWM signal
T_s	Period
THD	Total Harmonic Distortion
t	Tapering factor of a string of inverters
t_{OX}	Gate oxide thickness
μ	Carrier mobility
μ_n	Electron mobility
μ_p	Hole mobility
VDMOS	Vertical DMOS
V_c	Triangular carrier signal
V_{DS}	Drain-to-source voltage
V_G	Gate voltage
V_{GS}	Gate-to-source voltage
V_s	Input signal
V_{th}	Threshold voltage of a MOST
W	Channel width
W_n	Channel width of the nMOST
W_{opt}	Optimized width
W_p	Channel width of the pMOS

Chapter 1

Introduction

1.1 Motivation

This research programme is part of an industrial collaboration between NTU and a multinational semiconductor company, pertaining to the analysis, design and realization of analogue Class D audio Amplifiers (CDAs). The research work herein pertains to a conventional mid-voltage (20V) CDA design (based on pulse width modulation, see later) but with the output stage designed based on two different fabrication technologies - Double-diffused MOS (DMOS) technology and High-Voltage MOS (HVMOS) technology (as opposed to the more prevalent CMOS technology for typical low-voltage low-power applications).

At this juncture, although audio amplifiers in the audio market remain largely dominated by linear amplifiers (Class AB amplifiers), CDAs are increasingly gaining acceptance over the entire span of amplifiers, from micro power to high power amplifiers. The primary reason for the increasing preponderance of CDAs is largely due to their higher power efficiency (the ratio of the useful power delivered to the load over the total input power) over their linear counterparts, as the output transistors therein function only in the ohmic or cut-off regions (as opposed to the active regions in the linear amplifiers).

The advantages of higher efficiency are very worthwhile. They include an increased lifespan of remote power supplies (batteries) and smaller form factor, for portability and aesthetic reasons, arising from the elimination of the heat sink in many cases or at least a significantly reduced heat sink size.

Despite the very worthy high power efficiency advantage, some sections of the audio industry remains somewhat resistant to adopt CDAs largely due to the higher cost involved when compared to the classical Class AB realizations. The higher cost is usually due to the larger number of external components and a larger required silicon area – mainly due to the large (*W/L*) transistors in the output stage to keep the on-resistance of the output stage low (for high power efficiency, see later). These added costs may somewhat defeat the primary advantage (increased power efficiency) of the CDA.

As the output stage dissipates the most power in most audio amplifiers, the overall power efficiency of the amplifier largely depends on the design of the output stage. In most CDA designs, the size of the output stage easily occupies half or more of the entire integrated circuit (IC) area. In view of this, there is much motivation to research on the effects of different output stage configurations on power efficiency, and design methodologies to optimize the output stage with a balance between power efficiency and IC area.

While investigations into the power dissipation mechanisms and optimization for low voltage CMOS output stage have already been reported [Chang, *et.al.*, 2000], there is a lack of literature on the same (output stage) operating at higher voltage, and particularly in DMOS and HVMOS technology; nonetheless there are high voltage DMOS and HVMOS CDA designs reported in literature.

The considerations for the design of the output stage for low voltage ($\leq$ 5V) and higher voltage (20V range) applications are very different. A higher voltage renders the output stage more susceptible to breakdown and damage due to higher power dissipation and this makes protection a more important consideration (when compared to a lower voltage application). With a higher supply voltage, as it is expected that the power dissipation will increase, the output stage with a small R_{on} is required to keep the power dissipation within the IC low. Moreover, as the common low voltage CMOS output stage cannot be used for 20V application due to its process limitations (being unable to tolerate high

voltage due to breakdown), a HVMOS output stage or a DMOS output stage would be required.

When HVMOS is compared to DMOS, DMOS has the advantage of a short channel length (<0.5µm) with high breakdown voltage through the double-diffusion fabrication and this advantage translates to a lower R_{on} per unit transistor area.

At this juncture, the design of a DMOS- or HVMOS-based output stage appears to be largely empirical, where the rule-of-thumb is often applied. The rule-of-thumb is to design the R_{on} of the output stage to be as small as tolerable and the typical R_{on} is 0.2 - 0.3 Ω for an 8 Ω load. From a simplistic cost perspective, the smaller the R_{on}, the larger is the IC area required for the output stage, and hence, increased cost.

In view of the fact that the size of the IC area dedicated to the output stage is the major cost factor in CDA realizations, it is of interest to analytically determine the parameters/mechanisms that determine R_{on}, the effects of R_{on} on the power efficiency in a DMOS/HVMOS output stage realization and to investigate if the power efficiency can be optimized in view of the IC area.

1.2 Objectives

The overall objective of this M.Eng research programme is to establish a systematic analytical method to design and optimize the Class D output stage for mid-voltage (20V, for the application of home television sets) in DMOS and in HVMOS technology, for high power efficiency and low cost (small and realistic IC area). This involves:

(i) The design of a complete CDA output stage with protection circuits.

(ii) An investigation into different output stage configurations (half and full bridge) and the effects on power efficiency.

(iii) An investigation into power loss mechanisms in the DMOS output stage of Class D amplifiers to determine their output stage efficiencies. This analytical work includes the derivation of analytical expressions to model the mechanisms.

(iv) Following on (iii), an investigation of the same mechanisms in the HVMOS output stage of Class D amplifiers to determine their output stage efficiencies. As in (iii), the analytical work includes the derivation of analytical expressions to model the mechanisms.

(v) Following on (iii), the optimization of the DMOS output stage in Class D amplifiers to achieve high power efficiency in view of IC area. This includes the derivation of analytical expressions to determine the optimized width (W) of the output stage power transistors.

(vi) Following on (iv), the optimization of the HVMOS output stage in Class D amplifiers to achieve high power efficiency in view of IC area. As in (v), this includes the derivation of analytical expressions to determine the optimized width (W) of the output stage power transistors.

(vii) The verification of the analytical derivations in (i) - (vi) above against Cadence (Spectre) computer simulations for both the DMOS and HVMOS, and against measurements on a CDA IC embodying a DMOS output stage fabricated using a proprietary process.

1.3 Contributions

The contributions made in this research programme are the results of the objectives outlined above. Specifically, they are:

(i) Design of a simple non-overlapping logic circuit to reduce the possibility of short-circuit current in a CDA output stage.

(ii) Derivation of the mechanisms of power dissipation and of analytical expressions of these mechanisms and ultimately, the overall power dissipation and power efficiency of a DMOS output stage for Class D amplifiers.

(iii) Derivation of the mechanisms of power dissipation and of analytical expressions of these mechanisms and ultimately, the overall power dissipation and power efficiency of a HVMOS output stage for Class D amplifiers.

(iv) Following on (ii), establishment of a systematic analytical method to design and optimize the mid-voltage DMOS Class D output stage for high power efficiency in view of IC area.

(v) Following on (iii), establishment of a systematic analytical method to design and optimize the mid-voltage HVMOS Class D output stage for high power efficiency in view of IC area.

The contributions herein are significant as they provide insight to a CDA designer on the various parameters available to design the output stage to meet given specifications for mid-voltage applications.

1.4 Organization of Dissertation

This dissertation is organized as follows. Chapter 1 presents the introduction and overview of the project, including the motivation, objectives and contributions.

Chapter 2 presents a literature review of power audio amplifiers. The classical linear amplifiers include the well-known classical Class A, Class B and Class AB and the less-known Class C, Class E, Class G and Class H. As the main theme of this research

pertains to the CDA, the review of CDA is emphasized. This includes the different modulators used, particularly the pulse width modulation (PWM) and the pulse density modulation (PDM). Different output stage configurations and their effects on power efficiency are also reviewed. Finally, the power dissipation mechanisms and power efficiency of a low voltage CMOS output stage are reviewed.

In chapter 3, we discuss the challenges of operating the CDA output stage at higher voltage (20V range) which includes the protection circuits needed in practice. This is followed by a study of the DMOS technology and its output stage model in full bridge configuration. This model is used to determine the mechanisms of power dissipation and the power losses arising from these mechanisms. The efficiency of the full bridge DMOS output stage is thereafter determined. Finally, we propose an optimization method to optimize the output stage for power efficiency. Our theoretical results are verified with Cadence (Spectre) computer simulation and measurement of IC chip.

In chapter 4, we review the HVMOS technology and design a complete CDA output stage with protection circuits. After that, we employ the analytical model established in chapter 3 to a half bridge HVMOS output stage. We further derive the analytical expressions to determine its power dissipation mechanisms and to design the half bridge HVMOS output stage for optimum power efficiency. This is followed by the verification of the analytical model against Cadence (Spectre) computer simulation. We extend the half bridge model to a full bridge model and compare them based on power efficiency. Finally, this full bridge HVMOS model is used to compare the full bridge DMOS output stage with the full bridge HVMOS output stage, and discuss the practical implications.

The conclusions of the project and future work are drawn in chapter 5.

Chapter 2

Literature Review

This chapter reviews the literature on audio power amplifiers, including the well-known classical linear Class A, Class B and Class AB and the less-known Class C, Class E, Class G and Class H. As the main theme of this research pertains to the CDA, the CDA is reviewed more thoroughly.

As the primary objective of this research programme pertains to the design and optimization of the output stage based on DMOS and HVMOS, this review includes a review of a similar output stage design but is based on low-voltage CMOS. In addition, as the output stage usually contributes a significant power loss, different output stage configurations are reviewed.

2.1 A Review of Classical Linear Power Amplifiers

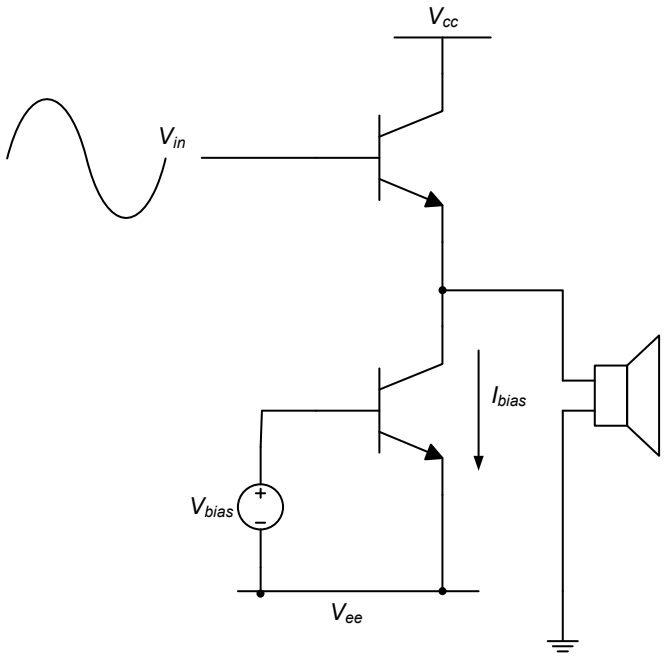
Power amplifiers are traditionally linear amplifiers that are typically classified by the biasing of their output stages. Even with identical input and gain stages, power amplifiers with different output stages exhibit different levels of performance and power efficiency. The most common classes of linear power amplifiers (Class A, Class B and Class AB) will be reviewed in the following sections.

2.1.1 Class A Amplifiers

In a Class A amplifier depicted in Figure 2.1(a), its output power transistors are always turned on regardless of the input signal. This means that even when the output current is zero, the power transistors are always conducting a current, I_{bias}. At the maximum output current I_{max}, a current of $I_{max} + I_{bias}$ will be flowing through the power transistors. With

the transistors of the Class A output stage conducting for the entire cycle, the conduction angle is 360˚ [Sedra, *et.al*., 1998]. Figure 2.1(b) shows the output waveform through an emitter follower which conducts for the entire cycle.

As the transistors are always operating in the active region, the distortion is typically low compared to other classes of linear amplifiers. However, the drawbacks are high power consumption and this yields very low power efficiency. For a single-ended output stage, the maximum efficiency is only 25% [Gray, *et.al*., 2001] while a push-pull stage offers a maximum of 50% [Kashiwagi, 1985]. A pertinent point to note is that practical audio amplifiers do not work at the maximum power all the time. Practically, this means that as the signal swing is on average small during a large portion of the operating time and due to the crest factor (the ratio of the peak value of the waveform over the root-mean square value of the waveform) of audio signals, the efficiency is usually considerably less, for example 5-10%. This can be seen in the power efficiency plot depicted in Figure 2.5 later.



(a)

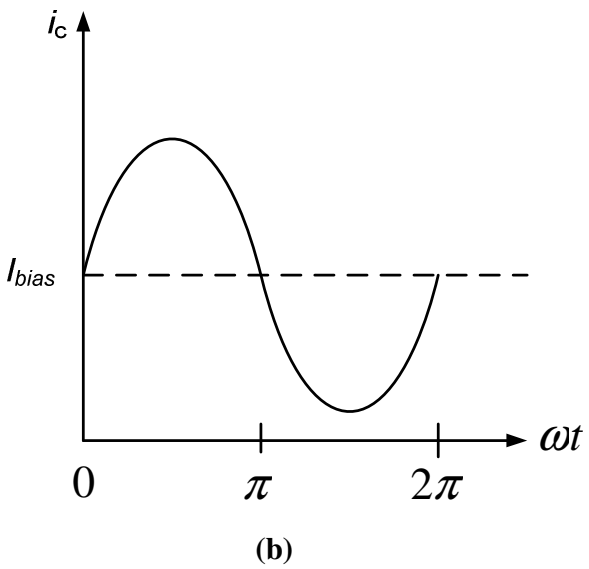
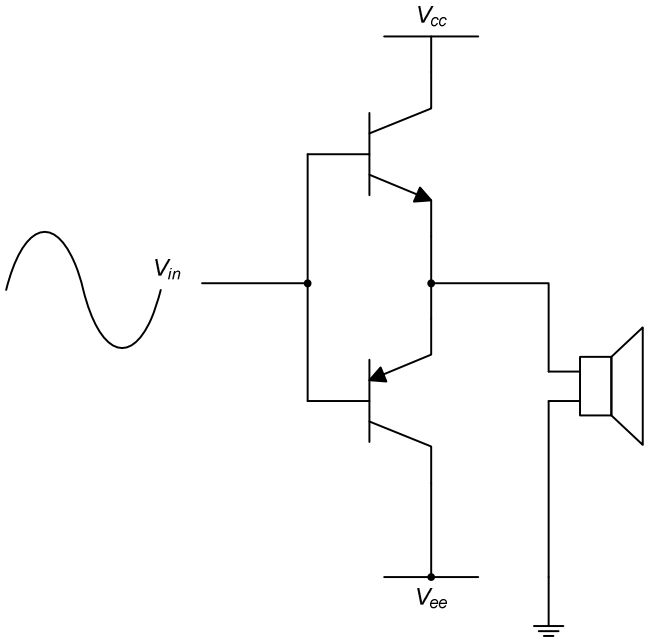


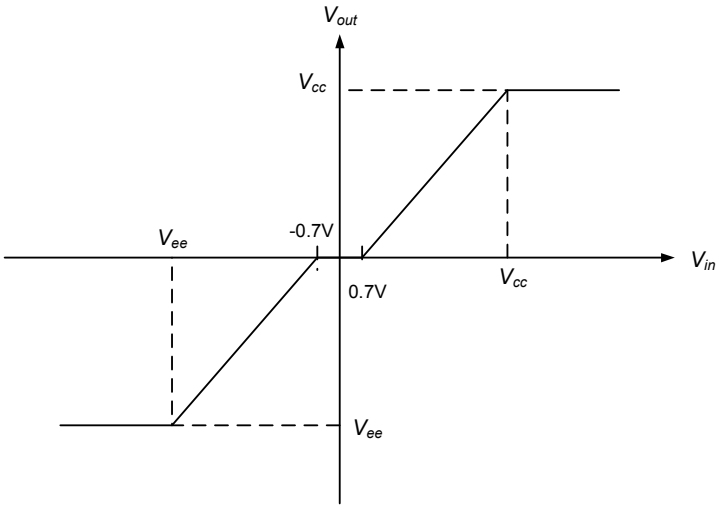
Figure 2.1 (a) Class A Output Stage, and (b) Class A Output Waveform

2.1.2 Class B Amplifiers

Compared to Class A, the Class B topology, depicted in Figure 2.2(a), offers a much higher efficiency at the expense of signal fidelity. The output stage consists of two power transistors that do not turn on simultaneously at any time. Each power transistor only conducts for half a cycle, as shown in Figure 2.2(c), thus having a conduction angle of only 180˚. When the input signal is zero or low (<±0.7V), both transistors are off, as shown in figure 2.2(b). The resulting dead zone contributes to crossover distortion, a severe and often unacceptable problem. The advantage, however, is that the Class B amplifier ensures that no power is wasted when there is no input signal. The maximum theoretical power efficiency for the Class B output stage is 78.5% [Kashiwagi, 1985; Gray, *et.al*., 2001]. However, as in the case of Class A amplifier, the efficiency, in practice, is much lower because of the average low signal swing and crest factor of audio signals. This can be seen in the comparison of power efficiency plot between different classes, depicted in Figure 2.5 later.



(a)



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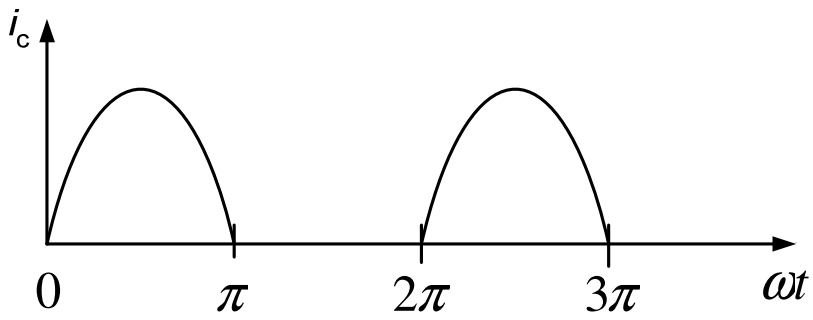
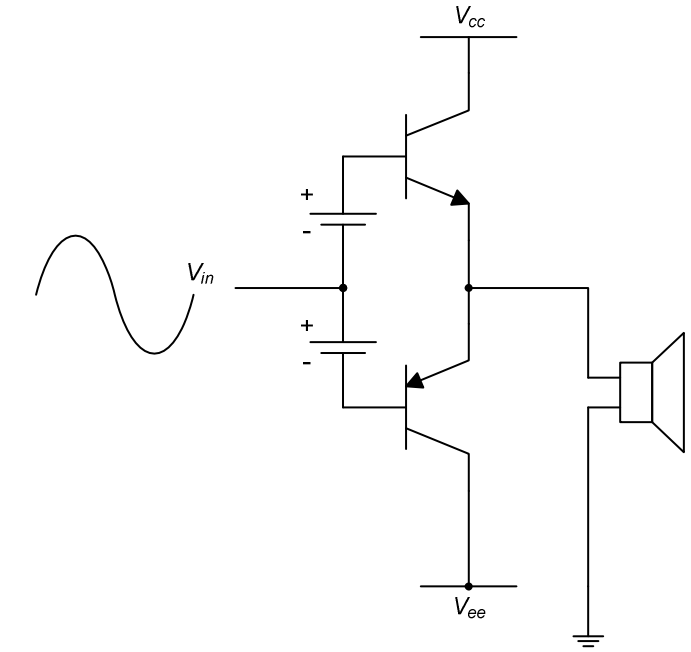


(c)

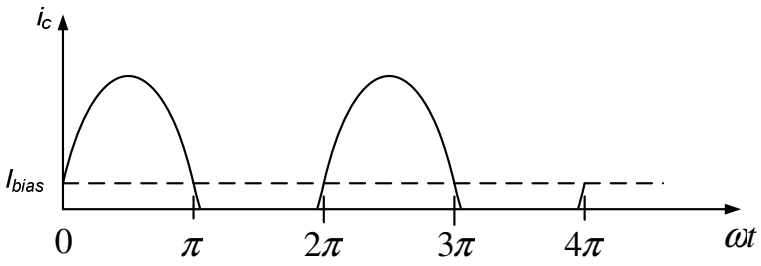
Figure 2.2 (a) Class B Output Stage, (b) Waveform depicting dead zone, and (c) Class B Output Waveform

2.1.3 Class AB Amplifiers

Class AB amplifier, as depicted in Figure 2.3(a), is a compromise between the Class A and Class B topologies. By simply adding a biasing circuitry to the Class B topology, the crossover distortion is drastically reduced while retaining some of the Class B efficiency. The biasing circuitry ensures that at least one of the output transistors is active between -0.7V to 0.7V. Hence, each of the transistors has a conduction angle of slightly more than 180˚ and usually much less than 360˚, as depicted in Figure 2.3(b). Although there is a short period where both transistors are turned on simultaneously, the small sacrifice in power efficiency results in a marked improvement in the fidelity of output signal. This power efficiency – fidelity compromise of the Class AB renders it the most popular solution in the industry today. The power efficiency of the Class AB amplifier is somewhere in between the Class A amplifier and the Class B amplifier (See Figure 2.5).



(a)



(b)

Figure 2.3 (a) Class AB Output Stage, and (b) Class AB Output Waveform

In summary, among the 3 classes of amplifiers discussed, Class A output stage provides the highest signal fidelity but lowest efficiency while Class B output stage gives the highest efficiency but lowest signal fidelity. Class AB output stage is a compromise with its signal fidelity and efficiency between the Class A and Class B output stages.

2.2 A Review of Non-Classical Amplifiers

2.2.1 Class C Amplifiers

The Class C amplifier [Douglas, 2000] has its power transistors conducting for less than half the cycle. It is usually used for radio frequency (RF) where an *LC* circuit is employed to smoothen out the current pulses. The Class C is, in general, inapplicable to audio amplifiers.

2.2.2 Class E Amplifiers

In a Class E amplifier [Douglas, 2000] , the transistors therein operate in a way such that it has either a small voltage across it or a small current through it almost all the time, resulting in low power dissipation. However, this method has thus far been applied to RF applications and there is little application for audio amplifiers.

2.2.3 Class G Amplifiers

This design methodology was first introduced by Hitachi [Douglas, 2000] in 1976 with the objective of improving the efficiency of the power amplifier. The Class G block design is depicted in Figure 2.4. As the crest factor of audio signal is low, resulting in low level signals, a low voltage rail (V_L and $-V_L$) is used (for lower output signals) and a high voltage rail (V_H and $-V_H$) is used for larger signals. This 'two voltage rail operation' reduces the overall power dissipation, particularly when the output signal is small. The Class G is known to have a typically power efficiency of ~ 60% to 75%.

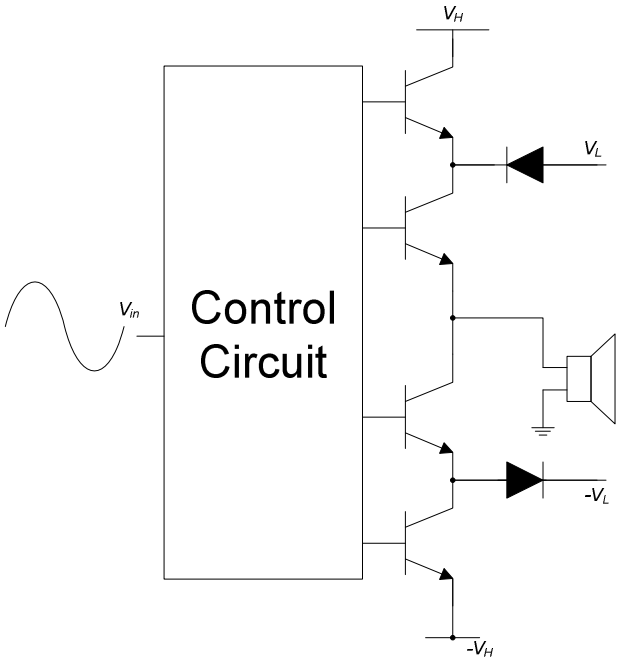


Figure 2.4 Class G Output Stage

2.2.4 Class H Amplifiers

A Class H amplifier [Douglas, 2000; Gennum Corp., 1996] takes the design of the Class G amplifier a step further by allowing the single supply rail to track the input signal, so as to provide just enough voltage for optimum operation of the output devices. Bootstrapping is a usual method used to achieve this. Generally, it has an efficiency of up to 85%.

In summary, the Class C and Class E amplifiers are generally applied for RF applications only. Class G and Class H amplifiers, on the other hand, offer alternative methods over the linear amplifiers to increase their power efficiencies. However, these amplifiers are inferior compared to CDAs in terms of power efficiency.

2.3 Class D Amplifiers (CDAs)

CDAs potentially offer the highest power efficiency compared to the amplifiers reviewed earlier. Typically, a CDA has an efficiency of 70% and in some designs, the efficiency can exceed 90% (see chapters 3 and 4 later). A comparison of power efficiency between Class A, Class B and Class D amplifiers is depicted in Figure 2.5. Being power efficient, it has low thermal dissipation, and the heat sink may be eliminated or largely reduced. This translates to other virtues of smaller and more compact design, with a lighter end product and better cost effectiveness. Higher power efficiency will also help to prolong battery life in portable applications.

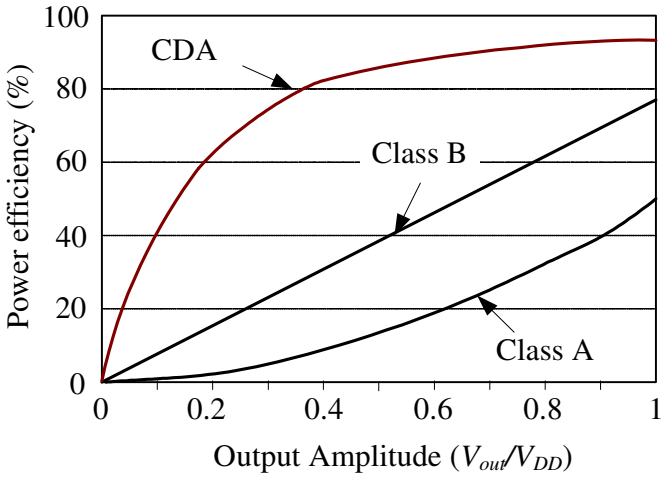


Figure 2.5 Power efficiencies of typical Class A, Class B and Class D amplifiers

The challenges of CDAs are their relatively higher complexity in design, particularly in terms of larger chip area and higher cost. A filter is also typically needed at the output to attenuate the high frequency carrier signal and this adds to the overall solution cost; a filterless design can also be implemented but there are implications on the choice (inductance) of the output loudspeaker. In view of practical use, the merits provided by the high efficiency of CDA must outweigh this cost.

Class D technology works based on the concept that the output transistors are either in the cutoff region (where voltage drop across the transistor is maximum with zero current) or in the triode region (where voltage drop across the transistor is minimum and current is delivered to the load), instead of the saturation region (for CMOS linear amplifiers). This is primarily because of the modulation process where the audio signal is modulated to a pulse-width-modulation (PWM) signal or a pulse-density-modulation (PDM) signal (see next section for modulation schemes), resulting in the output signal swinging from rail-to-rail.

The basic block of a typical CDA is depicted in Figure 2.6. An analog input signal goes into a modulator which converts the signal into pulses at the carrier frequency. The output stage buffers the pulse signals with sufficient drive (low impedance) to drive a low impedance load, usually a loudspeaker. This signal is then filtered through a low pass filter where the high frequency carrier components are attenuated, leaving the amplified audio band-limited signal.

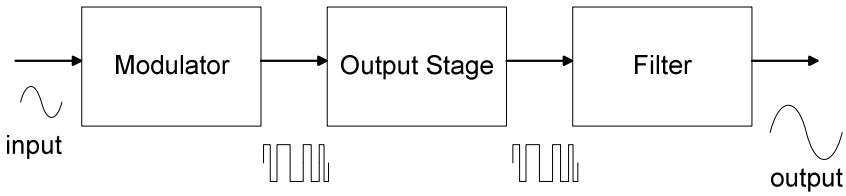


Figure 2.6 Block Diagram of Class D Amplifier

Having discussed the advantages and challenges of CDAs, and having presented the basic block design of a Class D system, the following sections will review the different types of modulation techniques. The advantages and disadvantages of these techniques will be reviewed, especially pertaining to efficiency.

2.3.1 A Review of Different Class D Modulators

The pulse modulation techniques can be classified into four basic types [Nielson, 1997]:

1. Pulse Amplitude Modulation (PAM)
2. Pulse Position Modulation (PPM)
3. Pulse Width Modulation (PWM)
4. Pulse Density Modulation (PDM)

PAM involves the conversion of a signal into a pulse train by varying the pulse amplitude. The advantage of PAM is the low bandwidth requirement which translates to a low carrier frequency requirement. PPM, on the other hand, involves the representation of the input signal by varying the position of the pulse in time. From a practical design perspective and application, PAM and PPM are both difficult to realize for commercial use due to their design complexity and relatively poor power efficiency.

PWM [Black, 1953; Murray, 1979; Jensen, 1987; Mellor, *et. al.*, 1991; Dondon, *et.al.*, 1999] and PDM [Candy, *et.al.*, 1992] are prevalent modulation techniques as they are relatively simple in hardware terms and can be designed to be power-efficient. The following sections will discuss these two modulators in turn and in detail.

2.3.1.1 Pulse Width Modulation (PWM)

The block design of a typical PWM CDA is depicted in Figure 2.7.

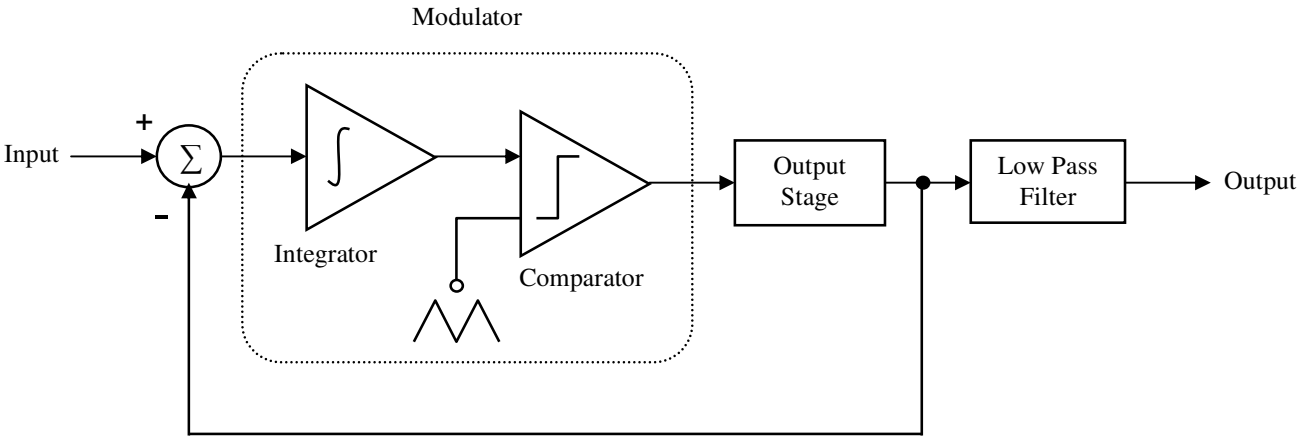


Figure 2.7 Block Diagram of PWM Class D Amplifier

PWM is a modulation scheme where the pulse width increases with the signal amplitude and this is depicted in figure 2.8. In a simplistic design, the modulator consists of an integrator followed by a comparator. The output of the integrator carrying an audio signal is compared with a triangular waveform of a much higher frequency (carrier frequency). The output of the comparator is the pulse width modulated audio signal in a pulse train. This is followed by the output stage and a low pass filter. After the output stage, the signal is negatively fed back to improve the linearity of the CDA.

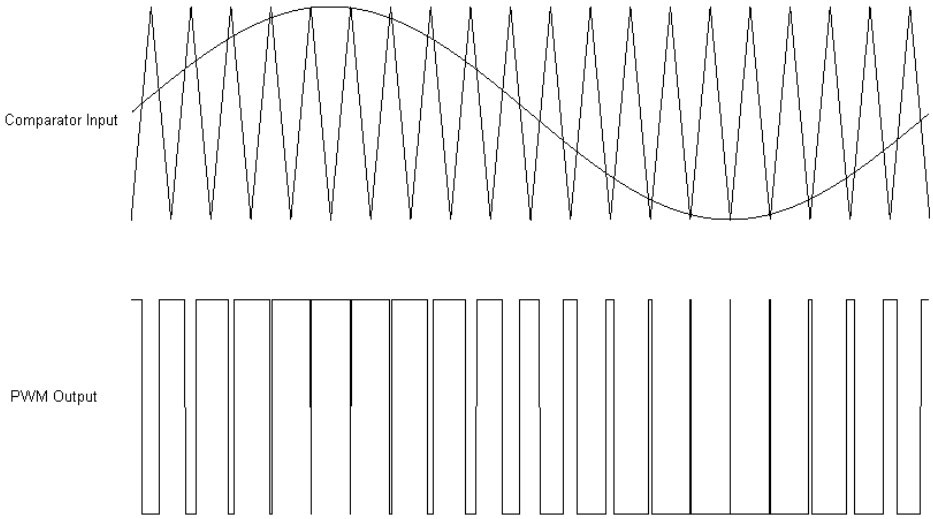


Figure 2.8 Waveforms of a PWM CDA

The pulse width modulated signal at the output of the integrator is a well established signal and it can be represented analytically [Black, 1953] as follows:

$$V_{out} = F_1(t) + F_1(-t) \tag{2.1}$$

where

$$F_1(t) = k + \frac{M}{2}\cos\omega_{mod}t + \sum_{m=1}^{\infty}\frac{\sin\omega_c t}{m\pi} - \sum_{m=1}^{\infty}\frac{J_0(m\pi M)}{m\pi}\sin(m\omega_c t - 2m\pi k)$$

$$-\sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty}\frac{J_n(m\pi M)}{m\pi}\sin(m\omega_c t + n\omega_{\mathrm{mod}}t - 2m\pi k - \frac{m\pi\omega_{\mathrm{mod}}}{2}) \tag{2.2}$$

and

ω_c = carrier frequency,

ω_{mod} = modulation frequency (signal frequency),

M = modulation index ($0 \le M \le 1$),

J_n = Bessel function of the first kind and nth order,

k = zero-input duty cycle of the PWM signal, i.e., the ratio of the pulse duration in the absence of modulation to the interval between the centre pulses.

Equation (2.1) expresses the output PWM signal in its positive and negative cycles and the components therein are delineated in equation (2.2). Specifically, in equation (2.2), the first term represents the inconsequential DC term (DC bias). The second term is the desired output signal, an amplified version of the input signal. The third term is a component of the carrier frequency at the output and the fourth term represents the harmonics of the carrier. These frequencies are inconsequential as they are out of the audio frequency band. Finally, the last term expresses the intermodulation between the carrier signal and the input signal. This is also called the Fold-back Distortion (FBD) and is undesired.

The overall switching frequency of the PWM is dependent on the frequency of the triangular waveform, the carrier frequency. This frequency is usually constant (unlike PDM where its switching frequency varies). The selection of this switching frequency is important as it affects both total harmonic distortion (THD) and power efficiency of the CDA. Shu and Chang [Shu *et.al*., 2006] have recently established the relationships between the non-linearities in a PWM CDA and the carrier frequencies. Specifically, it has been shown that in order to get low THD non-linearities, it is necessary that the carrier frequency must be much higher than the signal frequency. For audio application, with an upper limit of 20 kHz, a 200 kHz or higher carrier frequency is needed to produce acceptable THD (<0.1%). This frequency is low compared to a typical PDM that operates at a switching frequency of 500 kHz. We will later show that power efficiency decreases with higher frequency, and hence, PWM is relatively more power efficient.

In practice, the PWM method is arguably the most popular modulation technique due to its circuit simplicity (low quiescent current) and low frequency (carrier) operation and stability [Gaalaas, *et.al*., 2005] at high modulation indices (signal swings). These factors, in part, result in higher power efficiency than the PDM.

Classical linear high-fidelity amplifiers feature good power supply rejection ratio (PSRR) (- >60dB) and extremely low THD (<0.01%). Although the CDA can feature substantially higher power efficiencies than the classical linear amplifiers, a challenge of

a CDA design is to match (or exceed) its performance over its linear counterparts in other performance metrics, in particular the non-linearities such as PSRR and THD. These parameters will now be reviewed.

It has been shown that the open-loop PWM CDA, depicted in Figure 2.9, suffers from poor PSRR [Berkhout, 2002]. As the output transistors of CDA work in the triode region for an average of 50% of the time, the output voltage will track the supply voltage and any noise at the supply will be seen at the output. The modeling of the open-loop and closed-loop PWM CDA have been established [Ge, *et.al.*, 2007]. For the open-loop PWM CDA, the ratio of its output noise to its supply noise is $N_D = N/2$ [Berkhout, 2002], where N_D represents the output noise components introduced by the noise in the supply rail (N), that is it is only attenuated by a mere 6 dB. In practice, this is highly unsatisfactory.

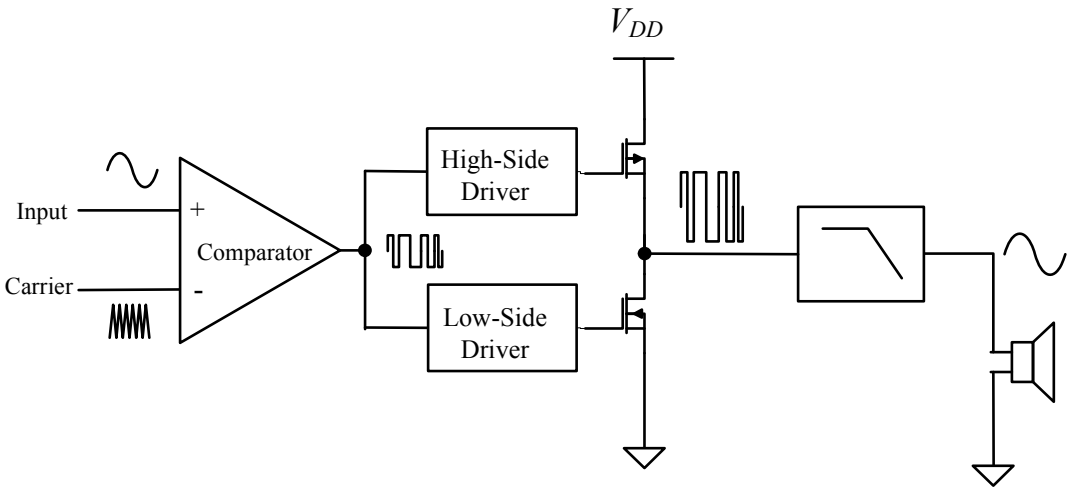


Figure 2.9 Open-Loop PWM CDA

As in the case of linear amplifiers where non-linearities are reduced by negative feedback with a reduction of (loop gain + 1), the power supply noise in closed-loop PWM CDAs is likewise reduced by a factor of (loop gain + 1). For the closed-loop PWM CDA [Ge, *et.al.*, 2007] depicted in Figure 2.10 and the ensuing model in Figure 2.11, its PSRR is:

$$\text{PSRR} = 20\log\left(\frac{1/2}{\left(1+\left|G_{int}\right|G_{PWM}H_1\right)}\right)\text{dB} \qquad (2.3)$$

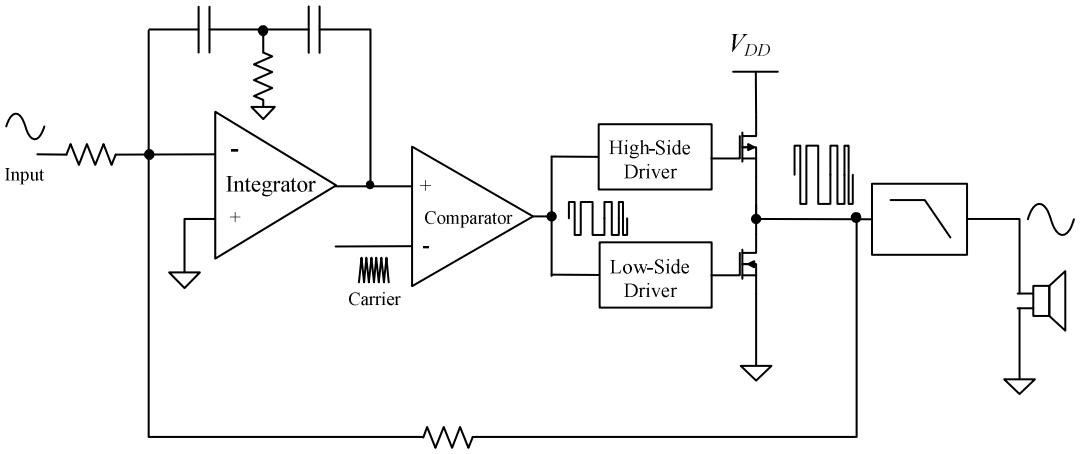


Figure 2.10 Closed-Loop PWM CDA

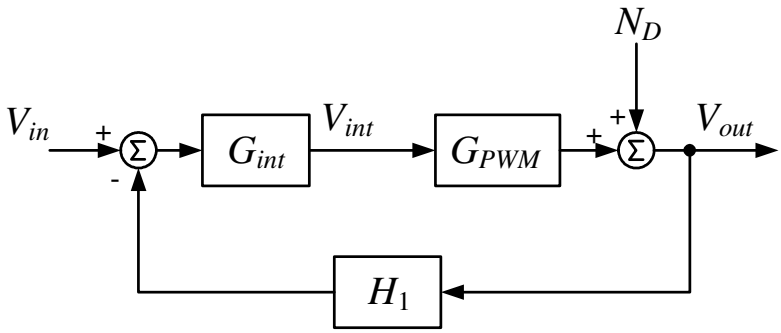


Figure 2.11 Model of Closed-Loop PWM CDA

It was shown that the three critical parameters that affect PSRR are the gain of the integrator, G_{int}, the gain of the PWM stage, G_{PWM} and the feedback factor, H_1. PSRR will improve as the abovementioned three parameters increase. It was recommended that G_{int} be increased to improve PSRR over the other 2 parameters as G_{int} carries the heaviest weighting in the loop gain equation. Increasing G_{PWM} reduces the Signal-to-Noise Ratio (SNR) – a highly undesirable effect, while increasing H_1 reduces the amplifier gain and

increases the amount of carrier component at the integrator output (hence reduce the dynamic range of the amplifier).

The open-loop PWM CDA is also known to have poor THD performance compared to the linear Class AB amplifier; this is not the case for a properly designed closed-loop CDA. In the case of the simplest PWM open-loop CDA, the non-linearity of the triangular carrier (usually generated by an RC circuit) at the pulse width modulator [Tan, *et.al.*, 2003] and the dead time of the output stage [Wu, *et.al.*,1999] are some of the mechanisms of the harmonic distortion. The THD for a practical open-loop PWM is typically 2% and this is generally undesirable.

The introduction of a feedback reduces the THD of the open-loop CDA by a factor of (loop gain + 1), but conversely introduces THD due to the combined phase and duty cycle error [Shu, *et.al.*, 2006]. The expression of the overall THD for the single feedback CDA (Figure 2.10) is:

$$\%\text{THD} \approx \sqrt{\left[\frac{1}{2}J_1\left(\frac{xM^2}{2}\right)\right]^2 + \left[\frac{1}{M(1+GH_{@3f_s})}\sum_{m=1}^{\infty} 2yJ_m\left(\frac{mA\pi}{2}\right)\cos m\theta J_3\left(\frac{mM\pi}{2}\right)\right]^2} \times 100\% \quad (2.4)$$

$$x = \pi f_s / 8\tau_2 f_c^2 \quad (2.4a)$$

$$y = 2(-1)^m / (m\pi) \quad (2.4b)$$

$$A \approx \frac{2J_0\left(\pi \frac{M}{2}\right)}{\pi} \sin 2\pi f_c t \times GH_{@f_c} \quad (2.4c)$$

where J is the Bessel function of the first kind,

A is the amplitude of the attenuated carrier signal at the integrator output,

M is the modulation index,

f_s is the frequency of the input signal,

τ is the time constant that is predetermined by the design of the loop filter (and its stability),

GH is the loop gain and

f_c is the carrier frequency.

The parameters available to a CDA designer are the loop gain, *GH* and the carrier frequency, f_c. Although usual methodology shows that increasing *GH* can help to decrease THD by (loop gain + 1), it was also observed that increasing *GH* will increase the harmonic components due to duty cycle error [Shu, *et.al.*, 2006]. In other words, increasing the loop gain may not necessarily improve the THD and this is somewhat converse to what is known in linear amplifier design. Finally, increasing the carrier frequency, f_c, can improve THD but it has implications on the power efficiency of the CDA and this will be further discussed in chapter 3.

2.3.1.2 Pulse Density Modulation (PDM) CDA

The PDM CDA is typically realized by means of the ΣΔ.

2.3.1.2.1 ΣΔ CDA

The ΣΔ CDA operates by the principle of PDM and its block design is shown in Figure 2.12. The input signal is fed to the modulator via a summing circuit. The modulator comprises an integrator followed by a one-bit quantizer. The output is a pulse density modulated signal (where its pulse density changes with the input signal) and this is depicted in Figure 2.13. The duty cycle of the pulse signal is proportional to the instantaneous value of the input analog signal, and the highest switching frequency occurs when the input signal is at its offset dc value. As in the PWM CDA, the output is buffered by the output stage. The low pass filter attenuates the high frequency components, and the amplified analogue audio signal is recovered.

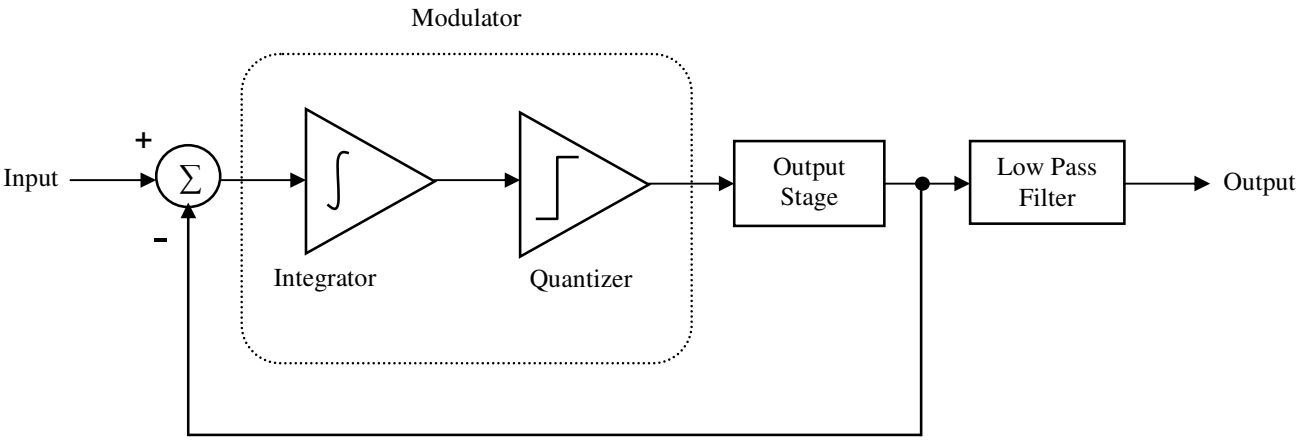


Figure 2.12 Functional Blocks of the PDM Class D Amplifier

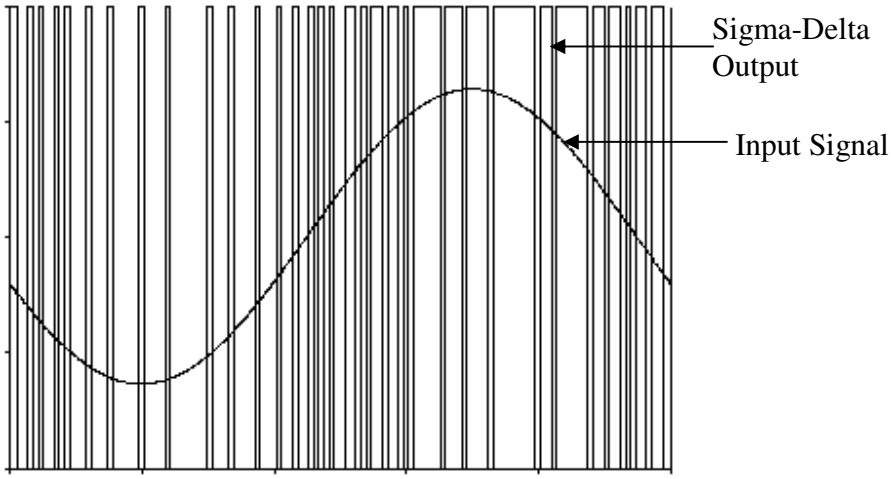


Figure 2.13 Waveforms of a ΣΔ CDA

The ΣΔ approach is a well established technique for ADCs and DACs [Candy, *et.al.*, 1992, Aziz, *et.al.*, 1996]. The primary advantage of ΣΔ CDA is its substantially lower non-linearity compared to the PWM and Bang-bang control (see section 2.3.1.2.4 later) approaches. This is somewhat akin to the ΣΔ modulation approach in data converters where a high-order (>3rd order) modulation is typically employed to shape the noise to a region which is out-of-band, that is to a frequency range not within the frequency band of interest. The major drawback of the PDM approach is that the sampling frequency is

typically high and this translates to higher switching loss, particularly at the output stage, which will degrade the power efficiency performance.

The quantization noise is induced during the quantization process and it is first reduced by oversampling. It is well established [Candy, *et.al.,* 1992; Shu, *et.al*., 2006] that the relationship between the quantization noise of a Nyquist-rate system (where the sampling frequency is twice of the maximum input frequency), N_s and that of an oversampled one, $N_{oversampled}$, is:

$$N_{oversampled} = \frac{N_s}{f_s / 2f_{BW}} \tag{2.5}$$

where f_s is the sampling frequency and

f_{BW} is the bandwidth of the system.

The quantization noise is further reduced by the noise shaping process. The in-band quantization noise, $N_{\Sigma\Delta 1}$, in the first order ΣΔ modulator can be written [Aziz, *et.al*., 1996; Shu, *et.al*., 2006] as:

$$\mathrm{N}_{\Sigma\Delta 1} = \int_{-f_{BW}}^{f_{BW}} \frac{N_{oversampled}}{f_s} \left|1 - \exp(-j2\pi f / fs)\right|^2 df \cong \frac{N_{oversampled}}{(f_s / 2f_{BW})^3} \times \frac{\pi^2}{3} \tag{2.6}$$

Similarly, the relationship for higher order ΣΔ modulator is given as follows:

$$\mathrm{N}_{\Sigma\Delta,n} = \int_{-f_{BW}}^{f_{BW}} \frac{N_{oversampled}}{f_s} \left|1 - \exp(-j2\pi f / fs)\right|^{2n} df \cong \frac{N_{oversampled}}{(f_s / 2f_{BW})^{2n+1}} \times \frac{\pi^2}{2n+1} \tag{2.7}$$

In equation (2.5), it is desired that the oversampling ratio (between an oversampled system and a Nyquist system) be as high as possible to obtain low noise. However, as earlier delineated, high oversampling ratio is undesirable because a high switching frequency results in high power dissipation at the output stage, which will lower the power efficiency of the overall system.

It is apparent from equation (2.6) and equation (2.7) that to achieve a lower in-band quantization noise, a higher order modulator is to be used. However, this requires more complex hardware and a compromise between noise performance and IC area (which will translate into cost) should be carefully considered. Moreover, more complex hardware will increase the quiescent current of the system which will increase power dissipation and lower power efficiency.

The ΣΔ quantizer can be categorized into two types:

i. Synchronous ΣΔ, and
ii. Asynchronous ΣΔ

2.3.1.2.2 Synchronous ΣΔ Quantizer

A typical synchronous design quantizer, as depicted in Figure 2.14, comprises a comparator followed by a D flip-flop which is controlled by an external clock. The output of the D flip-flop is digital in nature with high quantization noise due to the external sampling clock. The noise is suppressed by sampling with a high oversampling rate. To further mitigate the noise, a higher order ΣΔ is typically used (for example, a minimum 3rd order). A 3rd-order ΣΔ CDA can feature a total harmonic distortion plus noise (THD+N) of <0.1% at 500kHz clock frequency [Ge, *et.al.*, 2004], and a 7th-order ΣΔ CDA can feature a THD+N of <0.001% at 450kHz clock frequency [Gaalaas, *et.al.*, 2005].

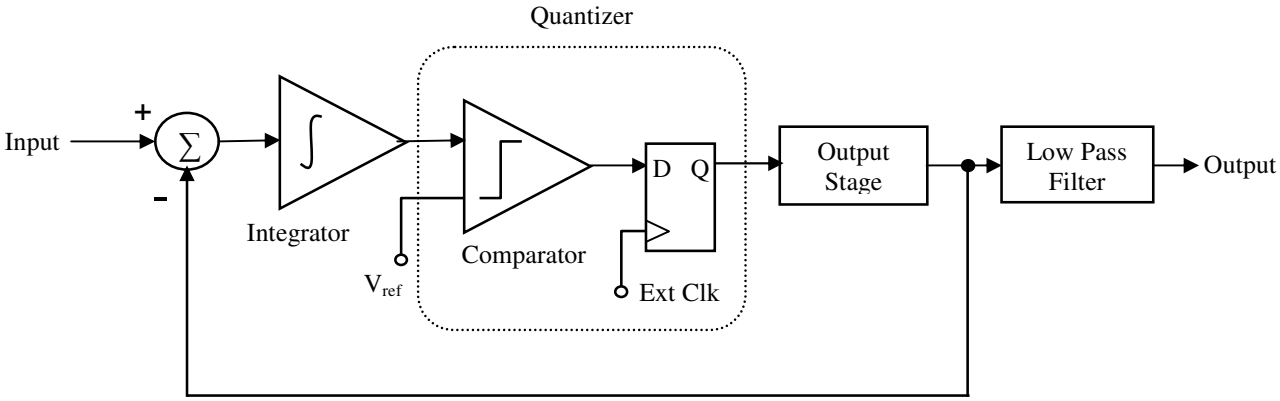


Figure 2.14 General Model of 1st-Order Synchronous ΣΔ Class D

The drawback of the synchronous ΣΔ is the complexity of the circuit, thereby requiring a larger IC area and resulting in relatively high power consumption and poorer power efficiency - the switching at a high frequency will also dissipate higher power in terms of switching losses (and poorer power efficiency).

2.3.1.2.3 Asynchronous ΣΔ Quantizer

The asynchronous design, depicted in figure 2.15, differs from the synchronous ΣΔ where a hysteresis comparator is used in place of the comparator and the D flip-flop in the case of the synchronous design. As the hysteresis comparator is continuously sampling the signal, the output is highly 'analogue' in nature. The primary advantage of the asynchronous design is that the modulator does not contain any quantization noise (as opposed to the synchronous approach). For example, the performance of a 1st-order asynchronous design is comparable to higher order (eg. 3rd-order) synchronous design [Noro, 2004] in terms of signal and noise performance. With a simpler circuit (lower order), the power consumption of an asynchronous design is lower, and potentially offers a higher power efficiency.

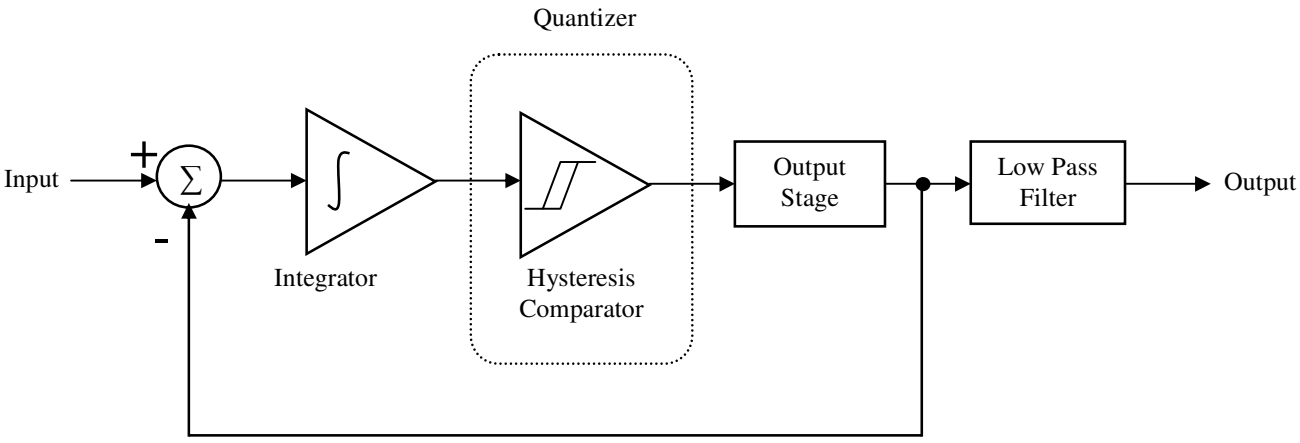


Figure 2.15 General Model of 1st-Order Asynchronous ΣΔ Class D

In the design of a CDA, it is always desirable to have both high power efficiency and low non-linearity at the same time. However, in practical application, there is a compromise

between the two. From a power efficiency viewpoint, the switching frequency must be kept as low as possible, thereby reducing the power dissipation associated with the output stage. To achieve low switching frequency, the comparator must be designed with a large hysteresis bandwidth. From a designer's viewpoint, a low speed low power op-amp operating at low frequency with a comparator of large hysteresis bandwidth is simple to design. However, to achieve low THD, the switching frequency must be designed to be as high as possible. This will require a comparator with very small hysteresis bandwidth. This small hysteresis comparator together with a high speed op-amp will consume more power and hence lower the overall power efficiency.

The analytical model for a typical asynchronous 1st-order PDM CDA is depicted in Figure 2.16. Equation (2.8) [Shu, *et.al.*, 2007] is the multi-dimensional Fourier series expression of the PDM output signal at V_{PDM} (normalized with respect to the power supply, V_{DD}):

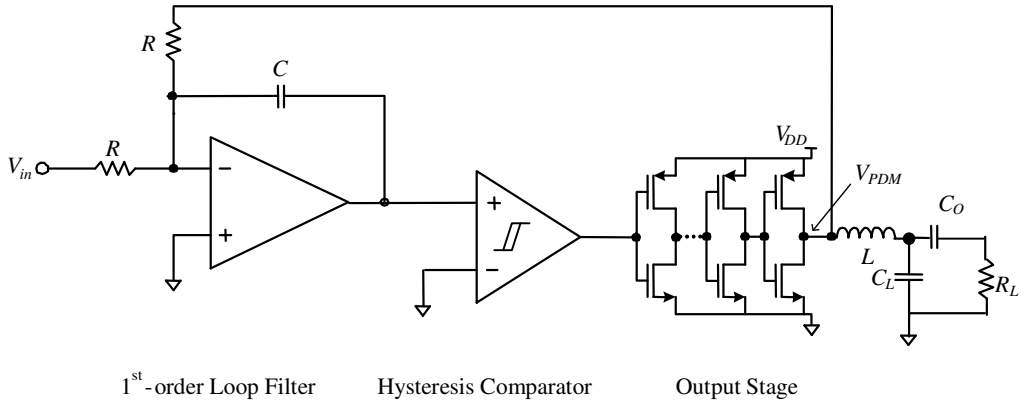


Figure 2.16 A typical 1st-order asynchronous PDM CDA

$$V_{PDM}(t) = \frac{1}{2} + \frac{M \sin \omega_{in} t}{2} + \sum_{m=1}^{\infty} \frac{2}{m\pi} \sum_{p=-\infty}^{\infty} \sum_{q=-\infty}^{\infty} (B_o \sin \omega_e t + B_e \cos \omega_e t) \tag{2.8}$$

where M is the modulation index,

ω_{in} is the angular frequency of the input signal,

$$\omega_e = m\left(1 - \frac{M^2}{2}\right)\omega_l + (2p+q)\omega_{in} \tag{2.8a}$$

ω_l is the idle carrier frequency when no input signal is applied,

$$\omega_l = \frac{\pi}{4RCV_h} \tag{2.8b}$$

V_h is the hysteresis bandwidth of the hysteresis comparator,

$$B_o = \frac{1-(-1)^q}{2} J_p(m\alpha) J_q(m\beta) \cos(m\frac{\pi}{2}) \tag{2.8c}$$

$$B_e = \frac{1+(-1)^q}{2} J_p(m\alpha) J_q(m\beta) \sin(m\frac{\pi}{2}) \tag{2.8d}$$

$$\alpha = \frac{M^2 \omega_l}{4\omega_{in}} \tag{2.8e}$$

$$\beta = \frac{\pi}{2} M \tag{2.8f}$$

$J_p(\ )$ is the Bessel function of the first kind with the order of p.

The carrier frequency of the PDM signal is as follows:

$$\omega_c = \omega_l (1 - M^2 \sin^2 \omega_{in} t) \tag{2.9}$$

Equation (2.8) expresses all the frequency components of V_{PDM}, and they consist of a linear part and a non-linear part. The linear part comprises the first two terms, which are the inconsequential DC bias and desired amplified input signal. The last term is the non-linear part comprising the carrier-related frequency components – the carrier plus its harmonics, and the intermodulation components between the input signal and the carrier.

This non-linear part encompasses the Electromagnetic Interference (EMI) and Fold-Back Distortion (FBD).

2.3.1.2.4 Bang-Bang Control Class D (BCCD) Amplifier

A modulation technique called the Bang-bang Control Class D (BCCD) can achieve a PDM-like output but with substantially simpler circuitry compared to the ΣΔ approach. A typical Bang-bang control design is depicted in Figure 2.17. The feedback network feeds the output signal back to the input stage and subtracts it from the input signal. The resultant signal is the error between the desired output and actual output. The Bang-bang controller, implemented using a hysteresis comparator, sets a small hysteresis band and instantaneously compares the error signal against its hysteresis band. Once the error exceeds the hysteresis band, the controller output state will change. The output of the controller, as a result, yields a train of pulses that transits between binary '0' and binary '1', a PDM-like signal similar to that of the asynchronous ΣΔ CDA as depicted in figure 2.18. As in the previous designs, the audio signal is recovered through the low pass filter after the output stage. As there is no integrator in the design, the audio signal is fed back after the low pass filter.

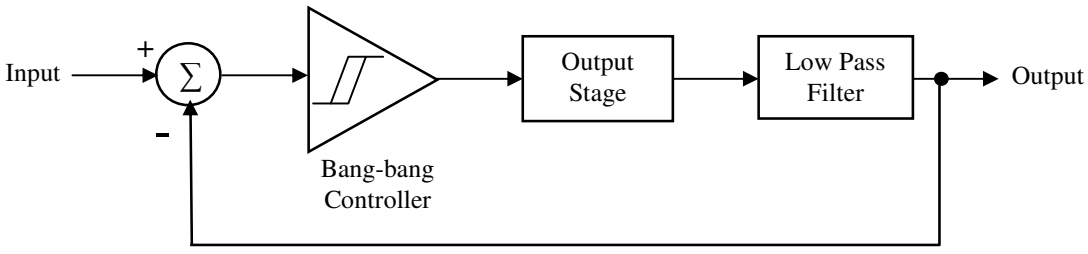


Figure 2.17 Block Diagram of Bang-bang Control Class D

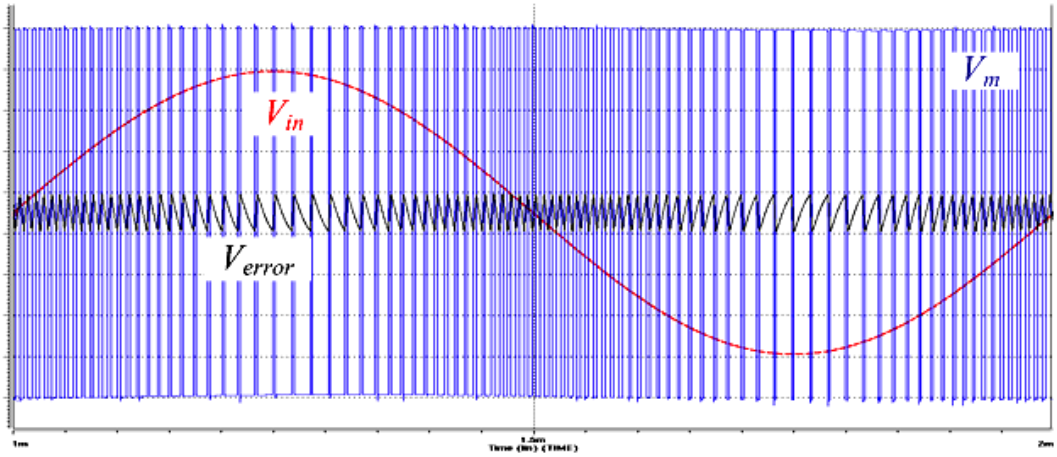


Figure 2.18 Waveforms of the BCCD

At present, the BCCD method is arguably the least popular approach because the fidelity of its output is the lowest compared to the PWM and the ΣΔ modulation approaches, particularly at high modulation indices. At low modulation indices, the BCCD approach can yield good fidelity, for example, the BCCD with current sensing feedback [Ge, *et.al.*, 2004] can achieve <0.1% THD that is comparable to 3rd-order ΣΔ -CDA. Nonetheless, there is some recent interest [Takagishi, 2002; Ge, *et.al.*, 2004; Jung, *et.al.*, 1998] in this approach because of the relatively simple hardware compared to the PWM and ΣΔ modulation approaches. In view of that, for low power applications, the quiescent power may become significant relative to the overall power consumption of a CDA and BCCD may offer an alternative for high efficiency design.

The PSRR of the BCCD has been established [Ge, *et.al.*, 2007]. A typical BCCD design is presented in figure 2.19 for further discussion accompanied by the PSRR expression in equation (2.10).

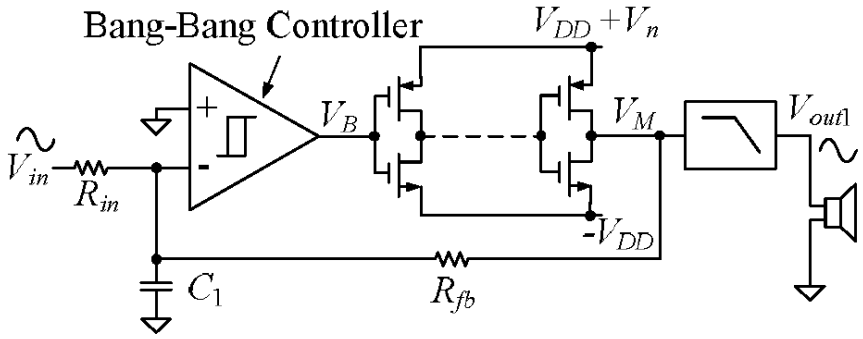


Figure 2.19 BCCD System Design

The PSRR expression of the BCCD amplifier (normalized with respect to the power supply, V_{DD}) is:

$$\text{PSRR} = 20\log\left(\frac{(rh)^2}{3}\left|j\frac{\omega_n}{\omega_p}+1\right|\right) \tag{2.10}$$

$$h = \frac{V_h}{V_{DD}} \tag{2.10a}$$

$$r = 1+\frac{R_{fb}}{R_{in}} = 1+G \tag{2.10b}$$

$$\omega_p = \frac{1}{(R_{in}\,//\,R_{fb})C_1} \tag{2.10c}$$

where V_n is the noise voltage,

ω_n is the supply noise frequency in rad/s,

V_{DD} is the supply voltage,

V_h is the hysteresis voltage of the Bang-bang controller,

R_{fb} is the feedback resistance,

R_{in} is the input resistance of the BCCD system,

G is the closed-loop gain, and

C_1 forms the low pass filter with R_{fb} as depicted in figure 2.19.

When the input signal is zero, the idle switching frequency (carrier) is also defined as:

$$f_{sw} = \frac{\omega_p}{4rh} \tag{2.11}$$

From equation (2.10), it is evident that PSRR will improve when r and h are small and ω_p is large relative to ω_n. These parameters are of importance as they are within the control of the designer. From equation (2.10) h will change by varying V_h, r will change by varying G and ω_p will change by varying R_{in}, R_{fb} and C_1. Evidently, there are implications to other design parameters like the closed-loop gain, G, and switching frequency of the BCCD. From equation (2.11), it is seen that improving the PSRR will also mean that the switching frequency, f_{sw}, is higher, which results in a higher switching loss at the output stage, and hence yield a poorer power efficiency.

2.3.2 Output Stage Configurations

It is unambiguous that the output stage has a big influence on the overall CDA, particularly the power efficiency and the required IC area. The well established output stage configurations are the *p*-channel-cum-*n*-channel inverter [Texas Instruments, 1999; Chang *et.al*., 2000] and the *n*-channel totem-pole [Berkhout, 2003; Texas Instruments, 2002] configurations. The following section will review these configurations and will also review the single-ended (half bridge) and full-bridge (Bridge Tied Load) designs.

2.3.2.1 Inverter Output Stage and *n*-channel Totem Pole Output Stage

The *p*-channel-cum-*n*-channel inverter output stage is arguably more popular than the totem pole design largely due to its simplicity in design. In low voltage applications, this design is prevalent and this is in part because the power dissipation arising from short-circuit current is low (see later).

In our view, of the two designs, the *n*-channel totem-pole configuration is the preferred design, despite its higher complexity, for the following two reasons. First, as the area requirement of the output stage is dominant in the overall CDA, the *n*-channel totem-pole configuration is advantageous as it requires a smaller IC area. This is because as electron mobility is ~3x higher than hole mobility, the *n*-channel transistor that replaces the *p*-channel is approximately 3x smaller. In the context of the overall output stage, this translates to an ~50% IC area reduction; in a *p*-channel-cum-*n*-channel inverter output stage, the area is 1x *n*-channel and 3x *p*-channel, compared to 2x *n*-channel in *n*-channel totem-pole configuration. In the context of the overall Class D amplifier where the output stage is assumed to occupy 50% of the area, this translates to a very worthwhile 25% area reduction.

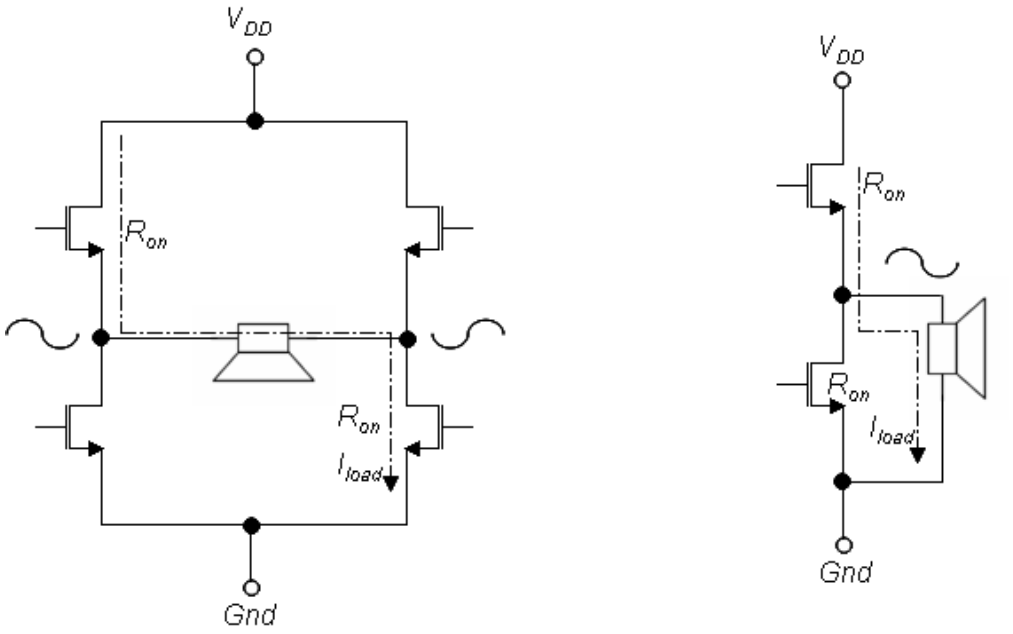
Second, as the power dissipation mechanisms of the output stage is in part due to the charging and discharging of the parasitic capacitances of the transistors in the output stage (see next section) and that the capacitance increases with the size of the transistor, the *n*-channel totem-pole configuration is advantageous in terms of the ensuing lower power dissipation (than the *p*-channel-cum-*n*-channel inverter). This is because the large *p*-channel transistor is replaced by the smaller *n*-channel transistor.

For these reasons, we will use the *n*-channel totem-pole configuration for our design of a DMOS output stage in chapter 3 and a HVMOS output stage in chapter 4. Nonetheless, note that this configuration is only applicable in mid-to-high voltage applications because the *n*-channel transistor (that replaces the *p*-channel transistor) requires a bootstrap voltage (above its gate turn-on voltage) to turn it on appropriately. Practically, this also means that the *n*-channel totem-pole configuration is seldom used in low-voltage applications due to the need for this high (and hardware expensive) turn-on voltage. This, in part, explains why many low voltage audio devices are designed to drive 16Ω or 32Ω (earphone) loads (as opposed to 4Ω or 8Ω loads in loudspeakers) – the demands on IC area and power for larger resistance loads are more relaxed.

2.3.2.2 Full Bridge Output Stage and Half Bridge Output Stage

There are two well-known methods to connect a loudspeaker to an amplifier – half-bridge (single-ended) and full-bridge (bridge-tied-load, BTL) – and both methods are equally prevalent. The half bridge topology is depicted in Figure 2.20(b) where the loudspeaker terminals are connected to the amplifier output and to ground. In this case, the signal swing of the amplifier is between voltage supply (if the output is rail-to-rail or slightly below voltage rail otherwise) and ground, the signal ground is usually between this maximum output and ground. A (ac coupling or dc decoupling) capacitor is usually placed between the output of the amplifier and the loudspeaker to prevent a DC current from flowing into the loudspeaker (not shown in Figure 2.20(b)) which would otherwise damage the loudspeaker. Note that as the impedance of the loudspeaker is typically small, the capacitance of this capacitor is large such that the cut-off frequency is below the lowest audio frequency (20Hz).

The full-bridge topology, depicted in Figure 2.20(a), on the other hand, has two 'effective' outputs, where it is simply two interconnected half bridge output stages (Figure 2.20(a)) whose outputs are 180º out of phase. In this case, the signal ground is between the maximum (positive swing) signal and minimum (negative swing) signal, that is ground. Put simply, there is now no DC bias and there is no need for the large capacitor required in the half bridge topology.



(a) **(b)**

Figure 2.20 (a) Full bridge configuration and (b) Half bridge configuration

In the context of amplifier (both linear and CDAs) power outputs, the full bridge configuration is able to provide 4 times more power compared to the half bridge for a given supply voltage because the output voltage is effectively doubled. In view of that, the full bridge configuration is preferred if there is a limitation in the supply voltage level. This is usually applied for low-to-mid voltage devices where the supply voltage level is limited.

In terms of noise performance, the full bridge has an advantage over the half bridge as noise that is common to both channels (eg. supply noise and ground noise) will be cancelled out to the first order.

In terms of output stage IC area consideration, it is apparent from Figure 2.20 that as the full bridge configuration requires 4 power transistors, as opposed to only 2 for the half bridge, the IC area for the former is two times that of the latter (assuming the same output stage design). Similarly, assuming that each output stage sources or sinks the same

amount of output (load) current, the power loss (due to capacitances and on-resistances (see next section)) of the former is also doubled with respect to the latter. From a practical perspective on power efficiency, for a half bridge and full bridge design, each embodying an identical output stage, the half-bridge design is more power efficient for a given output power. The simple proof for this is given in chapter 4 where a half bridge output stage is designed (using HVMOS); in chapter 3, we will design a full bridge output stage (using DMOS).

2.3.3 A Review of Power Efficiency of CDAs with a CMOS Output Stage

The output stage is an important section of the CDA as it dissipates the most power compared to the other parts of the circuits, and hence it largely determines the overall power efficiency. [Chang, *et.al*., 2000] has presented a method to analytically determine the efficiency of a low voltage CMOS *p*-channel-cum-*n*-channel inverter output stage in a CDA. The reported analysis is now reviewed and this serves as the preamble to our research work that will be delineated in the subsequent chapters in this dissertation.

The CMOS output stage was modeled by lumping the capacitances and resistances into gate capacitance, C_g, drain capacitance, C_d and on-resistance, R_{on} as shown in figure 2.21. *G*, *D*, *S* and *B* represent the gate, drain, source and body of the MOS transistor respectively.

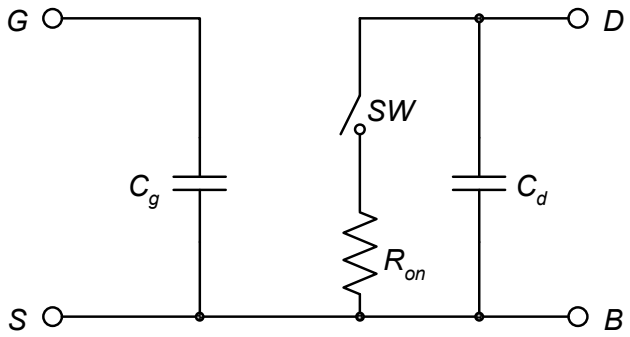


Figure 2.21 Lumped MOS Model

This lumped model is used to calculate the three major power dissipations:

(a) Power dissipation due to parasitic capacitance

$$P_C = \frac{1}{2} f_C C_P V_{DD}^{\ 2} \tag{2.12}$$

where f_c is the carrier frequency,

C_P is the total parasitic capacitance of the output stage, and

V_{DD} is the supply voltage.

(b) Power dissipation due to on-resistance

$$P_r = \frac{1}{T_S} \int_0^{T_S} i_o^2 R_{on} dt \approx \frac{1}{2} M^2 I_O^2 R_{on} \tag{2.13}$$

where T_S is the period,

M is the modulation index,

i_o is the time dependent output current,

I_O is the maximum output current, and

R_{on} is the total on-resistance of the output stage.

(c) Power dissipation due to short circuit current

$$P_S = I_{mean} V_{DD} \tag{2.14}$$

where I_{mean} is the mean value of the short-circuit current.

Due to the nature of an inverter output stage, there is always a short time during the transition when both the top transistor and the bottom transistor conduct. This forms a

short-circuit from the supply to ground. The power dissipation caused by this phenomenon of short-circuit or spike current [Elmasry, 1981; Veendrick, 1984; Haznedar, 1991] is known as the short-circuit current dissipation.

The total mean short circuit current of the two output inverters [Veendrick, 1984], one at each end of the full bridge output stage is

$$I_{mean} = \begin{cases} \frac{1}{6}\frac{\varepsilon_{ox}\mu}{t_{ox}L_{ch}}\frac{(V_{DD}-2V_{th})^3}{V_{DD}} f_c \tau W & \text{for } V_{DD} > 2V_{th} \\ 0 & \text{for } V_{DD} \le 2V_{th} \end{cases} \qquad (2.15)$$

where ε_{ox} is the permittivity of the gate oxide,

t_{ox} is gate oxide thickness,

f_c is the carrier frequency and

τ is the rise or fall time of the PWM signal.

Hence, the power dissipation, P_s, due to short circuit current can be derived as follows:

$$P_s = I_{mean}V_{DD} = \frac{1}{6}\frac{\varepsilon_{ox}\mu}{t_{ox}L}(V_{DD}-2V_{th})^3 f_c \tau W \qquad (2.16)$$

From the above equation, it can be seen that P_s increases with the switching frequency f_c and W/L ratio, and is highly dependent on V_{DD}. The last parameter is of particular interest in this dissertation as our work pertains to a mid voltage application.

The three power dissipation mechanisms for the full bridge output stage (comprising of 2 strings of N inverters), realized using the finger layout, are derived and summarized in Table 2.1 [Chang, *et.al.*, 2000]. In these derivations, it was assumed that

$L_n = L_p$ = minimum L and $\beta_n = \beta_p = \beta$, where L is channel length and β is the gain factor of a MOS transistor while n and p represent n-type and p-type transistors respectively.

Table 2.1 Summary of CMOS power dissipation mechanisms

Symbol	Formula
P_C	$\frac{1}{2}V_{DD}^2 f_c\left[2C_{pad} + (K_1 + K_2)W_P\sum_{i=0}^{N-1}t^{-i}\right]$
K_1	$2\left(1+\frac{1}{\alpha}\right)\left[C_{OX}L + (C_{GSO} + C_{GDO})\right]$
K_2	$2\left[\left(C_{JP} + \frac{C_{JN}}{\alpha}\right)L_{DS} + \left(1+\frac{1}{\alpha}\right)(C_{GDO} + 2C_{JSW})\right]$
P_S	$K_3(V_{DD} - 2V_{th})^3 f_c \tau W_P \sum_{i=0}^{N-1}t^{-i}$
K_3	$\frac{1}{6}\frac{\varepsilon_{OX}\mu_P}{t_{OX}L}$
P_r	$\frac{1}{T_S}\int_0^{T_S} i_o^2 R_{on} dt \approx \frac{1}{2}M^2 I_O^2 R_{on}$
R_{on}	$\frac{K_4 + \alpha K_5}{W_P} + \frac{2K_6}{(V_{DD} - V_{th})W_P}$
K_4	$(l_1 + 2l_3)R_P + 2(l_1 + l_2)R_{ctp}$
K_5	$(l_1 + 2l_3)R_N + 2(l_1 + l_2)R_{ctn}$
K_6	$\frac{L}{\mu_P C_{OX}}$

The symbols used are summarized in Table 2.2.

Table 2.2 Summary of symbols

α	W_p/W_n
C_{GSO}	Gate-to-source capacitance per unit gate width.
C_{GDO}	Gate-to-drain capacitance per unit gate width.
C_J	Zero-biased *p*-*n* junction area capacitance.
C_{JSW}	Zero-biased *p*-*n* junction periphery capacitance.
C_{OX}	Oxide capacitance per unit gate area.
C_{pad}	Bond pad capacitance.
M	Modulation index.
ε_{OX}	Permittivity of gate oxide.
L_{DS}	Length of the source or drain area.
R_L	Load resistance.
R_{ctn}	*n*-type contact resistance per contact
R_{ctp}	*p*-type contact resistance per contact
R_n	Source and drain area resistance per square of an *n*MOS Transistor (*n*MOST).
R_p	Source and drain area resistance per square of a *p*MOST.
τ	Rise or fall time of a PWM signal.
t	Tapering factor of a string of inverters.
t_{OX}	Gate oxide thickness.
μ_p	Hole mobility.
V_{th}	Threshold voltage of a MOST.
W_n	Channel width of the *n*MOST output stage inverter.
W_p	Channel width of the *p*MOST output stage inverter.

Figure 2.22 depicts the layout of an *n*MOST based on the finger structure and it illustrates the definitions of the dimensions of l_1, l_2, l_3, L_{DS} and W in Table 2.1.

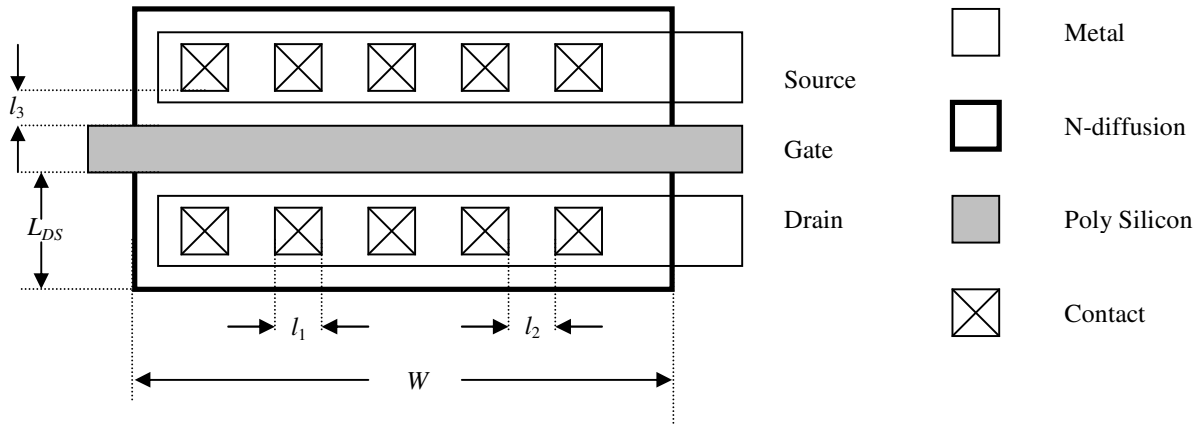


Figure 2.22 Layout of an *n*MOST

Based on the derived power dissipation equations, the efficiency of the output stage is shown to be:

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{DISS}} = \frac{P_{OUT}}{P_{OUT} + P_C + P_S + P_r} \tag{2.17}$$

where P_{OUT} is the output power and

P_{DISS} is the total power dissipation of the output stage.

To optimize the channel width W_P of the output transistor to a single modulation index, a function representing the total power dissipation (normalized) is defined:

$$F(W_P) = \frac{P_C}{P_{OUT}} + \frac{P_S}{P_{OUT}} + \frac{P_r}{P_{OUT}} \tag{2.18}$$

And the resultant expression for power efficiency in equation (2.17) is re-written as:

$$\eta(W_P) = \frac{1}{1 + F(W_P)} \tag{2.19}$$

To obtain maximum power efficiency, the following condition must be satisfied:

$$\frac{\partial F(W_P)}{\partial W_P} = 0 \tag{2.20}$$

and the optimized channel width for the desired modulation index M is finally obtained:

$$W_P = M \times \sqrt{\frac{B_1}{B_2 + B_3}} \tag{2.21}$$

where

$$B_1 = \frac{\left(K_4 + K_5 + \frac{2K_6}{(V_{DD} - V_{th})} \right)}{R_L} \tag{2.21a}$$

$$B_2 = M^{-2} R_L f_c (K_1 + K_2) \sum_{i=0}^{N-1} t^{-i} \tag{2.21b}$$

$$B_3 = \frac{2M^{-2} K_3 R_L (V_{DD} - 2V_{th})^3}{V_{DD}^2} f_c \tau \sum_{i=0}^{N-1} t^{-i} \tag{2.21c}$$

From equation (2.21), the highest efficiency of the CDA output stage can be obtained by optimizing the channel width W_P for a desired modulation index M.

We will use part of the abovementioned approach for our design and optimization of output stages for mid-voltage mid-power applications in the subsequent chapters in this dissertation.

2.4 Conclusions

This chapter has reviewed the classical linear amplifiers (Class A, Class B and Class AB), the less-known Class C, Class E, Class G and Class H amplifiers, and CDAs. Of all these classes, the CDA features the highest power efficiency. The modulation techniques of the CDA have also been reviewed and PWM is the most popular choice in industry due to its relatively simpler circuit design and lower power consumption, and with relatively good signal fidelity. Different output stage configurations have been reviewed and it was concluded that the *n*-channel totem pole output stage is preferred in this research programme due to its smaller area (thus higher power efficiency). Finally, the power dissipation of the CMOS output stage has also been reviewed.

Chapter 3

Analysis and Design of a CDA Output Stage based on DMOS

As delineated and reviewed in chapter 2, the mechanisms of power dissipation and the optimization of the Class D output stage based on CMOS technology for low voltage applications are established in literature [Chang, *et.al*., 2000]. However, the mechanisms of power dissipation of the Class D output stage based on Double-diffused MOS (DMOS) technology and the methods to optimize its power efficiency remain unreported in literature. Specifically at this juncture, the design methodologies to reduce power dissipation and to improve power efficiency for a DMOS output stage are empirical. For example, it is well-known that a lower output on-resistance usually yields lower power dissipation and hence higher power efficiency but at the cost of larger IC area, and that it is generally desirable that the output resistance be as low as tolerable.

At the outset, we remark that the design considerations for low voltage (5V and below) and higher voltage (20V) CDAs are different. In this chapter, the challenges of higher voltage applications will be first discussed, including the various protection circuits typically employed. We will thereafter investigate the mechanisms and derive the analytical expressions of power dissipation in a Class D output stage in DMOS technology. Based on these analyses, the power efficiency of DMOS Class D output stage is obtained. The derivation of the expression for power dissipation is significant as it provides insight to the designer on how various parameters can be varied and/or compromised to meet a given set of specifications. The analytical expressions are verified by comparing them against Cadence (Spectre) computer simulations and against practical measurements on a prototype IC.

This chapter is organized in the following manner. Section 3.1 presents some of the limitations of the CMOS output stage for high voltage operation, and these, in part, justify the need for a DMOS or HVMOS output stage. For completeness, protection circuits are also discussed. In section 3.2, the DMOS technology is reviewed as a preamble to our investigations. In section 3.3, the mechanisms of power dissipation in a DMOS Class D output stage are investigated and analytical expressions derived. The analytical derivations are verified with computer simulations and by measurements on an IC. In section 3.4, an analytical method to optimize the DMOS output stage for high power efficiency (in view of IC area) is presented. Finally, conclusions are drawn in section 3.5.

3.1 Challenges of Higher Voltage (20V) Application

In chapter 2, we reviewed the efficiency and optimization of the CMOS output stage for low voltage applications, typically $\leq$ 5V, and they are not directly applicable to a mid-voltage (20V) CDA for TV applications. Nonetheless, as we will later show, with some appropriate modifications made to the low voltage CMOS output stage model, the CMOS output stage model can be extended and hence applicable to higher voltage applications.

A higher voltage application (20V) poses a different set of challenges from the low voltage application. First, the most direct limitation is the process limitation of CMOS technology (low breakdown voltage, typically 5V) which requires the use of either High-Voltage MOS (HVMOS) or DMOS technology. Second, the high short-circuit current power dissipation, arising from the higher supply voltage, potentially reduces the power efficiency of the CDA to an unacceptable level. For a practical application, this short-circuit current loss should be limited or ideally be completely eliminated to retain the desired high power efficiency attribute of the CDA. Third, the higher supply voltage leads to an increased internal power dissipation of the IC. This will increase the likelihood of damage to the IC, in particular during transitions where short-circuit occurs. In practical design, protection circuits, in particular over-current protection, are embodied

to limit the short-circuit current. The following sections will address the abovementioned challenges.

3.1.1 Limitations of CMOS Output Stage at High Voltage

CMOS technology is very well established and despite its prevalence, it is typically only able to operate up to 5V due to the breakdown voltage of its *pn*-junction. Additional diffusion steps, such as that required for a HVMOS process, are needed to increase the breakdown voltage. One drawback of this HVMOS process is the larger minimum channel length between the source and drain to prevent breakdown, and the corresponding increased area for the realization of a transistor and hence the overall increased IC area. Ultimately, this increases the on-resistance (R_{on}) per unit area.

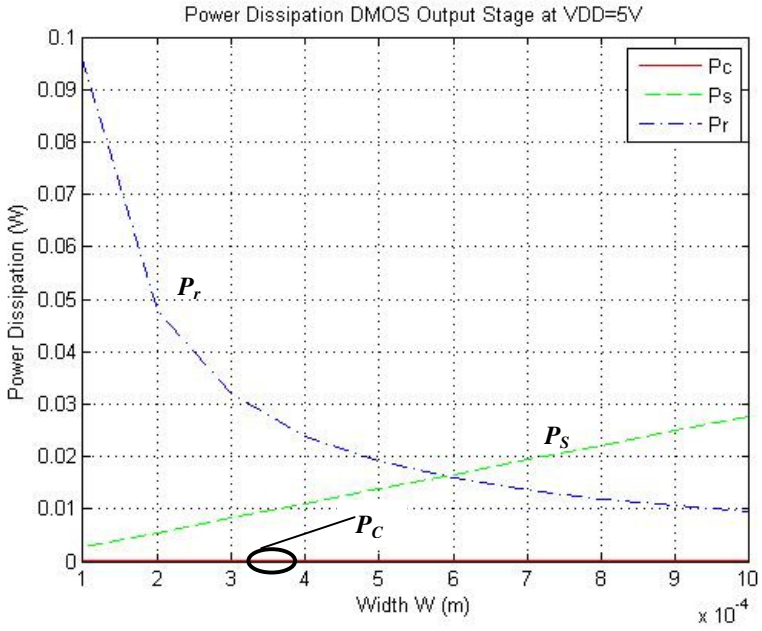
With a higher R_{on} per unit area compared to CMOS, a larger width, W, is usually adopted to keep the overall R_{on} of the output stage low. However, this larger transistor size not only adds on to the cost of a larger silicon area, it increases the parasitic capacitance of the output stage. From equation (2.12), it is easy to appreciate, and as expected, that a larger capacitance will increase the power loss P_C. If there is an increased R_{on}, from equation (2.13), the power loss P_r will increase.

In short, it can be appreciated that in order to retain or improve the power efficiency, R_{on} needs to be reduced without increasing the size of transistors or the size must be reduced without increasing the R_{on}. Compared to HVMOS, DMOS has the advantage of a high breakdown voltage and yet with a low R_{on} per unit area. Put simply, compared to HVMOS, the DMOS output stage can potentially achieve higher power efficiency and with a smaller IC area. A review on DMOS technology will be presented in section 3.2.

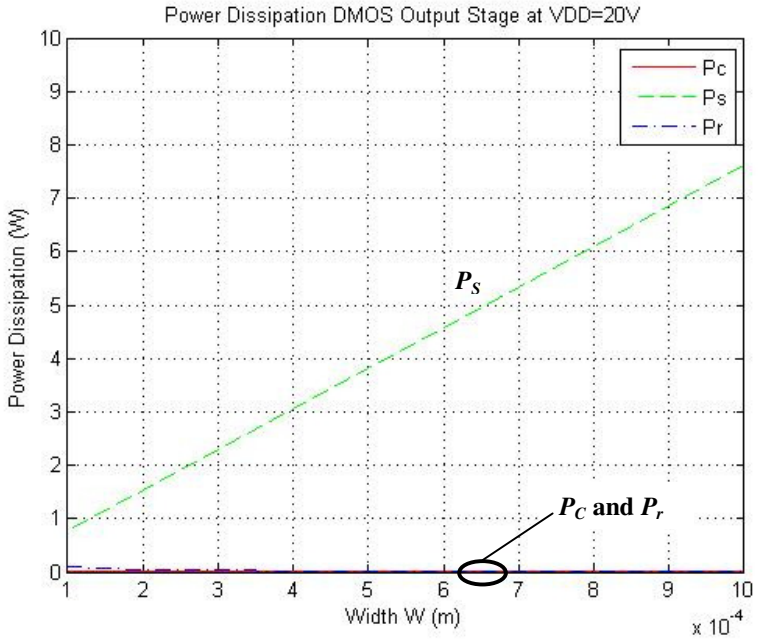
3.1.2 Short-circuit Current at High Voltage

As delineated in chapter 2, the short-circuit [Elmasry, 1981; Veendrick, 1984; Haznedar, 1991] current occurs during the transition time when both the top transistor and the bottom transistor of the output stage conduct simultaneously. The short-circuit current flows from the supply to ground. This can occur both to an inverter output stage (comprising a *p*-type and an *n*-type transistor) and the totem pole *n*-channel output stage (comprising only *n*-type transistors). For a low voltage application, this power dissipation is small and is usually tolerable. However, the short circuit current loss expression in equation (2.16) shows that a higher V_{DD} will increase the power dissipation by $(V_{DD}\text{-}2V_{th})^3$.

To exemplify the above, we simulate by means of MATLAB (to numerically compute equations (2.12), (2.13) and (2.16)) to depict in Figures 3.1(a) and 3.1(b) the power dissipations due to the on-resistance, parasitic capacitance and short circuit current for a CDA output based on DMOS for 5V and 20V respectively. The parameters are shown in Appendix A. Unlike low-voltage, it is apparent that at higher voltage (20V in Figure 3.1(b)), the short circuit current loss is dominant as P_c and P_r are relatively negligible. It is, hence, necessary to modify the output stage designs such that the short circuit current power dissipation is mitigated. In literature, this is usually achieved by adding a dead time block before the output stage to delay the turning on of one of the transistors so that at no time will the two transistors be turned on simultaneously to allow the flow of the short-circuit current. By means of HSPICE simulations on ideal models, we find that a dead time of 20 ns can reduce the short-circuit current to almost zero.



(a)



(b)

Figure 3.1 Power dissipations of a DMOS Output Stage at (a) 5V, and (b) 20V

Figure 3.2 illustrates the well adopted and well established method [White, *et. al.*, 2006; Apex Microtechnology, 2001; Morrow, 2004] of adding a dead time into the Class D output stage to ensure that both transistors do not turn on simultaneously.

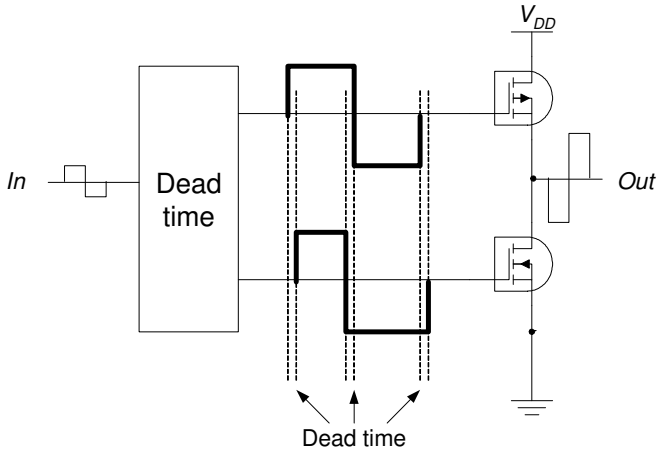


Figure 3.2 Class D output stage with dead time

There are several ways of implementing the dead time circuit. One method [White, *et. al.*, 2006] involves skewing the turn on and turn off times for each power switch transistor to implement a dead time such that neither transistor is on. This is achieved by creating the output stage with a relatively smaller (weaker drive) top transistor and a bigger (stronger drive) bottom transistor which yields a long rise time and a short fall time, as that shown in Figure 3.3. The dead time is accomplished by skewing the sizing ratio of transistors in the driver stage with skew factor, s. In Figure 3.3, t is the tapering ratio and a is the ratio of electron/hole mobility. In one reported design [White, *et. al.*, 2006], the output transistor size is 5190 µm for the P switch transistor, with a skew factor of $s = 3$ and tapering ratio of $t = 13$. These parameters yield a dead time of 40 ns, and the short-circuit current is virtually eliminated.

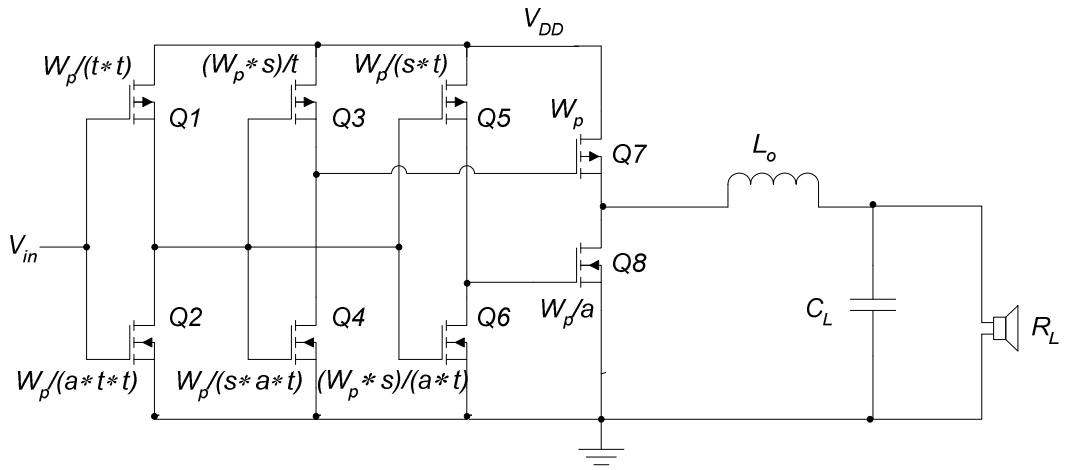
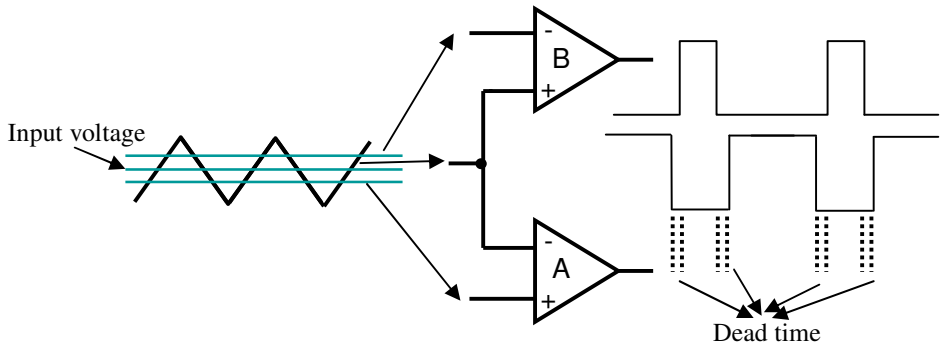
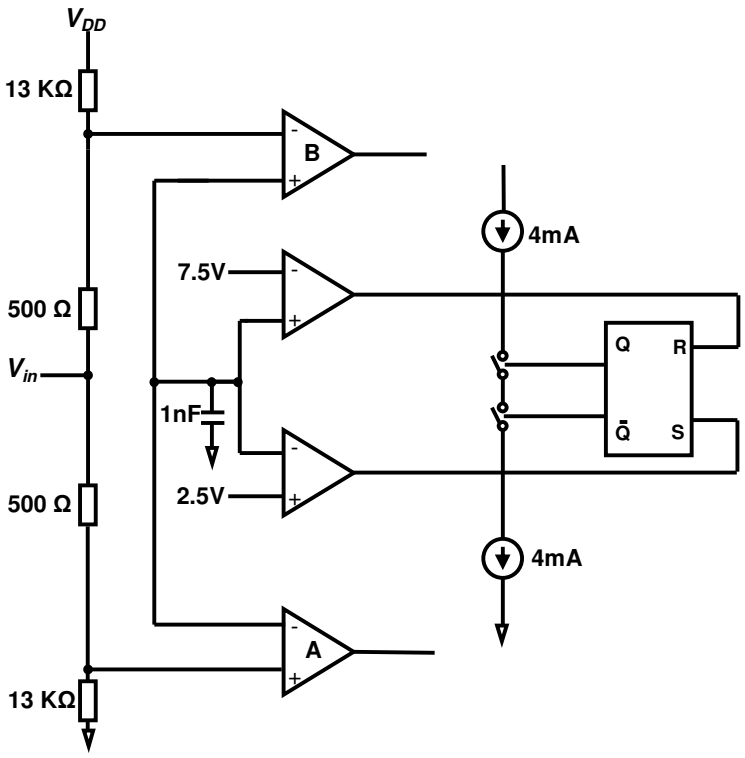


Figure 3.3 Dead time design by skewing method

Another reported method [Apex Microtechnology, 2001] pertaining to the *n*-channel totem pole output stage, involves creating an offset voltage in the input signal, as shown in Figure 3.4(a). This is done by pushing the input signal through a small resistor as shown in Figure 3.4(b) so that the dc voltages of the input seen by the comparators are slightly different which in turn modifies the duty cycle proportionally. Comparator A sees a slightly lower DC voltage compared to the input signal while comparator B sees a slightly higher dc voltage. These positive and negative voltage offsets produce a slightly shorter duty cycle in both comparators and thus create a dead time where both the upper and lower switches are off. Although the voltage drop across the 500 Ω resistors varies with the input signal, the total dead time is still constant because as one voltage drop decreases, the other will increase to compensate.



(a)

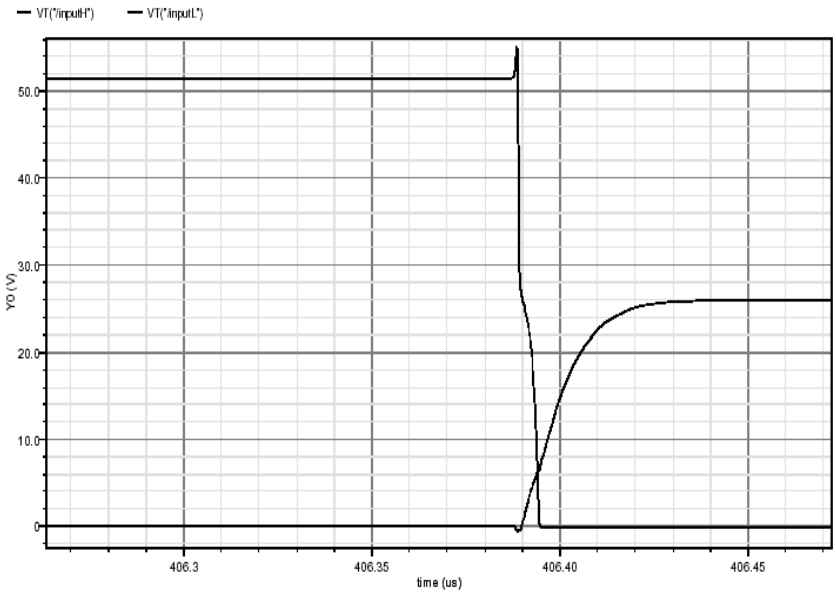


(b)

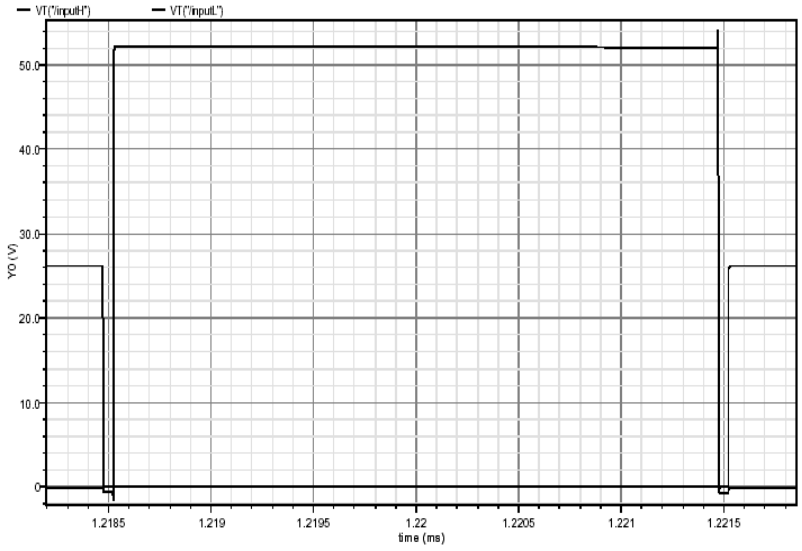
Figure 3.4 Dead time design by offset voltage (a) Block Diagram, and (b) Circuit Diagram

Of the two reported methods, the former yields a very simple design which can be implemented very easily just by skewing the size of the driver stage. However, it is not easy to control the dead time as it is dependent on the delay of rise time and fall time at the driver stage. With this delay, there is a chance that one of the transistors has not been turned off completely yet while the other turns on and this can still cause a small short-circuit current. We simulate both reported design methods. The simulated waveform of the gate voltages of the power transistors for the former approach is shown in Figure 3.5(a). Evidently, there is still a small overlap and a small short-circuit current can occur.

In Figure 3.5(b), the waveforms of the gate voltages of the latter approach are depicted. The waveforms are more well-defined making it less likely for short-circuit current to occur. However, the cost of this latter approach is an additional comparator.



(a)



(b)

Figure 3.5 Gate voltages of power transistors for (a) skew method and (b) offset voltage method

In summary, the latter method [Apex Microtechnology, 2001] is preferred, despite its higher quiescent current, because a short-circuit current (especially at high voltage application) is dominant.

Having a dead time does not necessarily guarantee that there will not be any short-circuit current. As the Class D output is typically connected to energy storage elements (the output filter), there may be a delay in switching off the power transistor. This delay can be both dependent on the size of the power transistor and the output signal. If this delay is longer than the dead time, a short-circuit can occur. One reported method [Morrow, 2004] to address this problem is to create a non-overlapping circuit in the driver stage by means of logic circuits. The logic circuit is designed to ensure that the top transistor must be in the 'off" state before the bottom transistor can be turned 'on'. In the same way, it is also required for the bottom transistor to be 'off" before the top transistor can be turned 'on'.

The design of this reported method is shown in Figure 3.6 for one output of a full bridge output configuration. Transistors $a1$ and $a2$ are for the first channel while $b1$ and $b2$ are for the second channel. The delay blocks shorten the duty cycles of both the top and bottom transistors to create the dead time. The non-overlapping logic (consisting of the NOT, NAND and NOR gates) further ensures that at no time will both transistors turn on simultaneously. For example, when $a2$ is still 'on', its gate will have the logic '1'. Going backwards through a NOT gate will give a '0' logic for $a2\_off$. With a '0' input, the NAND gate will output a '1'. This in turn will give a '0' logic for the output of the NOR gate regardless of input signal at *IN*. The logic '0' going through the *P*-gate drive will give the logic '1' at the gate of $a1$ and this ensures that $a1$ will not switch 'on'.

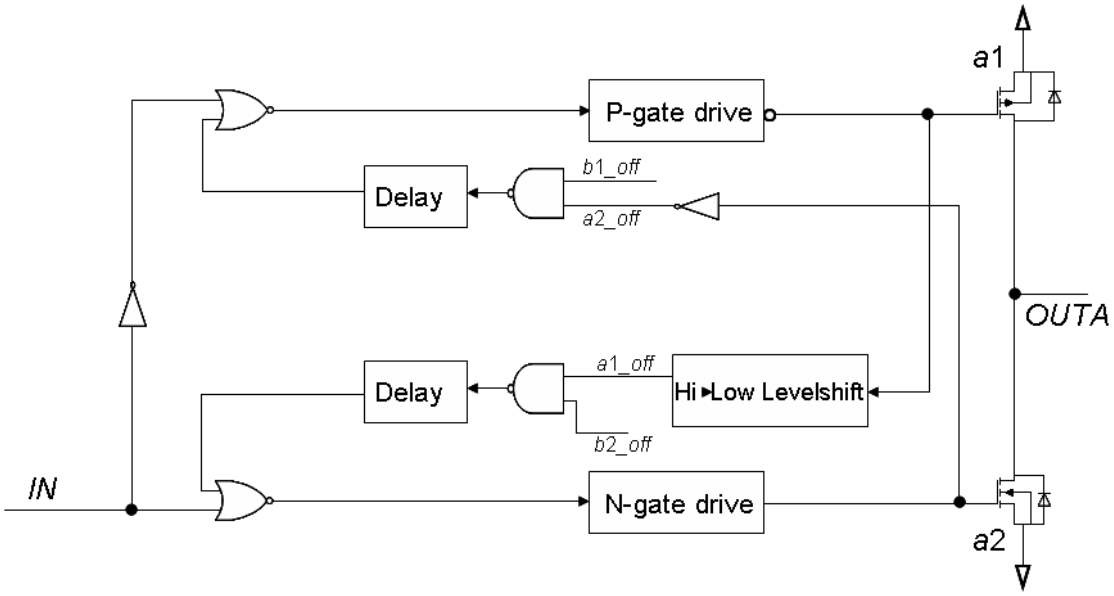


Figure 3.6 Dead time design with non-overlapping logic

3.1.3 Over-current Protection

As mentioned earlier, a higher supply voltage will likely increase the internal power dissipation of the IC which will in turn increase the likelihood of IC damage. This section will review the possible damage to the Class D output stage and the protection needed, in particular over-current protection.

Figure 3.7 shows the safe operating area (SOA), wherein a power transistor must operate, to avoid damage. The SOA of a typical power transistor has 3 limits [Berkhout, 2005]. The first is the maximum drain-source voltage limit, BV_{DS}, which is the largest voltage a power transistor can withstand without suffering from avalanche breakdown. Second, there a maximum current limit I_{MAX}, which is often determined by electro-migration in the metallization and bonding wires. Third, there is the maximum power dissipation limit P_{MAX}. This limit depends on the duration of the dissipation and the ability/capacity of the IC package to dissipate heat.

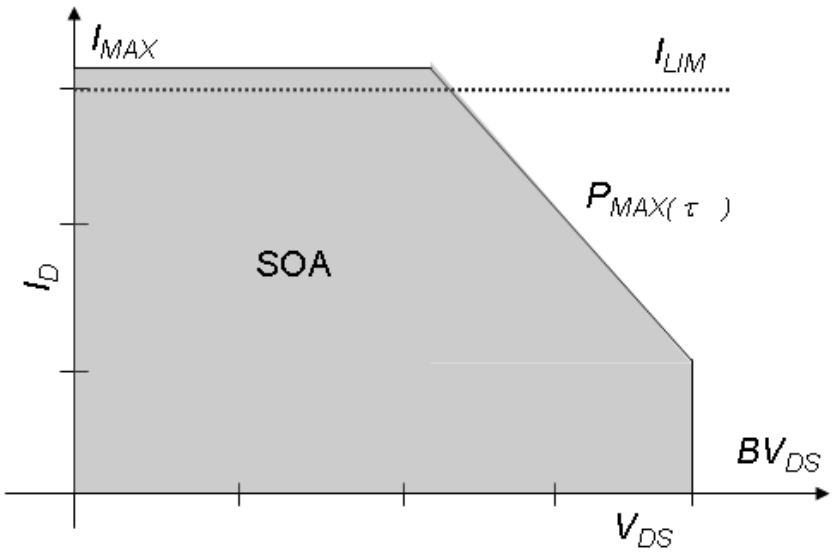


Figure 3.7 Safe Operating Area (SOA)

For a Class AB output stage, the power dissipation is often deemed the most important limit [Berkhout, 2005]. This is not the case for CDA where its power transistors are either switched 'off' or fully turned 'on'. In the 'off' state, no current flows through the transistor and the only concern then is the voltage limit. When the transistor is fully 'on', the power dissipation is usually related to the R_{on} of the power transistor. In a properly designed CDA, the R_{on} is very small (especially in DMOS technology), typically 0.1 ~ 0.3 Ω for an 8 Ω output load, and its SOA limit intersects with I_{MAX} rather than P_{MAX}. In this case, current limiting becomes the main concern in protection. If the current limit, I_{LIM}, is designed to be just below I_{MAX} of the SOA, the most economical size of the power transistors will be achieved without compromising reliability. Put simply, over-current protection design with well defined limits is highly desirable.

A well known (and typical) over-current protection circuit used in both CDA and Class AB amplifiers is shown in Figure 3.8. In the top power transistor, M_H, the current flowing into this transistor is detected by means of the voltage drop across the series resistor R_H. As the load current increases, the voltage drop across R_H will increase until it switches the state of the comparator. This in turn will send a signal to switch off the power transistors. There are two issues with this design. First, as R_H is in series with the power transistor, the power efficiency of the amplifier is compromised as the load current

must flow through this sense resistor. Hence, it is important to design R_H to be as small as possible. R_H is usually achieved by the metal resistance in the integrated circuits and the accuracy for such a small resistance (in milli-ohms) is very difficult to realize due to the tolerance of typical fabrication processes. Further, the resistance can vary due to process spread and temperature variations.

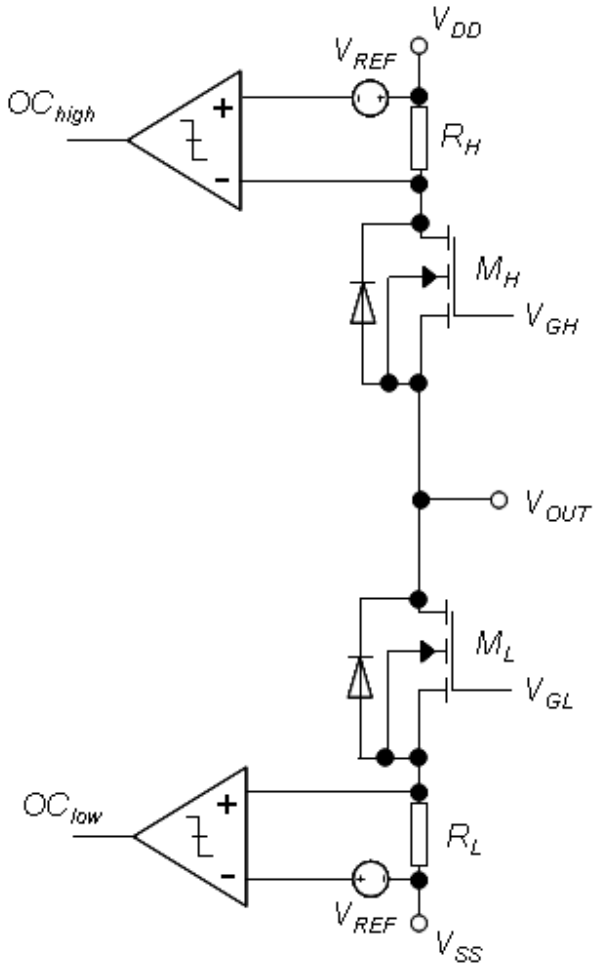
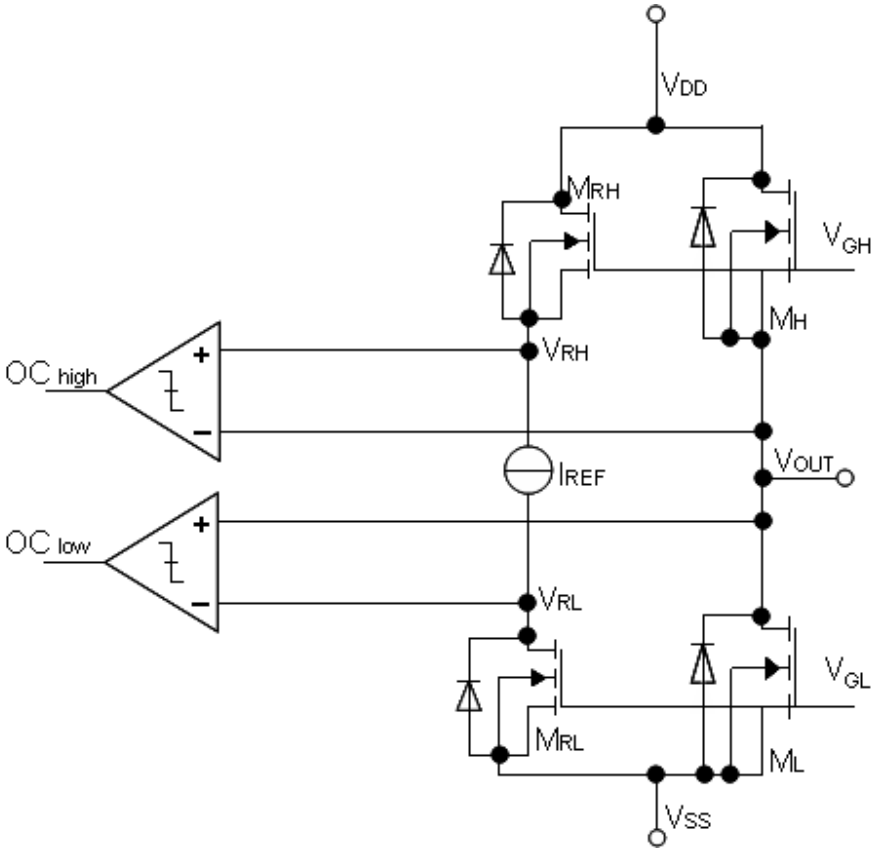


Figure 3.8 Conventional over-current protection

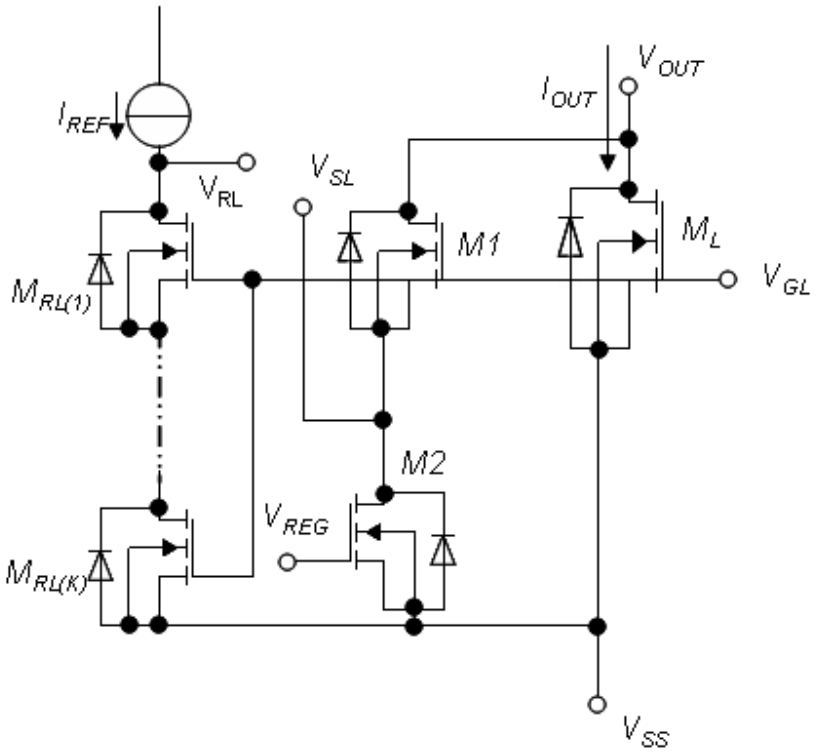
A more recent approach [Berkhout, 2005] is shown in Figure 3.9(a), implemented for the *n*-channel only totem pole output stage. In this design, the current through the power transistors is monitored by the voltage difference between V_{RH} and V_{OUT} for the upper power transistor M_H, and V_{RL} and V_{OUT} for the lower power transistor M_L. V_{RH} and V_{RL}

are reference voltages generated by the reference current I_{REF} flowing through the N-times smaller replica transistors (M_{RH} and M_{RL} respectively).

This design poses some complexity as it can only work if the power transistors are fully turned 'on', which is true for only half a cycle. In the positive cycle (M_H is delivering a current with M_L being switched 'off'), V_{OUT} will drop according to the output current flowing through its R_{on}. When the output current exceeds a certain designed threshold, OC_{high} will be triggered. Similarly, in the negative cycle, when the current flowing through the lower power transistor M_L exceeds the threshold, OC_{low} will be triggered. In the same way, the comparator can only be active if the corresponding power transistor is turned 'on'. For example, if the lower power transistor is switched 'off', the output voltage will be close to V_{DD}. This voltage will be higher than V_{RL} which will cause the lower comparator to trigger incorrectly.



(a)



(b)

Figure 3.9 (a) [Berkhout, 2005] Over-current protection, and
(b) Improved [Berkhout, 2005] over-current protection

To correct the problem, additional circuits [Berkhout, 2005] are added as shown in Figure 3.9(b). Since the concept is similar, only the lower side design is discussed. *M1* and *M2* are added where the gate and drain of *M1* are connected to the gate and drain of M_L respectively. *M2* is being turned 'on' all the time. Instead of sensing the voltage at V_{OUT}, which is constantly switching, the voltage at the source of *M1* (V_{SL}) is sensed. V_{SL} is being compared with the reference voltage V_{RL}, which is generated by I_{REF} through a series of transistors $M_{RL(1)}$ to $M_{RL(K)}$. When the power transistor M_L is turned 'on', both *M1* and *M2* are in triode region and they function as a linear voltage divider, reflecting a linear fraction of the drain-source voltage of the power transistor M_L. This results in an increase of the ratio *N*, depending on the size of *M1* and *M2*. When M_L is switched 'off', *M1* will be switched 'off' as well. With *M2* being turned 'on' all the time, V_{SL} will be pulled low and this does not trigger the comparator. The sense voltage V_{SL} will only

exceed the reference voltage V_{RL} when the power transistor M_L is switched 'on' and the output current I_{OUT} exceeds the over-current limit $I_{LIM} = I_{REF} * N$.

In summary, we have reviewed the problems faced by the conventional over-current protection circuit and improvements thereof. We recommend the improved design for practical output stage designs.

3.2 A Review on DMOS Technology

In this section, we will review DMOS technology as a preamble to our investigation into the design and optimization of the DMOS output stage.

DMOS technology is a variation of a MOS structure that addresses many of the voltage and on-resistance limitations of the conventional CMOS transistors. There are two main differences between the conventional CMOS Transistor (CMOST) and the DMOS Transistor (DMOST).

First, the channel length of a DMOST is formed by the difference between two sequential diffusions moving in the same direction from a common starting point [Antognetti, 1986] and this enables the channel length to be controlled easily down to a small feature size, below 0.5µm. A cross-section of an *n*-channel DMOST is depicted in Figure 3.10. The channel of the CMOST, on the other hand, is formed by the diffusion of the source and drain (shown in Figure 3.11) in the opposite direction and this, in some cases, makes the channel length more difficult to control compared to DMOST. The current-art minimum feature size of CMOS structures is very fine, down to 45 nm at this juncture. As delineated earlier, typical CMOS processes have a low breakdown voltage.

Second, as the channel (body) region of the DMOST is more heavily doped compared to the *N*- drain region, the junction will deplete further into the drain region than into the channel region when a reverse bias is applied across the drain-to-body junction. This enables the drain-to-body junction to withstand a significantly higher voltage with little

effect on the channel length. Conversely, in the case of a CMOST, when a large voltage is applied over the drain and source, the junctions will deplete at a quick rate into the lightly doped *P*- substrate, affecting the channel length between the drain and source. Since the junctions of the drain and source deplete quickly in the opposite direction toward each other, breakdown occurs very easily as the two depleted regions meet. It is also interesting to note that as the channel region of a DMOS is more heavily doped compared to CMOS, the DMOST has a lower channel resistance, hence, the potential to increase the power efficiency in an output stage of a CDA. The channel resistance of a CMOST, on the other hand, is known to be higher due to the higher resistivity of the channel material.

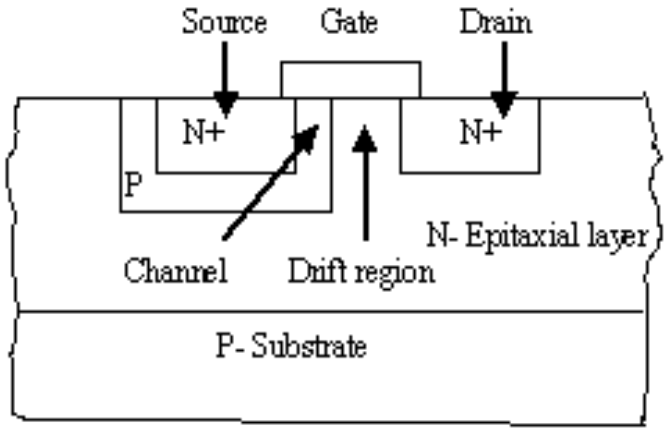


Figure 3.10 Cross-sectional view of a DMOST

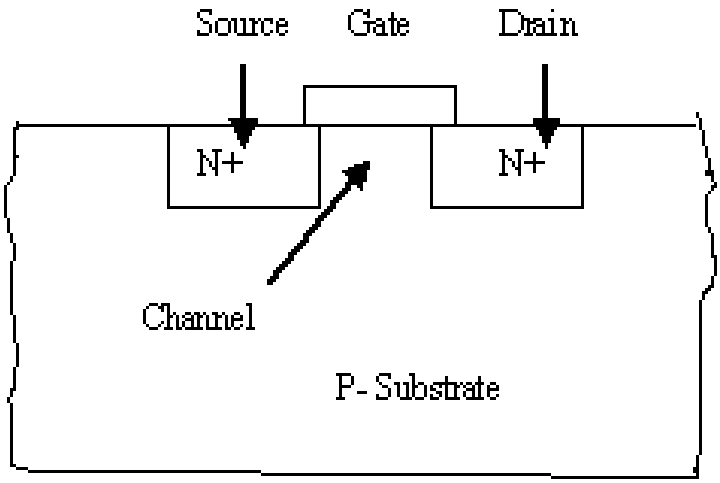


Figure 3.11 Cross-sectional view of a CMOST

Two of most common DMOS structures are the lateral DMOS (LDMOS), depicted in Figure 3.12, and the vertical DMOS (VDMOS), depicted in Figure 3.13. A significant difference between them is that the drain contacts of the LDMOS are made on its top surface. This structure is consequently larger than VDMOS, thereby compromising the layout efficiency, hence increased IC area and cost. On the other hand, the VDMOS does not have a drain contact at every source interval but the whole buried *N* layer forms the drain. This allows the VDMOS structures to be more densely packed.

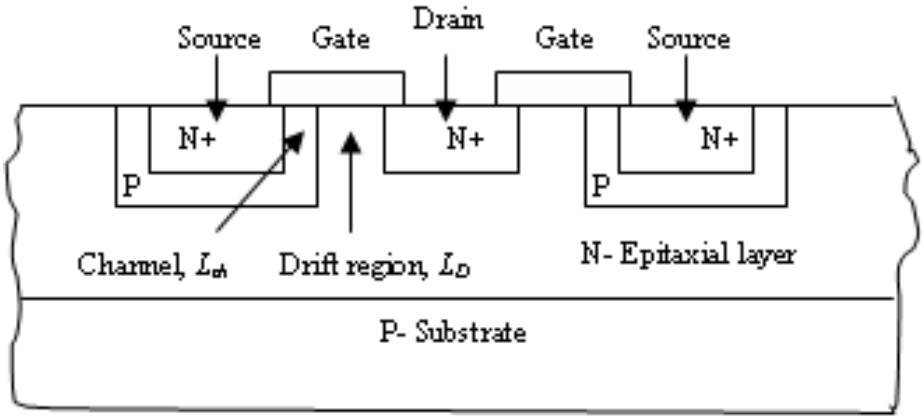


Figure 3.12 Cross-sectional view of LDMOS

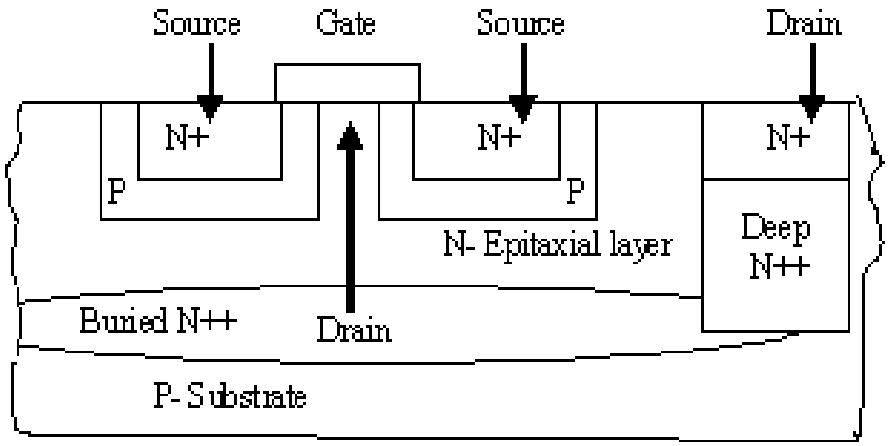


Figure 3.13 Cross-sectional view of VDMOS

From Figure 3.13, it is obvious that the drains of all the VDMOS are common. Since the drain forms the whole epitaxial layer, it is usually connected to the most positive potential, V_{DD}. This becomes a design constraint for VDMOS. By comparison, it is easier for design and connectivity in LDMOS as all the drains are separate and they can be connected individually.

VDMOS has the advantages of a higher breakdown voltage and a smaller overall area (due to the VDMOS having a smaller number of drain diffusions and contacts at the surface as shown in Figure 3.13) compared to LDMOS. However, having a smaller number of drain contacts will mean that its on-resistance is higher. LDMOS is preferred when designing for lower voltage application. As the path from drain to source is shorter, the on-resistance is lower. Moreover, with its gate extending to the *N*+ region, the resistance in the drift region is greatly reduced during conduction. This results in the LDMOS conducting a higher current per unit area.

In summary, as the power efficiency of the output stage for a mid-power CDA is the parameter of interest in this project, we recommend that LDMOS be used. It is more suitable largely because of its lower on-resistance.

3.3 Power Dissipation Mechanisms of DMOS Output Stage

We will now investigate the power dissipation mechanisms of the DMOS output stage. Specifically, our interests are to derive its efficiency and finally determine the optimum size of the output stage for highest power efficiency in view of IC area, as delineated in chapter 1 earlier.

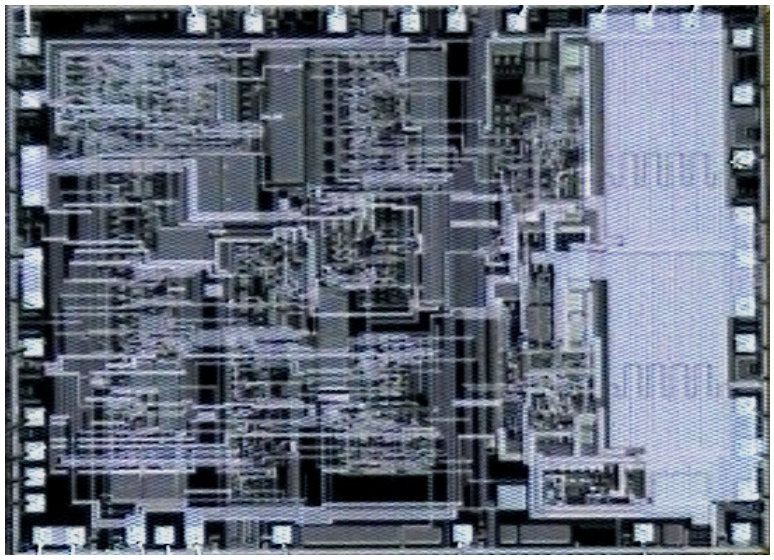


Figure 3.14 Picture of Class D Amplifier IC

In order to verify our theoretical work, an output stage is being fabricated using a proprietary 0.27μm, 15V DMOS process. A picture of the IC is depicted in Figure 3.14. As the design of the entire CDA remains the intellectual property of the sponsoring company, no process parameters can be shown and no circuit design will be discussed. In the next chapter, however, a detailed analysis will be presented based on a HVMOS process with its process parameters shown.

The block diagram of a typical Class D amplifier embodying a DMOS output stage (*n*-channel totem pole) in a full bridge configuration is shown in Figure 3.15 where V_{DD} is the supply voltage, V_S is the input signal, V_C is the triangular carrier signal, L_O, C_O and

C_L form the output filter and R_L is the resistor load. A PWM modulator as described in chapter 2 is used due to its circuit simplicity and low power dissipation. In this design, the *n*-channel totem pole output stage is used (as opposed to the *p*-channel-cum-*n*-channel inverter output stage) as the *n*-channel transistor is smaller in size compared to the *p*-channel transistor (see chapter 4 later). A smaller (sized in terms of IC area) output stage will result in a lower power loss, and hence higher power efficiency.

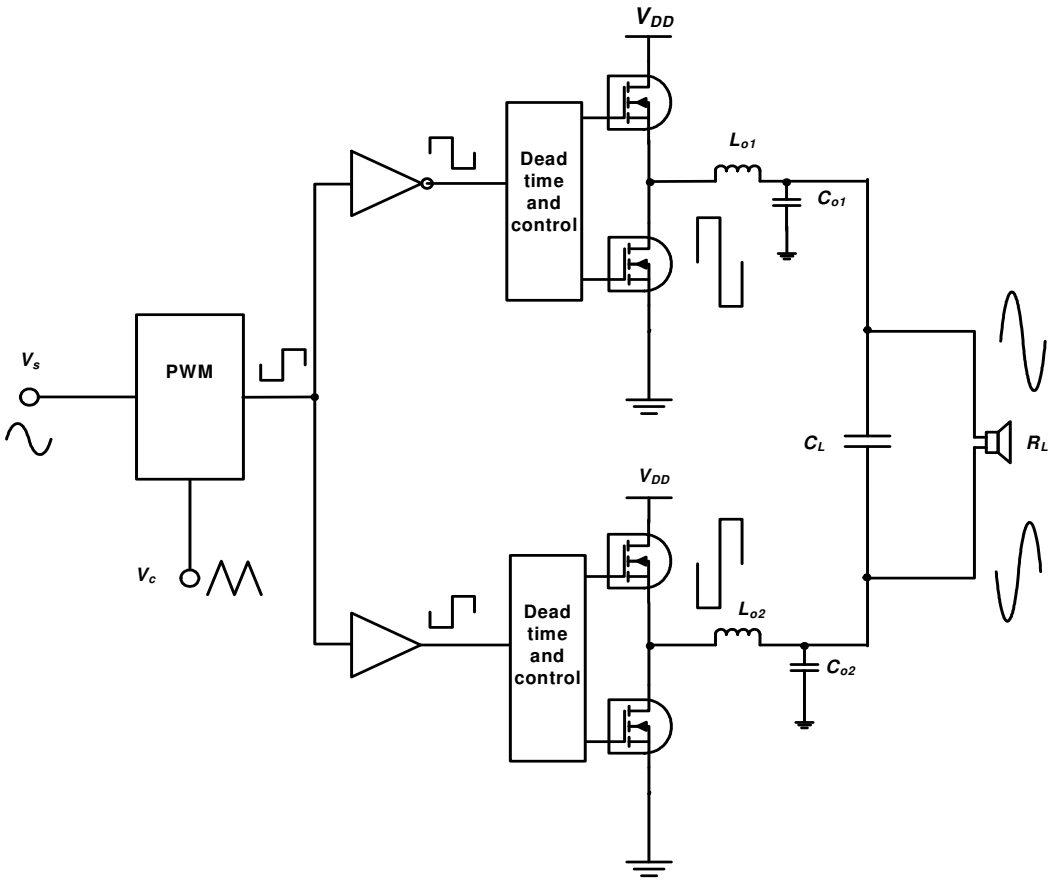


Figure 3.15 Block diagram of a PWM CDA embodying a DMOS output stage

The details of the DMOS output stage design in a full bridge configuration is depicted in Figure 3.16. Since the positive and negative channels are identical, only the positive channel is shown for simplicity of discussion. *Q1* and *Q2* form the *n*-channel totem pole DMOS output stage. *Q3* and *Q4* form the inverter pair for the top power transistor driver

while *Q5* and *Q6* form the bottom power transistor driver. As the top power transistor (*Q1*) is an *n*-channel transistor, a bootstrap is needed to supply a higher voltage to *Q3* to drive *Q1*.

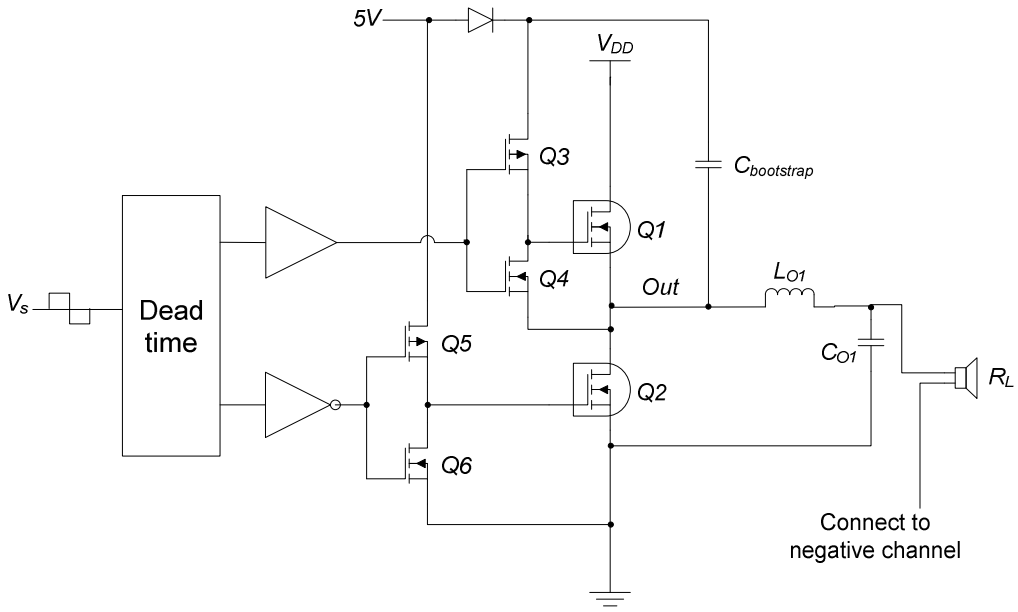


Figure 3.16 Block design of the DMOS output stage

From a simplistic view point, and using the analysis reported by [Chang, *et.al.,* 2000] for a CMOS output stage, the DMOS output stage can be modeled by two switches and an *LC* low pass filter as depicted in Figure 3.17. The output current through the load R_L is:

$$i_o(t) = DI_o \sin(2\pi f_s t) \tag{3.1}$$

where $I_o = (V_{DD}/R_L)$ is the maximum output current,

D is the duty cycle and

f_s is the input signal frequency.

In this model, the power dissipation due to leakage current in the reverse *pn*-junctions are not considered as it is negligible, even in micropower circuit designs [Vittoz, 1977; Castello and Gray, 1985].

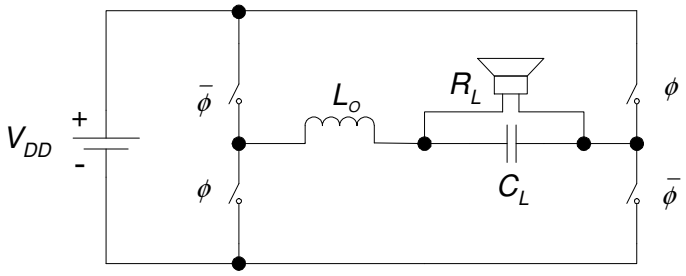


Figure 3.17 Full bridge output stage modeled by switches

To obtain a more precise model of the DMOS output transistor, consider first the difference between CMOS and DMOS. Figure 3.18 depicts the large signal model of a 4-terminal CMOS transistor (*D*, *G*, *S* and *B* represent the drain, gate, source and body respectively), which includes its parasitic capacitances and resistances. This model depicts the overall parasitic capacitance seen at the gate (which includes the gate-drain overlap capacitance C_{GDO}, the gate-body overlap capacitance C_{GBO} and the gate-source overlap capacitance C_{GSO}), the overall parasitic capacitance seen at the drain (which includes C_{GDO} and drain-body capacitance C_{BD}) and the parasitic resistance seen from the drain to source (which includes the drain resistance r_d and the source resistance r_{so}).

On the other hand, the DMOS model, which includes the 4-terminal MOS transistor in Figure 3.18, can be derived from the cross-sectional diagram in Figure 3.12 and is presented in Figure 3.19 (referenced from the process file). The relevant point in this model is that in the DMOS, its body and source are shorted to form only a 3-terminal device. The gate capacitance of a DMOS is the total gate capacitance of a MOS model and an extra gate-drain capacitance C_{GD}, which is the gate area overlapping the drift region as seen in Figure 3.12. From this model, it can also be seen that between the drain to source there is an epitaxial resistance R_{epi} and a body diode D_{BD}. A parasitic *pnp* transistor can also be found from Figure 3.12 with its emitter connected to the body (*p*-doped area under the source) of DMOS, base connected to the drain of DMOS and collector connected to the substrate of DMOS. $R_{epi\text{-}base}$ and R_{col} represent the base resistance and collector resistance of the parasitic *pnp* transistor. Finally, the drain

epitaxial region forms a *pn*-junction with the substrate, represented by D_{Dsub} and R_{sub} represents the substrate resistance.

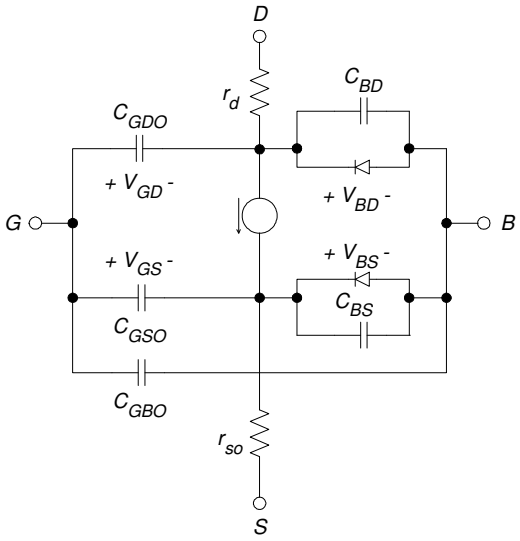


Figure 3.18 Large signal model of MOS transistor

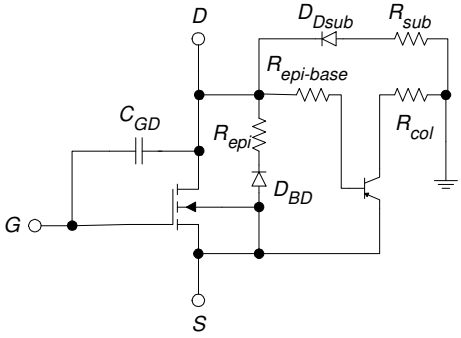
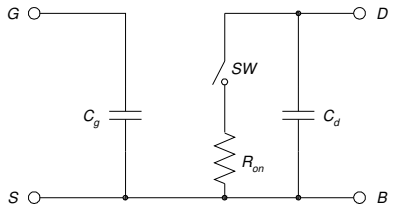


Figure 3.19 SPICE DMOS Model

In the consideration of power dissipation, the resistance across the drain and source, and the capacitance of the gate and drain are of particular interest. From the perspective of the SPICE DMOS model depicted in Figure 3.19, these pertain to parameters C_{GD} and R_{epi} and they will be later used to determine the power dissipation.

With the current source in the MOST (inside the DMOS model) modeled as a switch (*SW*) in series with a resistor during turn-on (and ignoring all other reversed-biased junctions that are not turned on), the lumped model of the DMOS transistor is similar to that of CMOST and is depicted in Figure 3.20.



C_g = lumped gate capacitance
C_d = lumped drain capacitance,
R_{on} = lumped on-resistance.

Figure 3.20 Lumped model of DMOS transistor

This lumped large signal model will be used later to describe the power dissipation mechanisms. In the following sections, we will also analyze the dominant power dissipations, P_C, and P_r in DMOS in detail. A single *n*-channel DMOS is considered in our analysis.

3.3.1 Power Dissipation Due To Parasitic Capacitance

In the positive switching cycle of the CDA output stage, charges are provided from the supply and stored in parasitic capacitances. These same charges are discharged to the ground in the negative switching cycle without any work done on the load. This power is hence dissipated in the IC as heat and is wasted. The calculation of the power dissipation due to parasitic capacitance remains largely similar to the CMOS output stage as reported in literature [Chang, *et.al.*, 2000]. The main differences, as we will now delineate, is in the modeling of the parasitic capacitances.

From the SPICE model, the gate capacitance of a single DMOS transistor is modeled as a MOS transistor with a short channel length and a gate-drain capacitance, C_{gd}, between the gate and the drift region. Reported characterization [Liu, *et.al.*, 1997] has shown that the capacitance effect of the gate oxide upon the drift region cannot be simply modeled by the gate drain overlap because the capacitance changes as the gate voltage changes. In the DMOS fabrication process used in this research programme, C_{gd}, is modeled by the verilog-A function as follows:

$$C_{gd} = \frac{C_{V1} \times C_{V2}}{C_{V1} + C_{V2}} \times \frac{W}{W_{unit}} \tag{3.2}$$

$$C_{V1} = c1 \times \left(1 + e^{k1 \times V_{DD} + offset1}\right) \tag{3.3}$$

$$C_{V2} = c2 \times \left(1 + e^{k2 \times V_{DD} + offset2}\right) \tag{3.4}$$

where $c1$, $c2$, $k1$, $k2$, $offset1$ and $offset2$ are process dependent parameters. They are simply constants obtained from the measurements/characterization of a fixed unit size transistor model of width W_{unit}. Hence, the total capacitance of C_{gd} is obtained simply by multiplying the factor of W/W_{unit}, where W is the total width of the output stage.

By adding the gate-drain capacitance, C_{gd}, to the well established MOS gate capacitance [David, *et.al*., 1997], the overall gate capacitance per transistor of DMOS is:

$$\begin{aligned} C_g &= [C_{gso}W + C_{OX}WL + C_{gdo}W + C_{gd}] \\ &= [(C_{gso} + C_{OX}L + C_{gdo})W + C_{gd}] \end{aligned} \tag{3.5}$$

where C_{gso} is the gate-to-source capacitance per unit width,
G_{gdo} is the gate-to-drain capacitance per unit width,
C_{OX} is the oxide capacitance per unit area and
L is the channel length.

In the determination of the drain capacitance, only the drain-to-gate capacitance is usually considered as it is dominant. The drain-to-substrate capacitance is formed by the epitaxial layer (*N*-) and the substrate (*P*-). As both the layers are lightly doped, the drain-

to-substrate capacitance are very small [Komachi, *et.al.*, 1997]. In our analysis, we will assume that the drain capacitance, C_d, is only modeled by the drain-to-gate capacitance.

$$C_d = [(C_j L_{DS} + 2C_{jsw} + C_{gdo})W + C_{gd}] \tag{3.6}$$

The source of the DMOS, shorted to its body, forms a parasitic capacitor with the epitaxial layer. As the epitaxial layer is lightly doped, this capacitance is relatively small. The overall source capacitance of the DMOS, C_s, is characterized by the process as:

$$C_s = k3 \cdot W + k4 \tag{3.7}$$

where $k3$ and $k4$ are process dependent parameters defined in the process file.

The total output parasitic capacitance, C_{OUT}, in the full bridge DMOS output stage includes 2 drains, 2 sources and that of the two interconnecting bond pads at the output stage.

$$C_{OUT} = 2C_d + 2C_s + 2C_{pad} \tag{3.8}$$

In the process used in our design, the DMOS power transistor has a 5V gate voltage limit (V_G = 5V), as defined by the process. The overall power dissipation due to parasitic capacitance of the DMOS output stage in full bridge configuration (includes the total output parasitic capacitance, C_{OUT}, and the capacitance from 4 gates) is simply:

$$P_C = \frac{1}{2} f_C \left\{ V_{DD}{}^2 C_{OUT} + V_G{}^2 (4C_g) \right\} \tag{3.9}$$

As expected, the power dissipation increases with switching frequency, f_c, and with supply voltage, V_{DD} and gate voltage V_G. From a power dissipation perspective, hence high power efficiency, it is of interest to keep f_c low. However, as discussed in chapter 2, it has been established that a low f_c has undesirable implications to the non-linearities of

CDAs. It is also important to keep the output transistor area and its parasitic capacitances to the minimum for low power dissipation, hence high power efficiency.

3.3.2 Power Dissipation Due to On-Resistance (R_{on})

The power dissipation due to on-resistance is highly dependent on the load current drawn that passes through the power transistors, and on the resistance seen in the path. As mentioned earlier, a mid-to-high voltage application draws considerable current and it makes this power loss significant. The on-resistance is the overall resistance seen from the drain to the source and includes the contact resistance, body resistance of the diffusion layer and the channel resistance when the transistor is turned on. As the sheet resistance of metal line is negligible, it will be ignored in this analysis.

The on-resistance of a LDMOS transistor comprises the body resistance, r_b, channel resistance, r_{ch}, and the drift region (epitaxial) resistance, r_{epi}, and these resistances will now be delineated in turn.

3.3.2.1 Body Resistance

The magnitude of the body resistance depends very much on the fabrication process and layout techniques. The body resistance consists of the sheet resistance of the drain and source and the contact resistance between metal and doped silicon, that is:

$$r_b = r_c + r_s \tag{3.10}$$

where b, c and s denote body, contact and sheet respectively.

Using the established methodology [Chang, *et.al.,* 2000] to determine the total body resistance of a CMOS transistor for a finger layout, we determine the same for a poly-gate DMOS transistor, depicted in Figure 3.21:

$$r_b = r_c + r_s = \frac{2[\left(\frac{l_1}{2} + l_3\right)R_s + (l_1 + l_2)R_{ct}]}{W} \tag{3.11}$$

where R_s is the diffusion sheet resistance in Ωm and

R_{ct} is the process contact resistance in Ωm.

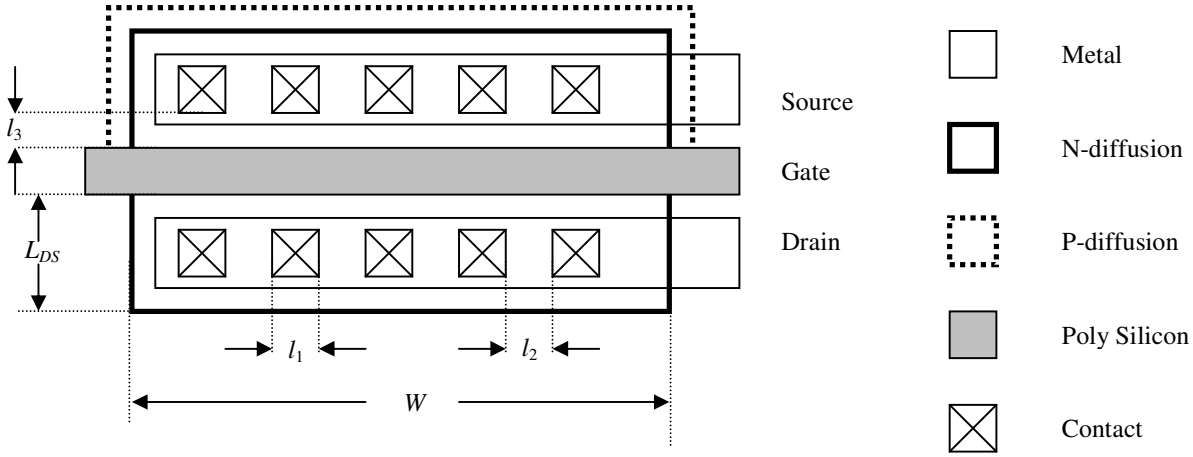


Figure 3.21 Layout of DMOS transistor

3.3.2.2 Channel Resistance

The DMOS transistor in the output stage operates in the triode (linear) region when it is 'on'. In this region, the channel resistance, r_{ch} can be estimated [Sun, *et.al.*, 1980] to be:

$$r_{ch} = \frac{V_{DS}}{I_{DS}} \tag{3.12}$$

where V_{DS} is the drain-to-source voltage and

I_{DS} is the drain-to-source current.

In the triode region, the drain current is given by:

$$I_{DS} = \beta\left[(V_{GS} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2\right] \tag{3.13}$$

$$I_{DS} \approx \beta(V_{GS} - V_{th})V_{DS} \tag{3.14}$$

where β is the gain factor of the DMOST,

V_{GS} is the gate-source voltage and

V_{th} is the threshold voltage of the DMOST.

Since V_{DS} is small, equation (3.13) can be simplified to equation (3.14). Using this approximation, the channel resistance when the transistor is turned on can be expressed as:

$$r_{ch} = \frac{V_{DS}}{I_{DS}} \approx \frac{1}{\mu C_{OX}(V_{GS} - V_{th})}\frac{L}{W} \tag{3.15}$$

where μ is the carrier mobility.

3.3.2.3 Drift Region Epitaxial Resistance

This is the resistance of the epitaxial layer (*N*-) under the poly-silicon area between the *N*+ diffusion (drain) and the body (channel region). The epitaxial layer, being lightly doped, has a high sheet resistance. However, when the gate is biased, negative charges will accumulate under the gate and this greatly reduces the resistance in this region, thus giving the DMOS transistor its low on-resistance attribute. Hence, the epi-resistance, r_{epi}, is highly dependent on the gate voltage and the process parameters.

This epi-resistance, represented by a BSIM-3 model according to the fabrication process, is analytically modeled [Eldo Device Equations Manual, 2004]:

$$r_{epi} = R_{dsw} \frac{1 + P_{rwg}(V_{GS} - V_{th})}{10^6 \times W} \tag{3.16}$$

where R_{dsw} is the resistance per unit width, and

P_{rwg} is the gate bias coefficient.

Both parameters are process dependent and they are constants obtained from the measurement of a fixed size model transistor.

In summary, the total on-resistance of the DMOS is the sum of the body resistance, channel resistance and the epitaxial resistance:

$$R_{on} = r_b + r_{ch} + r_{epi} \tag{3.17}$$

Hence, the total power dissipation due to on-resistance for a single DMOS transistor is

$$P_r = \frac{1}{T_S} \int_0^{T_S} i_o^2 R_{on} dt = \frac{1}{2} M^2 I_o^2 R_{on} \tag{3.18}$$

As expected, the power dissipation increases as a square of modulation index, M and output current, I_O. From a designer's perspective, these parameters are not within his/her control as these are part of the product specification (often specified by customers). The only parameter available to the designer is the on-resistance - a low R_{on} is desired to obtain low power dissipation due to R_{on}, P_r.

3.3.3 Power Efficiency of DMOS Output Stage and its Verification

3.3.3.1 Power Efficiency

At this juncture, we have determined all parameters pertaining to the power losses in the DMOS CDA output stage. By ignoring the short-circuit current power, P_S, (assuming the dead time has eliminated the short-circuit current completely), the power efficiency of the DMOS output stage is expressed as:

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{DISS}} = \frac{P_{OUT}}{P_{OUT} + P_C + P_r} \tag{3.19}$$

For completeness, and for application of the model for practical use, we will now describe several practical considerations. First, there are additional resistances outside of the power transistor of the output stage, including bonding wires, lead frames and PCB tracks. We lump all these additional resistances together and term them package resistance, R_{pkg}. The effect of R_{pkg} is not negligible as the package resistance, in a practical real-life case, is measured to be ~300 mΩ, compared to the total on-resistance of the output stage (single channel) which is only ~140 mΩ (for a transistor whose W = 88 mm and L = 0.27 μm). This observation also implies that there is a point of diminishing return in reducing the output resistance of the output stage.

Second, some short-circuit power loss should usually be considered in practice. This is because as delineated in the earlier part of this chapter, a dead time circuit may not necessarily eliminate all the short-circuit current, particularly when the output signal is low. During this time, the discharging at the output is slow and the top transistor retains its 'on' state while the bottom transistor turns on. Consider the DMOS output stage in Figure 3.16. To switch off *Q1*, its gate must be discharged through *Q4* and this current must flow to the output since *Q2* is not supposed to be switched 'on' yet. However, if this discharging is slow, *Q2* might turn 'on' first before *Q1* is switched 'off' and this causes a short-circuit current. We verify this by a circuit simulation of Figure 3.16,

shown in Figure 3.22. The sine wave on the top represents the low pass filtered output signal. The waveform at the bottom, on the other hand, is the short-circuit current flowing through the output power transistors *Q1* and *Q2*. It is observed that during the time when output signal is low, short-circuit current occurs. From simulations, the short-circuit power loss is estimated to be ~100 mW.

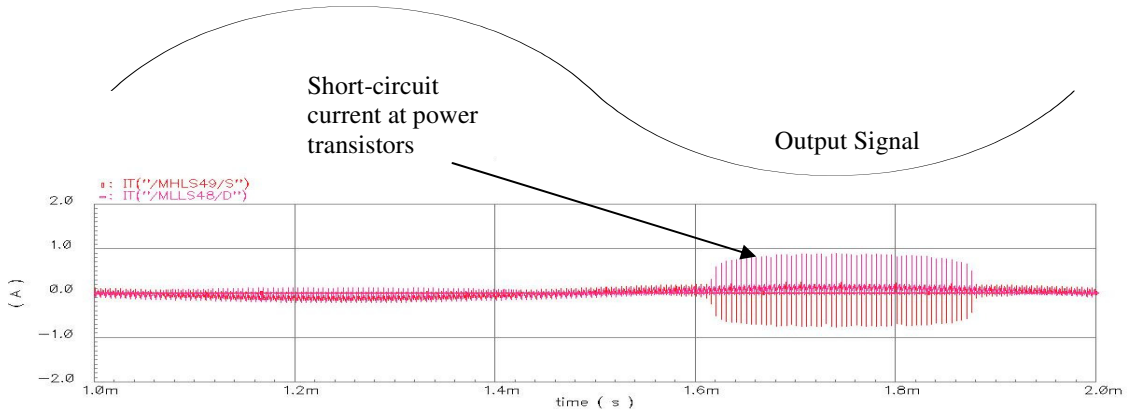


Figure 3.22 Waveforms showing short-circuit current at power transistors

In summary, the power efficiency of a practical model taking into consideration the power loss due to package resistance, P_{pkg}, and short-circuit current, P_S, is:

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{DISS}} = \frac{P_{OUT}}{P_{OUT} + P_C + P_S + (P_r + P_{pkg})} \tag{3.20}$$

where $(P_r + P_{pkg}) = \frac{1}{2} M^2 I_o^2 (R_{on} + R_{pkg})$ (3.20a)

3.3.3.2 Verification

We verify the model given in analytical equation (3.20) against computer (Spectre) simulation and on the basis of measurements on an actual IC embodying a DMOS output stage (whose output transistor having a width of W = 88 mm, and length, L = 0.27 μm) over the entire range of modulation indices from 0 to 1. In Figure 3.23, the DMOS

output stage is operated under the circuit conditions of V_{DD} = 12V, R_L = 8 Ω, f_c = 200 kHz and f_s = 1 kHz.

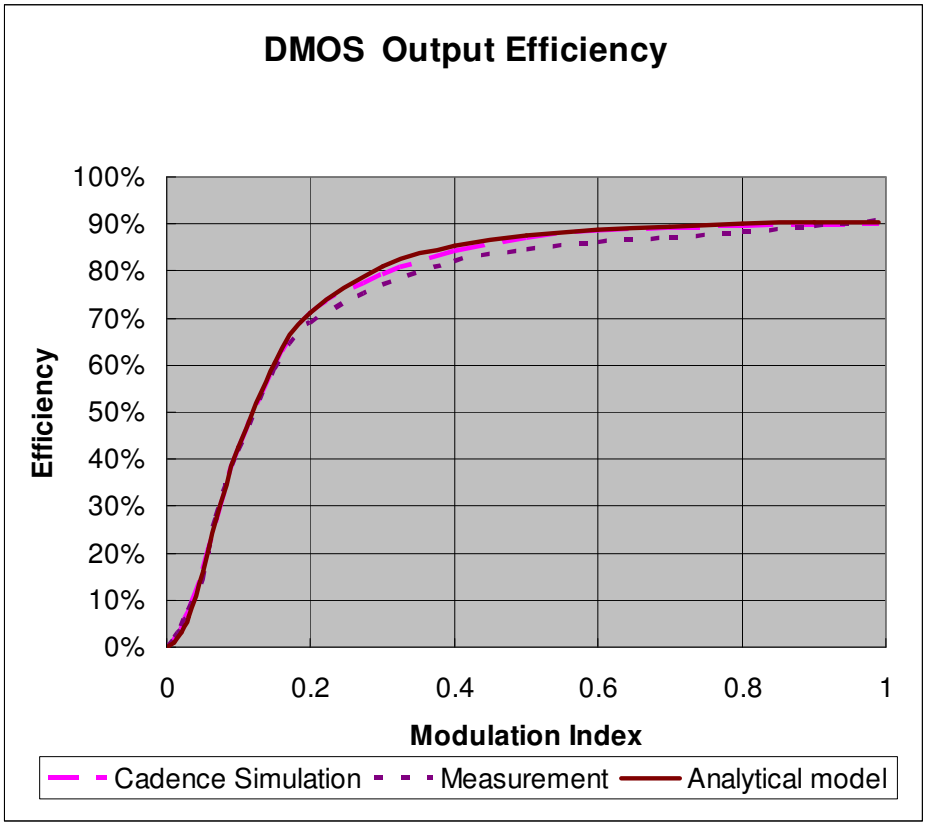


Figure 3.23 Comparison of analytical model, simulation and measurement results for efficiency

The results, presented in Figure 3.23, show that the power efficiency obtained analytically (equation (3.20)) agrees well with that obtained from simulations and from measurements. This serves to verify the validity of the analytical model. The small difference between the analytical (and simulation) and the measurements may be attributed to the simple assumption of short-circuit power loss and higher order effects of power loss in a practical application. In our analytical model, it was assumed that the input signal to the output stage is a perfect square pulse. However, a practical square pulse is exponential in nature.

3.3.3.3 Other Considerations

It is our view that the efficiency plot in Figure 3.23 is somewhat unsatisfactory in the sense that the overall efficiency is not high when compared to a typical CMOS output stage – because DMOS provides for much lower R_{on}. As delineated, this is largely because of the presence of the short-circuit current. To circumvent this, we propose a simple circuit augmentation to the design shown in Figure 3.16 to eliminate the undesirable short-circuit current. This simple augmentation is a non-overlapping logic circuit shown within the dotted box in Figure 3.24.

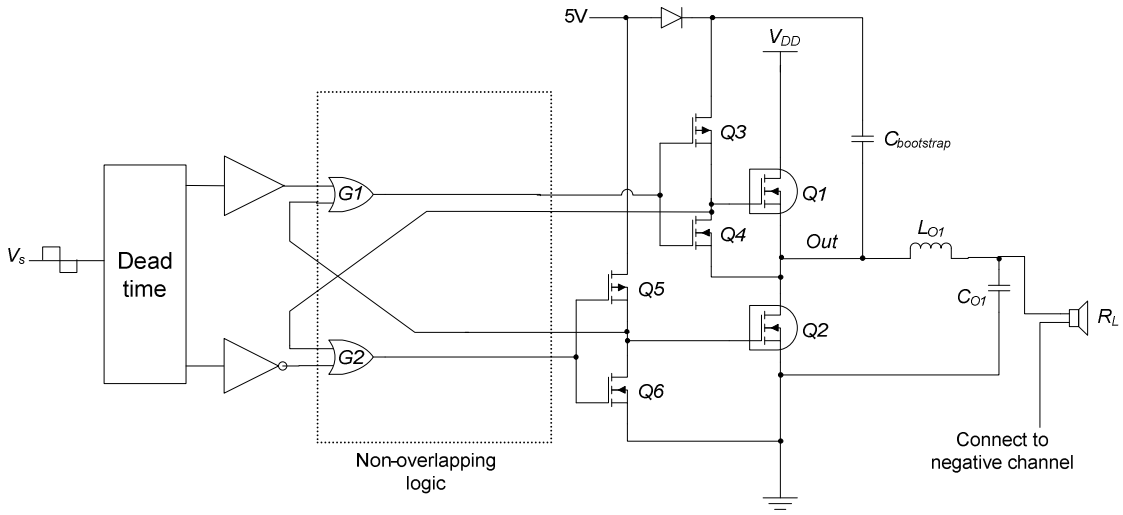


Figure 3.24 DMOS output stage with non-overlapping logic

The non-overlapping logic ensures that *Q2* does not turn 'on' when *Q1* is still active. For example, if *Q1* is still active, the gate of *Q1* will be 'high'. This will mean that the input to *G2* will also be 'high'. Therefore, regardless of the input signal, *G2* will have an output 'high' to the gates of *Q5* and *Q6* inverter pair. This feeds a 'low' to the gate of *Q2* and ensures that *Q2* will always be 'off" when *Q1* is still active. Similarly, if *Q2* is still active, the gate of *Q2* will be 'high'. This will mean that the input to *G1* will also be 'high'. Therefore, regardless of the input signal, *G1* will have an output 'high' to the gates of *Q3* and *Q4* inverter pair. This feeds a 'low' to the gate of *Q1* and ensures that *Q1* will always be 'off" when *Q2* is still active

The elimination of this short-circuit current is verified by means of computer simulations.

As P_S is now eliminated, the power efficiency is:

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{DISS}} = \frac{P_{OUT}}{P_{OUT} + P_C + (P_r + P_{pkg})} \tag{3.21}$$

Using the same circuit condition as our earlier verification (V_{DD} = 12V, R_L = 8 Ω, f_c = 200 kHz and f_s = 1 kHz), we plot the power efficiency of the output stage obtained analytically against computer simulations and the results are shown in Figure 3.25.

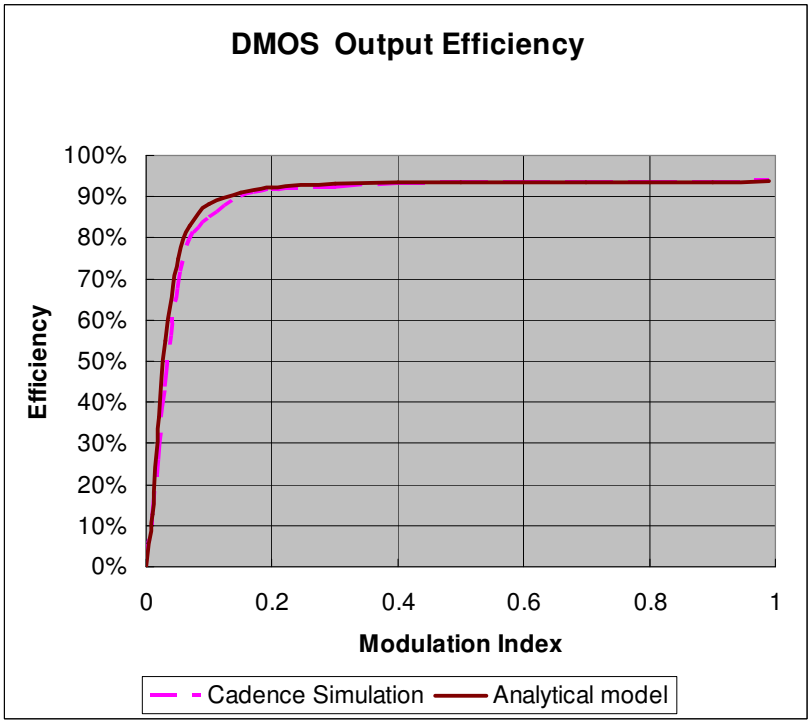


Figure 3.25 Efficiency curves with non-overlapping logic counter-measure

It can be seen that the power efficiency obtained analytically agrees well with computer simulations and this supports the validity of our analytical model. This plot also depicts

that if high efficiency is desired, particularly at low modulation indices, it is imperative to totally eliminate the short-circuit current.

In conclusion, two practical power efficiency models of the DMOS output stage has been derived. One model, which includes the short-circuit power loss, has been verified by means of computer simulations and practical IC measurement. A proposed simple non-overlapping logic design to eliminate the short-circuit power loss in the second model, has been verified against computer simulations.

3.4 Optimization of the Class D Output Stage in DMOS

Following section 3.3, there is a clear motivation to design a Class D DMOS output stage with high efficiency. Further, as the size of the output stage can easily occupy half or even more of the entire IC area, the motivation extends to an optimization of the output stage with a balance between power efficiency and chip area.

As delineated earlier, the design of the DMOS output stage of a CDA is largely empirical where the rule of thumb method is applied to obtain a small on-resistance (up to the maximum tolerable size), typically about 0.2 to 0.3 Ω for a 20V TV application (and noting that $R_{pkg} \approx 300$ mΩ). However, from an optimization perspective, decreasing R_{on} (thus decrease P_r) by increasing the width of the power transistor will conversely (and undesirably) increase the power loss due to capacitances, P_C. Put simply, there will be a point of diminishing return[+] where P_C becomes dominant over P_r and the overall efficiency decreases even if the width is increased further.

Another disadvantage of the empirical method to design the output stage to be as large as possible is cost/economical reason, where a smaller IC area is more economical than a larger one. We will now describe an optimization methodology for the DMOS output stage.

[+]Note that, from a practical perspective, this point of diminishing return should also consider the effect of R_{pkg} and R_{pkg} is substantially smaller for advanced (but more expensive) packages.

3.4.1 Optimization Methodology for DMOS Output Stage

The summary of the power dissipation mechanisms of DMOS output stage in full bridge configuration is shown in table 3.1. The terms are grouped according to the channel width, *W*.

Table 3.1 Summary of power dissipation mechanisms in DMOS

Symbol	Formula
P_C	$\frac{1}{2} f_C \{V_{DD}^2 (2C_d' + 2k_3) + V_G^2 (4C_g')\} W + \frac{1}{2} f_C V_{DD}^2 (2C_{pad} + k_4)$
C_d'	$C_{gdo} + \frac{C_{V1} \times C_{V2}}{C_{V1} + C_{V2}} \times \frac{1}{W_{unit}}$
C_g'	$C_{OX} L + C_{gso} + C_{gdo} + \frac{C_{V1} \times C_{V2}}{C_{V1} + C_{V2}} \times \frac{1}{W_{unit}}$
P_r	$\frac{1}{2} M^2 I_O^2 \frac{2R_{on}'}{W}$
R_{on}'	$r_{epi}' + r_{ch}' + r_b'$
r_{epi}'	$R_{dsw} \times \frac{1 + P_{rwg}(V_{DD} - V_{th})}{10^6}$
r_{ch}'	$\frac{L}{\mu_n C_{OX} (V_{GS} - V_{th})}$
r_b'	$2 \times \left[\left(\frac{l_1}{2} + l_3 \right) R_s + (l_1 + l_2) R_{ct} \right]$
P_{OUT}	$\frac{1}{2} M^2 I_O^2 R_L$
η	$\frac{P_{OUT}}{P_{OUT} + P_r + P_C + P_{pkg}}$

From the efficiency (η) equation, note that P_{OUT} and P_{pkg} are independent of channel width, *W*, while P_r is inversely proportional to *W*, and P_C is directly proportional to *W*. There is therefore an optimum width, W_{opt}, where power efficiency, η, is the highest. This optimum width can be obtained when the sum of (P_r + P_C) is minimum. To find

that point, we first define a function for total power dissipation, $F(W) = P_r + P_C$. By setting $\delta F(W)/\delta W = 0$, we can solve for W to find the minimum $F(W)$ which gives the maximum power efficiency.

We redefine the power dissipations P_r and P_C as functions of channel width, W.

$$P_r = A\frac{1}{W} \tag{3.22}$$

where

$$A = M^2 I_O^2 R_{on}' \tag{3.22a}$$

$$P_C = B + CW \tag{3.23}$$

where

$$B = \frac{1}{2} f_c V_{DD}^2 (2C_{pad} + k_4) \tag{3.23a}$$

and

$$C = \frac{1}{2} f_c \left\{ V_{DD}^2 (2C_d' + 2k_3) + V_G{}^2 (4C_g') \right\} \tag{3.23b}$$

Therefore, the equation for total power dissipation P_{tot} in terms of channel width, W, is:

$$\begin{aligned} P_{tot} &= F(W) \\ &= P_r(W) + P_C(W) \\ &= A\frac{1}{W} + B + CW \end{aligned} \tag{3.24}$$

For minimum power dissipation, the optimum channel width, W_{opt}, is obtained as follows:

$$\frac{\partial F(W)}{\partial W} = 0 \Rightarrow C - A\frac{1}{W^2} = 0$$

$$\therefore W_{opt} = \sqrt{\frac{A}{C}} = \sqrt{\frac{M^2 I_O^2 R_{on}'}{f_c\left\{V_{DD}^2(C_d'+k_3) + V_G{}^2(2C_g')\right\}}} \qquad (3.25)$$

In summary, we have established an optimization methodology for the DMOS output stage to obtain optimum power efficiency. We will now continue to investigate how the design of the size of the DMOS output stage is affected by the modulation index, M.

3.4.2 Area Optimization based on Modulation Index

[Chang, *et.al.*, 2000] has shown that optimization at peak power (modulation index, $M = 0.9$) for a CMOS output stage requires a very large output stage area. However, it is well established that due to the crest factor of audio signals, the signal swing is typically low, around $M = 0.2$. In view of this, we propose that for a practical DMOS output stage design, the optimization be done for $M = 0.2$.

To better delineate the abovementioned choice, we plot in figure 3.26, the efficiency curves of two typical DMOS output stages where one is optimized based on $M = 0.2$ (solid line) and the other based on $M = 0.9$ (dotted line) with all other design variables kept invariant.

We note that the power efficiency beyond the modulation index where it was optimized for (eg. $M = 0.2$ for the solid line), remains relatively flat. However, the power efficiency below the point where it was optimized for, drops rapidly. Therefore, to ensure that power efficiency is high throughout a larger modulation index range, it is more sensible to optimize at a lower M.

Optimizing at $M = 0.2$, the transistor width is $W = 31.7$ mm while optimizing at $M = 0.9$, $W = 142.8$ mm, translating to an increased area of ~4X. It can be seen that optimization for a high M requires an area that is many times larger without real advantage in the efficiency. Further, the efficiency (for an optimization at high M, $M = 0.9$) at low modulation when audio signals typically are (due to the crest factor) is lower than the case where the optimization is at lower M ($M = 0.2$). In short, we recommend an optimization (for a DMOS output stage) at low M.

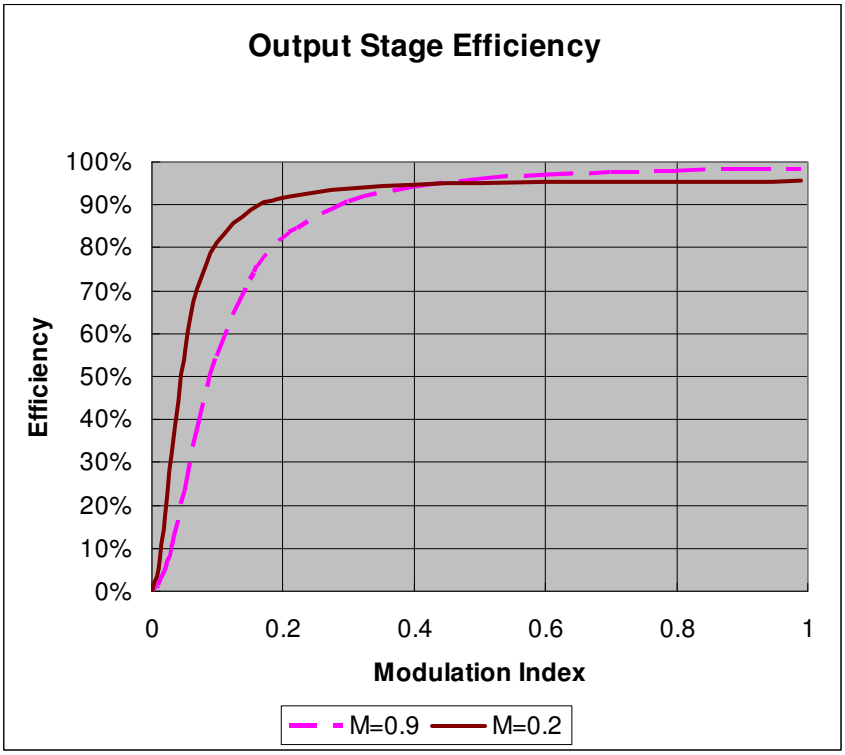


Figure 3.26 Efficiency curves optimized at different modulation indices

3.4.3 Optimization of DMOS Output Stage based on $M = 0.2$

We apply equation (3.25) to the DMOS output stage optimized for $M = 0.2$, and obtain an optimized channel width, $W_{opt} = 88$ mm, with a maximum power efficiency of 94%

(inclusive of losses in R_{pkg}). The power efficiency waveform was shown in Figure 3.25 in the previous section. We note that the power efficiency without considering R_{pkg} is 97%, which means that a large portion of power loss is caused by the package resistance, and this is a parameter that is not available to the designer.

In this design, the on-resistance is calculated and measured (on the actual IC) to be 140 mΩ. Compared to the load of 8 Ω, it is less than 2% of the load. In conclusion, DMOS technology is able to realize an output stage of very low on-resistance and hence, yield very high power efficiency. However, if the package resistance is too high, it will defeat the advantage of the low on-resistance provided by the DMOS output stage.

3.5 Conclusions

In this chapter, we have discussed the challenges of operating the CDA at a higher voltage (20V) and the need for protection circuits. The limitations of CMOS for mid-to-high voltage have justified the need for either HVMOS or DMOS. We have reviewed DMOS technology and have derived analytical expressions for the power dissipation mechanisms, power efficiency and optimization for the DMOS output stage. The derived expressions have been verified by means of Cadence computer simulations and measurement of an IC. We have also proposed a circuit improvement to a reported circuit that reduces the possibility of short-circuit current. Finally, we have shown the advantages of optimizing the output stage at low modulation indices.

Chapter 4

Optimization and Design of a Class D Output Stage in HVMOS

In chapter 3, we described the design and optimization of a Class D output stage based on DMOS in a full bridge *n*-channel totem pole configuration. In this chapter, we will describe the same for that in HVMOS but for a half bridge configuration. As delineated in chapter 2, a full bridge is simply a double single-end (half bridge) whose outputs are 180˚ out of phase (i.e. inverted with respect to the other); the work in this chapter for a half bridge can easily be extended to the full bridge. In the context of a CDA output, the output power of a full bridge is 4 times larger than the half bridge. The HVMOS process used in this chapter is that based on the Austria Microsystems (AMS) 0.35μm CMOS process with the 50V HVMOS module.

As in chapter 3, the work in this chapter includes the optimization of the output stage for maximum efficiency under a specified condition. The motivation for the work presented in this chapter is as that described in chapter 3. Specifically, as the output stage dissipates the most power in most audio amplifiers, the overall power efficiency of the amplifier largely depends on the design of the output stage, and that the size of the output stage can easily occupy half or more of the entire IC area. In short, the motivation is to optimize the output stage with a balance between power efficiency and chip area.

This chapter is organized as follows. Section 4.1 starts with a review on HVMOS technology to show its difference from DMOS. In section 4.2, the design of a CDA output stage with protection circuits is shown. Section 4.3 derives the analytical expressions for the mechanisms of power dissipation and power efficiency in HVMOS half bridge output stage. In section 4.4, the optimization method is presented and its results are verified against computer simulations. In section 4.5, the half bridge model is extended to full bridge and a comparison is made between the two. This is followed by a

comparison between HVMOS and DMOS based on full bridge configuration in section 4.6. Finally, the conclusions are drawn in section 4.7.

4.1 Review of Conventional HVMOS

Conventional High-Voltage MOS (HVMOS) is very much similar to LDMOS (in fact, DMOS is part of the family of HVMOS) in terms of its cross-sectional layout. It consists of its source diffused inside a *p*-well (depicted in Figure 4.1), which is an existing layer in a conventional HVMOS diffusion process. In contrast, the source of the DMOS transistor is diffused inside an additional body layer that is more highly doped than the *p*-well. This yields the primary advantage of DMOS over HVMOS - its lower R_{on} (hence, a higher power efficiency). However, this additional diffusion layer comes with extra cost which makes the overall diffusion cost in DMOS much more expensive.

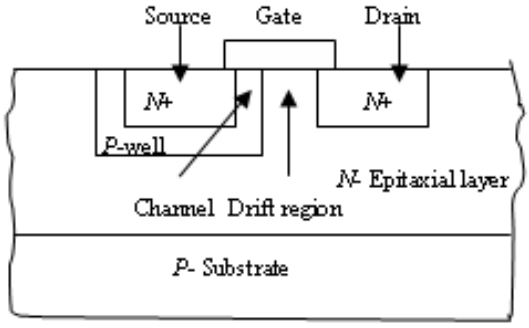


Figure 4.1 Cross-sectional layout of a typical HVMOS

Since the cross-sectional layout of the conventional HVMOS and the DMOS are very similar, from a simplistic view point, the HVMOS can be represented by the same model as the DMOS, depicted in Figures 3.18 and 3.19 earlier. The following analyses for HVMOS in this chapter will hence assume the same models used for DMOS. However, as both the HVMOS transistor and DMOS transistor come from different fabrication houses, their parameter characterizations are slightly different, and these differences will be clearly stated in the analyses.

4.2 Design of Protection Circuits for CDA Output Stage in HVMOS

In chapter 3, we reviewed the limitations of CMOS at higher voltage (20V range) applications and justified the use of DMOS output stage or HVMOS output stage. We further reviewed various considerations for the design of output stage at higher voltage, particularly the dead time design with non-overlapping logic and over-current protection. In view of these considerations for a practical realization, we also implement these circuits to obtain appropriate dead times and protection circuits to the HVMOS output stage to achieve a complete output stage design. Figure 4.2 depicts the output stage embodying these circuits including our simple non-overlapping logic to ensure that the short-circuit current is virtually eliminated.

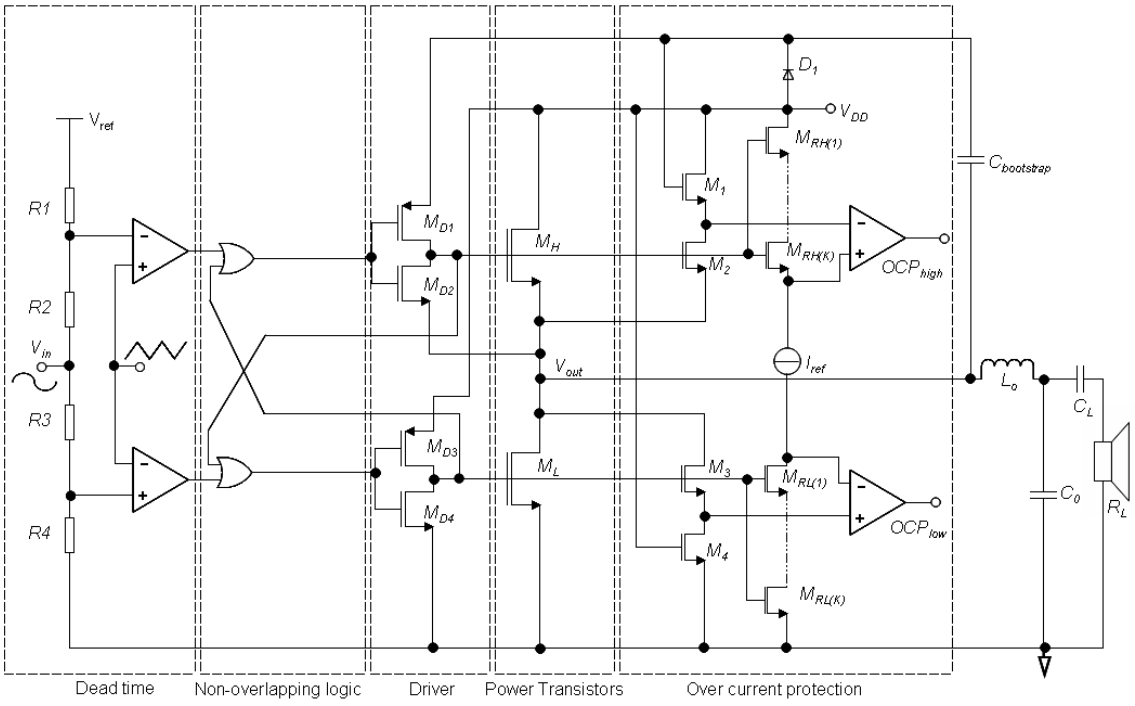


Figure 4.2 Output stage with protection circuits

The dead time design [Apex Microtechnology, 2001] is shown in the left most block. In this design, V_{ref} is connected to V_{DD} which gives V_{in} a biasing voltage equal to half V_{DD} ($V_{DD}/2$). In the same way, the triangular waveform must also be biased to $V_{DD}/2$. *R1* is designed to be the same as *R4*, and *R2* is the same as *R3*. The offset voltages to the comparators are created by V_{in} passing through *R2* and *R3*. The ratio of *R1* and *R2* (similarly *R3* and *R4*) will determine the offset voltage which will in turn create a dead time for the output stage. By setting *R1* = *R4* = 50 kΩ and *R2* = *R3* = 250 Ω, we obtain a dead time of 50 ns. The simulation result is depicted in Figure 4.3, where the gate voltages of the top and bottom power transistors are shown with respect to time.

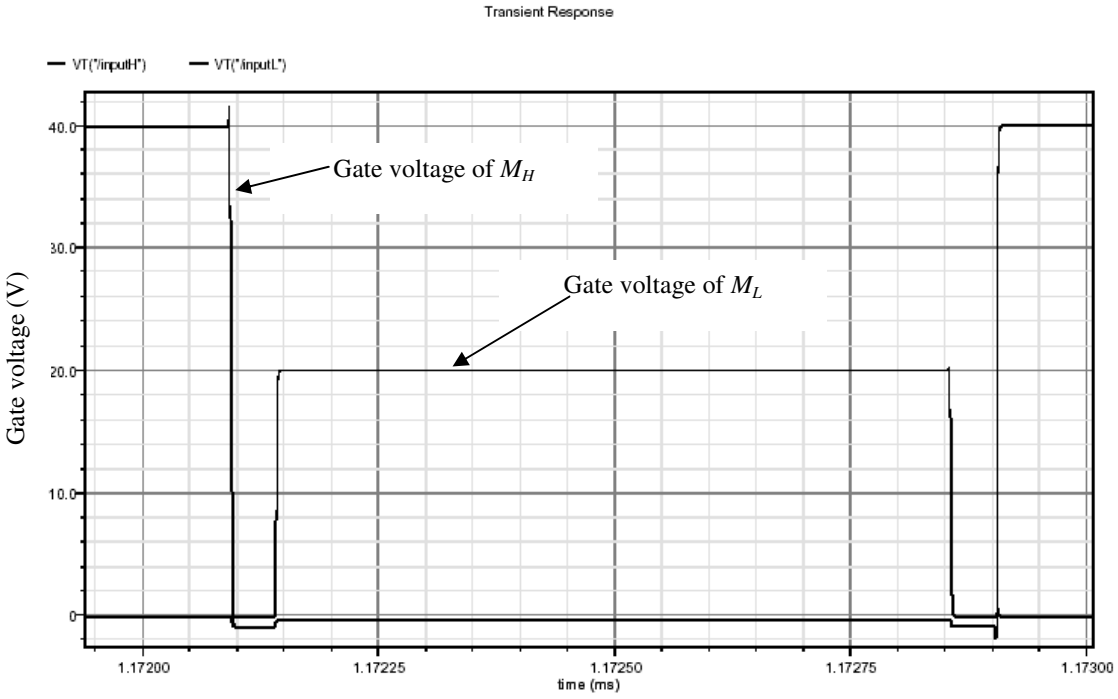


Figure 4.3 Dead time simulation result

Following the dead time block is the proposed simple non-overlapping logic block. This logic ensures that the bottom power transistor must be turned off before the top power transistor turns on, and vice versa. The next 2 blocks to the right are the driver stage (M_{D1}, M_{D2}, M_{D3} and M_{D4}) and the output power transistors (M_H and M_L). A tapering ratio of 12 (with respect to the output power transistor) is used.

The following block (dotted box in the extreme right) is the over-current protection block. According to the current limitation of a typical bonding wire, we design the current limit to be below 3.5 A as the probability of damage starts to increase beyond that current limit. Using the formula provided by [Berkhout, 2005], $I_{LIM} = N * K * I_{ref}$ (see section 3.1.3 in chapter 3), we set $N = 20\,000$, $K = 6$ and $I_{ref} = 25$ µA to obtain an estimated current limit of 3 A. In this design, N is made large to keep the overall IC size small as there are 2 large (power transistors) and 16 smaller replica transistors in the design of over-current protection. The layout of these transistors must be part of or near the power transistors for good matching purpose. The simulation result is depicted in Figure 4.4 where the over-current protection kicks in when I_{out} reaches ~3.27 A (where the comparator switches state).

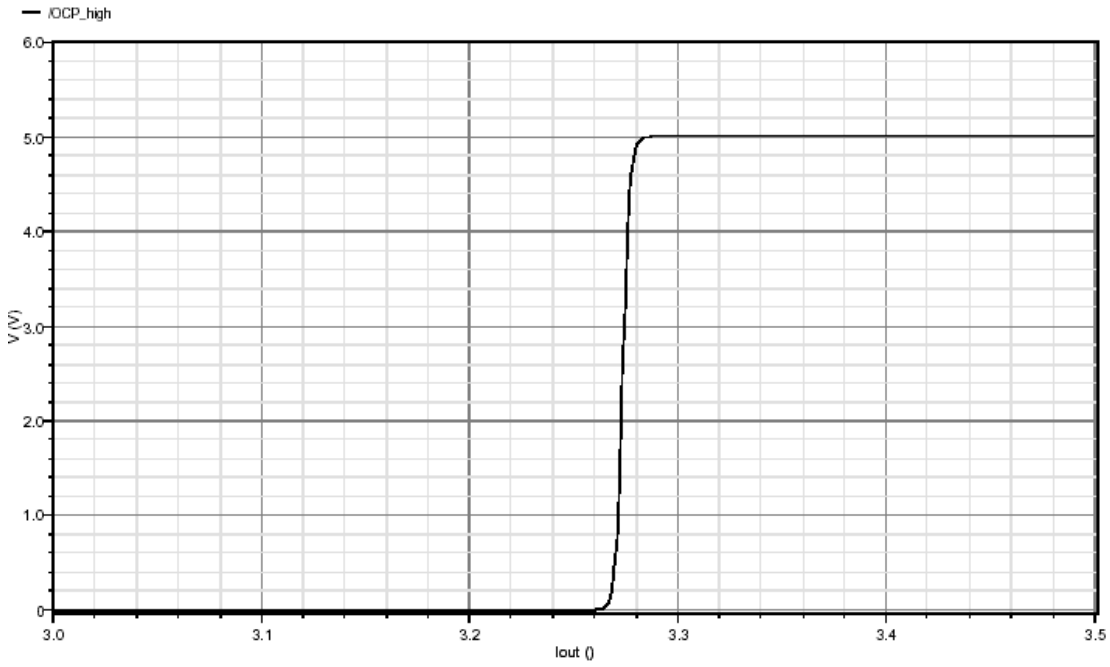


Figure 4.4 Over-current protection simulation

Finally, D_1 and $C_{bootstrap}$ form the bootstrap, L_O and C_O form the output filter, C_L is the decoupling capacitor and R_L is the output load. A summary of all the design values are tabulated in table 4.1.

Table 4.1 Summary of design values in HVMOS

SYMBOLS		SYMBOLS	
V_{DD}	20 V	$R1 = R4$	50 kΩ
V_{ref}	20 V	$R2 = R3$	250 Ω
I_{ref}	25 μA	R_L	8 Ω
N	20 000	C_L	100 μF
K	6	C_O	0.22 μF
$W_{MH} = W_{ML}$	W_{opt}	L_O	100 μH
$W_{MD1} = W_{MD3}$	W_{opt} /4	$C_{bootstrap}$	1 μF
$W_{MD2} = W_{MD4}$	W_{opt} /12		
$W_{M1} = W_{M2} = W_{M3} = W_{M4} = W_{MRH1}...W_{MRH6} = W_{MRL1}...W_{MRL6}$			W_{opt} /N

In conclusion, we have designed the full CDA output stage with protection circuits for HVMOS. The design has been verified against Cadence (Spectre) computer simulations.

4.3 Power Dissipation Mechanisms of HVMOS Output Stage

In chapter 3, we designed a CDA DMOS output stage based on the full bridge *n*-channel totem pole configuration. In this section, we will design the same but for a variation, the half bridge *n*-channel totem pole configuration as described in section 4.1. The pertinent section of the complete CDA output depicted in Figure 4.2 earlier is extracted to Figure 4.5.

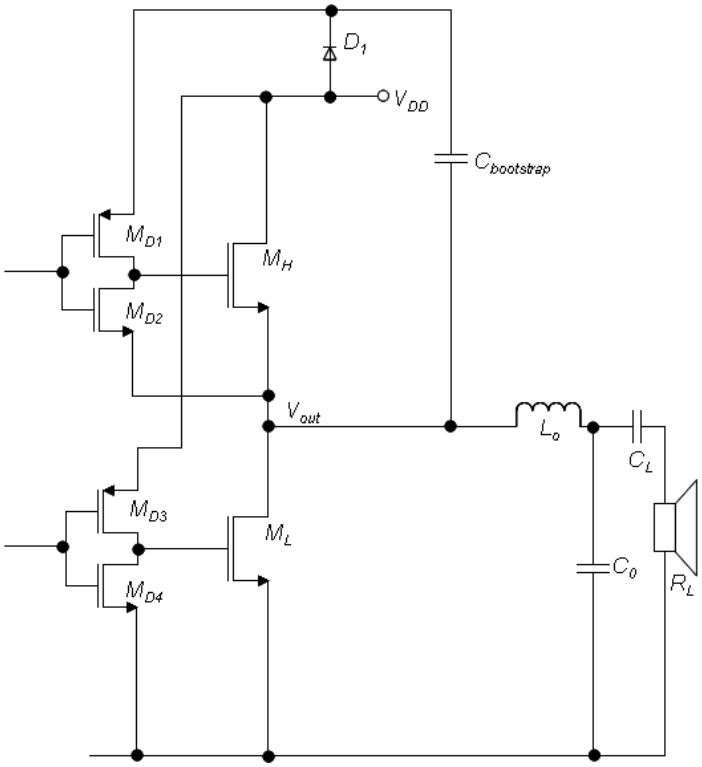


Figure 4.5 Output Stage based on half bridge *n*-channel totem pole configuration

In this analysis (similar to the DMOS example in chapter 3), it is assumed that the short-circuit current is totally eliminated and the term P_S is taken out of the power loss calculation. The power dissipation mechanisms of HVMOS are very similar to that of DMOS, with slight differences which will be discussed later.

4.3.1 Parasitic Capacitance of HVMOS

As delineated in chapter 3, the maximum gate-to-source voltage that can be applied to the DMOS is only 5V. This is due to the thin gate oxide of the DMOS process. From the basic capacitor equation, $C = \frac{\varepsilon(Area)}{t_{ox}}$, where ε is the permittivity, *Area* is the area of gate over the drain and t_{ox} is the oxide thickness, a smaller t_{ox} will yield a larger capacitance.

In the DMOS process used for this research programme in chapter 3, this capacitance is significant and it is characterized by an additional gate to drain capacitance C_{gd}. In contrast, the maximum gate voltage that can be applied to the gate of HVMOS (based on the HVMOS process used) is 20V. This higher voltage tolerance requires a larger oxide thickness (to prevent breakdown) which also means that the associated parasitic capacitance would be smaller, compared to DMOS. In fact, for the model defined by the AMS process, C_{gd} is not included in the characterization of parasitic capacitance as it is negligible.

Another point worth noting is that the minimum channel length of the HVMOS is typically longer than that of the DMOS. For example, for the available processes available to us, the minimum channel length of the HVMOS and DMOS is 1μm and 0.27μm respectively. On the whole, because of the smaller channel length, hence smaller area of the DMOS gate, the overall capacitance of the DMOS is smaller than that of HVMOS, despite the larger capacitance per unit area. In short, the DMOS would have a higher power efficiency over HVMOS not only because of the smaller capacitance but also the reduced on-resistance (See section 4.3.2 later).

For the HVMOS process used in this programme, the characterization method of the capacitance is the same as that of a CMOS model as delineated in chapter 2. The overall parasitic capacitance, C_P, of the *n*-channel HVMOS output stage is:

$$C_P = (C_{go} + C_{do})W \tag{4.1}$$

where C_{go} is the gate associated capacitance per unit width:

$$C_{go} = 2 \times (C_{OX}L + C_{gso} + C_{gdo}) \tag{4.1a}$$

and C_{do} is the output associated capacitance per unit width:

$$C_{do} = 2\times(C_j L_{DS} + 2C_{jsw}) + C_{gso} + C_{gdo} \tag{4.1b}$$

4.3.2 Parasitic Resistance of HVMOS

The model used to describe the resistance in HVMOS is largely similar to that of DMOS with the addition of a drain resistance r_d, which is a value defined by the process. Similar to the DMOS model, the overall R_{on} of the HVMOS transistor changes with width W. As mentioned earlier, HVMOS has a longer channel length in a p-well diffusion. This results in the HVMOS having a larger channel resistance compared to DMOS. A simple model of the HVMOS transistor is shown in Figure 4.6.

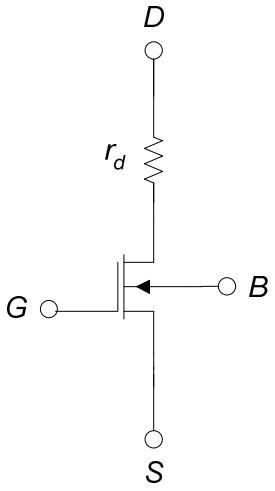


Figure 4.6 A simple HVMOS model

Therefore, the overall on-resistance of a HVMOS is:

$$R_{on} = r_b + r_{ch} + r_{epi} + r_d \tag{4.2}$$

4.3.3 Power Dissipation and Efficiency of HVMOS

It is well established that the power delivery of a half bridge output stage is 4 times smaller than that of a full bridge output stage. Therefore, a factor of ¼ must be multiplied for the calculation of output power, P_{OUT}, and resistance power loss, P_r. Apart from this, the power dissipation mechanisms of the HVMOS are similar to that of DMOS. The summary of power dissipation mechanisms and efficiency in HVMOS is shown in table 4.2. This is based on the assumption that there is no short-circuit current loss.

Table 4.2 Summary of power dissipation mechanisms in HVMOS

Symbol	Formula
P_C	$\frac{1}{2}V_{DD}^2 f_C (C_P W + 2C_{pad})$
C_P	$C_{go} + C_{do}$
C_{go}	$2\times\{C_{OX} L + (C_{gso} + C_{gdo})\}$
C_{do}	$2\times(C_j L_{DS} + 2C_{jsw}) + C_{gso} + C_{gdo}$
P_r	$\frac{1}{8} M^2 I_O^2 R_{on}$
R_{on}	$\frac{R_b + R_{ch} + R_{epi} + R_d}{W}$
R_{epi}	$R_{dsw} \times \frac{1 + P_{rwg}(V_{DD} - V_{thn})}{10^6}$
R_{ch}	$\frac{L}{\mu_n C_{OX}(V_{DD} - V_{thn})}$
R_b	$2\times\left[\left(\frac{l_1}{2} + l_3\right)R_S + (l_1 + l_2)R_{ctn}\right]$
P_{OUT}	$\frac{1}{8} M^2 I_O^2 R_L$
η	$\frac{P_{OUT}}{P_{OUT} + P_r + P_C}$

In summary, the differences between the models of HVMOS and DMOS have been described and the power dissipation mechanisms of the HVMOS have been derived.

4.4 Optimization of HVMOS Output Stage and its Verification

4.4.1 Optimization

As in chapter 3, noting that P_r is inversely proportional to channel width, W, while P_C is directly proportional to W, there is an optimum width, W_{opt}, where power efficiency, η, is the highest. It happens when the sum of $(P_r + P_C)$ is minimum. To find that point, we again define a function for total power dissipation, $F(W) = P_r + P_C$, and by setting $\delta F(W)/ \delta W = 0$, we are able to solve for a W to find the minimum $F(W)$ which gives the maximum power efficiency.

Let us redefine the power dissipations P_r and P_C as functions of channel width W.

$$P_r = A'\frac{1}{W} \tag{4.3}$$

where

$$A' = \frac{1}{8} M^2 I_O^2 \left(R_b + R_{ch} + R_{epi} + R_d\right) \tag{4.4}$$

$$P_C = B' + C'W \tag{4.5}$$

where

$$B' = f_c V_{DD}^2 C_{pad} \tag{4.6}$$

and

$$C' = \frac{1}{2} f_c V_{DD}^2 (C_P) \tag{4.7}$$

Therefore, the equation for total power dissipation P_{tot} in terms of channel width W is:

$$\begin{aligned} P_{tot} &= F(W) \\ &= P_r(W) + P_C(W) \\ &= A'\frac{1}{W} + B' + C'W \end{aligned} \tag{4.8}$$

For minimum power dissipation, the optimum channel width W_{opt} is obtained as follows:

$$\frac{\partial F(W)}{\partial W} = 0 \Rightarrow C' - A'\frac{1}{W^2} = 0$$

$$\therefore W_{opt} = \sqrt{\frac{A'}{C'}} = \sqrt{\frac{M^2 I_O^2 \left(R_b + R_{ch} + R_{epi} + R_d\right)}{4 f_c V_{DD}^2 (C_P)}} \tag{4.9}$$

At this juncture, we have established an optimization methodology for the HVMOS output stage to obtain optimum power efficiency. We will now verify the analytical model against computer simulations.

4.4.2 Verification

In this research programme, the aim in this chapter is to design a CDA output stage for home TV application with the design specifications tabulated in table 4.3. This design is based on a 0.35µm CMOS process with 50V HVMOS module. The process parameters are shown in table 4.4.

Table 4.3 Design Specifications

SYMBOLS		SYMBOLS	
Supply Voltage, V_{DD}	20 V	Rise & fall time of PWM signal, τ	5 ns
Input signal frequency, f_s	1 kHz	Load, R_L	8 Ω
Switching frequency, f_c	200 kHz	Filter Inductance, L_O	100 μH
Modulation Index, M	0.2	Filter Capacitance, C_O	0.22 μF

Table 4.4 Process Parameters

PARAMETERS		PARAMETERS	
V_{thn}	2.509 V	R_n	75 Ω/□
μ_n	497 cm^2/V.S	R_{ctn}	30 Ω/cont.
t_{ox}	4.92 x10^{-8} m	R_d	8.339 x10^{-3} Ω m
ε_{ox}	3.45x10^{-11} F/m	R_{dsw}	1390 Ω m
C_{ox}	7.02x10^{-4} F/m	P_{rwg}	0
C_j	0.83x10^{-3} F/m	L	1.0 μm
$C_{gso} = C_{gdo}$	0.2x10^{-9} F/m	L_{DS}	3.2 μm
C_{gbo}	0.14x10^{-9} F/m	l_1=l_2	0.4 μm
C_{jsw}	0.25x10^{-9} F/m	l_3	0.3 μm
C_{pad}	2 pF/pad		

By means of MATLAB to numerically compute equation (4.9) (based on optimization of $M = 0.2$ as in chapter 3) and using the above specifications and process parameters, the optimum width of the HVMOS output stage is $W_{opt} = 31.7$mm (31,700µm). With this optimized width, we plot the efficiency of the HVMOS output stage over the whole range of modulation index, M (0 to 1). This analytical result is verified against Cadence (Spectre) computer simulation (depicted in Figure 4.7). Our analytical model agrees well with the simulation results and this proves the validity of our analytical model. Similar to the case of DMOS in chapter 3, the minor difference at low modulation indices are attributed to higher order effects of power loss. At low modulation indices, this power loss becomes more significant compared to output power, and hence, power efficiency is affected.

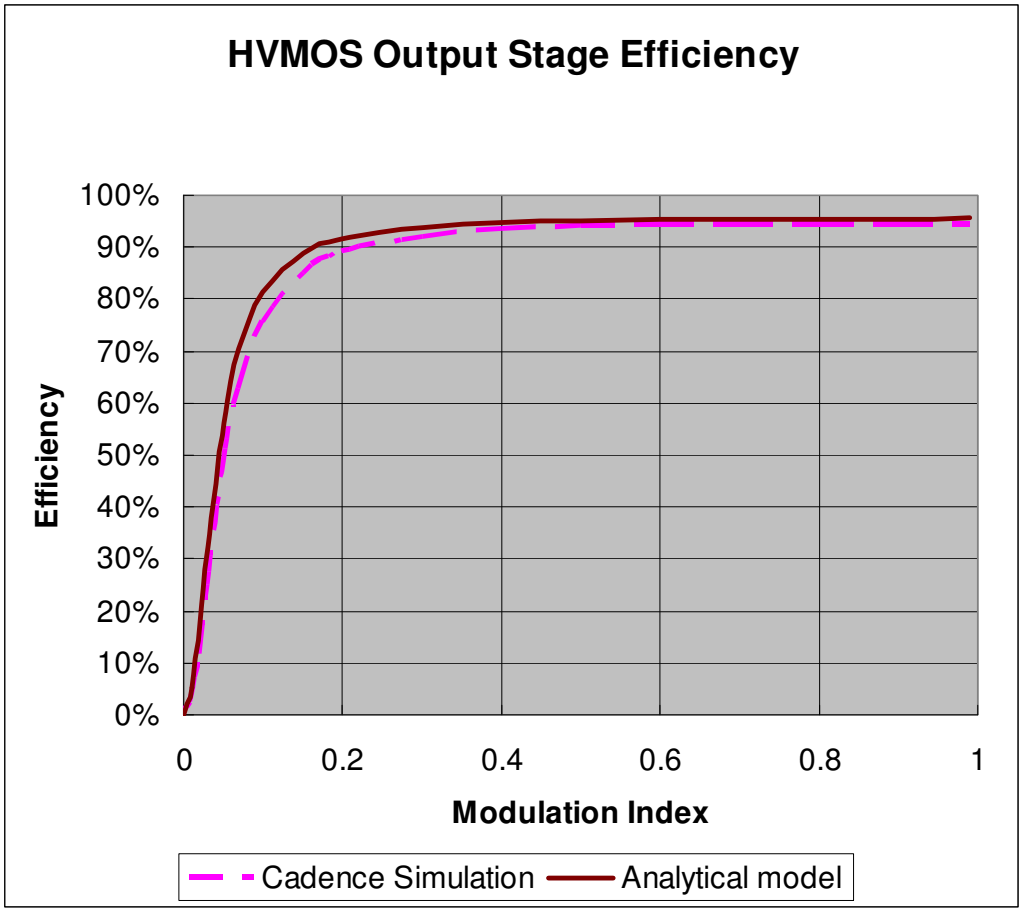


Figure 4.7 Power efficiency of analytical model and computer simulation

4.5 Comparison between Half Bridge and Full Bridge

In the previous section, we have optimized a half bridge CDA output stage based on HVMOS and verified the results against computer simulation. In practical applications, a half bridge and a full bridge amplifier can be used interchangeably (for example, several CDA ICs comprise half bridge ICs that can serve as a stereo amplifier with two independent single-ended outputs or a mono single full bridge output), due to cost availability and convenience. Therefore, in this section, we will extend our analysis to the full bridge configuration and investigate the power efficiencies of an output stage (optimized in half bridge) operating in full bridge configuration and an output stage (optimized in full bridge) operating in half bridge configuration.

To extend this work to the full bridge, we note that its output power delivery (assuming the same design (W and L) for half bridge and full bridge) is 4 times larger than the half bridge. Note that it is assumed that the load resistance, $R_L >> R_{on}$, the on-resistance. As delineated in chapter 2 (a full bridge is equivalent to 2 half bridges), the area of a full bridge is 2 times that of the half bridge and this results in a 2x increase of the power dissipation due to C_P.

Another parameter that affects power efficiency is the R_{on} of the output stage. From Figure 2.20 in chapter 2, it can also be seen that the load current of the full bridge output stage goes through 2 x R_{on}, as opposed to the half bridge where the load current only flows through 1 x R_{on}. We note that as R_{on} is in series with the load, if the power delivered to the load (for a full bridge) is 4 times higher, the power dissipated through R_{on} will increase by the same factor. Since the load current goes through 2 x R_{on} (for the full bridge), the on-resistance power dissipation will be 8 times larger compared to the half bridge.

In view of that, the following changes apply to the half bridge analytical expressions with respect to the full bridge:

$$(P_O)_{\text{full bridge}} \approx 4(P_O)_{\text{half bridge}}$$
$$(P_r)_{\text{full bridge}} \approx 8(P_r)_{\text{half bridge}}$$
$$(P_C)_{\text{full bridge}} = 2(P_C)_{\text{half bridge}}$$
$$(R_{on})_{\text{full bridge}} = 2(R_{on})_{\text{half bridge}}$$
$$(C_P)_{\text{full bridge}} = 2(C_P)_{\text{half bridge}}$$

We apply the above changes to our analytical model to obtain the efficiency curve for a full bridge CDA output stage based on HVMOS. In this application, we simulate a CDA output stage (designed and optimized for half bridge) operating in full bridge configuration. In Figure 4.8, we plot the power efficiency curves of the same output stage operating in half bridge and in full bridge.

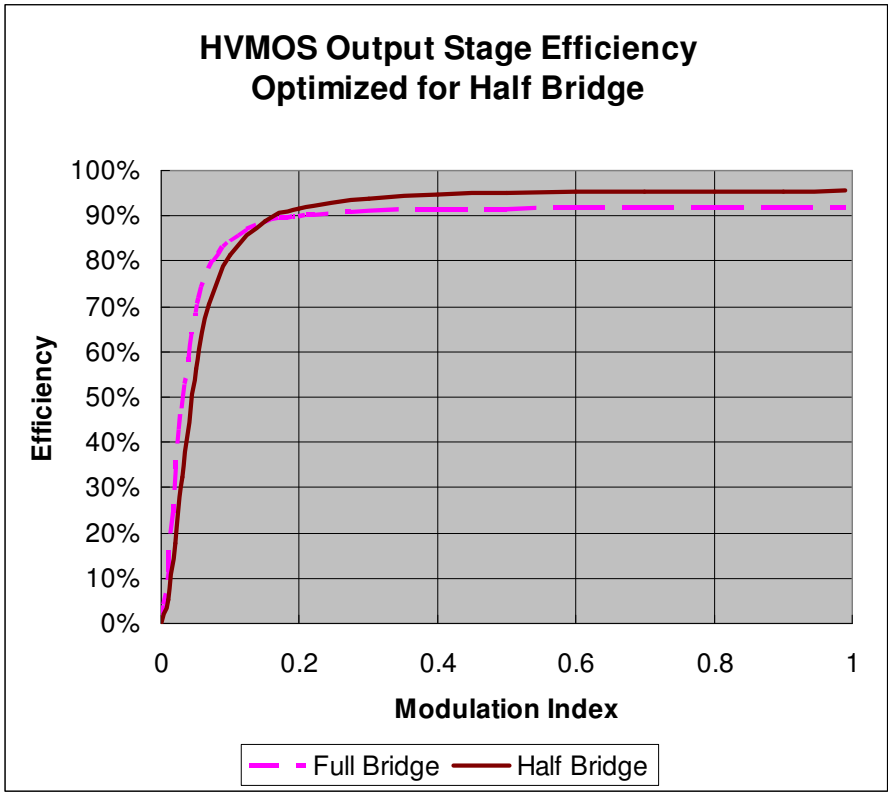


Figure 4.8 Power efficiency curves of HVMOS optimized for half bridge

In this simulation, we show that a CDA output stage optimized for half bridge at $M = 0.2$ (Output power = 0.25W) yields a power efficiency of 92%. However, if this same CDA output stage were to be used in a full bridge configuration at the same output power ($M = 0.1$), the power efficiency drops to 85%. This drop of power efficiency at $M = 0.2$ is significant and the drop becomes more rapid as the modulating signal gets smaller (M gets smaller). Based on this significant drop in power efficiency, it is not advisable to use a CDA output stage optimized for half bridge (at $M = 0.2$) in a full bridge configuration if the same power output is considered (and taking into account the crest factor of audio signals).

Consider now, a CDA output stage optimized for full bridge, as earlier delineated, and its application on a half bridge application. Based on the same circuit condition as the half bridge (V_{DD} = 20V, R_L = 8 Ω, and f_c = 200 kHz) we optimize the CDA output stage for full bridge at $M = 0.2$ and obtained an optimized width of W_{opt} = 63.5 mm. In Figure 4.9, we plot the power efficiency curves of the (same) output stage operating in half bridge and in full bridge.

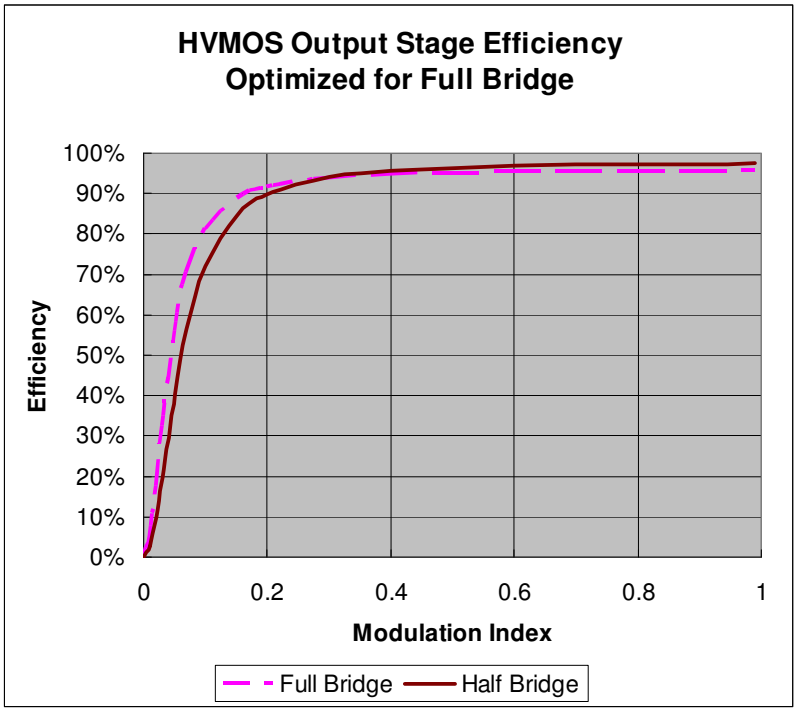


Figure 4.9 Power efficiency curves of HVMOS optimized for full bridge

In Figure 4.9, we show that a CDA output stage optimized for full bridge at $M = 0.2$ (Output power = 1W) yields a power efficiency of 92%. However, if this same CDA output stage were to be used in a half bridge configuration at the same output power ($M = 0.4$), the power efficiency will be 96%, which is higher than the full bridge configuration.

There are two considerations here. First, as the crest factor of audio signals is high, the expected average modulation index is $M = 0.2$. This means that if the CDA is operated at $M = 0.4$, the likelihood of signal dipping is high, usually an unacceptable situation in high fidelity application. Second, further to the first, this half bridge output stage can only provide a maximum power (at $M = 1$) that is 4x lower than when it is configured for full bridge. In this example, the output stage in full bridge application is able to deliver a power of 25W at $M = 1$. However, when it is configured for half bridge, the power at $M = 1$ is only 6.25W.

Based on the consideration of power efficiency, a CDA output stage optimized for full bridge at $M = 0.2$ is able to operate in half bridge with higher power efficiency (than full bridge operation).

4.6 Comparison between HVMOS and DMOS

In this section, we will compare the full bridge HVMOS output stage against the full bridge DMOS output stage. In this comparison, we optimize the HVMOS output stage for modulation index, $M = 0.2$ with the same circuit condition as the full bridge DMOS output stage ($V_{DD} = 12$V, $R_L = 8\ \Omega$, and $f_c = 200$ kHz) and obtained an optimized width of $W_{opt} = 67.2$ mm. The power efficiency curve of this full bridge HVMOS output stage (inclusive of package resistance, $R_{pkg} = 300\ m\Omega$) is plotted (in Figure 4.10) against the full bridge DMOS output stage as in chapter 3 (also for package resistance, $R_{pkg} = 300\ m\Omega$).

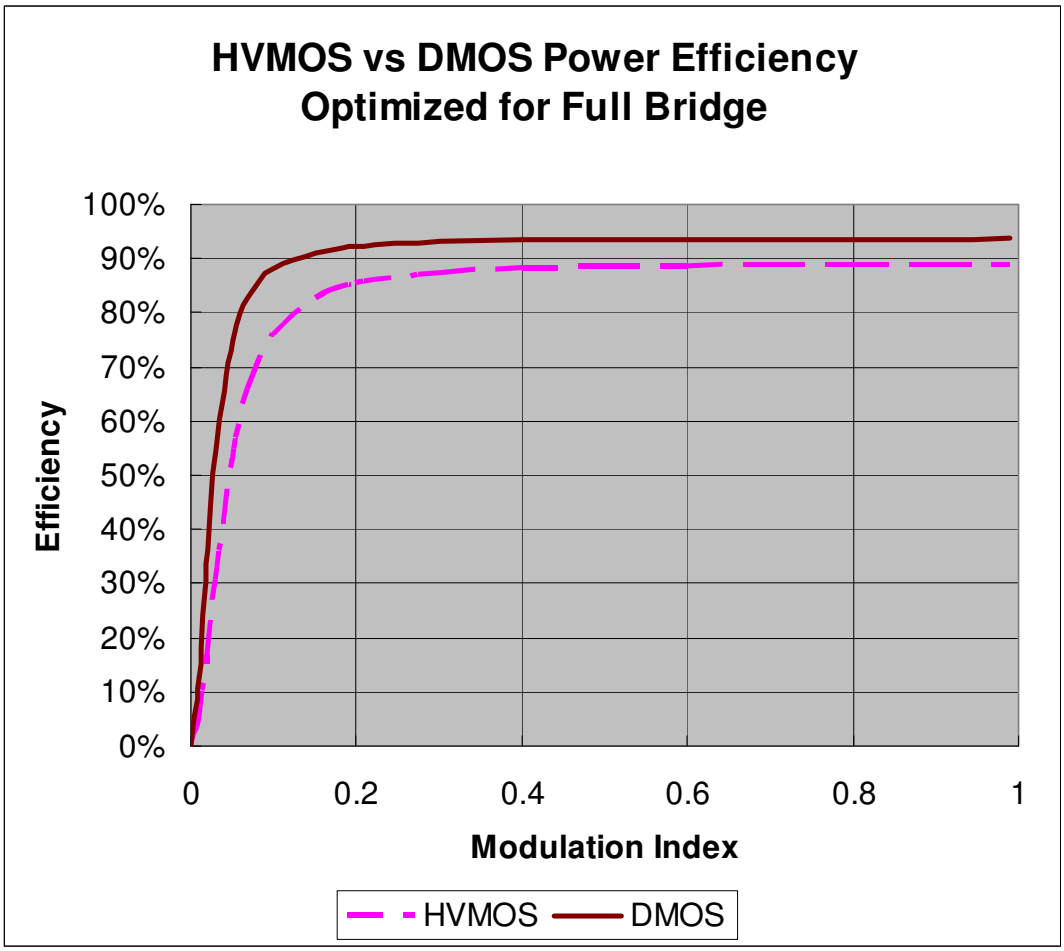


Figure 4.10 Power efficiency curves of HVMOS and DMOS

In Figure 4.10, the optimum power efficiency of the HVMOS at $M = 0.2$ is 85%, while that of the DMOS at the same modulation index is 92%. Besides, we observe that the power efficiency of DMOS is higher than that of HVMOS throughout the whole range of modulation index from 0 to 1. This concludes that DMOS provides a higher power efficiency than HVMOS for the same circuit condition and power output. However, this is usually achieved with extra cost as the diffusion process of DMOS is more expensive than HVMOS.

4.7 Conclusions

In this chapter, we have reviewed the HVMOS and designed a full CDA output stage based on HVMOS with protection circuits. We have also derived the analytical expressions for the power dissipation mechanisms and efficiency, and proposed an optimization method for the *n*-channel totem pole half bridge output stage, based on HVMOS, to obtain an optimum power efficiency for a given modulation index. The analytical model has been verified against Cadence (Spectre) computer simulation. We have compared the power efficiencies of an optimized half bridge output stage design used for as a full bridge output stage design, and vice versa; the optimized point was $M = 0.2$. We found that an optimized half bridge is generally unsuitable for a full bridge application while the converse is generally suitable (save the limited signal swing). Finally, a comparison between the power efficiencies of the full bridge HVMOS output stage and DMOS output stage has shown that DMOS yields higher power efficiency.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

The overall research objective of this M.Eng research programme is to establish a systematic analytical method to design and optimize the CDA output stage for mid-voltage (20V) applications using DMOS and HVMOS technology. The primary motivation of this research is the realization of a power-efficient amplifier at a reasonable cost (small and realistic IC area). The advantages include an increased lifespan of remote power supplies (batteries) and smaller form factor, for portability and aesthetic reasons, arising from the elimination of the heat sink in many cases or at least a significantly reduced heat sink size.

A literature review has been presented in chapter 2 and it clearly delineates the motivation of the work herein. Among the amplifiers reviewed, the CDA not only offers the highest power efficiency, it does not compromise on its signal and noise performance (THD and PSRR) if properly designed. A review on the modulators also concluded that PWM has an advantage over PDM in terms of power efficiency as it can operate at a lower switching frequency (lower switching loss) and due to its circuit simplicity (lower quiescent power loss). Different output stage configurations have also been reviewed and the *n*-channel totem pole output stage has advantages of higher power efficiency and smaller IC area requirement than the *p*-channel-cum-*n*-channel inverter output stage (typical of CMOS low voltage designs). The low voltage CMOS output stage has also been reviewed.

A review of the design of a DMOS- or HVMOS-based output stage has shown that their designs are largely empirical, where a rule-of-thumb is often applied. Sometimes, the rule-of-thumb method can result in an IC area that is larger than analytically required, and it rendered the design cost ineffective. This established the motivation of the overall

objective of this research - to establish a systematic analytical method to design and to optimize the Class D output stages. This involved the secondary objectives (i) – (vii), delineated in chapter 1.

Chapters 3 and 4 have reported the investigative research work to accomplish the secondary objectives. Analyses pertaining to DMOS technology were presented in chapter 3 while those pertaining to HVMOS were presented in chapter 4.

For objective (i), to design a complete CDA output stage with protection circuits, a literature review on protection circuits has been presented in chapter 2 and the problems of operating an output stage at high voltage has been investigated in chapter 3. The reported solutions have been applied and presented in chapter 4 and in the course of our investigation, we have designed a non-overlapping logic circuit to reduce the possibility of short-circuit current in a CDA output stage.

For objective (ii), to investigate different output stage configurations and their effects on power efficiency, a literature review has been presented in chapter 2 and it was concluded that the *n*-channel totem pole is better than the *p*-channel-cum-*n*-channel inverter on the basis of higher power efficiency and smaller IC area requirement (for our application). In chapter 4, we have further compared the power efficiencies between the half bridge and full bridge configurations and have concluded that an optimized half bridge is generally unsuitable for a full bridge application while the converse is generally suitable (save the limited signal swing)

For objectives (iii) and (iv), to investigate the power loss mechanisms and power efficiencies of DMOS output stage and HVMOS output stage, two different sets of analytical expressions have been derived to model the power dissipations and power efficiencies of the DMOS output stage (chapter 3) and the HVMOS output stage (chapter 4). It was observed that two physical parameters (the total lumped parasitic capacitance, C_P, and the total lumped on-resistance, R_{on}, associated to the output stage) and one design parameter (the switching carrier frequency, f_c) are available to the

designer. A lower f_c will result in lower switching loss, and eventually lead to higher power efficiency. However, there must be a balance between C_P and R_{on} as both parameters are inter-related (lower R_{on} will result in higher C_P) in terms of power loss and hence, affect the overall power efficiency.

The balance between C_P and R_{on} has been derived in objectives (v) and (vi), which are to optimize the DMOS output stage and the HVMOS output stage for optimum power efficiency in view of IC area. An analytical expression to optimize the width of the output stage power transistor has been derived (in chapter 3 for DMOS and in chapter 4 for HVMOS) to obtain optimum power efficiency for a given modulation index. In this analysis, the IC area has also been considered. It has been concluded that optimizing the output stage at lower modulation index not only requires a smaller IC area, it can also improve the power efficiency at low modulation indices (small input signal), and this is of particular pertinence in view of the crest factor of audio signals. As in objective (ii), it was also observed that in order to achieve both higher power efficiency and smaller output stage area, the *n*-channel totem pole output stage is preferred over the *p*-channel-cum-*n*-channel inverter output stage. In chapter 4, we have also compared the power efficiencies of the full bridge DMOS output stage and the full bridge HVMOS output stage and concluded that DMOS can yield higher power efficiency.

Finally, for objective (vii), the analytical expressions in objectives (i) - (vi) have been verified against Cadence (Spectre) computer simulations for both the DMOS output stage and HVMOS output stage, and on the basis of measurements on a fabricated CDA IC embodying a DMOS output stage.

In conclusion, the above analyses herein give designers better insight and appreciation of the potential problems that may surface when designing the CDA for higher voltage (mid-voltage) operations, in particular higher power efficiency in view of IC area.

5.2 Future Work

In view of the investigative work in this dissertation, we recommend the following as future work:

(i) We propose an investigation into the parameters that affect both power efficiency and non-linearity so as to design a CDA optimized with a balance between power efficiency and non-linearity. From our review, we observed that non-linearity (THD and PSRR) will improve when the switching frequency increases. This increase in switching frequency will cause the power efficiency to deteriorate. As both power efficiency and non-linearity are key specifications in the design of a CDA, it is worthwhile to look to a balance between the two.

It will be particularly interesting if a method of improving non-linearity can be proposed that is not frequency dependent.

(ii) We propose an investigation to improve power efficiency of the CDA output stage at low modulation index. In our research, we observed that despite the high power efficiency at high modulation index, the power efficiency drops drastically when the modulation index is low. From our review, this drastic drop in power efficiency is due to switching loss from parasitic capacitance associated to the output stage, characterized by $P_C = \frac{1}{2} C_P V_{DD}{}^2 f_c$, which becomes dominant at low input signal levels. This switching loss can be minimized by reducing the 3 parameters, namely the parasitic capacitance associated to the output stage, C_P, supply voltage, V_{DD}, or the switching frequency, f_c. We propose:

(a) Firstly, the possibility of segregating the output stage into different segments such that some segments will be turned off and separated when a low input signal is detected. This may possibly reduce C_P, which will in turn reduce the power loss.

(b) Secondly, the study into the possibility of merging the Class D technology with the Class G or Class H so that when a low input signal is detected, a lower V_{DD} is used. This objective here is to reduce P_C.

(c) Thirdly, a new modulation technique such that when a low input signal is detected, the switching frequency will slow down. This objective here is to reduce f_c which will eventually reduce the switching loss, P_C. Interestingly, this is somewhat the opposite of PDM where the highest switching frequency (most dense switching) occurs at low input signal. This is also different from PWM which has a fixed switching frequency.

(iii) We propose an investigation into the parameters that determine the power efficiency of the PDM CDA. The switching frequency of PDM is changing, as opposed to PWM which is fixed. From our literature review, we observed that in view of the crest factor of audio signals, the practical input audio signal is low and this might have implications on the power efficiency. At low input signal, the PDM is also switching at its fastest frequency and this may greatly increase the switching loss.

(iv) We propose to extend the investigation of power efficiency to filterless CDA. One method of realizing a filterless CDA is to increase the switching frequency to very high (eg. 800 kHz) and using a more inductive loudspeaker. The proposed investigation includes the tri-state modulation scheme [Chen, *et.al.*, 2001] where both the upper transistor and bottom transistor are switching in phase when input is zero.

References

[1] Analog Devices, "Class-D Audio Power Amplifier", Preliminary Technical Data AD1990/AD1992/AD1994/AD1996, 2005.

[2] Apex Microtechnology Corporation, "Pulse Width Modulation Amplifier", Application Note 30, February 2001.

[3] Austria Mikro Systeme (2006), "AMS HVMOS Process Parameters".

[4] Aziz P. M., Sorensen H. V., Der Spiegel J. V. (1996), "An Overview of Sigma-Delta Converters", *IEEE Signal Processing Magazine*, Vol. 13, No. 1, pp. 61-84, Jan 1996.

[5] Black H.S. (1953). Modulation Theory. Princeton, NJ: Van Nostrand, pp. 263-281.

[6] Bob Zurek, Meeting Highlights, "Audio Power Amplifier: A Brief History", *the Chicago section, Audio Engineering Society*, April 10, 2002.

[7] C. Cini, "A high efficiency, mixed-technology motor driver", Application note, STM.

[8] Candy J.C. and Temes G.C., "Oversampling Sigma-Delta Data Converters: Theory, Design and Simulation", Piscataway, NJ, *IEEE Press*, 1992.

[9] Carlo Cini, "Smart Power Processes For LSI Circuits", Application Note AN446, Dec 2003.

[10] Castello R. and Gray P.R. (1985), "A High-Performance Micropower Switched-Capacitor Filter", *IEEE J. Solid-State Circuits*, Vol. SC-20, No. 6, pp. 1122-1132.

[11] Chang J.S., Gwee B.H., Lon Y.S. and Tan M.T., "A novel low-power low-voltage Class D amplifier with feedback for improving THD. Power efficiency and gain linearity", *ISCAS'01*, Vol. 1, pp. 635-638, May 2001.

[12] Chang J.S., Tan M.T., Cheng Z. and Tong Y.C. (2000). "Analysis and Design of Power Efficient Class D Amplifier Output Stages". *IEEE Trans. CAS I: Fund Theory and App.,* Vol. 47*,* No. 6 pp. 897-902.

[13] Chen, *et.al.,* Texas Instruments, "Modulation Scheme for Filterless Switching Amplifiers", US Patent No. 6211728 B1, Apr 2001.

[14] Cheng Z. H. (1995), “Analysis and Design of a Micropower Low-Voltage Class D Audio Amplifier”, *Master Thesis, Nanyang Technological University, Singapore*, 1995.

[15] Christoph Deml, "Input and Reverse Transfer Capacitance Measurement of MOS-Gated Power Transistors Under High Current Flow", *IEEE Trans. Industry Applications,* Vol. 37, No. 4, July 2001.

[16] Corsi *et.al.,* Texas Instruments, "Concept and Method to Enable Filterless, Efficient Operation of Class-D Amplifiers", US Patent No. 6262632 B1, Jul 2001.

[17] Dan White, Sina Balkir, Michael Hoffman (2006), "CMOS Class D Amplifier with Output Optimization", *Audio Engineering Society*, Convention Paper 6859.

[18] David A. Johns and Ken Martin (1997), Analog Integrated Circuit Design, John Wiley & Sons, Inc..

[19] Don Dapkus and Robin Chen, "High-Efficiency Audio Amplification Using Class-D Audio Power Amplifiers", *IIC-Taipei Conference Proceedings*, Texas Instruments.

[20] Dondon, P.; Micouleau, J.M., "An original approach for the design of a Class D power switching amplifier-an audio application", *Electronics, Circuits and Systems. Proceedings of ICECS '99*, Vol. 2, pp. 161-164, Sep 1999.

[21] Douglas S. (2000), Audio Power Amplifier Design Handbook, 2nd Edition, Newsnes.

[22] Edison Fong, Droman C. Pitzer and Richard J. Zeman, "Power DMOS for High-Frequency and Switching Applications", *IEEE Trans. Electron Devices,* Vol. ED-27, No. 2, Feb 1980.

[23] Eldo Device Equations Manual, 2004

[24] Elmasry M.I. (1981), "Digital MOS Integrated Circuit: A Tutorial", Digital MOS Integrated Circuits, *New York, IEEE Press*, pp. 4-27.

[25] Eric Gaalaas, "Class D Audio Amplifiers: What, Why, and How", Analog Dialogue, 2006.

[26] Gaalaas E., Liu B.Y., Nishimura N., Adams R. and Sweetland K. (2005), "Integrated Stereo Delta-Sigma Class D Amplifier", *IEEE J. Solid-State Circuits*, Vol. 40, No. 12, pp. 2388-2397.

[27] T. Ge and J.S. Chang, “Power Supply Noise in Bang-Bang Control CDA,” *IEEE International Symposium on Circuits and Systems*, May 2007.

[28] T. Ge, J.S. Chang, W. Shu and M.T. Tan, “Modelling and analysis of PSRR in analog PWM Class D amp,” *IEEE International Symposium on Circuits and Systems*, pp. 1386-1389, May 2006.

[29] Ge T., Chang J.S., Shu W., Tan M.T. and Gwee B.H. (2007), "Modeling and Analysis of PSRR and IMD in Analog PWM Class D Amplifiers". *IEEE Journal of Solid-State Circuits*, (accepted for publication), 2007.

[30] Ge T., Shu W., Tan M.T., & Chang J.S. (2004). "A Low Power Low Voltage Class D Amp Based On Sigma-Delta And Bang-Bang Control". *IEEE International Workshop On Biomedical Circuits And Systems*, pp. S1.3INV-13 - 16.

[31] Ge T., Tan M.T., & Chang J.S. (2005). "Design And Analysis Of A Micropower Low-voltage Bang-Bang Control Class D Amplifier" *IEEE International Symposium On Circuits And Systems,* Vol. 1, pp. 224-227.

[32] Gennum Corp. (1996), "GC590 Linear Class H Amplifier", *GC590 Preliminary Data Sheet,* pp. 161-166, 1996.

[33] Gray P.R., Hurst P.U., Lewis S.H., & Meyer R.G. (2001). Analysis and Design of Analog Integrated Circuits, Fourth Edition, John Wiley & Sons, Inc..

[34] Harry J. M. Veendrick, "Short-Circuit Dissipation of Static CMOS Circuitry and Its Impact on the Design of Buffer Circuits", *IEEE Journal of Solid-State Circuits*, Vol. Sc-19, No. 4, Aug 1984.

[35] Haznedar H. (1991), Digital Microelectronics, Benjamin/Cummings Publishing Co., Inc., pp. 68-112 and 134-138.

[36] Hong M.Y. and Dimitri A. Antoniadis, "Theoretical Analysis and Modeling of Submicron Channel Length DMOS Transistors", *IEEE Trans. Electron Devices*, Vol. 42, No. 9, Sept 1995.

[37] IEEE spectrum, March 2003. *Digital Audio's Final Frontier*.

[38] International Rectifier, "HV Floating MOS-Gate Driver ICs", Application Note AN-978, December 2005.

[39] Israelsohn, Joshua, "Class D Gen3", *EDN*, pp. 49-58, April 15, 2004.

[40] J. Olsson, R. Valtonen, U. Heinle, L. Vestling, A. Söderbäg* and H. Norde, "A Capacitance-voltage measurement method for DMOS transistor Channel length extraction", *Proceeding of IEEE 1999 International Conference, Micorelectronic Test Structures,* Vol. 12, March 1999.

[41] Jensen J.A. (1987), "A New Principle for a High-Efficiency Power Audio Amplifier for Use with a Digital Preamplifier", *J. Audio Eng. Soc.*, Vol. 35, No. 12, pp. 984-993.

[42] Jorge Cerezo, "Class D Audio Amplifier Performance Relationship to MOSFET

Parameters", Application Note AN-1070, www.irf.com.

[43] Jun Honda and Jonathan Adams, "Class D Audio Amplifier Basics", Application Note AN-1071.

[44] Jung N.S., Kim N.I., & Cho G. H. (1998). "A New High-Efficiency and Super-Fidelity Analog Audio Amplifier with the aid of Digital Switching Amplifier: Class D Amplifier", *IEEE PESC* '98, pp. 457-463.

[45] Kashiwagi (1985), "A High Efficiency Audio Power Amplifier Using A Self Oscillating Switching Regulator". *IEEE Transaction on Industry Application,* Vol. IA-2*I*, No. 4, pp. 906-911.

[46] Komachi Tomonori, Nakaya Makoto, Tsuhako Jyukichi (1997), "Low Output Capacitance Solid State Relay", *Yokogawa Technical Report English Edition*, No. 23.

[47] Lee J.W., Lee J.S., Lee G.S., and Kim S.A., "2 W BTL single-chip CDA with very high efficiency for audio applications", *ISCAS'00*, Vol. 5, pp. 493-496, 2000.

[48] Li S.C., Lin V.C.-C., Nandhasri K. and Ngarmnil J., "New high efficiency 2.5V/0.45W RWDM Class-D Audio Amplifier for Portable Consumer Electronics", *IEEE Trans. CAS I,* Vol. 52, pp. 1749-1774, Sept 2005.

[49] Liu C.M. and James B. Kuo, "Quasi-Saturation Capacitance Behavior of a DMOS Device", *IEEE Trans. Electron Devices,* Vol. 44, No. 7, July 1997.

[50] Marco Berkhout (2002), "Integrated Class D Amplifier", *112th Convention of Audio Engineering Society*, Germany, May 2002.

[51] Marco Berkhout (2003), "A Class D Output Stage with Zero Dead Time", *IEEE International Solid-State Circuits Conference*. Paper 7.5

[52] Marco Berkhout (2003), "An Integrated 200-W Class-D Audio Amplifiers", *IEEE J. Solid-State Circuits*, Vol. 38, pp. 1198-1206, Jul 2003.

[53] Marco Berkhout (2005), "Integrated Overcurrent Protection System for Class-D Audio Power Amplifiers", *IEEE J. Solid-State Circuits*, Vol. 40, No. 11, pp. 2237-2245.

[54] Mellor P.H., Leigh S.P., Cheetham B.M.G. (1991), "Reduction of spectral distortion in class D amplifiers by an enhanced pulse width modulation sampling process", *IEE Proc*, Pt. G, Vol. 138, No. 4, pp. 441-448.

[55] Michael A. and Vladimir R., "Comparison of Lateral and Vertical DMOS Specific On-Resistance", Philips Laboratories, *IEEE*, 1985.

[56] Murari B., Bertotti F. and Vignola G.A. (1995), Smart Power ICs, PRODUserv Springer Produktions-Gesellschaft, Berlin.

[57] Murray J.M., Oleszek G.M. (1979), "Design Considerations in Class D MOS Power Amplifiers", *IEEE Trans. on Industrial Electronics and Control Instrumentation*, Vol. IECI-26, No. 4, pp. 211-218.

[58] Nielsen K. (1997), "A Review and Comparison of Pulse Width Modulation (PWM) Methods for Analog and Digital Input Switching Power Amplifiers", *102nd AES Convention*, 1997.

[59] Noro (2004). "Self-operating PWM Amplifier". US Patent No. 6707337 B2.

[60] Oh K.S., "MOSFET Basics", Fairchild Semiconductor, Jul 2000.

[61] Paolo Antognetti (1986), Power Integrated Circuits: Physics, Designs, and Applications, McGraw-Hill Book Company.

[62] Paul Morrow, Eric Gaalaas, Oliver McCarthy (2004), "A 20-W Stereo Class-D Audio Output Power Stage in 0.6-µm BCDMOS Technology", *IEEE J. Solid-State Circuits*, Vol. 39, No. 11, pp. 1948-1958.

[63] Ralph Jocher, "Introduction to Power MOSFETs and Their Applications", AN-558, National Semiconductor, Dec 1988.

[64] Rene P. Zingg, "On the Specific On-Resistance of High-Voltage and Power Devices", *IEEE Trans. Electron Devices,* Vol.51, No.3, March 2004.

[65] Robert S. Scott, Gerhard A. Franz and Jennifer L. Johnson, "An Accurate Model of Power DMOSFET's Including Interelectrode Capacitances", *IEEE Trans. Power Electonics*, Vol.6, No.2, April 1991.

[66] S.C. Sun and James D. Plummer, "Modeling of the On-Resistance of LDMOS, VDMOS, and VMOS Power Transistors", *IEEE Trans. Electron Devices,* Vol. ED-21, 1980.

[67] Sameer Pendharkar, Robert Pan, Takehito Tamura, Bob Todd and Taylor Efland, "7 to 30V state-of-art power device implementation in 0.25µm LBC7 BiCMOS-DMOS process technology", *Proceedings of 2004 International Symposium on Power Semiconductor Devices & ICs,*Kitakyushu, pp. 419-422, 2004.

[68] Score, *et.al.,* Texas Instruments, "Modulation Scheme for Filterless Switching Amplifiers with Reduced EMI", US Patent No. 6614297 B2, Sep 2003.

[69] Sedra A.S. and Smith K.C. (1998), Microelectronic Circuits, 4th Edition, Oxford University Press.

[70] Seong-Dong Kim, Cheol-Min Park and Jason C. S. Woo, "Advanced Model and Analysis of Series Resistance for CMOS Scaling Into Nanmeter Regime – Part II: Quantitative Analysis", *IEEE Trans Electron Devices,* Vol. 49, No. 3, March 2002.

[71] Shu W., Chang J.S., Ge T., and Tan M.T., "FBD and EMI in the PDM Class D Amplifier", *ISCAS'07* (submitted for publication), 2007.

[72] Shu W., Chang J.S., Ge T., and Tan M.T., "Fourier Series Analysis for Nonlinearities due to Power Supply noise in Open-Loop PWM Class D Amplifiers", *IEEE APCAS*, pp. 721-724, Dec 2006.

[73] Shu W., Chang J.S., Ge T., and Tan M.T., "Fourier Series Analysis of the Nonlinearities in Analog Closed-loop PWM Class D Amplifiers", *IEEE International Symposium on Circuits and Systems*, 2006.

[74] Takagishi T. (2002), "Class D Audio Amp," US Patent No. 6420930.

[75] Tan M.T. (1997), Analysis, Design and IC Implementation of an Audio Class D Amplifier for Micropower Low-Voltage Applications, *Master Thesis, Nanyang Technological University, Singapore.*

[76] Tan M.T., J.S. Chang, H.C Chua and B.H. Gwee, "An investigation on the parameters affecting total harmonic distortion in a CDA", *IEEE Trans. CAS I*, Vol. 50, No. 10, Oct 2003.

[77] Texas Instruments, "Advanced Low-Voltage Technology", Jul 1999.

[78] Texas Instruments, "True Digital Audio Amplifier TAS5110 PWM Power Output Stage", Sep 2002.

[79] Texas Instruments, "Design Considerations for Class-D Audio Power Amplifiers", Application Report, Aug 1999.

[80] Texas Instruments, "Reducing and Eliminating the Class-D Output Filter", Application Report, Aug 1999.

[81] V.A.K. Temple and P.V. Gray, "Theoretical Comparison of DMOS and VMOS Structures for Voltage and On-Resistance", General Electric Company, *IEEE*, 1979.

[82] Vishay Siliconix, "P-Channel MOSFETs, the Best Choice for High-Side Switching", Document No. 70611, Mar 1997.

[83] Vittoz E.A. and Fellrath J. (1977), "CMOS Analog Integrated Circuits based on Weak Inversion Operation", *IEEE J. Solid-State Circuits*, Vol. SC-12, No. 3, pp. 224-231.

[84] Vrej Barkhordarian, International Rectifier, "Power MOSFET Basics", www.irf.com.
[85] W. Marshall Leach, "The Class-D Amplifier", 2001.

[86] Wolfgang Pribyl, "Integrated Smart Power Circuits Technology, Design and Application", Siemens Mikroelektronik, Austria.

[87] Wu C.M., Lau W. and Chung H.S., "Analytical technique for calculating the output harmonics of an H-bridge inverter with dead time", *IEEE Trans. CAS 1,* Vol. 46, No. 5, May 1999.

[88] Zhang Jason (2004), "Choosing the Right Power MOSFET Package", International Rectifier.

Appendix A

The parameters used to calculate Figure 3.1 (page 50), based on a standard *n*-channel DMOS, are shown below:

f_c	200 kHz
M	0.2
τ	5 ns
R_L	8 Ω
I_O	V_{DD} / R_L
V_{thn}	1.137 V
μ_n	450.8 cm^2/V.S
t_{ox}	1.35 x10^{-8} m
ε_{ox}	3.45x10^{-11} F/m
C_J	1.0 x10^{-15} F/m
C_{GSO}	1.0 x10^{-15} F/m
C_{GDO}	1.0 x10^{-15} F/m
C_{JSW}	1.0 x10^{-10} F/m
C_{pad}	2 pF/pad
R_n	105 Ω/□
R_{ctn}	73 Ω/cont.
L	0.35 μm
L_{DS}	5.4 μm
$l_1=l_2$	0.8 μm
l_3	3.8 μm