NANYANG TECHNOLOGICAL UNIVERSITY

VOLTAGE REFERENCE CIRCUITS FOR LOW VOLTAGE APPLICATIONS

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Voltage Reference Circuits for Low Voltage Applications

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Summary

Two current mode CMOS voltage reference circuits were designed in this project. These two circuits were constructed using two different processes: the Austria Micro Systems (AMS) 0.6 µm and AMI Semiconductor (AMIS) 0.5 µm technologies. The proximity of threshold voltages of the MOSFET transistors (0.85 V in AMS 0.6 µm and 1 V in AMIS 0.5 µm) to the supply voltage had created challenging problems to the low voltage (< 1.2 V) circuits.

A voltage reference circuit with 1 V supply was successfully implemented using the AMS 0.6 µm technology. The designed output voltage at 0.6 V achieved a temperature coefficient (*TC*) of 11.7 ppm/ºC and a power supply rejection ratio (*PSRR*) of about -54 dB. Other than using an enhancement feature in the amplifier, the self-cascode composite transistor was also implemented in the entire voltage reference circuit to further improve on the *PSRR* as well as on the current accuracy.

In the second design, a voltage reference circuit with only MOSFET transistors and resistors was designed. The core circuit (proportional-to-absolute-temperature current generator) was constructed using sub-threshold operated NMOS transistors instead of the bipolar transistors. A resistance reduction technique has been explored in this work in order to resolve the large resistance value necessary for attaining the low power specification in the low voltage regime. For the same resistance values in equivalent circuits, the proposed work has an advantage of power saving when compared to the conventional method of circuit construction. Nonetheless, the *TC* at 1.2-V supply was simulated to be of around 62 ppm/ºC., which was not as good as the first design. The achievable *PSRR* was about -50 dB, and comparable to that obtained in the earlier design. Supply dependency of the work is simulated to be 1.65 mV/V over a range of 1.2 V to 1.9 V supply voltage under typical transistor model. Other than typical case simulation, simulation results with 4-corner models are also provided in each section and all the graphs are plotted in Appendix C.

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Chapter 1

Introduction

1.1 Background

The feature of low-voltage and low-power, in the context of System-On-Chip (SOC) application are gaining focus rapidly as a result of steadily growing demand on battery-powered portable and miniaturized electronic appliances in today's market. These application ranges from small biomedical systems such as hearing aids, to larger and more sophisticated devices, like digital camera, music player, hand phone and laptop.

From devices point of view, as the feature size of the semiconductor devices continue to scale down, the electric field in the devices will increase and the power consumption per area rise due to high packing density. This leads to degradation in the reliability of the integrated circuits (ICs) such as the package-related failure, electro-migration (EM), and silicon interconnection fatigue. It is therefore a must to develop low-voltage and low-power ICs to cater to the foreseeable problems due to device dimension shrinkage. It is anticipated that the CMOS transistor may have a channel length of merely 25 nm in the future [1]. This unavoidable trend on developing low voltage and low power designs is not just attributed to the technology constraints discussed earlier, but also due to the need to prolong battery life-span.

Many analog and digital circuits require voltage references. The reference establishes a stable voltage point, for used by other sub-circuits, to help generate predictable and repeatable results. This reference point should not fluctuate significantly under various operating conditions, such as during varying power supply voltages, temperature drifts, or transient loading events. A few examples of

circuit applications where references are intrinsically required are the digital-to-analog converters (DAC), analog-to-digital converters (ADC) and linear regulators. These sub-systems are of course the fundamental elements that make up cellular phones, laptops and many other popular electronic products.

By definition, a bandgap reference circuit (BRC), one type of voltage reference circuits (VRC), is a voltage reference whereby the output voltage is referred to the bandgap energy of the semiconductor employed in the circuit. Conventional voltage mode bandgap structures allow us to achieve a reference voltage of about 1.2 V, with minimum sensitivity to temperature variation. However, when the supply voltage goes down to 1.2 V or below, it is no longer possible to use the conventional voltage mode structures. Hence, the current mode approach which employs additional currents to establish the zero *TC* voltage should be used.

The intention to design low voltage and low power voltage reference circuit creates many design problems. This is because the available voltage headroom is reduced accordingly. This makes it especially challenging for circuit designs that engage the standard CMOS process since the threshold voltage of the devices are close to the lowest supply voltage that the circuit intends to achieve, at say 0.85 V for both the PMOS and NMOS in the case of AMS 0.6 μm process, for a single supply of 1 V. These constraints not only impose difficulties in the implementation of the widely-used conventional design style of cascode method (stacking of devices) for the purpose of obtaining better rejection to power supply noise, but also limits the input common mode voltage of the amplifier that directly affect its performance for example the voltage gain. Other than the issues discussed, the resistors to be used in the circuit are generally larger so as to keep the total supply current low for reduced power consumption. This then leads to a larger die area.

The critical parameters of a voltage reference are mainly characterized by the circuit's average temperature coefficient (*TC*), power consumption, accuracy, supply dependency and power supply rejection ratio (*PSRR*). The average *TC* is generally expressed in parts per million per Kelvin, ppm/K (or degree Celsius, ppm/ºC)

1.2 Objectives

The objective of this project is to design a CMOS voltage reference circuit that can operate at a supply voltage of 1.2 V or below. The complete circuit block will be simulated, laid out and fabricated using the AMS 0.6 µm CMOS n-well process and AMIS 0.5 µm CMOS n-well process for two different proposed works respectively.

The focus will be mainly on addressing the issues mentioned in the previous section and to improve the performance parameter of the voltage reference circuit through the use of different design techniques. The basic guidelines are listed below:

- Operating at supply voltage as low as 1.2 V.
- A temperature operating range of 0ºC to 100ºC.
- With fairly independent of temperature coefficient, of below 50 ppm/ºC.
- Having a good *PSRR* of more than 40 dB at 1 kHz.

1.3 Major Contribution

This research work had demonstrated a 1 V CMOS voltage reference circuit with improvement in *PSRR* performance by using the gain enhancement amplifier and the technique of self-cascode composite transistor, which is easier to be employed in low voltage regime as compared to conventional cascode transistor. The work proposed in Chapter 4 also provides a way to reduce the large resistor in the voltage reference core circuit due to low power requirement and an alternative solution to address the problem of limited input common mode voltage of the PMOS input stage amplifier. Both voltage reference circuit designed offers cost saving potential as the circuit is implemented in a relatively cheaper process with a higher threshold voltage.

In conclusion, objectives of this research are accomplished successfully. Two voltage reference circuits with improved power supply rejection ratio and reduction in resistance are demonstrated.

1.4 Organization of Work

This thesis consists of five chapters. The introduction at Chapter 1 provides the background, objective of the work. Literature review on the circuit strategies for voltage reference with low supply voltages will be discussed in Chapter 2. Chapter 3 presents the first design of the voltage reference circuit together with the simulation and measurement results. The second proposed work on resistance reduction is detailed in Chapter 4. Finally, the conclusion and recommendation for future development are given in Chapter 5.

Chapter 2

Literature Review

Voltage reference provides a constant output voltage that is independent of temperature, supply voltage, line noise, process variation and other operating conditions in an idea case. It therefore plays an important role in circuit systems and finds wide applications in circuitries such as oscillators, Phase Lock Loops (PLLs), Analog-to-Digital (A/D) and Digital-to-Analog (D/A) Converters, Dynamic Random Access Memories (DRAM), etc.

This chapter gives a brief discussion on the principle of voltage reference. A review on both the conventional and state-of-the arts of the voltage reference circuitries will also be provided.

2.1 Principle of Voltage Reference

There are number of ways to realize reference voltage in IC. These methods include: (1) the use of zener diode that breaks down at a known voltage when reversed biased [32], (2) the deployment of the difference in the threshold voltages between an enhancement transistor and a depletion transistor [8], and (3) through cancellation of negative temperature dependence of a p-n junction via the Complementary-to-Absolute Temperature (CTAT) using a positive temperature dependence Proportional-to-Absolute Temperature (PTAT) circuit [2], which incidentally is the most popular approach nowadays.

2.1.1 Complementary-to-Absolute Temperature - A Negative Temperature Coefficient [3]

The forward biased base-emitter voltage, V_{BE}, of bipolar transistors exhibits a negative temperature coefficient (TC) [3]. According the [3], the collector current of a bipolar transistor is defined as:

$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right) \tag{2.1}$$

where V_T is the thermal voltage, which is equal to kT/q. I_S is the saturation current in the forward-active region which can be further expressed as:

$$I_S \approx bT^{4+m} \exp\frac{-E_g}{kT}, \tag{2.2}$$

where b is a proportionality factor, $m \approx -3/2$, and $E_g \approx 1.12$ eV is the bandgap energy of silicon. Re-writing Equation (2.1) and expressing I_C as a function of V_{BE}, followed by taking the derivative of V_{BE} with respect to temperature, T, the behavior of I_C as a function of the temperature can be easily obtained.

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T}\ln\frac{I_C}{I_S} - \frac{V_T}{I_S}\frac{\partial I_S}{\partial T}. \tag{2.3}$$

From (2.2),

$$\frac{\partial I_S}{\partial T} = b(4+m)T^{3+m}\exp\frac{-E_g}{kT} + bT^{4+m}(\exp\frac{-E_g}{kT})(\frac{E_g}{kT^2}). \tag{2.4}$$

Therefore,

$$\frac{V_T}{I_S}\frac{\partial I_S}{\partial T} = (4+m)\frac{V_T}{T} + \frac{E_g}{kT^2}V_T. \tag{2.5}$$

With the aid of (2.3) and (2.5),

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_T}{T}\ln\frac{I_C}{I_S} - (4+m)\frac{V_T}{T} - \frac{E_g}{kT^2}V_T$$
$$= \frac{V_{BE} - (4+m)V_T - E_g/q}{T}. \qquad (2.6)$$

Equation (2.6) gives the *TC* of the base-emitter voltage at a given temperature, *T*, revealing dependence on the magnitude of V_{BE} itself. With $V_{BE} \approx 593$ mV, which is used in the design in Chapter 3, and $T = 300$K, $\partial V_{BE}/\partial T \approx -2.2$ mV/K.

MOSFETs in weak inversion exhibit similar characteristic as BJT. The drain current in weak inversion is expressed as follows [4]:

$$I_D = \frac{W}{L} I_{DO} e^{\frac{V_G}{nV_T}} \left(e^{-\frac{V_S}{V_T}} - e^{-\frac{V_D}{V_T}} \right) \qquad (2.7)$$

where *W/L* is the effective geometrical shape factor of the transistor; and V_G, V_S, and V_D are the gate, source, and drain potentials, with respect to the substrate/bulk. The characteristic current I_{DO} is very sensitive to process and temperature variations, whereas the slope factor *n* is fairly controllable but is still dependent on temperature. *n* can be found using the following formula:

$$n = 1 + \frac{C_{BC}}{C_{OX}} + \frac{q \times NFS}{C_{OX}} \qquad (2.8)$$

where C_{BC} is the bulk junction capacitance per unit area, C_{OX} is the gate oxide capacitance per unit area and *NFS* is the fast surface-states.

To ensure that the transistor is operating in the weak inversion/sub-threshold region, it has to fulfilled the conditions where, $I_D \le \frac{W}{L}\mu C_o \frac{(n-1)}{e^2} V_T^2$ with $V_D - V_S > 3V_T$.

2.1.2 Proportional-to-Absolute Temperature – A Positive Temperature Coefficient

Most of the Proportional-to-Absolute Temperature (PTAT) generators are constructed using bipolar junction transistors, BJT. This is because BJT has been proven to be the most reproducible, predictable (± 2 to 5 %), and well-defined electronic component to yield the PTAT and CTAT characteristics. The relationship of PTAT was first discovered by *Hilbiber* in 1964 [5]. According to his finding, PTAT is in fact the difference between two BJTs whereby each operates with unequal emitter current densities. Figure 2.1 provides an illustration of the concept.

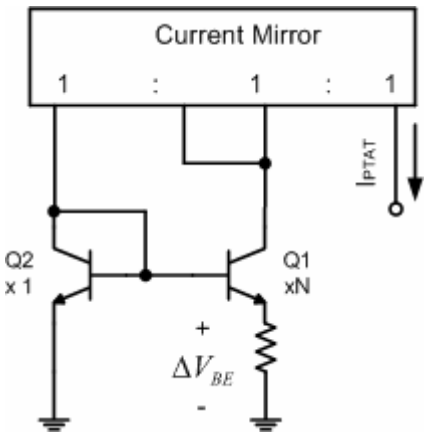


Figure 2. 1 Generation of PTAT component using BJT.

By applying Kirhhoff's Voltage Law (KVL) to the loop involving transistors Q_1, Q_2 and R, and assuming the base current to be negligible, the following equation can be obtained.

$$\begin{aligned}\Delta V_{BE} &= V_{BE1} - V_{BE2} \\ &= V_T \ln\left(\frac{I_{C1}}{I_{S1}}\right) - V_T \ln\left(\frac{I_{C2}}{I_{S2}}\right) \\ &= V_T \ln\left(\frac{I_{C1}}{A_{E1} \times I_S}\right) - V_T \ln\left(\frac{I_{C2}}{N \times A_{E1} \times I_S}\right)\end{aligned}$$

$$\Delta V_{BE} = V_T \ln(N) = \frac{kT}{q} \times \ln(N) \qquad (2.9)$$

where I_{C1} and I_{C2} are the collector currents of Q_1 and Q_2 respectively, A_E is the emitter area of Q_2 and the emitter area of Q_1 is N times larger than Q_1.

By differentiating the above equation, it can be shown that the V_{BE} difference gives rise to a positive temperature coefficient that is independent of the collector currents of the two BJTs.

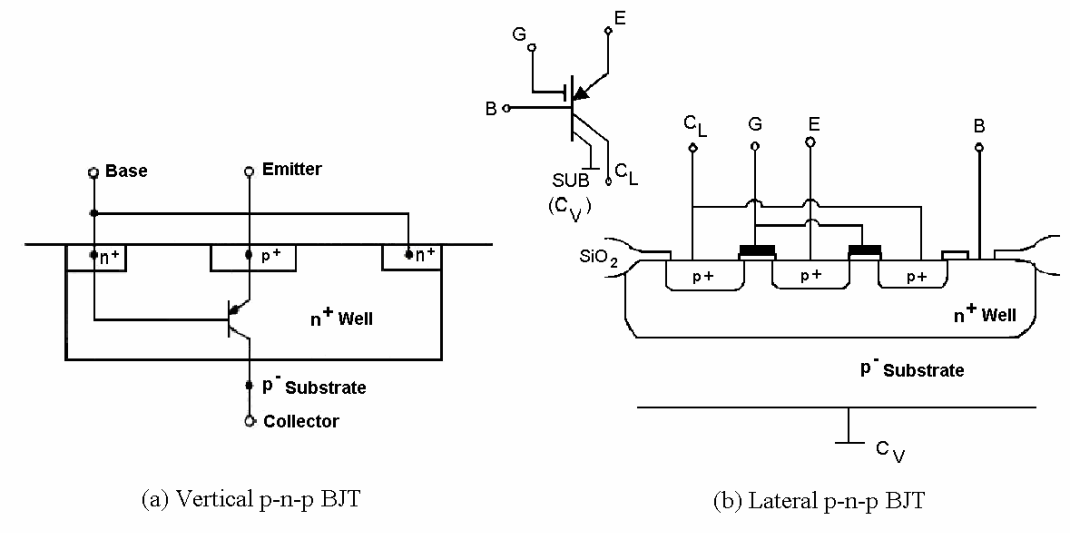


Figure 2. 2 Parasitic BJT in CMOS n-well process.

As scalable and cost effective CMOS technology becomes a dominant process in today's market, many circuits are designed using CMOS. However, to construct a voltage reference in CMOS, the BJT required would to be the parasitic components. They are the vertical and lateral BJTs when implemented in CMOS process. The symbol and the corresponding cross sectional view of the two BJTs are show in Figure 2.2. These transistors have intrinsic limitations which surface during the development of high performance voltage references. The main drawback is the series base resistance due to large lateral dimension between the base contact and the effective emitter region [2]. Another major source of error is the offset voltage of amplifier, leading to a large variation in the output of reference voltage and consequently, to a very large degradation of the temperature stability [6].

Using the same topologies as the BJT counterpart, MOSFET can also be used to generate the required PTAT component as well [7] [8] [9]. Figure 2.3 demonstrates

the creation of PTAT using MOSFET. Note however that the MOSFET devices must be operated at the sub-threshold (weak inversion) region. This is because under the sub-threshold condition, the drain current is exponentially dependent on the gate-source voltage, V_{GS}, and it is this characteristic that is exploited by the circuit topology.

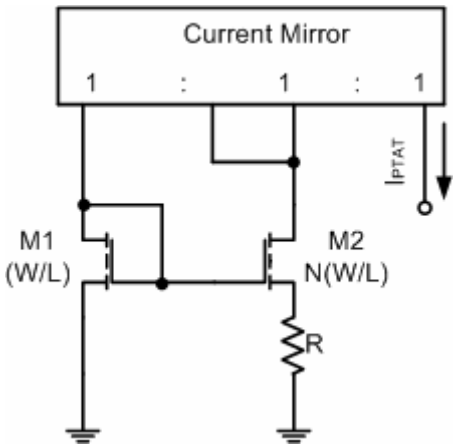


Figure 2. 3 Genertation of PTAT component using MOSFET [10].

By applying KVL to the voltage loop of Figure 2.3, the relationship of the output current can be derived, where

$$I_{PTAT} = \frac{V_T}{R}\ln\left[\frac{N(W/L)}{(W/L)}\right] = \frac{V_T}{R}\ln(N) \qquad (2.10)$$

Although it is feasible to implement PTAT with sub-threshold MOS devices, its leakage currents can actually overwhelm the drain current at moderately high temperature [11]. As a result, the temperature range for which a sub-threshold device is useful may instead be limited.

2.2 Conventional Voltage Reference – Voltage Mode Approach

The first voltage reference circuit was proposed by *Robert Wildar* in 1971 [12]. The design made used of the summation of two complementary temperature dependent components, namely V_{BE} and V_T. The two parameters are related by M, which is a temperature compensation factor (see Figure 2.4). Since then, the

temperature stability of the voltage reference circuits are continuously being improved through new circuit designs and technology enhancement. An example of such is the used of the curvature-compensated voltage reference circuit [13].

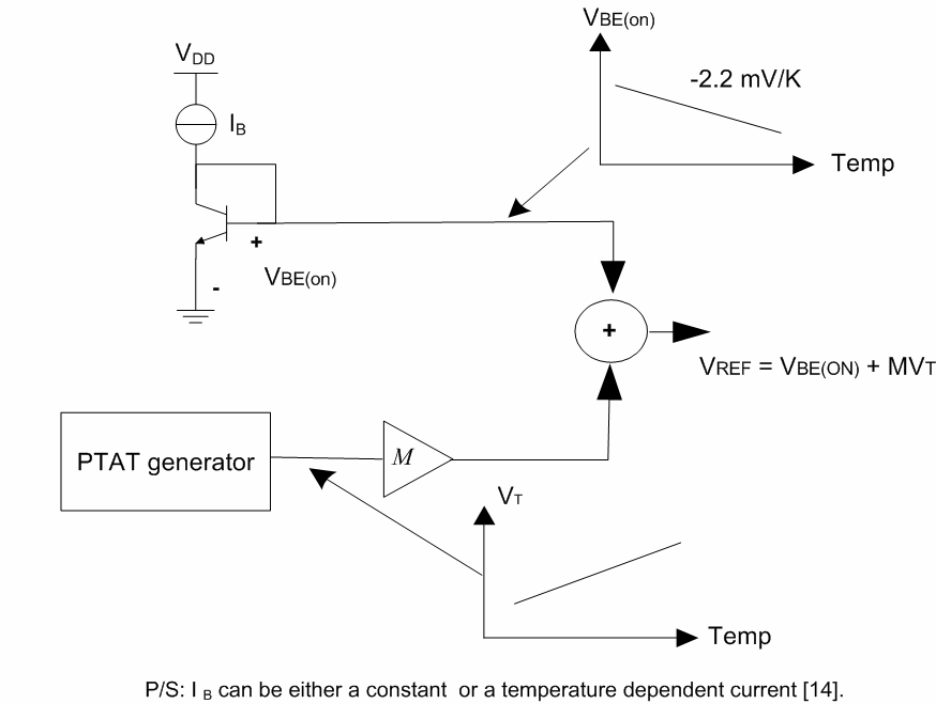


Figure 2. 4 Hypothetical voltage mode voltage reference circuit [14].

Shown in Figure 2.5 is the actual implementation of the conventional voltage reference [14]. The amplifier with gain of A senses V_X and V_Y, driving the top terminals of R_1 and R_2 ($R_1 = R_2$) such that X and Y settle to approximately equal voltages. This will also cause the currents flowing through R_1 and R_2 to be the same. By taking in offset voltage, the following equations can be derived.

$$I_2 R_3 = V_{BE1} - V_{BE2} = V_T \ln(N) + V_{OS}$$

$$I_2 = \frac{1}{R_3}\left[V_T \ln(N) + V_{OS}\right] \qquad (2.11)$$

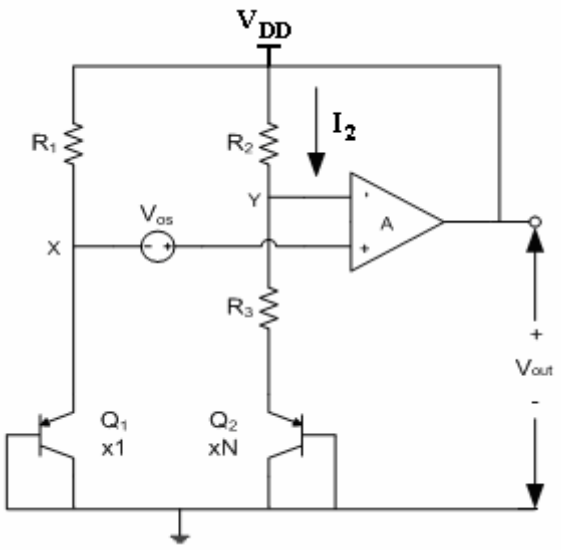


Figure 2. 5 Conventional voltage reference circuit in CMOS n-well process.

The output voltage is obtained at the output of the amplifier,

$$V_{out} = V_{EB2} + I_2(R_3 + R_2)$$
$$= V_{EB2} + \left[V_T \ln(N) + V_{OS}\right] \times \left(1 + \frac{R_2}{R_3}\right) \qquad (2.12)$$

For a zero *TC*, it is required that $(1 + R_2/R_3) \times \ln(N) \approx 17.2$ at room temperature and the output voltage approximately equal to 1.25 V, which is close to the bandgap voltage of silicon. That is also how the name of bandgap reference is derived. It is obvious that the output voltage is always greater than 1.2 V, and so the supply voltage must be greater than 1.2 V. Thus, voltage mode approach is not suitable for implementing low-voltage bandgap reference, where the power supply is usually lower than 1.2 V.

2.3 Low Supply Voltage Reference – Current Mode Approach

In order to overcome the limitations discussed in the previous section of the voltage mode approach, the current mode approach proposed by *H. Banba et al.* [15] becomes a favorite design style for low supply voltage reference circuit.

The idea of generating the voltage reference using current-mode approach is to sum up two currents, PTAT and CTAT currents, to yield a zero temperature coefficient current, I_{ZTC}. The output voltage is generated by transforming the I_{ZTC} into voltage through a resistor. Figure 2.6 illustrates this concept schematically.

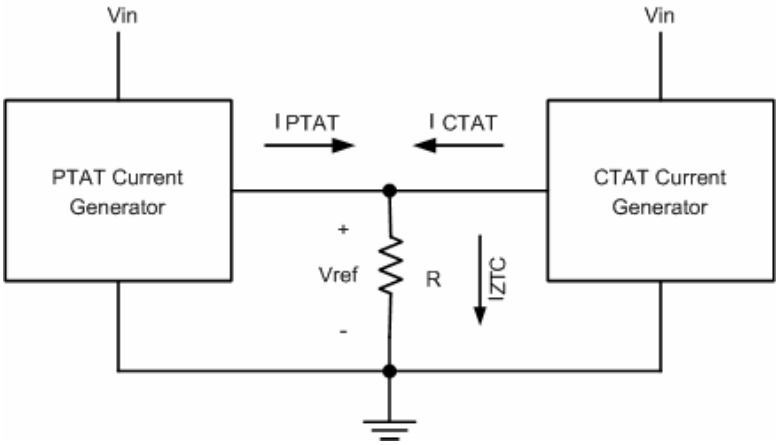


Figure 2. 6 Hypothetical current mode voltage reference circuit.

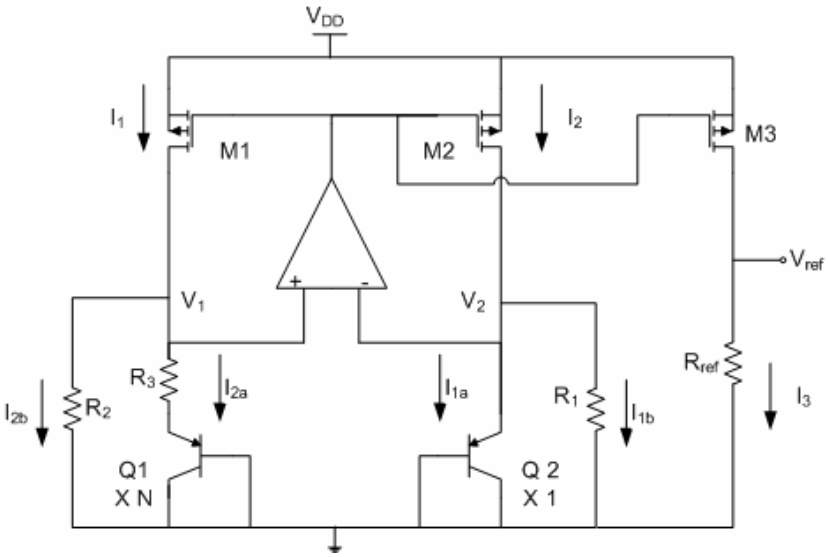


Figure 2. 7 *H. Banba et al.* voltage reference circuit [15].

The schematic diagram shown in Figure 2.7 is a voltage reference circuit proposed by *Banba et al.*. By enforcing both V_1 and V_2 at equal potential through the negative feedback of the op-amp, a loop formed by Q_1, Q_2, R_1, R_2 and R_3 produces a desired positive and negative temperature current. Assuming the aspect ratio of transistors M1 and M2 to be the same, and that the resistance of R_1 is the same as R_2, the circuit yields $I_1 = I_2$ and $I_{1b} = I_{2b}$. Both the positive and negative *TC* currents can be expressed by the following equations:

$$I_{PTAT} = I_{1a} = I_{2a} = \frac{\Delta V_{EB}}{R_3} = \frac{V_{EB2} - V_{EB1}}{R_3} = \frac{V_T \ln N}{R_3} \tag{2.13}$$

$$I_{CTAT} = I_{1b} = I_{2b} = \frac{V_{EB2}}{R_1} \tag{2.14}$$

where N is emitter area ratio.

And the temperature independent current is:

$$I_{ZTC} = \frac{V_T \ln N}{R_3} + \frac{V_{EB2}}{R_1} \tag{2.15}$$

I_{ZTC} is mirrored to the V_{ref} branch to yield the output reference voltage. Hence, V_{ref} can be represented as follow:

$$V_{ref} = R_{ref} \times \left[\frac{V_{EB2}}{R_2} + \frac{V_T \times \ln(N)}{R_3} \right] \tag{2.16}$$

As can be seen in Equation (2.16), the resistance is in ratio form. This implies that even if the resistors have finite *TC*, as long as the same type of resistor is used, the temperature effect will be cancelled out. Thus, the matching of the resistors becomes a crucial factor to ensure the accuracy of the reference voltage.

In *Banba's* [15] work, the op-amp inputs are connected to V_1 and V_2, and that is a diode drop. For op-amp with PMOS input stage, such input voltage level is unlikely to keep the two PMOS transistors operating in the saturation region, especially if the circuit is designed in a process that has transistor's threshold voltage as high as 0.85 V at room temperature and yet have to work within a supply voltage of only 1 V.

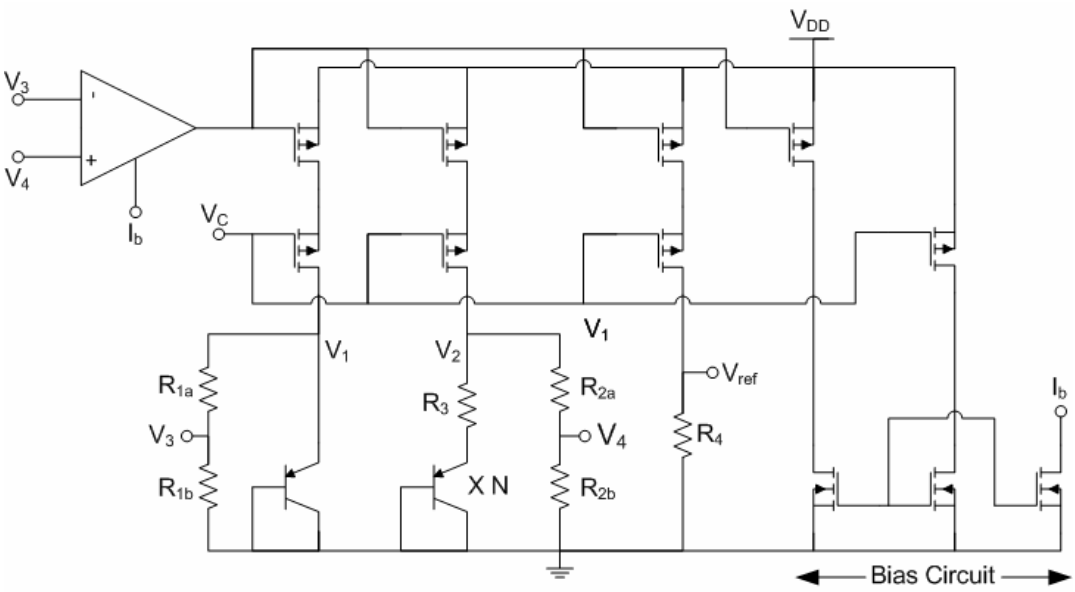


Figure 2. 8 Modified voltage reference proposed by *Waltari et al.*

Figure 2.8 is the design proposed by *Waltari el al.* [16] on solving the above drawback in *Banba's* work. This modified circuit suggested that resistors R_1 and R_2 be divided into two series connected resistors, which is R_{1a} and R_{1b} for R_1, and R_{2a} and R_{2b} for R_2. Instead of connecting V_1 and V_2, the op-amp inputs are tie to V_3 and V_4. This allows the voltages to be controlled within the common mode input voltage of the op-amp through the adjustment of resistance values. The deduced output voltage is formularized as follows:

$$V_{ref} = \frac{R_4}{R_{(1,2)}}\left[V_{EB} + \frac{R_{(1,2)}}{R_3} \times V_T \ln(N)\right] \tag{2.17}$$

The same topology had been adopted by *K. N. Leung* [17]. The focus is to use low cost process and so the devices' threshold voltages are usually higher than those in the advanced processes. Other than this, improvements over this basic topology at low supply voltages include the curvature compensation [18]-[20], reduced power consumption [21], improved *PSRR* [22], etc.

In order to form a loop to create the PTAT component, the design of the voltage reference circuit often utilize op-amp to ensure or to maintain the two nodes at the same voltages at the differential inputs (see V_3 and V_4 in Figure 2.8). Thus, parameters like gain, phase margin, offset, etc., must all be carefully considered.

The op-amp should have a certain gain, say 60 dB, without bandwidth constraints over the temperature range of interest. With that, the difference between V_3 and V_4 will be negligible over the desired operating temperature range.

An example of a low voltage op-amp circuit [20] is presented in Figure 2.9. This permits a saving of voltage headroom of 0.15 V. The circuit does not engage conventional input differential stage but instead, two grounded BJTs (Q_3 and Q_4) are employed. Hence, the required bias currents are replicated from the reference core circuit. A two-stage structure is used in the design as the low supply voltage prevents the use of cascode configuration. Although such structure offers a solution that is suitable for op-amp applications with low supply voltage, with a reported dc gain of 60 dB, it requires costly BiCMOS process, which incidentally is not available for this project.

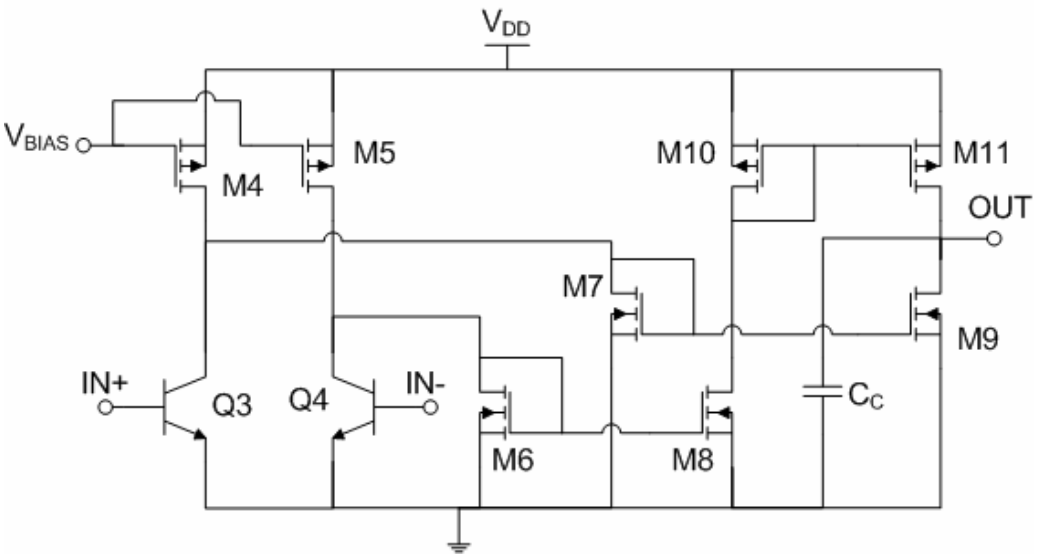


Figure 2. 9 Low offset op-amp [20].

The voltage reference circuit proposed by *K. N. Leung* [17] suggested a low voltage amplifier with dc level-shifting current mirror. As depicted in Figure 2.10, the proposed amplifier employs a dc level-shifting current mirror [23] with balanced op-amp so as to ensure the amplifier functioning properly within 1 V supply voltage. However, the gain may not be high enough to sustain the performance over a wide temperature range since it is only a one-stage amplifier.

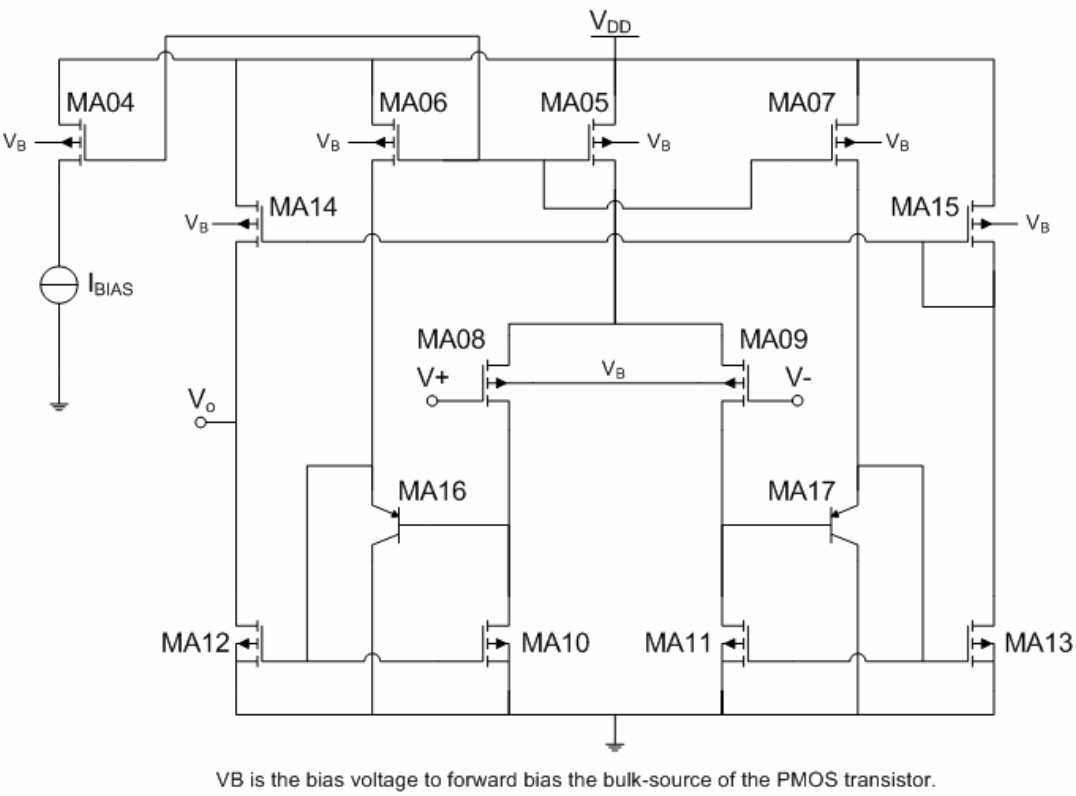


Figure 2. 10 Amplifier with dc level-shifting [17].

2.4 Summary

In the voltage reference context, two approaches are used to generate reference voltage, namely, the voltage mode and current mode. In voltage approach, although it has been widely used for the past few decades, the method is only applicable to supply voltage that are greater than 1.2 V. this then becomes a bottleneck for low voltage (< 1.2 V) circuit. Therefore, to generate a reference voltage that is lower than 1.2 V, the current mode approach is used. Having said that, the current mode approach requires more resistors to achieve the same function as compared to the conventional voltage mode topology. The current mode is therefore not only expected to occupy a larger die area as well as having more matching issues.

A numbers of publications [15] – [22] based on the current mode approach have been reported in recent years. These works include: low supply (< 1 V) voltage reference without the need of low V_{TH} device [17], improvement in *TC* performance [20], improved *PSRR* performance [22] [24], etc. Other than this,

several design styles had also been proven to be able to attain low reference voltage [25] [26]. However, limitations such as supply voltage and reference voltage constraints, high resistance used (large die area), high power consumption, etc, must all be overcome in order to ensure better performance.

Chapter 3

1 V Supply Voltage Reference Circuit

Insensitivities to temperature variation and noisy digital supply noise are the desired key performance parameters of a voltage reference circuit (VRC) in a mixed-signal system. In order to improve the power supply rejection ratio (*PSRR*), a self-cascode composite transistor technique and a gain enhancement amplifier have been employed in the proposed VRC. The proposed work, which built on Austria Mikro Systeme (AMS) CMOS 0.6 μm, n-well process, has a temperature coefficient (*TC*) of 30.15 ppm/°C, a *PSRR* of -54 dB, and a current consumption of 32 μA at 1 V supply voltage.

In this design, Mentor Graphics simulation and layout tools, Design Architect IC and IC station, are adopted. Unless specify, simulation results shown in this chapter are all simulated using BSIM3v3 typical models at 27°C.

3.1 Introduction

PSRR is one of the key performances in VRC design. The scaling down of power supplies significantly diminishes the voltage headroom of VRC. As a result, the *PSRR* performance is anticipated to degrade drastically. This is because the conventional cascoding (stacking of devices) and pre-regulated techniques [10] that are used to yield high output impedance can hardly be implemented in low supply condition. The use of the advanced CMOS technologies reported in [15] [22] [25] offer straight forward solution to the problem. This however is at the expense of higher cost in exchange of the “easy solution”.

The proposed VRC in this chapter is based on a published work by *K. N. Leung* [17]. Design techniques such as self-cascode composite transistor [27], and gain enhancement amplifier have been added to improve the *PSRR* of VRC.

3.2 Process Information

A solid understanding on device process is crucial in the design and layout of integrated circuits (ICs). This is especially useful where many of the many limitations impose on the performance of the circuits are closely related to the process used.

3.2.1 Threshold Voltage of MOSFET

The proposed 1 V VRC is built on standard Austria Mikro Systeme (AMS) CMOS 0.6 µm, n-well process. The threshold voltage, V_{TH}, of the process is a bottleneck in the actual implementation of low voltage circuits and it is a critical parameter to decide the lowest supply voltage that a circuit can work on. For the AMS 0.6 µm n-well CMOS process, the NMOS and PMOS transistors exhibit threshold voltages of around 0.85 V and -0.80 V, at 27°C respectively. These two figures are considered high as compared to those advanced process, say 0.18-µm process or even smaller feature size technology, which has lower threshold voltage.

I. Threshold Voltage versus Channel Length Characteristic

Depicted in the Figures 3.1 and 3.2 are the threshold voltages of the NMOS and PMOS transistors versus the channel length and different channel width respectively. These data are extracted from BSIM3v3 models using simulation tool – Design Architect IC. Due to drain induced barrier lowering (DIBL) effect the threshold voltage decreases as channel length is decreased [28], see Figure 3.1. In order to operate transistor with rather constant V_{TH}, at a particular biasing condition, the channel length is preferably greater than 1.3 µm. However, working with a NMOS transistor with channel length that is at 1.3 µm, the design will be prone to process variation, especially if the channel length decreases to below 1.3 µm

during fabrication. To make the design less vulnerable to process variations, the channel lengths of the NMOS transistors are designed to be at least 2 µm. Exception to this rule can then be allowed for the transistors used such that they can perform their function well even if their V_{TH} drops due to having short channel effect.

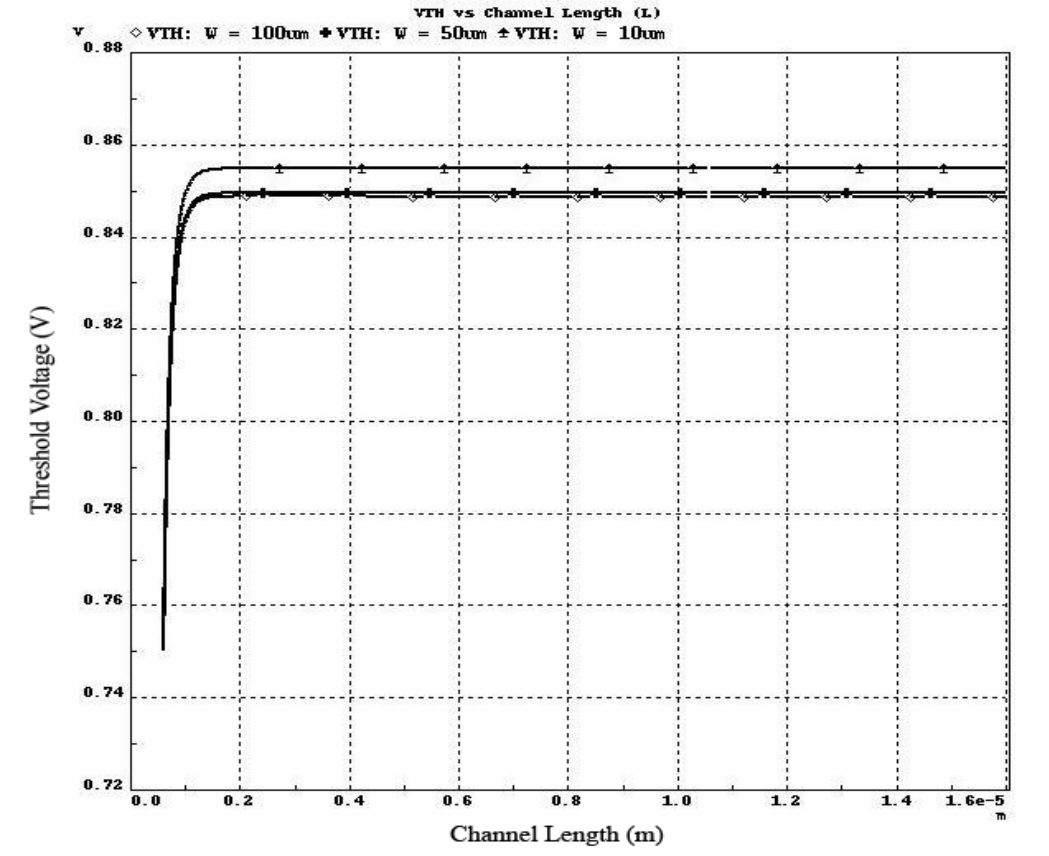


Figure 3. 1: NMOS - V_{TH} versus channel length (L), with W = 10 µm, 50 µm, and 100 µm.

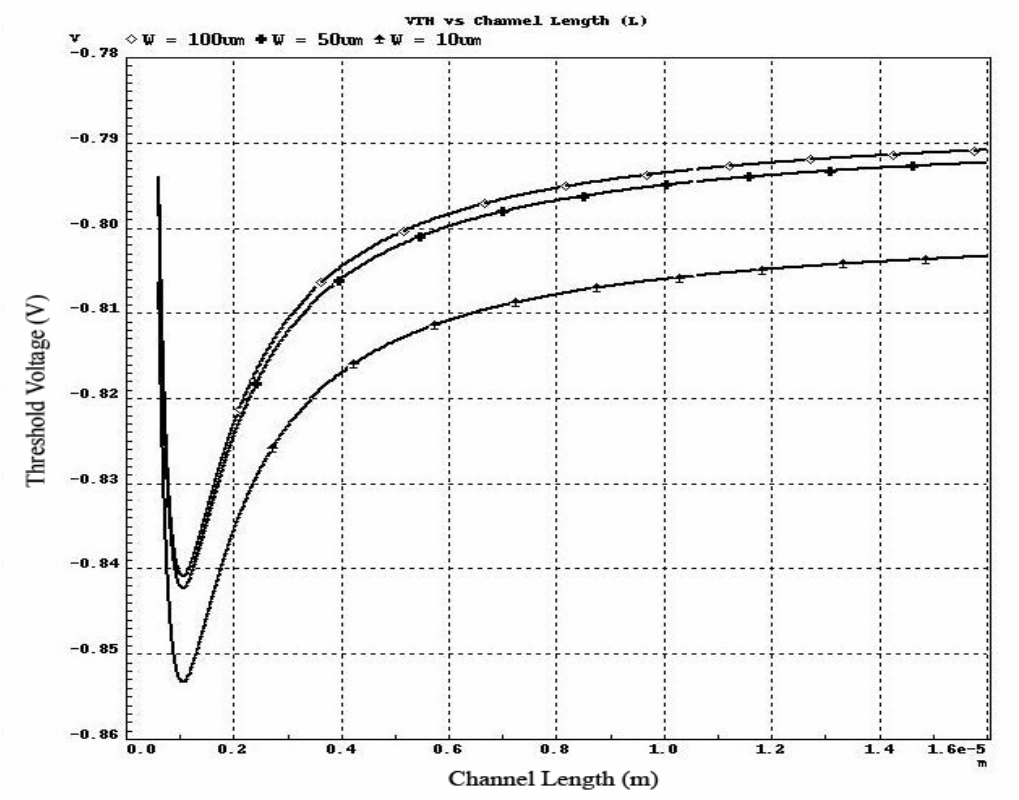


Figure 3. 2: PMOS - V_{TH} versus channel length (L), with W = 10 µm, 50 µm, and 100 µm.

In Figure 3.2, the variation of the PMOS transistor V_{TH} with channel length is illustrated. Similar to the V_{TH} drop seen in the NMOS transistor, the PMOS suffers DIBL effect at channel length less than 1 µm, causes the magnitude of V_{TH} drops quickly [28]. Unlike the NMOS transistor, the magnitude of V_{TH} does not roll-off immediately at short channel lengths. Instead it suffers reverse short channel effect (RSCE) [28]. As a result there is a peaking in the magnitude of V_{TH} as the channel length decreases to around 1 µm. Since PMOS transistors are marginally biased in saturation region at low supply voltage of 1 V therefore the channel length has to be chosen carefully so that the variation of V_{TH} is lesser when process error comes into the picture. As indicated in Figure 3.2, the threshold voltage changes quickly once the channel length drops below 4 µm. In order to have less V_{TH} variation, it is preferable to design PMOS transistors that have channel length that are greater than 4 µm. In cases where the aspect ratio is very large, it maybe necessary to design PMOS transistors with channel length that are smaller than 4 µm, to help reduce the silicon area required. For these PMOS transistors, the channel length must still be above 1 µm as the PMOS transistors may also suffer from the sharp V_{TH} roll-off due to the short channel length effect.

II. Threshold Voltage versus Temperature Characteristic

The VRC design has to maintain a stable output reference voltage over a temperature range, for example 0°C to 100°C. With a low supply voltage, say 1 V. The changes in the MOS transistors' V_{TH} due to temperature variation may cause some of the transistors to work in the sub-threshold region. This may cause the VRC performance to be inaccurate.

To investigate the changes of V_{TH} due to temperature variations, the variation of V_{TH} due to temperature changes are derived for both the NMOS and PMOS transistors and are shown in Figures 3.3 and 3.4, respectively. The two figures are obtained through simulation using BSIM3v3, typical model.

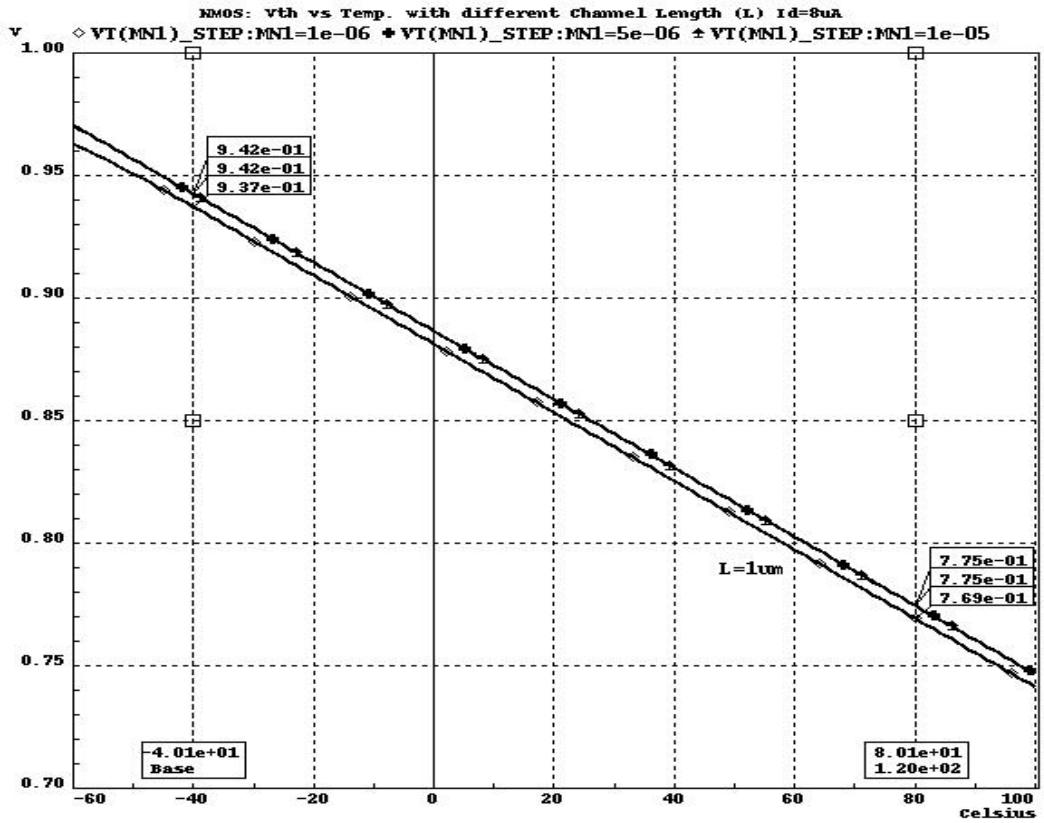


Figure 3. 3: NMOS - V_{TH} versus temperature with L = 1 µm, 5 µm, and 10 µm.

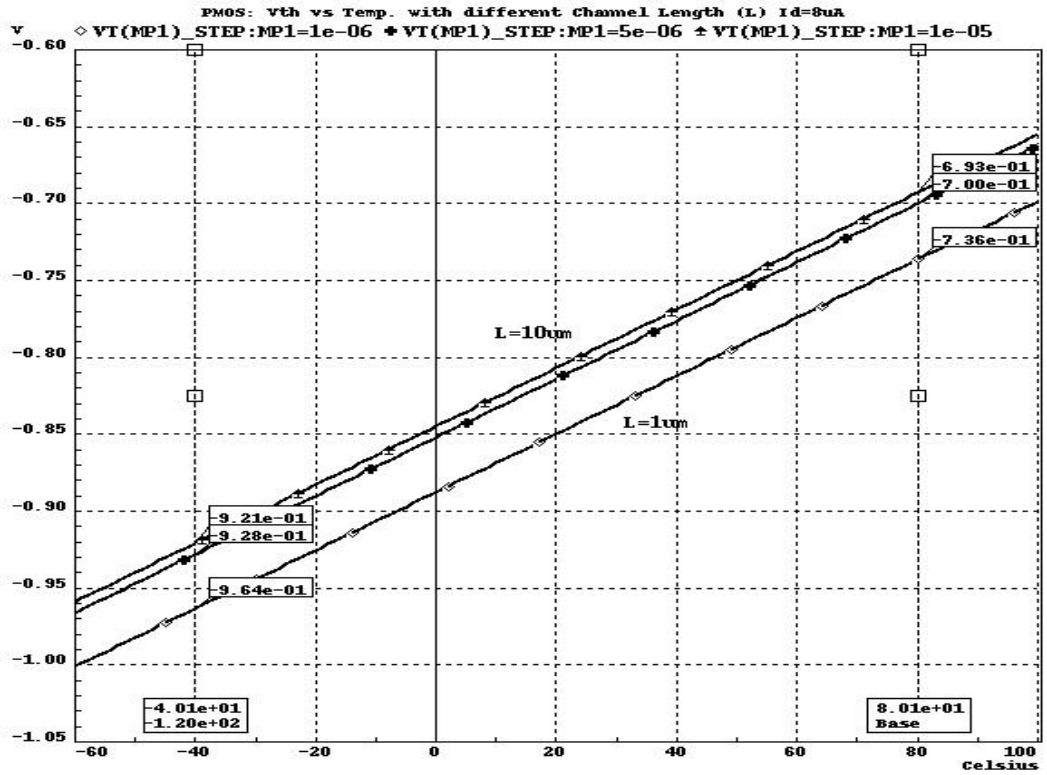


Figure 3. 4: PMOS - V_{TH} versus temperature with L = 1 µm, 5 µm, and 10 µm.

As is evident from Figure 3.2, when the temperature decreases from 85°C to -40°C, i.e., over the commercial range, the V_{TH} of the NMOS transistor increases by about 0.167 V. Similarly for the PMOS transistor, V_{TH} increases by about 0.228 V. To illustrate the changes better, the variations for both the NMOS and PMOS transistors can be derived from Figures 3.3 and 3.4 through simple linear equations. Shown in Equations (3.1) and (3.2) are the threshold voltages as a function of temperature for both the NMOS and PMOS, respectively.

$$V_{TH,N} = -1.4 \times 10^{-3} T + 0.88 \tag{3.1}$$

$$V_{TH,P} = 1.9 \times 10^{-3} T - 0.89 \tag{3.2}$$

With limited voltage headroom, it is predicted that the VRC will not function accurately when the temperature drop due to some of the transistors move into the sub-threshold region. To limit this effect, the VRC will be designed to operate in the range 0°C to 100°C. The design of the VRC will consider the V_{TH} to be at its maximum at 0°C.

3.2.2 Bipolar Junction Transistor Characteristic

Bipolar junction transistors (BJTs) are desirable to generate the PTAT and CTAT currents. As mentioned earlier in Section 2.1.2, the BJT presents in the CMOS n-well process is the parasitic PNP transistor, which is the vertical transistor, used in the VRC design.

The common-emitter current gain, β, changes as the collector current, I_C, changes. The change in β may cause inaccuracies in the current generating circuit. Thus, the BJTs need to be biased at a point with minimum β variation when the I_C changes.

In Figure 3.5, β variation is small when I_C increases from 10 nA to 10 µA. Thus, a suitable I_C can be chosen from this region to provide a proper biasing. As show in Figure 3.6, this I_C region is also suitable for use when temperature changes since β remains relatively constant.

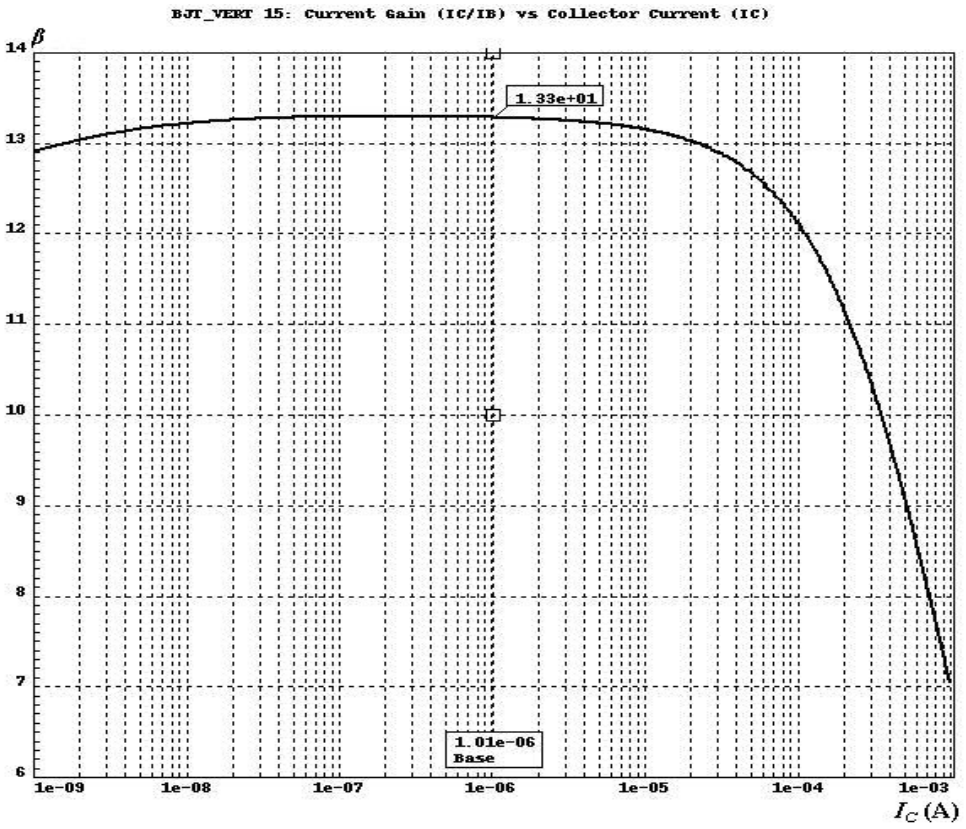


Figure 3. 5: β versus collector current (I_C) of vertical BJT.

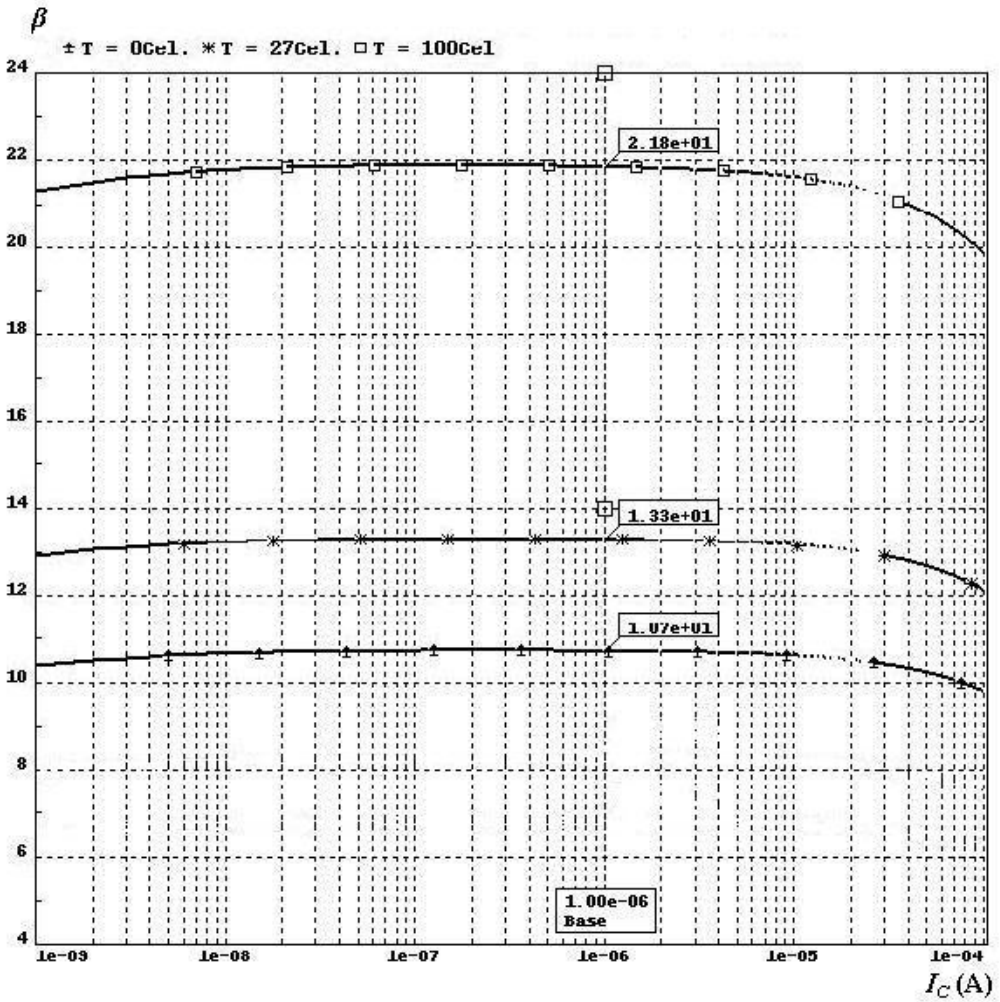


Figure 3. 6: β versus I_C with temperature of 0°C, 27°C, and 100°C.

The biasing condition for the other transistors in the circuit can be determined once the emitter-base voltage, V_{EB}, of the PNP transistor is known. In this design of the VRC, a current of 1 µA is chosen to bias the PNP transistor. Figure 3.7 illustrates a plot of V_{EB} versus I_C. As can be seen, at 1 µA the V_{EB} is 0.592 V. By applying equation (2.6) $\partial V_{BE}/\partial T \approx$ -2.2 mV/°K can be obtained.

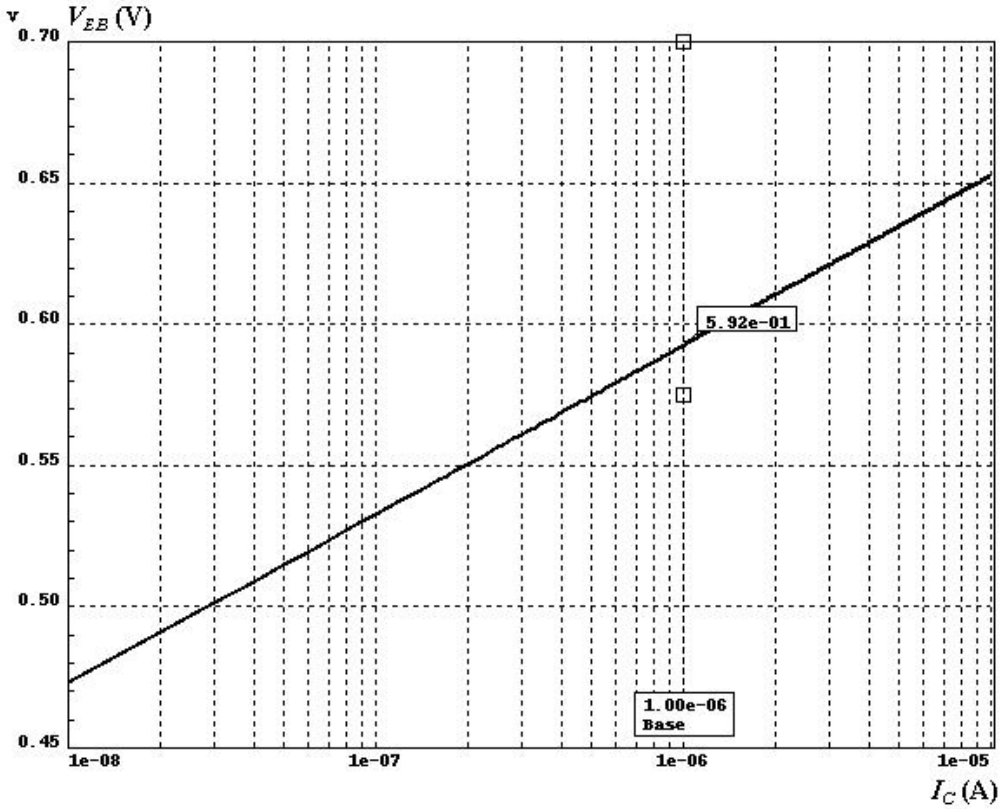


Figure 3. 7: V_{EB} versus I_C of vertical BJT.

3.3 Proposed Voltage Reference Circuit [17]

A voltage reference circuit has been design and shown in Figure 3.8 is the overall proposed design. It consists of: (1) PTAT and CTAT current generating circuits that together can create the zero *TC* current (also known as voltage reference core circuit), (2) a low voltage operational amplifier for providing the feedback control to the voltage reference circuit, and (3) a current mirror constructed by self-cascode composite transistors that aims to improve the *PSRR* performance and the accuracy of mirroring. More detail description of the circuit's operation is provided in the following sub-sections.

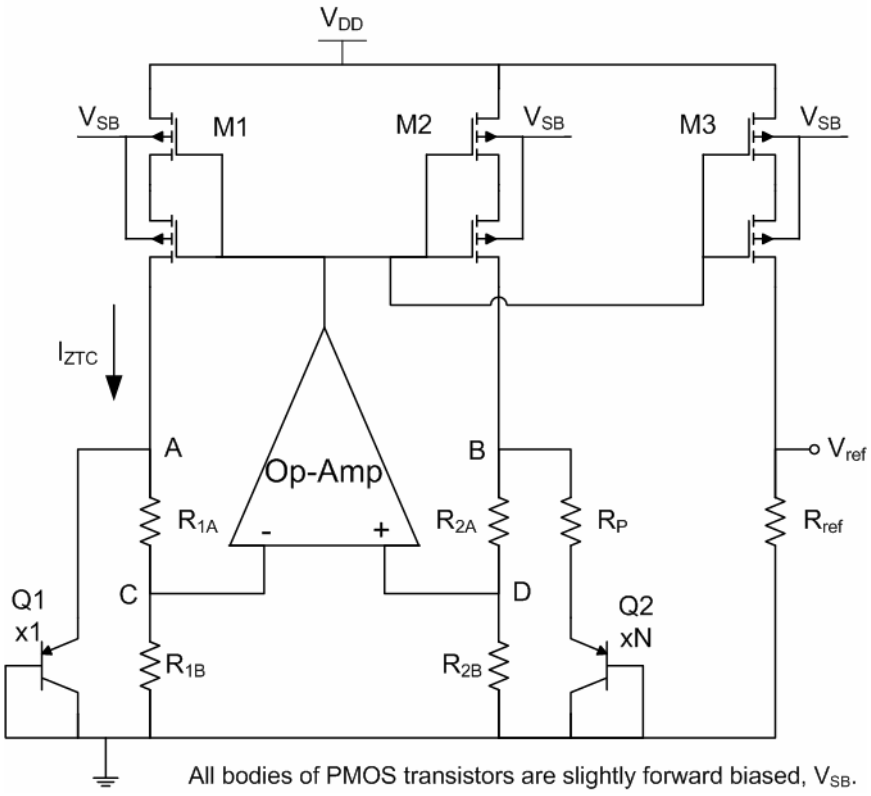


Figure 3. 8: Overall voltage reference circuit design.

3.3.1 Voltage Reference Core Circuit

Due to process constraint the parasitic PNP transistors available in the CMOS process for our proposed design have to be engaged for the generation of PTAT and CTAT currents. In the design of VRC, amplifier with PMOS transistor input

stage is used. In order to ensure the PMOS transistors operating within the common-mode input range, the two terminals of the amplifier are connected to nodes C and D instead of nodes A and B (see Figure 3.8). The existing of amplifier enforces nodes C and D to have equal potential. By setting $R_{1A} = R_{2A}$ and $R_{1B} = R_{2B}$, nodes A and B will be able to achieve the same potential. Therefore, a loop formed by Q1, R_{1A}, R_{2A}, R_P, and Q2 generates a current given by

$$I_{ZTC} = \frac{V_{EB,Q1}}{R_1} + \frac{V_T \times \ln(N)}{R_P} \tag{3.3}$$

where N is the emitter area ratio, and $R_{1,2} = R_{1A} + R_{1B} = R_{2A} + R_{2B}$. The current I established by the current mirror, formed by M1, M2 and M3, is injected to R_{ref}, forming the reference voltage V_{ref}, where

$$V_{ref} = \frac{R_{ref}}{R_{1,2}}\left[V_{EB,Q1} + \left(\frac{R_{1,2}}{R_P}\ln N\right)V_T\right] \tag{3.4}$$

From the above equation, the value of R_P, $R_{1,2}$ and N can be found by differentiating V_{ref} with respect to temperature, and then setting it to zero.

$$\frac{\partial V_{ref}}{\partial T} = \frac{R_{ref}}{R_{1,2}} \times \frac{\partial V_{EB,Q1}}{\partial T} + \frac{\ln N}{R_P} \times \frac{\partial V_T}{\partial T} = 0 \tag{3.5}$$

Since $(\partial V_T/\partial T) = k/q \approx 0.087$ mV/°C and $(\partial V_{EB}/\partial T) \approx -2.2$ mV/°C, by substituting these values into Equation (3.5), the resistors ratio,

$$\frac{R_{1,2}}{R_P} = \frac{25.29}{\ln N} \tag{3.6}$$

For better matching of PNP transistors as well as to suppress the effect of op-amp's offset voltage, it is better to have a big emitter ratio, N. In this design, N is chosen to be 24 due to die area constraint. Hence, the ratio between $R_{1,2}$ and R_P becomes 7.958.

To obtain the values of $R_{1,2}$ and R_P, Equation (3.3) is used. As such, it is necessary to set the branch current. As mentioned before, I_{PTAT} is set to 1 µA, which is within the constant β value shown in Figure 3.6. By setting I_{ZTC} = 2 µA and substituting $R_{1,2}/R_P = 7.958$ into Equation (3.4), the resistance values for $R_{1,2}$ and R_P are calculated to be 625.3 kΩ and 78.6 kΩ, respectively, under room temperature, in which $V_T \approx 26$ mV and $V_{EB} \approx 0.593$ V (see Figure 3.7). Due to the non-ideal effect, these values are initial figures to be used in the iteration before the exactly values are obtained.

Due to the high resistance values, the high resistivity polycrystalline silicon resistor (RPOLYH), which owns the highest sheet resistance of 1.2 kΩ is available in AMS 0.6 µm CMOS process, is employed in the implementation to keep the resistors' area as small as possible. Shown in Equation (3.7) is the relationship between the resistance, length, and width of RPOLYH.

$$R = 1200 \times \frac{L}{W - 0.1} \tag{3.7}$$

where R is the required resistance in ohms, L and W are the length and width of the RPOLYH resistance in micro meter (µm), respectively.

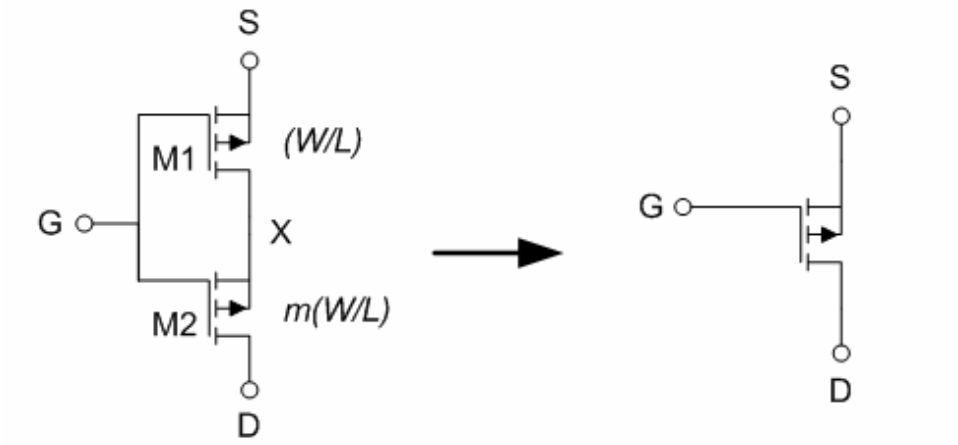
To minimize the length of the resistor, the minimum width of 5 µm, specified by the AMS 0.6 µm CMOS process is chosen. The length of the resistors therefore can be calculated accordingly.

3.3.2 Self-cascode Composite Transistor

A better accuracy of current mirroring and *PSRR* performance can be achieved through the use of conventional cascode transistor [10]. However, the higher operating voltage of a regular cascode transistor is a major drawback and is not suitable for low voltage applications. For that reason, the self-cascode composite

PMOS transistor, reported by *C. Galup-Montoro* [27] is introduced in the proposed VRC design (see Figure 3.8).

Depicted in Figure 3.9 is a self-cascode composite PMOS transistor, which can be equivalent to a single transistor. The working principle of the composite transistor is discussed in the following paragraphs.



(a). Self-cascode composite PMOS transistor (b). Equivalent transistor

Figure 3. 9: PMOS composite transistor.

For the composite transistor to function properly, both M1 and M2 should satisfy the following conditions respectively:

$$V_S - V_G - \left|V_{TH,P}\right| > 0 \tag{3.8}$$

$$V_X - V_G - \left|V_{TH,P}\right| > 0 \tag{3.9}$$

By adding each side of Equation (3.9) with a "-V_S" term, Equation (3.10) can be rewritten as follows [see Equation (3.10)].

$$V_S - V_X < V_S - V_G - \left|V_{TH,P}\right| = V_{SD,(SAT)} \tag{3.10}$$

From the above equation, it can be deduced that transistor M1 must be operating in the linear region, whereas transistor M2 can work either in the saturation or in the linear region depends on the drain voltage, V_D. For the composite transistor to be

operating in the saturation mode, transistor M2 must be in saturation as well. Hence, currents for the two transistors can be expressed as,

$$I_1 = \beta_1 \left(V_{SG} - \left|V_{TH,P}\right| - \frac{1}{2} V_{SX} \right) V_{SX} \tag{3.11}$$

$$I_1 = \frac{1}{2} \beta_2 \left(V_{SX} - V_{SG} - \left|V_{TH,P}\right| \right)^2 \tag{3.12}$$

Solving the current equations, Equation (3.13) can be obtained,

$$I_1 = \frac{1}{2} \frac{\beta_1 \beta_2}{\beta_1 + \beta_2} \left(V_{SG} - \left|V_{TH,P}\right| \right)^2 = \frac{1}{2} \beta_{eq} \left(V_{SG} - \left|V_{TH,P}\right| \right)^2 \tag{3.13}$$

where $\beta_1 = \mu_p C_{ox}(W/L)$ and $\beta_2 = \mu_p C_{ox} * m * (W/L)$. Thus, β_2 can be further expressed as,

$$\beta_{eq} = \frac{m}{m+1} \beta_1 = \frac{1}{m+1} \beta_2 \tag{3.14}$$

Because PMOS transistor M2 works in saturation region while transistor M1 always operates in linear region. The source-to-drain voltage of M1, $V_{SD,M1}$, is so small that there is no discernable $V_{SD,(SAT)}$ difference in both the composite and simple transistors (see Equation (3.14)). This explains why self-cascode structure can be fitted adequately in low voltage regime.

$$V_{SD,(SAT)-eq} = V_{SD,(SAT)-M2} + V_{SD-M1} = V_{SD,(SAT)-M2} + I_{D2} R_{M1} \tag{3.15}$$

where $R_{M1} = \dfrac{1}{\mu_p C_{ox} (W/L) \left(V_{SG} - \left|V_{TH,P}\right| \right)}$.

Other than offering low operating voltage, the structure is able to deliver higher equivalent output impedance as compare to a single transistor. The output

resistance, r_o, can be derived through small signal analysis of the self-cascode composite transistor [27], whereby

$$r_o = g_{m2}r_2r_1 - r_2 - r_1 \approx \left(g_{m2}r_1 - 1\right)r_2 = \left(mg_{m1}r_1 - 1\right)r_2 = \left(m - 1\right)r_2 \qquad (3.16)$$

Assuming the output resistance (r_1) of M1 that operates in linear region is much smaller than the output resistance (r_2) of M2, which operates in saturation region.

3.3.3 Low Voltage Gain Enhancement Amplifier

Op-amp is one of the critical components in the VRC design. It forces nodes C and D of the VRC core (refer to Figure 3.8) to be the same by forming feedback loops from the amplifier output to its inputs.

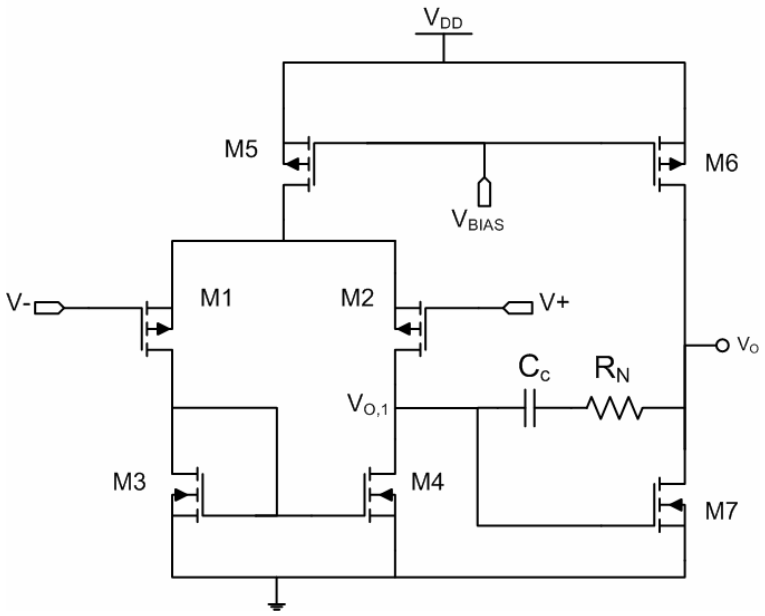


Figure 3. 10 Conventional op-amp.

Due to the common mode voltage requirement of VRC discussed in Section 3.3.1, the VRC can only accommodate amplifier with PMOS input stage. Therefore, PMOS input stage is selected in the proposed op-amp design. In order to minimize the input offset voltage of the amplifier, a balanced configuration has to be employed in the input stage. For the conventional PMOS input stage shown in Figure 3.10, the source-drain voltage of the input transistor M2 is dependent on the

output voltage or the voltage at the input of the next stage. Such unbalanced structure brings several problems, such as large input offset voltage and a reduced dynamic range. Whereas the structurally balanced configuration of Figure 3.11 offers an improved input offset voltage since the source-drain voltage of the input transistors (M9 and M10) are almost the same. The drawback of the amplifier is the greater number of transistors needed and a higher current consumption since there are more branches from V_{DD} to ground. Nevertheless, it can be noted that this extra current is in the order of a few microamperes. Hence, the advantages of this configuration out weights the problems and worthwhile to be implemented.

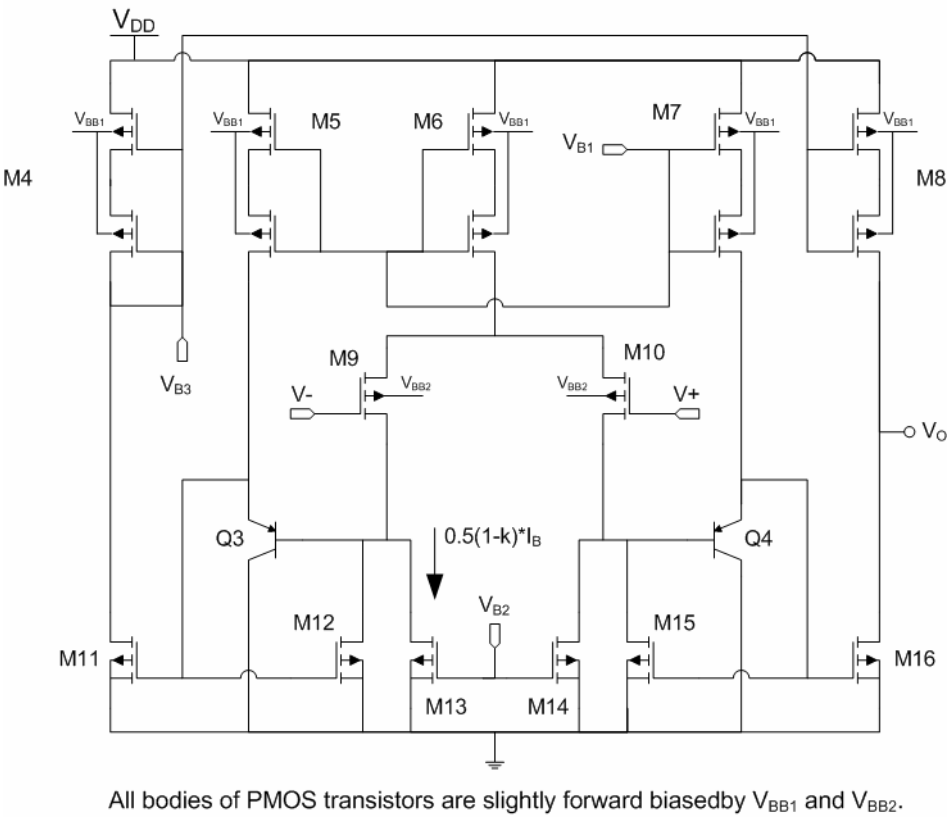


Figure 3. 11 Gain enhancement amplifier.

In order to ensure that the low voltage amplifier can function properly, a dc level-shifting current mirror [17] must be used. The circuit presented in Figure 3.12(a) is part of the amplifier shown in Figure 3.11 without dc level-shifting current mirror. Assuming $V_{SG,M9} \approx V_{GS,M12}$ for $|V_{TH,P}| \approx V_{TH,N}$. The source-drain voltage of M9, $V_{SD,M9}$, can be represented by:

$$V_{SD,M9} = (V-) + V_{SG,M9} - V_{GS,M12} \approx (V-) \tag{3.17}$$

Under circumstances such as when $V_{TH,N} > |V_{TH,P}|$, $V_{SD,M9}$ will be lesser than V-. This may caused the transistor M9 to operate in the triode region if the input voltage $(V-) = \left[R_{1B}/(R_{1A}+R_{1B})\right] \times V_{EB,Q1}$ is less than the saturation voltage.

By adding a dc level-shifting current mirror using the parasitic vertical BJT transistor of Figure 3.12(b), the problem resolved. The source-drain voltage of M9 is now given by:

$$V'_{SD,M9} = (V-) + V_{SG,M9} + V_{EB,Q3} - V_{GS,M12} \tag{3.18}$$

This ensures that M9 always operate in the saturation region even when (V-) = 0 V, providing that $V_{TH,N}$ is not greater than $|V_{TH,P}|$ by more than 0.6 V

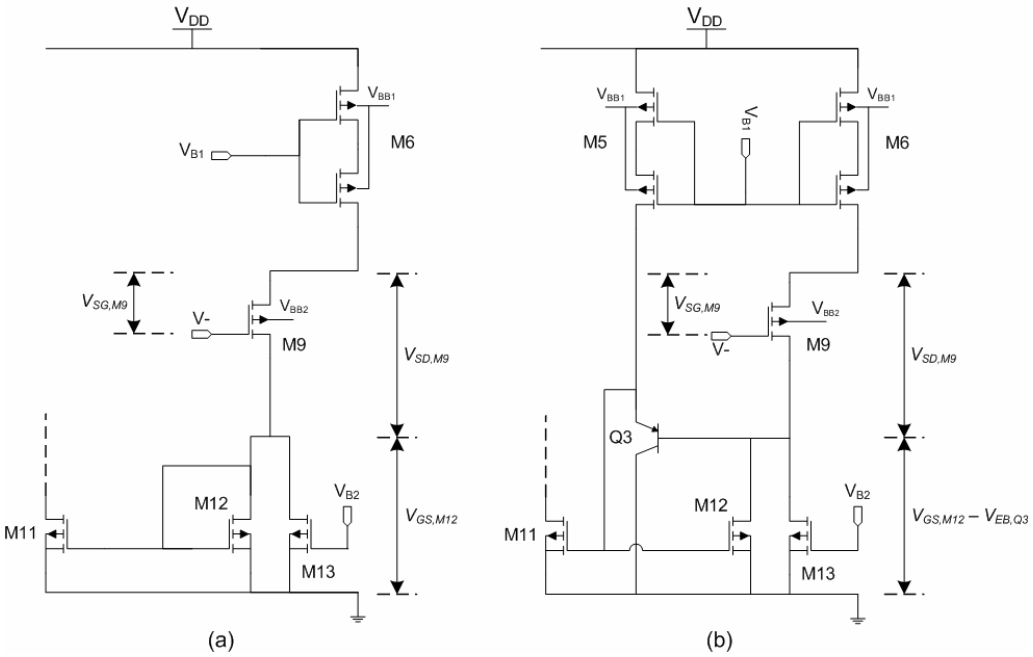


Figure 3. 12 Current mirror in amplifier. (a) Without dc level-shifting (b) With dc level-shifting.

Back to Figure 3.11, two NMOS transistors (M13 and M14) are introduced and placed in parallel to transistors M12 and M15 respectively, to form a gain enhancement amplifier. Such configuration will divide the current from input

transistor (M9 and M10) into two, causing smaller current flow through transistors M12 and M15. By letting the current mirror ratios of M11 to M12, M15 to M16, and M4 to M8 equal to 1, the overall voltage gain increases and can be approximated using the following equation:

$$A_v = g_{m,M9} \times \frac{R_{o,M16//M8}}{2} \tag{3.19}$$

where $g_{m,M9}$ is the transconductance of transistor M9 and $R_{o,M16//M8}$ is the output impedance of the amplifier. Assuming M16 and M8 have the same output impedance. The equation can be further deduced and described by:

$$A_v = \sqrt{\mu_p C_{OX} \left(\frac{W}{L}\right)_{M9} I_B} \left(\frac{1}{\lambda k I_B}\right) = \sqrt{\frac{\mu_p C_{OX} (W/L)_{M9}}{I_B}} \times \frac{1}{\lambda k} \tag{3.20}$$

where I_B is the biasing current of M6, λ is the channel modulation parameter and $0 < k < 1$. Keeping other parameters as constant, small value of k helps to increase the voltage gain of the amplifier. However, it is expected the -3 dB bandwidth of the amplifier will be smaller when compare to one that is without gain enhancement feature. This is because the gain enhancement amplifier is realized through the increase of impedance.

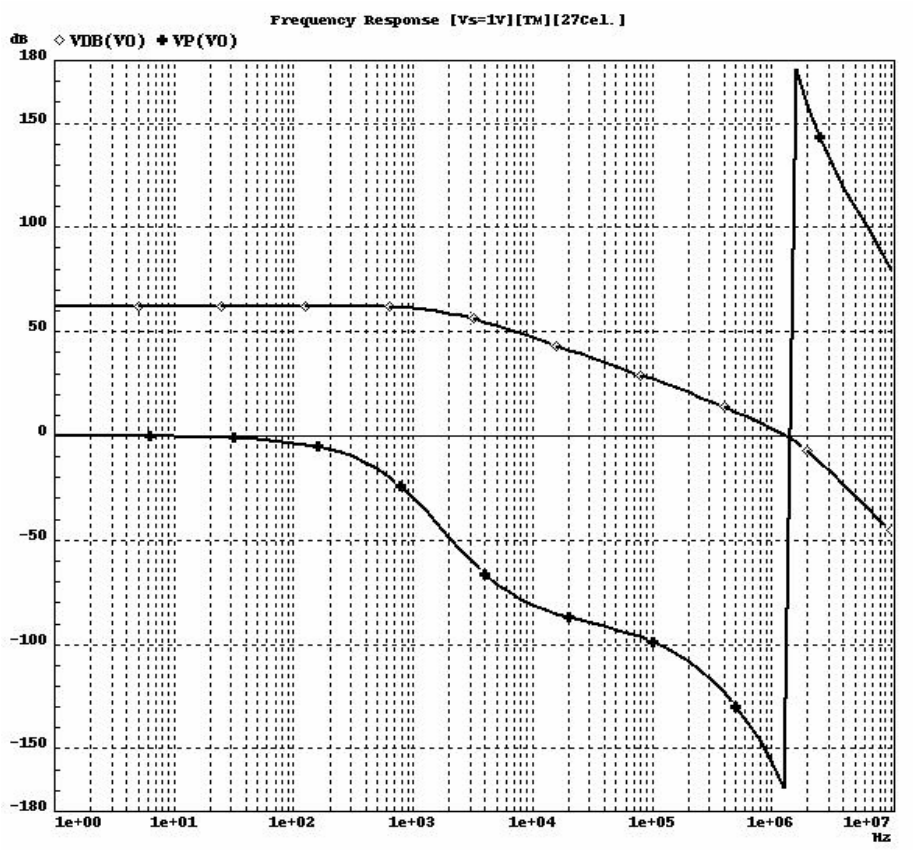


Figure 3. 13 Frequency response of the amplifier.

The amplifier needs to be simulated individually in order to investigate its performance. Figure 3.13 shows the gain and frequency response of the low voltage amplifier with common-mode input voltage of 0.15 V. Since the output of the amplifier in the VRC drives only the gates of few PMOS transistors, the amplifier is simulated with a capacitance loading of 2 pF. The simulation result indicates that the amplifier has a gain of 62.3 dB, a gain bandwidth product of 1.5 MHz, and a phase margin of 39°.

3.3.4 Bulk-Source Junction Biasing (Body Biasing) of PMOS

The standard CMOS AMS 0.6 µm, n-well process used in the implementation of the proposed design has threshold voltages, V_{TH}, of -0.8 V for the PMOS transistor and 0.85 V for the NMOS transistor, at room temperature. This relatively high V_{TH} is a bottleneck when the supply voltage goes below 1 V. Because of the negative temperature dependency of V_{TH}, the circuit can easily shut down or malfunction under cold condition. To eliminate such fragility, V_{TH} has to be brought down by

method of slightly forward biasing the source-bulk junction of the PMOS transistors. The relationship between V_{TH} and source-bulk voltage, V_{SB}, described by [28] is shown below:

$$\left|V_{TH,P}\right| = \left|V_{TH,P0}\right| + \gamma\left(\sqrt{2|\phi_F| - V_{SB}} - \sqrt{2|\phi_F|}\right) \tag{3.21}$$

where $|V_{TH,P0}|$ is the threshold voltage of PMOS transistor (with zero biased source-bulk voltage), γ is the body bias coefficient, and $|\phi_F|$ is the bulk Fermi potential.

Two temperature independent voltages are created in the circuit (see Figure 3.14): voltage V_{BB2} is used to slightly forward bias the source-bulk junction of the amplifier PMOS input transistors, M9 and M10, whereas the remaining PMOS transistors are biased through V_{BB1} (refer to Figure 3.14 for details). To avoid turning "on" of the p-n junction between the p-diffusion and n-well, in the source to bulk voltage, V_{SB}, of each PMOS transistor is kept below 0.4 V across the temperature range of interest.

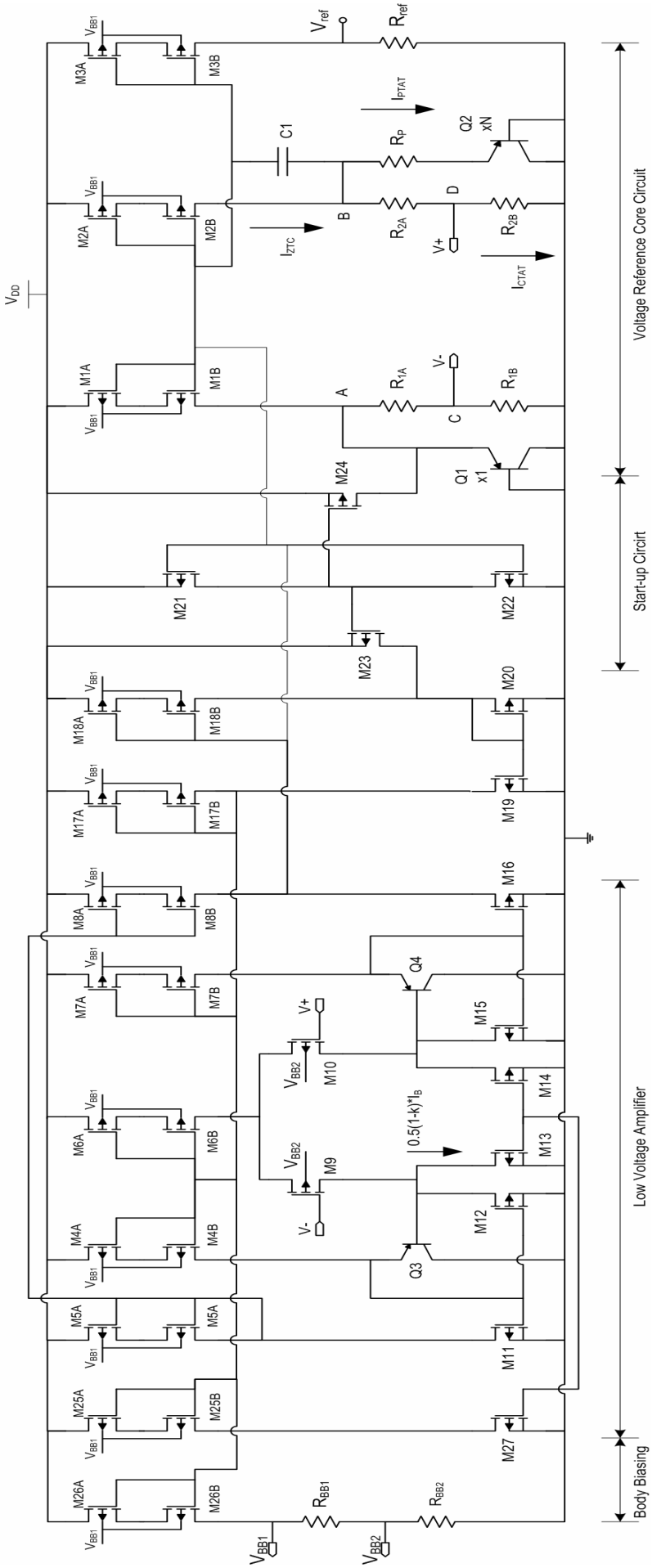


Figure 3. 14 Complete schematic diagram of the voltage reference circuit.

3.4 Results

The 1.0 V voltage reference circuit of Figure 3.14 was successfully fabricated, with a total silicon area of 0.5 mm^2. The circuit micrograph is presented in Figure 3.15. The current consumption of the circuit is around 32 µA at 1.0 V supply.

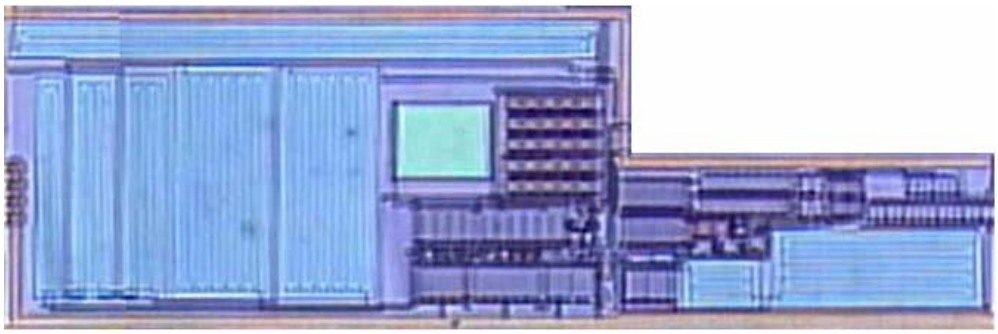


Figure 3. 15 Micrograph of the voltage reference circuit.

3.4.1 Temperature Coefficient

The optimum output voltage for minimum temperature coefficient (*TC*) in a voltage reference depends on the operating temperature range of interest. The average *TC* of a VRC is generally specified over the commercial temperature range, that is 0°C to 70°C [34] at the minimum, and maybe specified also over the industrial range of -40°C to 85°C [35]. Assuming that the output voltage versus temperature curve is symmetrical above and below the nominal reference voltage, the middle of the operating temperature range will be a temperature point where the output voltage is of a minimum *TC*. For examples, 35°C for the commercial temperature range, and 50°C for 0°C to 100°C.

The simulated temperature dependency of the VRC is analyzed in the plot of Figure 3.16. From the figure, the reference voltage obtained at 27°C for a 1.0 V supply voltage is around 600.33 mV. The calculation shows that the temperature dependency of the proposed work for the temperature range of 0°C to 100°C under 1.0 V supply voltage is 11.86 ppm/°C.

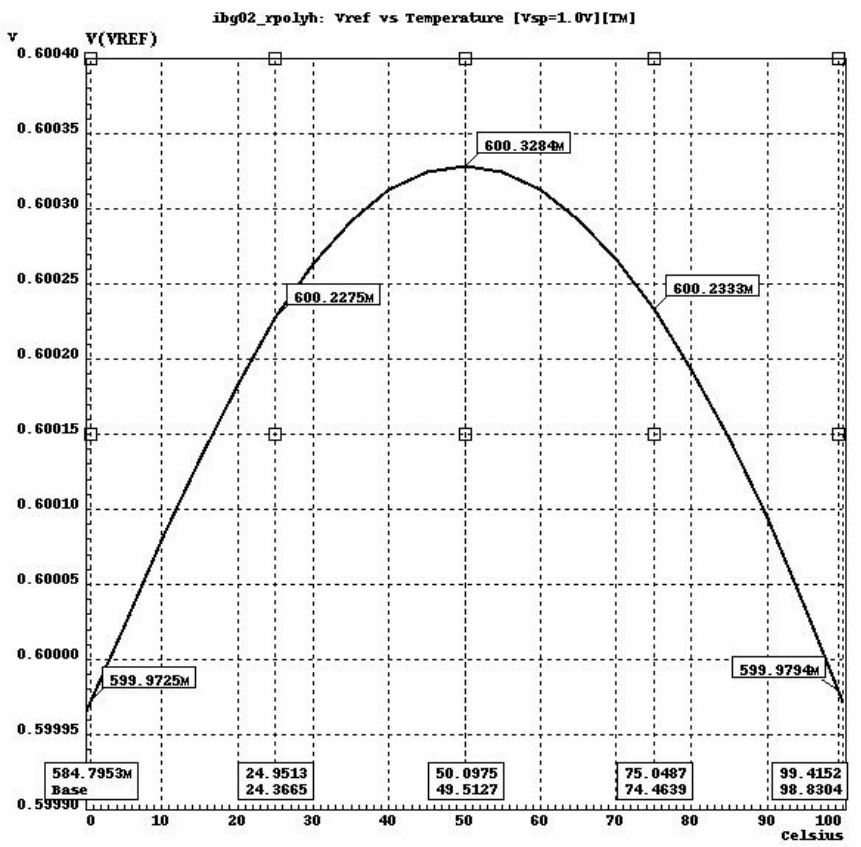


Figure 3. 16 Temperature dependency of the VRC at 1-V supply voltage.

The detail work out of the temperature coefficient is presented in the below steps:

$$TC_{(0°C\sim 50°C)} = \left(\frac{1}{600.2275} \times \frac{600.3284 - 599.9725}{50 - 0} \times 10^6 \right) \text{ppm/°C}$$

$$= 11.86 \text{ ppm/°C}$$

From the measurement, the reference voltage at 27°C under 1 V supply voltage is 549.83 mV, which is of about 50 mV deviation from the simulated one. Such deviation is due to the input offset voltage of the op-amp, current mirror and resistors mismatch. As seen in Figures 3.16 and 3.17, both the measurement and simulation results fitted quite well except at low temperature range, from 0°C to 20°C. Within this range the measured voltage points are slightly lower than what we expected. Consequently an asymmetrical concave curve is obtained instead of the symmetrical one seen in Figure 3.16. The discrepancy is due to some of the transistors operating out of the saturation region, under extreme condition of low temperature and low voltage supply. To compare with the simulation result on *TC*

performance, with data points from 0°C to 50°C, worst case condition are considered for the calculation of temperature dependency. It is revealed that the *TC* under measurement is about 30.15 ppm/°C, with a difference of 18.29 pmm/°C when compare to the simulated *TC*.

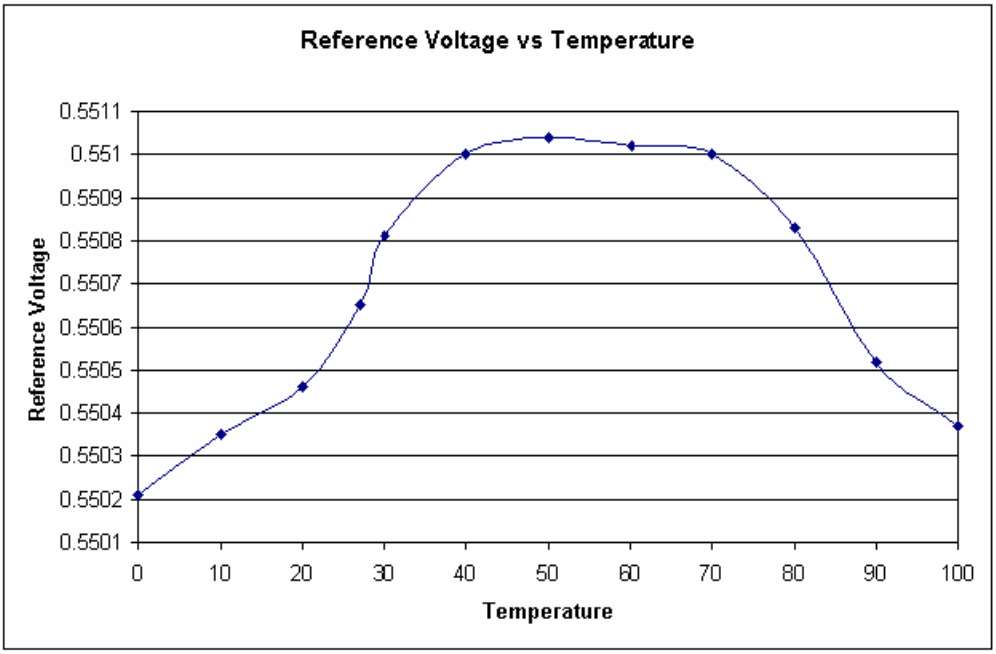


Figure 3. 17 Measured temperature coefficient of the VRC.

3.4.2 Supply Dependency

Depicted in Figure 3.18 is the simulated plot of the VRC as a function of supply voltage under room temperature condition. It can be seen that the output voltage remains almost constant from 0.9 V to 1.8 V. For supply voltage that is smaller than 0.9 V, the reference voltage begins to vary significantly from the nominal value of 0.6 V. This is because at below this range, the amplifier gain drops quickly and its systematic input offset increases drastically causing the VRC core to fail.

However, instead of 0.9 V, the measurement result projected 1 V to be the lowest operating supply voltage (see Figure 3.19). This implies that the amplifier's performance degrades earlier in the actual implementation than the simulated one.

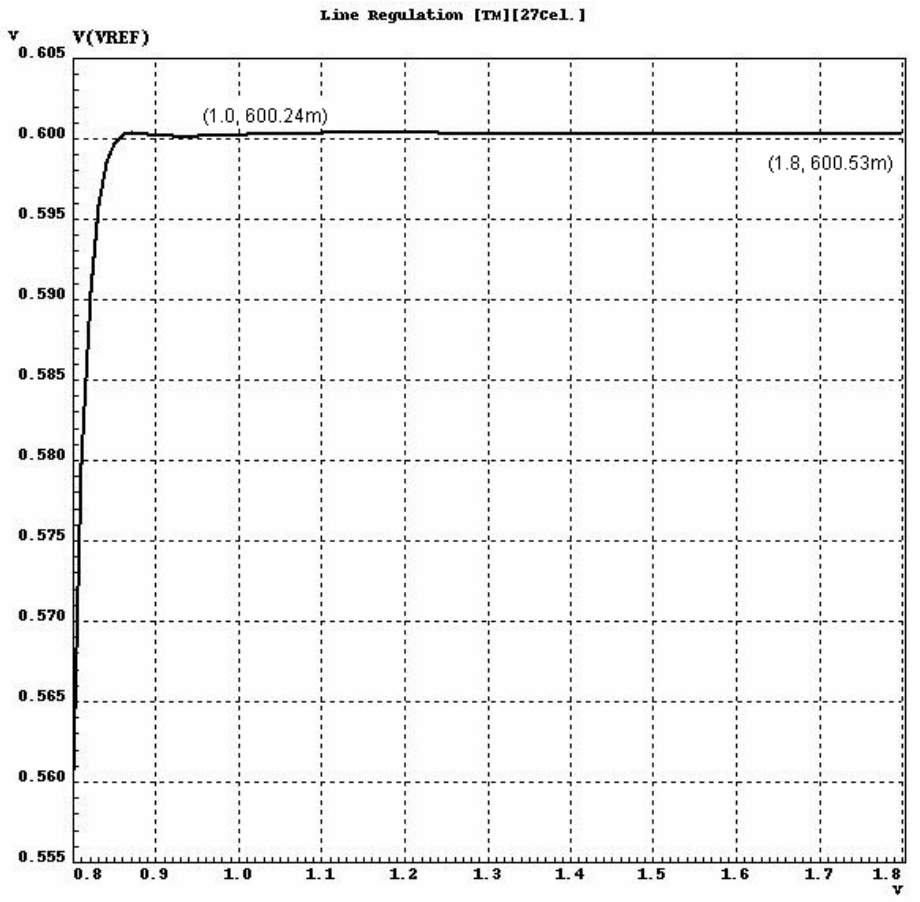


Figure 3. 18 Simulated supply dependency of VRC.

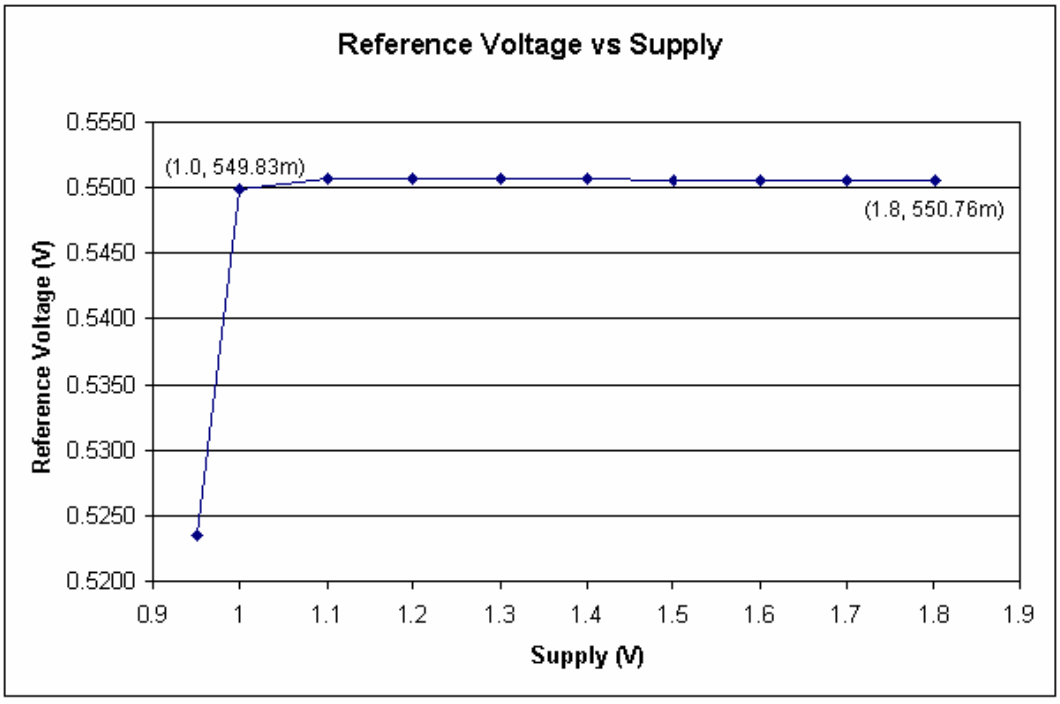


Figure 3. 19 Measured supply dependency of VRC.

3.4.3 PSRR

The *PSRR* presented in Figure 3.20 is obtained based on the typical condition, i.e., with supply voltage of 1 V and at a temperature of 27°C. For frequencies below 400 Hz, the circuit achieves *PSRR* smaller than -51 dB. Beyond 400 Hz, the *PSRR* starts to increase approximately at 20 dB/dec.

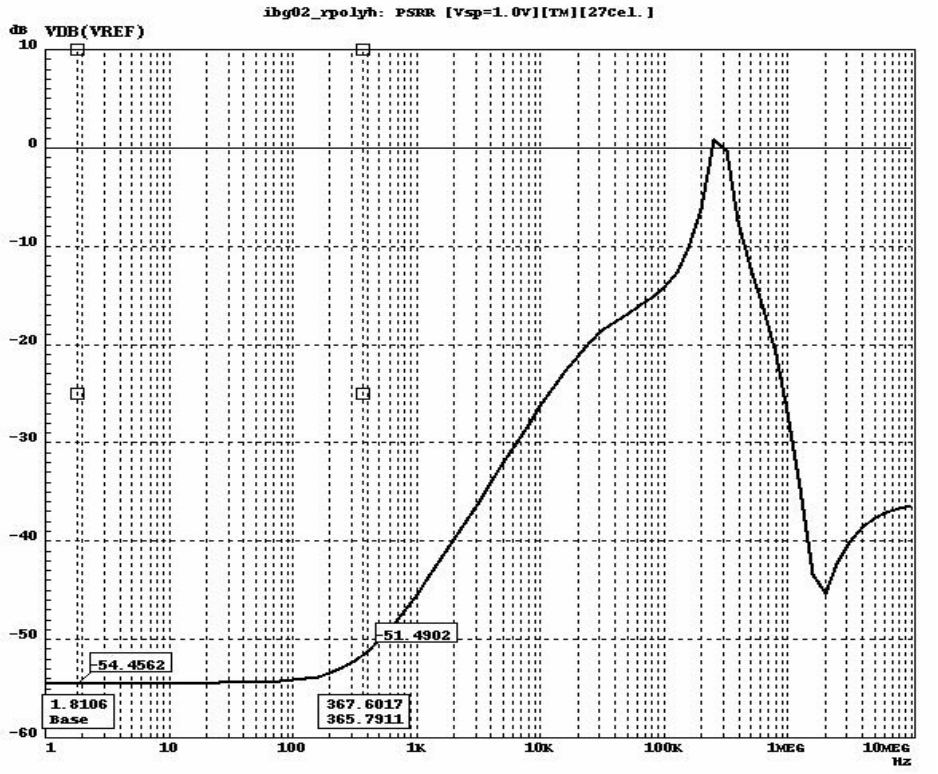


Figure 3. 20 Simulated *PSRR* of the VRC when V_{DD} = 1-V.

3.5 Summary

The VRC that operate under 1 V supply voltage has been designed, discussed and simulated. The simulated VRC achieved a *TC* of 11.86 ppm/°C and a *PSRR* of (-54.5 dB), consuming a power of 32 µW. The main feature here is that the circuit is constructed using relatively high V_{TH} devices, and operating under low supply voltages. If a lower V_{TH} is available for the design, the achievable supply can be further reduced, to less than 1 V. In this proposed VRC design, larger values of resistors are employed so that the circuit can achieve low power consumption. As a result, the design occupies a large die area.

In the actual measurement of the 1 V voltage reference circuit, instead of 0.6 V, a reference voltage of 549.83 mV is obtained. A worst case *TC* of 30.15 ppm/°C is also noted, from 0°C to 50°C. The error voltage caused by the input offset voltage of the amplifier and the mismatch of the resistors is found to be the root of such discrepancy. One way to suppress the offset voltage of the op-amp is to increase the emitter area ratio, *N*, of the VRC. Due to die area constraint in this work, a good resistors matching has to be compromised in the actual implementation. Therefore accuracy issue due to the resistors mismatch is unavoidable.

Both the simulation and measurement results are tabulated in the following table.

Table 3.1: Simulated and measured data of the 1 V VRC.

Parameters	Simulation	Measurement
Technology	AMS 0.6 µm, CMOS process	
V_{TH} (27°C)	$V_{TH,P}$ = -0.80 V, $V_{TH,N}$ = 0.85 V	
Supply voltages	0.9 V to 1.8 V	1.0 V to 1.8 V
Reference voltage, V_{ref} @ 1.0 V, 27°C	600.24 mV	549.83 mV
Supply dependency @ 27°C	0.36 mV/V	1.16 mV/V
TC (0°C ~ 100°C) @ 1 V	11.86 ppm/°C	30.15 ppm/°C

Chapter 4

A 1.2 V CMOS Voltage Reference Circuit

A low supply voltage reference circuit constructed only by MOSFETs and resistor is studied and discussed. Other than the threshold voltage reduction and sub-threshold operated transistor techniques, a resistance reduction technique is also implemented in the design. The proposed design presented in this work deployed the standard CMOS 0.5 μm, n-well process. A reference voltage of 200.46 mV is simulated at room temperature. A temperature coefficient of 64.1 ppm/°C is achieved at 1.2 V, with current consumption of 38 μA.

Cadence Spectra and Virtuaso are used for simulation and layout respectively in this design work. Unless specify, simulation results shown in this chapter are all simulated using BSIM3v3 typical models at 27°C.

4.1 Introduction

The resistive subdivision method [15], [29] solves the constraint on conventional bandgap voltage level [30] and is able to address the low supply issue to gain widespread application in state-of-the-art designs [17] [20] [21]. However, as the supply continues to reduce, the common collector structure of the parasitic vertical BJT in CMOS technology, which is commonly use to form PTAT current generator, and the input common-mode input voltage of the amplifier become a barrier in the design. The solution to the problems is to use low threshold voltage devices [15], [23] or design techniques that were proposed previously in [17], [20]. This is however achieved at extra cost, especially for the solutions reported in [15], [20], [23] because of their association with advanced CMOS technology, BiCMOS process, and DTMOST, respectively. All in all, the resistive subdivision approach reported in [17], which is a current-mode approach, provides the best solution

although more resistors are required to construct the circuit, which again translated into more die area. This situation becomes more severe if lesser current has to be consumed in the design, to fulfill low power specification or if high-poly resistor is not available in a process.

The proposed design presented in this chapter is a VRC with only MOSFETs and resistors that engage standard CMOS 0.5 µm n-well process. This modified structure provides an alternative solution for addressing the above-mentioned issues.

4.2 MOSFETs' Threshold Voltage

Since a different process is employed, there is a need to determine the behavior of threshold voltage against temperature. A NMOS threshold voltage characteristic versus temperature is depicted in Figure 4.1.

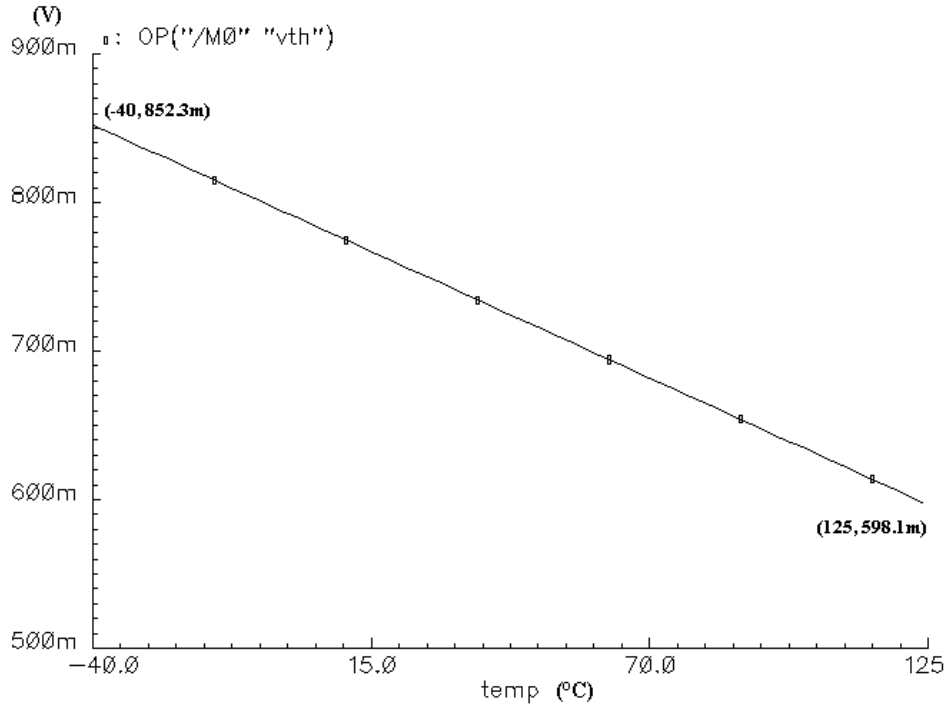


Figure 4. 1 Threshold voltage of NMOS versus temperature.

The threshold voltage of NMOS is inversely proportional to the temperature. At room temperature, the V_{TH} of NMOS is about 0.75 V. Illustrated in the figure are

the voltages at two extreme temperatures, -40°C and 125°C. With these two coordinates, the V_{TH} behavior can be formularized as follows:

$$V_{TH,N} = -1.55\times10^{-3}T + 0.79 \tag{4.1}$$

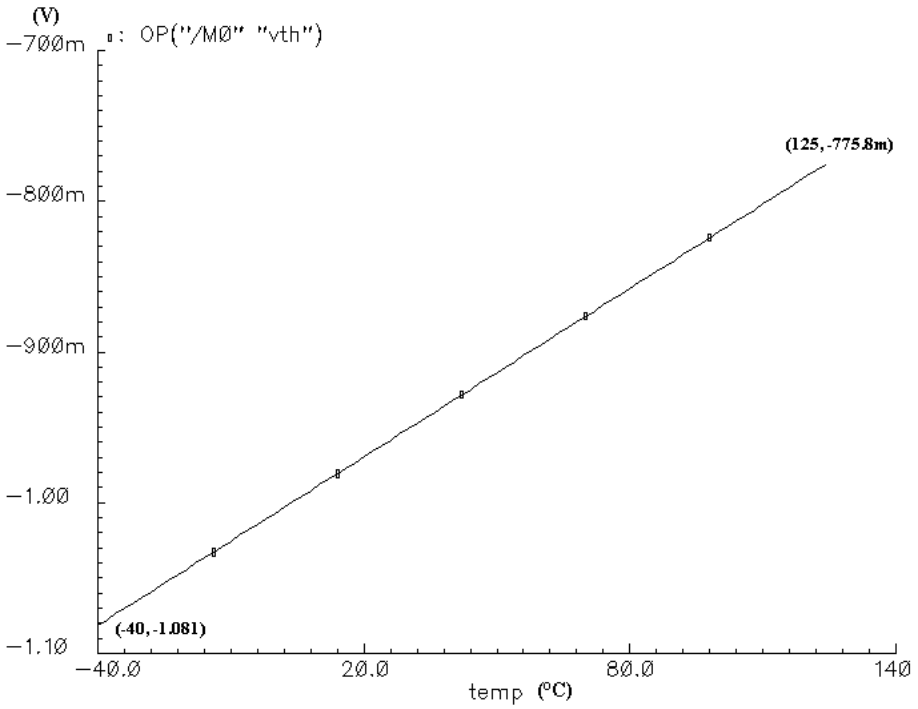


Figure 4. 2 Threshold voltage of PMOS versus temperature.

For PMOS transistor, the threshold voltage increases linearly with temperature. The voltage can hit as high as -1.081 V when temperature goes down to -40°C, see Figure 4.2. The calculated TC is 1.86×10^{-3} ppm/°C and the threshold voltage of PMOS transistor can be described through the following equation:

$$V_{TH,P} = 1.86\times10^{-3}T - 1.007 \tag{4.2}$$

Clearly it can be observed that any VRC builds on AMIS 0.5-µm process is unlikely to function over temperatures of -40°C to 125°C at supply voltage of 1 V without body biasing the transistors since the V_{TH} hits beyond 1 V at zero degree Celsius. In order to lower down the V_{TH} of PMOS transistor, body biasing technique is therefore is necessary in this work.

4.3 Proposed Voltage Reference Circuit

The low voltage VRC of Figure 4.3 provides an overview to the proposed design of this project. In the following sub-sections, detail discussions will be presented, focusing on: weak inversion of NMOS transistor, PTAT and CTAT generators which form the core circuitry of VRC, low voltage op-amp, and the body biasing circuitry. The complete circuit can be found in Figure 4.11.

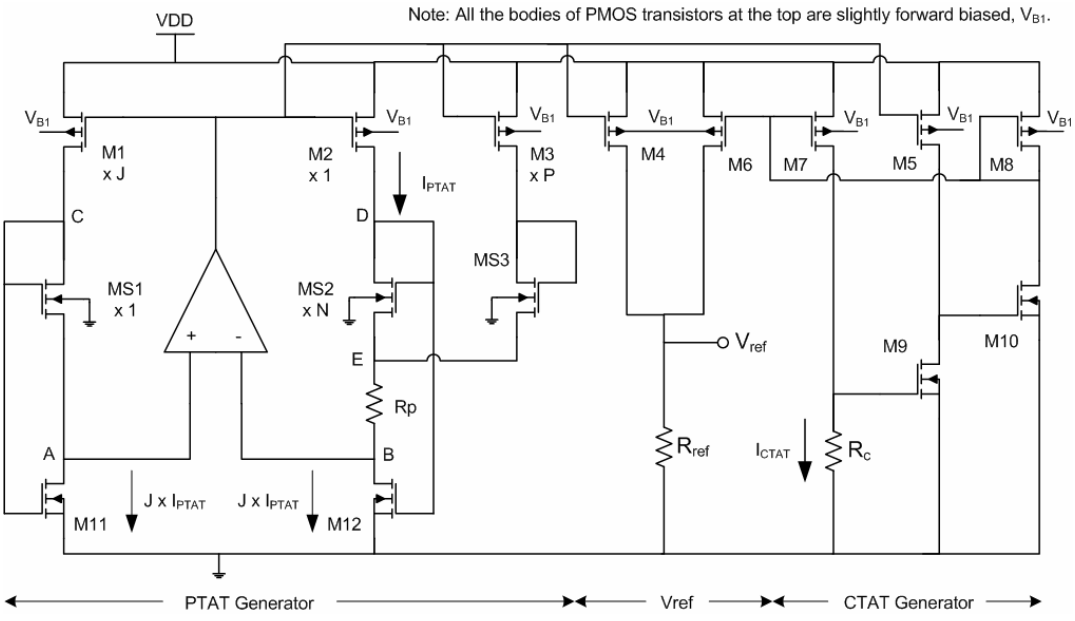


Figure 4. 3 Proposed voltage reference circuit.

4.3.1 Sub-Threshold Operated NMOS Transistor

In this work, bipolar transistor is no longer a key element for the generation of the PTAT and CTAT currents. Instead, NMOS transistor is used as a substitute, as discussed earlier in Section 2.1.2. The idea of the proposed design is to make use of the sub-threshold regime, also known as weak inversion, to operate the NMOS transistor. This permits NMOS derive characteristics that are similar to the bipolar transistor to obtain the required two currents. According to [4], the drain current of MOSFET in sub-threshold mode can be expressed by,

$$I_D = SI_{DO} e^{\left(\frac{V_G}{nV_T}\right)} \left[e^{-\left(\frac{V_S}{V_T}\right)} - e^{-\left(\frac{V_D}{V_T}\right)} \right] \tag{4.3}$$

when the following condition is satisfied,

$$I_D \leq \frac{n-1}{e^2} S \mu C_{OX} V_T^2 \tag{4.4}$$

with

$$V_D - V_S \geq 3V_T \tag{4.5}$$

where S is the geometrical shape factor of the transistor's aspect ratio, W/L; I_{DO} is the characteristic current; n is the slope factor; C_{OX} is oxide capacitance per unit area; V_G, V_D, V_S are the gate, drain and source voltages of the transistor; and V_T is the thermal voltage (= kT/q).

Back to Figure 4.3, it is a must that the NMOS transistors, MS1, MS2, MS3 and M9 operate in the sub-threshold mode. Hence, the gate-to-source voltage, V_{GS}, of the three transistors have to be lesser than $V_{TH,N}$ throughout the operating temperature range.

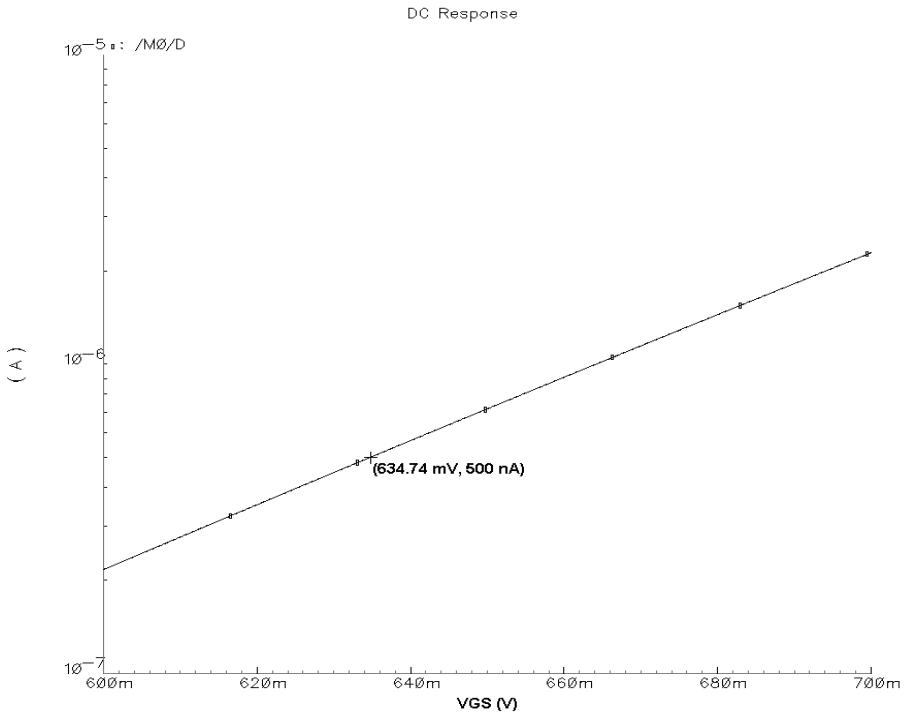


Figure 4. 4 Diode connected NMOS: I_D versus V_{GS} characteristic.

Figure 4.4 demonstrates the I_D versus V_{GS} characteristic of a sub-threshold operated diode-connected NMOS using the AMIS 0.5 µm CMOS process. A drain current of 0.5 µA is obtained with a gate-source voltage of 634.74 mV. The NMOS is chosen for use in the proposed VRC.

4.3.2 Voltage Reference Core Circuit

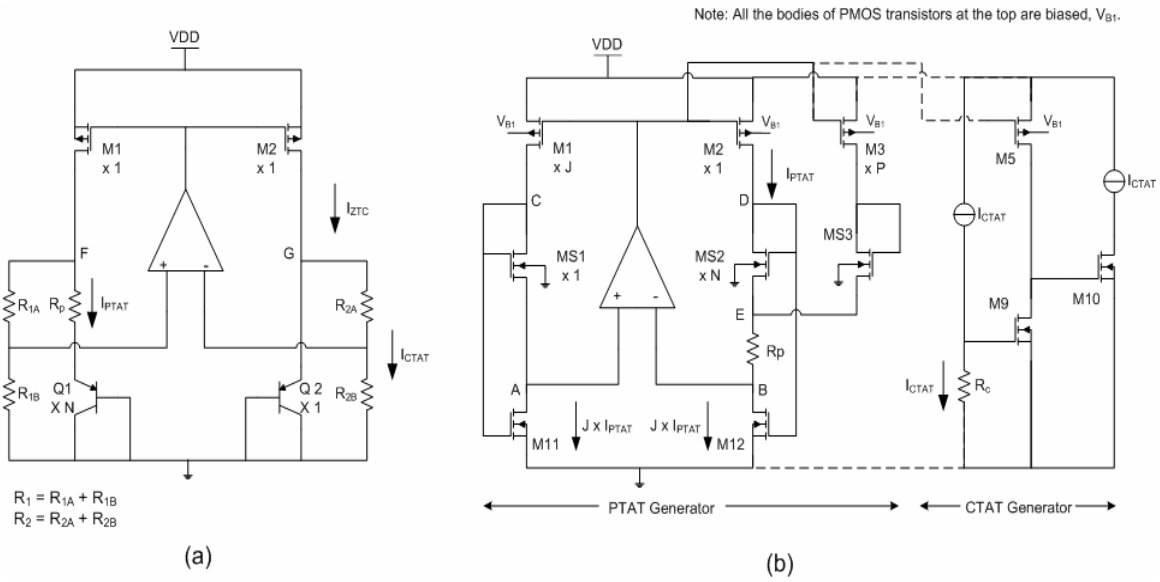


Figure 4. 5 Voltage reference core, (a) *K. N. Leung*'s work [17], (b) Proposed design.

The reference core circuit is made up of PTAT and CTAT generators as discussed earlier in Figure 4.3. When compared to the work of previous chapter, the VRC presented in this chapter separates both PTAT and CTAT generators. This is clearly illustrated in Figure 4.5.

Instead of connecting two resistors, R_1 and R_2, at node F and G, respectively, to form the CTAT component [see Figure 4.5 (a)], the CTAT now created with only one resistor, R_C [refer to Figure 4.5(b)]. Other than this, an additional branch, consists of transistors M3 and MS3, is introduced in the design. Such changes in the structure are implemented with the intention of reducing the resistor count and the resistance.

Because of the elimination of R_1 and R_2 [refer to Figure 4.5(a)] in current design, two saturation mode operated transistors M11 and M12 are placed in the core circuit. With this method, the voltage at node A and B, $V_{DS,\,M11}$ and $V_{DS,\,M12}$, can be accommodated within the input common mode range of the op-amp.

Although changes are made in the proposed design, the working principle, however, remains the same. Since NMOS has been used to replace the BJT in the core circuit, as a diode-connected sub-threshold operated NMOS transistor, the drain current can be expressed as Equation (4.3). And because of the fact that $e^{-\left(\frac{V_D}{V_T}\right)} = e^{-\left(\frac{V_G}{V_T}\right)} \ll e^{-\left(\frac{V_S}{V_T}\right)}$. Therefore $e^{-\left(\frac{V_D}{V_T}\right)}$ is ignored and the drain current is simplified as:

$$I_D = SI_{DO} e^{\left(\frac{V_G}{nV_T}\right)} e^{-\left(\frac{V_S}{V_T}\right)} \tag{4.6}$$

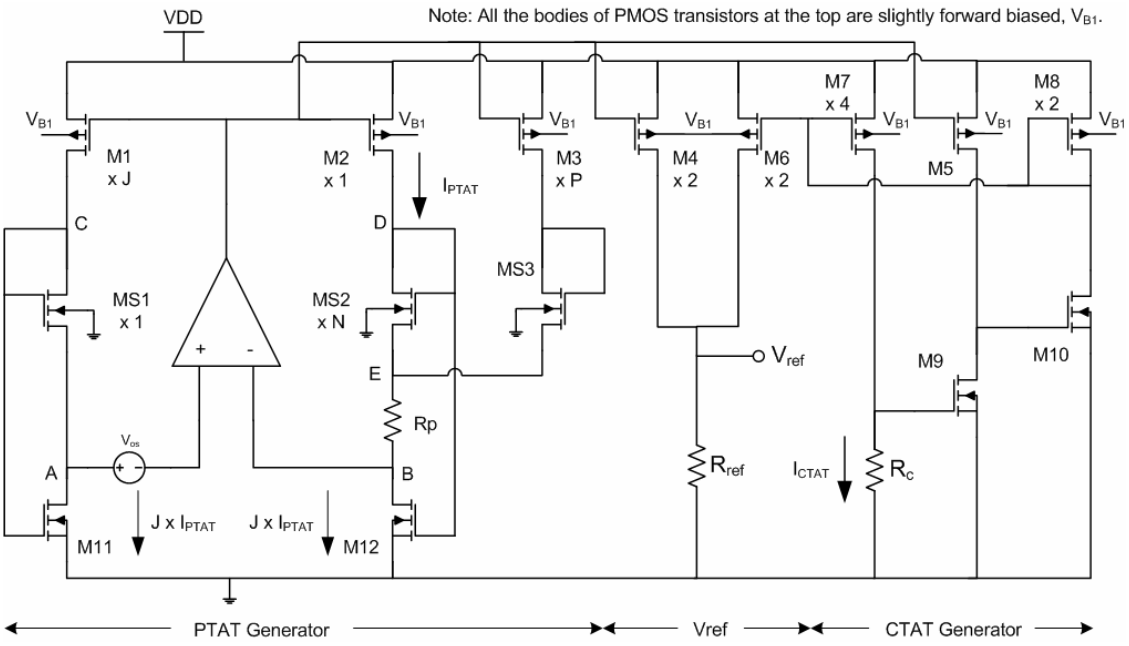


Figure 4. 6 Proposed voltage reference circuit with offset voltage effect.

By considering the effect of op-amp's offset voltage, the VRC circuit is now illustrated in Figure 4.6. And the positive temperature dependent current, I_{PTAT}, can be derived. Letting the aspect ratio of transistor M11 and M12 be the same, the drain currents of M1 and M2 can be expressed as:

$$I_{D,M1} = I_{D,MS1} = S_{MS1} I_{DO} e^{\left(\frac{V_{G,MS1}}{nV_T}\right)} e^{-\left(\frac{V_A}{V_T}\right)} \tag{4.7}$$

$$I_{D,M2} = I_{D,MS2} = S_{MS2} I_{DO} e^{\left(\frac{V_{G,MS2}}{nV_T}\right)} e^{-\left(\frac{V_E}{V_T}\right)} \tag{4.8}$$

By finding the ratio of Equations (4.7) and (4.8),

$$\frac{I_{D,MS1}}{I_{D,MS2}} = \frac{S_{MS1} I_{DO} e^{\left(\frac{V_{G,MS1}}{nV_T}\right)} e^{-\left(\frac{V_A}{V_T}\right)}}{S_{MS2} I_{DO} e^{\left(\frac{V_{G,MS2}}{nV_T}\right)} e^{-\left(\frac{V_E}{V_T}\right)}} \tag{4.9}$$

From Figure 4.6, the drain current relationship of M1 and M2 maybe determined, whereby:

$$I_{D,M1} = J \times I_{D,M2} \tag{4.10}$$

Since the aspect ratio of M11 and M12 are the same, and both are biased with the same current, the gate voltages of the transistors will be equal. That is $V_C = V_D = V_{G,MS1} = V_{G,MS2}$. Equation (4.9) can therefore be simplified as:

$$J = \frac{S_{MS1} \times e^{-\left(\frac{V_A}{V_T}\right)}}{S_{MS2} \times e^{-\left(\frac{V_E}{V_T}\right)}} \tag{4.11}$$

where $S_{MS1} = (W/L)_{MS1}$, $S_{MS2} = N(W/L)_{MS1}$.

$$\ln\left(J \times N\right) = \ln\left[e^{\left(\frac{V_E - V_A}{V_T}\right)}\right] = \frac{V_{EB} - V_{OS}}{V_T} \tag{4.12}$$

Substitute $V_{EB} = (1+P)I_{PTAT} \times R_P$ and re-arranging Equation (4.12),

$$I_{PTAT} = \frac{1}{(1+P)R_P} \times V_T \times \ln\left(J \times N\right) + V_{OS} \tag{4.13}$$

On the other hands, the negative temperature dependent current, I_{CTAT}, is created [33]:

$$I_{CTAT} = \frac{V_{GS,M9}}{R_C} \tag{4.14}$$

where $V_{GS,M9} \approx 0.634$ V in this design.

From Figure 4.6, the summation of the two current is:

$$I_{ref} = \frac{2}{\left(1+P\right)R_P} V_T \left[\ln\left(J \times N\right) + V_{OS}\right] + \frac{V_{GS,M9}}{2R_C} \tag{4.15}$$

And the reference voltage is a result of the summation of two currents passing through a resistor, R_{ref}, is:

$$V_{ref} = R_{ref}\left\{\frac{2}{(1+P)R_P}V_T\left[\ln(J\times N)+V_{OS}\right]+\frac{V_{GS,M9}}{2R_C}\right\} \qquad (4.16)$$

From Equation 4.16, the temperature effect of resistors can be easily cancelled out as long as the same resistor type is employed in the design. This is because the resistance is used in ratio form. However, the effect of op-amp's offset voltage remains a problem to be solved in this work. Instead of suppressing the offset voltage effect by increasing the area, *N*, of the diode-connected transistor that was reported in [17], a PTAT current that is of *J* times larger is mirrored from M2 to M1 [3] to create the same offset voltage suppressing effect (as [17]), and consuming lesser die area. The unfortunate consequence here is that the current consumption has to be compromised.

As mentioned before, the additional branch constructed by M3 and MS3 serves the purpose of reducing the resistance of R_P. By injecting a current of $P\times I_{PTAT}$ at node E through this newly created branch, the resistance of R_P can be cut down by $(1+P)$ times, see Equation (4.16). In fact same target can be achieved without additional branch form by M3 and MS3 is needed. The drawback is that a larger current will be needed to mirror to transistor M1 in order to obtain the same offset voltage suppression effect for the overall accuracy of the reference circuit.

To further illustrate the idea, I_{PTAT} be 0.5 µA and *J*, the current factor, to be 3. The current consumption by M1 is 1.5 µA. To ensure that M11 and M12 are having the same biasing condition, $I_{DS,\,M11}$ must equal to $I_{DS,\,M12}$. Hence, the condition shown below has to be fulfilled:

$$J = 1+P \qquad (4.17)$$

Using Equation (4.17), current factor, P, is found to be 2 and the current needed will be 1 µA. The total current consumption in PTAT generator therefore is 3 µA.

In the design of reference circuit, current I_{PTAT} is set to be 0.5 µA, J = 3, P = 2, N = 8 and the designed reference voltage, V_{ref}, is 0.2 V. To determine the value of resistors, R_P, R_C and R_{ref}, the differentiation of V_{ref} in Equation (4.16) with respect to temperature, T, has to be equaled to zero.

$$\frac{\partial V_{ref}}{\partial T} = \frac{2 \times \ln(J \times N)}{(1+P) R_P} \times \frac{\partial V_T}{\partial T} + \frac{1}{2R_C} \times \frac{\partial V_{GS,M9}}{\partial T} = 0 \tag{4.18}$$

where $\partial V_T / \partial T$ = 0.087 mV/°C and $\partial V_{GS,M9} / \partial T \approx$ -1.55 mV/°C. By substituting all the values into Equation (4.18), the relationship between R_P and R_C becomes:

$$\frac{R_C}{R_P} = 4.2045 \tag{4.19}$$

For the ease of calculation, the offset voltage in Equation (4.13) is ignored. Hence resistor R_P is found to be 55.09 kΩ. With Equations (4.15) and (4.16), the calculated R_C and R_{ref} are therefore 231.61 kΩ and 84.28 kΩ, respectively.

The values of R_P, R_C and R_{ref} only provide a good starting point for the iteration process to find the actual resistances needed. This is because the method shown above does not consider the non-ideal effect of op-amp, such as finite gain and the input offset voltage of an actual op-amp.

Due to the high resistance values, the high resistance poly resistor (Hi-R Poly) will be use in the implementation as it has the highest sheet resistance of 1 kΩ available in the AMIS 0.5 µm process.

4.3.3 Low Voltage Op-Amp

A conventional two-stage op-amp [14] is commonly used in many designs. Shown in Figure 4.7 is the low voltage op-amp employed in this work. The op-amp is biased using a simple current mirror from the core circuit.

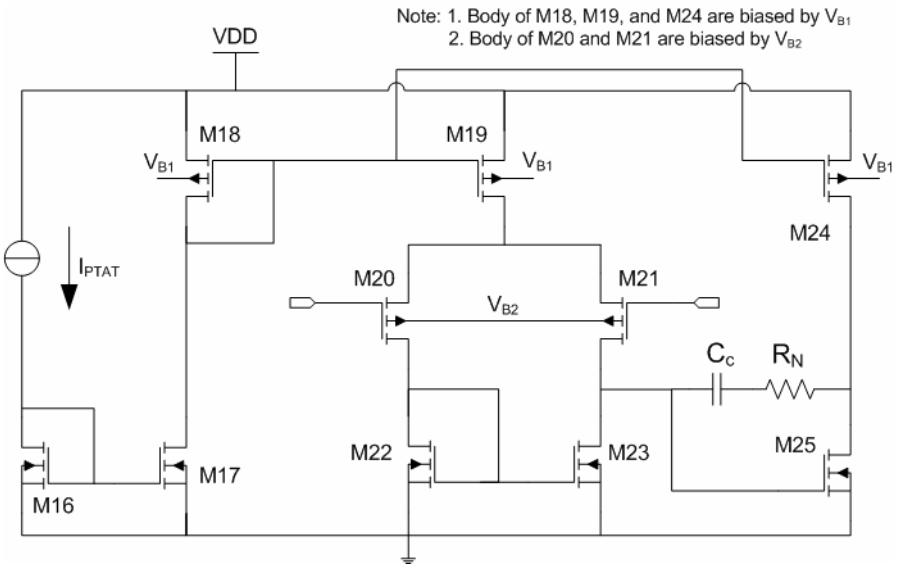


Figure 4. 7 Conventional two-stage op-amp with low supply voltage.

Note that the bodies of PMOS transistors are biased through two externally created voltages, namely V_{B1} and V_{B2}. This is to lower down the threshold voltage of PMOS transistor so that the op-amp can be ensured to operate under a supply voltage of 1.2 V. The details will be discussed on the following sub-section.

Before the op-amp can be used, its frequency response must be compensated so that its phase margin preferably is greater than 45° over the temperature of interest so that it can remain stable at the extreme circumstances. Figure 4.8 presents the gain and frequency response of the low voltage op-amp, loaded with a 4 pF capacitance, after frequency compensation using Miller capacitor, C_C, of 10 pF and a nulling resistor, R_N, of 10 kΩ.

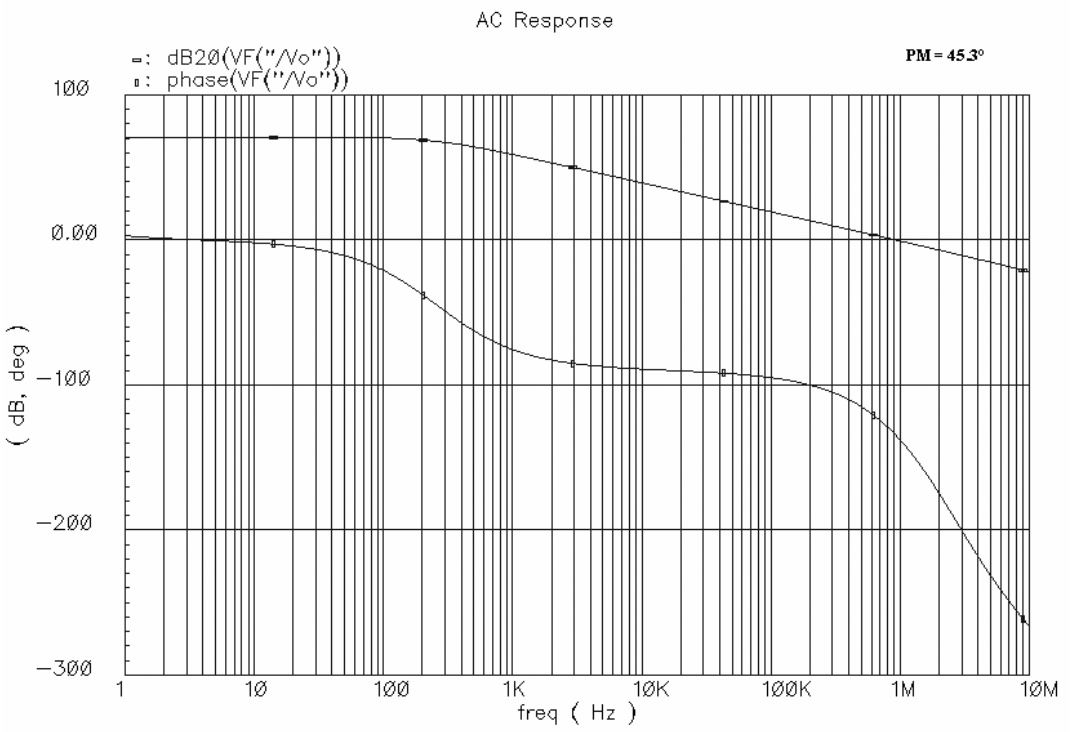


Figure 4. 8 Frequency response of op-amp.

As seen in Figure 4.8, the phase margin of the op-amp is about 45.3° after employing the Mirror compensation.

By referring to Figures 4.6 and 4.7, the minimum supply voltage, $V_{DD,\,MIN}$, of the voltage reference circuit is determined by $V_{DS,M11}$ (or $V_{DS,M12}$), $V_{GS,\,M21}$ (or $V_{GS,M20}$), and $|V_{GS,\,M19}|$. Since transistors M11, M12, M20, M21 and M19 are operating in saturation mode; the minimum supply voltage can be described using the following equation:

$$V_{DD(MIN)} = \left|V_{TH,P}\right| + 3\left|V_{DS(SAT)}\right| \tag{4.20}$$

4.3.4 Source-Bulk Junction Biasing Circuit

The standard CMOS AMIS 0.5 µm, n-well process used in the implementation of the proposed design has threshold voltages, V_{TH}, of -0.96 V for PMOS transistor and 0.74 V for NMOS transistor at room temperature. This relatively high V_{TH} is a bottleneck when the supply voltage goes to 1.2 V or below. Because of the

negative temperature dependency of V_{TH}, the circuit can easily shut down or malfunction under cold condition. To eliminate such fragility, V_{TH} has to be brought down by the method of forward biasing the source to bulk of the PMOS transistor. The relationship between the source-bulk voltage, V_{SB}, and threshold voltage is described by Equation 3.22.

Forward biasing the source (p^+ diffusion) to bulk (n-well) terminals of the PMOS transistor means to turn on p-n junction across these two terminals. This will allow a leakage current to flow from source to bulk and consequence will induce unwanted effects to the circuit. In order the keep the leakage current small and yet achieve a smaller threshold voltage, the forward bias voltage has to be small, at below 0.4 V. Calculation shown that the threshold voltage drops to 0.869 V after its V_{SB} is biased to 0.4 V.

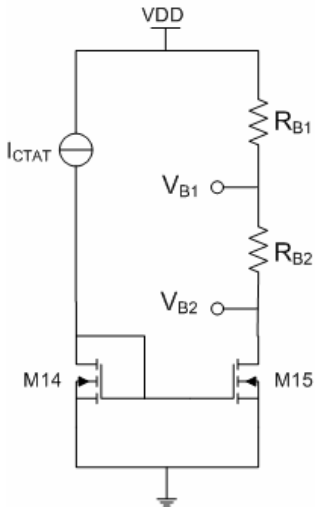


Figure 4. 9 Source-bulk junction biasing circuit.

Depicted in Figure 4.9 is the source-bulk junction biasing circuit used in the VRC circuit. Voltage V_{B1} is used to slightly forward bias the bulk terminal of the op-amp input transistor, whereas the remaining bulk terminals of PMOS transistors are biased through V_{B1}. In the design of V_{B1} and V_{B2}, the power supply variation has to be considered. In order to not to turn on the source-bulk junction completely as the supply voltage increases, V_{B1} and V_{B2} have to increase accordingly with supply voltage so that the voltages different between V_{DD} and V_{B1}, and between V_{DD} and V_{B2} remain constant throughout the supply voltage of interest (1.2 V to 1.9 V). Here, voltage V_{B1} is designed to be 0.3 V lower than the supply voltage, which

means $V_{SB1} = V_{DD} - V_{B1} = 0.3$ V. For the PMOS transistors of the input stage of op-amp, the bulk voltage, V_{B2}, are about 0.4 V lower than the source voltage. Figure 4.10 is the simulated V_{B1} and V_{B2} against supply voltage changes.

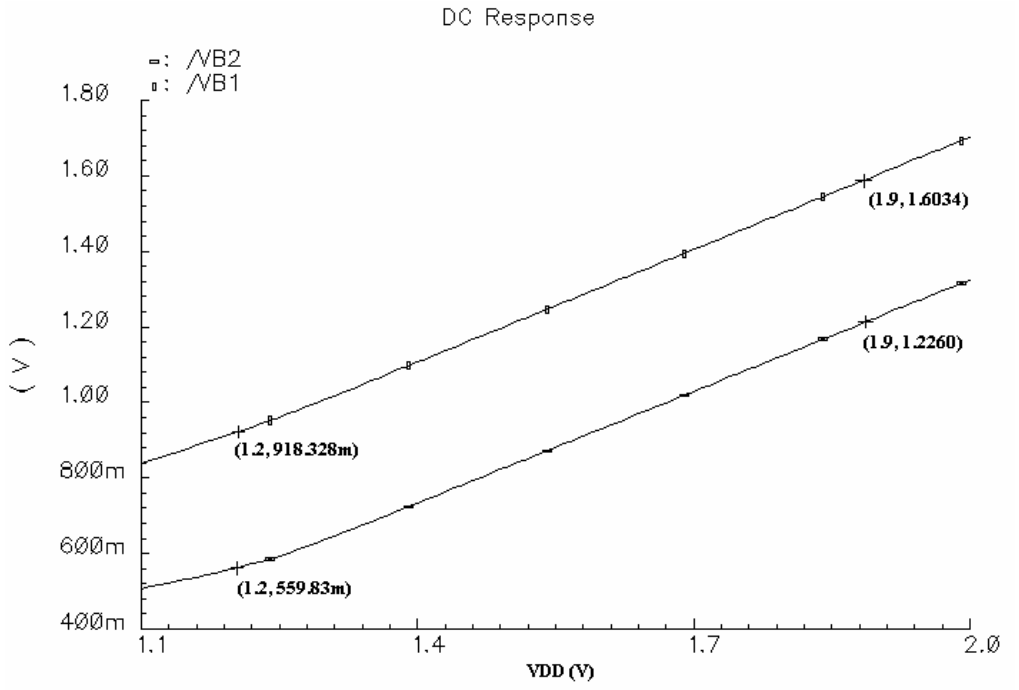


Figure 4. 10 V_{B1}, V_{B2} versus supply voltage.

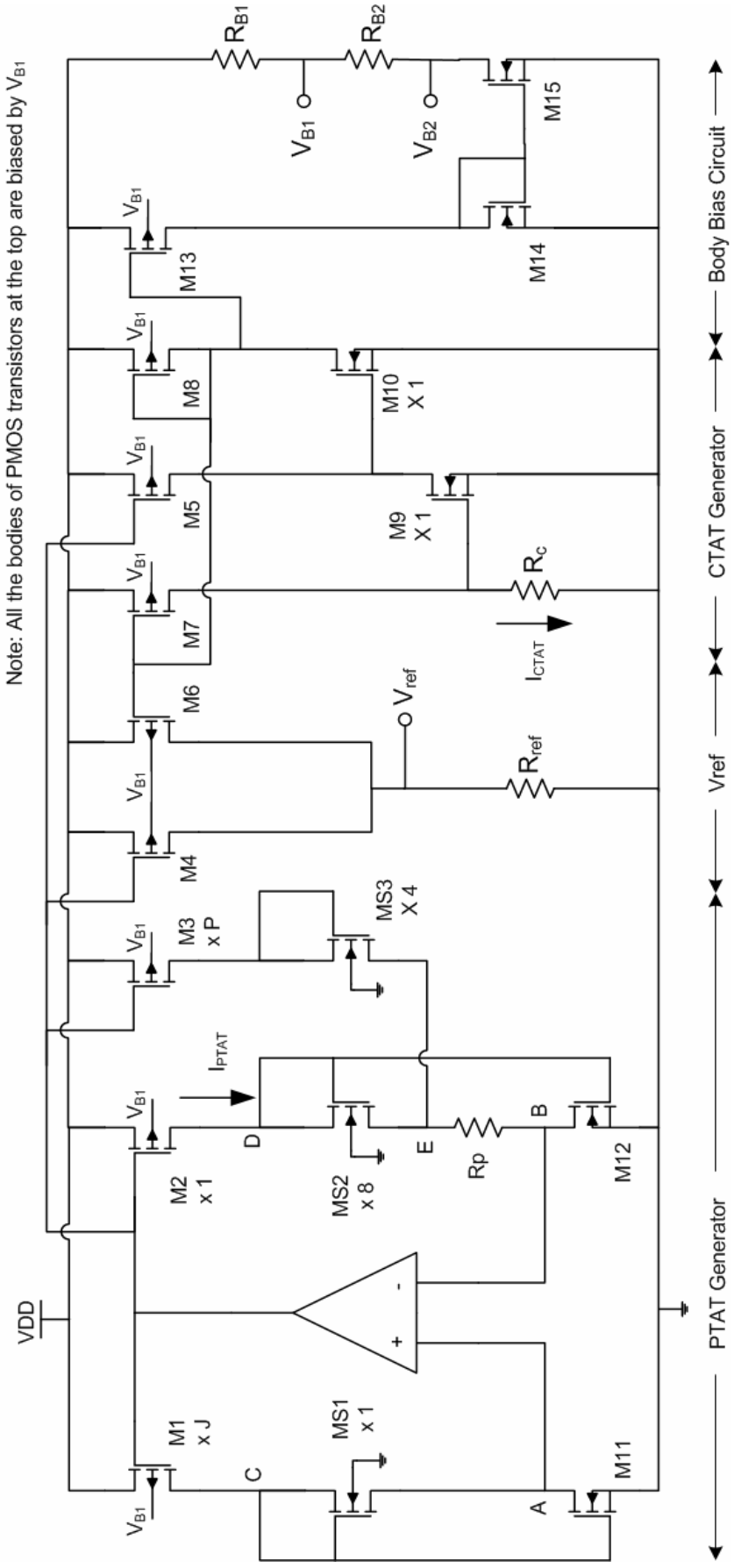


Figure 4. 11 Complete schematic of the proposed voltage reference circuit.

4.4 Layout

The layout of the VRC employs analog layout techniques such as inter-digitized, common-centroid, and other matching rules, to minimize the effect of practical layout problems that come from microscopic fluctuations in dimensions, dopings, oxide thickness, process biases, contact resistances, non-uniform current flow, diffusion interactions, mechanical stress, temperature gradients, and a host of other causes [31].

In this section, the layout of the sub-threshold operated NMOS transistor is addressed specifically. Refer to Figure 4.11, there are total number of fifteen sub-threshold operated NMOS transistor. Due to the large aspect ratio of the NMOS transistor, W/L = 60 μm/1 μm, it is hard to match all the transistors using the layout techniques [34] mentioned in the previous paragraph. Shown in Figure 4.12 is the layout of the sub-threshold operated NMOS transistor. By applying this layout, not only the matching of these NMOS transistors can be done easily, it also helps to reduce the parasitic capacitance due to the sharing of drain and source area.

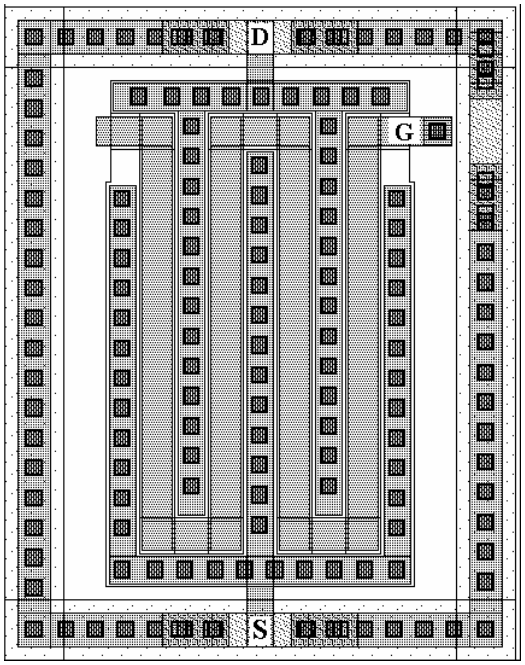


Figure 4. 12 Layout of sub-threshold operated NMOS transistor.

Figure 4.13 is the floor plan of the sub-threshold operated NMOS transistor. A common-centroid layout technique is employed for better matching.

Figure 4. 13 Floor plan of sub-threshold operated NMOS transistors.

Figure 4.14 depicts the complete layout of the VRC. The layout area is 0.12 mm^2.

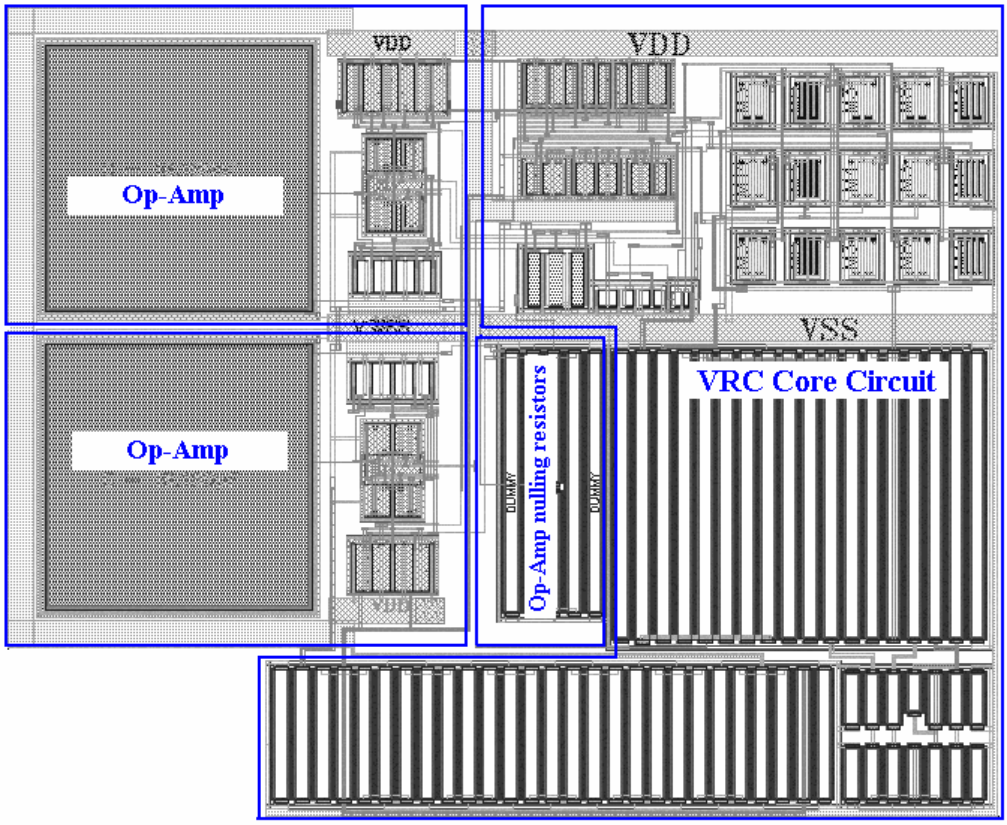


Figure 4. 14 Complete layout of the proposed voltage reference circuit.

4.5 Results

4.5.1 Temperature Coefficient

Plotted in Figure 4.15 is the simulated temperature dependency of the proposed VRC at 1.2 V supply voltage, with temperature ranging from -40°C to 125°C. The reference voltage obtained at 27°C is 200.455 mV. With the data points available in the figure, the worst temperature coefficient (*TC*) of the 1.2 V VRC maybe calculated.

$$TC_{(-40°C \sim 56°C)} = \left| \frac{1}{200.455} \times \frac{201.604 - 200.371}{-40 - 56} \times 10^6 \right| \text{ppm/°C}$$

$$= 64.07 \text{ ppm/°C}$$

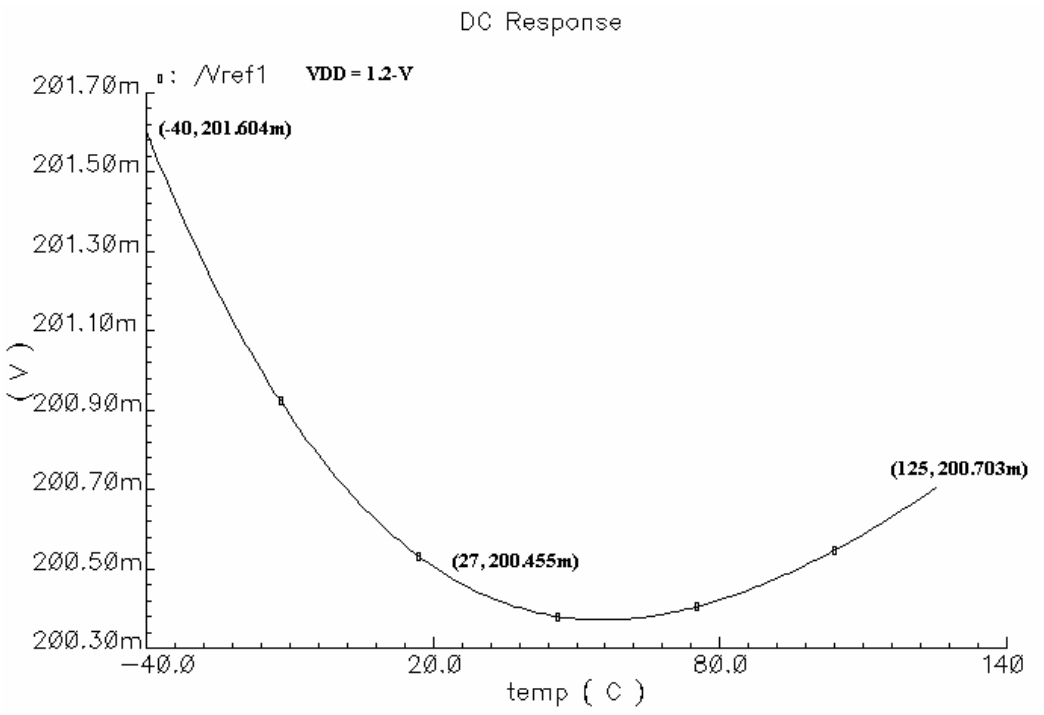


Figure 4. 15 Temperature coefficient of VRC at 1.2 V.

In another words, the peak-to-peak change of reference voltage within the temperature range of 165 is 1.224 mV.

Figure 4.16 depicts the temperature dependency at different supply voltages: 1.2 V, 1.5 V and 1.9 V.

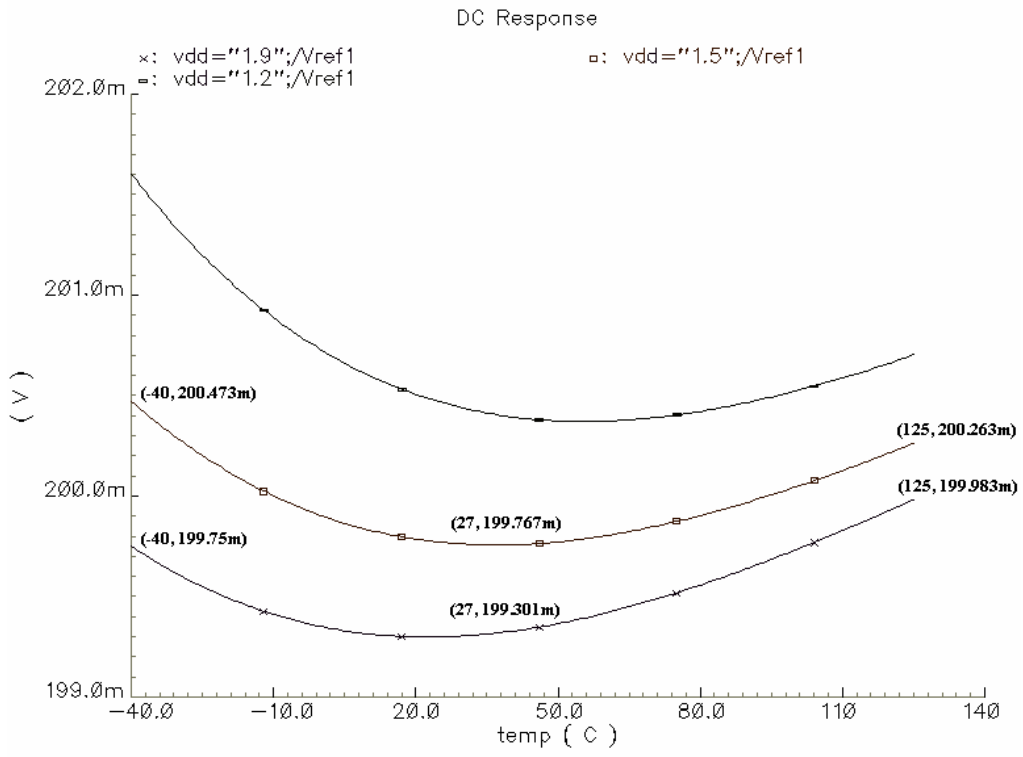


Figure 4. 16 Temperature dependency at different supply voltage.

Using the *TC* calculation in previous page, the *TC*s for supply voltages of 1.5 V and 1.9 V, can be calculated:

$$TC_{(-40°C \sim 37°C),@1.5-V} = \left| \frac{1}{199.767} \times \frac{200.473 - 199.757}{-40 - 37} \times 10^6 \right| \text{ppm/°C}$$

$$= 46.55 \text{ ppm/°C}$$

$$TC_{(23°C \sim 125°C),@1.9-V} = \left| \frac{1}{199.301} \times \frac{199.299 - 199.983}{23 - 125} \times 10^6 \right| \text{ppm/°C}$$

$$= 33.65 \text{ ppm/°C}$$

Tabulated in Table 4.1 are the simulated typical and 4-corner results. All graphs are plotted in Appendix C.

Table 4.1: Simulated *TC* performance under 4-corner models.

Corner (NMOS, PMOS)	*TC* (ppm/°C)		
	1.2 V	1.5 V	1.9 V
TYP (Typ, Typ)	64.07	46.55	33.65
WCP (Fast, Fast)	64.91	50.65	42.48
WCS (Slow, Slow)	74.67	57.22	42.03
WC0 (Slow, Fast)	71.82	43.10	30.16
WC1 (Fast, Slow)	74.56	63.12	56.54

4.5.2 Supply Dependency

From Figure 4.17, it can be seen that the reference voltage starts to decrease when supply voltage increases. The rate of change, ranging from 1.1 V to 1.2 V, is about -7.45 mV/V. The root of cause for such drastic change is found to be the deterioration of the op-amp performance at voltage of below 1.2 V. This is because some of the transistors start to operate either in sub-threshold or the linear region.

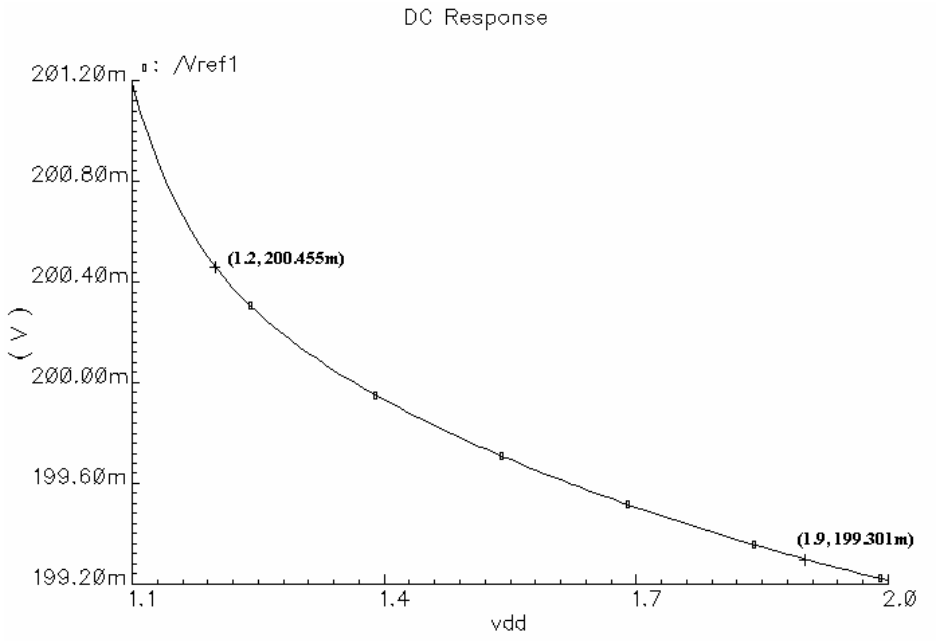


Figure 4. 17 Plot of supply dependency.

As compared to the supply dependency of -7.45 mV/V, the reference voltage decreases at a slower rate, of approximately 1.65 mV/V when the supply voltage varied from 1.2 V to 1.9 V. The reduction in the reference voltage within the operating supply voltage is caused by the imperfection of the current mirror. Therefore, the supply dependency performance can be improved through the use of better current mirror.

Table 4.2 summarizes the supply dependency of proposed work under 4-corner models. See Appendix C for details.

Table 4.2: Simulated supply dependency under 4-corner models.

Corner (NMOS, PMOS)	V_{ref} @ Supply voltage		Rate of change
	1.2 V	1.9 V	
TYP (Typ, Typ)	200.459 mV	199.300 mV	1.66 mV/V
WCP (Fast, Fast)	189.663 mV	188.586 mV	1.54 mV/V
WCS (Slow, Slow)	211.510 mV	210.367 mV	1.63 mV/V
WC0 (Slow, Fast)	209.680 mV	208.313 mV	1.95 mV/V
WC1 (Fast, Slow)	191.047 mV	190.369 mV	0.97 mV/V

4.5.3 PSRR

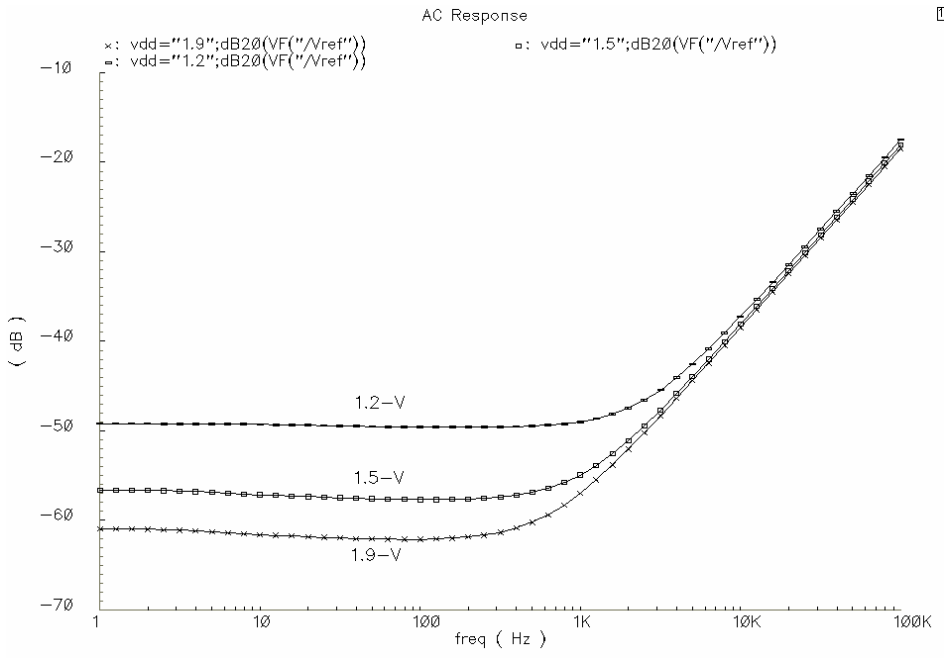


Figure 4. 18 Plot of *PSRR*.

Given in Figure 4.18 is the *PSRR* of the complete VRC. At 1.2 V supply voltage, the circuit is able to obtain a *PSRR* of -49 dB and a -3 dB bandwidth of 1.5 kHz. As the supply voltage increases, the *PSRR* performance becomes better. However, the bandwidth starts to shrink. Such phenomenon is because of the decrease of current as the supply voltage increases and eventually degrades the performance of the op-amp.

Other than typical case, all 4-corner models are simulated and the detail results are showing in Appendix C. Tabulated in Table 4.3 is the summary of the results:

Table 4.3: Simulated *PSRR* performance of 4-corner models:

Corner (NMOS, PMOS)	*PSRR* (dB), Bandwidth (Hz)		
	1.2 V	1.5 V	1.9 V
TYP (Typ, Typ)	-49.00, 1.50 k	-56.44, 1.06k	-60.83, 664.14
WCP (Fast, Fast)	-50.48, 2.20 k	-56.48, 1.13 k	-60.59, 737.93
WCS (Slow, Slow)	-42.56, 4.20 k	-58.54, 693.57	-64.52, 316.23
WC0 (Slow, Fast)	-46.40, 2.73 k	-54.49, 1.65 k	-57.89, 962.22
WC1 (Fast, Slow)	-51.18, 1.75 k	-61.86, 479.91	-67.32, 237.37

4.5.4 Transient Simulation

Transient simulation is carried out to check the transient response of the voltage reference circuit. This is a crucial step, to ensure that the VRC can start up and power down properly right after the supply change.

Figure 4.19 illustrates the power up and down responses of the reference circuit. Within 10 ms of time, the circuit is able stabilize at 0.2 V after supply voltage is ramp up to 1.2 V [see Figure 4.19 (a)]. From Figure 4.19 (b), it can be seen that the reference circuit is completely turned off in less than 0.1 ms of the shutting down of the supply 1.2 V.

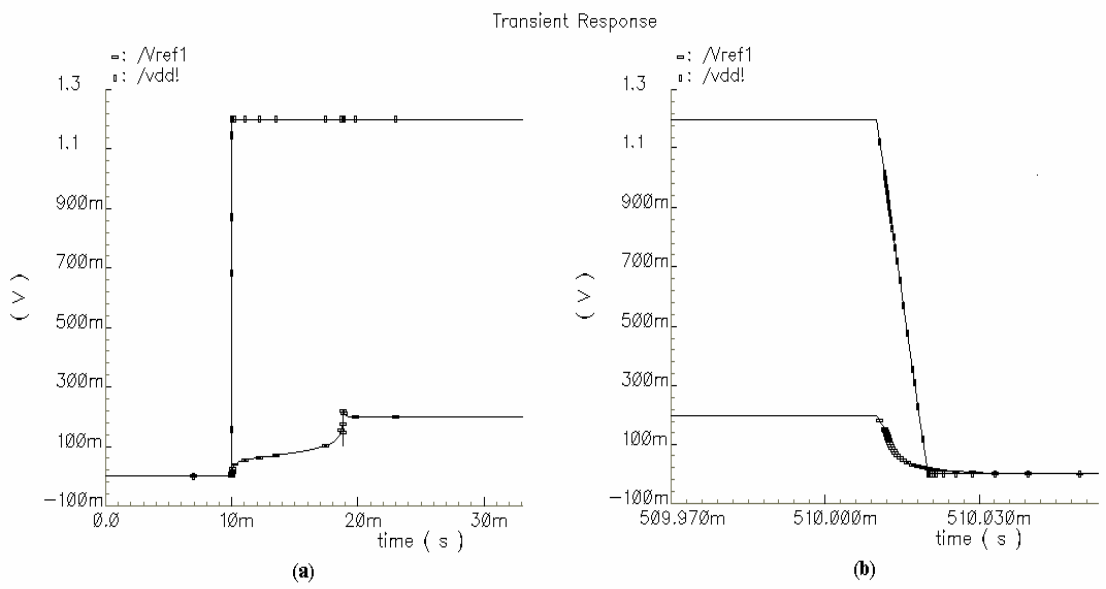


Figure 4. 19 (a) Start up simulation and, (b) Power down response of the VRC.

From 4-corner simulations (see Appendix C), it shows that the circuit reaches the designed value of 0.2 V within 10 ms, except the slow NMOS slow PMOS case which takes about 15 ms to stabilize. And it shuts down within 0.1 ms under all cases.

4.6 Summary

A new low supply voltage of 1.2 V VRC has been constructed using only MOSFETs and resistors, without requiring low threshold voltage devices. In this architecture, sub-threshold operated NMOS transistors are used in the core circuit design for the creation of both PTAT and CTAT components. A resistance reduction technique has been demonstrated in the PTAT current generator. In additional, an alternative solution to the input common-mode of the op-amp under a low supply voltage is suggested. Due to the high threshold voltages of the transistors, a body bias circuitry is added to reduce the threshold voltage of the PMOS transistor.

At 1.2 V supply voltage, the reference voltage of the proposed VRC is 200.41 mV. It consumes a total current of 38 µA and having a *PSRR* of -49.6 dB. A *TC* of 64.1 ppm/°C is calculated at the same supply voltage. The supply dependency of the circuit within the supply range of 1.2 V to 1.9 V is 1.65 mV/V.

To summarized, the performance of the 1.2 V VRC is given in Table 4.4.

Table 4.4: Performance summary of 1.2 VRC.

Parameters	**Simulated**
Technology	AMIS 0.5 µm, CMOS process
V_{TH} (27°C)	$V_{TH,P}$ = -0.96 V, $V_{TH,N}$ = 0.74 V
Supply voltages	1.2 V to 1.9 V
Supply current	38 µA @ 1.2 V
Reference voltage, V_{ref}	200.41 mV @ 1.2 V, 27°C
Supply dependency	1.65 mV/V (1.2 V to 1.9 V)
TC (-40°C to 125°C)	64.1 ppm/°C @ 1.2 V
PSRR @ DC	-49.6 dB

The *TC* performance of the proposed work is not as good as expected. However, this performance parameter can be further improved through the implementation of the curvature compensation.

Chapter 5

Conclusion and Recommendations

5.1 Conclusion

In this project, two voltage reference circuits that can operate with power supplies of 1 V and 1.2 V have been design using the current mode approach. The two circuits are implemented using two different processes, namely the AMS 0.6-µm CMOS and AMIS 0.5-µm CMOS processes.

A simple self-cascode composite transistor structure [27] is adopted in the first design to improve the power supply rejection ratio of the reference circuit. The low voltage op-amp, known as operational transconductance amplifier (OTA), chosen for the use in the reference circuit has enhanced its gain for having high *PSRR* performance. The silicon measurement on voltage reference circuit is able to achieve a temperature coefficient of 30.15 ppm/°C without curvature compensation for temperature ranging from 0°C to 100°C under the 1 V supply voltage. The circuit designed can work under a supply voltage of between 1 V to 1.8 V. At 1 V supply voltage, the *PSRR* of the VRC is able to reach -54.5 dB.

The second voltage reference circuit presented in chapter four is made up of only CMOS transistors and resistors reference circuit. Sub-threshold operated NMOS transistor replaced BJT as key component in PTAT and CTAT generators. The proposed change in the core circuit offers not only reduction in resistance value but also having features of offset voltage suppression and reduction in current consumption. Body biasing technique is again employed in this design to bring down the threshold voltage of PMOS transistor in the VRC. Simulation revealed a *TC* of 64.1 ppm/°C for temperature varying from -40°C to 125°C, under 1.2 V supply. The imperfect current mirror directly caused a 1.154 mV change in

reference voltage for supply ranging from 1.2 V to 1.9 V. *PSRR* performance in this design is around -49 dB at 1.2 V supply.

The threshold voltage of MOSFET transistor is the major constraint in the design of VRC. Although techniques such as body biasing can be adopted for smaller threshold voltage, the source-to-bulk voltage should preferably be less than 0.4 V, so as not to incur large leakage current. Besides adopting circuit topology to improve the *PSRR* performance of the reference circuit, the proposed work offers an alternative way to reduce the die area, through the reduction of resistance value.

5.2 Recommendations

The use of advanced technologies with smaller device lengths such as standard 0.35 µm process can help to get rid of the design bottleneck in low voltage regime due to the threshold voltage of the transistor. With smaller threshold voltages offered by the advanced technologies, low power circuit can be easily realized in sub 1 V supply voltage.

To further enhance the temperature dependency performance, the existing curvature compensation techniques [10] [20] or new ideas are encouraged in the proposed works. With this, the *TC* is likely to be below than 10 ppm/°C.

Without using the curvature compensation technique, 5-terminal lateral p-n-p BJT (Figure 2.2) can be used to replace the sub-threshold operated NMOS transistor in the design of the pure CMOS reference circuit for better *TC*. However, the current consumption has to be traded-off as the part of the current will be wasted through the intrinsic vertical BJT structure in the lateral p-n-p BJT.

The inaccurate simple current mirror used in the second design (see Figure 4.11) created performance issue as the supply voltage increased. A more accurate current mirror, such as the cascode current, may be implemented in the improved version for better performance in supply dependency.

Instead of biasing the low voltage op-amp in the second design (refer to Figure 4.11) through a positive temperature dependent current, a temperature independent current is more reliable for maintaining constant performance throughout the temperature and supply ranges of interest. This can ensure stability in the overall performance of the voltage reference circuit.

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Appendix A

The following table tabulates all the components' values used in the 1 V VRC.

Table A.1: Detail design of 1 V VRC circuit.

Component	Type	Width (*W*)*	Length (*L*)*	Multiplier (*N*)
M1A	PMOS	50	6	4
M1B	PMOS	50	6	2
M2A	PMOS	50	6	4
M2B	PMOS	50	6	2
M3A	PMOS	50	6	4
M3B	PMOS	50	6	2
M4A	PMOS	25	6	2
M4B	PMOS	25	6	1
M5A	PMOS	62.5	10	2
M5B	PMOS	62.5	10	1
M6A	PMOS	50	6	8
M6B	PMOS	50	6	4
M7A	PMOS	25	6	2
M7B	PMOS	25	6	1
M8A	PMOS	62.5	10	2
M8B	PMOS	62.5	10	1
M9	PMOS	50	4	7
M10	PMOS	50	4	7
M11	PMOS	50	10	1
M12	NMOS	50	10	1
M13	NMOS	25	4	3
M14	NMOS	25	4	3
M15	NMOS	50	10	1
M16	PMOS	50	10	2
M17A	PMOS	50	6	4
M17B	PMOS	50	6	2
M18A	PMOS	50	6	4
M18B	PMOS	50	6	2
M19	NMOS	20	4	1
M20	NMOS	20	4	1
M21	PMOS	50	6	4
M22	NMOS	50	5	1
M23	NMOS	6	8	1
M24	NMOS	6	8	1
M25A	PMOS	25	6	2
M25B	PMOS	25	6	1

M26A	PMOS	50	6	4
M26B	PMOS	50	6	2
M27	NMOS	20	4	1
Q1	VERT15	-	-	1
Q2	VERT15	-	-	24
Q3	VERT15	-	-	1
Q4	VERT15	-	-	1
R_P	RPOLYH	10	660	-
R_{1A}	RPOLYH	10	3800	-
R_{1B}	RPOLYH	10	1327	-
R_{2A}	RPOLYH	10	3800	-
R_{2B}	RPOLYH	10	1327	-
R_{BB1}	RPOLYH	10	412.5	-
R_{BB}	RPOLYH	10	2475	-
C_1	CPOLY	155.2	160	-

* Width and Length are in micro centimeter (μm).

VERT 15: Vertical p-n-p BJT in AMS CMOS 0.6 μm process.
RPOLYH: High resistance poly resistor in AMS CMOS 0.6 μm process.
CPOLY: Double poly capacitor in AMS CMOS 0.6 μm process.

Appendix B

The following table presents all the components' values used in the 1.2 V VRC. See Figure 4.12 for reference.

Table B.1: Detail design of 1.2 V VRC circuit.

Component	Type	Width (*W*)*	Length (*L*)*	Multiplier (*N*)
M1	PMOS	15	3	3
M2	PMOS	15	3	1
M3	PMOS	15	3	2
M4	PMOS	15	3	2
M5	PMOS	15	3	1
M6	PMOS	12	3	2
M7	PMOS	12	3	4
M8	PMOS	12	3	2
M9	NMOS	60	1	1
M10	NMOS	60	1	1
M11	NMOS	5	2	1
M12	NMOS	5	2	1
M13	PMOS	12	3	2
M14	NMOS	20	5	1
M15	NMOS	20	5	2
M16	NMOS	6	3	1
M17	NMOS	6	3	4
M18	PMOS	18	3	1
M19	PMOS	18	3	4
M20	PMOS	12	2	6
M21	PMOS	12	2	6
M22	NMOS	12	3	2
M23	NMOS	12	3	2
M24	PMOS	18	3	2
M25	NMOS	12	3	2
M26	PMOS	15	3	1
MS1	NMOS	60	1	1
MS2	NMOS	60	1	8
MS3	NMOS	60	1	4
R_P	HY	330.5	5	1
R_{ref}	HY	425	5	1
R_C	HY	5	1180	1
R_{B1}	HY	5	550	1
R_{B2}	HY	5	700	1

R_N	HY	5	50	1
C_C	PP	104.8	104.8	1

* Width and Length are in micro centimeter (μm).

HY: High resistance poly resistor in AMIS CMOS 0.5 μm process.
PP: Double poly capacitor in AMIS CMOS 0.5 μm process.

Appendix C

4-corner models simulation results:

C.1. *TC* performance

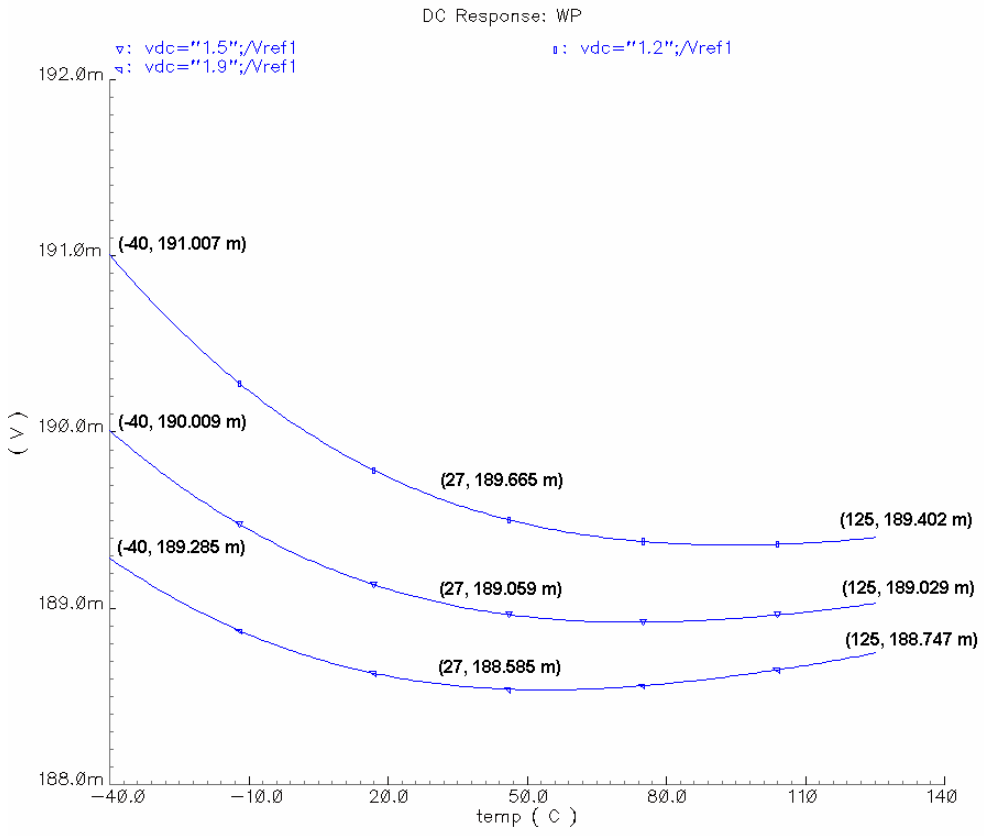

Figure C.1 Simulated *TC* with fast transistor model.

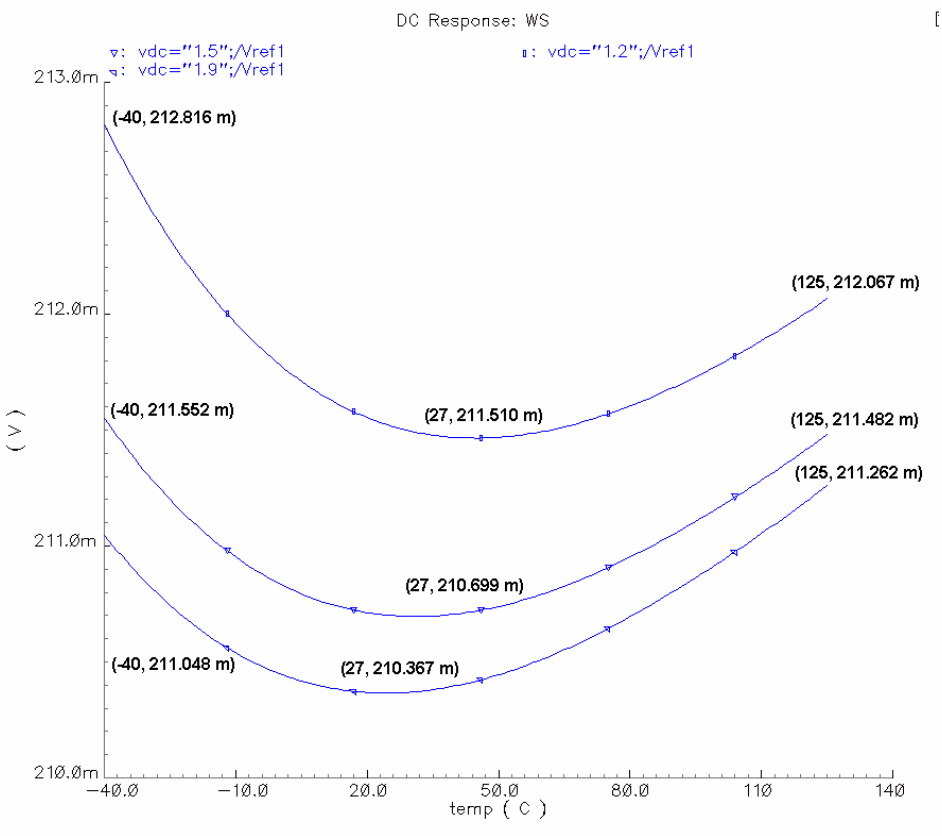

Figure C.2 Simulated *TC* with slow transistor model.

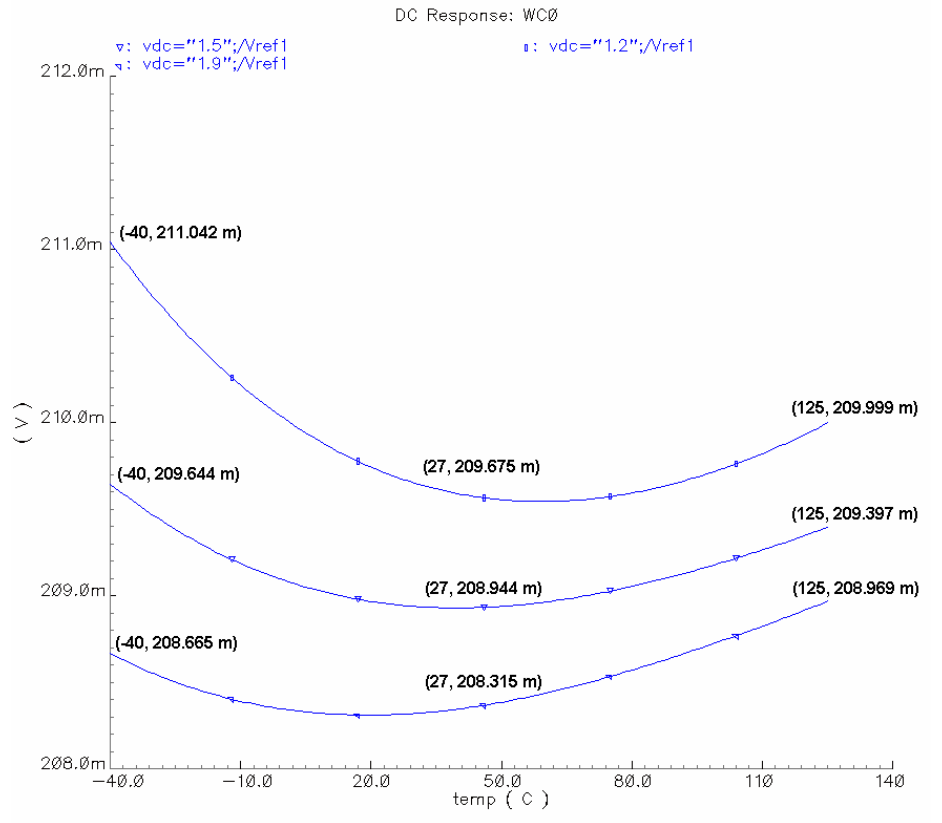

Figure C.3 Simulated *TC* with slow NMOS & fast PMOS transistor models.

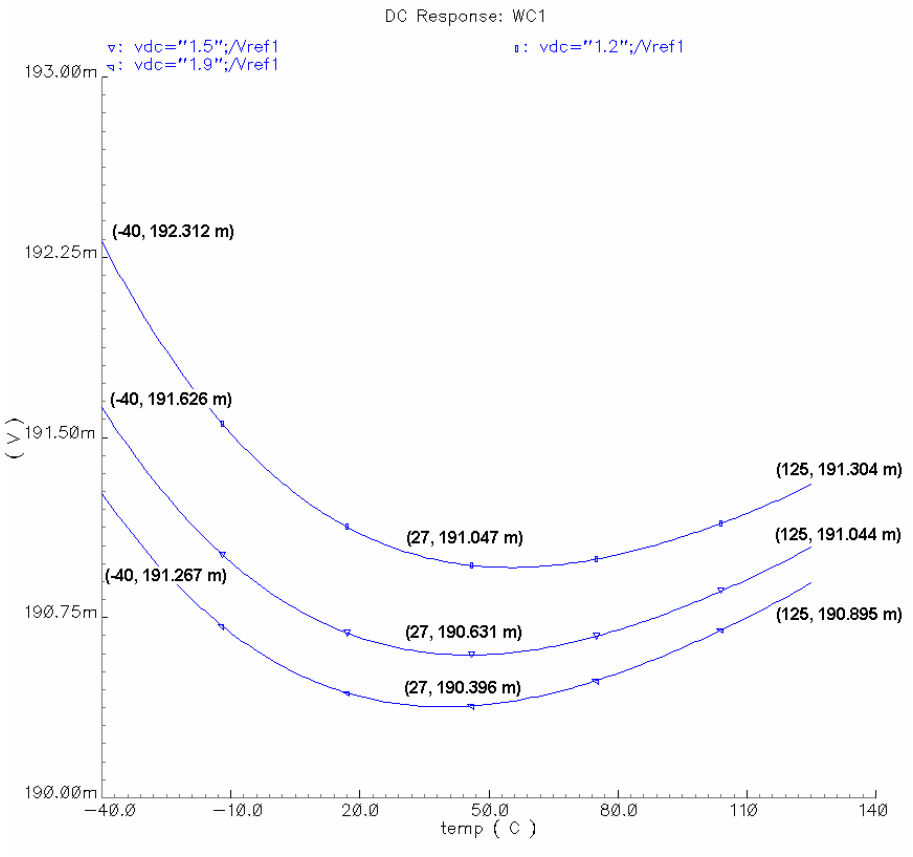

Figure C.4 Simulated *TC* with fast NMOS & slow PMOS transistor models.

C.2. Supply dependency

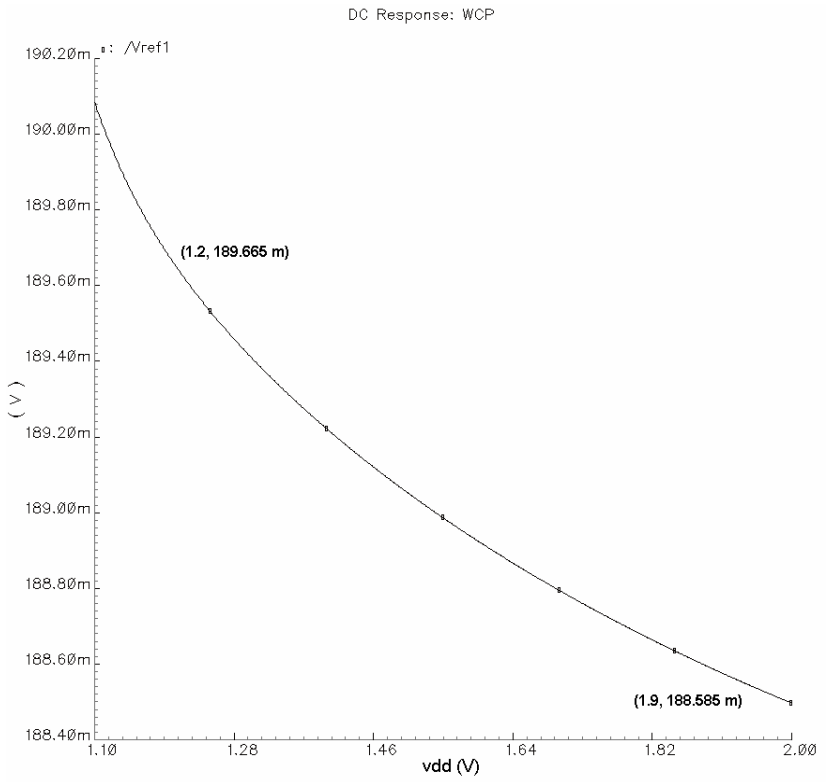

Figure C.5 Simulated supply dependency with fast transistor model.

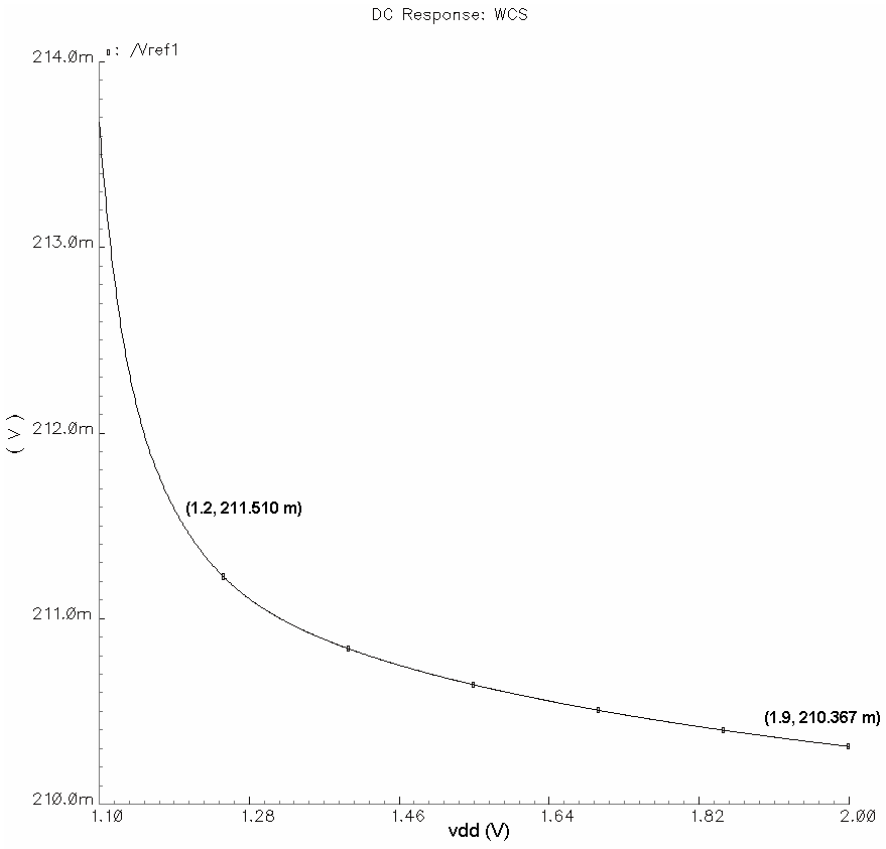

Figure C.6 Simulated supply dependency with slow transistor model.

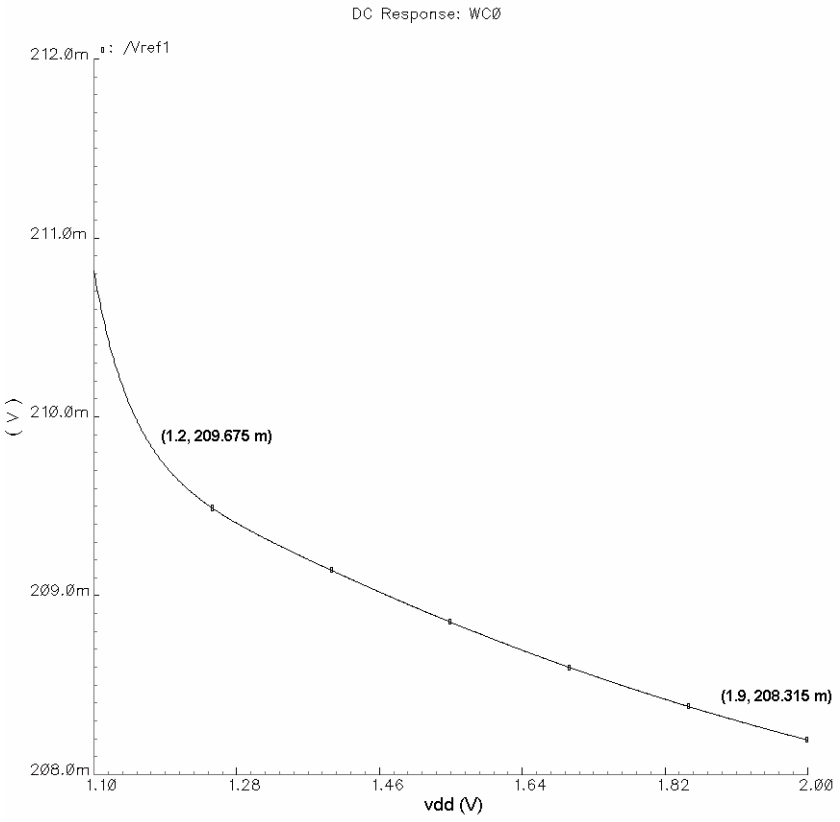

Figure C.7 Simulated supply dependency with slow NMOS & fast PMOS transistor models.

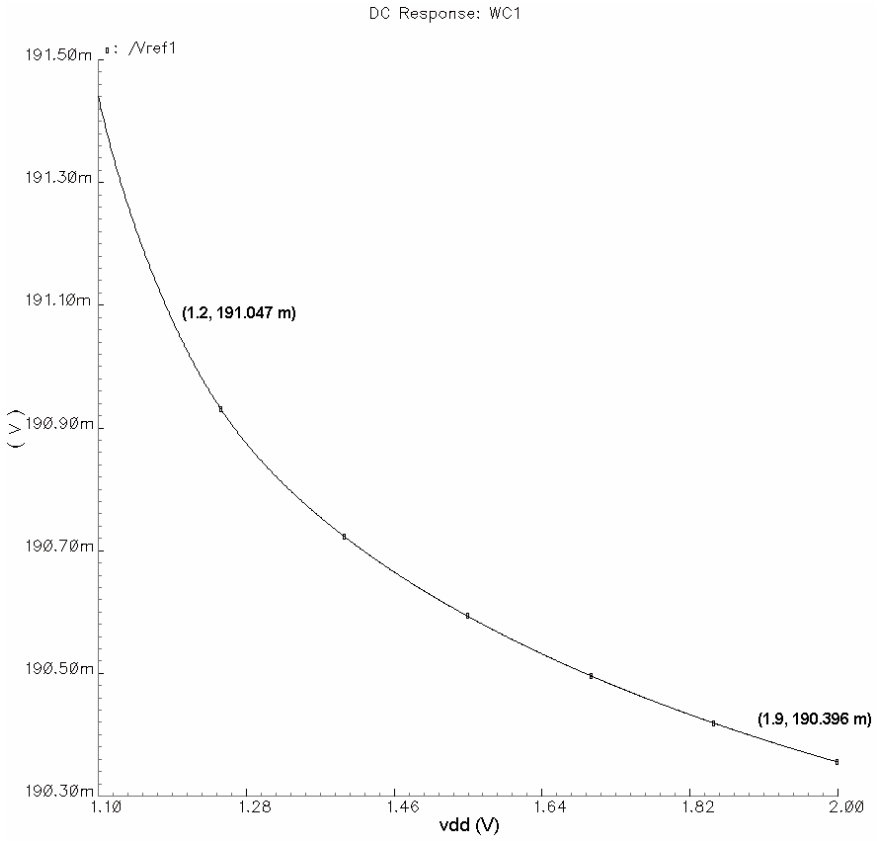

Figure C.8 Simulated supply dependency with fast NMOS & slow PMOS transistor models.

C.3. PSRR

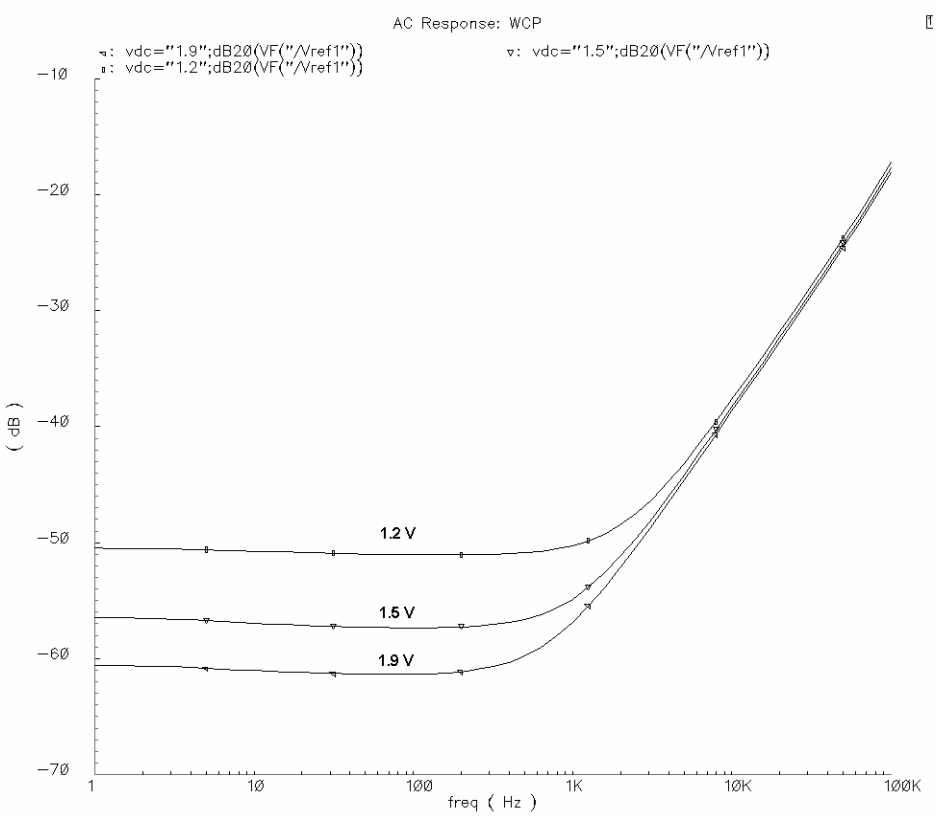

Figure C.9 Simulated *PSRR* with fast transistor model.

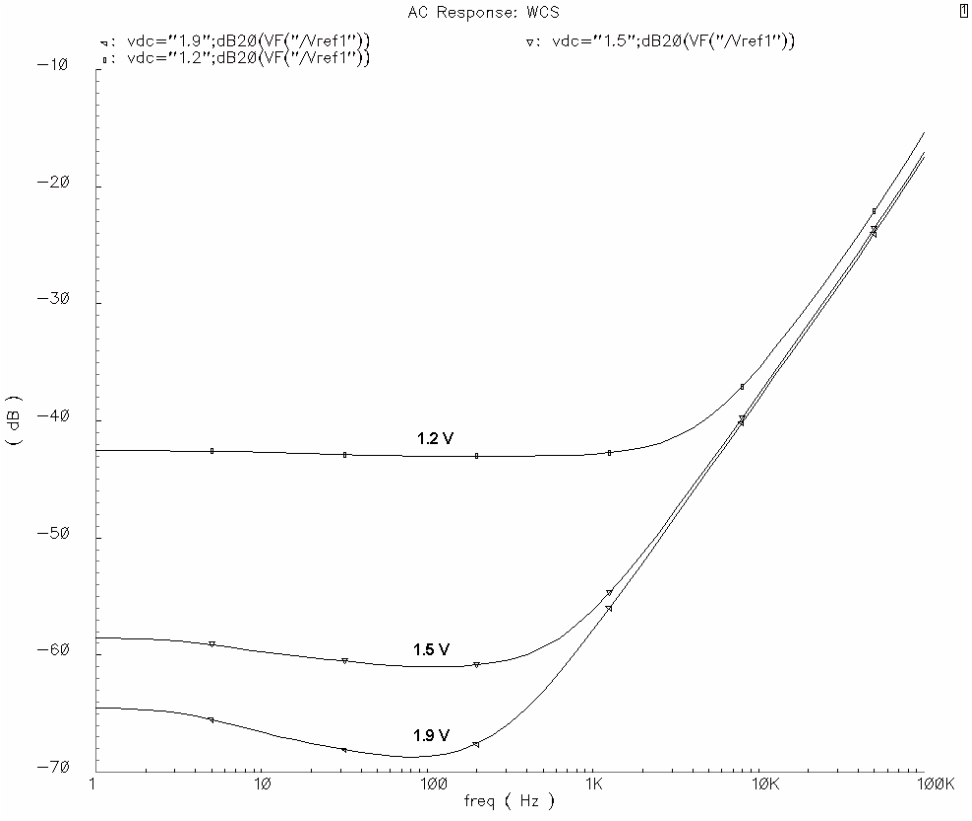

Figure C.10 Simulated *PSRR* with slow transistor model.

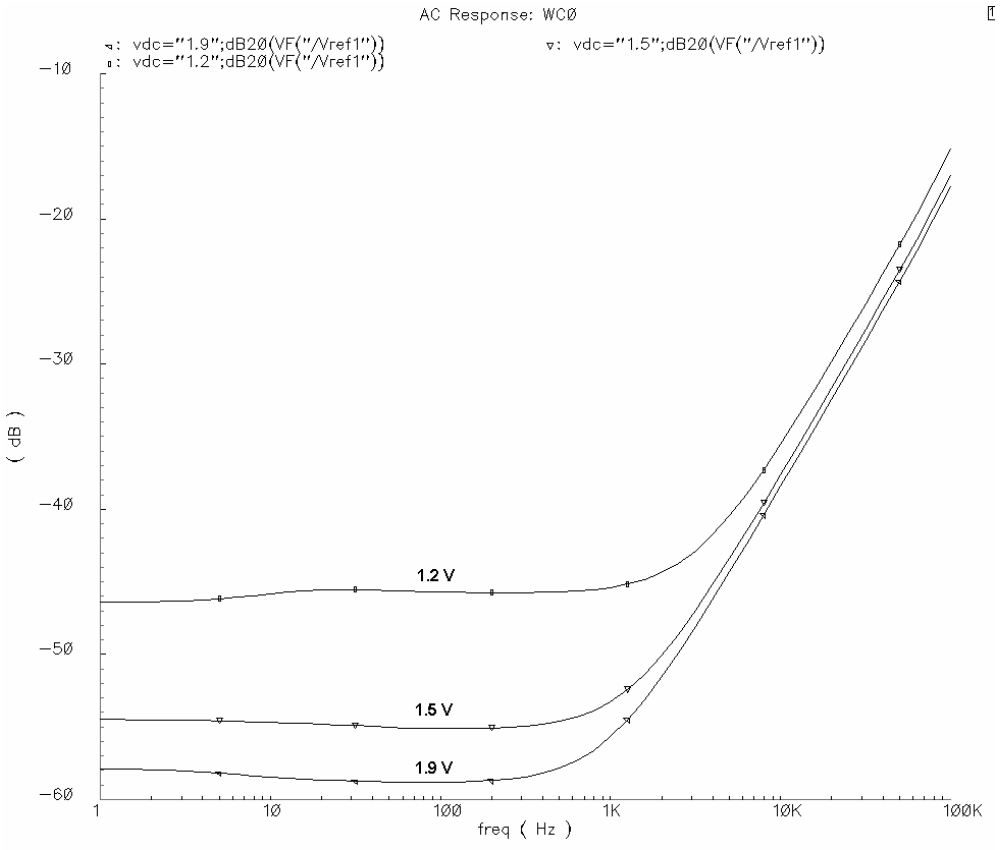

Figure C.11 Simulated *PSRR* with slow NMOS & fast PMOS transistor models.

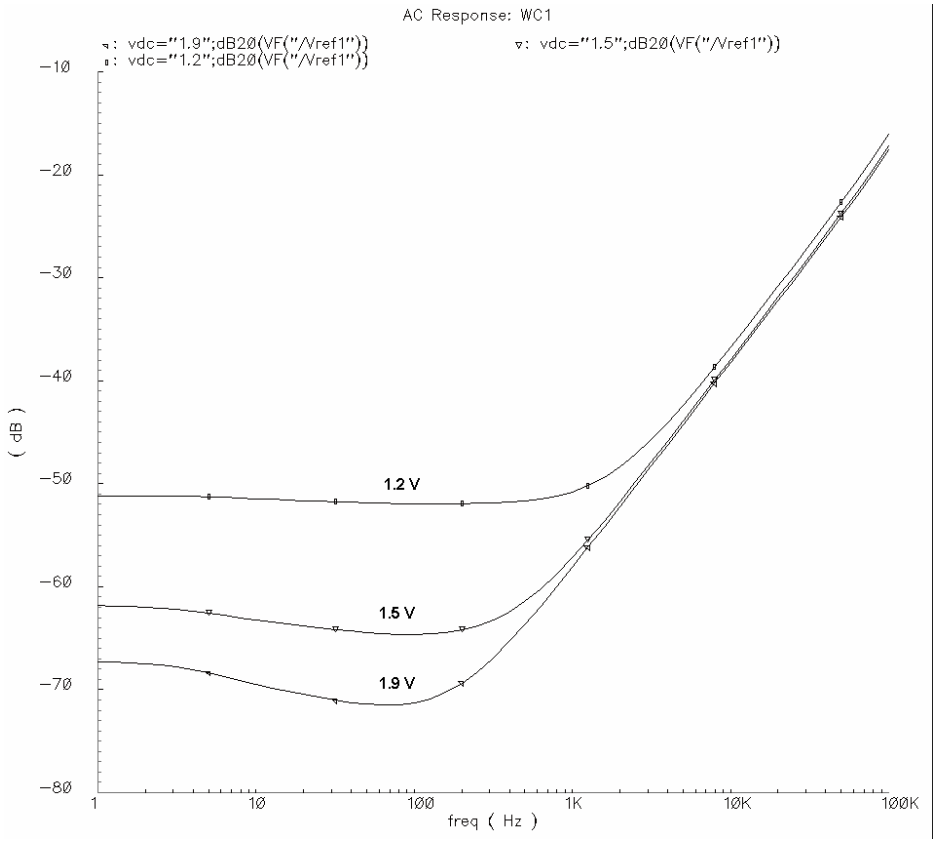

Figure C.12 Simulated *PSRR* with fast NMOS & slow PMOS transistor models.

C.4. Transient simulation

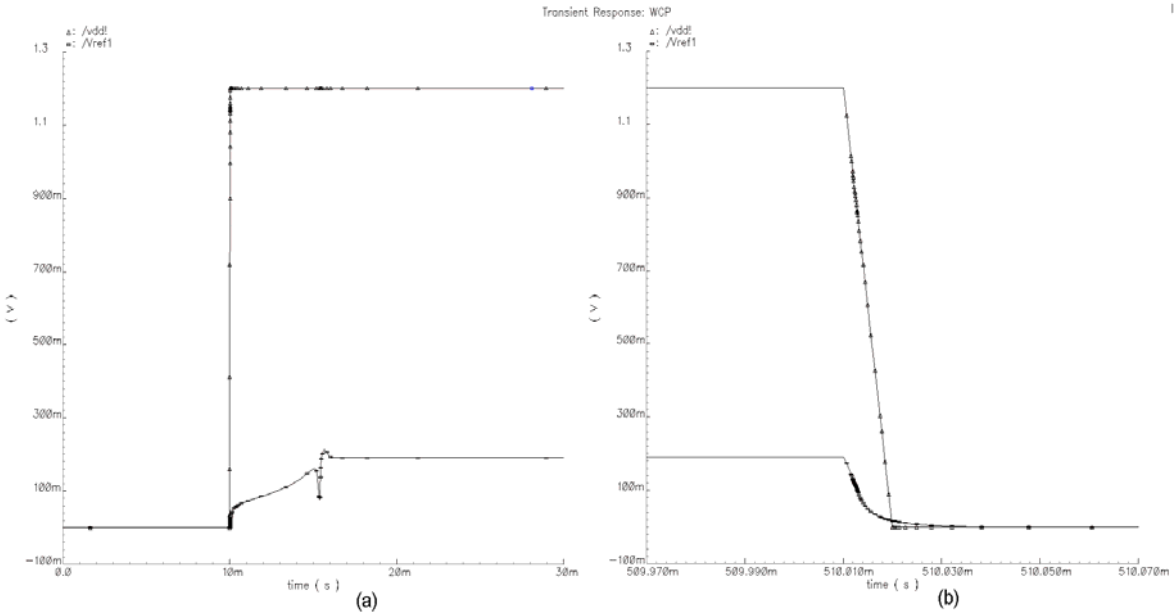

Figure C.13 (a) Start up simulation and, (b) Power down response with fast transistor model.

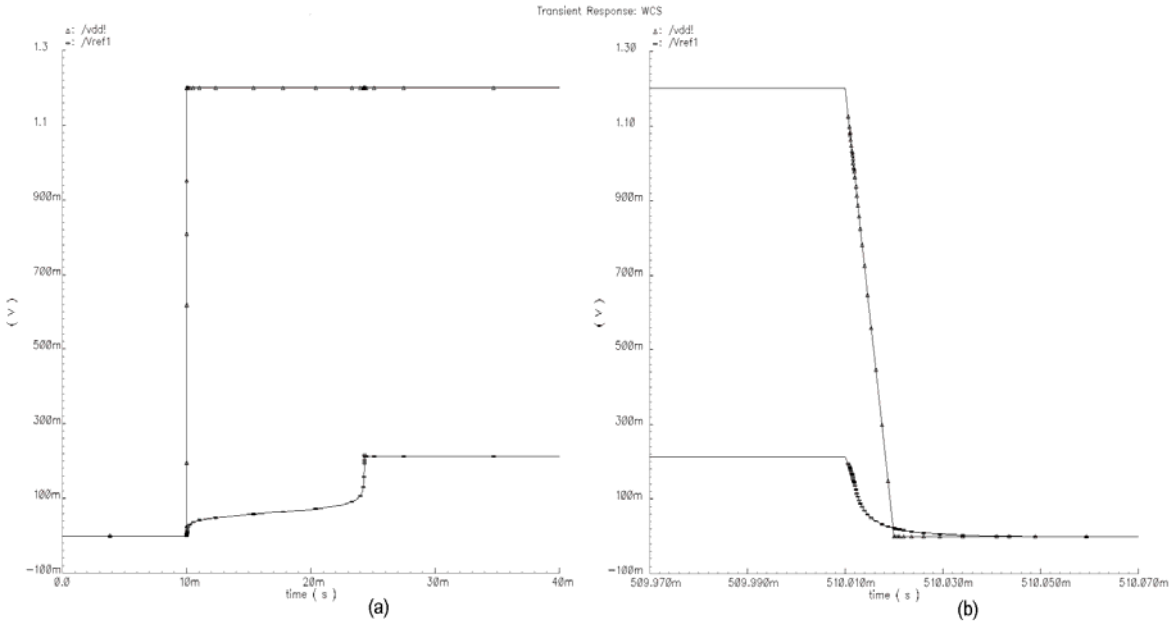

Figure C.14 (a) Start up simulation and, (b) Power down response with slow transistor model.

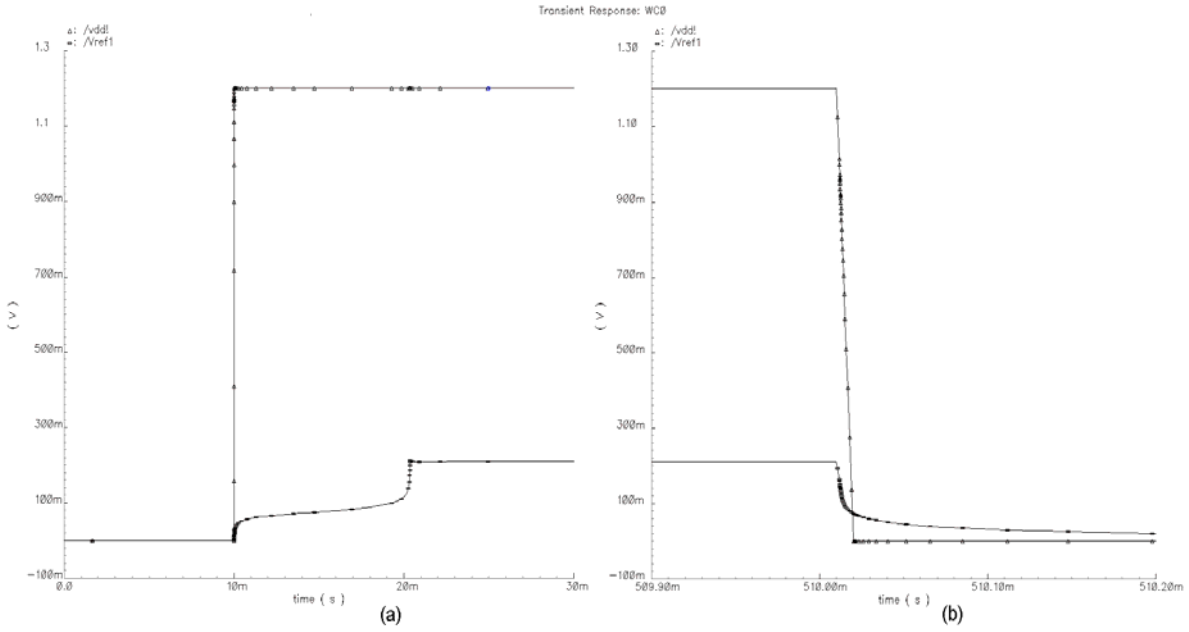

Figure C.15 (a) Start up simulation and, (b) Power down response with slow NMOS & fast PMOS transistor models.

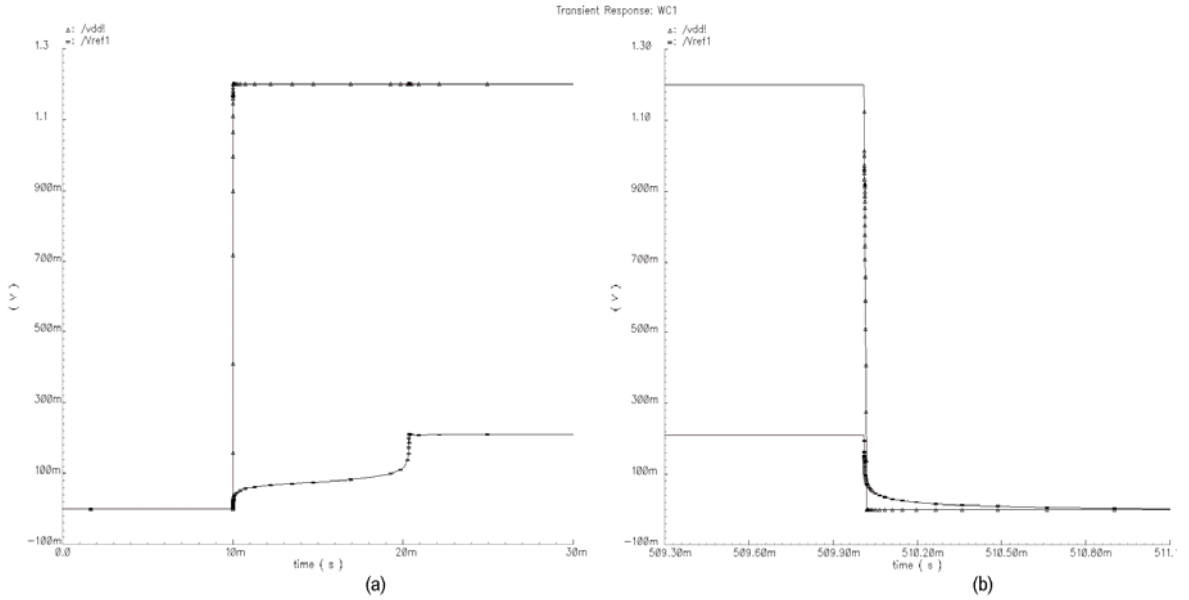

Figure C.16 (a) Start up simulation and, (b) Power down response with fast NMOS & slow PMOS transistor models.