Temperature Compensated dB-linear Digitally Controlled Variable Gain Amplifier with DC Offset cancellation

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***Abstract*—This paper presents a compact digitally controlled variable gain amplifier (DVGA) with capabilities of both temperature compensated linear-in-decibel (dB-linear) gain control and DC offset cancellation (DCOC) without making use of either the feedback or the feed-forward loop. The proposed DVGA design is a 3 stage inductorless cascaded amplifier that is integrated with a temperature compensated dB-linear gain control, a DCOC, an output common mode feedback (CMFB), a 6-bit digital gain control (with a 64 step resolution), a power shutdown mode, and a linearizer for improving the 1-dB gain compression point. The design is fabricated using a commercial 0.18-μm SiGe BiCMOS technology. The DVGA has a measured gain range of 18.4 dB with an average step size of 0.3 dB, a 3-dB bandwidth from 2 MHz to 1.9 GHz with a ±0.75 dB gain flatness from 2.75 MHz to 1.2 GHz, an input 1-dB gain compression point better than -12.5 dBm, an input return loss better than 12 dB, an output return loss better than 16 dB, and a DC power consumption of 12.2 mW from a 1.8 V supply. The core DVGA, by excluding the I/O measurement pads, occupies a die area of 160 μm x 300 μm.**

***Index Terms*—Common mode feedback, dB-linearity, DC offset cancellation, Digital gain control, Digital Variable Gain Amplifier, Exponential current converter, Linear-in-decibel gain characteristics, Linearizer, Low power design, SiGe BiCMOS, Temperature compensation, Variable gain amplifier**

I. Introduction

A VARIABLE gain amplifier (VGA) is an indispensible part of wired and wireless transceivers [1-14]. As the state-of-the-art is advancing, the level of integration of the microwave and the millimeter-wave transceivers are gradually increasing towards single chip solutions [2]. For the VGA to be presented as a key building block in the compact transceiver system, it is desirable to possess certain enhanced characteristics, such as low power consumption, small die-footprint, good impedance matching at the input and output to maximize the RF power transfer, insensitive to Process-Voltage-Temperature (PVT) variations, high linearity for both RF input as well as the gain control input, wide bandwidth, good passband gain-flatness, and easy interface with the digital baseband processor [3].

As the process technology is advancing, many of the desirable design characteristics, for instance the low power consumption, small die area, broad dynamic range, and wide bandwidth that are also related to the VGA performance can be accomplished [4]. The remaining characteristics, primarily the PVT insensitivity and the linearity, can be achieved by proper design techniques and understanding the properties and limitations of the components supported by the fabrication process [5-6].

DC offset is the most prevailing consequence of the process variation in differential circuits. There are various circuit design methods to overcome the DC offset, specifically by implementing the DC offset canceller (DCOC) such as, the feedback offset cancellation [8], [11] and feed-forward offset cancellation [12] using low pass filters (LPF), AC coupling between the stages using large decoupling capacitors [10], and the complex digital signal processing (DSP) offset cancellation technique [13]. As a comparison among the passive DCOC (using resistors and capacitors), RC-LPF with the same cutoff frequency, has the passband insertion loss more than the high pass filter (RC-HPF). This is mainly due to the large filter resistor of the RC-LPF that appears in series along the RF signal path. For substantial DC offset suppression using the RC-LPF for the feedback and feed-forward DCOC, the amplitude of the DC component filtered out by the LPF must be equal to or greater than the DC component in the actual signal. To achieve the required loop gain, amplifiers are incorporated in the DCOC loop [8], [11-12]. The amplifiers compensates the loss due to the LPF and significantly cancels the DC offsets present in the signal. However, amplifiers consume additional DC power. The DCOC using DSP is based on the feedback from the digital baseband by tracking the average signal value. It is a complicated approach consuming more DC power and die area [13]. Therefore, the need for a low loss, low power, and compact DCOC becomes apparent.

A few of the circuit design techniques for temperature compensation are the biasing voltage predicting method [7]

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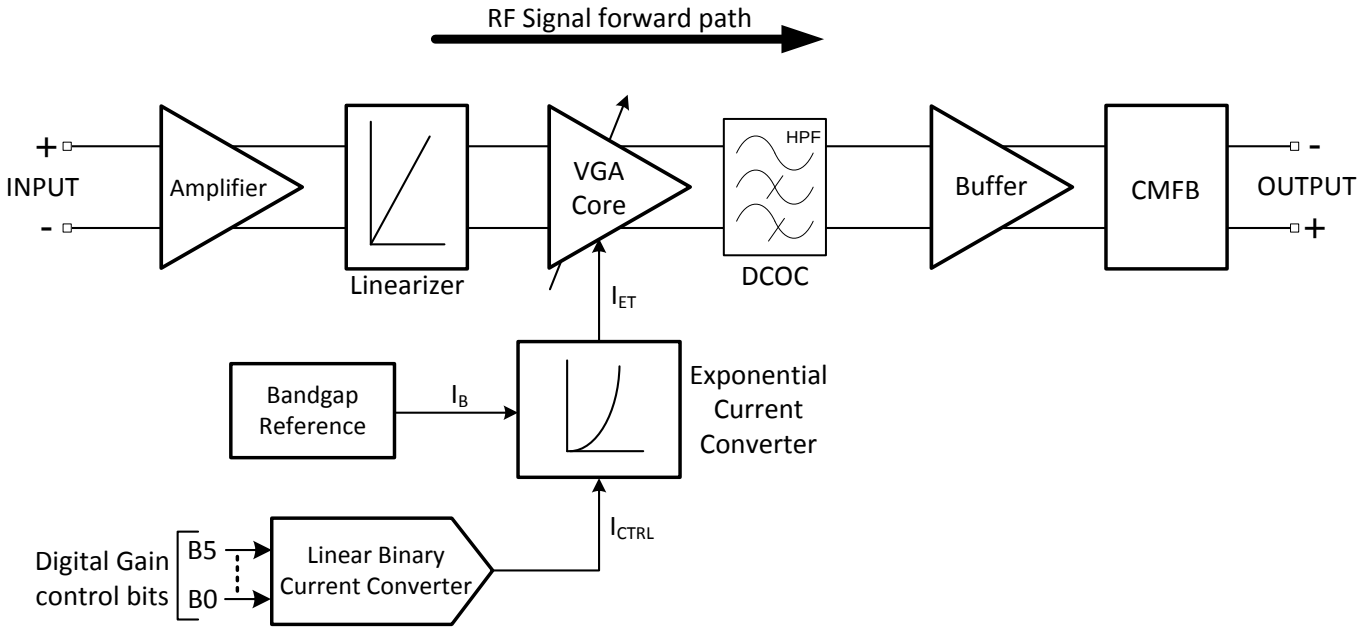

Fig. 1. Block diagram of the proposed temperature compensated dB-linear DVGA with DCOC

and the method of stabilizing the circuit parameters affected by temperature [8-10]. For low power applications, a temperature insensitive VGA that is effective over a wide temperature range is desirable and additionally, an uncomplicated design that consumes less power becomes essential.

The linearity performance of the building blocks in the RF transceiver ensures a large dynamic range and a longer communication distance coverage [14]. It is desirable that each transceiver building block, including the VGA, supports large signal amplitudes without saturation and in this course of action consumes low DC power.

In this paper, a thorough design consideration for commercial viability based on the low cost, long battery life, good linearity, and temperature insensitivity is perceived and a low power digitally controlled variable gain amplifier (DVGA) integrated with linear-in-decibel gain control (dB-linearity), passive DCOC, and relatively high linearity is studied and developed. The related core circuit blocks of the proposed DVGA, such as the digital gain control block with dB-linearity, the temperature compensation, the DCOC, the linearizer, and the output common mode feedback (CMFB), are analyzed theoretically and verified experimentally. By merely employing bipolar transistors and canceling the effect of the thermal voltage (V_T) across the transistor's base-emitter junction, a temperature compensated DVGA with good dB-linear gain characteristics is achieved. The proposed DVGA design also has a low loss passive RC-HPF DCOC with fast settling time capability, a pre-distortion linearizer achieving good linearity and a steady CMFB output.

This paper is structured as follows. Section II describes the proposed design topology. The circuit analysis with deduction of the proposed design is detailed in Section III and the DVGA frequency response is determined in Section IV. Section V provides the experimental results that are proven using on-wafer measurement. Finally, the paper conclusion is given in Section VI.

II. Design Topology

The proposed temperature independent dB-linear DCOC DVGA is a fully differential 3 stage cascaded amplifier with symmetric structure along the RF signal path. The architecture of the proposed DCOC DVGA is summarized as a block diagram in Fig. 1. The first and the last stages of the DCOC DVGA are the fixed gain amplifier and the buffer stage with output CMFB, respectively. This design arrangement serves 2 critical purposes, namely, to provide a good broadband matching to a low 50 Ω resistance that is independent of the DVGA gain setting, as described in [14] and to provide a fixed common mode input/output DC voltage that is also independent of the DVGA gain setting, for aiding in a straightforward integration with other transceiver building blocks. The differential interface at the DVGA input/output could comprise of the off-chip large ac coupling capacitors or the on-chip DC level shifters to bias the next stage transistors. As discussed in Section III, the input fixed gain amplifier with transimpedance load [15] operates as a pre-distortion linearizer, achieving a good DVGA linearity performance and by using an output buffer with NMOS active load, the proposed DCOC DVGA achieves a steady CMFB output [16].

The VGA core shown in Fig. 1 provides both input signal differential gain and attenuation based on the digital 6-bit gain control information (B_5~B_0). The 6-bit digital control information is internally converted to the VGA gain control parameter (I_{ET}) by using a linear 6-bit binary current converter, a bandgap reference with Proportional to Absolute Temperature (PTAT) current source and a temperature compensated exponential current converter. The proposed DCOC DVGA can be directly interfaced to a digital baseband without the need of a digital to analog converter (DAC). The DAC significantly complicates the design and also increases the DC power consumption [17].

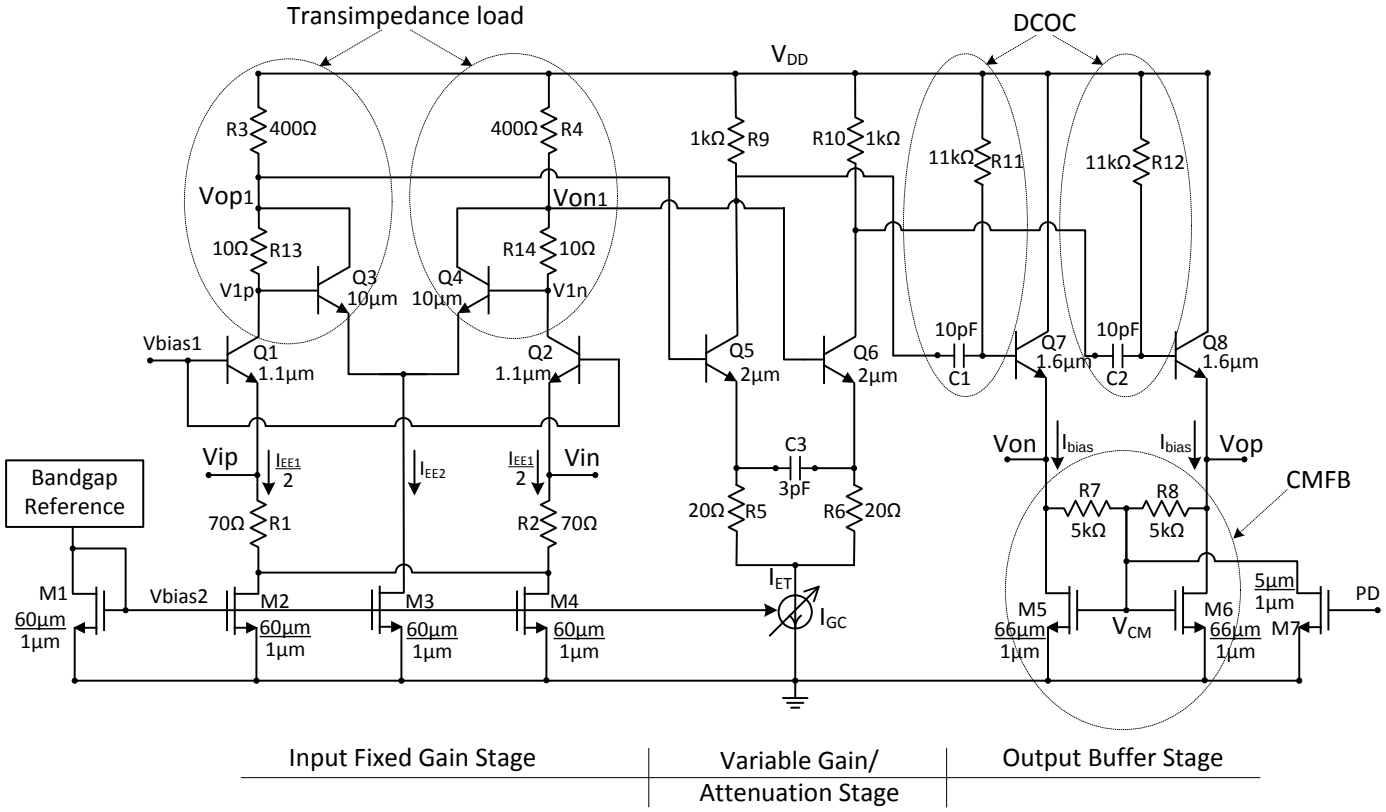

Fig. 2. Complete circuit schematic diagram of the proposed DCOC DVGA

In addition, the proposed DVGA has a differential DCOC at the output of the VGA core based on a passive low-loss RC-HPF that takes stability into consideration by avoiding any feedback or feed-forward loops along the signal path and improves the DVGA settling time.

In the following section, a detailed theoretical analysis and design considerations for each of the blocks discussed in the proposed DCOC DVGA topology are described.

III. Circuit Design Description

A. VGA Core and Digital Gain control

The proposed DCOC DVGA shown in Fig. 2 is a fully differential 3-stage cascaded amplifier with a common emitter amplifier as the VGA core. The overall DVGA gain is determined by the product of the gains of all the stages cascaded. The first and last stages of the DVGA have fixed gain, and hence, the VGA core's gain variation is linearly reproduced as the variation of the overall DVGA gain. Henceforth, the equations can be derived based on VGA core's gain (A_v) and ascertained that the analysis is applicable to the overall DVGA's gain.

The operating principle of the VGA core is based on the gain variation discussed in [14] that is obtained from the variable transconductance (g_m) of the amplifier and is controlled by the biasing current (I_{ET}).

For enhancing the dynamic range of the VGA, to compensate for the signal strength variations caused by the wireless/wired communication channel, the linear-in-decibel gain control is desirable. The proposed DVGA claims to achieve dB-linearity by using circuit design improvement over the linear gain control shown in [14]. The correlation between the gain and the gain control biasing current is shown in (1) and (2) as,

$$A_v = g_{m5,6} \cdot R_{9,10} \tag{1}$$

where, $R_{9,10}$ is the load resistance and $g_{m5,6}$ is the transconductance of the transistor pair Q5/Q6 given as.

$$g_{m5,6} = \frac{\delta I_{CT}}{\delta V_{be}} = \frac{\alpha}{\eta \cdot V_T} \cdot \left[\sum_{n=0}^{5} B_n \cdot I_n \cdot 2^n + I_{\min} \right] \tag{2}$$

where the common base current amplification factor α, the ideality factor η and the thermal voltage V_T are indicated for the transistor pair Q5/Q6, I_n (n = 0 to 5) are the constant coefficients of the estimated linear gain function, B_n (n = 0 to 5) are the digital bit value (either '1' or '0') received from the digital baseband and $I_{\min}$ is the DC current corresponding to minimum gain when all the digital control bits B_n are reset ('0').

The transconductance $g_{m5,6}$ from (2) implies a linear variation of gain associated with the 6-bit digital gain control word (B_5~B_0) as verified in [14]. Since the variable biasing current I_{ET} (shown in Fig. 2) controls the transconductance $g_{m5,6}$ and is derived from the bandgap reference (V_{bias2}), the gain (A_v) is also insensitive to the temperature variations.

The VGA core's gain from (1) in decibel (dB) is,

$$A_v, dB = 20 \cdot \log_{10}(g_{m5,6} \cdot R_{9,10}) \tag{3}$$

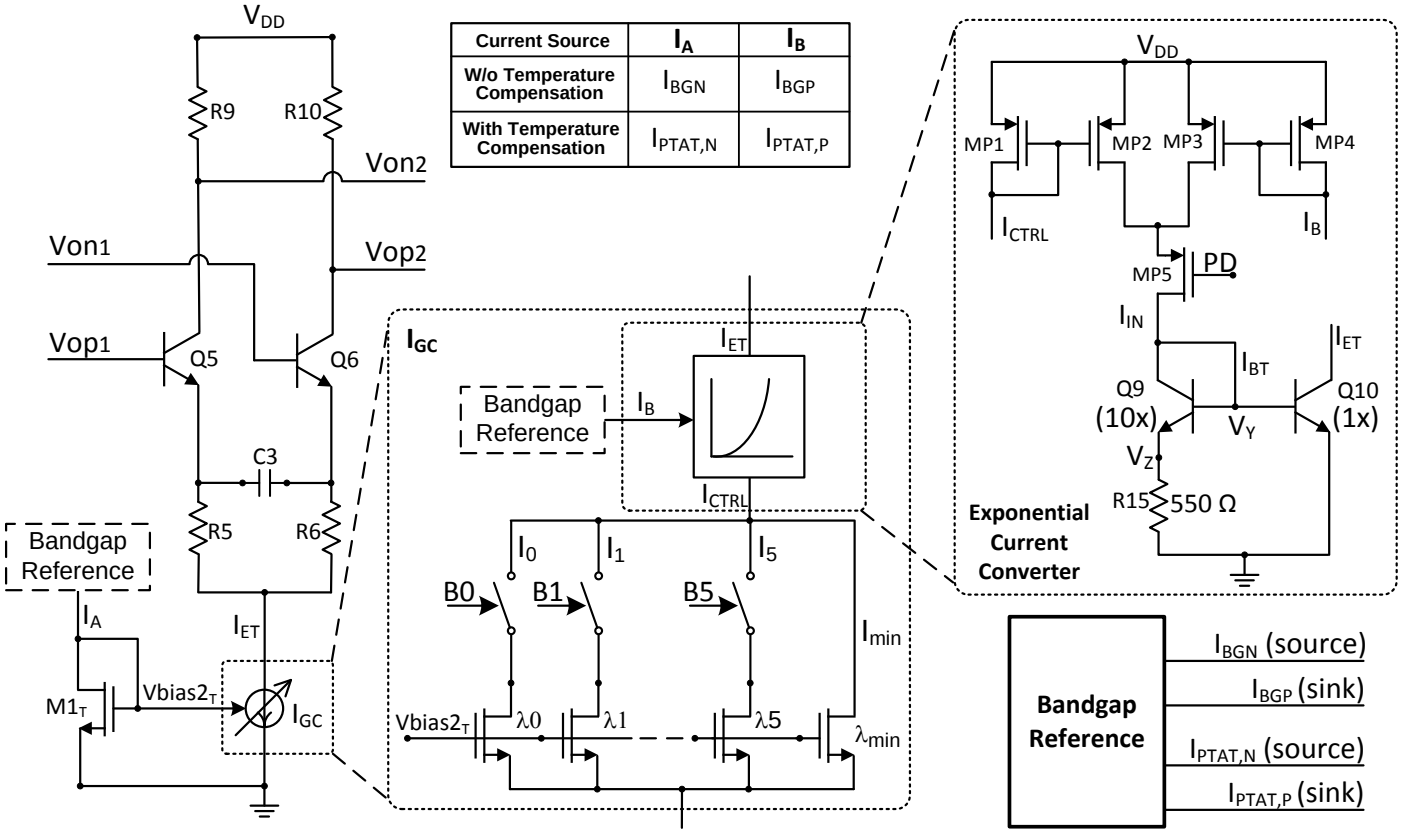

Fig. 3. Core VGA with linear-in-decibel gain control without and with temperature compensation

From (3), the gain A_v, dB is a logarithmic function of the gain control current I_{ET}.

Although the gain control block in [14] has a good temperature insensitive gain variation, it does not possess the dB-linearity characteristics. In order to increase the dynamic range and to provide a minimum error for linear-in-decibel gain variation, the above mentioned gain control block is enhanced to include an exponential current converter block as shown in Fig. 3, and the circuit performing the exponential current conversion is the proposed dB-linearizer, which converts the linear current I_{IN} to exponential gain control current I_{ET}.

The proposed dB-linearizer comprises of a bipolar transistor pair (Q9/Q10). The voltage drop across R_{15}, by neglecting I_{BT}, is given as,

$$\Delta V_{BE} = I_{IN} \cdot R_{15} = V_{BE,10} - V_{BE,9} \tag{4}$$

The exponential gain control current I_{ET} is reduced to,

$$I_{ET} = \left(\frac{I_{IN}}{10}\right) \cdot e^{\left(\frac{I_{IN} \cdot R_{15}}{V_T}\right)} \tag{5}$$

By using (2) in (3) along with $\eta \approx 1$ and $\alpha \approx 1$, the VGA gain is given as,

$$A_v, dB = 20 \cdot \log_{10}\left(\frac{I_{ET}}{V_T} \cdot R_{9,10}\right) \tag{6}$$

By using (5) in (6), we get,

$$A_v, dB = K_1 \cdot I_{IN} + 20 \cdot \log_{10}(K_2 \cdot I_{IN}) \tag{7}$$

where, $K_1 = \left(\frac{20 \cdot R_{15} \cdot \log_{10} e}{V_T}\right)$ and $K_2 = \left(\frac{R_{9,10}}{10 \cdot V_T}\right)$.

Both the terms in (7) are a function of I_{IN} and differentiating (7) by I_{IN} we get,

$$\frac{\delta A_v, dB}{\delta I_{IN}} = K_1 + \frac{20}{I_{IN} \cdot \log_e 10} \tag{8}$$

From (7) and (8), the first term indicating dB-linearity is the dominating term for the VGA gain control and the contribution of the second term is insignificant. This dB-linear gain control characteristics is emphasized by the measurement results.

This additional circuit shown in Fig. 3, introduced as the exponential current converter, using few circuit components, significantly improves the DVGA dB-linearity by consuming low DC power and small die area. Since the exponential current conversion is accomplished by using the bipolar junction transistors, the inherent temperature sensitivity of the junction potential appears and the need for the temperature compensation becomes apparent.

B. Temperature Compensation of the Gain Control Block

The DVGA (without dB-linearity) illustrated in [14] has the gain control biasing current I_{ET} derived from the bandgap reference and therefore the DVGA gain is less temperature sensitive as shown in Fig. 4.

Unlike in the proposed DVGA shown in Fig. 3, though the temperature independent currents I_{CTRL} and I_{BGP} are derived from the bandgap reference, due to the temperature dependency of the bipolar junction devices in the exponential current converter, the gain control biasing current I_{ET} eventually becomes temperature sensitive.

The low value unsalicided polysilicon resistor from the process design kit (PDK) that is used in this proposed design has very small temperature coefficient [4], and hence the variation of the resistance against temperature (T) can be neglected for the temperature analysis as,

$$\frac{\delta R_{15}}{\delta T} \approx \frac{\delta R_{9,10}}{\delta T} \approx 0 \tag{9}$$

From (5), temperature (T) variation of the biasing current is given as,

$$\frac{\delta I_{ET}}{\delta T} = \left(\frac{1}{10}\right)\cdot e^{\left(\frac{I_{IN}\cdot R_{15}}{V_T}\right)}\cdot\frac{\delta I_{IN}}{\delta T} + \left(\frac{I_{IN}\cdot R_{15}}{10\cdot V_T^2}\right)\cdot e^{\left(\frac{I_{IN}\cdot R_{15}}{V_T}\right)}\cdot\left(V_T\frac{\delta I_{IN}}{\delta T} - I_{IN}\frac{k}{q}\right) \tag{10}$$

Hence the most temperature sensitive block of the proposed DVGA is the exponential current conversion and care must be taken to nullify the temperature sensitivity of this block without further complicating the design. The condition for the temperature insensitivity is,

$$\frac{\delta I_{ET}}{\delta T} \approx 0 \tag{11}$$

As an initial assumption, if the first term of (10) is considered to be insignificant, then (11) becomes,

$$\left(\frac{I_{IN}\cdot R_{15}}{10\cdot V_T^2}\right)\cdot e^{\left(\frac{I_{IN}\cdot R_{15}}{V_T}\right)}\cdot\left(V_T\frac{\delta I_{IN}}{\delta T} - I_{IN}\frac{k}{q}\right) \approx 0 \tag{12}$$

Hence,

$$\frac{\delta I_{IN}}{\delta T} = \frac{I_{IN}}{T} \tag{13}$$

From (13), for accomplishing temperature compensation of the gain control bias current I_{ET} it is apparent that the current I_{IN} has to be derived from a proportional to absolute temperature (PTAT) current source.

By design, the bandgap reference provides temperature independent constant currents as $I_{BG,N}$ and $I_{BG,P}$ of 50 µA shown in Fig. 3. For the PTAT, currents $I_{PTAT,N}$ and $I_{PTAT,P}$ that are also derived from the bandgap reference have a constant temperature gradient of current equal to $\left(\frac{50\mu A}{274.15^{O}K}\right) = 0.182\ \mu A/K$ (also shown in Fig. 3).

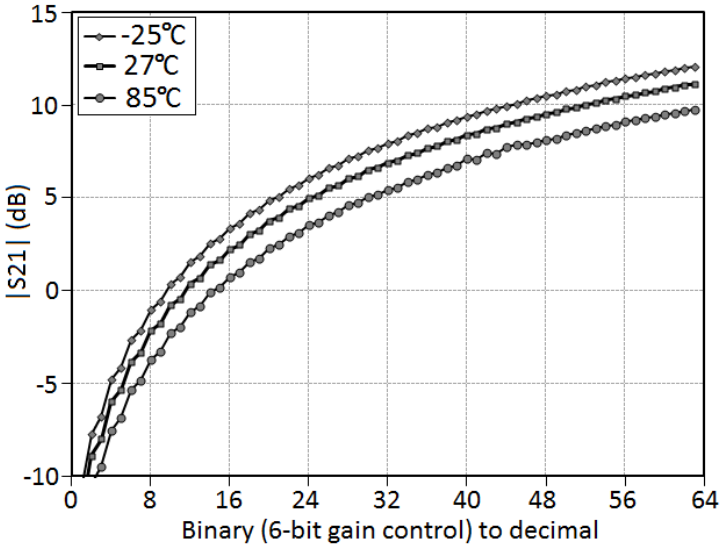

Fig. 4. Simulated gain characteristics against temperature for the DVGA without dB-Linearizer

By substituting the designed values in the first term of (10) along with V_T = 26 mV (at room temperature) and $\frac{\delta I_{IN}}{\delta T}$ = 0.182 µA/K we get,

$$\left(\frac{1}{10}\right)\cdot e^{\left(\frac{I_{IN}\cdot R_{15}}{V_T}\right)}\cdot\frac{\delta I_{IN}}{\delta T} \approx 10^{-8} \tag{14}$$

From (14), we can verify that the assumption made in (10) to arrive at (12) is valid. Hence the temperature sensitivity of the proposed dB-linearizer can be overcome by deriving the gain control current from the PTAT current source and feeding it to the exponential current converter at the specific nodes as shown in Fig. 3.

Extending the analysis further to determine the temperature effect on the overall gain of the proposed DVGA, using (5) and (6) we get,

$$\frac{\delta A_v, dB}{\delta T} = \frac{20\cdot V_T}{I_{IN}\cdot(\log_e 10)}\cdot\left(1+\frac{I_{IN}}{V_T}\cdot R_{15}\right)\cdot\frac{\delta}{\delta T}\left(\frac{I_{IN}}{V_T}\right) \tag{15}$$

The DVGA gain that is temperature compensated is obtained from (15) as,

$$\frac{\delta A_v, dB}{\delta T} = 0 \tag{16}$$

Using (16), we get,

$$\frac{\delta}{\delta T}\left(\frac{I_{IN}}{V_T}\right) = \frac{1}{V_T^2}\cdot\left(V_T\cdot\frac{\delta I_{IN}}{\delta T} - I_{IN}\cdot\frac{\delta V_T}{\delta T}\right) = 0 \tag{17}$$

As discussed previously, by using I_{IN} from the PTAT current source of bandgap reference ($I_{PTAT,N}$ and $I_{PTAT,P}$), with

(13) substituted in (17), a temperature independent DVGA gain control is accomplished and the condition in (16) is satisfied.

If we consider the scenario that the current I_{IN} is derived from the bandgap reference constant current source (I_{BGN} and I_{BGP}) with $\frac{\delta I_{IN}}{\delta T} = 0$, then (15) reduces to,

$$\frac{\delta A_v, dB}{\delta T} = \frac{20}{\log_e 10} \cdot \left(1 + \frac{I_{IN}}{V_T} \cdot R_{15}\right) \cdot \left(-\frac{1}{T}\right) \qquad (18)$$

From (18), the temperature gradient of the DVGA gain is negative and the DVGA gain decreases as the temperature increases. This is signified by the simulation plot of gain with different operating temperatures for the dB-linear DVGA (see Fig. 3) without temperature compensation as shown in Fig. 5.

The improved version of the gain control block with a linear to exponential current converter using the PTAT currents eventually improves the dB-linearity and is also insensitive to temperature variations. As shown in Fig. 5, the temperature compensation of the proposed exponential current converter is accomplished by using the currents ($I_{PTAT,N}$ and $I_{PTAT,P}$) from a PTAT current source of the bandgap reference. The rest of the amplifier, which is inherently temperature insensitive, is biased from the constant temperature insensitive currents (I_{BGN} and I_{BGP}) of the bandgap reference.

From Fig. 5, due to the small current (I_{CTRL}) involved in the minimum gain DVGA state, the majority portion of the gain control current (I_{ET}) is from the PTAT source ($I_{PTAT,P}$) directly and nullifies the temperature sensitivity of the DVGA gain better than the maximum gain DVGA state.

From this investigation we can deduce that, by incorporating the exponential current converter (using the bipolar transistors and a resistor) along with the PTAT currents, the proposed DVGA achieves a temperature compensated dB-linear gain control that occupies small die area and consumes low DC power.

C. Input Fixed-gain Amplifier with Linearizer

The input stage shown in Fig. 2 is similar to the previous DVGA design from the same authors [14] except for the inclusion of the resistors R13/R14. With this inclusion, the input stage transforms into a common base (CB) amplifier with transimpedance load circuit [15] and R13/R14 as the shunt feedback resistors for the transistor pair Q3/Q4. As the input CB stage does not possess the Miller effect, the contributing pole frequencies due to this stage along with the transimpedance load are moved farther away and the DVGA bandwidth is unaffected. This transimpedance load that apparently consumes low DC power acts as a pre-distortion linearizer in improving the DVGA linearity significantly.

The improvement in the DVGA linearity due to this transimpedance load circuit can be justified by understanding the large signal analysis as described in [14] along with the addition of shunt resistors R13/R14. The output signal

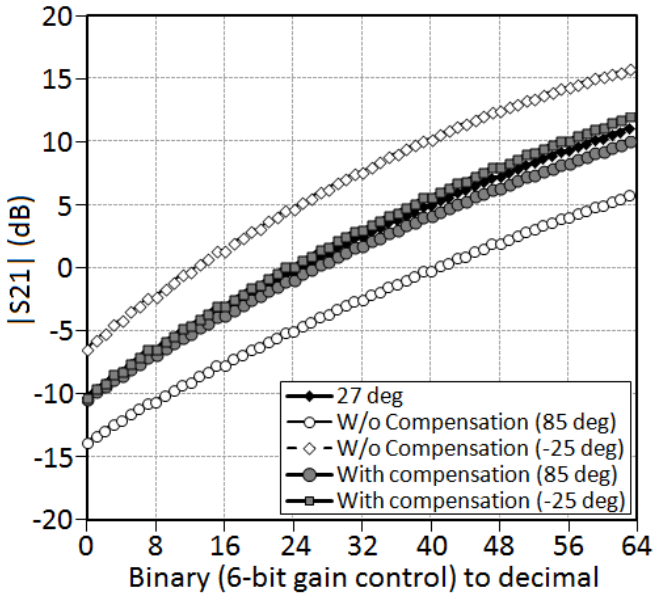

Fig. 5. Simulated gain characteristics against temperature for the DVGA using dB-Linearizer with and without temperature compensation

distortion based on the non-linearity arises due to the altering of the DC bias conditions by large voltage signal swing at the input of the DVGA stages. For simplifying the expressions in the large signal analysis, we assume that $R13 = R14 = R_f$ and $R3 = R4 = R_L$. The maximum voltage signal swing at the input of the differential transimpedance circuit is the DC voltage difference [18] and is given by,

$$\begin{aligned} V_{1p} - V_{1n} \cong & \left(R_f + R_L\right) \cdot I_{EE1} \cdot \tanh\left(\frac{V_{ip} - V_{in}}{2 \cdot V_T}\right) \\ & - \left(\frac{R_f + R_L}{\beta} + R_L\right) \cdot I_{EE2} \cdot \tanh\left(\frac{V_{1p} - V_{1n}}{2 \cdot V_T}\right) \end{aligned} \qquad (19)$$

$$\begin{aligned} V_{op1} - V_{on1} = & R_L \cdot I_{EE1} \cdot \tanh\left(\frac{V_{ip} - V_{in}}{2 \cdot V_T}\right) \\ & - \left(\frac{R_L}{\beta}\right) \cdot I_{EE2} \cdot \tanh\left(\frac{V_{1p} - V_{1n}}{2 \cdot V_T}\right) \end{aligned} \qquad (20)$$

where, β is the dc common emitter current gain of transistors.

From (19), we find that the DC voltage difference $V_{1p} - V_{1n}$ is obtained based on the input voltage $V_{ip} - V_{in}$ and by iterative subtraction. This difference voltage $V_{1p} - V_{1n}$ gradually settles and the final difference output voltage is computed as shown in (20). The subtraction terms based on $V_{1p} - V_{1n}$ in (19) and also in (20) are originated due to the negative feedback offered by the transimpedance stage and hence provides a regulation of the DC voltages. Therefore the transimpedance stage performs the pre-distortion linearization by stabilizing the bias point of the VGA core. The contribution of the transimpedance circuit on the linearity and also the stability is determined by the current I_{EE2} controlled by the M3 NMOS current source. By introducing the shunt feedback

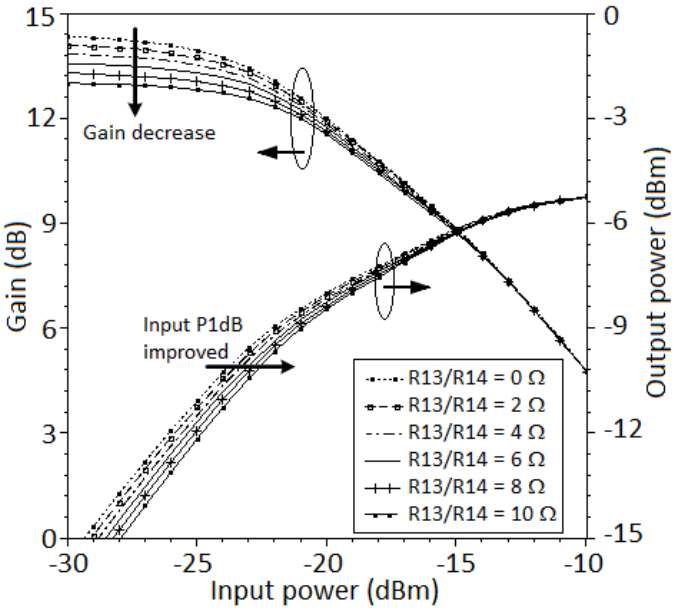

Fig. 6. Simulated DVGA linearity with varying R13/R14 resistors of the Transimpedance load linearizer at 1 GHz frequency

resistor R_f, without affecting the DC power consumption, an additional improvement of the DVGA linearity is achieved over [14] for the whole gain range and is evident from experimental results shown in Table I. In addition to the linearity improvement discussed in [14], the resistors R13/R14 introduced as a part of the transimpedance load circuit contributes further in improving the linearity of the proposed DVGA. This can be explained using the simulation plot shown in Fig. 6 by varying the resistors R13/R14 from 0 Ω to 10 Ω for maximum gain state. We observe that, as the resistor value increases, there is a decrease in gain and a corresponding increase in the input P1dB with the output P1dB unchanged. This characteristics is similar to the linearity improvement illustrated in [14] and the linearity is further improved without any additional power consumption and significant die area.

D. DC Offset Canceller (DCOC)

The DC offset canceller of the proposed DVGA can be considered as the partial AC coupling DCOC using the low-loss high pass filter (HPF). Unlike for the AC coupling that requires large capacitors between each stage to achieve cutoff frequency closer to DC, the DCOC in the proposed DVGA alleviates the need for a large capacitor value by choosing a large HPF resistor value to achieve the lower cutoff frequency with smaller capacitor. The resistor of the HPF is in parallel with the input impedance of the emitter follower buffer which is large and hence the desired cutoff frequency is determined by the parallel resistance combination. The large HPF resistor, other than minimizing the capacitor size, also provides biasing for the common-collector (CC) buffer stage. The design of the HPF in the DCOC is explained in the sub-section F along with the CMFB circuit design.

Inherently, the DCOC design is simplified for the bipolar differential pairs and hence the proposed design is based on only one DCOC stage between the final two DVGA stages. This cancels the DC offset from propagating further, unlike for the CMOS multi-stage VGAs wherein the DCOC is applied to each stage to avoid saturation at any of the output stages [30]. The DCOC in the proposed DVGA can suppress most of the offset generated or propagated along the signal path with a low cutoff frequency and large gain roll off. Although the DCOC occupies nearly 50% die area of the proposed DVGA, the overall core DVGA area is only 160 µm x 300 µm.

E. Buffer with Common Mode Feedback (CMFB)

The output differential buffer stage of the proposed DCOC DVGA design incorporates the CMFB that enforces the output common mode voltage to a fixed value. The proposed DVGA ascertains both the input and output common mode voltages to predetermined values by using the input fixed gain amplifier and the output CMFB respectively, ensuring that the DVGA biasing is stable and gain-independent.

The CMFB, as shown in Fig. 2, is self regulating based on the voltage V_{CM} set by the emitter follower bias current I_{bias}. The gate currents of the MOS transistors M5 and M6 and eventually the voltage drop across the resistors R7 and R8 are negligible. This results in a back-to-back diode-connected MOS transistor configuration that operates in the saturation mode and sets the DC voltage equal to V_{CM} by averaging the output voltages V_{on} and V_{op} as,

$$V_{CM} = \sqrt{\frac{2 \cdot I_{bias}}{\beta_N}} + V_{THN} \tag{21}$$

where, $\beta_N = \mu_n \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_N$ with μ_n, C_{ox}, $\left(\frac{W}{L}\right)_N$ and V_{THN} are the electron mobility, gate oxide capacitance per unit area, aspect ratio, and threshold voltage of the NMOS transistors M5/M6, respectively.

This CMFB provides a wideband 50 Ω output resistive matching that is independent of the resistance value R7/R8 and is equivalent to the parallel combination of the reciprocal of the M5 and M6 NMOS transconductance as,

$$Z_{OUT} = \frac{1}{g_{mN5}} \| \frac{1}{g_{mN6}} \tag{22}$$

where, g_{mN5} and g_{mN6} are the transconductance of the M5 and M6 NMOS transistors, respectively.

The transistor M7 is introduced in the design to switch OFF M5 and M6 active loads of the emitter follower buffer during the *power down* mode.

F. Design of DCOC and CMFB of the proposed design

Figure 7 shows the circuit schematic and the half circuit equivalent of the output buffer with the DCOC and CMFB.

Step 1: Determining aspect ratio of NMOS M5/M6

A large common mode voltage (V_{OCM}) is avoided that may shut off the transistor pair Q7/Q8. Since the gate current I_X shown in Fig. 7 is negligible, the voltage drop across resistors

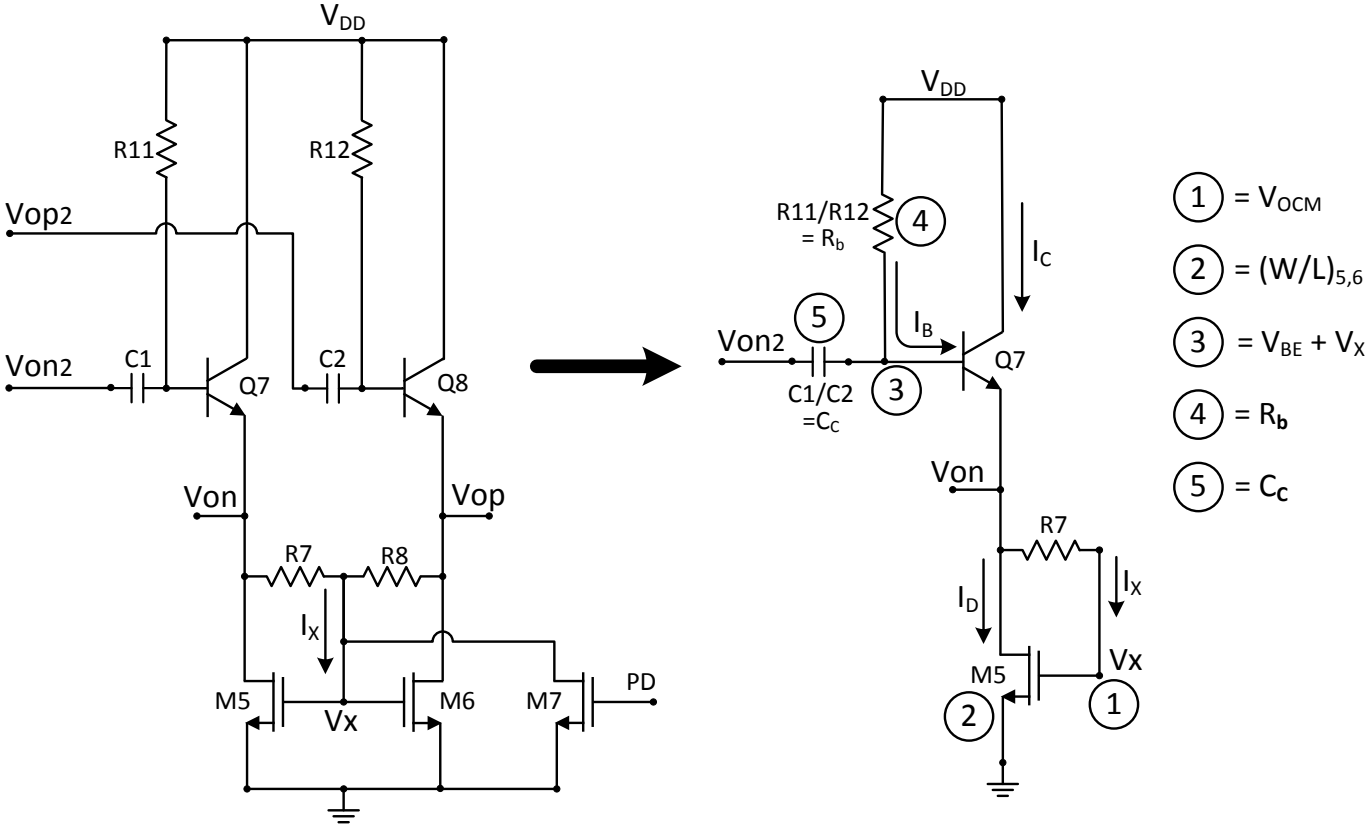

Fig. 7. Output Buffer stage with DC offset canceller (DCOC) and common mode feedback (CMFB) design

R7/R8 is negligible and the V_{OCM} voltage becomes the gate-source voltage V_X of the NMOS pair M5/M6. This results in the diode-connected transistors M5/M6 to be operating in the saturation region. By knowing the optimum operating currents I_B and I_C of the transistors Q7/Q8, the aspect ratio for M5/M6 can be obtained as,

$$\left(\frac{W}{L}\right)_{5,6} = \frac{2 \cdot I_D}{K_{Pn} \cdot \left(V_X - V_{THN}\right)^2} \approx \frac{66\mu m}{1\mu m} \tag{23}$$

Step 2: Determine resistance for output buffer biasing

The base voltage for biasing the transistors Q7/Q8, by neglecting the voltage drop across R7/R8, is $V_{BE} + V_X$. R11/R12 are used for biasing the output differential buffer and form a part of the DCOC HPF design.

$$R_b = \frac{V_{DD} - \left(V_{BE} + V_X\right)}{I_B} \approx 11\,k\Omega \tag{24}$$

Step 3: DCOC HPF design

The effective parallel resistance between R_b and the input resistance $\left(R_{in}\right)$ of the output buffer along with the C_C capacitor forms the DCOC HPF design. The filter cutoff frequency is given by f_{P1}. For practical design consideration based on $\left(R_L << R_b << R_{in}\right)$, we can neglect R_{in} and R_L values, and the DCOC capacitor value is obtained as,

$$C_C \cong \frac{1}{2\pi \cdot f_{P1} \cdot \left(R_b\right)} \approx 10\,pF \tag{25}$$

G. DVGA Power Shutdown

The proposed DVGA is designed for low power application, by consuming minimum DC power and with a provision of the *power down* mode, during which the non-functional DVGA in the transceiver system can be turned OFF, using a digital control pin (PD/PwrDwn). The DC current dissipated is insignificant when the *power down* mode of the DVGA is active. By using the *power down* mode digital control pin , the simulation settling time of the proposed DVGA switching from OFF (*power down* mode) to ON (normal mode) state is 1.5 µs and ON to OFF state is 0.5 µs as shown in Fig. 8.

IV. Small Signal Analysis

To understand the frequency response of the proposed DVGA, we consider the half circuit AC equivalent of the CE variable gain stage (VGA core) as shown in Fig. 9 (a) and the hybrid-π model in Fig. 9 (b). The contribution of the input CB (fixed gain amplifier) and the output CC (buffer) stages on the frequency response can be ignored [14]. Since the peaking capacitor is connected between the emitters of the CE stage, for half circuit implementation the value of $2\times C3$ is considered [15]. R_{in} represents the input resistance of the emitter follower buffer.

The frequency response shown in Fig. 10 is due to the dominant poles and zeroes from the DCOC and the gain-peaking capacitor, C_P. At low frequency, the contribution of the parasitic capacitors (C_π and C_μ) can be neglected to obtain the low frequency small signal gain equation (26)

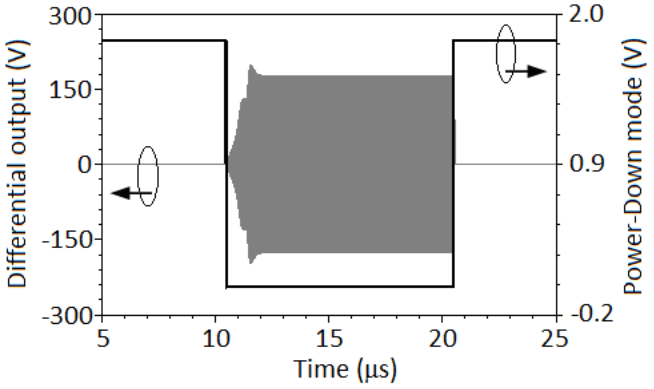

Fig. 8. Simulated DVGA switching time

shown in bottom of the page. The low frequency poles and zeroes obtained from (26) are,

$$f_{Z1} = \frac{\omega_{Z1}}{2\pi} = 0 \tag{27}$$

$$f_{P1} = \frac{1}{2\pi \cdot C_C \cdot \left[\left(R_b \parallel R_{in}\right) + R_L\right]} \approx 1.4 \times 10^6\ Hz \tag{28}$$

$$f_{Z2} = \frac{1}{2\pi \cdot R_E \cdot C_P} \approx 1.3 \times 10^9\ Hz \tag{29}$$

$$f_{P2} = \frac{1}{2\pi \cdot C_P \cdot \left[R_E \parallel \left(r_\pi + r_b\right)/\left(\beta + 1\right)\right]} \approx 1.6 \times 10^9\ Hz \tag{30}$$

The zero f_{Z1} provides the initial launch (with a gain slope = +20-dB/decade) of the gain plot with a high pass filter response until the pole frequency f_{P1} is reached. Then, the mid-band flat response with gain A_{v0} proceeds towards the

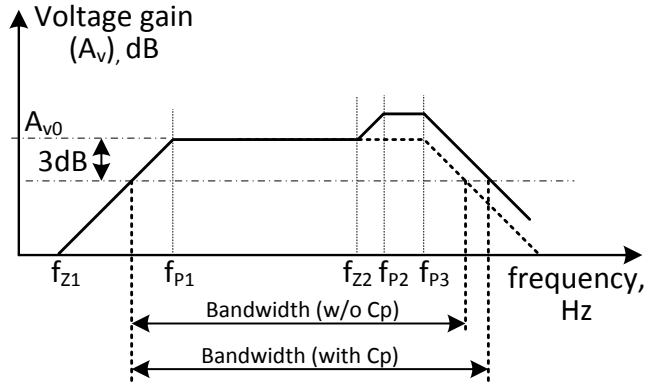

Fig. 10. DVGA frequency response

high frequency pole (along the dashed line) at f_{P3} (without the peaking capacitor C_P). The parasitic capacitors (C_π and C_μ) of the transistor pair Q5/Q6 and the interconnects then drops the gain at high frequency from f_{P3} onwards as given in (31).

$$f_{P3} = \frac{1}{2\pi \cdot \left[C_\pi + C_\mu \cdot \left\{1 + g_m \cdot \left(R_b \parallel R_L \parallel R_{in}\right)\right\}\right] \cdot \left(r_\pi \parallel r_b\right)} \approx 1.8 \times 10^9\ Hz \tag{31}$$

Due to the peaking capacitor C_P, an additional zero is introduced at f_{Z2} that initiates the peaking and the parasitic capacitors of the transistor pair Q5/Q6 with the interconnects then drops the gain from f_{P3} (31) onwards. The contribution of the pole at f_{P2} depends on the value of the parasitic resistances (r_π and r_b) of the transistors and eventually rolls-

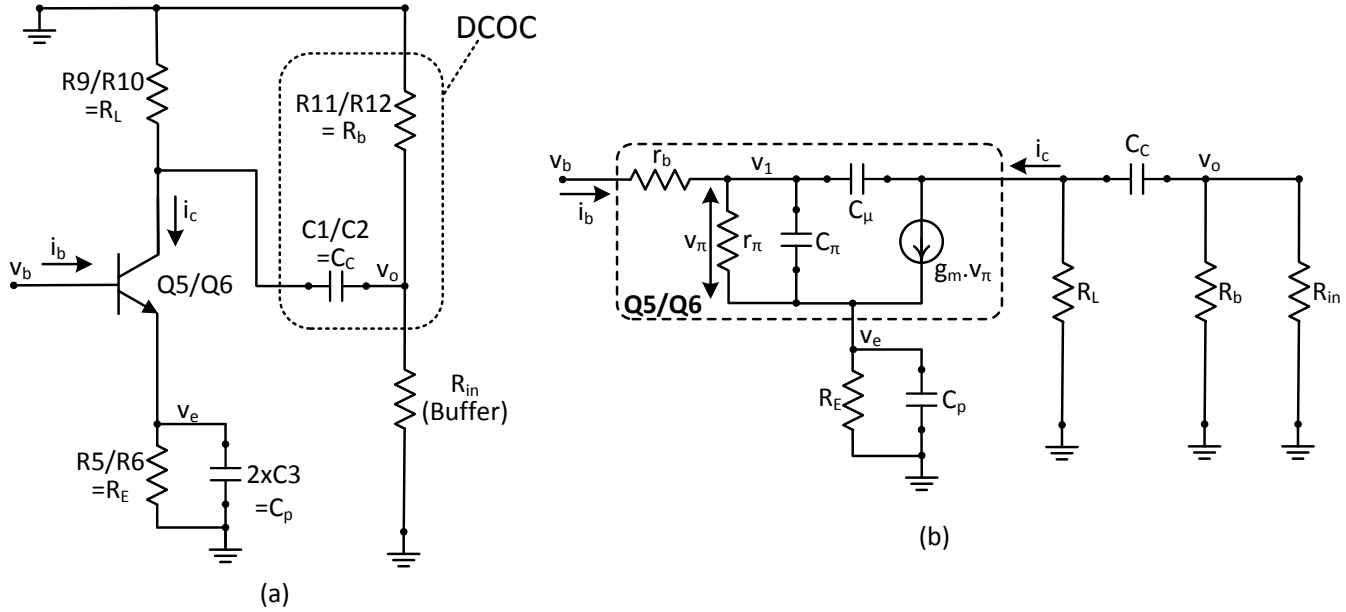

Fig. 9. Half circuit of the CE amplifier stage with DCOC (a) AC equivalent circuit (b) hybrid-π model of the BJT

$$A_v(s) = \frac{v_O}{v_b} = \frac{\left(-g_m\right) \cdot \left(R_b \parallel R_L \parallel R_{in}\right) \cdot s \cdot \left(s + \dfrac{1}{R_E \cdot C_P}\right)}{s^2 + s \cdot \left[\dfrac{1}{C_P \cdot \left\{R_E \parallel \left(r_\pi + r_b\right)/\left(\beta + 1\right)\right\}} + \dfrac{1}{C_C \cdot \left(R_b \parallel R_{in} + R_L\right)}\right] + \dfrac{1}{C_P \cdot R_E \cdot C_C \cdot \left(R_b \parallel R_{in} + R_L\right)}} \tag{26}$$

off the gain into the stop band. As a result of incorporating the peaking capacitor C_P, an increase in the 3-dB bandwidth of the proposed DVGA at the upper cutoff frequency is observed as shown in Fig. 10. The bandwidth extension, due to the peaking capacitor, based on simulation is from 1.8 GHz to 2.45 GHz and is observed only for the DVGA maximum gain mode.

However the lower cutoff frequency of the DVGA is determined by the pole at f_{P1}, which depends on the DCOC components and the input resistance of the output buffer, R_{in}. The pole at f_{P1} can be moved to a lower frequency by either increasing C_C at the cost of die area or by increasing R_b (limited by R_{in}) that may affect the biasing of the output buffer or by increasing R_L which by (31) may reduce the upper cutoff frequency, f_{P3} of the DVGA.

V. Experimental Results

The proposed temperature compensated dB-linear DVGA with DCOC design is realized using a 0.18 µm SiGe BiCMOS process from Tower Jazz Semiconductors. The DVGA core die area is 160 µm × 300 µm and the overall area including the probing pads is 1.01 mm × 0.83 mm. The microphotograph of the proposed DVGA in the wafer is shown in Fig. 11. The performance of the DVGA is experimentally verified by means of on-wafer probing with the Agilent E8364B PNA Network Analyzer and HP 8970B Noise Figure meter. The DVGA, during its normal operation, consumes a DC current from 6.1 mA to 6.8 mA depending on the gain, and during the *power down* mode, it dissipates a DC current of 310 µA from a supply voltage of 1.8 V.

The measurement system consists of a wafer probe station with RF GSSG probes for probing the DVGA differential input and output, along with a 7-pin DC probe that provides 6-bit digital gain control (B_5~B_0) and a pair of individual DC probes for the VDD supply voltage and the *power down* mode control (PwrDwn).

The proposed DVGA using the gain-control block with the exponential current converter has better dB-linear transfer characteristics, and this is implied in the measured gain characteristics against the simulation result as shown in Fig. 12 plotted against the 6-bit digital gain control input with B_5 as most significant bit and B_0 as the least significant bit. The plot shown in Fig. 12 suggests that the gain step error is minimized at the extremes of the DVGA gain range providing uniform gain steps. The proposed DVGA achieves dB-linearity over the entire gain range and the operating bandwidth as shown in Fig. 13. The gradual drop in the measured gain as compared to the simulation result is observed for the DVGA gain setting towards the maximum gain. This gain drop can be accounted for the smaller actual transistor β against the modeled value of Q9 and Q10 transistor (See Fig. 3) at large collector current. The upper cut-off frequency increases from 1.9 GHz to 2.3 GHz as the DVGA gain changes from low gain to high gain mode. The bandwidth extension is observed at high gain mode

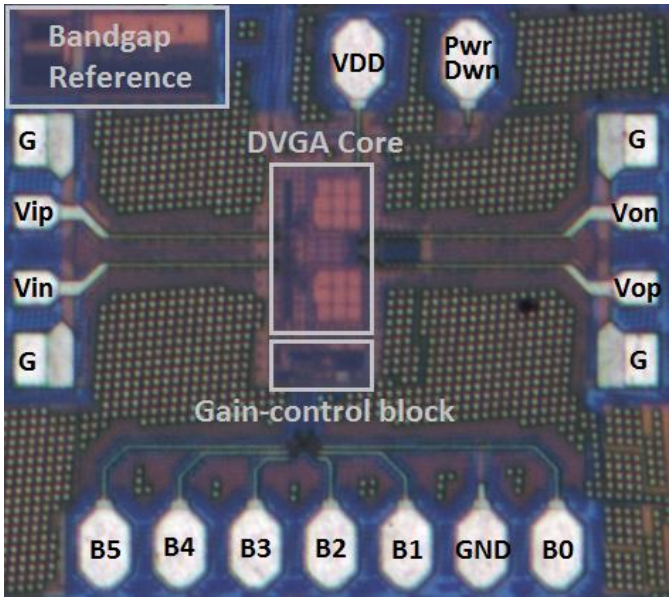

Fig. 11. DVGA microphotograph with bandgap reference and measurement pads (core area: 160 µm × 300 µm, total area: 1.01 mm × 0.83 mm)

due to the Early effect of the Q10 transistor (See Fig. 3) with larger collector current as compared to the low gain mode. The variation of measured DVGA gain and noise figure are complementary against the digital gain control input, as shown in Fig. 12, that is measured at 0.9 GHz frequency. The measured noise figure (NF) plot against frequency, as shown in Fig. 14, suggests that the variation of NF with gain control input, unlike the gain steps, is not uniform and is mainly due to the fixed gain input stage amplifier [14] that suppresses the following DVGA stages' noise contributions until the gain control input sets the overall DVGA to start attenuating. The noise figure measurement start frequency is 0.3 GHz and it is limited by the noise source and the remote receiver module of the noise figure measurement system.

The measured gain variation against digital gain control code over different temperatures, as shown in Fig. 15, suggests

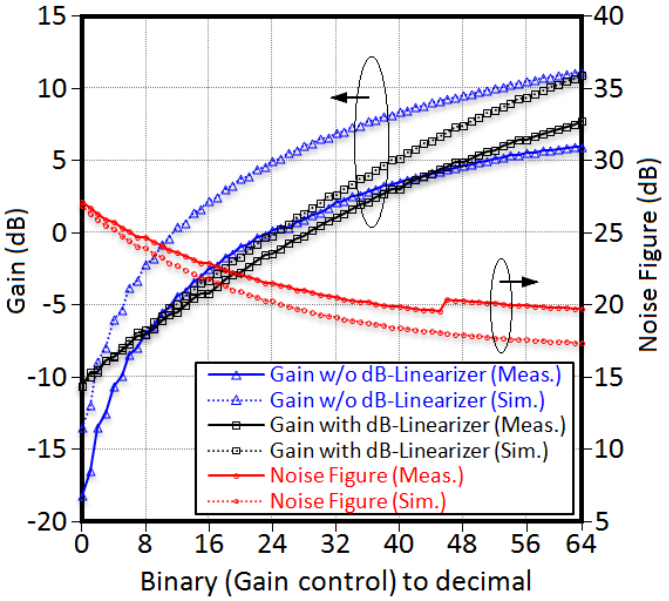

Fig. 12. Simulated and measured DVGA gain dB-Linear characteristics and noise figure with dB-Linearizer at 0.9 GHz frequency

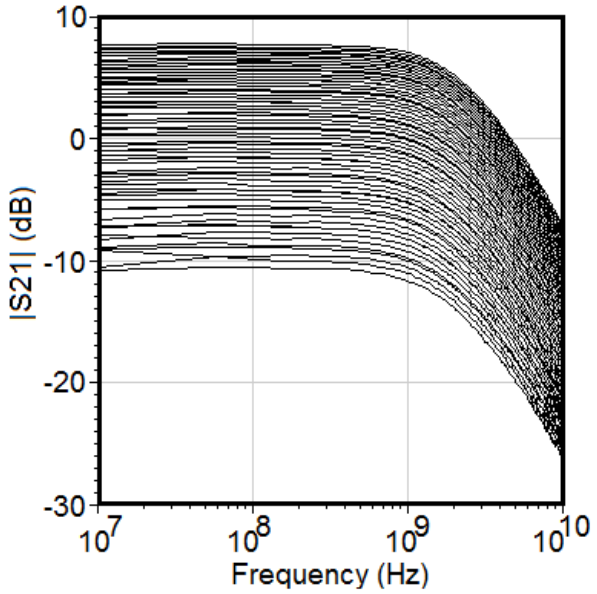

Fig. 13. Measured DVGA gain plot for all the 64 gain steps

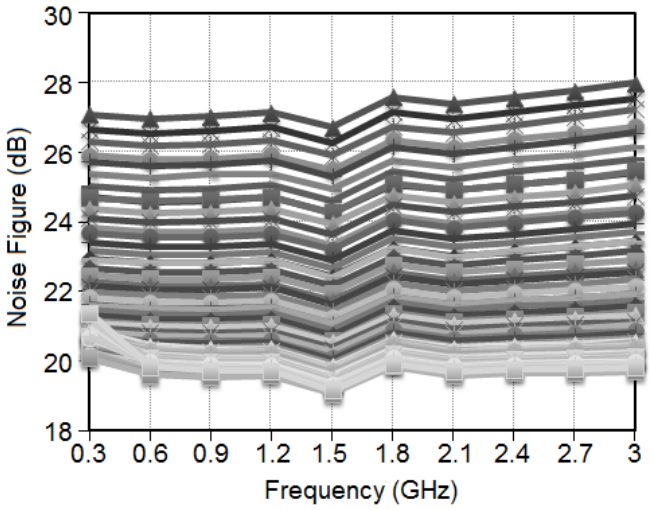

Fig. 14. Measured DVGA noise figure for all the 64 gain steps

that the proposed temperature compensation technique improves the gain insensitivity for temperature variations as ascertained in Section II and predicted by the simulation results (shown in Fig. 5).

The gain compression in the proposed DVGA topology is determined by the VGA core. Fig. 16 shows the variable gain control obtained by adjusting the bias current (I_{ET}). Based on Fig. 16, the VGA core is normally operated in the dark gray region (between points B and C), which is the linear region for the small signal input. As the input RF signal amplitude increases and the VGA gain is set to high gain mode (bias point is at B), the VGA core approaches the non-linear region or the gain compression region (light gray region, from point B towards point A) based on the positive peak of the RF signal riding over the I_{max} bias point (point B). Conversely, for the VGA minimum gain setting, the VGA enters the non-linear region (light gray region, from point C towards point D) based on the negative peak of the RF signal wave over the I_{min} bias

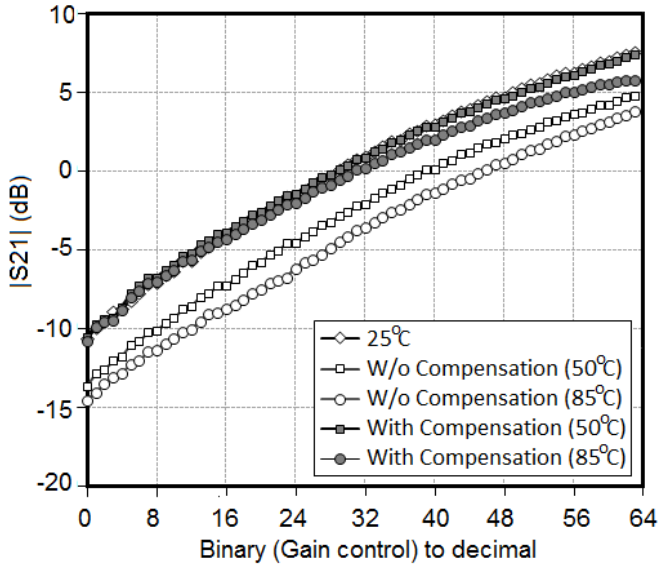

Fig. 15. Measured gain characteristics against temperature for the DVGA using dB-Linearizer with and without temperature compensation

point (point C) as shown in Fig. 16. The margin between the I_{max} (point B) and the point at which the VGA core transistors saturate (point A) determines the input P1dB for the maximum gain mode and similarly, the gap between I_{min} (point C) and the point at which the VGA core transistors goes into cut-off region (point D) determines the input P1dB for the minimum gain mode. Accordingly, for the proposed DVGA as shown in Fig. 17 and Fig. 18, there is a possibility that the input P1dB is almost the same for both the maximum and the minimum gain setting, and the gain difference for the maximum and the minimum gain setting is reflected in the output P1dB.

The fixed gain wideband low input impedance CB stage and the low output impedance CC buffer provides excellent wideband matching to 50 Ω resistance as shown in Fig. 19. The input return loss is better than 12 dB and the output return

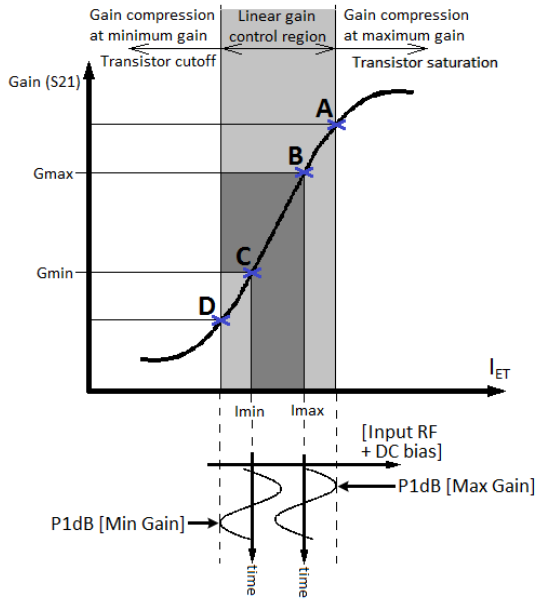

Fig. 16. VGA gain characteristics against the gain control bias current

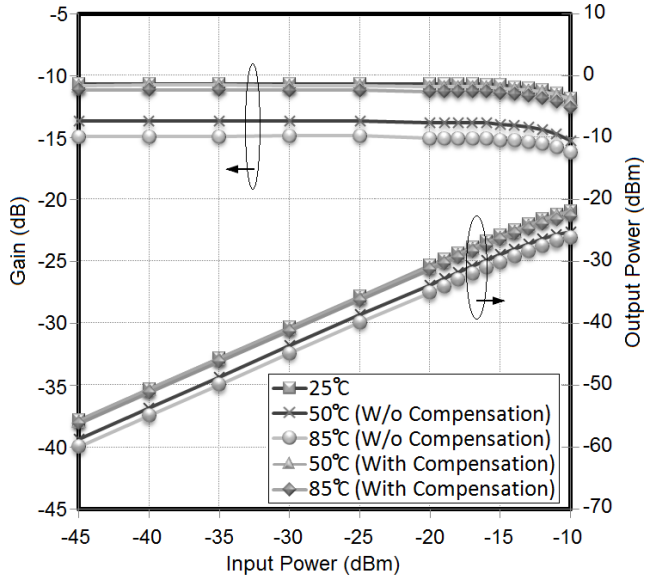

Fig. 17. Measured P1dB plot for minimum DVGA gain against temperature

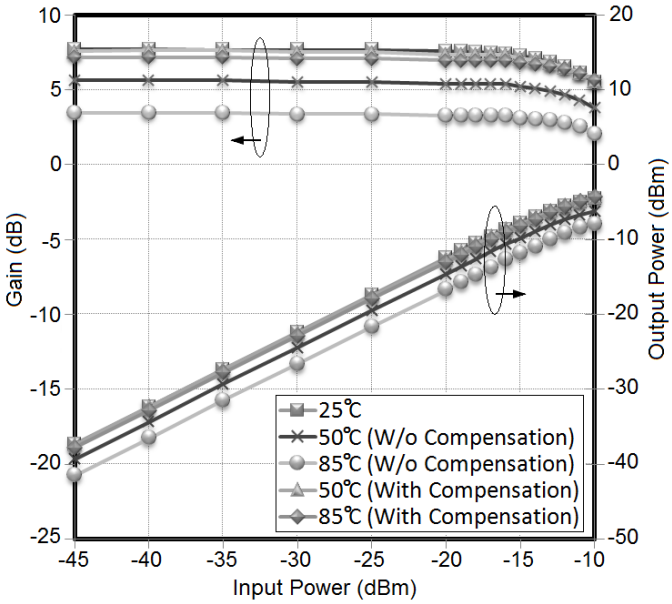

Fig. 18. Measured P1dB plot for maximum DVGA gain against temperature

loss is better than 16 dB over the entire gain and frequency range of the proposed DVGA.

The lower limit on the frequency range of the S-parameter measurement is set by the Agilent E8364B PNA at 10 MHz. To prove the validity of the proposed DCOC design on the DVGA lower cutoff frequency, the low frequency DVGA gain measurement is accomplished by using the RoHS SMBV100A signal generator and the Agilent E4407B ESA-E series spectrum analyzer. The measurement plot was obtained from 1 MHz to 10 MHz for both maximum and minimum DVGA gain control input as shown in Fig. 20, by nullifying the cable and equipment losses. By comparing the plots in Fig. 13 and Fig. 20, we find that the maximum and minimum DVGA gain at 10 MHz frequency are correspondingly the same, suggesting that the proposed low frequency gain measurement technique is consistent with the S-parameter measurement using PNA. Based on the differential gain plot in Fig. 21, the simulated gain roll-off at DVGA lower cutoff frequency is 20 dB/decade

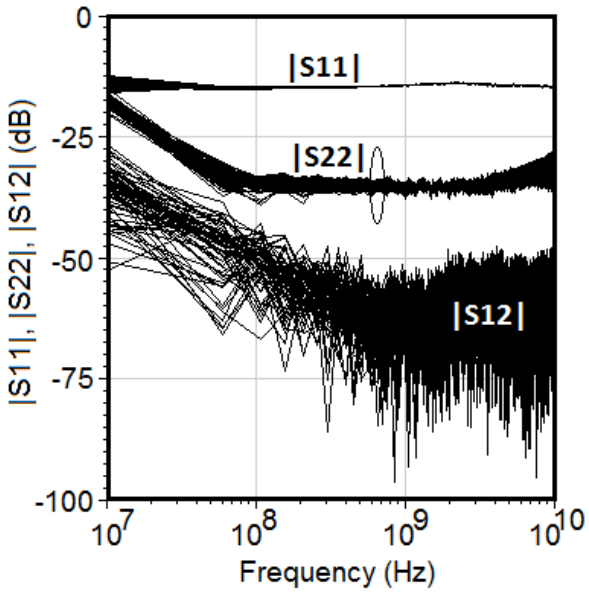

Fig. 19. Measured DVGA input/output return loss and reverse gain for all the 64 gain steps

for both maximum and minimum DVGA gain. By extrapolating the curves (as determined in [12] and [30]) towards DC (f = 0 Hz), which is 6 decades in the backward direction, we can estimate the DC offset rejection for the proposed DCOC DVGA to be large. From the Fig. 21, we can infer that the return loss of the DVGA is improved in measurement similar to the simulation result for the entire operating frequency range.

By careful physical layout design of the proposed DCOC DVGA, ensuring symmetry along the differential RF path, the measured DC offset at the differential output due to mismatch is measured to be within ±2 mV. In this proposed DVGA design, the CMFB circuit also contributes to the suppression of the output DC offset. In addition, the ability of the proposed DCOC to reject the DC offset voltage injected at the input (by using the Bias-Tee) is verified by the measurement plot shown in Fig. 22. We observe that for both maximum and minimum DVGA gain, with ±200 mV input DC offset, the output DC offset is < ±3 mV. The proposed DCOC has better DC offset rejection as compared to [11] and [30], that measures maximum input DC offset of 100 mV and 120 mV, respectively with output DC offset of 18 mV and 14 mV, respectively.

The overall performance of the proposed DVGA is compared with the state-of-the-art VGA designs and is compiled in Table I. The proposed DVGA design, without significantly increasing the circuit complexity, simultaneously has the on-chip DCOC, the dB-linearity and the temperature compensation. These three characteristics are desirable for the integration of the VGA design in the SoC for low cost consumer applications requiring good gain control precision. Moreover, the proposed DVGA has the design advantage of the overall high linearity performance, wide multi-decade bandwidth, with low power consumption and compact die area unlike the design works published in [7] and [8].

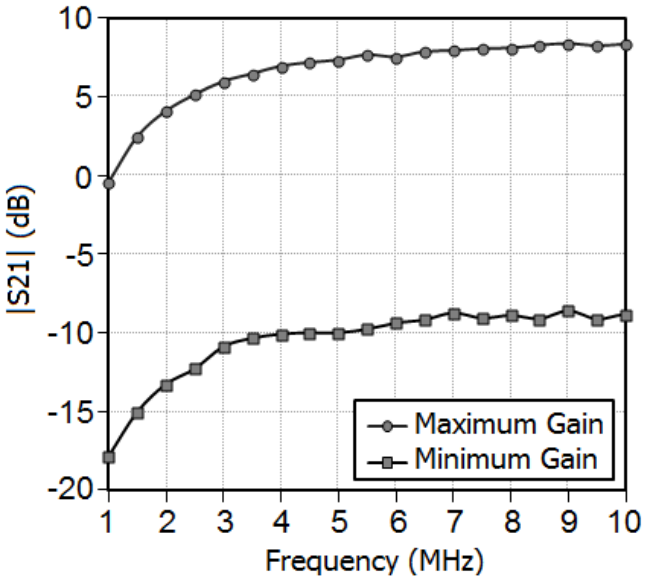

Fig. 20. Measured low frequency gain plot for maximum and minimum DVGA gain

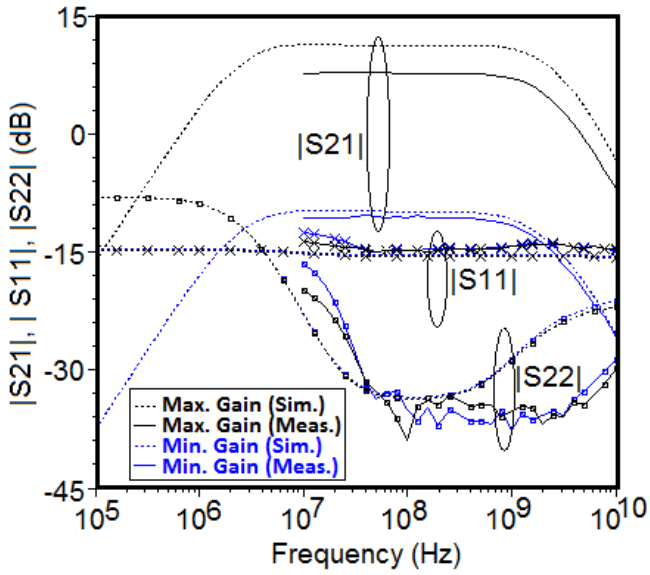

Fig. 21. Measured and simulated gain and return loss plot for maximum and minimum DVGA gain

VI. Conclusion

This paper presents a compact digitally controlled variable gain amplifier (DVGA) using SiGe BiCMOS technology with a temperature compensated dB-linear gain control and a DC offset cancellation technique. The proposed DVGA is aimed for commercial applications taking into consideration the low cost, low power consumption, PVT insensitivity, dB-linearity, power shutdown mode control, stability, and improved linearity. A comprehensive analysis investigating the proposed DVGA for dB-linear digital gain control, temperature compensation, pre-distortion linearization, and DC offset compensation is provided and verified by both simulation and experiment. The measured DVGA achieves a gain range of 18.4 dB, a 3-dB bandwidth from 2 MHz to 1.9 GHz with a ±0.75 dB gain flatness from 2.75 MHz to 1.2 GHz, an input 1-dB gain compression point better than -12.5 dBm, an input return loss better than 12 dB, an output return loss better than 16 dB and a maximum DC power consumption of 12.2 mW from a 1.8 V supply. The core DVGA, excluding the I/O measurement pads, occupies a die area of 160 µm x 300 µm.

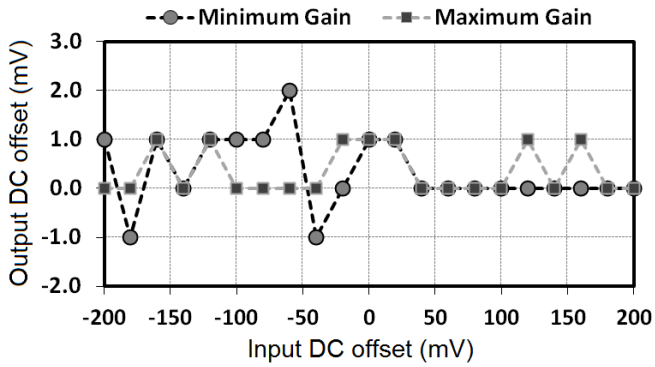

Fig. 22. Measured DVGA DC offset

Acknowledgment

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TABLE I

PERFORMANCE SUMMARY OF VARIABLE GAIN AMPLIFIERS

Reference	Technology	Gain Control	-3dB Bandwidth [Hz]	Gain Range [dB]	Input P1dB [dBm]	On-chip DCOC	dB-linearity	T.C.†	Noise Figure [dB]	Power [mW]	Active Area [mm x mm]
[8]	0.18 μm CMOS	Analog	4M to 0.9 G	-38.8 to 55.3	-10.8 to -59.1	Yes	Yes	Yes	6.8 **	20.5	0.195 ***
[11]	90 nm CMOS	Analog	0.1 M to 2.2 G	-10 to 50	-13 to -55	Yes	No	No	17 to 30	2.5	0.014 ***
[19]	0.18 μm CMOS	Analog	0.4 M to 2 G	-16 to 34	-	Yes	No	No	-	40	0.7
[20]	0.18 μm CMOS	Analog	32 M to 1.05 G	-52 to 43	-17 to -48	No	Yes	Yes	-	6.5	0.4 ***
[21]	0.18 μm CMOS	Analog	380 M to 2.2 G	-13.5 to 13.5	-5 *	No	Yes	No	6.5 to 28.6	19.8	0.108 ***
[22]	0.18 μm CMOS	Analog	430 M to 2.33 G	-3.3 to 9.5	-9 *	Yes	Yes	No	6.3 to 7.9	16.2	0.409
[23]	0.18 μm CMOS	Digital	30 M to 1.4 G	-6.5 to 15.5	-	Yes	Yes	No	5.8 to 17.5	6.5	0.034 ***
[24]	0.18 μm CMOS	Digital	48 M to 0.86 G	-34 to 16	+11 to -15	Yes	Yes	No	2.4 to 24.5	30.6	0.25
[25]	90 nm CMOS	Digital	0.8 G	-29 to 23	-26 to -15	No	No	No	-	16.8	0.04
[26]	90 nm CMOS	Digital	0.29 G	28 to 46	-6	No	Yes	No	-	14	0.03 ***
[27]	0.13 μm CMOS	Fixed	3 G to 9.4 G	12 (fixed gain)	-6	No	-	No	3.3	30	0.83
[28]	0.13 μm CMOS	Digital	0.8 G to 9 G	0 to 2.5	+1.0	No	Yes	No	9.5	40	1.5
[7]	0.13 μm SiGe	Analog	0. 2 M to 7.5 G	-10 to 30	-	Yes	Yes	Yes	-	72	1.0
[29]	0.18 μm SiGe	Analog	0.2 G to 2.5 G	50	-	Yes	Yes	No	-	102	1.8
[14]	0.18 μm SiGe	Digital	DC to 5.6 G	-16.5 to +6.5	-17 to -27	No	No	Yes	16.5 to 27.1	7.9	0.01 ***
This work	**0.18 μm SiGe**	**Digital**	**2 M to 1.9 G**	**-10.6 to +7.8**	**-11 to -12.5**	**Yes**	**Yes**	**Yes**	**21.4 to 27.1**	**12.2**	**0.048** ***

* minimum measured P1dB ** simulation noise figure
*** Core die area (excluding I/O pads) † Temperature Compensation

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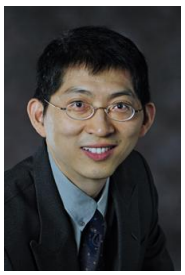

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