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Electrolyte-gated neuromorphic transistors for brain-like dynamic computing

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ABSTRACT

In recent years, the rapid increase in the data volume to be processed has led to urgent requirements for highly efficient computing paradigms. Brain-like computing that mimics the way the biological brain processes information has attracted growing interest due to extremely high energy efficiency. Particularly, dynamics play an essential role in neural spike information processing. Here, we offer a brief review and perspective in the field of electrolyte-gated neuromorphic transistors for brain-like dynamic computing. We first introduce the biological foundation of dynamic neural functions. Then dynamic synaptic plasticity, dynamic dendritic integration, dynamic neural functions, and bio-inspired somatosensory systems realized based on the electrolyte-gated neuromorphic transistors are presented. At last, conclusions and perspectives are given.

I. INTRODUCTION

The digital computer relies on the Boolean logic and the von Neumann architecture, and its performance improvement depends on the scaling of the complementary metal–oxide–semiconductor (CMOS) transistor via Moore's law. The increase in the energy density and the upcoming physical limit have slowed down the scaling trend. In addition to scaling difficulties, the physical separation between the processor and the memory and their performance mismatch in the von Neumann architecture result in a large amount of energy consumption and latency.

Our brain is an extremely energy-efficient computing system that combines computation and storage with a low power consumption of ∼20 W.[1] In the past few decades, brain-inspired computing has attracted a wide range of research interests.[2–7] At the software level, artificial neural networks based on deep learning algorithms have realized a wide range of achievements.[8] Algorithms running on the von Neumann architecture still serially perform the calculation, which is energy and time inefficient. At the hardware level, brain-inspired circuits based on CMOS technology require a large number of transistors to emulate a synapse or a neuron.[9] The human brain consists of $\sim 10^{11}$ neurons and $\sim 10^{15}$ synapses.[10,11] The hardware implementation of artificial synapses and neurons at the device level followed by bottom-up engineering is a highly promising way for brain-inspired computation.[12–17] Several technical routes including two-terminal devices and multi-terminal transistors have made great progress in artificial synaptic and neuronal devices and hardware neural networks.[18–28]

The ability of two-terminal memristive devices to alter their conductance according to the external stimuli is similar to the ability of synapses to change their connection strength (synaptic weight, W).[18,29] When arranged into crossbar arrays, in-memory computing can accelerate the training and inference process of artificial neural networks.[13,30] In-memory computing requires the device to exhibit linear and symmetric conductance modulation, high endurance, low switching noise, long-time retention, etc.[4] However, two-terminal devices usually behave non-ideal device characteristics and their crossbar arrays usually suffer from the sneak path current issues.[30,31] Compared with resistive coupling two-terminal devices, capacitive coupling transistors have a lower static power consumption and can emulate the neural functions better.[32] With a gate (G) control, the transistor can inherently

suppress the sneak path current.[33,34] In-memory computation circuits are expected to work at a high frequency like digital circuits.[30]

However, the human brain operates in an asynchronous and highly parallel way, and the information processing units of the brain, namely, synapses and neurons, work in a low frequency of tens of hertz to process spike information dynamically.[35–37] The neuron receives spatiotemporal spike trains from a number of other neurons through synapses. The computation performed by a single neuron is the transformation of synaptic input spike trains into an appropriate output spike train.[38] The synaptic weight can be constantly modulated by neural activities. Dynamic synapses provide a specific way to transform temporal patterns of spike trains to spatiotemporal patterns of synaptic events.[39] In neural spike information processing, the capability of the dynamic tuning of the synaptic weight gives rise to a significant temporal spike pattern representation and processing capabilities. In addition, such computation power may increase exponentially when the specific dynamics of pre-synaptic mechanisms vary quantitatively.[40] The dynamic spike information processing in neural networks by synapses and neurons is performed through ionic processes.[35,36] Interestingly, the modulation of the electrolyte-gated transistor is based on the control of the ions in the electrolyte, and the relaxation time of ions in electrolyte-gated transistors takes a few tens of milliseconds, which is similar to the ion process in synapses and neurons. This characteristic enables the electrolyte-gated transistor capable of dynamic synaptic and neuronal spike information processing capabilities. Furthermore, the electrochemical modulation of the electrolyte-gated transistor may contribute to the synaptic weight modulation. The ion provides rich dynamic characteristics, which makes the electrolyte-gated transistor favorable for the realization of brain-like dynamic computing.[41–53]

In this article, we start with the introduction of biological dynamic neural functions and then we explain the operation mechanism of the electrolyte-gated transistor. Later, we will give a brief review of electrolyte-gated transistors for brain-like dynamic computation. At last, conclusions and perspectives in this field are given.

II. BIOLOGICAL DYNAMIC NEURAL FUNCTIONS

In the human brain, a large number of synapses ($\sim 10^{15}$) and neurons ($\sim 10^{11}$) are connected to form a complex neural network.[10,11] As shown in Fig. 1(a), the neuron usually contains the dendrite, the soma (also called the cell body), the axon, and multiple pre-synaptic terminals.[36] The dendrite usually connects with other neurons via synapses and receives spike signals from other neurons. The soma integrates the received signals, and if the integration reaches the threshold, the neuron will emit an electrical spike signal, also called an action potential. Then, the action potential propagates down the axon to its end. Near its end, the axon divides into enlarged fine branches, called pre-synaptic terminals, which can contact other neurons via synapses, as shown in Fig. 1(b). The neuron transmitting the signal is the pre-synaptic neuron and the neuron receiving the signal is the post-synaptic neuron. The pre-synapse and the post-synapse are separated by a small distance called the synaptic cleft. When the action potential arrives at the pre-synaptic terminal, it will stimulate the pre-

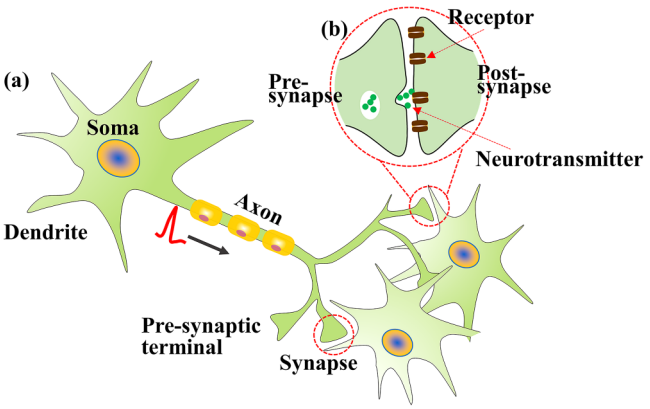

FIG. 1. (a) Schematic diagram of a biological neuron. (b) Schematic illustration of a biological synapse.

synaptic terminal to release neurotransmitters. Then, the neurotransmitter diffuses across the synaptic cleft and binds with the receptor on the post-synaptic membrane. This binding will cause ion influx into the post-synaptic terminal and generate post-synaptic potential/current, altering the membrane potential (V_{mem}) of the post-synaptic neuron. The neuron membrane is only a few nanometers thick; thus, there is appreciable capacitance between the inside and outside of the membrane ($\sim \mu F/cm^2$).[54,55] If the influx ions are cations (Na^+ and K^+, for example), the cation influx will cause excitatory post-synaptic potential/current (EPSP/EPSC), driving the post-synaptic neuron near the membrane potential threshold to emit an action potential; otherwise, the anion influx (Cl^-, for example) will cause inhibitory post-synaptic potential/current (IPSP/IPSC), driving the post-synaptic neuron away from the membrane potential threshold to emit an action potential. For the post-synaptic potential, which is lower than the threshold, it will take tens of milliseconds to decay back to the resting potential. This dynamic decay process plays an important role in temporal information processing.[35,36]

The contribution of pre-synaptic neurons to the spike signal integration of post-synaptic neurons can be greatly modulated by altering the synaptic connection strength. The ability of the synapse to change its connection strength between neurons is known as synaptic plasticity, and the synaptic plasticity exhibits a wide range of dynamics.[56] Various types of synaptic plasticity and the time scale over which they operate indicate that the synapse plays a significant role in neural spike information processing, not just information transmitting.[57] Short-term synaptic plasticity refers to the synaptic weight change in a dynamic range of milliseconds to seconds.[58–60] On this time scale, the synaptic weight strengthening and weakening are known as short-term potentiation and depression, respectively. Short-term synaptic plasticity, which dynamically modulates synaptic transmission efficiency, can greatly change the way pre-synaptic neurons activate their post-synaptic neurons. Numerous functional roles have been proposed for dynamic short-term plasticity such as synaptic filtering, sound localization, and adaptation.[57,61]

Long-term synaptic plasticity is the synaptic weight change that lasts for a long time (maybe a few years or even a lifetime).[62–65] On this long time scale, the synaptic weight strengthening and weakening are referred to as long-term potentiation and depression, respectively. Long-term synaptic plasticity is believed as the foundation of memory and learning ability.[64] The synaptic weight can be modulated by neural activities. The spike-timing-dependent plasticity (STDP) synaptic learning rule changes the synaptic weight by the relative timing between the pre- and post-synaptic spikes.[66] For example, if the pre-synaptic spikes lead the post-synaptic spikes in time by a few tens of milliseconds, it leads to long-term potentiation, and the reverse time order will result in long-term depression. The spike-rate-dependent plasticity (SRDP) synaptic learning rule alters the synaptic weight by the spike frequency of the pre-synaptic spikes.[67] High-frequency pre-synaptic spikes will lead to long-term potentiation, and low-frequency pre-synaptic spikes will result in long-term depression.

Most neurons in the central neural system receive thousands of synaptic inputs, and the post-synaptic neuron integrates all the ionic spike signals and gives rise to a simple output: action potentials.[35] During the spike neural information processing, the information is encoded in the relative timing of the pre-synaptic spike signals (time) from different pre-synaptic terminals (space). This spatiotemporal spike information coding enables the neural system to operate in an extremely high efficient way.[68] The post-synaptic neuron integrates the pre-synaptic spike signals spatially and temporally.[35] As shown in Fig. 2(a), spatial integration is the summation of EPSPs generated at different synapses at the same time. As shown in Fig. 2(b), temporal integration is the summation of EPSPs generated at the same synapse if they occur in quick succession with the time interval between each less than tens of milliseconds. This EPSP integration represents the simplest form of neuronal integration in the central neural system. In general, the dendrite exhibits diverse properties, such as morphological features, which will contribute to synaptic integration. For example, the position of synapses on the dendritic branch will contribute to neuronal integration. The order of the pre-synaptic spike sequence also contributes to the integration, resulting in a distinct post-synaptic response.[68]

As shown in Fig. 3(a), when the spatiotemporal integrated post-synaptic membrane potential (V_{mem}) reaches the threshold, the neuron will fire an action potential. Then, the action potential is transmitted to other neurons through synapses. As for the post-synaptic potential, which is lower than the threshold, it will decay to the resting potential.[35,36] Some neuronal computation models, such as the Hodgkin–Huxley neuron model, the leaky integrate-and-fire (LIF) neuron model, and the integrate-and-fire (IF) neuron model, have been proposed.[55,69] The Hodgkin–Huxley neuron model is essential but complex in computational neuroscience. It contains four equations and tens of parameters that describe the membrane potential, the activation of K^+ and Na^+ current, and the leakage current. The parameters in such a model are not only biologically meaningful, but the model allows researchers to investigate the questions related the synaptic integration, effects of dendritic morphology, dendritic cable filtering, etc.[70] The IF model and LIF model are characterized by the membrane

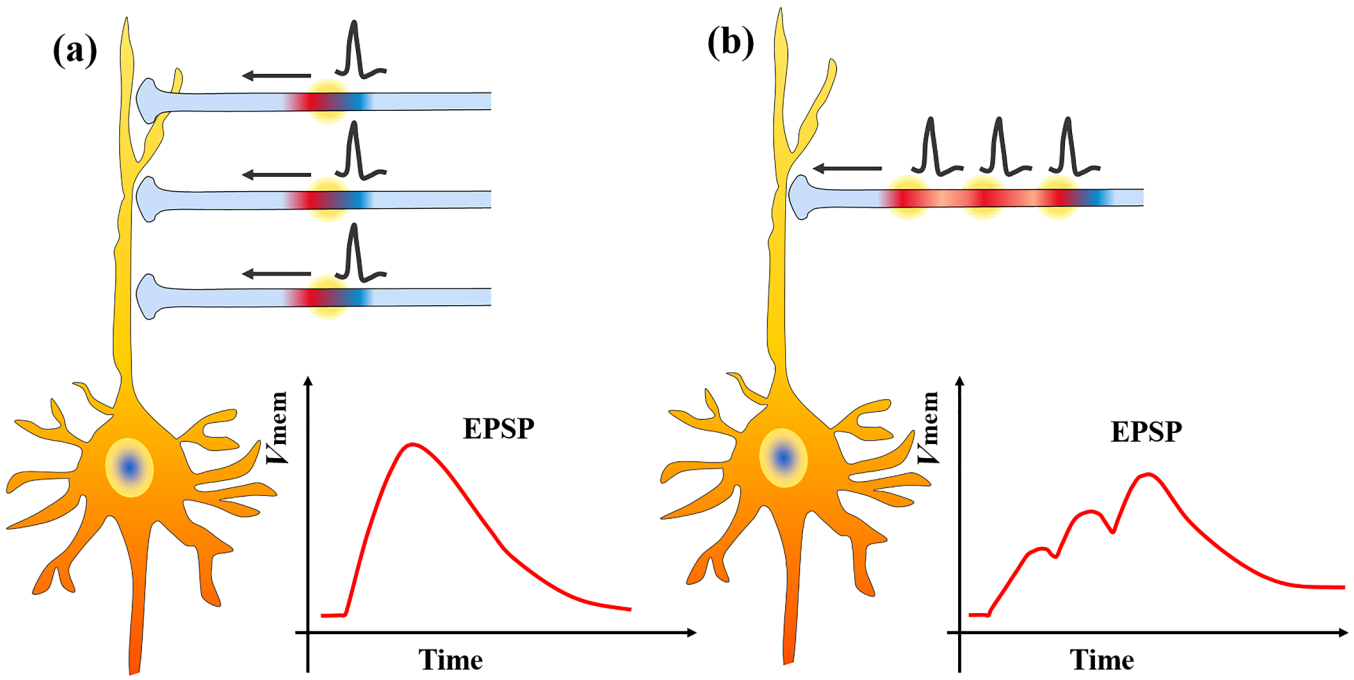

FIG. 2. (a) Schematic illustration of spatial integration of EPSP. (b) Schematic illustration of temporal integration of EPSP.

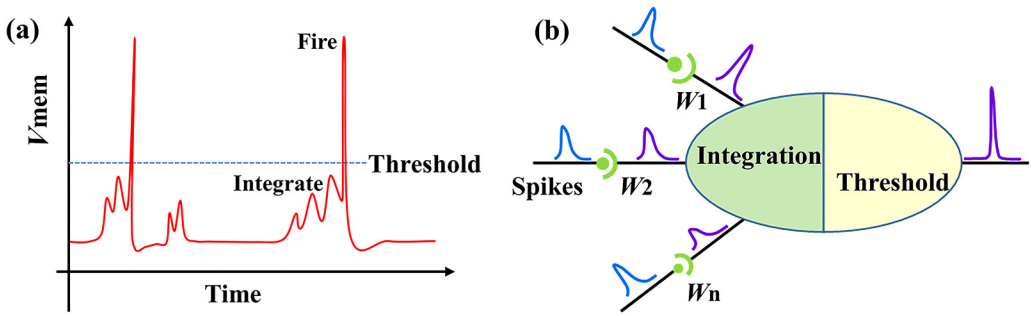

FIG. 3. (a) Schematic illustration of action potentials generated in a neuron. (b) Schematic illustration of an integrate-and-fire (IF) neuron model.

potential, in which the spatial structure of the neuronal dendrite is neglected.[71] The IF and LIF models decide whether to fire a spike by comparing the membrane potential with the threshold, as shown in Fig. 3(b). The IF neuron model retains its membrane potential until it fires.[71] Unlike the IF model, the membrane potential in the LIF model will leak out in a short time if it is lower than the threshold, which is in line with the biological neuronal behavior.

III. ELECTROLYTE-GATED NEUROMORPHIC TRANSISTORS

As early as the 19th century, the concept of electric-double-layer (EDL) in the electrolyte was first described.[72] In the 1970s, the electrolyte-gated transistor based on EDL modulation was proposed.[73] As shown in Fig. 4(a), electrolyte-gated transistors have the same structure as field-effect transistors, but the dielectric layer is replaced with the electrolyte. There are abundant anions and cations in the electrolyte. As shown in Fig. 4(b), the ions will move and accumulate at the interface under the electric field. The accumulated ions form the giant EDL capacitance at the order of several μF/cm^2, leading to low operation voltage.[74] When the voltage applied to the gate is relatively low, the channel conductance is modulated by the gate voltage through EDL capacitance, which corresponds to the field-effect modulation of the electrolyte-gated transistor. In this case, when the gate voltage is removed, the ions accumulated at the interface can diffuse back to their equilibrium position completely. As shown in Fig. 4(c), when the gate voltage is high enough, the ions in the electrolyte may penetrate across the electrolyte/channel interface to electrochemically dope the channel or the electrolyte may react with the channel, which corresponds to the electrochemical modulation of the electrolyte-gated transistors. The ion in the electrolyte provides rich dynamic characteristics, which makes the electrolyte-gated transistor favorable for the realization of brain-like dynamic computing.

In 2009, Jiang *et al.* reported a type of indium–gallium–zinc-oxide (IGZO)-based electrolyte-gated EDL transistors.[75] They clarified the interfacial ion modulation mechanism of the nanogranular SiO_2 electrolyte grown at room temperature by plasma-enhanced chemical vapor deposition. The ultra-low operation voltage of metal oxide thin-film transistors was realized. Then, they explored the application of the metal oxide semiconductor-based electrolyte-gated transistor in brain-like dynamic computing and realized some essential dynamic neural functions such as short- and long-term synaptic plasticity, synaptic filtering, and dendritic integration algorithm.[76–83]

In the past decade, electrolyte-gated transistors have attracted a great deal of attention in neuromorphic devices and systems due to low operation voltage and diverse dynamics similar to synapses and neurons.[84–91] In the following, we will introduce recent progress in brain-like dynamic computation realized in electrolyte-gated transistors and their systems including dynamic synaptic plasticity, dynamic dendritic integration, dynamic neural functions, and bio-inspired somatosensory systems. In the first part, short-term synaptic plasticity, long-term synaptic plasticity, and synaptic learning rules realized in electrolyte-gated transistors and their operation mechanisms are discussed. The second part introduces the dynamic dendritic integration implemented in multi-gate electrolyte-gated transistors. The multi-gate input terminals enable the emulation of the dendritic integration. Later, some essential dynamic neural functions, such as orientation selectivity and sound azimuth location, realized in electrolyte-gated transistors/systems are presented. At last, in cooperation with sensors, electrolyte-gated transistor-based bio-inspired somatosensory systems are discussed.

A. Dynamic synaptic plasticity

The relaxation time constant of ions in the electrolyte is in the tens of milliseconds, which is comparable to the dynamic time constant of the short-term synaptic plasticity.[84,85,92] In the dynamic synaptic plasticity emulation, as shown in Fig. 5(a), the gate terminal is used as the pre-synaptic terminal and the source/drain (S/D) is used as the post-synaptic terminal. The channel current records the post-synaptic current. Due to the ion diffusion characteristics in the electrolyte, the artificial synapse based on the electrolyte-gated transistor can emulate the dynamic relaxation behavior of EPSC.[41,88,93,94] In 2013, Kim *et al.* proposed a carbon nanotube-based polymer electrolyte-gated transistor for EPSC emulation.[41] As shown in Fig. 5(b), when the pre-synaptic spike (electrical gate pulse) arrives, a spike appears, and then it takes tens of milliseconds for the EPSC to relax to its initial state, which is similar to the dynamic relaxation behavior of EPSC in the biological synapse.[95] The dynamic

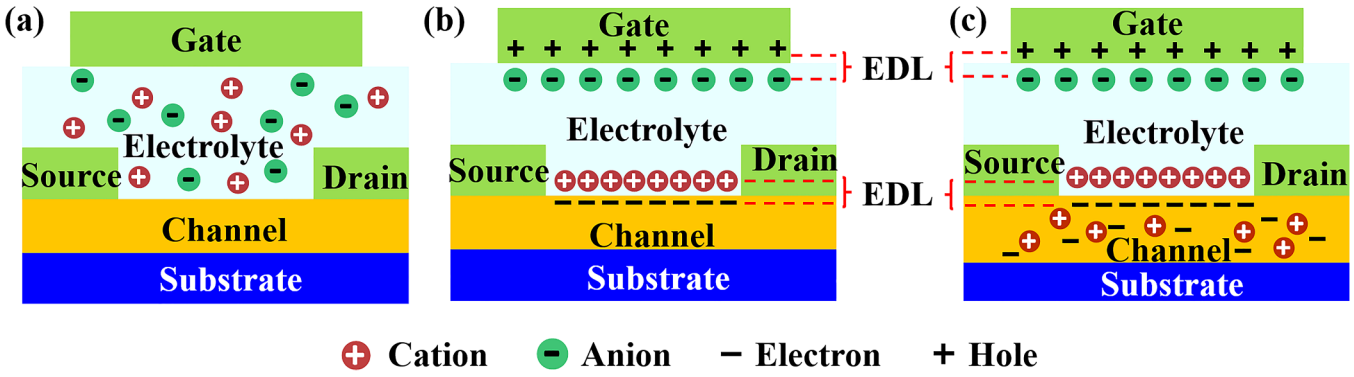

FIG. 4. (a) Structure diagram of a top gate electrolyte-gated transistor. (b) Schematic diagram of the EDL modulation of the electrolyte-gated transistor. (c) Schematic diagram of the electrochemical modulation of the electrolyte-gated transistor.

relaxation process in the emulated EPSC is due to the diffusion process of the ions that are accumulated at the channel/electrolyte and gate/electrolyte interfaces. This dynamic relaxation behavior of the EPSC is the foundation for the emulation of temporal information processing and short-term synaptic plasticity such as paired-pulse facilitation (PPF) and dynamic synaptic filtering.[96–108]

Paired-pulse facilitation (PPF) is a type of significant dynamic short-term plasticity in which the amplitude of the post-synaptic response triggered by the second pre-synaptic spike (A_2) is larger than that triggered by the first pre-synaptic spike (A_1) when the second spike closely follows the first.[58] Zhou *et al.* proposed a flexible IGZO-based nanogranular SiO_2 electrolyte-gated transistor for

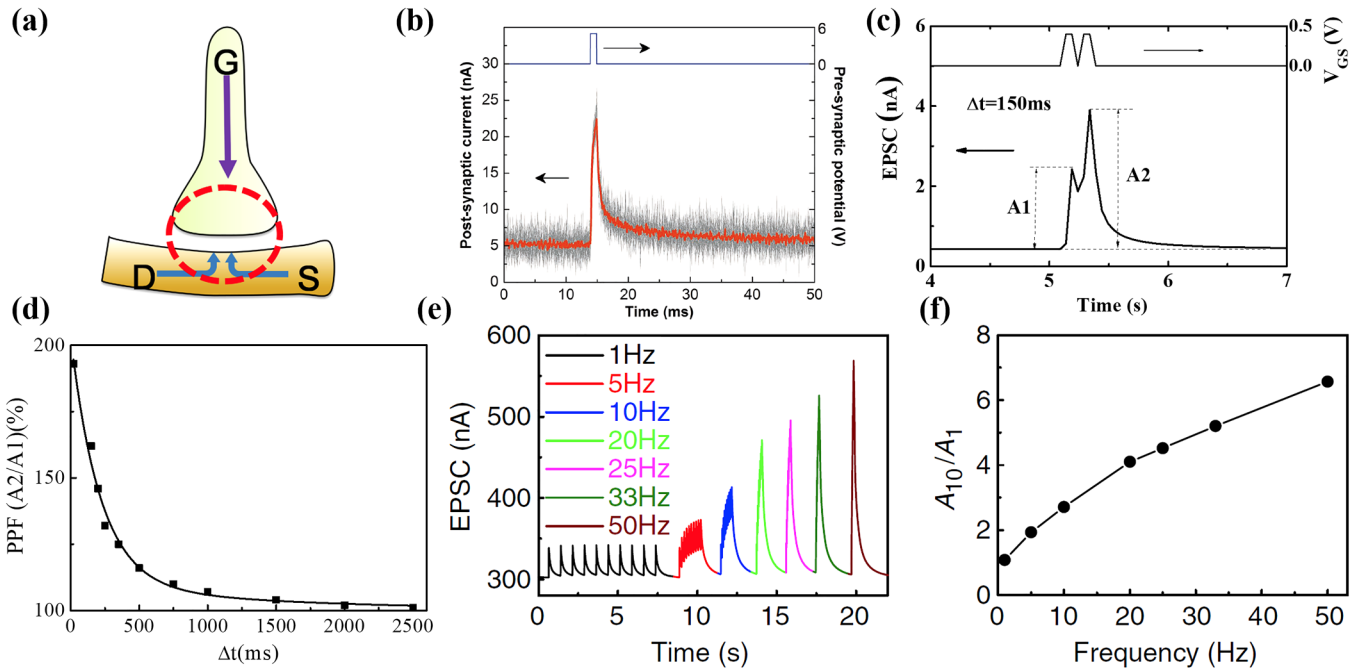

FIG. 5. Dynamic short-term synaptic plasticity emulated in electrolyte-gated transistors. (a) Schematic diagram of an artificial synapse based on an electrolyte-gated transistor. Reproduced with permission from Yang *et al.*, ACS Appl. Mater. Interfaces **8**, 30281–30286 (2016). Copyright 2016 American Chemical Society. (b) EPSC triggered by an electrical gate pulse. Reproduced with permission from Kim *et al.*, Adv. Mater. **25**, 1693–1698 (2013). Copyright 2013 John Wiley and Sons. (c) and (d) EPSC triggered by two successive electrical gate pulses; PPF ratio plotted as a function of the time interval between the two gate pulses. Reproduced with permission from Zhou *et al.*, IEEE Electron Device Lett. **36**, 198–200 (2015). Copyright 2015 IEEE. (e) and (f) EPSC triggered by gate pulse sequences with different frequencies; filtering gain as a function of the frequency of the gate pulse sequence. Reproduced with permission from Zhu *et al.*, Nat. Commun. **5**, 3158 (2014). Copyright 2014 Springer Nature.

PPF emulation.[109] As shown in Fig. 5(c), the channel current amplitude triggered by the second gate pulse (A_2) is obviously larger than that triggered by the first gate pulse (A_1), realizing the PPF behavior successfully. When the second gate pulse arrives, the ions accumulated at the channel/electrolyte interface triggered by the first pulse have not fully diffused back to their equilibrium position. The ions triggered by the second gate pulse will be augmented by the residual ions; thus, the PPF behavior is mimicked. As shown in Fig. 5(d), the PPF ratio (A_2/A_1) decreases with the time interval between the gate pulse. The longer the time interval between the two gate pulses is, the fewer residual ions will remain and the smaller the PPF ratio will be. Additionally, paired-pulse depression (PPD), which is the opposite phenomenon of PPF, was also realized in electrolyte-gated neuromorphic transistors.[110–114]

Dynamic short-term plasticity contributes to dynamic temporal filtering, which plays a significant role in neuronal spike information processing.[61,115,116] Zhu *et al.* proposed a type of indium-zinc-oxide (IZO)-based nanogranular SiO_2 electrolyte-gated transistors for mimicking dynamic synaptic temporal filtering.[77] As shown in Fig. 5(e), the EPSC amplitude triggered by the pre-synaptic spike (gate pulse) sequence increases with the frequency of the gate pulse, realizing the high-frequency dynamic temporal filtering. The filtering gain (A_{10}/A_1), defined as the ratio of the EPSC amplitude triggered by the tenth spike (A_{10}) and that triggered by the first spike (A_1), increases from ~1 to ~7 when the pulse frequency increases from 1 to 50 Hz [Fig. 5(f)].

The electrochemical doping/de-doping of ions to the semiconductor may lead to long-term changes in the channel conductance, which enables the emulation of dynamic long-term synaptic plasticity.[117–125] Wan *et al.* proposed a type of IZO-based junctionless nanogranular SiO_2 electrolyte-gated transistors for the emulation of long-term plasticity.[126] As shown in Fig. 6(a), when a high electrical voltage is applied to the gate, the protons in the nanogranular SiO_2 electrolyte may penetrate across the electrolyte/channel interface into the IZO channel. This is an irreversible n-type electrochemical doping process and the conductance of the IZO channel increases. As shown in Fig. 6(b), after the stimulation of high-voltage gate pulses (pre-synaptic spikes), a high permanent channel conductance of ~120 μS is obtained; thus, the long-term potentiation is emulated successfully.

The reversible electrochemical doping/de-doping or reaction can increase/decrease the channel conductance reversibly, which enables the electrolyte-gated transistor to emulate both the long-term potentiation and long-term depression.[127–131] van de Burgt

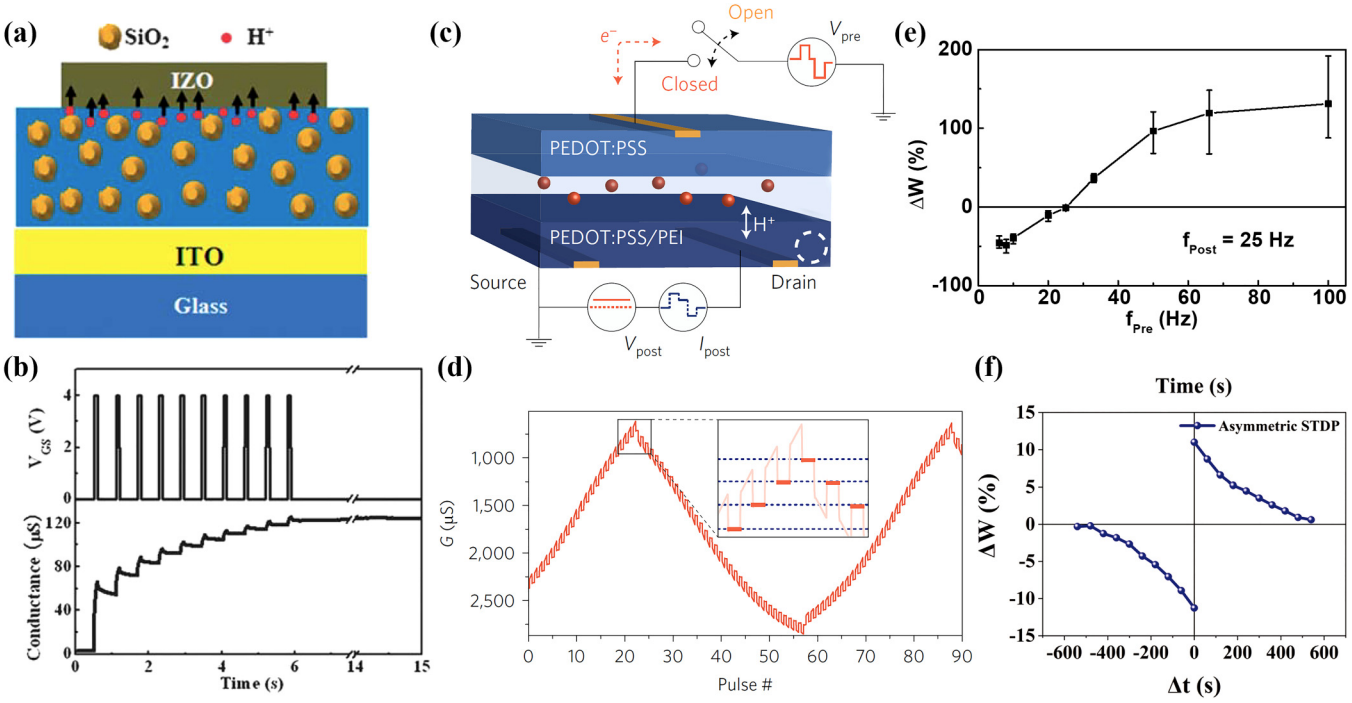

FIG. 6. Long-term synaptic plasticity and synaptic learning rules in electrolyte-gated synaptic transistors. (a) and (b) Schematic diagram of the electrochemical doping at the interface IZO/SiO_2 electrolyte; IZO channel conductance triggered by ten successive gate pulses. Reproduced with permission from Wan *et al.*, Nanoscale **5**, 10194–10199 (2013). Copyright 2013 Royal Society of Chemistry. (c) and (d) Schematic structure of PEDOT:PSS-based electrochemical device; long-term potentiation and depression as a function of pulse number. Reproduced with permission from van de Burgt *et al.*, Nat. Mater. **16**, 414–418 (2017). Copyright 2017 Springer Nature. (e) Synaptic weight change as a function of the frequency of pre-synaptic spikes. Reproduced with permission from Yang *et al.*, ACS Appl. Mater. Interfaces **8**, 30281–30286 (2016). Copyright 2016 American Chemical Society. (f) Synaptic weight change plotted as a function of the relative timing between pre- and post-synaptic spikes. Reproduced with permission from Ge *et al.*, Adv. Mater. **31**, 1900379 (2019). Copyright 2019 John Wiley and Sons.

et al. reported a type of non-volatile organic electrochemical three-terminal devices to realize long-term plasticity.[132] As shown in Fig. 6(c), the conductance of poly(3,4-ethylene dioxythiophene): polystyrene sulfonate (PEDOT:PSS) film partially reduced with poly(ethylenimine) (PEI) is used to record the synaptic weight, which is interfaced with the pre-synaptic terminal (PEDOT: PSS) via Nafion electrolyte. When a positive pre-synaptic potential is applied to PEDOT:PSS, protons will flow from the pre-synaptic electrode across the Nafion electrolyte into the post-synaptic terminal, resulting in the protonation of PEI. The holes will be removed from the PEDOT backbone in the post-synaptic terminal, reducing the electronic conductivity, and the reaction will be reversed when a negative voltage is applied to the pre-synaptic terminal and the post-synaptic electronic conductivity will increase. As shown in Fig. 6(d), the post-synaptic conductance will increase and decrease when positive and negative voltage pulses are applied to the pre-synaptic terminal, respectively. Both long-term potentiation and depression are implemented. As the synaptic weight updating can be realized in the electrolyte-gated synaptic transistor, great progress has been made in the artificial neural network simulation based on the crossbar arrays.[34,133–145]

Synaptic learning rules, such as SRDP and STDP, that dominate the long-term synaptic plasticity can be realized in electrolyte-gated transistors.[147–153] Yang *et al.* proposed an IZO-based modified graphene-oxide electrolyte-gated transistor to emulate the SRDP learning rule.[79] The pre-synaptic spike sequences and post-synaptic spike sequences are applied to the gate terminal and drain terminal, respectively. The pre-synaptic spike frequency increases from 2 to 100 Hz, and the post-synaptic spike frequency is fixed at 25 Hz. As shown in Fig. 6(e), the synaptic weight change increases from ∼−50% to ∼120% when the pre-synaptic spike frequency increases from 2 to 100 Hz, achieving the emulation of SRDP. Ge *et al.* reported a ferrite-based electrolyte-gated transistor for STDP emulation.[146] N, N-Diethyl-N-(2-methoxyethyl)-N-methylammonium bis-(trifluoromethylsulphonyl)-imide (DEME-TFSI), a type of ionic liquids, is used as the gate electrolyte. Ferrite SrFeOx is used as the channel and its conductance modulation is based on the electrochemical effect induced topotactic phase transformation. Pre- and post-synaptic spikes are fed into the gate terminal through a multiplexer. As shown in Fig. 6(f), if the pre-synaptic spike arrives prior to the post-synaptic spike, long-term potentiation occurs; and if the pre-synaptic spike arrives after the post-synaptic spike, long-term depression occurs. Thus, STDP synaptic learning rule is emulated successfully in such a ferrite-based electrolyte-gated transistor.

B. Dynamic dendritic integration

As shown in Fig. 7(a), the dendrite of the post-synaptic neuron receives numbers of electrical spike signals from thousands of pre-synaptic neurons through synapses in the central neural system.[35,36] The cell body of the post-synaptic neuron integrates all the signals spatiotemporally. As shown in Fig. 7(b), because of the giant lateral ionic/electronic coupling effect, multiple in-plane gates

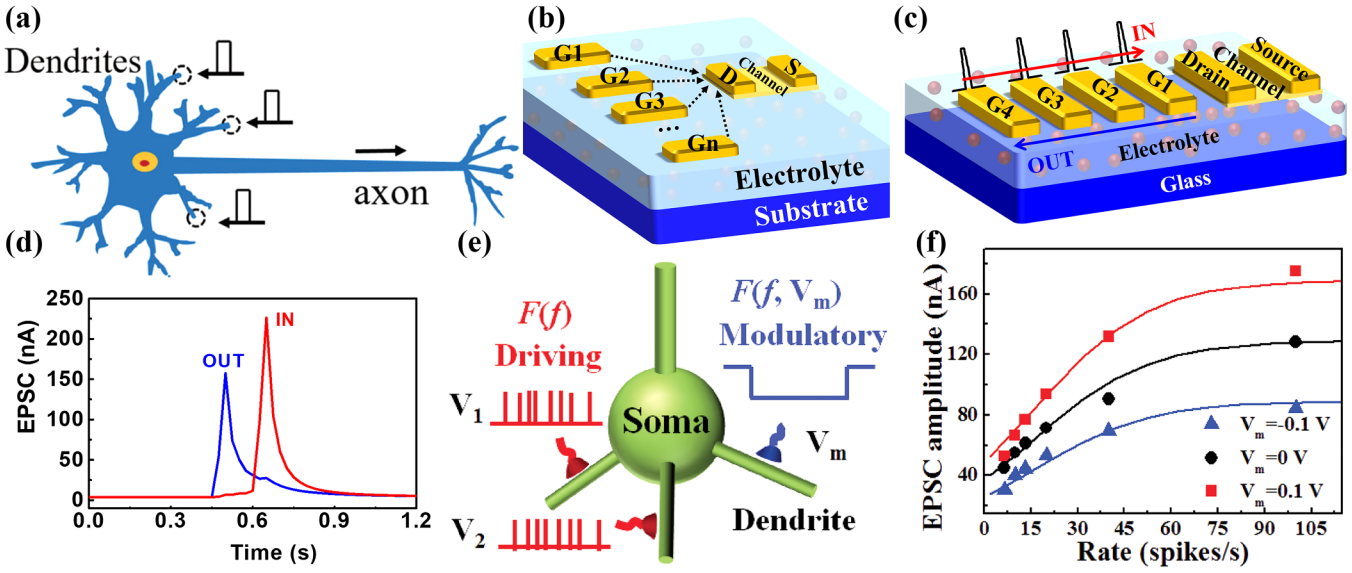

FIG. 7. Dynamic dendritic integration functions in multi-gate electrolyte-gated transistors. (a) Schematic diagram of the biological dendritic integration. Reproduced with permission from Hu *et al.*, J. Mater. Chem. C **7**, 682–691 (2019). Copyright 2019 Royal Society of Chemistry. (b) Schematic structure of a lateral coupled multi-gate electrolyte-gated transistor. (c) and (d) Schematic illustration of ordered pulse sequences (IN and OUT) applied to the gate of the IGZO-based lateral coupled electrolyte-gated transistor; post-synaptic response to the ordered pre-synaptic spike sequences. Reproduced with permission from He *et al.*, Adv. Mater. **31**, 1900903 (2019). Copyright 2019 John Wiley and Sons. (e) and (f) Schematic diagram of the rate-coding scheme with two driving synaptic inputs and one modulatory synaptic input; modulatory neural input–output relationship emulated by the multi-gate electrolyte-gated transistor. Reproduced with permission from Wan *et al.*, Adv. Mater. **28**, 3557–3563 (2016). Copyright 2016 John Wiley and Sons.

can be coupled with the channel through the huge EDL capacitance in the electrolyte-gated transistor.[77,154–162] Such a multi-gate structure enables the electrolyte-gated transistor to realize dendritic spatiotemporal integration functions and hardware neural networks.[82,163–170] The multiple-gate terminals are used as the numerous synaptic input terminals on the dendrites, and the source/drain is used as the soma of the post-synaptic neuron to integrate the spike signals spatiotemporally.

The dendritic discrimination of the dynamic spatiotemporal synaptic input spike sequences is the foundation of the brain function and underlies the perception, recognition, and motor output.[68] This dendritic discriminability was achieved by an IGZO-based multi-gate lateral coupled electrolyte-gated neuromorphic transistor.[82] As shown in Fig. 7(c), the gate pulse sequences applied to the multi-gate are used as the spatiotemporal pre-synaptic signals. The channel current records the integrated post-synaptic current. The multi-gate electrolyte-gated neuromorphic transistor is not only sensitive to ordered spike sequences [Fig. 7(d)] but also sensitive to the random spike sequences, realizing the dendritic discriminability of the dynamic spatiotemporal pre-synaptic spike sequences.

The modulation of neuronal arithmetic in the scheme of rate-coding was reported by Wan *et al.* on a multi-gate IZO-based graphene-oxide electrolyte-gated transistor.[78] Figure 7(e) illustrates the rate-coding scheme where the information is encoded by the rate (f) of the driving input. In this work, the driving input is defined by the rate of the spike applied through the gate terminal, and the modulatory input is defined as the modulatory voltage (V_m) applied to the other gate terminal. Figure 7(f) shows the neural input–output relationship modulated by V_m. When the V_m increases from −0.1 to 0.1 V, the saturation EPSC almost doubles, indicating that the modulatory voltage can modulate the neuronal arithmetic characteristics to a large extent.

C. Dynamic neural functions

Some essential dynamic neural functions, such as orientation selectivity,[171] associative learning,[172–178] pain-perceptual nociceptor,[179,180] and sound azimuth location,[82] were implemented by multi-gate electrolyte-gated transistors or their networks. Gkoupidenis *et al.* reported a multi-gate PEDOT:PSS-based aqueous NaCl electrolyte-gated transistor for orientation selectivity.[171] As shown in Fig. 8(a), they proposed a definition of different orientations by spatial gate pulse patterns. The spatial pattern is determined by simultaneously applying pulses on three gates. As shown in the upper panel of Fig. 8(b), the increased percentage in the response current amplitude (I_0, $t \to 0$) compared to the lowest

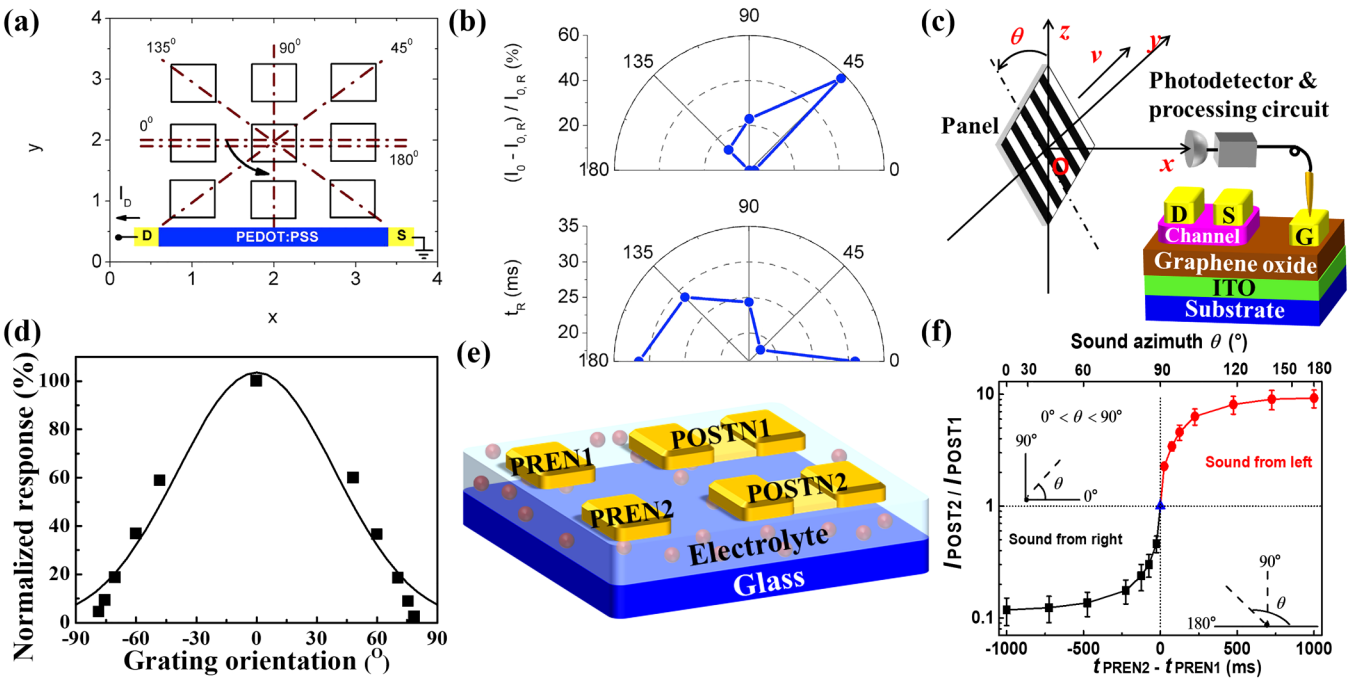

FIG. 8. Dynamic neural functions emulated in electrolyte-gated neuromorphic transistors. (a) Definition of different orientations by spatial gate pulse patterns. (b) Upper panel: drain current increase percentage of the response current amplitude (I_0, t→0) compared to the lowest reference response current amplitude ($I_{0,R}$). Lower panel: relaxation time (t_R) of the depolarization drain current. Reproduced with permission from Gkoupidenis *et al.*, Sci. Rep. **6**, 27007 (2016). Copyright 2016 Springer Nature. (c) and (d) Schematic structure of the orientation tuning experiment; normalized drain current response as a function of the orientation angle. Reproduced with permission from Wan *et al.*, Adv. Mater. **28**, 3557–3563 (2016). Copyright 2016 John Wiley and Sons. (e) and (f) Schematic structure of the hardware network consisting of two gate terminals and two pairs of source/drain terminals; ratio of the amplitude of the current of I_{POST2} and I_{POST1} plotted as a function of the time interval between the two pre-synaptic pulses and the sound azimuth. Reproduced with permission from He *et al.*, Adv. Mater. **31**, 1900903 (2019). Copyright 2019 John Wiley and Sons.

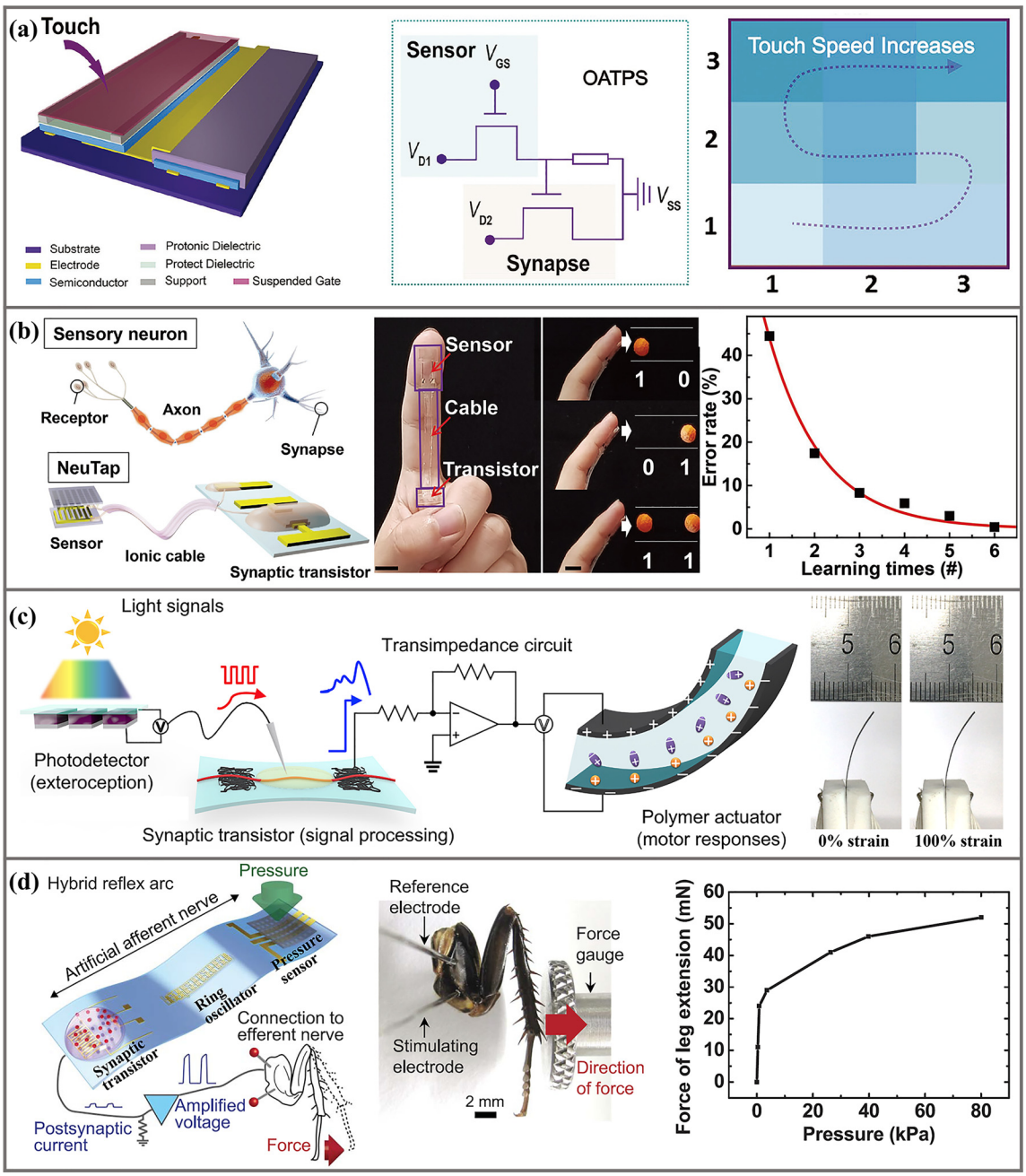

FIG. 9. Artificial somatosensory systems based on electrolyte-gated transistors. (a) Left panel: schematic structure of the dual-organic-transistor-based tactile-perception element; middle panel: equivalent circuit of the dual-organic-transistor-based tactile-perception element; right panel: schematic illustration of the tactile-perception function with different touch speeds. Reproduced with permission from Zang *et al.*, Adv. Mater. **29**, 1606088 (2017). Copyright 2017 John Wiley and Sons. (b) Left panel: schematic illustration of a sensory neuron and an artificial neuromorphic tactile processing system; middle panel: photograph of the neuromorphic tactile processing system and the illustration of different patterns; right panel: pattern recognition error rate plotted as the learning times. Reproduced with permission from Wan *et al.*, Adv. Mater. **30**, 1801291 (2018). Copyright 2018 John Wiley and Sons. (c) Left panel: schematic illustration of the artificial stretchable organic electrolyte-gated transistor-based sensorimotor system; right panel: digital images of displacement of the polymer actuators when the transistor is at 0% and 100% strain. Reproduced with permission from Lee *et al.*, Sci. Adv. **4**, eaat7387 (2018). Copyright 2018 Author(s), licensed under a Creative Commons Attribution (CC BY) license. (d) Left panel: schematic diagram of the hybrid reflex arc; middle panel: photograph of a detached cockroach leg and a force gauge; right panel: force of leg extension as a function of the pressure duration. Reproduced with permission from Kim *et al.*, Science **360**, 998–1003 (2018). Copyright 2018 The American Association for the Advancement of Science.

reference response current amplitude ($I_{0,\ R}$) reflects the orientation. In addition, as shown in the lower panel of Fig. 8(b), the relaxation time (t_R) of the depolarization drain current also represents the orientation. The dynamic spatiotemporal orientation selectivity function thus can be realized by the electrolyte-gated neuromorphic transistor.

Orientation tuning function was reported on a multi-gate IZO-based graphene-oxide electrolyte-gated transistor by Wan *et al.*[78] As shown in Fig. 8(c), they built a simple visual system model consisting of a photodetector and a processing circuit connected to the gate of the neuronal transistor. For each orientation, the panel moves from side to side at a v speed. Every time the grating pattern edge moves across the coordinate origin, which can be detected by the photodetector, the processing circuit will emit a voltage pulse to the pre-synaptic gate terminal of the neuronal transistor. Figure 8(d) shows the normalized channel current response to the neuronal transistor plotted as a function of the orientation. The experimental data can be well fitted by a Gaussian function with a half-width of ∼44° measured at the half-height, which is comparable to some biological experiments.[181]

Sound location plays a significant role in information exchange, foraging, dodging the predator, etc. The sound location mainly depends on the time difference between the two ears.[182] He *et al.* constructed a neural system for sound azimuth detection based on multi-gate IGZO electrolyte-gated transistors.[82] As shown in Fig. 8(e), the artificial neural system contains two gate terminals and two pairs of source/drain terminals, which are regarded as pre-synaptic neurons (PREN1 and PREN2) and post-synaptic neurons (POSTN1 and POSTN2), respectively. To mimic the sound azimuth detection, a gate pulse is applied to PREN2 and then another pulse is applied to PREN1 when the sound comes from the right direction and vice versa. The time interval between the two gate pulses represents the time difference between the two ears. Figure 8(f) shows the ratio of the amplitude of the current of POSTN2 and POSTN1 (I_{POST2}/I_{POST1}) at the end time of the last PREN pulse as a function of the time interval between the two pre-synaptic pulses and the sound azimuth. Thus, the sound azimuth detection function can be realized in such a simple hardware artificial neural network.

D. Bio-inspired somatosensory systems

The somatosensory system processes complex spike sensory information through the distributed network of receptors, neurons, and synapses.[183] Artificial intelligent information processing systems with sensory and perception functions are highly desired. The electrolyte-gated transistor enables the information processing abilities of artificial sensory systems.[83,183–191] In the following part, we will discuss the recent progress in electrolyte-gated transistor-based artificial spike sensory information processing systems.

In 2017, Zang *et al.* proposed the first tactile-perception system with signal processing functionality based on organic electrolyte-gated transistors.[188] A suspended-gate organic transistor and an organic electrolyte-gated transistor are used as the pressure sensor and the information processing unit, respectively [left and middle panel in Fig. 9(a)]. By taking advantage of the temporal spike information processing ability of the electrolyte-gated organic transistor, sensory information, such as touching pressure intensity, duration, and frequency [right panel in Fig. 9(a)] can be efficiently processed.

An artificial neuromorphic tactile processing system (NeuTap) with sensory perception learning was developed by Wan *et al.*[189] As shown in the left panel of Fig. 9(b), this system consists of a resistive pressure sensor and electrolyte-gated synaptic spike information processing transistor, which are connected by an ionic cable. The pressure sensor converts tactile information into electrical signals, the ionic cable transmits the signals to the synaptic transistor, and then the synaptic transistor processes the tactile information. The response current of the synaptic transistor to the different patterns shows different dynamic relaxation characteristics. This feature can be used to recognize different tactile patterns. Supervised learning is utilized to mimic the perceptual learning process, which reduces the tactile pattern recognition error rate from ∼44% to ∼0.4% [right panel in Fig. 9(b)].

Additionally, Lee *et al.* reported an artificial stretchable organic electrolyte-gated transistor-based sensorimotor system.[190] As shown in the left panel of Fig. 9(c), the sensorimotor system contains a photodetector, an organic electrolyte-gated transistor, a trans-impedance circuit, and a polymer actuator, which are used to convert light stimuli to voltage spikes, process optical spike sensory signals, convert post-synaptic current into voltage signals, and mimic muscle fiber, respectively. When light pulses are applied to the photodetector, the post-synaptic current is converted into voltages to operate the actuator [right panel in Fig. 9(c)], mimicking the biological sensorimotor system.

In order to mimic the way that the biological neural network processes spike information faithfully, Kim *et al.* introduced a ring oscillator to convert bias voltage into electrical spikes in a hybrid reflex arc.[183] As shown in the left panel in Fig. 9(d), the hybrid reflex arc consists of a resistive pressure sensor, an organic ring oscillator, an electrolyte-gated synaptic transistor, and a biological actuator (detached cockroach leg). The resistive pressure sensor converts pressure into different voltage outputs, the ring oscillator converts the voltage output into pre-synaptic spikes with different frequencies, and the electrolyte-gated transistor processes the spike information. The post-synaptic current is then amplified to stimulate the biological efferent nerves and muscles to initiate movement. The force of the biological detached leg extension increases with the increase of the pressure intensity [right panel in Fig. 9(d)] and duration applied to the pressure sensor. This hybrid bio-electronic system has potential applications in neurorobotics and neuroprosthetics.

IV. CONCLUSIONS AND PERSPECTIVES

The past decade has witnessed great progress in brain-like dynamic computation based on electrolyte-gated transistors and their systems. In summary, we have reviewed the latest progress in the field of electrolyte-gated transistor-based brain-like dynamic computing. The biological dynamic neural functions were introduced first and then we explained the operation mechanism of the electrolyte-gated transistor. Later, we reviewed the latest progress in dynamic synaptic plasticity, dynamic dendritic integration,

dynamic neural functions, and bio-inspired somatosensory systems realized based on electrolyte-gated transistors.

In the traditional CMOS circuit, we pursue faster speed whether at the device or circuit level. In the human brain, spike information processing is performed in an asynchronous and massively parallel way. The synaptic and neuronal spike information processing is an ionic process with various ranges of dynamics. What is important in this process is not the speed like the digital circuit but the spike information processing capabilities contained in this dynamic process. The electrolyte-gated transistor provides a promising platform for dynamic spike information computing because of its diverse ionic dynamic characteristics. Although great progress has been made in brain-like dynamic computing based on electrolyte-gated transistors, challenges remain, which we will discuss in detail below:

(1) Although the working mechanisms of the human brain are not completely clear at present, which requires continued breakthroughs in neuroscience, there are still some essential working rules of the brain that we should take into account in brain-like computation implementation, such as synaptic plasticity, synaptic learning rules, and spike-timing information coding. Great progress has been made in implementing basic spike information processing neuro-rules. However, most of the work achieved only one or part of the neuro-rules. For example, many works only achieved some synaptic plasticity functions. Table I shows a brief comparison of the most representative electrolyte-gated transistors and the neural functions they implemented. The computational neuron model introduced in the second part, such as the Hodgkin–Huxley neuron model and the LIF model, has been rarely reported based on electrolyte-gated transistors. As mentioned above, the electrolyte-gated transistor can easily achieve the dynamic spatiotemporal integration function. The "fire" function of the LIF model may learn from threshold-switching memristors.[192,193]
(2) Up to now, various types of electrolytes and channel materials have been developed in electrolyte-gated neuromorphic transistors including organic and inorganic materials. Organic materials have many advantages such as mechanical flexibility, low-cost processing, and bio-compatibility. Inorganic materials hold a great advantage in being compatible with the existing micro-processing technology. The device's controllability and

TABLE I. Comparison of different types of electrolyte-gated transistors.

Channel materials	Electrolyte materials	Neural functions	Reference
IZO	Nanogranular SiO_2	PPF, high-pass filtering, long-term potentiation, STDP, non-linear summation	51, 76, 87, and 150
IZO	Graphene oxide	Dendritic arithmetic modulation, orientation tuning, collision avoidance response, SRDP	78 and 79
IZO	Chitosan	Meta-plasticity, nociceptors	161 and 180
IGZO	Chitosan	Dendritic spatiotemporal integration, hardware neural network for sound azimuth detection, tactile sensing information processing, silent synapse conversion	47, 82, and 83
IGZO	Bio-polysaccharide	Associative learning	176
IGZO	Pectin-based polysaccharide	Linear classification	48
ITO	Sodium alginate	Pain-perceptual nociceptor emulation	179
ITO	$CaCl_2$/PVA	Visual-haptic fusion sensory information processing	191
$SmNiO_3$	Ionic liquid	Synaptic weight modulation, STDP	128
WO_3	$LiClO_4$/PVA	Synaptic weight modulation, neural network simulation	131
$NdNiO_3$	Porous silica	Long-term plasticity	124
$LiCoO_2$	LiPON	Synaptic weight modulation, neural network simulation	137
α-Nb_2O_5	Li_xSiO_2	Synaptic weight modulation, detecting moving orientation	129
$SrFeO_x$	Ionic liquid	Long-term plasticity, STDP	146
VO_2	Porous solgel silica	High-pass filtering, long-term memory	118
α-MoO_3	$LiClO_4$/PEO	Synaptic weight modulation, neural network simulation	135
MoS_2	PVA	PPF, spatiotemporal information processing	154
MoS_2	Chitosan	PPF, high-pass filtering	155
Trigonal selenium	$LiClO_4$/PEO	PPF, high-pass filtering	102
P-Si	$RbAg_4I_5$	STDP	84
Carbon nanotube	PEG	PPF, STDP	41
PEDOT: PSS	Aqueous NaCl	Orientation selectivity	171
P3HT	Ionic gel	Spatiotemporal information processing	167
P3HT	Ionic gel	Short- and long-term plasticity, haptic information processing	185
Polymer	Ionic gel	Haptic information processing	183

TABLE II. Comparison of different materials used in electrolyte-gated transistors.

	Material types	Advantages	Current issues/challenges
Channel materials	Metal oxide semiconductors (IGZO, IZO, ITO, etc.)	Low-processing temperature, high uniformity, compatible with existing micro-processing technology	Electrical stress instability
	Low-dimensional semiconductors (MoS_2, carbon nanotube, etc.)	Great potential in device scalability	Difficulties in the growth of large-area high-quality materials
	Organic semiconductors (P3HT, PEDOT:PSS, etc.)	Mechanical flexibility, low-cost processing, and bio-compatibility.	Low device reproducibility and relatively low yield, device-to-device variability
Electrolyte materials	Inorganic solid-state electrolytes (nanogranular SiO_2, Al_2O_3, etc.)	Compatible with the existing micro-processing technology, low-processing temperature	Easy to produce dust during low temperature growth
	Ionic liquids and ionic gels (DEME-TFSI, etc.)	Relatively high ion diffusivity, low-processing temperature	Not compatible with the existing micro-processing technology, encapsulation issues
	Polymer or biopolymer electrolytes (chitosan, $LiClO_4$/PEO, etc.)	Low-processing temperature, low-processing price	Not compatible with the existing micro-processing technology

endurance can be enhanced through encapsulation. However, some electrolytes, such as ionic liquids, may become limitations for the practical use of electrolyte-gated neuromorphic transistors. Many materials claim to be promising, but still not one or a few of them have become the champion materials. This will cause the scientific effort to spread thin among different materials and device architectures. Table II shows the commonly used channel/electrolyte materials in electrolyte-gated transistors and their advantages and current issues/challenges. As this field develops in the future, material winners are expected to emerge, which will help researchers focus on the deeper understanding of how to map dynamic neural spike information computing functions to the electrolyte-gated transistors and their systems.

(3) At the device level, we hope that the electrolyte-gated neuromorphic transistors exhibit a variety of dynamics compared with the permanent stability that the traditional CMOS transistors pursue. When integrated into large-scale neuromorphic circuits, high device scalability and low device-to-device variability are desired, which requires further investigation. As we can see in Table I, much work has been done in this field at the device level, but work on the brain-like dynamic computing architecture has been rarely reported. In the human brain, neurons and synapses are arranged in a three-dimensional space to construct a complex neural network with powerful spike information processing capabilities. In order to realize the connection complexity like the neural networks, three-dimensional integration technologies may be needed.

(4) Most of the existing neural network algorithms are based on the existing digital computers. The brain-like dynamic computation algorithm is in its early stage, which requires the researchers to devote efforts in this field and draw inspiration from neurobiology. We may need to develop algorithms that mimic the dynamic dendritic integration function to efficiently process spatiotemporal spike information. The synapse constantly alters its synaptic weight through synaptic learning rules, such as STDP learning rules, which may inspire dynamic learning algorithms in spiking neural networks. The human brain encodes the information in a dynamic spatiotemporal way efficiently through spiking, and not only time but also space carries information. The collaborative implementation of the hardware brain-like dynamic computing and the dynamic spike information processing algorithms may unleash a great huge of computation capability.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

DATA AVAILABILITY

Data sharing is not applicable to this article as no new data were created or analyzed in this study.

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