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Package and Board Level Reliability Modeling of Advanced CSP Packages for Telecommunication Applications

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A thesis submitted to the Nanyang Technological University
in fulfilment of the requirement for the degree of
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LIST OF SYMBOLS

a	acceleration (m/s^2)
c	coefficient of restitution
C	moisture concentration (mg/mm^3)
C_p	specific heat (J/kg.K)
C_{sat}	saturated moisture concentration (mg/mm^3)
D	moisture diffusivity (mm^2/s)
D_o	moisture diffusion coefficient (mm^2/s)
E	modulus (MPa)
f	void volume fraction
f_o	initial void volume fraction
F	force (N)
F_r	failure rate (%)
g	gravitational acceleration ($9.81 m/s^2$).
G	strain energy release rate (N/m)
G_m	peak acceleration (m/s^2).
h	thickness of the specimen.(mm)
H	drop height (m)
k	thermal conductivity (W/m.K)
K	spring constant (N/m)
l	characteristic length of the smallest element (mm)
m	mass (kg)
M_{sat}	saturated mass of moisture absorbed (mg)
M_t	mass of moisture absorbed at time t (mg)
N	solder joint fatigue life (cycle)
N_{50}	mean impact life (cycle)
N_o	crack initiation life (cycle)
N_p	crack propagation life (cycle)
P	vapor pressure (MPa)
p_g	saturated vapor pressure (MPa)
Q	activation energy (ev)
R	Boltzmann constant (8.83e-5 ev/K)

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t	time (s)
Δt	critical time step (s)
T	temperature (K)
V	velocity (m/s)
V_a	actual impact velocity (m/s)
V_t	theoretical impact velocity (m/s),.
w	moisture wetness
x, y, z	rectangular coordinates (mm)
α	coefficient of thermal expansion (ppm/°C)
α_T	thermal diffusivity (mm^2/s)
β	slope of Weibull plot
β_m	coefficient of moisture expansion (mm^3/mg)
η	characteristic life at 63.2% failure rate (cycle)
ε_p	vapor pressure induced strain
ε_h	hygro strain
ψ	mode mixity (°)
ρ	density (kg/m^3)
σ	stress (MPa)
σ_{xz}	shear stress (MPa)
σ_z	peeling stress (MPa)
ν	Poisson's ratio

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LIST OF TERMS

BGA	Ball Grid Array
C^2BGA	Conduction-cooled Ball Grid Array
CAE	Computer-aided-engineering
CFDEM	Crack Flank Displacement Extrapolation Method
CME	Coefficient of Moisture Expansion
CSP	Chip Scale Package
CTE	Coefficient of Thermal Expansion
CTOD	Crack Tip Opening Displacement
DA	Die Attach
DFR	Design for Reliability
DMA	Dynamic Mechanical Analyzer
DNP	Distance to Neutral Point
DOE	Design of Experiment
FC	Flip-chip
FEA	Finite Element Analysis
FEM	Finite Element Modeling
HTS	High Temperature Storage test
IC	Integrated Circuits
ICCG	Incomplete Cholesky Conjugate Gradient
IPD	Integrated Passives Device
JCG	Jacobi Conjugate Gradient
MC	Mold Compound
MEMS	Microelectromechanical Systems
MLF	Micro LeadFrame
MLP	Micro Lead Package
PCB	Printed Circuit Board
PCG	Preconditioned Conjugate Gradient
PCT	Pressure cooker test
QFN	Quad-Flat-No-lead
QFP	Quad Flat Pack
QON	Quad Outline Non-lead

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RVE	Representative Volume Element
RH	Relative Humidity
SED	Strain Energy Density
SiP	System-in-package
SO	Small Outline
SON	Small Outline Non-lead
TCT	Thermal Cycling Test
TFBGA	Thin-profile Fine-pitch Ball Grid Array
TGA	Thermo-gravimetric Analyzer
THS	Temperature Humidity Storage test
TMA	Thermo-mechanical Analyzer
UBM	Underbump Metallization
UF	Underfill
VCC	Virtual Crack Closure
VFBGA	Very thin-profile Fine-pitch Ball Grid Array
WB	Wirebond
WL-CSP	wafer-level CSP
WLP	Wafer-level Package

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LIST OF PUBLICATIONS

Journals (2002-2004)

1. Tee, T.Y., Kho, C.L., Yap, D., Toh, C., Baraton, X., and Zhong, Z.W.
"Reliability Assessment and Hygroswelling Modeling of FCBGA with No-flow Underfill"
Microelectronics Reliability Journal, 2003, Vol. 43(5), pp. 741-749.

   Tee outlined the work. Tee conducted the modeling and analysis with integration of multi-displinary work, and established the correlation between modeling and experiments. Kho performed the assembly of packages. Yap conducted the reliability tests. Toh characterized the material properties under Tee's guidance. Baraton collected the package geometry specifications. Tee wrote the paper under the supervision of Zhong.
   (Extracted from Chapter 3 of thesis)

2. Tee, T.Y. and Zhong, Z.W.
"Integrated Vapor Pressure, Hygroswelling, and Thermo-mechanical Stress Modeling of QFN Package during Reflow with Interfacial Fracture Mechanics Analysis"
Microelectronics Reliability Journal, 2004, Vol. 44(1), pp. 105-114.

   Tee outlined the work. Tee conducted modeling and analysis. Tee wrote the paper under the supervision of Zhong.
   (Extracted from Chapter 4 of thesis)

3. Tee, T.Y., Ng, H.S., Yap, D., Baraton, X., and Zhong, Z.W.
"Board Level Solder Joint Reliability Modeling and Testing of TFBGA Packages for Telecommunication Applications"
Microelectronics Reliability Journal, 2003, Vol. 43(7), pp. 1117-1123.

   Tee outlined the work. Tee conducted the modeling and analysis, and established correlation between modeling and experiments. Ng characterized the material properties and compiled the modeling results under Tee's guidance. Yap conducted the reliability tests. Baraton collected the package geometry specifications. Tee wrote the paper under the supervision of Zhong.
   (Extracted from Chapter 5 of thesis)

4. Tee, T.Y., Ng, H.S., Yap, D., and Zhong, Z.W.
"Comprehensive Board-Level Solder Joint Reliability Modeling and Testing of QFN and PowerQFN Packages"
Microelectronics Reliability Journal, 2003, Vol. 43(8), pp. 1329-1338.

   Tee outlined the work. Tee conducted the modeling and analysis, and established correlation between modeling and experiments. Ng characterized the material properties and compiled the modeling results under Tee's guidance. Yap conducted the reliability tests. Tee wrote the paper under the supervision of Zhong.
   (Extracted from Chapter 5 of thesis)

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5. Tee, T.Y., Frezza, G., Lim, M., Ng, H.S., Ziglioli, F., and Zhong, Z.W.
"Design for Board Level Reliability of a Miniaturized MEMS Package: Stacked Die TQFN"
International Journal of Computational Engineering Science (IJCES), 2003, Vol. 4(2), pp. 347-350.

Tee outlined the work. Tee conducted the modeling and analysis. Frezza designed the package. Lim compiled the modeling results and Ng characterized the material properties; both under Tee's guidance. Ziglioli collected the package geometry specifications. Tee wrote the paper under the supervision of Zhong.
(Extracted from Chapter 6 of thesis)

6. Tee, T.Y. and Zhong, Z.W.
"Board Level Solder Joint Reliability Analysis and Optimization of Pyramidal Stacked Die BGA Packages"
Microelectronics Reliability Journal, 2004, Vol. 44(12), pp. 1957-1965.

Tee outlined the work. Tee conducted modeling and analysis. Tee wrote the paper under the supervision of Zhong.
(Extracted from Chapter 6 of thesis)

7. Tee, T.Y., Ng, H.S., Baraton, X., Kaire, D., and Zhong, Z.W.
"Board Level Solder Joint Reliability Analysis of Stacked Die Mixed Flip-Chip and Wirebond BGA"
Accepted, to be published in Microelectronics Reliability Journal, 2005.

Tee outlined the work. Tee conducted the modeling and analysis. Ng characterized the material properties and compiled the modeling results under Tee's guidance. Baraton and Kaire collected the package geometry specifications. Tee wrote the paper under the supervision of Zhong.
(Extracted from Chapter 6 of thesis)

8. Tee, T.Y., Ng, H.S., Lim, C.T., Pek, E., and Zhong, Z.W.
"Drop Test and Impact Life Prediction Model for QFN Packages"
Journal of Surface Mount Technology, 2003, Vol. 16(3), pp. 31-39.

Tee outlined the work. Tee conducted the modeling and analysis with correlation to experiments. Ng characterized the material properties and compiled the modeling results under Tee's guidance. Pek conducted the drop test under Lim's supervision and Tee's guidance. Tee wrote the paper under the supervision of Zhong.
(Extracted from Chapter 7 of thesis)

9. Tee, T.Y., Ng, H.S., Lim, C.T., Pek, E., and Zhong, Z.W.
"Impact Life Prediction Modeling of TFBGA Packages under Board Level Drop Test"
Microelectronics Reliability Journal, 2004, Vol. 44(7), pp. 1131-1142.

Tee outlined the work. Tee conducted the modeling and analysis with correlation to experiments. Ng characterized the material properties and compiled the modeling results under Tee's guidance. Pek conducted the drop test under Lim's supervision and Tee's guidance. Tee wrote the paper under the supervision of Zhong.
(Extracted from Chapter 7 of thesis)

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10. Tee, T.Y., Luan, J.E., Pek, E., Lim, C.T., and Zhong, Z.W.
"Dynamic Responses during Board Level Drop Test with Modal Analysis and Spectrum Analysis"
Accepted, to be published in Microelectronics Reliability Journal, 2004.

Tee outlined the work. Tee conducted the modeling and analysis with correlation to experiments. Luan compiled the modeling results under Tee's guidance. Pek conducted the drop test under Lim's supervision and Tee's guidance. Tee wrote the paper under the supervision of Zhong.
(Extracted from Chapter 7 of thesis)

11. Tee, T.Y., Yi, S., Shen, L.X., Su, F., and Zhong, Z.W.
"Comprehensive Numerical and Experimental Analysis of Matrix TFBGA Warpage"
Journal of Surface Mount Technology, 2004, Vol. 17(2), pp. 11-17.

Tee outlined the work. Shen and Tee conducted the modeling and analysis with correlation to experiments. Su performed warpage measurements under Yi's supervision. Tee wrote the paper under the supervision of Zhong.
(Related to future research work, not reported in thesis)

All the works reported in thesis were reviewed and accepted for journal publication by international experts in this area of research.

Conferences (2002-2004)

1. Tee, T.Y., Ng, H.S., and Zhong, Z.W.
"Virtual Prototyping of IC Packages with Multiphysics Modeling"
4th ASEAN ANSYS Conference, Singapore, Nov. 2002.

Tee outlined the work. Tee conducted the modeling and analysis. Ng characterized the material properties and compiled the modeling results under Tee's guidance. Tee wrote the paper under the supervision of Zhong.

2. Tee, T.Y., Ng, H.S., Bugnard, J., Yap, D., and Zhong, Z.W.
"Solder Joint Fatigue Analysis of FCOB Using Global / Local Modeling Approach"
4th ASEAN ANSYS Conference, Singapore, Nov. 2002.

Tee outlined the work. Tee conducted the modeling and analysis with correlation to experiments. Ng characterized the material properties and compiled the modeling results under Tee's guidance. Bugnard collected the package geometry specifications. Yap conducted the reliability tests. Tee wrote the paper under the supervision of Zhong.

3. Tee, T.Y., Ng, H.S., Lim, C.T., Pek, E., and Zhong, Z.W.
"Application of Drop Test Simulation in Electronic Packaging"
4th ASEAN ANSYS Conference, Singapore, Nov. 2002.

Tee outlined the work. Tee conducted the modeling and analysis with correlation to experiments. Ng characterized the material properties under Tee's guidance. Pek conducted the drop test under Lim's supervision and Tee's guidance. Tee wrote the paper under the supervision of Zhong.

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4. Tee, T.Y., Lim, M., Ng, H.S., Baraton, X., Kaire, D., and Zhong, Z.W.
"Design Analysis of Solder Joint Reliability for Stacked Die Mixed Flip Chip and Wirebond BGA"
4th EPTC Conference, Singapore, Dec. 2002, pp. 391-397.

Tee outlined the work. Tee conducted the modeling and analysis. Lim compiled the modeling results and Ng characterized the material properties, both under Tee's guidance. Baraton and Kaire collected the package geometry specifications. Tee wrote the paper under the supervision of Zhong.

5. Tee, T.Y., Lim, M., Ng, H.S., Baraton, X., and Zhong, Z.W.
"Design Analysis and Optimization of Wirebond Stacked Die BGA Packages for Improved Board Level Solder Joint Reliability"
Keynote Paper, EuroSIME Conference, France, Mar. 2003, pp. 207-213.

Tee outlined the work. Tee conducted the modeling and analysis. Lim compiled the modeling results and Ng characterized the material properties, both under Tee's guidance. Baraton collected the package geometry specifications. Tee wrote the paper under the supervision of Zhong.

6. Tee, T.Y., Ng, H.S., Lim, C.T., Pek, E., and Zhong, Z.W.
"Board Level Drop Test and Simulation of QFN Packages for Telecommunication Applications"
ICEP03 Conference, Japan, Apr. 2003, pp. 221-226.

Tee outlined the work. Tee conducted the modeling and analysis with correlation to experiments. Ng characterized the material properties and compiled the modeling results under Tee's guidance. Pek conducted the drop test under Lim's supervision and Tee's guidance. Tee wrote the paper under the supervision of Zhong.

7. Tee, T.Y., Ng, H.S., Lim, C.T., Pek, E., and Zhong, Z.W.
"Board Level Drop Test and Simulation of TFBGA Packages for Telecommunication Applications"
53rd ECTC Conference, New Orleans, USA, May 2003, pp. 121-129.

Tee outlined the work. Tee conducted the modeling and analysis with correlation to experiments. Ng characterized the material properties and compiled the modeling results under Tee's guidance. Pek conducted the drop test under Lim's supervision and Tee's guidance. Tee wrote the paper under the supervision of Zhong.

8. Tee, T.Y., Ng, H.S., and Zhong, Z.W.
"Design for Package and Board Level Reliability with CAE"
Invited Paper, SEMICON Advanced Packaging Technology Symposium, Singapore, Aug. 2003, pp. 59-67.

Tee outlined the work. Tee conducted the modeling and analysis. Ng characterized the material properties and compiled the modeling results under Tee's guidance. Tee wrote the paper under the supervision of Zhong.

9. Tee, T.Y., Ng, H.S., Yap, D., and Zhong, Z.W.
"Board Level Solder Joint Reliability Modeling and Testing of Fine-pitch CSP Packages for Telecommunication Applications"
SEMICON Advanced Packaging Technology Symposium, Singapore, Aug. 2003, pp. 31-36.

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Tee outlined the work. Tee conducted the modeling and analysis with correlation to experiments. Ng characterized the material properties and compiled the modeling results under Tee's guidance. Yap conducted the reliability tests. Tee wrote the paper under the supervision of Zhong.

10. Tee, T.Y., Zhou, T., Lim, M., and Zhong, Z.W.
"Design Analysis of Board Level Solder Reliability for Thermally Enhanced BGAs"
SMTA Conference, Chicago, USA, Sep 2003, pp. 374-380.

Tee outlined the work. Tee conducted the modeling and analysis with correlation to experiments. Zhou designed the package. Lim compiled the modeling results under Tee's guidance. Tee wrote the paper under the supervision of Zhong.

11. Tee, T.Y., Ng, H.S., and Zhong, Z.W.
"Design Optimization of Wafer-Level CSP Solder Joint Reliability"
EMAP03 Conference, Singapore, Nov. 2003, pp. 184-189.

Tee outlined the work. Tee conducted the modeling and analysis. Ng characterized the material properties and compiled the modeling results under Tee's guidance. Tee wrote the paper under the supervision of Zhong.

12. Tee, T.Y., Lim, M., Pan, S., Lam, P., and Zhong, Z.W.
"Design Analysis of TFBGA with Customized Solder Joint Fatigue Model"
EMAP03 Conference, Singapore, Nov 2003, pp. 309-315.

Tee outlined the work. Tee conducted the modeling and analysis with correlation to experiments. Lim compiled the modeling results under Tee's guidance. Pan and Lam provided technical support on PAKSI software. Tee wrote the paper under the supervision of Zhong.

13. Tee, T.Y., Ng, H.S., and Zhong, Z.W.
"Design for Enhanced Solder Joint Reliability of Integrated Passives Device under Board Level Drop Test and Thermal Cycling Test"
5th EPTC Conference, Singapore, Dec. 2003, pp. 210-216.

Tee outlined the work. Tee conducted the modeling and analysis. Ng characterized the material properties and compiled the modeling results under Tee's guidance. Tee wrote the paper under the supervision of Zhong.

14. Tee, T.Y., Ng, H.S., Luan, J.E., Yap, D., Loh, K., Pek, E., Lim, C.T., and Zhong, Z.W.
"Integrated Modeling and Testing of Fine-pitch CSP under Board Level Drop Test, Bend Test, and Thermal Cycling Test"
ICEP04 Conference, Japan, Apr. 2004, pp. 35-40.

Tee outlined the work. Tee conducted the modeling and analysis with correlation to experiments. Ng characterized the material properties and Luan compiled the modeling results under Tee's guidance. Yap conducted the reliability tests. Loh collected the package geometry specifications. Pek conducted the drop test under Lim's supervision and Tee's guidance. Tee wrote the paper under the supervision of Zhong.

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15. Tee, T.Y., Lim, M., Ng, H.S., Baraton, X., Frezza, G., Chiu, A., and Zhong, Z.W. "Design for Enhanced Board Level Solder Joint Reliability of Stacked Die CSPs" Invited Paper, SEMICON Advanced Packaging Technology Symposium, Singapore, May 2004, pp. 151-155.

    Tee outlined the work. Tee conducted the modeling and analysis. Lim compiled the modeling results and Ng characterized the material properties, both under Tee's guidance. Baraton collected the package geometry specifications. Frezza and Chiu designed the packages. Tee wrote the paper under the supervision of Zhong.

16. Tee, T.Y., Luan, J.E., Pek, E., Lim, C.T., and Zhong, Z.W. "Novel Numerical and Experimental Analysis of Dynamic Responses under Board Level Drop Test" EuroSIME Conference, Belgium, May 2004, pp. 133-140.

    Tee outlined the work. Tee conducted the modeling and analysis with correlation to experiments. Luan compiled the modeling results under Tee's guidance. Pek conducted the drop test under Lim's supervision and Tee's guidance. Tee wrote the paper under the supervision of Zhong.

17. Tee, T.Y., Luan, J.E., Pek, E., Lim, C.T., and Zhong, Z.W. "Advanced Experimental and Simulation Techniques for Analysis of Dynamic Responses during Drop Impact" 54th ECTC Conference, Las Vegas, USA, June 2004, pp. 1088-1094.

    Tee outlined the work. Tee conducted the modeling and analysis with correlation to experiments. Luan compiled the modeling results under Tee's guidance. Pek conducted the drop test under Lim's supervision and Tee's guidance. Tee wrote the paper under the supervision of Zhong.

Based on the thesis research work, total of 17 conference papers were published and presented in 13 conferences worldwide, including 1 keynote paper and 2 invited papers.

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ABSTRACT

Market for telecommunication products (e.g., mobile phones) is very competitive, demanding products which are more reliable, higher performance, lighter, smaller, cheaper, and shorter time-to-market. These technology requirements are possible with the recent development of advanced Chip Scale Packages (CSPs), such as thin-profile fine-pitch Ball Grid Array (TFBGA), Quad-Flat-No-lead (QFN), and wafer-level CSP (WL-CSP). However, due to limited product development time, these CSPs are usually not tested and studied in detail before introduction to the market. As a result, the package design may not be optimized for various reliability requirements, e.g., popcorn, thermal cycling test, and drop test.

Computer-aided-engineering (CAE) or modeling, is getting popular as an efficient tool for design analysis and improvement, and even virtual prototyping. This thesis presents a novel and comprehensive research on package and board level reliability modeling of advanced CSPs. Main areas of research interest are moisture diffusion modeling, hygroswelling modeling, integrated stress modeling, and solder joint reliability modeling during board level thermal cycling test and drop test. A series of advanced finite element models are established for various types of CSPs with hundreds of design cases. These modeling results provide useful design guidelines for package designers to enhance the product reliability, and save time, cost and manpower in performing the reliability tests. With these models, the time of typical reliability evaluations (e.g., thermal cycling test) can be reduced from months to hours, which indirectly shortens the time-to-market of product.

The physics of failure behind various reliability issues is well understood through sophisticated mathematical models and constitutive equations. These models are

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validated through excellent correlation with actual reliability tests and failure analysis. The novel theories developed in this research project are whole-field vapor pressure modeling, integrated package stress modeling with interactions of multiphysics phenomena, modified Darveaux's method for fatigue modeling, global/local 3D model for efficient solution, warpage-solder joint fatigue life correlation, and drop impact life prediction model.

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CHAPTER 1 INTRODUCTION

1.1 BACKGROUND AND MOTIVATION

A Chip Scale Package (CSP) is defined as any Integrated Circuits (IC) package with package area less than 1.5 times of its die area, or package width less than 1.2 times of its die width, or sometimes can be any fine-pitch (0.5mm or less) area-array package [1]. In recent years, CSPs have become popular in the industry due to their high demand in telecommunication applications, such as mobile phones, PDAs, and other portable and hand-held devices. CSPs have advantageous of small footprint, light weight, and high electrical performance.

Thin-profile Fine-pitch Ball Grid Array (TFBGA), Quad-Flat-No-lead (QFN), and Wafer-Level CSP (WL-CSP) are the recent advanced CSPs developed for the telecommunication applications. TFBGA is widely used due to its moderate cost, high density and high performance interconnect technology, suitable for medium pin-count applications. QFN is preferred because of its low cost and good thermal and electrical performance, usually used in low pin-count applications. As for WL-CSP, it is getting popular with the decreasing manufacturing cost, targeted for high pin-count and high performance applications, due to its high density area-array interconnect technology.

Design for Reliability (DFR) is a concept on up-stream product design, anticipating possible failures even before the product is manufactured or tested. Due to rapid technology evolution and shorter product development time, there has been lack of advanced research in design for reliability of advanced CSPs. There are relatively few publications available for semiconductor industry to learn to enhance the CSPs and board designs, e.g. for QFN, stacked die BGA, and Microelectromechanical Systems (MEMS) packages. Therefore, there is a strong need for design recommendations of CSPs. Besides, failure mechanisms of CSPs under popcorn, board level solder joint

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reliability under thermal cycling test and drop test, are still not well investigated. For example, handheld telecommunication devices are susceptible to drop impact, but there is very little research work done on these CSPs.

Computer-aided-engineering (CAE) or computer modeling becomes highly demanded in the reliability analysis of IC packages due to the recent advances in high-speed computer and development of more sophisticated finite element modeling (FEM) software. CAE is a convenient tool for virtual-prototyping [2] and design for reliability [3]. Traditional design-build-test-redesign type of package development cycle is no longer efficient for competitive semiconductor industry, which emphasizes on short time-to-market. For standard package and board level reliability tests, typically it can take up to 3-4 months to complete. The tests also require expensive test equipment and manpower for data collection. With validated computer models, the Design of Experiment (DOE) studies of package geometry, material properties, and test conditions become more efficient, with saving in time, cost and manpower to the company. Figure 1.1 describes the role of CAE in the new package development. The optimized design is proposed by CAE to shorten the package development cycle. Besides, CAE is also useful for new package validation to evaluate the feasibility of new package concept without any investment in prototyping and testing [4].

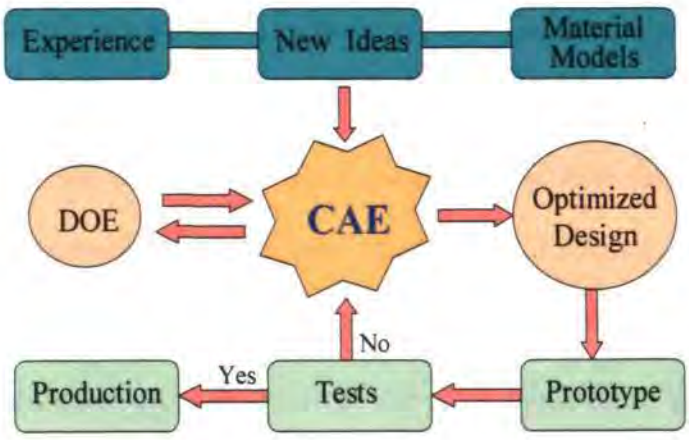

Figure 1.1 Role of CAE in new package design

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1.2 OBJECTIVES

The objectives of this thesis research project are to

1) understand physics of failures of CSPs under pressure cooker test, moisture sensitivity test, thermal cycling test, and drop impact test, which determine the package and board level reliability performance.
2) establish new modeling methodologies which are lacking in current research, e.g., integrated package stress modeling and drop impact life prediction.
3) develop a series of advanced multiphysics models with good correlation to experimental test results, as tools for design for reliability.
4) apply the validated models with detailed DOE design analysis on various types of advanced CSPs, so that design guidelines can be recommended to improve or even optimize the package and board level reliability.

1.3 SCOPE

The modeling analyses are divided into two main categories: package and board levels (see Figure 1.2). For package level, an integrated package stress model is proposed to study the combined effects of moisture diffusion, heat transfer, thermo-mechanical stress, hygro-mechanical stress, vapor-pressure-induced stress, and coupled with fracture mechanics analysis. As for board level, solder joint reliability during thermal cycling test and drop test is the main concern, and life prediction models are needed. For each of the eight main types of models, it requires detailed knowledge of material models and constitutive equations. The theory of physics for each model has to be well-understood. ANSYS/Mechanical/LS-DYNA software is applied for modeling. The computer programs written are fully parametric, suitable for design analysis with material or geometry variations. For moisture and hygroswelling material

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properties, special material characterization techniques are required due to lack of published data from material suppliers. Most of the modeling results are compared and correlated with the actual reliability tests performed by other researchers.

The advanced CSPs studied cover TFBGA, QFN, WL-CSP packages of the current technology. Some variations of these CSPs are also be studied, following the trends of technology over the past 1-2 years, e.g., Conduction-cooled BGA (C^2BGA), PowerQFN, stacked die BGA, MEMS package, and Integrated Passives Device (IPD).

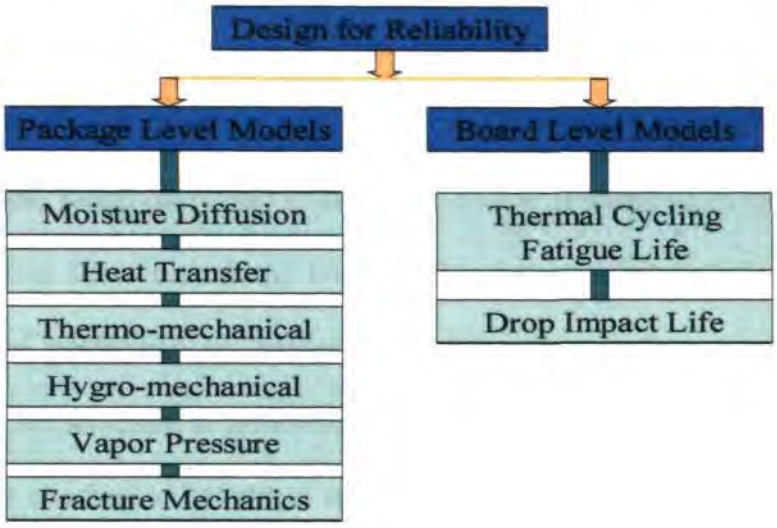

Figure 1.2. Types of package and board level reliability models established

1.4 THESIS LAYOUT

The thesis is divided into 9 main chapters: introduction, literature review, moisture diffusion and hygroswelling modeling, integrated package stress modeling, board level solder joint reliability modeling, applications of solder joint fatigue modeling, board level drop impact modeling, and conclusions and recommendations. In each of the main chapters, there is an individual section on introduction, theories applied or established, descriptions of models, reliability tests results, modeling results, and summary for that particular topic.

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CHAPTER 2 LITERATURE REVIEW

2.1 ELECTRONIC PACKAGING

An electronic or IC package is the housing which assures environmental protection to the IC chip and provides for complete testing and high-yield assembly to the next level of interconnection [5]. Usually, there are three main levels of packaging, i.e. package, board, and system levels.

At level 1 packaging, the IC is assembled into a package such as Quad Flat Pack (QFP) or Ball Grid Array (BGA) using wirebonding or flip-chip bumping assembly techniques. Figure 2.1 shows an example of typical process flow for BGA package. Firstly, epoxy die attach (polymer) is dispensed on top of substrate (a chip carrier), and a piece of silicon die is placed and bonded after thermal curing of die attach. Then, wirebonding is performed to connect the die with substrate using gold wires. Subsequently, the structure is protected by epoxy mold compound (molding). Lastly, solder balls are attached to bottom of substrate, to provide a path for signal to transmit to the next level of interconnect, i.e. board level.

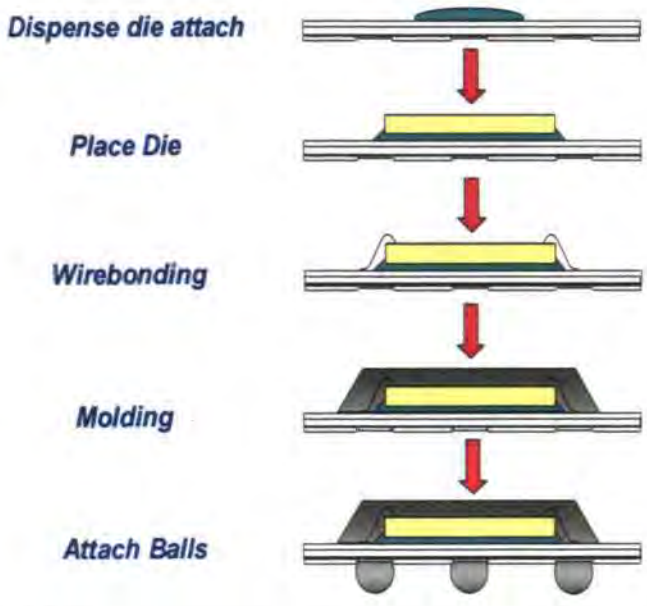

Figure 2.1. Typical assembly processes of a BGA package

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At Level 2 packaging, the IC package is mounted to the printed circuit board (PCB) using SMT (surface mount technology). The solder balls are melted and solidified to connect the package and PCB. Finally, the board sub-assembly can be assembled into a system (Level 3 packaging), e.g. a motherboard of personal computer or a mobile phone, as a final functional product.

Figure 2.2 shows an example of IC packaged in a flip-chip CSP, being assembled to a PCB, and finally added to a mobile phone. The reliability of CSPs at both package and board level is the main focus in this thesis, as it will affect the functionality of final product. Packaging has four major functions, i.e. signal distribution, power distribution, heat dissipation, and mechanical/environmental protection [6]. The emphasis of this thesis is to enhance the mechanical reliability of CSPs. In addition, package components must be manufactured and assembled at affordable costs. Therefore, the design guidelines recommended in the following chapters are ensured to be practical, studied according to industrial needs. Sometimes, a compromise may be required between reliability and cost.

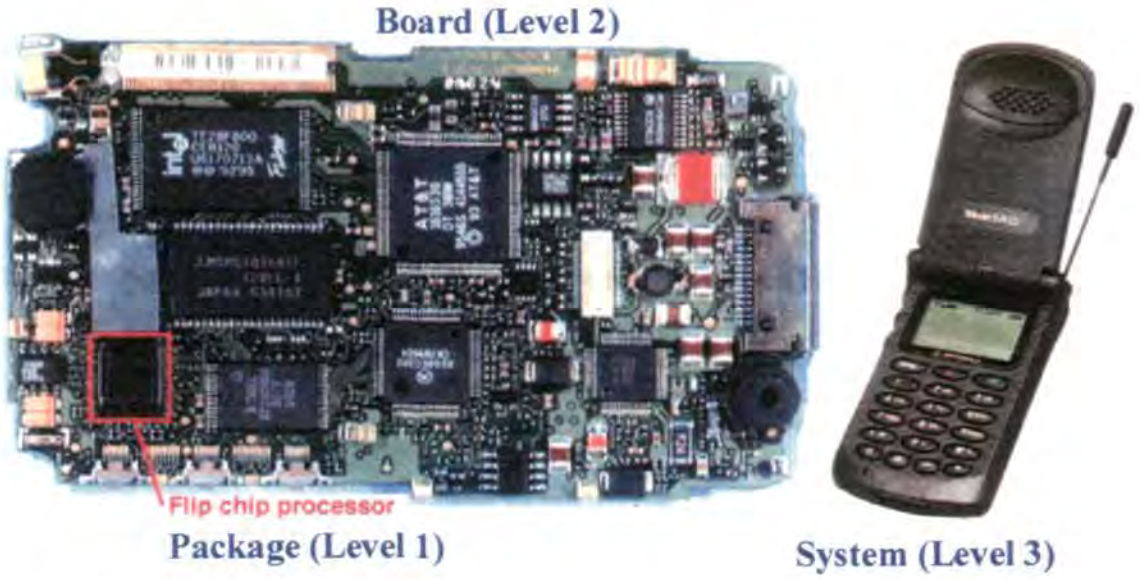

Figure 2.2. Mobile phone assembly at package, board and system levels

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2.2 MODELING OF CSP

The trend of microelectronics product today is moving towards high density and low cost integrated circuit packaging [7]. These factors have promoted the development of CSPs [8-11] such as fine-pitch BGA, FCBGA, wafer-level package (WLP), and QFN. Figure 2.3 shows the evolution of electronic packages over the past few decades, with development moving towards CSPs.

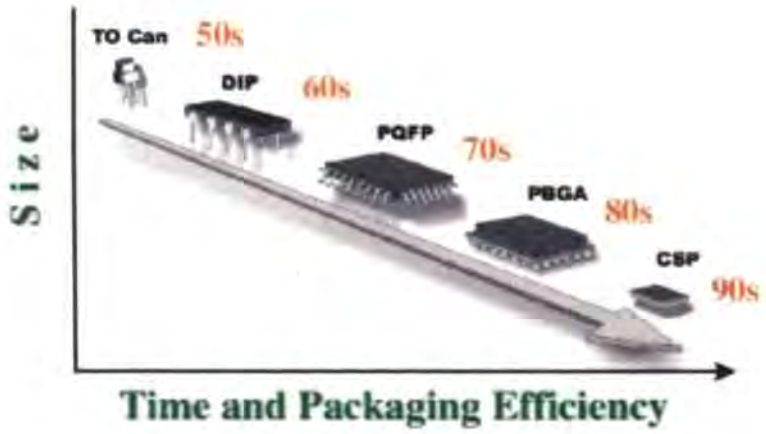

Figure 2.3. Evolution of electronic packages

However, due to the requirement of fast time-to-market, new types of CSPs usually are designed based on previous experience of bigger-size IC packages. It usually takes at least 1-2 years to develop comprehensive validated models on all aspects of package reliability. Therefore it is not surprised that most publications in this area of research, are based on CSPs that are developed at least one year ago. To cope with this practical design constraint, the types and scope of CSPs studied in this thesis are reviewed from time to time to ensure that the latest CSP designs are considered. For example, recent technology advancement and interest in stacked-die CSPs, MEMS package, lead-free solder joint, and drop impact test are also included in the later stage of research work.

The current literatures available on CSP modeling are very focused on one particular type of CSP and certain reliability issues [12-22], e.g., package warpage, die cracking,

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delamination, and solder joint fatigue. IC package design should be an integrated process, with consideration of all aspects of reliability concerns. It may require a compromise in design, e.g., lead-free solder is useful to enhance the solder joint fatigue life under thermal cycling test, but may not for drop test. Therefore, this thesis provides comprehensive modeling analyses on both package and board level reliability modeling. To ensure sufficient depth of modeling, only three types of most popular CSPs, i.e. TFBGA, QFN, and WL-CSP, are chosen as test vehicles. QFN, in particular, has relatively few numbers of publications [23-26]. This thesis has contributed to several new publications related to original research of QFN.

In literature, usually only effects of a few design parameters of interest are studied by modeling [13-14]. In this thesis, most practical design parameters and variations are considered, e.g., die area size, die thickness, package area size, package thickness, substrate and board thickness, solder joint size and shape, mold compound and die attach materials. The models created are fully parametric, and convenient for DOE type of analysis which involves large matrix of design cases.

2.3 MOISTURE DIFFUSION MODELING

Numerous studies in the literature [27-37] reported the damaging effect caused when plastic packages are stored in a noncontrolled humidity environment. During solder reflow of surface mount devices, the temperature of package is raised to more than 220°C (see Figure 2.4). The moisture absorbed in the plastic package becomes vaporized and exerts a high pressure along the critical interfaces. This could induce a failure mechanism often referred to as "popcorn" package cracking [38].

Moisture ingress, either through the bulk encapsulant or along the interface between the leadframe/substrate and mold compound, can accelerate delamination in plastic

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packages. At each interface, moisture can hydrolyze the epoxy, degrading the interfacial chemical bonds. However, different mold compound materials respond differently to moisture exposure. In addition, surface cleanliness is a crucial requirement for good adhesion. Oxidized surfaces, such as copper-alloy leadframes exposed to high temperatures, often lead to delamination [6].

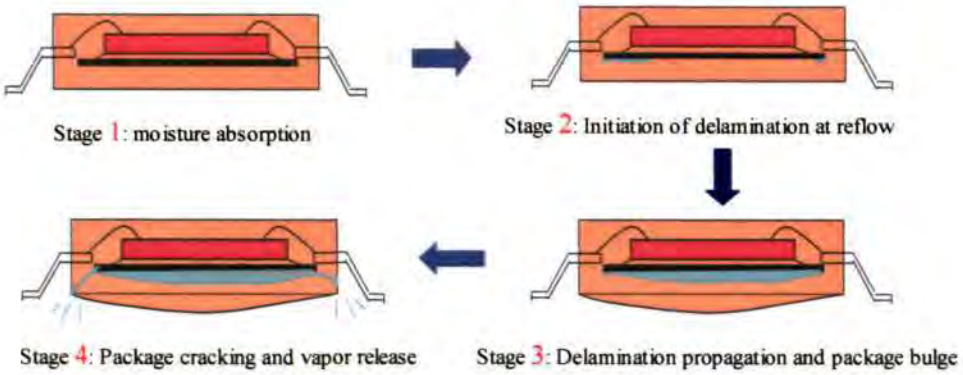

Figure 2.4. Process of package delamination and popcorn failure

Poborets et al. [39] showed that there is a relation between package weight gain and package cracking or delamination. Kitano et al. [40] showed that the package cracking is not controlled by the absolute moisture weight gain, rather it is due to the local moisture concentration at the critical interface. Moisture transport models developed for plastic encapsulated packages are readily available [41] but cannot be easily extended to account for multi-layer materials used to fabricate typical CSPs.

Mass transfer is mass in transit as the result of a species concentration difference in a mixture. In modeling, the transient moisture diffusion equation is analogous to heat conduction, and it can be described by Fick's Second Law [42] as

$$\frac{\partial C}{\partial t} = D\left(\frac{\partial^2 C}{\partial x^2} + \frac{\partial^2 C}{\partial y^2} + \frac{\partial^2 C}{\partial z^2}\right) \tag{2.1}$$

where C is the local moisture concentration, x, y, z are the spatial coordinates, D is the diffusivity which measures the rate of diffusion, and t is the time. Just as a temperature

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gradient constitutes the driving potential for heat transfer, a moisture concentration gradient in a package provides the driving potential for transport of moisture.

Assuming 1-dimensional moisture diffusion in a thin disc specimen, by integrating Eq. (2.1) over time and space (x), the moisture uptake of the specimen when exposed to a constant temperature and humidity environment is described as [43]

$$\frac{M_t}{M_{sat}} = 1 - \sum_{n=0}^{\infty} \frac{8}{[(2n+1)\pi]^2} \exp\left(\frac{-D(2n+1)^2\pi^2 t}{h^2}\right) \tag{2.2}$$

where M_t is the mass of moisture absorbed at time t, M_{sat} is the saturated mass of moisture absorbed, and h is the thickness of the specimen.

However, unlike temperature, the moisture concentration is discontinuous along the bi-material interface. Therefore, Galloway and Miles [43] introduced a new dependent variable, partial pressure, which is continuous across the multi-material interfaces, to resolve this computational problem. Eq. (2.1) can be rewritten as

$$\frac{\partial P}{\partial t} = D\left(\frac{\partial^2 P}{\partial x^2} + \frac{\partial^2 P}{\partial y^2} + \frac{\partial^2 P}{\partial z^2}\right) \tag{2.3}$$

where P is partial pressure, defined as

$$P = \frac{C}{S} \tag{2.4}$$

where S is solubility of gas in the solid.

However, this approach has a fundamental limitation, i.e. requiring moisture to retains its gas state in the solid package material. This is not the case for most IC packages, as usually the moisture absorbed is condensed as liquid water in the microvoids [44]. In Section 3.4.1, another moisture modeling methodology applied in this research will be highlighted. It uses wetness or normalized moisture concentration

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approach, as compared to partial pressure method mentioned above. ANSYS software can only accept the wetness approach, and therefore it is applied in the model.

Previously, moisture diffusion modeling was performed by researchers [45] on older leaded packages (eg. TQFP and SOJ) and larger PBGA packages. There is a lack of research related to moisture diffusion modeling of CSPs. The focus of this thesis is to apply the established moisture diffusion model on the analysis of CSPs such as FCBGA with no-flow underfill and QFN, which are susceptible to moisture-induced failures, but have relatively very few publications in this area of research.

2.4 HYGROSWELLING MODELING

Polymeric materials swell when absorbs moisture. Each material has different swelling rate. The mismatch in expansion induces so called hygroswelling or hygro-mechanical stress, and it is analogous to thermo-mechanical stress. The theories of hygroswelling modeling applied will be presented in Section 3.4.2.

While some researchers [46-51] have reported the adverse effects of hygro-swelling on package integrity, this type of analysis has yet to become a common practice. Its effect is usually ignored in the analysis of package stress and fracture. The limitation is mainly because [52]

a) Unlike coefficient of thermal expansion (CTE), material data on coefficient of moisture expansion (CME) is lacking. There is no standard characterization procedure.

b) Hygroswelling stress analysis requires prior knowledge of moisture distribution in the package, which can only be obtained through modeling. Moisture diffusion modeling, especially of multi-material system, remains unfamiliar to many researchers.

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c) The magnitude of hygroswelling strain was deemed to be insignificant compared to that of thermal strain.

The values of CME have been measured for different types of package materials [53], i.e. die attach, underfill, mold compound, and BT substrate. Nguyen et al. [47] has reported measurement of CME for two commercially available mold compound materials at room temperature. Liu et al. [54] has established a model which can fundamentally explain the shift of the crack-tip loading mode from sliding to opening mode during moisture absorption. They pointed out that the CME is an important parameter in influencing package fracture. The research in this thesis emphasizes on measurement of CME and application of hygroswelling modeling in QFN and FCBGA with no-flow underfill, which no researcher has studied before.

2.5 VAPOR PRESSURE MODELING

Moisture absorption and the ensuing high vapor pressure generated is known to induce popcorn failure [55-58]. Package cracking results from internal stresses generated by the reflow solder temperature profile during the assembly of plastic-encapsulated devices on circuit cards.

JEDEC (Solid State Technology Association) standard [59] is widely used to conduct reliability tests on moisture sensitivity of the electronic packages. Modeling of vapor pressure within the package during reflow is the key element in understanding the physics and mechanism of moisture-induced failures. Previous researchers [40, 43-45] assumed that the delamination exists before reflow, and considered the vapor pressure as traction loading subjected to the delaminated interfaces. There were some studies done and a few methods were proposed to estimate the vapor pressure acting on the delaminated interface. Bhattacharyya et al. [60] proposed that

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$$P = \frac{kT_j N_a H_i \rho_{i.sat} \exp\left(2740\left[\frac{1}{T_i} - \frac{1}{T_j}\right]\right)}{M_o} \qquad (2.5)$$

where P = vapor pressure in the package

$T_{i,j}$ = initial and reflow temperature respectively

N_a = Avogadro's number (6.023×10^{23} /mol)

H_i = humidity

$\rho_{i,sat}$ = initial density of the saturated vapor at T_i

M_o = molecular weight of the water molecules (18gm/mol)

On the other hand, Sawada et al. [61] stated that

$$P = C_1 \cdot A \cdot RH \cdot T \qquad (2.6)$$

where P = vapor pressure in the package

C_1 = 4.8×10^{-3}

A = a constant depends on package resin

RH = relative humidity of the surrounding vapor

T = reflow temperature

Since the vapor pressure is generated anywhere in the package, it is necessary to investigate the whole field vapor pressure distribution before the package delamination. The research in this thesis applies the theories developed by Fan and Tee [62-63], and implements the whole-field vapor pressure modeling using finite element method. For the first time, the vapor pressure distribution in QFN package is well studied here. This approach is different from other vapor pressure theories, as it does not require assumption of delamination to occur before reflow. More details of vapor pressure modeling will be given in Section 4.2.5.

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2.6 INTERFACIAL FRACTURE MECHANICS

Strength of material approach usually uses stress as the failure criteria, e.g., when stress is larger than strength, failure will occur. However, when there is a defect or flaw in the material, the stress is infinite at the crack tip. The modeling stress results are usually mesh-size dependent, and only useful for relative design comparison. Therefore, for delamination modeling, fracture mechanics approach has to be applied with consideration of both stress and crack size.

In some cases, delamination may be initiated due to high interfacial stresses. Although there is no clear criterion to predict the initiation of delamination, one approach is to determine the interfacial shearing and peeling stresses, and make a comparison with the interfacial shear and peel strength. Delamination is expected to initiate, when the following equation is satisfied [64]:

$$\left(\frac{\sigma_{xz}}{\sigma'_{xz}}\right)^2 + \left(\frac{\sigma_{zz}}{\sigma'_{zz}}\right)^2 \geq 1 \qquad (2.7)$$

where σ_{xz} and σ_{zz} are interfacial shear and peel stresses respectively, and σ'_{xz} and σ'_{zz} are experimentally-determined interfacial shear and peel strength respectively. Once initiated, the delamination may or may not propagate, depending on the energy available for it to propagate. Interfacial fracture mechanics is typically applied to predict the propagation of delamination. Detailed description of this complex topic is beyond the scope of this thesis. The focus here is more on application of common interfacial fracture mechanics modeling methods in delamination analysis of IC packaging.

Figure 2.5 shows that there are three main types of fracture modes, i.e. opening (Mode 1), shearing (Mode 2), and tearing (Mode 3). For 2-dimensional analysis, usually only Modes I and II are considered.

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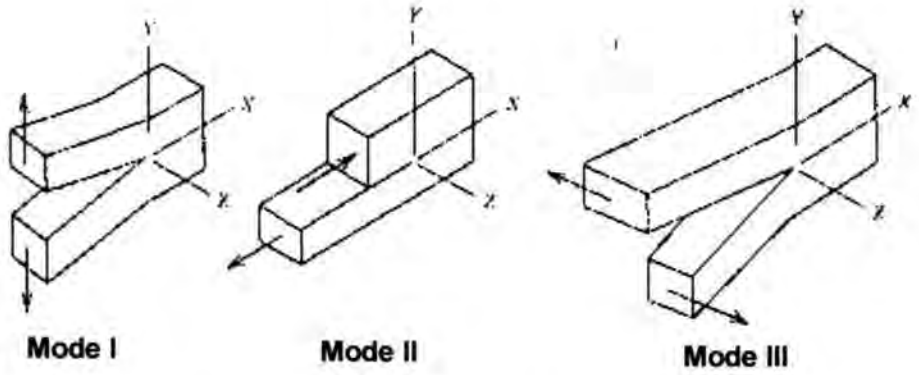

Figure 2.5. Three types of fracture modes

Due to the elastic mismatch of a bi-material, an interface crack tip as shown in Figure 2.6 experiences both normal and shear stresses. The elastic mismatch between the two materials is governed by the Dundurs' parameters (α, β) [65]. For plane strain condition,

$$\alpha = \frac{(1-\nu_2)/\mu_2 - (1-\nu_1)/\mu_1}{(1-\nu_2)/\mu_2 + (1-\nu_1)/\mu_1} \tag{2.8}$$

$$\beta = \frac{1}{2}\frac{(1-2\nu_2)/\mu_2 - (1-2\nu_1)/\mu_1}{(1-\nu_2)/\mu_2 + (1-\nu_1)/\mu_1} \tag{2.9}$$

where ν_1 and ν_2 are the Poisson's ratios of the bi-materials, μ_1 and μ_2 are the shear moduli of the bi-materials. Another important bi-material constant related to the Dundurs' parameters is the oscillatory index

$$\varepsilon = \frac{1}{2\pi}\ln\frac{1-\beta}{1+\beta} \tag{2.10}$$

While the concept of critical stress intensity factor (SIF) to predict fracture in structures have already been developed and applied to other areas of engineering, the first suggestion of applying SIF criterion to actual plastic IC packages appears to be Hattori et al. [66]. Later, other researchers [67-69] have applied various fracture mechanics methods in delamination and popcorn analysis.

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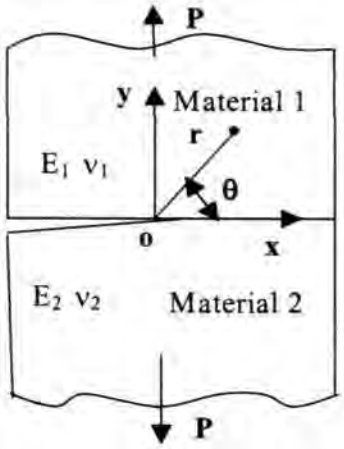

Figure 2.6. Interface crack

Unlike fracture mechanics of homogeneous material, the theories of interfacial fracture mechanics are much more complicated [70-72]. The stress near the crack tip appears to be oscillating. Several numerical methods such as J-integral, Crack Tip Opening Displacement (CTOD), and Virtual Crack Closure (VCC) methods, can be applied to obtain the numerical solution [73-76]. Lin and Tay [74] employed a modified J-Integral methodology for analyzing interfacial delamination under hygrothermal loading during solder reflow. An initial defect or delamination is assumed to exist at the interface.

The focus of research here is to apply VCC method (see Section 4.2.7 for further details) in the delamination analysis of QFN package. There is no other publication related to interfacial fracture mechanics modeling of QFN. More importantly, an integrated package stress model is established with considerations of multiphysics (whole-field distribution of moisture, temperature, and vapor pressure), combined stresses (thermo-mechanical, hygro-mechanical, and vapor-pressured induced), and interfacial fracture mechanics. Currently, there is a lack of package delamination model with detailed considerations in this area of research.

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2.7 SOLDER JOINT FATIGUE MODELING

Fatigue is a common failure mechanism for most structural and electrical failures, known to occur in metals, polymers and ceramics. For a simple flip-chip on board structure, there is CTE thermal mismatch between the silicon chip (2.8 ppm/°C) and FR4 board (16 ppm/°C). During cooling, FR4 board shrinks more than silicon die, and therefore the solder joints are deformed inwards (see Figure 2.7). Under repeated heating and cooling cycles during thermal cycling test, irreversible plastic and creep strains are induced in the solder joints, causing fatigue failure to the component.

Figure 2.7. Deformation of solder joints during thermal cycling test

Generally, there are two main approaches in determining the number of cycles to fatigue failure. The first approach is stress-controlled fatigue (to be discussed in Section 2.8), using elastic stress as failure criterion to calculate the fatigue life, usually applicable for high-cycles fatigue such as vibration. The second approach is strain-controlled fatigue, applying plastic or creep strain to predict the life of low-cycle fatigue, e.g., thermal cycling test.

Solder joint interconnects serve two important purposes: 1) to form the electrical connection between the component and the substrate, and 2) to form the mechanical bond that holds the component to the substrate. Predicting solder joint fatigue has been one of the electronic industry's most difficult problems. Successful prediction of solder joint fatigue failure depends on the ability to accurately model the behavior of solder joints.

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For typical solder materials (e.g. 63Sn37Pb), creep is the dominant process during thermal cycling condition. Steady-state creep behavior of solder can be expressed by a constitutive equation in the form of [77]

$$\frac{d\epsilon_s}{dt} = C_{ss}[\sinh(\alpha\sigma)]^n \exp(\frac{-Q_a}{kT}) \quad (2.11)$$

where $\frac{d\epsilon_s}{dt}$ is the steady state strain rate, k is the Boltzmann's constant, T is the absolute temperature, σ is the applied stress, Q_a is the apparent activation energy, n is the stress exponent, α is the stress level at which the power law dependence breaks down, and C_{ss} is a constant.

There are many approaches used by researchers [77-106] in the modeling of solder joint fatigue life, e.g. stress-based, plastic/creep strain-based, energy-based, and damage accumulation-based [107]. Darveaux methodology [77-79] is a common approach used in the fatigue modeling which applies both energy and damage accumulation-based theories. Over the past few years, this model has been widely applied by many researchers [80-81]. In Darveaux's method, crack initiation life (N_o) and crack propagation life (N_p) are calculated:

$$N_o = K_1 (SED)^{K_2} \quad (2.12)$$

$$N_p = a / [K_3 (SED)^{K_4}] \quad (2.13)$$

where K_1, K_2, K_3, and K_4 are constants, SED is strain energy density per cycle, and a is the length of critical pad interface. The characteristic life (η) of solder joint is given as

$$\eta = N_o + N_p \quad (2.14)$$

For plastic strain-based fatigue models, Coffin-Manson, Solomon, Engelmaier, and Miner predict the fatigue life based on calculation or experimental determination of the applied plastic shear strain. Coffin-Manson fatigue model was the most popular approach before the introduction of Darveaux's model. The total number of cycles to

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failure (N_f) is dependent on the plastic strain amplitude ($\Delta\varepsilon_p$), the fatigue ductility coefficient (ε'_f) and the fatigue ductility exponent (c). The relationship among these variables is given by the well-known Coffin-Manson Equation [82]:

$$\frac{\Delta\varepsilon_p}{2} = \varepsilon'_f (2N_f)^c \tag{2.15}$$

Experimental data are required to determine the constants and are typically collected by application of strain gauges.

Solomon's [83] low cycle fatigue model relates the plastic shear strain range ($\Delta\gamma_p$) to number of cycles to failure (N_p)

$$\Delta\gamma_p N_p^{\alpha} = \theta \tag{2.16}$$

where α and θ are constants. This fatigue model has been applied to leaded plastic quad flat packages and underfilled flip-chip by various researchers. However, since this model does not account for creep, it has limited practical use for solder joints [83-85].

The fatigue life predicted by Engelmaier fatigue model [83] is given by

$$N_f = \frac{1}{2}\left[\frac{\Delta\gamma}{2\varepsilon'_f}\right]^{1/c} \tag{2.17}$$

where $\Delta\gamma$ is total shear strain, ε'_f is fatigue ductility coefficient, and the variable, c, is a function of frequency and temperature. Pang et al. [83] reported $2\varepsilon'_f$ of 0.65 in applying Engelmaier's model to underfilled flip-chip. This fatigue model improves on Solomon's model and Coffin-Manson's model by including effects of cyclic frequency, temperature, and elastic-plastic strains.

Creep can be separated into two possible mechanisms, matrix creep and grain boundary creep. Knecht and Fox [86] have proposed a simple matrix creep fatigue model relating the solder microstructure and the matrix creep shear strain range:

$$N_f = \frac{C}{\Delta\gamma_{mc}} \tag{2.18}$$

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where C is a constant, which is dependent on failure criteria and solder microstructure, and $\Delta\gamma_{mc}$ is the strain range due to matrix creep.

By applying Miner's linear superposition principal, both plastic and creep strain can be considered in a strain-based fatigue model. This model combines the Solomon fatigue model with the Knecht and Fox creep model, and is given by [83-85]

$$\frac{1}{N} = \frac{1}{N_P} + \frac{1}{N_C} \tag{2.19}$$

where N is total number of cycles to failure, N_p is fatigue life due to plastic strain, and N_c is fatigue life due to creep strain.

For fatigue modeling of area-array IC packages, energy-based model is more popular, as the accuracy of absolute life prediction usually is within ±2x variation (by Darveaux's method), and the relative trend of results are consistent when compared with experimental data. However, Darveaux's model and correlation constants were originally developed for large plastic BGA packages, and the accuracy of results is compromised when it is applied in the analysis of fine-pitch CSPs. In this thesis, a modified Darveaux's method is proposed for advanced CSPs studied, using a global-local modeling approach. This novel method has excellent correlation with solder joint fatigue lives obtained from the experiments. Two sets of unique correlation constants are established for accurate fatigue life prediction of TFBGA and QFN packages. Currently, these correlation constants are lacking in research publications, especially for advanced CSPs. In addition, the global-local model approach helps to significantly reduce the long computational time, and maintain the same level of accuracy.

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2.8 DROP IMPACT SIMULATION

An impact is a forceful collision or contact between two bodies over a very short period of time. Due to increasing demand of mobile phone, drop impact has become a critical concern to both consumers and manufacturers. Board level drop test is a form of accelerated test to evaluate the robustness of package under impact.

The governing equation of a one-degree-of-freedom linear dynamic system can be expressed as

$$M\ddot{x} + C\dot{x} + Kx = F \tag{2.20}$$

where M, C and K are the system mass, damping coefficient, and spring constant respectively, while x, $\dot{x}$, and $\ddot{x}$ are the displacement, velocity and acceleration respectively, and F is force, usually function of time.

The overall drop impact process involves a series of energy transformation. Firstly, the drop table falls down freely from a certain height, and its potential energy is converted into kinetic energy. Then, the drop table hits the strike surface and creates an impact pulse with certain G level and pulse duration. Finally, the impact forces are transmitted through mounting screws to PCB, solder joints, and components. At the same time, the initial force causes the PCB to bend and induce stress in solder joints.

From kinematics, the theoretical impact velocity during free fall just before impact, V_b, can be related to drop height, H, by

$$V_b = \sqrt{2gH} \tag{2.21}$$

where g is the gravitational acceleration (9.81m/s^2). According to impulse and momentum theory [108], the velocity after impact, V_a, is in the range between 0 (zero rebound) and -V_b (full rebound). Assuming V_a is some fraction of V_b, $V_a = cV_b$, then

$$-mcV_b - mV_b = -\int_0^T mG(t)dt \tag{2.22}$$

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$$V_b = \frac{1}{1+c}\int_0^T G(t)\,dt \qquad (2.23)$$

where c is the coefficient of restitution, and its value is between 0 (perfectly plastic impact) and 1 (perfectly elastic impact), $G(t)$ is the acceleration at time t during impact, T is the pulse duration, and m is the mass.

Many engineering components must withstand numerous load or stress reversals during their service lives. For stress-controlled cyclic loading, there is a popular S-N diagram (see Figure 2.8) based on empirical data, stating that the fatigue life increases with lower stress amplitude, and there is a fatigue endurance limit where the fatigue life is infinite when the stress level is significantly low [109].

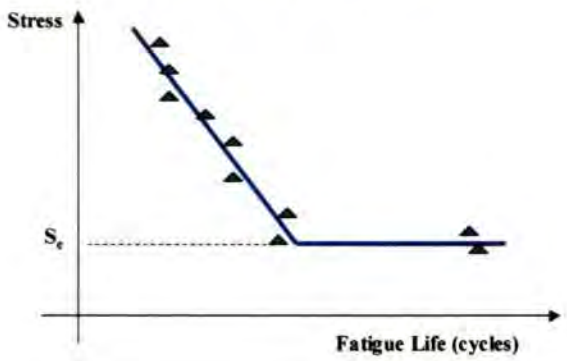

Figure 2.8. S-N diagram for stress-controlled fatigue

Publications related to board level drop test and simulation are very limited [110-114]. Early drop test simulation work was reported by Wu [111-112], who used LS-DYNA to model drop test at both component and product levels. Zhu [113] applied submodeling technique to study the board level BGA drop test, but the experimental work is limited. Sogo and Hara [114] developed a 2-step model to reduce the computational time, and showed some correlation of time-dependent solder ball strain between drop test and simulation. However, the details of drop test parameters such as shock level experienced by the solder joint were not provided. Arra et al. [115] has studied the performance of lead-free solder under dynamic mechanical loading using a

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free-fall drop test. The mechanical shock and random vibration response of personal computer motherboards were measured and modeled by Pitarresi et al. [116]. The effect of strain rate on solder joint failure under mechanical loading was reported by Geng et al. [117].

The state of the art of drop test modeling is only on qualitative analysis for relative design comparison of solder stresses. There has been a lack of life prediction model in the area of research on board level drop test, and it will be addressed in this thesis. For the first time, an accurate quantitative solder joint impact life model is proposed to relate the stress and actual impact life based on power law (see Section 7.6).

2.9 SIMULATION SOFTWARE

In this thesis, a commercial finite element software, ANSYS (Version 6.0), is applied extensively in various areas of modeling (see Figure 2.9). It is a multi-purpose modeling software with capabilities in structural, thermal, fluid, electromagnetics, and multi-physics analyses. It is a user-programmable tool, allowing parametric design analysis. ANSYS is a popular software of choice by many researchers for design analysis of IC packages. In particular, ANSYS/Mechanical is applied for structural (static) and heat / mass transfer analysis using implicit numerical methods, whereas ANSYS/LS-DYNA with explicit solver is used in dynamic simulation of drop impact. The research work in this thesis has resulted in many novel ANSYS models, making a contribution to both academia and industry.

The ANSYS models established do not directly consider the effect of strength or failure criterion (e.g., see Eq. (2.7)). There is no post-failure element which can allow the structure to break when the stress exceeds the strength, i.e. damage occurs.

ANSYS software enables researchers and engineers to perform the following tasks:

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1) Build computer models or transfer CAD models of structures, products, components, or systems.
2) Apply operating loads or other design performance conditions.
3) Study physical responses, such as stress levels, temperature distributions, or electromagnetic fields.
4) Optimize a design early in the development process to reduce production costs.
5) Do prototype testing in environments where it otherwise would be undesirable or impossible (for example, biomedical applications).

A typical ANSYS analysis has three distinct steps, i.e. 1) build the model, 2) apply loads and obtain the solution, 3) review the results. Model generation is usually the most time-consuming part. Therefore, parametric programmed model is preferred over the GUI (Graphical User Interface) model in the research work here. The same model can then be modified conveniently for extensive design analysis.

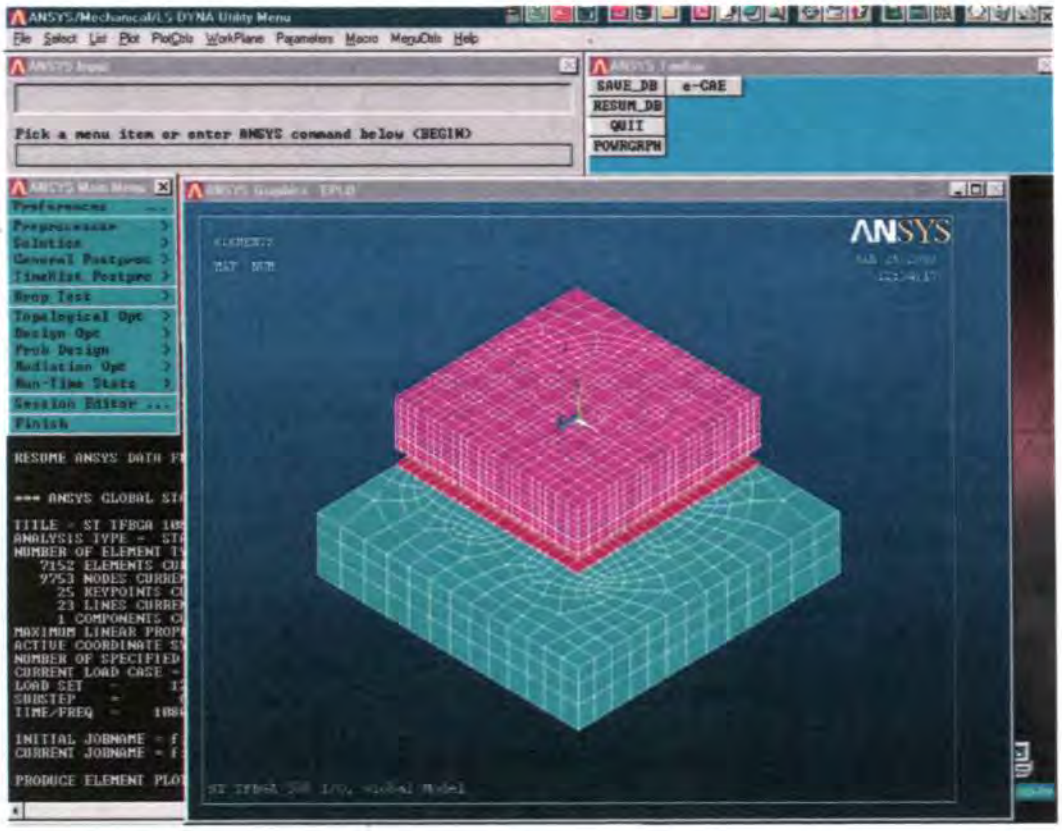

Figure 2.9. A typical IC package model in ANSYS

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The ultimate purpose of a finite element analysis is to re-create mathematically the behavior of an actual engineering system. In other words, the analysis must be an accurate mathematical model of a physical prototype. In the broadest sense, this model comprises all the nodes, elements, material properties, real constants, boundary conditions, and other features that are used to represent the physical system.

In this thesis, sources of thermo-mechanical material properties used as modeling input are mostly provided by respective material suppliers (e.g. CTE and moduli of epoxy materials) or through in-house testing (for special measurement, e.g. CME). For material with unknown Poisson's ratio, usually a value of 0.3 is assumed, as it is a common value for packaging materials at room temperature. This assumption will not change the relative stress comparison of design cases which is the main interest. If there is any inaccuracy in calculation of stress, it can also be adjusted at later stage, e.g. using correlation constants for impact life prediction.

In the solution phase of the analysis, the computer takes over and solves the simultaneous set of equations that the finite element method generates. The results of the solution are:

1) Nodal degree-of-freedom values, which form the primary solution.

2) Derived values, which form the element solution.

The element solution is usually calculated at the elements' integration points.

Several methods of solving the system of simultaneous equations are available in the ANSYS program: sparse direct solution, frontal direct solution, Jacobi Conjugate Gradient (JCG) solution, Incomplete Cholesky Conjugate Gradient (ICCG) solution, Preconditioned Conjugate Gradient (PCG) solution, and an automatic iterative solver option (ITER). The numerical method applied in each solution method is not elaborated here, as it is beyond the thesis scope.

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Nevertheless, suitable solver, i.e. PCG solution, is chosen for the 3D models generated in this research work. The PCG solver is best suited for structural analysis [141]. It is valid for elements with symmetric, sparse, definite or indefinite matrices. This solver is available only for static or steady-state analyses and transient analyses. The PCG solver usually requires less than ¼ of the disk file space used by the frontal solver. Savings increase with the problem size. The PCG solver usually runs faster than the frontal solver for large models (wavefront greater than about 1000). It is especially well suited for large models with solid elements 50000 to 1000000 degree-of-freedom.

After building the model and obtaining the solution, post-processing is required to review the results of an analysis. It is probably the most important step in the analysis, because it helps to understand how the applied loads affect the design, how good the finite element mesh is, and so on. Two post-processors are available: POST1, the general postprocessor, and POST26, the time-history postprocessor. POST1 allows reviewing of results over the entire model at specific load steps and substeps (or at specific time-points or frequencies. On the other hand, POST26 allows reviewing of variation of a particular result item at specific points in the model with respect to time or frequency. It is particularly useful for drop impact simulation, as results throughout the entire impact duration can be extracted.

2.10 SUMMARY

Comprehensive literature review on relevant topics has justified the direction and scope of research here, i.e. integrated package stress modeling, board level solder joint fatigue modeling, and drop impact life prediction modeling. Due to limited writing space available in this thesis, it is challenging to provide detailed literature review for each type of modeling analysis.

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CHAPTER 3 MOISTURE DIFFUSION AND HYGROSWELLING MODELING

3.1 INTRODUCTION

There is an increasing trend toward miniaturization in the electronics industry. Electronics products are getting smaller, lighter and faster which demand for more compact and efficient electronic packaging. The use of flip-chip interconnection has inherent advantages over the conventional wire bonding techniques for electronic packaging in terms of higher packaging density and better performance. No-flow underfill process for flip chip interconnection has gained popularity in the industry during recent years due to its simpler and shorter process flow, compared with conventional capillary flow underfill process. The elimination of assembly steps enables high throughput and reduces process complexity [118]. In addition, the use of snap-cure no-flow underfill material further eliminates the process time. However, the reliability of such package must be examined to ensure its performance.

The no-flow underfill adhesives used in this study are non-filled, as the presence of the fillers might inhibit the solder reflow connection process. In comparison with conventional capillary flow underfill materials, which are highly filled with silica or other filler, the modulus of no-flow underfill is lower while coefficient of thermal expansion (CTE) is expected to be higher. Underfill material is an important factor for reliability of flip-chip BGA (FCBGA) interconnection.

Pressure cooker test (PCT) under 121°C/100%RH, is a stringent accelerated test for moisture-sensitive package, especially with underfill material. The moisture weakens the interfacial adhesion strength, generates internal vapor pressure during reflow, and induces tensile hygroswelling stress on underbump metallization (UBM) during PCT. Previous researchers [53] have shown that hygroswelling of underfill is the key factor

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for UBM failure during PCT. However, so far there is no hygroswelling material characterization and modeling done for no-flow underfill (snap/post-cure) material. No-flow underfill absorbs more moisture than conventional underfill, due to lack of fillers as moisture barrier. Therefore, no-flow underfill is more susceptible to moisture-induced failures.

In this study, FCBGA (8x8mm, 80 I/O), both unmolded and molded packages (see Figure 3.1), are used as the test vehicles for modeling studies and reliability tests. The substrate is similar as used in TFBGA package, which only has 0.22mm thickness. The control case chosen is unmolded FCBGA-8x8, with no-flow underfill type A, and die thickness of 0.525mm. Parametric studies are performed to study the effects of no-flow underfill materials (types A, B & C), package type (molded vs. unmolded), die thickness (0.525 vs. 0.325mm), and substrate size (8x8 vs. 6x6mm) on the stresses of UBM during reflow and PCT. For each case, only one design parameter is varied with respect to the control case. The moisture diffusion modeling (85°C/85%RH) is first performed to study the relative moisture distribution of various underfill materials. Then, the results of moisture diffusion are used in the hygroswelling modeling. Independent thermo-mechanical stress modeling is also applied to calculate the stress during reflow. The failure criteria applied are the maximum normal peeling stress (S_y) and shear (S_{xy}) stresses on UBM, which contribute to the UBM-opening failure during PCT.

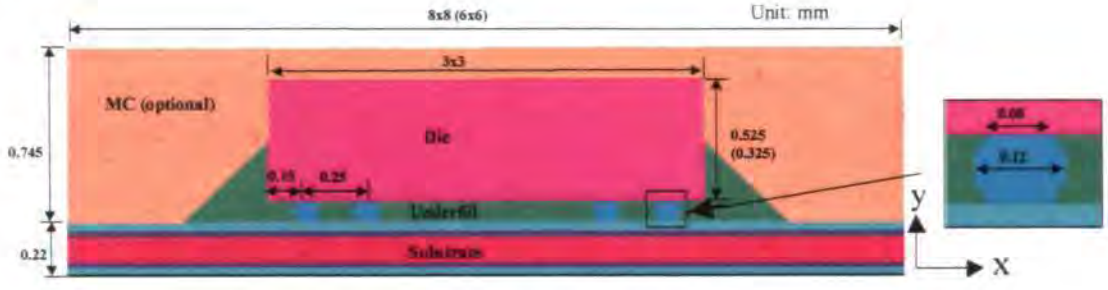

Figure 3.1. Schematic of FCBGA-8x8mm package

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3.2 MATERIAL CHARACTERIZATION

Three types of no-flow underfill (epoxy-based) materials (identified by UF A, B, and C) were obtained from commercial sources. The underfill materials are divided into two categories i.e. snap-cure and conventional cure. Conventional cure type underfill requires additional post curing at 165°C for 1 hour and snap-cure type material requires no further curing as it is polymerized during the solder reflow stage.

In the solder wettability tests, underfill material was first dispensed on the substrate. Two eutectic solder spheres were placed at proximity on the underfill and lightly pressed down such that they were in contact with the copper trace. The specimen was then under reflow. The spreading of the reflowed solder was observed visually and wetting angle was measured with a contact angle meter. The wetting percentage (see Figure 3.2), *w%*, is defined by

$$w\% = \left(\frac{2b - a}{a} \right) \cdot 100\ \% \qquad (3.1)$$

where a is the solder height, and b is half of solder width after reflow. A higher wetting percentage has a lower contact angle, and therefore better wettability.

Figure 3.2. Wettability measurement

The results of solderability and wettability test on Cu/Ni/Au surface are shown in Table 3.1. In this evaluation trial, good wettability is denoting as having a wetting percentage of >80% while poor wettability is classified when the wetting percentage is

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<80%. Underfill-A, B, and C exhibit good solderability and wettability demonstrated by the merging of two eutectic solders balls after the reflow process. Wettability of conventional post-cure underfill is slightly better than snap-cure underfill.

Table 3.1. Results of solderability, wettability, and degree of cure

UF	Cure Condition	Solderability	Wettability	Degree of Cure
A	Snap-cure	Good	83 %	71 %
B	Post-cure	Good	87 %	72 %
C	Snap-cure	Good	81 %	93 %

Differential Scanning Calorimeter (DSC) was used to study the curing profile and curing kinetics of the underfill materials. An uncured sample of about 10mg was placed in a hermetic aluminum pan and heated to about 250°C at a rate of 5°C/min to obtain the curing profile. The heat enthalpy recorded is the energy required to obtain fully cured condition. An exothermic peak exhibits during the curing reaction. The degree of cure can then be determined (see Table 3.1). Underfill-A requires a post cure to achieve fully cured condition and Underfill-B needs a longer post cure time.

Coefficient of Thermal Expansion (CTEs) of cured underfill materials were measured using Thermo-mechanical Analyzer (TMA). No-flow underfill has a much larger CTE value compared with conventional underfill, because it has no low-CTE fillers. The large CTE mismatch among underfill, solder bump, and die may induce high thermal stress. The storage modulus (E) and glass transition temperature (T_g) were determined by Dynamic Mechanical Analyzer (DMA). The results are listed in Table 3.2 as input for modeling. CTE_1 and CTE_2 are CTEs below and above T_g respectively. E_1 and E_2 are moduli below and above T_g respectively. The underfill samples characterized were fully cured to ensure stable material properties during the testing. The characterization of hygroswelling properties will be introduced in Section 3.4.2.

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Table 3.2. Thermo-mechanical material properties

Materials	CTE_1 (ppm/°C)	CTE_2 (ppm/°C)	T_g (°C)	E_1 (GPa)	E_2 (GPa)	Poisson's Ratio
Silicon Die *	2.6	-	-	155	-	0.25
BT Substrate *	15	-	-	21	-	0.35
Copper *	17	-	-	120	-	0.3
Solder Mask *	59	-	-	4	-	0.35
Eutectic Solder Bump *	24.7	-	-	31.7	-	0.4
Underfill A #	78.1	213.2	124	2.4	1.9	0.35
Underfill B #	86.1	223.7	129	3.1	1.9	0.35
Underfill C #	55.8	159.9	120	2.7	1.65	0.35
Mold Compound #	8	36	147	24.5	-	0.3

Sources: * material suppliers, # in-house testing. *E* of UF and MC are storage modulus.

3.3 RELIABILITY TESTS

The test vehicle, TFBGA 8x8 packages with daisy-chained die and two categories of underfill materials, i.e. snap-cure type and conventional post cure type were selected for assembly. The evaluation matrix was divided into molded and unmolded FCBGA to understand their reliability. After assembly, the samples were baked at 125°C for 24 hours before subjecting to four different reliability tests condition as shown in Table 3.3. Electrical continuity test was selected as the failure criteria, and resistance measurements were taken at various intervals to monitor the continuity of the daisy chain.

Table 3.4 shows the reliability test results (failure rates) of unmolded and molded FCBGA packages. For each case, 30 samples were tested. The packages have passed most of the reliability tests such as thermal cycling test (TCT), high temperature storage test (HTS), and temperature humidity storage test (THS), but failed the PCT after 168 hours (after Level-3 moisture preconditioning and reflow). For unmolded FCBGA, underfill material A is the best choice. It passes all the reliability tests, except PCT with

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10% failure. For the molded version, underfill material B has the best performance, with 10% failure in PCT. Generally, unmolded FCBGA has better PCT results than molded FCBGA.

Table 3.3. Reliability test conditions

Reliability Test		**Stress Conditions**	**Inspection Intervals**
Precond. JL3 + Thermal Cycling	TCT	-40 / +150°C	100, 500, 1000 cycles
Temp. Humidity Storage	THS	85°C / 85%RH	1000 hrs
Precond. JL3 + PCT	PCT	121°C/100%RH 2 atm	0, 96, 168hrs
High Temp. Storage	HTS	150°C	500, 1000hrs

Table 3.4. Reliability test results (failure rates) of FCBGA

UF	**Package Type**	**TCT 1000 cyc**	**THS 1000 hr**	**PCT 168 hr**	**HTS 1000 hr**
A	Unmolded	0 %	0 %	10 %	0 %
	Molded	0 %	0 %	100 %	0 %
B	Unmolded	0 %	0 %	30 %	0 %
	Molded	0 %	0 %	10 %	0 %
C	Unmolded	0 %	0 %	63 %	0 %
	Molded	7 %	0 %	100 %	27 %

Typical failures after PCT are UBM-opening and die/underfill delamination (see Figure 3.3). It is suspected the failures are due to hygroswelling of no-flow underfill. Therefore, there is a need for comprehensive modeling to analyze the package on moisture distribution, thermal stress during reflow, and hygroswelling stress during PCT.

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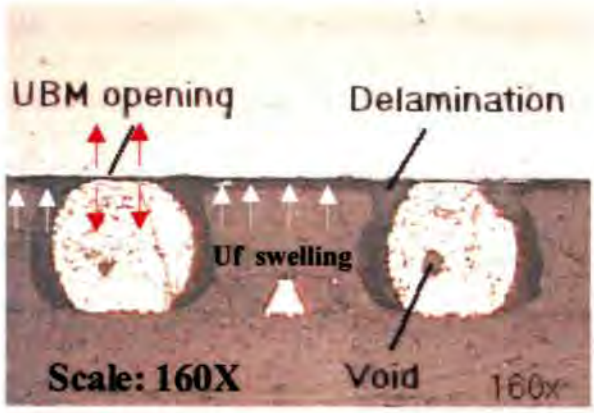

Figure 3.3. Typical moisture induced failures during PCT

3.4 Finite Element Models

3.4.1 Moisture Diffusion Model

The research work here applies another approach to normalize the moisture concentration, i.e. moisture wetness, w, as the field variable, which is also continuous across multi-material interface [44, 52]. It is defined as

$$w = \frac{C}{C_{\text{sat}}}, \quad 1 \geq w \geq 0 \tag{3.2}$$

where C_{sat} is the maximum moisture concentration that can be absorbed by the material, the lower limit $w = 0$ means it is dry, and the upper limit $w = 1$ means it is fully saturated with moisture. The Eq. (2.1) can be rewritten as

$$\frac{\partial w}{\partial t} = D\left(\frac{\partial^2 w}{\partial x^2} + \frac{\partial^2 w}{\partial y^2} + \frac{\partial^2 w}{\partial z^2}\right) \tag{3.3}$$

and it may be solved as a typical transient heat transfer problem using any commercial FEA software with implicit solver. The time step applied in modeling is 604.8s.

2D FEA half-model (due to symmetry) is established for the FCBGA, with fine meshing around the critical region (see Figure 3.4). Same geometry model is used for moisture, hygroswelling, and thermo-mechanical modeling, but different element types,

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loadings, and solutions are applied. For moisture absorption modeling, the initial condition is $w = 0$ for the whole package, and the boundary condition is $w = 1$ at the external interfaces which are exposed to ambient moisture (see Figure 3.5). Centerline of package is symmetric (mass flux = 0).

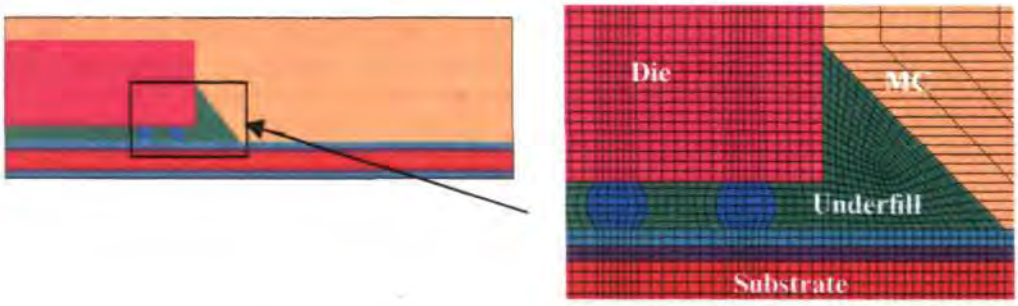

Figure 3.4. FEA model of molded FCBGA

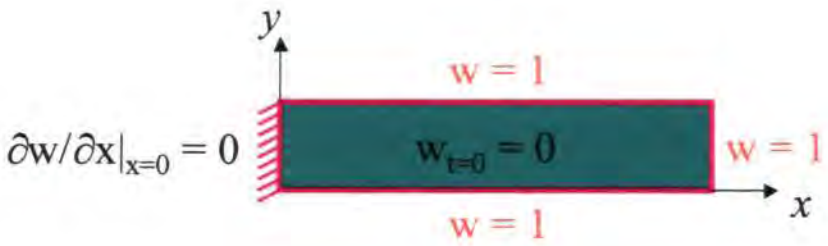

Figure 3.5. Initial and boundary conditions of moisture diffusion model

The moisture properties, i.e. diffusivity and C_{sat}, characterized under 85°C/85%RH, are listed in Table 3.5. The moisture properties can be obtained by curve-fitting the moisture weight gain data of a thin disc specimen with the solution of 1D moisture diffusion. Underfill B has the largest C_{sat}, and Underfill C has the highest diffusivity. Die, copper, and solder bump are assumed to be impermeable to moisture, i.e. do not absorb moisture, so they have zero diffusivity and C_{sat}. Besides, the moisture diffusion rate on interfaces of adjacent materials may be higher due to possible delaminated area or voids filled with air. For simplicity, this effect is not considered in the model.

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Table 3.5. Moisture and hygroswelling material properties at 85°C/85%RH

Materials	D (mm^2/s)	C_{sat} (mg/mm^3)	CME (mm^3/mg)	Total Hygro Strain (C_{sat} x CME)
Underfill A	9.02e6	0.0152	0.18	0.0027
Underfill B	1.55e6	0.0329	0.22	0.0072
Underfill C	1.14e5	0.0112	0.31	0.0035
Mold Compound	2.79e6	0.0043	0.4	0.0017
Solder Mask	4.83e5	0.0143	0.2	0.0029
BT Substrate	2.13e6	0.0075	0.4	0.0030

* Sources: all from in-house testing

Since the moisture properties at PCT (121°C/100%RH) cannot be characterized, the moisture distribution under 85°C/85%RH is calculated for relative comparison of different underfill materials. In the model, a factor of 100/85 is applied to estimate C_{sat} under 100%RH. The actual moisture distribution under PCT for 168hr should be more severe than under JEDEC Level 1. Alternatively, the diffusivity and C_{sat} at PCT may be extrapolated using equations published by Galloway et al. [43].

3.4.2 Hygroswelling Model

Coefficient of moisture expansion (CME) is a measure of change in material strain with moisture concentration. Here, it is the ability of material to expand when subjects to moisture absorption during moisture preconditioning. Due to CME mismatch among various materials, the hygro-mechanical or hygroswelling stress is induced. The concept is analogous to CTE mismatch and thermo-mechanical stress, which we are more familiar with. The hygro-mechanical problem can be solved using the same procedure as a typical thermo-mechanical solution. The moisture loading applied is from 0% to 100% of moisture concentration. The centerline of package is symmetric (no x-displacement), simply supported at the package center (see Figure 3.6).

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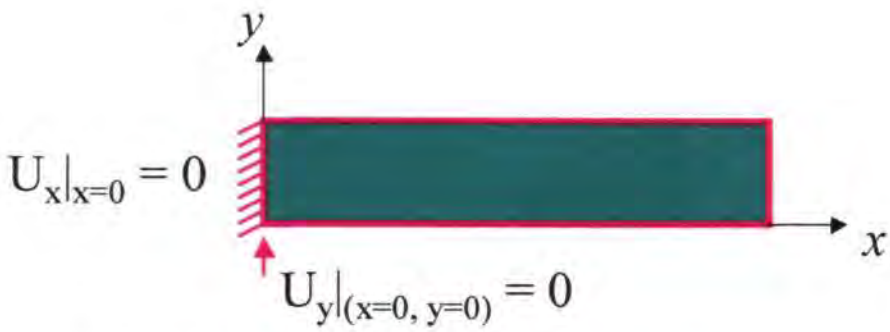

Figure 3.6. Boundary conditions of structural model

The general hygroswelling characterization technique was developed [52-53]. For this study, two identical underfill disc samples are preconditioned with moisture under 85°C/85%RH for about 2 weeks. Then the samples are monitored for desorption under Thermo-gravimetric Analyzer (TGA) and Thermo-mechanical Analyzer (TMA) respectively at the same time at 85°C temperature for about one day. Both TMA and TGA show very close time-dependent curves (see Figure 3.7) because the initial moisture content and desorption condition are also close. The change in linear dimension (sample thickness direction) and weight can be related by CME, obtained from the slope of the graph, strain vs. concentration (see Figure 3.8):

$$\varepsilon_h = \beta_m C \tag{3.4}$$

where ε_h is the linear hygro strain, β_m is the CME, and C is the moisture concentration. The values of CME measured for no-flow underfill and mold compound materials are shown in Table 3.5. Underfill B has the largest hygro strain, due to the relatively large C_{sat} and CME values. Die, copper, and solder bump materials are assumed to have zero CME, i.e. has no hygroswelling. All materials are considered as linear elastic.

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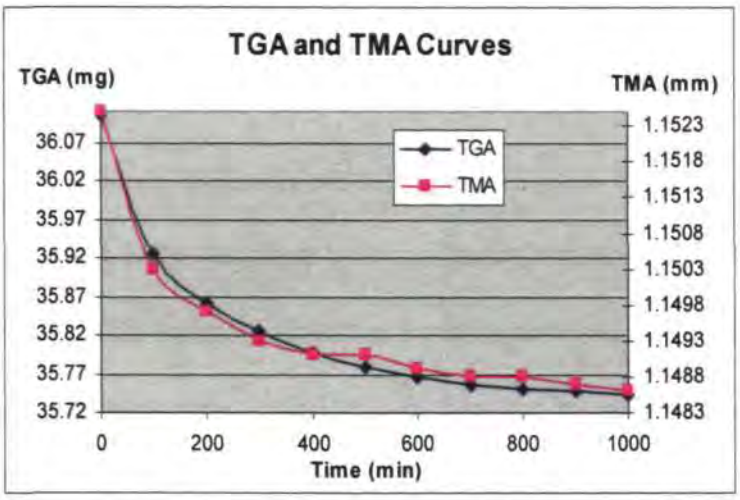

Figure 3.7. TGA and TMA curves for Underfill C

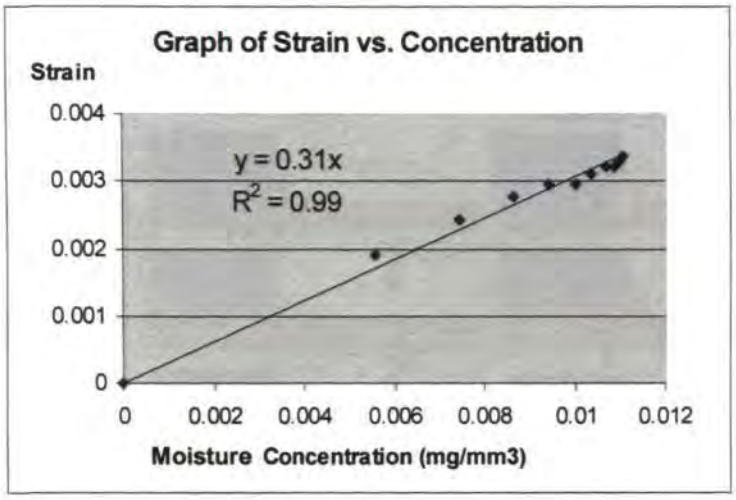

Figure 3.8. Computation of CME for Underfill C

3.4.3 Thermo-mechanical Model

Linear-elastic thermo-mechanical stress model is established. Linear-elastic model is preferred due to faster solution speed and availability of material properties, making it suitable for design analysis. The temperature loading is from curing temperature of underfill or mold compound (if molded) to the reflow temperature of 220°C. Boundary conditions are shown in Figure 3.6. The thermo-mechanical material properties used in the modeling are shown in Table 3.2.

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3.5 DISCUSSION OF RESULTS

3.5.1 Moisture Diffusion

From results of moisture diffusion modeling (see Figure 3.9), it is shown that the unmolded packages are fully saturated with moisture (wetness, w = 1) after 12 hours under 85°C/85%RH. The transient moisture wetness distribution is only dependent on the diffusivity of the materials. Underfill C has the highest diffusivity, therefore saturated the fastest. However, once saturated, the final moisture concentration is only dependent on C_{sat}. Therefore, Underfill B has the highest moisture concentration according to Eq. (3.2). Interface material properties are not considered.

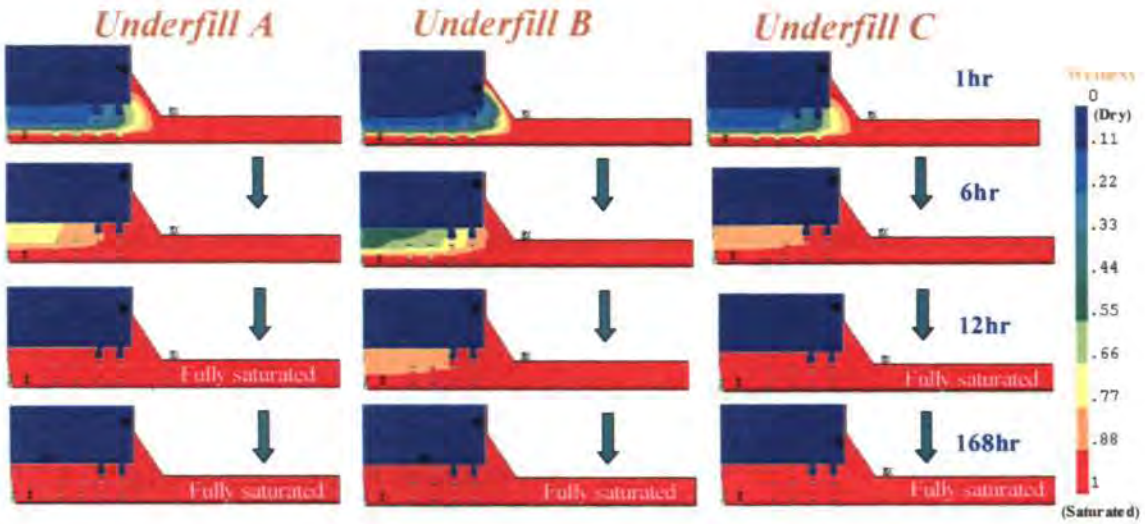

Figure 3.9. Transient moisture distribution for Underfill A-C (unmolded)

Figure 3.10 shows that molded package saturated slower than unmolded package, but both types of packages are fully saturated after 168 hours of moisture preconditioning under 85°C/85%RH. Under the more severe PCT condition (121°C/100%RH), the packaging materials will have even higher diffusivity and C_{sat}. Therefore, both the unmolded and molded packages will be fully saturated at a faster rate during PCT than under 85°C/85%RH.

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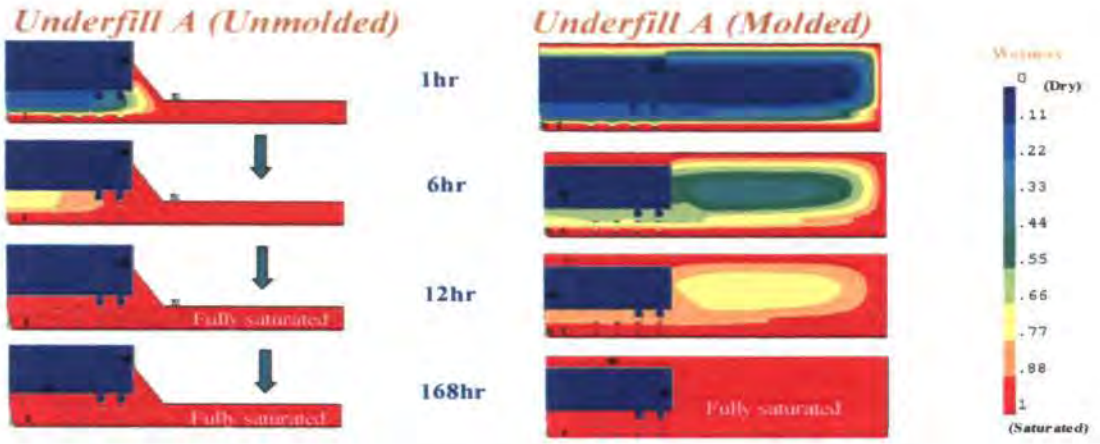

Figure 3.10. Transient moisture distribution of unmolded vs. molded package

In the subsequent hygroswelling modeling, the moisture distribution can be assumed to be uniform, equal to the C_{sat} of the materials. There is no moisture concentration gradient within the material. If the package is not fully saturated, the moisture concentration distribution results have to be input as the final moisture loading in the hygroswelling model, instead of assuming $w = 1$ (fully saturated) throughout the package.

3.5.2 Hygroswelling Stress During PCT

Figure 3.11 shows that during PCT, the normal hygroswelling stress (S_y) acting on UBM and solder bump is mostly tensile (peeling mode), causing the UBM-opening failure. Shear stress of lower magnitude also contributes to the interfacial delamination. The swelling of underfill induces compressive normal stress on the die/underfill interface (see Figure 3.3), but the UBM (die/bump) is under tensile normal stress, because the solder bump doesn't absorb, nor swell with moisture.

From the parametric studies, unmolded FCBGA with Underfill-A has the lowest hygroswelling stress. Previous reliability test results (Table 3.4) also show that

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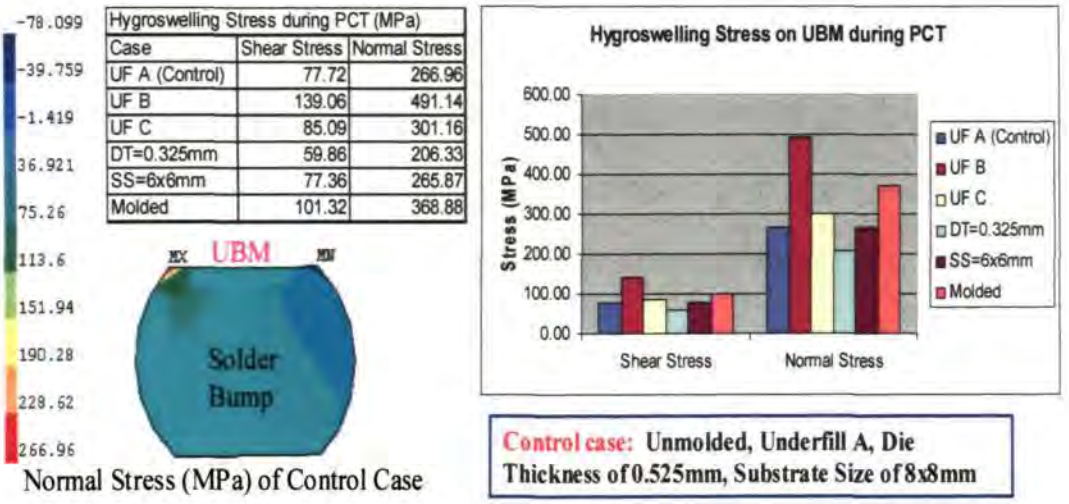
unmolded FCBGA with Underfill-A has the best performance. Underfill-A has the least hygroswelling strain (see Table 3.5), due to relatively low C_{sat} and CME. Interfacial adhesion strength of underfill under high temperature and high moisture condition, is also an important consideration. For better UBM reliability during PCT, material suppliers may need to compromise in the formulation of no-flow underfill materials, to achieve low values of both C_{sat} and CME.

Unmolded FCBGA with smaller die thickness of 0.325mm has 23% lower stress than FCBGA with die thickness of 0.525mm, but substrate size has little effect on UBM stress. Molded package has 38% larger stress than unmolded package (for Underfill A), due to additional CME mismatch with mold compound material. This correlates well with reliability test results that unmolded package generally performs better than molded package during PCT.

Since the test vehicles experience several tests (moisture preconditioning at Level 3, followed by reflow and 168 hours of PCT), the actual failure mechanism is more complex, and could be a mixed mode. The moisture-induced failures could be contributed by combined effects of process defects, interfacial adhesion strength, moisture, vapor pressure, thermal stress, and hygroswelling stress.



Hygroswelling Stress during PCT (MPa)		
Case	Shear Stress	Normal Stress
UF A (Control)	77.72	266.96
UF B	139.06	491.14
UF C	85.09	301.16
DT=0.325mm	59.86	206.33
SS=6x6mm	77.36	265.87
Molded	101.32	368.88

Figure 3.11. Design analysis on hygroswelling stress induced during PCT

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3.5.3 Combined Hygroswelling Stress and Thermo-mechanical Stress During PCT

At PCT condition of 121°C/100%RH, there is a combination of both hygroswelling stress and thermal stress. During temperature cooling, from underfill curing temperature to 121°C of PCT, the thermal stress induced on UBM and solder bump is compressive, acting against the tensile hygroswelling stress (see previous results in Section 3.5.2). For the unmolded package with Underfill-A, the compressive stress is 262MPa, close to the tensile hygroswelling stress of 267MPa. Compressive thermal stress during PCT is also observed by Wong et al. [53]. Vanlandingham et al. [119] and Zheng et al. [120] show that T_g of material can reduce up to 20°C below its dry state value, when the sample is subjected to humid environment. Therefore, at 121°C, all underfill materials studied here may be above T_g. Under high CTE_2, the thermal stress induced is even more compressive, 278MPa, greater than the hygroswelling stress. Underfill with high CTE helps to generate compressive stress, against the tensile hygroswelling stress.

In order for failure to occur during PCT, the hygroswelling stress must be much greater than the thermal stress. Previous hygroswelling stress modeling was performed based on CME at 85°C. Wong et al. [53] show that CME is a strong function of temperature. At 121°C, the CMEs of materials can be about 2 times higher than values measured at 85°C. When CME is doubled, the hygroswelling stress is also doubled accordingly. For the case with Underfill-A, the magnitude of hygroswelling stress can be as high as 534MPa, much larger than the thermal stress of 278MPa. Therefore, the hygroswelling stress is the dominant stress. For relative comparison among design variations, the previous results based on assumption of CME at 85°C are still valid.

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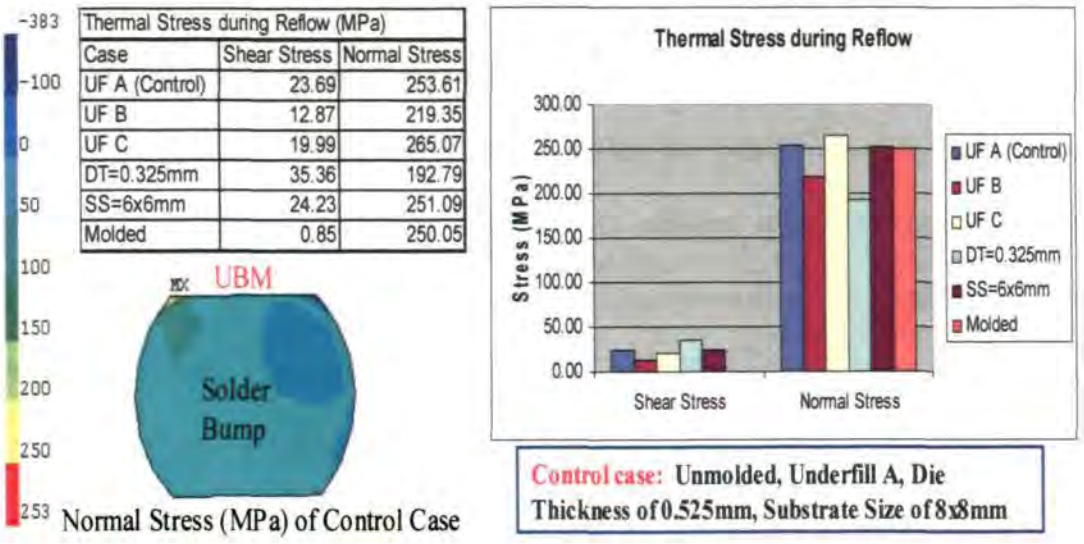
3.5.4 Thermo-mechanical Stress During Reflow

Figure 3.12 shows that during reflow, the normal thermal stress (S_y) acting on UBM and solder bump is also mostly tensile, and therefore has a negative effect on UBM reliability. The magnitude of normal and shear thermal stresses induced during reflow are much lower than the hygroswelling stresses during PCT. More failures are observed during PCT than during reflow. The UBM and underfill/die adhesion strength may be affected during reflow, but the package still manage to pass the electrical test (solder bump resistance measurement). The subsequent hygroswelling stress during PCT is the main factor causing the underfill/die interfacial delamination and UBM opening failure. The effect of vapor pressure is not considered in this model. Details of vapor pressure modeling will be introduced and discussed in later Section 4.2.5.

Parametric studies show that the thermal stresses are close for these three types of underfill materials, because there is no large variation in the underfill thermo-mechanical material properties. Unmolded FCBGA with smaller die thickness of 0.325mm has 24% lower stress than FCBGA with die thickness of 0.525mm. Substrate size and molded package have little effect on thermal stress of UBM during reflow.



Thermal Stress during Reflow (MPa)		
Case	Shear Stress	Normal Stress
UF A (Control)	23.69	253.61
UF B	12.87	219.35
UF C	19.99	265.07
DT=0.325mm	35.36	192.79
SS=6x6mm	24.23	251.09
Molded	0.85	250.05

Figure 3.12. Design analysis on thermal stress induced during reflow

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3.6 SUMMARY

The package reliability of FCBGA packages with no-flow underfill materials is evaluated. Comprehensive moisture diffusion, hygroswelling, and thermo-mechanical models are established to study FCBGA-8x8 with no-flow underfill under moisture preconditioning, reflow, and PCT. The actual failure mechanism is complex, contributed by combined effects of process defects, interfacial adhesion strength, moisture, vapor pressure, thermal stress, and hygroswelling stress. From modeling, the UBM stress calculations correlate well with the reliability test results. Moisture-hygro-thermo-mechanical modeling can be an useful tool to analyze and enhance the reliability of FCBGA against moisture-induced failures.

Moisture diffusion modeling shows that both unmolded and molded packages are fully saturated during PCT. High moisture concentration weakens the critical interfacial adhesion, generates vapor pressure during reflow, and induces tensile hygroswelling stress on UBM during PCT. Hygroswelling stress induced during PCT is found to be greater than thermal stress generated during reflow. The UBM-opening and die/underfill delamination failures occur mostly during PCT. Although the packages did not fail during reflow, the reliability could have been affected.

Parametric studies from modeling show that underfill with lower C_{sat} and CME has lower hygroswelling stress on UBM and therefore has better reliability performance. FCBGA with smaller die thickness also helps to enhance the UBM reliability during reflow and PCT. However, the substrate size has little effect. In general, a molded package has larger hygroswelling stress on UBM during PCT than an unmolded package.

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CHAPTER 4 INTEGRATED PACKAGE STRESS MODELING

4.1 INTRODUCTION

QFN packages are getting popular as a low-cost solution for applications with low pin-count requirements. QFN is also known as MLF (Micro LeadFrame), MLP (Micro Lead Package), QON (Quad Outline Non-lead), or SON (Small Outline Non-lead) package. It is a type of CSP and can be assembled and molded in matrix form for cost-saving. A schematic of QFN-8x8mm (52 leads) package used in this study is shown in Figure 4.1. The peripheral leads are exposed at the package bottom for soldering to the board. Extra soldering under the center die pad and at diagonal corners is optional. Currently, there are not many publications available on reliability modeling of QFN packages. Moisture induced failures during moisture preconditioning and reflow are main concerns for QFN packages.

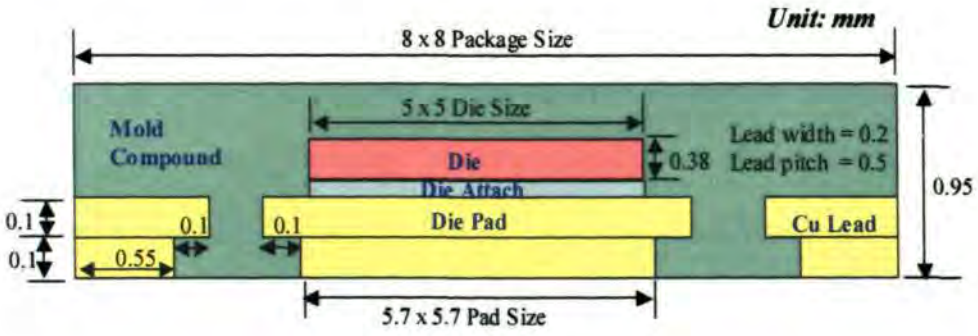

Figure 4.1. Schematic of QFN 8x8mm (52L) package

The moisture-induced failures, e.g., popcorn and delamination, of IC packages are common phenomena during solder reflow. Usually the package is first preconditioned at certain temperatures to absorb moisture. Then failures occur partly due to sudden vaporization of moisture in the package at high temperature condition. Therefore, it is

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critical to evaluate the strength of internal vapor pressure generated in the package during reflow. The popcorn failure was first postulated by Fukuzawa et al. [38] in 1985, and later supported by many publications [43-45].

4.2 TYPES OF MODELING

The integrated stress modeling during reflow requires five types of modeling, i.e. moisture diffusion during moisture preconditioning and reflow, thermal modeling, hygro-mechanical modeling, thermo-mechanical modeling, and vapor pressure modeling. 2D half-model is established for QFN. For all types of models, the same finite element geometry model is used, but different element types, boundary conditions, loadings, and solutions are applied. The theories and procedures for each type of modeling are briefly explained in the following sections.

4.2.1 Moisture Diffusion Modeling

The theory of moisture diffusion modeling applied was previously explained in Section 3.4.1. Initial and boundary conditions applied are shown in Figure 3.5. The moisture properties, i.e. diffusivity and C_{sat}, characterized under 85°C/85%RH, are listed in Table 4.1. The moisture properties can be obtained by curve-fitting the moisture weight gain data of a thin disc specimen with the analytical solution of 1D moisture diffusion. Die and copper leadframe are assumed to be impermeable to moisture, i.e. do not absorb moisture, and therefore they have zero diffusivity and C_{sat}.

The moisture weight gain curve of mold compound under 85°C/85%RH is shown in Figure 4.2. This is a typical curve with a high moisture absorption rate at the beginning (first few days), and then reaching steady state or saturation at longer time. It was found that the weight gain curve-fitted by Fick's Law solution (Eq. (2.2)) overestimates

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the moisture absorption rate at longer time. The non-Fickian behavior of test sample could be that moisture diffusion close to saturation stage is dominant by a slow rate of water condensation from vapor to liquid phase. The C_{sat} of material is much higher than the moisture density in the humidity chamber. Therefore, some of the vapor-phase water must be condensed into liquid water, to make more room for moisture diffusion at vapor phase from ambient into the microvoids in the material. At the beginning of weight gain test, moisture density in the microvoid is low, therefore there is no condensation, and the curve can be fitted well with Fick's Law. At longer time, the slower condensation process is dominant. Therefore, the moisture diffusivity at vapor phase is reduced at higher moisture concentration, or the so-called non-Fickian behavior. The effect of this condensation process shall be studied in detail in future.

Table 4.1. Moisture and hygroswelling material properties

Material	D (mm^2/s)	C_{sat} (mg/mm^3)	β, CME (mm^3/mg)	Hygro Strain (β x C_{sat})
Mold Compound	7.43e-7	7.06e-3	0.222	1.57e-3
Die Attach	1.25e-5	6.20e-3	0.520	3.22e-3

* Sources: all from in-house testing

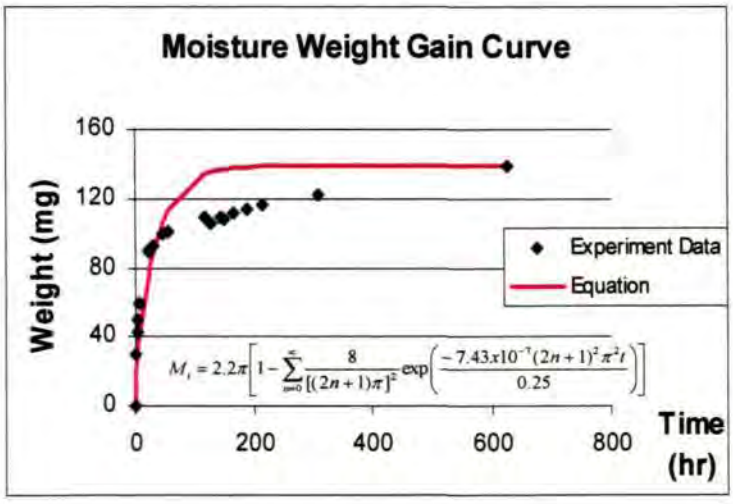

Figure 4.2. Moisture weight gain curve for mold compound

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Moisture desorption diffusivity is also an important material property, especially during reflow, to determine the moisture weight loss. Moisture diffusivity during desorption at reflow is larger than absorption at preconditioning temperature. Figure 4.3 shows the effect of temperature (30°C to 220°C) on moisture diffusivity during desorption for mold compound, D (MC), and die attach, D (DA). The diffusivity is larger at higher temperature, and the relationship can be described by the following equation:

$$D = D_o e^{\frac{Q}{RT}} \tag{4.1}$$

where D_o is the diffusion coefficient, Q is the activation energy (ev), R is the Boltzmann constant (8.83e-5 ev/K), and T is the absolute temperature (K). The D_o and Q of mold compound and die attach materials during desorption are listed in Table 4.2.

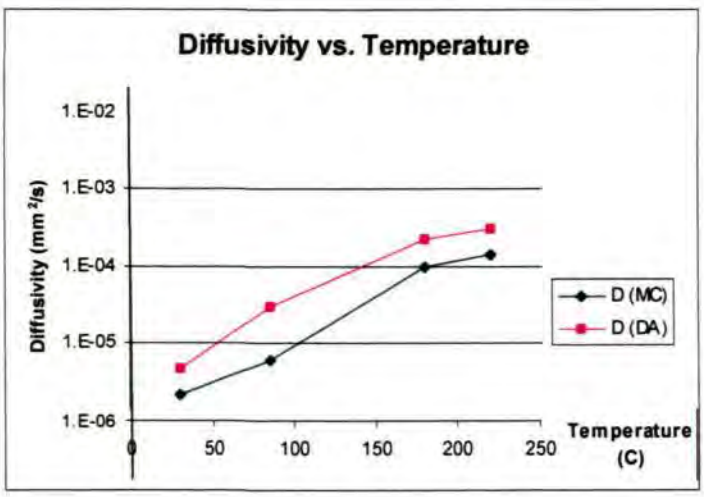

Figure 4.3. Diffusivity as a function of temperature

Table 4.2. Diffusivity constants of moisture desorption

Material	D_o (mm²/s)	Q (ev)
Mold Compound	0.18	-0.304
Die Attach	0.35	-0.293

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4.2.2 Thermal Modeling

Similar to mass diffusion, the following transient heat conduction equation can be solved to obtain the temperature distribution in the IC package during reflow.

$$\frac{\partial T}{\partial t} = \alpha_T \left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} \right) \tag{4.2}$$

where T is the temperature, x, y, z are the spatial coordinates, and α_T is the thermal diffusivity. The effect of phase change is not considered in this model. The thermal material properties, specific heat (C_p), thermal conductivity (k), and density (ρ) are listed in Table 4.3. They are related to thermal diffusivity (α_T) by:

$$\alpha_T = \frac{k}{\rho \cdot C_p} \tag{4.3}$$

Table 4.3. Thermal material properties

Material	C_p (J/kg.K)	k (W/m.K)	ρ (kg/m^3)
Copper	385	390	8950
Die	712	108	2330
Mold Compound	900	0.67	2088
Die Attach	800	1.2	2400

* Sources: all from material suppliers

The initial condition is interior of package set at room temperature (see Figure 4.4). The boundary condition used is fixed external surface temperature, according to the reflow temperature profile measured, within the specification of JEDEC test standard (e.g. maximum temperature of 220°C, +5/-0°C). The effects of convection coefficient (h) and ambient temperature in the multi-zone oven are considered indirectly by measuring the surface temperature of the package. The centerline of package is symmetric (heat flux = 0).

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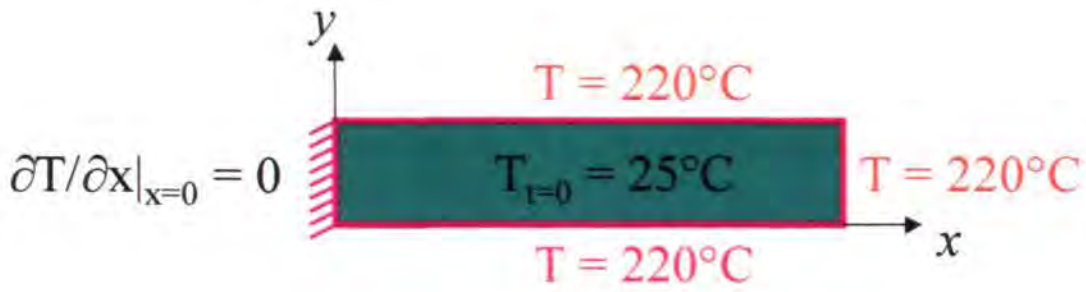

Figure 4.4. Initial and boundary conditions of heat transfer model

4.2.3 Hygro-mechanical Modeling

The theory of hygro-mechanical modeling and material characterization procedure of CME were explained in Section 3.4.2. For mold compound samples tested, both TMA and TGA show very close time-dependent curves (see Figure 4.5) because the initial moisture content and desorption condition are also close. According to Eq. (3.5), CME can be computed from the slope of the graph (see Figure 4.6), strain vs. concentration. The values of CME measured for mold compound and die attach are shown in Table 4.1. Die and copper leadframe materials are assumed to have zero CME, i.e. no hygroswelling. All materials are considered as linear elastic.

For this case, the hygro strain is as high as the thermal strain. For example, the mold compound hygro strain is equivalent to thermal strain with mold compound CTE of 34.9ppm/°C under the same temperature loading of 175-220°C using the analogous Eqs. (3.5) and (4.4):

$$\varepsilon_T = \alpha \Delta T \tag{4.4}$$

where ε_T is the thermal strain, α is the CTE, and ΔT is the temperature loading. The boundary conditions applied are similar to previous hygro-mechanical model (see Figure 3.6).

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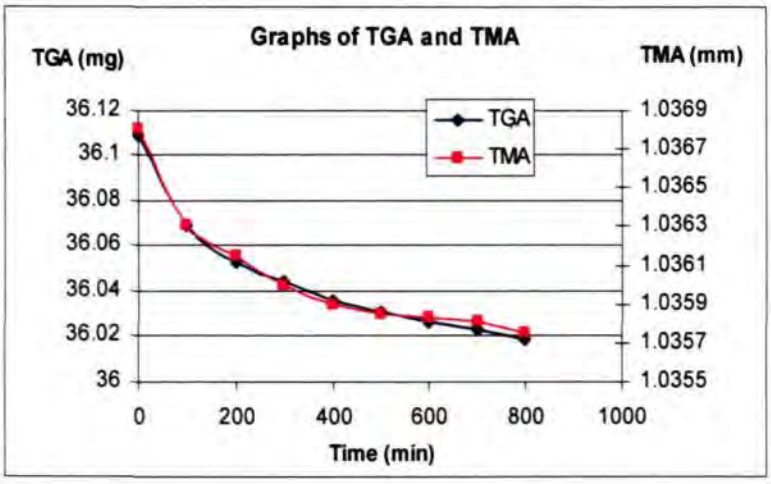

Figure 4.5. Hygroswelling material characterization

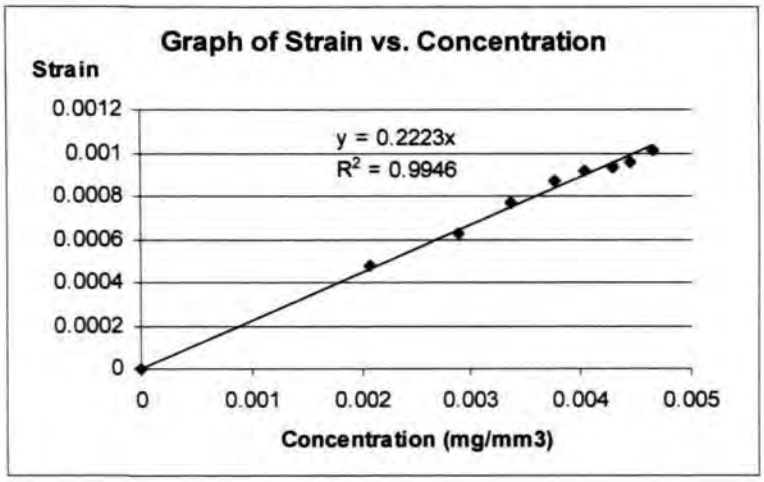

Figure 4.6. Computation of mold compound CME

4.2.4 Thermo-mechanical Modeling

Linear-elastic thermo-mechanical stress model is applied. The temperature loading applied is from the post mold cure temperature of mold compound, 175°C, to the reflow temperature of 220°C. The thermo-mechanical material properties used in the modeling are shown in Table 4.4. The boundary conditions applied are similar to previous thermo-mechanical model (see Figure 3.6).

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Table 4.4. Thermo-mechanical material properties

Material	Modulus at 220°C (GPa)	Mean CTE (ppm/°C)
Copper *	127.4	17.4
Die *	131	2.8
Mold Compound #	1.1	34
Die Attach #	0.043	170

Sources: * material suppliers, # in-house testing. MC and DA: storage modulus used.

4.2.5 Vapor Pressure Modeling

Representative Volume Element (RVE) approach is applied to estimate the vapor pressure generated inside the material. Consider a very small representative material sample, termed RVE. From the microscopic level, the RVE is large enough to be statistically representative of the material properties at this location. Therefore, a field quantity, the void volume fraction, f, can be defined as

$$f = \frac{dV_f}{dV}, \quad 1 \geq f \geq 0 \tag{4.5}$$

where dV_f is the void volume and dV is the element volume. When $f = 1$ (fully voided), it implies that the delamination occurs at this location. The void volume fraction is a field variable, and has different evolution at different locations. It evolves faster along the interface than inside the material if the interfacial adhesion is weak. However, the initial micro-voids are distributed randomly but uniformly in the material, and thus the initial void volume fraction, f_0, is a material property.

A useful quantity, the moisture density in the voids, can be described as

$$\rho_m = \frac{dW_m}{dV_f} = \frac{dW_m / dV}{dV_f / dV} = \frac{C}{f_0} \tag{4.6}$$

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where dW_m is the moisture weight in a RVE. In addition, the transition temperature, T_l, can be defined as the temperature at which the moisture in the voids is fully transformed to vapor phase,

$$\rho_m(x_i, T_0) = \rho_g(T_l) \tag{4.7}$$

where $\rho_g\ (T_l)$ is the saturated vapor density at temperature T_l, and T_0 is the preconditioning temperature at which the moisture is absorbed.

There are three distinct cases at which vapor pressure can be computed [62-63]. It is assumed that the water vapor follows the ideal gas law for Cases 1 and 2. The vapor pressure can be calculated based on the local moisture concentration after preconditioning which determines the transition temperature, T_l.

The first case is when the moisture density in the voids is low enough such that all the moisture becomes vaporized at preconditioning temperature, T_0:

$$p = \frac{C\, p_g(T_0) T}{f\, \rho_g(T_0) T_0} \quad \text{when} \quad T_0 \geq T_l \tag{4.8}$$

where p is the pressure and p_g is the saturated vapor pressure.

In the second case, the moisture is fully vaporized at a temperature between preconditioning temperature, T_0, and the peak reflow temperature, T:

$$p = \frac{p_g(T_l) T}{T_l} \quad \text{when} \quad T \geq T_l \geq T_0 \tag{4.9}$$

For the last case, the moisture is not fully vaporized even at reflow temperature, T:

$$p = p_g(T) \quad \text{when} \quad T_l \geq T \tag{4.10}$$

This case uses thermodynamics table, instead of ideal gas assumption, for saturated pressure calculation at particular temperature.

The initial void volume fraction, f_0, may be estimated from the material temperature-dependent moisture property. According to Eq. (4.6), when saturated, the local

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concentration, C, is the same as C_{sat}. Therefore, the initial void volume fraction can be expressed as following

$$f_0 = \frac{C_{\text{sat}}}{\rho_m} \tag{4.11}$$

Since $\rho_m \approx 1.0\text{g/cm}^3$, we have

$$f_0 \approx C_{\text{sat}}\big|_{100°C\,/\,100\%RH} \tag{4.12}$$

where 100°C/100%RH is selected as the near-saturated condition, and unit of C_{sat} is in g/cm^3 or mg/mm^3. Alternatively, we may measure the C_{sat} of test sample in boiling water to accelerate the moisture absorption. Eq. (4.12) provides a simple way to measure the approximate magnitude of the voids existing in materials. The estimation is at the lower-limit since the moisture usually exists as a mixture of water and vapor at 100°C/100%RH. Table 4.5 lists the results of the initial void volume fraction (f_o) for mold compound and die attach used. The accuracy of f_o is actually not critical in this particular study because of its low sensitivity on vapor pressure results, and it will be discussed in the later section.

Table 4.5. Initial void volume fraction

Material	f_o
Mold Compound	0.83%
Die Attach	0.76%

The linear vapor pressure induced strain (ε_p) may be estimated by

$$\in_p = \frac{1-2\nu}{E} p \tag{4.13}$$

where ν is the Poisson's ratio, E is the modulus, and p is the average vapor pressure. The modulus of mold compound drops a few orders at the reflow temperature, and thus

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the vapor pressure strain may become as important as thermal or hygro strain. For example, for mold compound with saturated vapor pressure of 2.32MPa, the strain induced is equivalent to thermal strain (see Eq. (4.4)) with CTE of 18ppm/°C under the same 175-220°C temperature loading. The magnitude of this vapor pressure induced strain is in the same order as hygro and thermal strains. The vapor pressure strain induces additional mismatch to the package, in addition to the CTE (thermo-mechanical strain) and CME (hygro-mechanical) mismatch. It must also be pointed out that such an expansion is directly related to the vapor pressure distribution, rather than the moisture distribution.

4.2.6 Integrated Stress Modeling

Figure 4.7 shows the methodology of integrated stress modeling to calculate the package stress induced during reflow. The five models mentioned earlier are related to one another. Result of moisture distribution from the moisture diffusion model is used as input for both the vapor pressure model and the hygro-mechanical model. On the other hand, the temperature distribution from the thermal model is applied in both vapor pressure model and thermo-mechanical model.

The stress and strain induced by vapor pressure, thermo-mechanical, and hygro-mechanical models are combined into an equivalent linear elastic stress model to compute the package stress and strain induced during reflow. The hygro strain and vapor pressure induced strain are converted to an equivalent thermal strain, defined by CTE under the same temperature loading (175-220°C).

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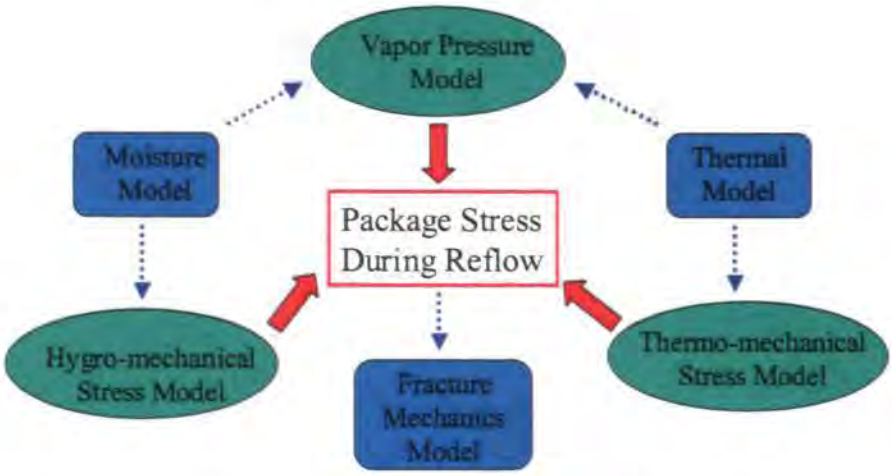

Figure 4.7. Integrated package stress model during reflow

4.2.7 Interfacial Fracture Mechanics Modeling

Subsequently, the integrated package stress is analyzed with linear interfacial fracture mechanics. There are several possible ways used by researchers for fracture mechanics analyses [67], e.g., J-integral method, Virtual Crack Closure (VCC) method, and Crack Flank Displacement Extrapolation Method (CFDEM), depending on the type of application. Here, VCC method with non-singular crack-tip element (see Figure 4.8) can be applied conveniently in modeling using ANSYS software to calculate the strain energy release rate, G, of a crack, assumed along the die/mold compound and die/die attach corner interfaces, which are the potential delamination layers. Crack-tip elements used are PLANE82, or 6-nodes 2D triangular elements. Raju [121] developed a convenient approach to compute G and the mode mixity, ψ, based on the crack opening displacements and the nodal forces. The work required to extend the crack by Δa is equivalent to the work needed to close the crack tip by Δa. The mode I (G_I) and mode II (G_{II}) components of G and mode mixity are described by

$$G_I = \frac{1}{2\Delta a}(F_{y1}\Delta v_j + F_{y2}\Delta v_i) \tag{4.14}$$

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$$G_{II} = \frac{1}{2\Delta a}(F_{x1}\Delta u_j + F_{x2}\Delta u_i) \tag{4.15}$$

$$G = G_I + G_{II} \tag{4.16}$$

$$\psi = \tan^{-1}\sqrt{\frac{G_{II}}{G_I}} \tag{4.17}$$

where Δa is the crack extension, F_{x1}, F_{x2}, F_{y1}, and F_{y2} are the x and y components of nodal forces per unit thickness at nodes 1 and 2, Δu_i, Δu_j, Δv_i, and Δv_j are the x and y displacements at nodes i and j (see Figure 4.8). From Eq. (4.17) it is clear that when mode I is dominant, $G_I > G_{II}$, mode mixity is less than 45° (vice versa for mode II).

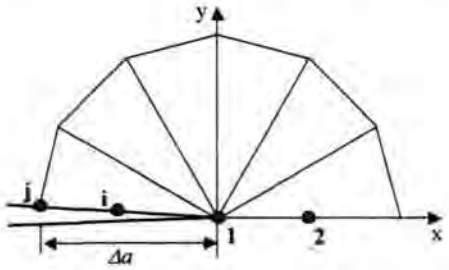

Figure 4.8. Non-singular crack-tip elements

4.3. DISCUSSION OF RESULTS

4.3.1 Moisture Diffusion Modeling

The transient moisture wetness distribution in QFN (symmetric half model) is shown in Figure 4.9, ranging from 0 to 100% saturation. The moisture diffuses into the package through mold compound, and gradually spreads into die attach layer. At the end of 168 hours of moisture preconditioning under 85°C/85%RH, the package is almost fully saturated with moisture. During the 5-minute solder reflow, external package surface loses a significant amount of moisture due to high moisture desorption rate. The moisture diffusivity is a few orders higher at reflow temperature than moisture preconditioning temperature. However, the moisture concentration in the

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interior of the package, including critical die attach and die/mold compound interfaces, still remains relatively unchanged. The local moisture concentration in these critical interfaces determines the strength of interfacial adhesion and magnitude of internal vapor pressure induced, which partially lead to moisture induced failures, e.g., delamination and popcorning, in the package.

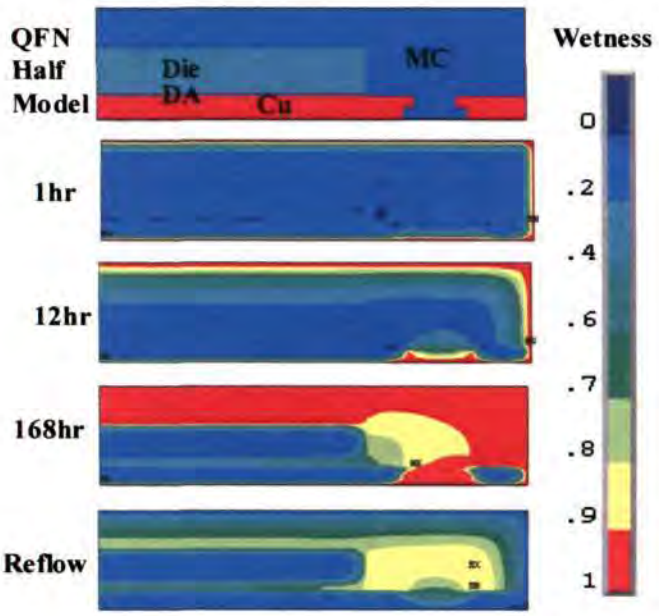

Figure 4.9. Transient moisture wetness distribution

4.3.2 Thermal Modeling

The solution of thermal model is analogous to moisture diffusion. However, the thermal diffusivity is much larger than the moisture diffusivity. Figure 4.10 shows the temperature distribution in the package during 5-minute reflow (from 25°C to peak temperature of 220°C). Heat is conducted faster in die and copper leadframe than in mold compound. When the external surface is heated to 220°C after 5 minutes, the internal package reaches this uniform temperature within a few seconds. Therefore, in the subsequent thermo-mechanical and vapor pressure models, temperature distribution during reflow (5 minutes) can be assumed to be uniform throughout the package.

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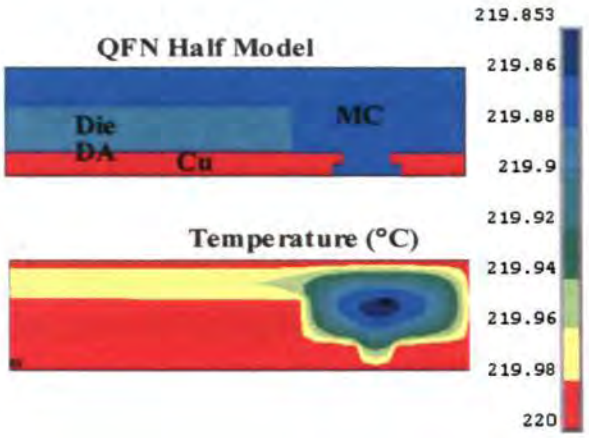

Figure 4.10. Package temperature distribution during reflow

4.3.3 Vapor Pressure Modeling

From the transient moisture distribution (see Figure 4.9), the corresponding vapor pressure distribution at reflow temperature of different moisture preconditioning time can be calculated (see Figure 4.11) based on Eqs. (4.8)-(4.10). Case 3 of saturated pressure is mostly encountered here.

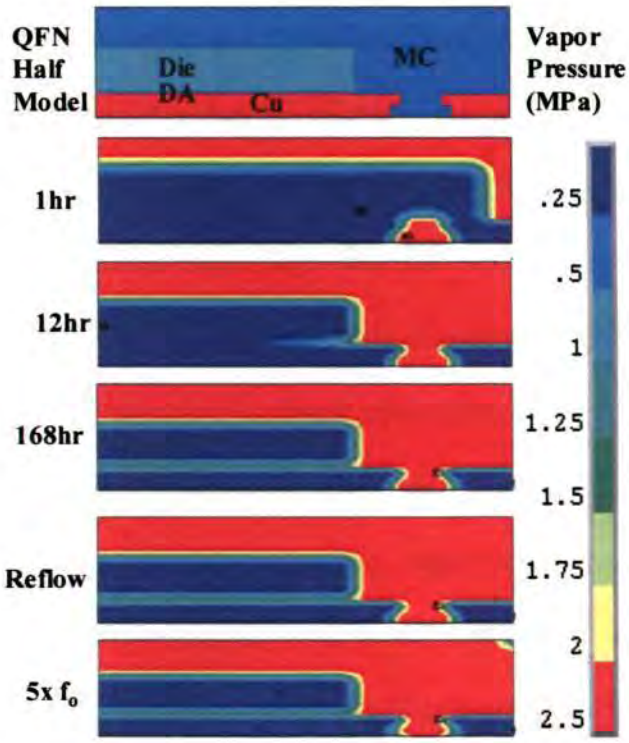

Figure 4.11. Vapor pressure distribution at reflow temperature

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It is interesting to note that moisture diffusion and vapor pressure models have very different rates of saturation. For moisture diffusion, the distribution gradually reaches near-saturation at 168 hours of moisture preconditioning. However, for vapor pressure, the distribution reaches saturated pressure at reflow temperature with only 12 hours of moisture preconditioning under 85°C/85%RH. This implies that at JEDEC Level 1, the void moisture density exceeds its critical density value after about 12 hours. Subsequent addition of moisture density has no effect on the saturated pressure. Therefore, the vapor pressure induced strain is related directly to vapor pressure distribution, rather than to moisture distribution.

At 1 hour of moisture preconditioning (see Figure 4.11), the void moisture density is below the critical value. Therefore, the vapor pressure has closer distribution pattern as moisture diffusion, with lower vapor pressure inside the package, and gradually larger towards the external package surface. This corresponds to Cases 1 and 2 (Eqs. (4.8)-(4.9)), which assume ideal gas behavior for non-saturated pressure conditions. Comparison is made with vapor pressure obtained from thermodynamics table, and the ideal gas assumption only has less than 5% of error. Anyway, for JEDEC Level 1 with 168 hours of moisture preconditioning, saturated pressure (Case 3, Eq. (4.10)) is always encountered, and its magnitude is much larger than the vapor pressure in Cases 1 and 2.

The effect of initial void volume fraction (f_o) is also studied. When f_o is increased 5 times, the vapor pressure distribution is almost unchanged (see Figure 11), because the void moisture density is still above the critical value. It is important to point out that although f_o (until 5 times) has little effect on vapor pressure, it may weaken the interfacial adhesion. Exact measurement of f_o is not critical for Level 1, but it can be important for low moisture conditions, e.g., Level 3 or below, due to low void moisture density.

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4.3.4 Integrated Stress Modeling

The total strains induced by thermo-mechanical, hygro-mechanical, and vapor pressure loadings in mold compound and die attach are listed in Table 4.6. For hygro-mechanical and vapor pressure induced strains, they are converted into equivalent mean CTEs, under the same 175-220°C temperature loading, so that all three models can be integrated in a thermo-mechanical model with equivalent strains. For example, hygro-mechanical strain of mold compound is 1.57e-3 (see Table 1, according to Eq. (3.4)), and the equivalent mean CTE is computed as 1.57e-3/(220°C-175°C) = 34.9ppm/°C. The total equivalent CTE is much larger than only considering equivalent CTE of individual model. Therefore, the thermal stress and strain due to mismatch of these three models are much higher than values of individual model.

Table 4.6. Total strains and equivalent CTEs in integrated stress model

	Mold Compound		**Die Attach**	
	Total Strain	**Equivalent mean CTE (ppm/°C)**	**Total Strain**	**Equivalent mean CTE (ppm/°C)**
Thermo-mechanical	1.53e-3	34	7.65e-3	170
Hygro-mechanical	1.57e-3	34.9	3.22e-3	71.6
Vapor Pressure	8.14e-4	18.1	2.16e-2	479.6
Integrated (total)	3.91e-3	87	3.25e-2	721.2

The relative package warpage or vertical displacement distributions during reflow among various models (not the same scale) are shown in Figure 4.12. Thermo-mechanical model has upward warpage, opposite in direction as compared to hygro-mechanical and vapor pressure induced stress models. This is because for hygro-mechanical and vapor pressure induced stress models, the die and copper leadframe do

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not absorb moisture, and therefore have zero CME and vapor pressure. For thermo-mechanical model, all the materials have different non-zero CTEs. As for the integrated model, the warpage distribution is more complex, a mixture of all three models. The integrated model is very different from the individual models.

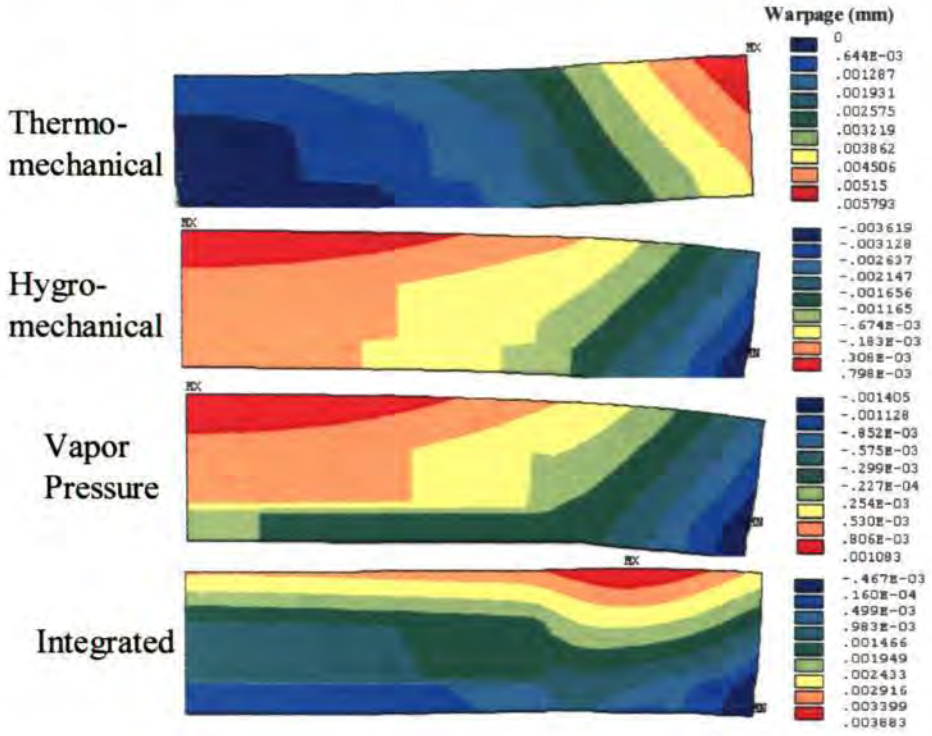

Figure 4.12. Comparison of warpage distributions

The Von Mises stress distribution in mold compound for the integrated model is shown in Figure 4.13. The maximum stress is located at the junction of die, die attach, and mold compound. This location is the same for all other models, despite they have different warpage distribution. However, the magnitude of the maximum stress is different (see Figure 4.14). For Von Mises stress, the principle of superposition is not applicable here, because it is an equivalent stress, linearity is no longer valid. For other stress components, the stress computed by integrated stress model equals exactly to the sum of stresses given by three basic stress models mentioned above. Among the three models, thermo-mechanical stress is the highest. The integrated stress model has about

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50% larger maximum stress in mold compound than the thermo-mechanical stress model. Without considering the hygro-mechanical and vapor pressure induced stresses, the package stress during reflow would have been underestimated.

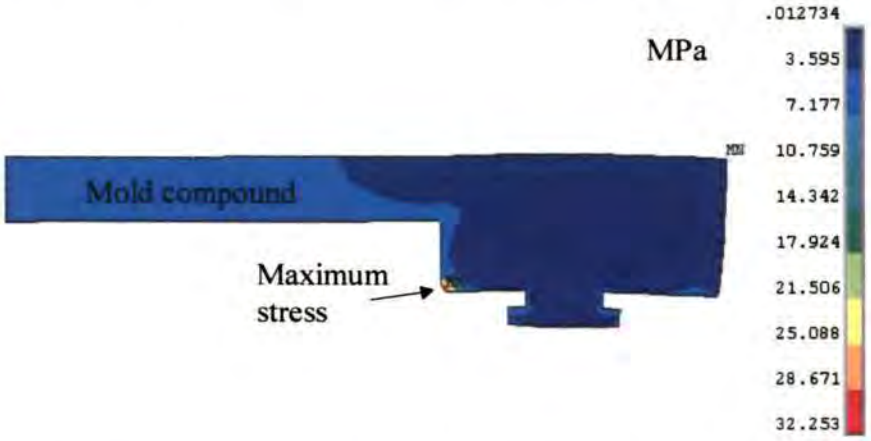

Figure 4.13. Integrated model: Von Mises stress distribution

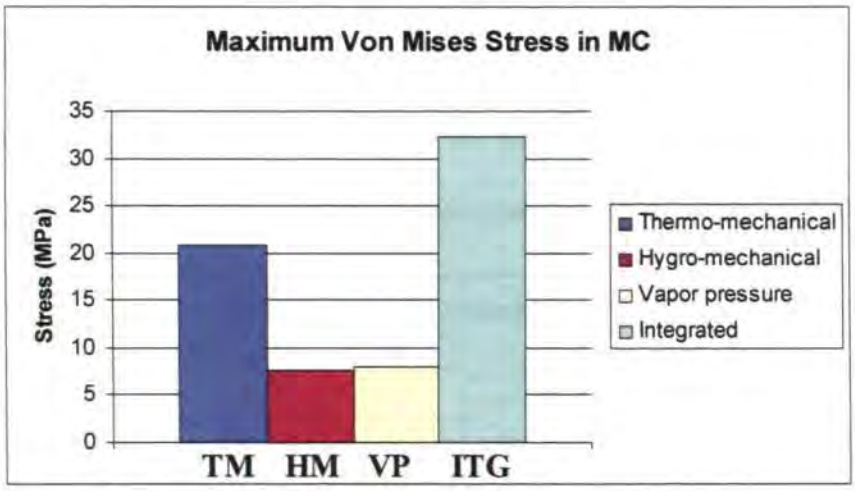

Figure 4.14. Comparison of maximum Von Mises stresses

Besides the difference in stresses, the considerations of moisture diffusion and vapor pressure also have impact on interfacial adhesion strength. The interfacial adhesion should be characterized under reflow temperature with the same level of moisture preconditioning.

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4.3.5 Interfacial Fracture Mechanics Modeling

Two potential failure interfaces, i.e. die/mold compound and die/die attach, are further analyzed for delamination. An initial crack of 0.1mm is assumed at the die corner (both top and bottom interfaces), which is induced by the integrated stress under the thermo-mechanical, hygro-mechanical, and vapor pressure loadings. Once the delamination is initiated, the vapor pressure fills up the cavity quickly and saturated vapor pressure of 2.32 MPa is generated to open-up and extend the crack length. The initial delamination will propagate when G is larger than G_c, critical interfacial toughness of the bi-material. G_c depends strongly on mode mixity, and generally G_c increases with larger mode mixity. It is the strongest under the pure mode II (mode mixity = 90°). The values of G_c have to be determined experimentally.

Figure 4.15 shows that G (calculated by Eqs. (4.14)-(4.16)) increases with crack length at both interfaces studied. The effect of crack length is very significant for die/mold compound interface. If this interface has an initial crack, the crack may be extended by the vapor pressure until the whole interface is fully delaminated.

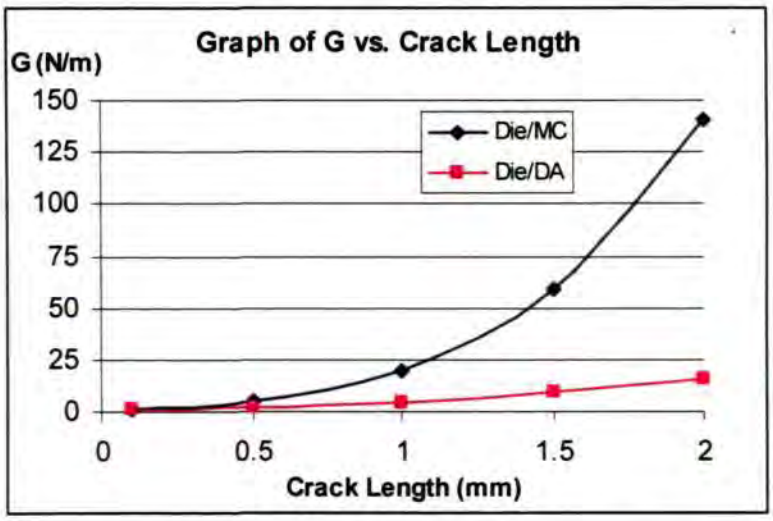

Figure 4.15. Effect of crack length on strain energy release rate (G)

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Figure 4.16 shows that the mode mixity (calculated by Eq. (4.17)) decreases with longer crack length, gradually changed from in-plane shear mode (mode II) to opening mode (mode I). This is because the contribution of vapor pressure loading becomes greater with longer crack length, and naturally it acts to open-up the interfacial gap. For die/mold compound interface, mode mixity becomes stable when crack length exceeds 1mm. However, for die/die attach interface, mode mixity continues to decrease with crack length. Therefore, the interfacial fracture toughness is also reduced, and the crack is more susceptible to further delamination.

It should be noted that the interfacial fracture mechanics theories are very complex and modeling is very challenging. The modeling calculations are made with highly oscillating stress field.

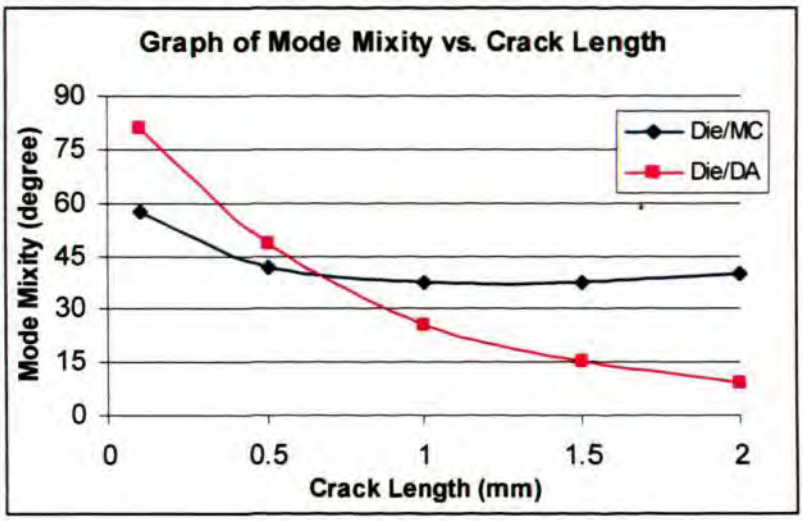

Figure 4.16. Effect of crack length on mode mixity

4.4 SUMMARY

The actual package failure mechanism during reflow is complex, contributed by combined effects of process defects, interfacial adhesion strength, moisture, vapor pressure, thermo-mechanical stress, and hygro-mechanical stress. Therefore, there is a need for comprehensive studies on moisture diffusion, thermal, hygro-mechanical

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stress, thermo-mechanical stress, and vapor pressure modeling. An integrated stress model with interfacial fracture mechanics is then established to study the QFN package stress, and compute the strain energy release rate when delamination is initiated. It is an useful tool to analyze and enhance the reliability of package, minimizing the delamination and popcorn failures encountered during reflow.

The package vapor pressure distribution during reflow is the key factor in understanding the failure mechanism. Moisture diffusion model is applied to predict the local moisture concentration at the critical interfaces, which can be used for subsequent vapor pressure calculations. High moisture concentration weakens the critical interfacial adhesion, generates vapor pressure during reflow, and induces hygro-mechanical stress in the package. The vapor pressure induces additional mismatch to the package, which is of the same order as the CTE and CME mismatch. When the interfacial adhesion is reduced to the level below the stress predicted by the integrated stress model, delamination will occur.

For both die/mold compound and die/die attach interfaces, G increases with a longer crack length, and mode mixity decreases with a longer crack length. The propagation of an initial crack depends on the relative values of G and G_c. The contribution of vapor pressure to interfacial delamination is significant, especially when there is a defect or crack along the interface.

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CHAPTER 5 BOARD LEVEL SOLDER JOINT RELIABILITY MODELING

5.1 INTRODUCTION

Board-level solder joint reliability is important for CSPs during thermal cycling test. The typical test condition required is -40°C to 125°C to ensure a reliable package performance under the extreme operating conditions. The required fatigue life varies among the customers, e.g., 1000 cycles under -40°C to 125°C thermal cycling test.

However, the process of thermal cycling test is time-consuming and costly. Therefore, FEA modeling [78-107, 122-130] is widely used as an analysis tool for solder joint reliability, especially during the design stage of new package. A fatigue life prediction accuracy of ±2x is generally considered adequate due to the complex nature of solder material's creep behavior, and also uncertainty in the board level thermal cycling test.

Here, modeling and testing of three types of 0.5mm pitch CSPs are analyzed for TFBGA, QFN, and WL-CSP. Complete board level solder joint reliability comprises of thermal cycling test, drop test, vibration test, bending test, and twisting test. TFBGA, for example, has different failure mode and mechanism under thermal cycling and drop test. Design engineers have to compromise on various board level design constraints and customer requirements. The design recommendations given in this chapter are based on thermal cycling test.

5.2 BOARD LEVEL THERMAL CYCLING TEST

Board level thermal cycling tests were performed on TFBGA, QFN, and WL-CSP. Test board with daisy-chain routing is used to monitor the resistance change resulted from solder joint failure. Resistance reading above 300Ω is considered as a failure by

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event detector, a real-time resistance monitoring system. The test standard followed is JESD22-A104-B, and thermal profile of -40°C to 125°C (40 min/cycle) is applied.

The cycles to failure, Weibull plots of these CSPs can be obtained from thermal cycling tests. The Weibull equation can be fully described with the availability of two Weibull parameters, β and η, by

$$N = \eta[-\ln(1-F_r)]^{\frac{1}{\beta}} \tag{5.1}$$

where N is the solder ball fatigue life at corresponding failure rate (F_r), β is the slope of Weibull plot, and η is the characteristic life at 63.2% failure rate, which can be correlated directly with FEA predicted fatigue life, computed from strain energy density (SED) per cycle.

5.3 TFBGA FATIGUE MODEL

5.3.1 Background

TFBGA packages are now widely used in the telecommunication applications, e.g., mobile phone, because of its high density and high performance interconnect technology. TFBGA has thin substrate of 0.22mm, 0.6mm mold compound thickness, and fine ball pitch of 0.5mm. It is a type of CSP and can be assembled and molded in matrix form for cost-saving.

5.3.2 SOLDER JOINT FATIGUE MODEL

Both global and local 3D finite element models are constructed for TFBGA on board to predict the fatigue life of solder joint during the thermal cycling test. Figure 5.1 shows a sample model of TFBGA108 - 7x7mm, 0.5mm pitch, with 3 rows peripheral solder balls. Temperature-dependent material properties are considered for the TFBGA

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package materials used, e.g. CTEs of mold compound and die attach materials, and modulus of solder material. Stress-free temperature is assumed to be 125°C, highest temperature of thermal cycling test. The boundary conditions are similar to typical structural model (see Figure 3.6), except here is a 3D model. For solder material, Anand's viscoplastic model [78] is applied to describe the creep behavior (see Appendix for more details). The rest of the materials are assumed to be linear elastic. Board material is considered to be orthotropic. The thermo-mechanical material properties, i.e. CTEs, T_g, moduli, and minor Poisson's ratio, are listed in Table 5.1.

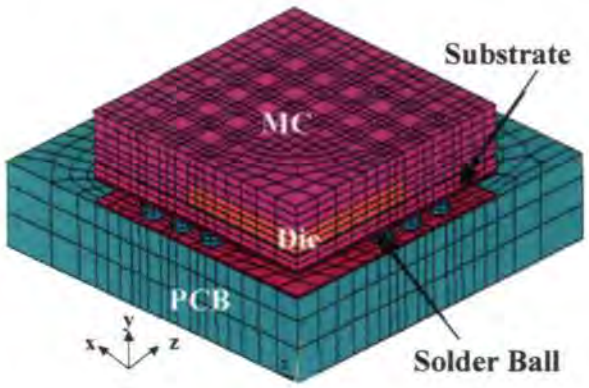

Figure 5.1. Model for TFBGA108 – 7x7 on board

Table 5.1. Material properties applied in TFBGA model

Materials	**CTE1 (ppm/°C)**	**CTE2 (ppm/°C)**	**T_g (°C)**	**Modulus (GPa)**	**Poisson's Ratio**
Silicon Die	2.8		-	131	0.3
Cu Pad	17.7		-	117	0.3
Mold Compound	8	32	165	25.02	0.3
Die Attach	72	145	24	0.5	0.3
Eutectic Solder Ball	25		-	$35.37-0.15T_{[°C]}$	0.4
Solder Mask	95		-	5	0.3
FR4 Board	x,z : 17.6 (in-plane) y : 64.1 (out-of-plane)		-	x,z : 25.4 y : 11	xy: 0.39 yz: 0.39 xz: 0.11
BT Substrate	x,z : 12.42 (in-plane) y : 57 (out-of-plane)		-	x,z : 26 y : 11	xy: 0.39 yz: 0.39 xz: 0.11

* Sources: all from material suppliers. Modulus of MC and DA are storage modulus.

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Firstly, global model with rough-mesh solder balls is solved to identify the critical solder ball with the maximum plastic work or strain energy density (SED) per cycle. The solution time required is about half of detailed local model. The critical solder ball for TFBGA108 studied is observed to be at the diagonal package corner (see Figure 5.2). Then, a local model with much finer mesh is established for the critical solder ball, and solved to obtain accurate SED along the top layer of solder ball, which is the potential failure interface for crack propagation. The local model has detailed pad design, e.g. SMD (Solder Mask Defined) pad on substrate side and NSMD (Non Solder Mask Defined) pad on PCB side, with realistic shape of non-spherical solder ball (see Figure 5.3). The element mesh mismatch between interfaces of local and global models are linked by constraint equations to interpolate the displacements along the boundary. This methodology saves the long computational time required for global model with fine solder mesh for all solder balls, but still obtains reasonable accuracy of results required for the critical solder ball. However, it requires detailed and complex geometry model construction.

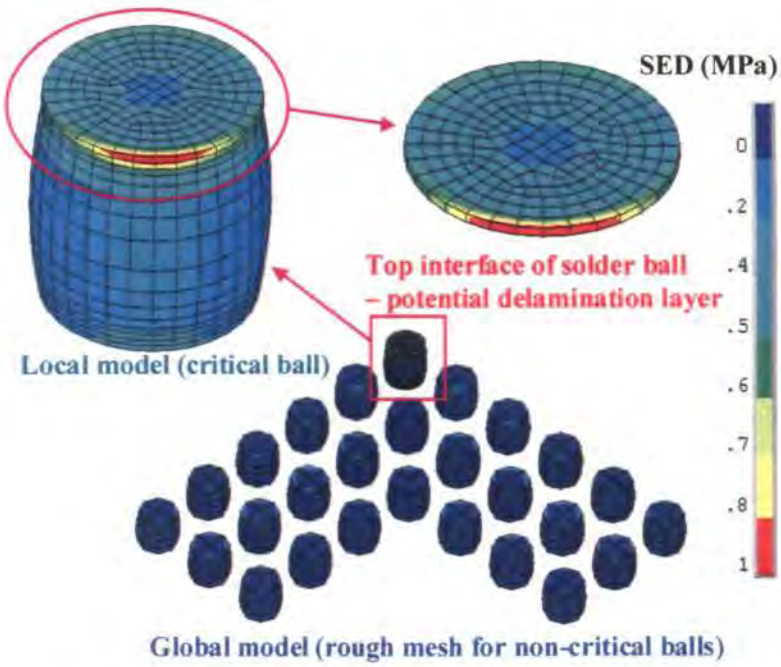

Figure 5.2. Transition from global to local model

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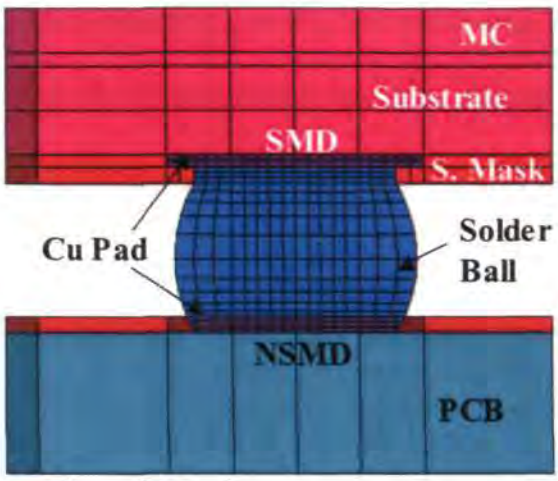

Figure 5.3. Details of local model for critical solder ball

Modified Darveaux's method is applied to calculate the average SED per cycle accumulated along the critical failure interface, i.e. top solder layer. Larger SED leads to shorter solder joint fatigue life. The SED obtained from the viscoplastic modeling can then be related to compute the characteristic life:

$$\eta = a / [C_1 (SED)^{C2}] \qquad (5.2)$$

where η is the fatigue life at 63.2% failure rate, C_1 *and* C_2 (0.93E-7 and 1.59 respectively) are the unique correlation constants derived in this thesis, and a is the length of critical pad interface (diameter of solder mask opening). This modified approach does not consider the crack initiation life (see Eqs. (2.7)-(2.9)), and assumes that the crack propagation life is dominant. This assumption is confirmed by good FEA-thermal cycling correlation (see later section).

There are no universal correlation constants, because these values are dependent on the type of packages and finite element model constructed. Since the original constants published by Darveaux were derived for larger BGA packages [78-79], there is a need to modify the constants for application in TFBGA and other CSPs. The constants can be curve-fitted from correlation of FEA and thermal cycling test data, to minimize the

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errors induced during board assembly, testing, and modeling. The same constants can then be applied confidently for further design analysis. This approach is more accurate than using the original Darveaux constants.

5.3.3 FEA-THERMAL CYCLING CORRELATION

From the failure analysis (see Figure 5.4), it is clear that the diagonal solder joint fails first, and the crack initiated propagates through the top solder ball interface. The failure mode and location agree well with the maximum SED predicted by modeling (see Figure 5.2).

Figure 5.4. Failure analysis of solder ball

Board level thermal cycling tests were performed on seven different types of TFBGA packages. Figure 5.5 shows that the FEA-thermal cycling correlation is within ±13% error, which is much better than ±2x error acceptable by Darveaux [78-79]. Correlation constants (C_1 and C_2) in Eq. (5.2) are iterated such that the fatigue life differences between modeling and experiment data are minimized using least square fit method. Similar modified constants are applied throughout the rest of parametric studies of package geometry and material properties, to obtain a consistent relative comparison of solder joint fatigue life. In future, when there are more thermal cycling

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results available for other cases, the correlation constants may be fine-tuned further for more accurate fatigue life prediction. Nevertheless, for typical design analysis of solder joint performance, the relative life prediction is more meaningful.

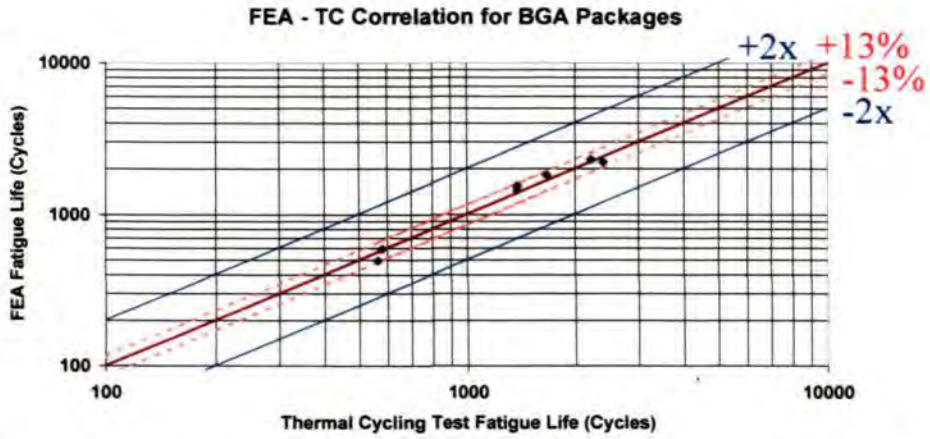

Figure 5.5. Correlation of modeling and thermal cycling tests for TFBGA

5.3.4 Design Analysis of TFBGA

The validated TFBGA fatigue model is applied for parametric studies of package geometry and material properties, to enhance the board level solder joint reliability. There are 14 effects studied relative to the control case (printed in bold font, one effect studied at a time), and results are tabulated in Table 5.2. The package details of the control case, TFBGA108-7x7, is listed in Table 5.3. For parametric studies, one design variable will be changed at a time with respect to the control case. Design optimization is not considered as it requires knowledge of package manufacturability and material availability, which is usually unknown during the early design phase of a new package.

It is a comprehensive analysis on effects of TFBGA die area size, die thickness, ball standoff, maximum ball diameter, solder mask opening, board size, board thickness, substrate thickness, mold compound thickness, modulus and CTE of mold compound, temperature range of thermal cycling test, ball layout pattern (number of balls remains constant), and number of solder balls (ball pitch is constant).

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Table 5.2. Summary of TFBGA parametric studies

No	Design Variations	Values	Life (cycles)	% Difference
1	Die size	**3.74^2 mm**	1547	-
		4.74^2 mm	1186	-23.3
2	Die Thickness	**0.235 mm**	1547	-
		0.375 mm	1450	-6.3
3	Ball Standoff	**0.25 mm**	1547	-
		0.30 mm	1720	11.2
4	Max. Ball Diameter	**0.30 mm**	1547	-
		0.40 mm	1303	-15.8
5	Solder Mask Opening	**0.275 mm**	1547	-
		0.350 mm	2410	55.8
6	Board Size	**10x10 mm**	1547	-
		20x20 mm	1398	-9.6
7	Board Thickness	**1.0 mm**	1547	-
		1.6 mm	1060	-31.5
8	Substrate Thickness	**0.22 mm**	1547	-
		0.30 mm	1683	8.8
9	MC Thickness	0.5 mm	1618	4.6
		0.6 mm	1547	-
10	MC Modulus	20 GPa	1683	8.8
		25 GPa	1547	-
11	MC CTE	**8 ppm/°C**	1547	-
		11 ppm/°C	1887	22.0
12	TC Temp. Range	**-40 to 125°C**	1547	-
		0 to 100°C	4503	191.2
13	Ball Layout Pattern	**Depopulated**	1547	-
		Full Array	1338	-13.5
14	Number of Solder Balls	**108**	1547	-
		144	1639	6.0

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Table 5.3. Package parameters for the correlation case

Design Parameters	Values
Package Size	7x7 mm
I/O	108 (3 rows Depopulated Array)
Die Size	3.74x3.74 mm
PCB Thickness	1 mm
Ball Standoff	0.25 mm (eutectic solder)
Ball Pitch / Diameter	0.5 / 0.3 mm
Solder Mask Opening	0.275 mm
MC Thickness	0.6 mm
Substrate Thickness	0.22 mm
TC Test Condition	-40 to 125°C

Effect of Die Size

Bigger die size has shorter fatigue life, because the die edge is closer to the critical diagonal ball, resulting in more local CTE mismatch. The die also reduces the overall package CTE, leading to greater global CTE mismatch with the board, and more stress induced in the solder ball. For the TFBGA package studied, the Distance to Neutral Point (DNP) effect is more dominant than the die edge effect. Therefore, the failure occurs at the outermost diagonal corner solder joint, instead of under the die corner.

Effect of Die Thickness

Die thickness has little effect on fatigue life. Thicker die has worse solder joint performance, because there is more local CTE mismatch between die and solder joint. Thicker die implies that the overall CTE of package is lower, resulting in more global CTE mismatch with the FR4 board. Thinner board is more compliant, and therefore the strain induced in critical solder ball is lower.

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Effect of Ball Standoff

Higher ball standoff helps to increase the fatigue life. By changing the ball standoff from 0.25mm to 0.3mm, the fatigue life can be enhanced by 11%. The larger separation distance of solder helps to reduce the shear strain induced during thermal cycling.

Effect of Maximum Ball Diameter

For the barrel-shape solder ball studied, the maximum ball diameter (with the same ball standoff and solder mask opening) has negative effect on fatigue life. This effect may be solder joint shape-dependent. The collapse of solder ball during reflow leads to larger maximum ball diameter and shorter ball standoff (combination of two negative effects studied), which weaken the fatigue life.

Effect of Solder Mask Opening

For SMD pad design, size of solder mask opening determines the interfacial length of solder ball and upper copper pad. According to Eq. (5.2), larger solder mask opening requires longer time for crack to propagate through the failure interface. This effect is very significant.

Effect of Board Size

The board size has little effect on fatigue life. Bigger board size will induce slightly larger global CTE mismatch with the package. Therefore, in fatigue modeling, smaller board size may be assumed to reduce the computational time.

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Effect of Board Thickness

Thicker board has much lower fatigue life because the global CTE mismatch between package and board is increased. Thinner board is more compliant, and therefore the strain induced in critical solder ball is reduced. It is important to use consistent board size and thickness in the thermal cycling test to minimize variations among packages of similar type.

Effect of Substrate Thickness

Thicker substrate only slightly improves the fatigue life by increasing the overall package CTE, and reducing global CTE mismatch with the board. It implies that future substrate design can be thinner to reduce the cost, without significant negative effect on the fatigue life.

Effect of Mold Compound Thickness

Sometimes thinner mold compound is desired to assemble thinner package. Here, thinner mold compound leads to slightly longer fatigue life. The CTE of mold compound used is close to the mean CTE of the package (die + substrate + mold compound). Therefore, the thickness of mold compound has little effect on the fatigue life.

Effect of Mold Compound Modulus

Lower mold compound modulus helps to slightly increase the fatigue life because the material is less stiff, therefore inducing less stress to the neighboring materials.

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Effect of Mold Compound CTE

Higher mold compound CTE helps to increase the fatigue life, as it increases the mean package CTE, and reduces the CTE mismatch with PCB. Ideally, there should be an optimum mold compound CTE (see Section 5.4.4 on QFN) which minimizes the global CTE mismatch between the package and the board. This requires more modeling trials of different CTE values, ranging from 8 to 30 ppm/°C, which will be reported in the future study.

Effect of Temperature Range of Thermal Cycling

The effect of temperature range of thermal cycling on solder joint reliability is significant. Thermal cycling test with larger temperature difference results in lower fatigue life, due to larger thermal induced stress and strain. Test condition of 0 to 100°C has 191% longer fatigue life than –40°C to 125°C temperature range. Therefore, it is important to set a standard test condition for thermal cycling test. Modeling can be useful to convert the past experimental data obtained from different sources or various test conditions.

Effect of Ball Layout Array

With the same number of I/O (108 for this case), depopulated array ball layout (3 rows peripheral) has better fatigue performance than full array (slightly larger ball pitch), because it makes use of more critical peripheral solder balls to support the maximum SED induced. For full array, solder balls under the center of package are "wasted" because they have relatively lower SED than the solder ball under the package edge. The depopulated array helps to distribute the SED more uniformly among the

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solder balls. Alternatively, dummy balls may be used for critical diagonal corner balls, at the expense of extra cost, to improve the fatigue life.

Effect of Number of Solder Balls

For fixed ball pitch, package with more solder balls (full array of 144 balls vs. depopulated array with 108 balls) helps to slightly improve the fatigue life because the SED is shared by more solder balls. However, since the critical balls are along the package peripheral, the extra balls of full array under the package center have no significant improvement on the fatigue life.

5.4 QFN FATIGUE MODEL

5.4.1 Background

QFN, a type of leadframe Chip Scale Package (CSP), is getting popular as a low-cost solution for applications with low pin-count requirements. A schematic of QFN-8x8mm package used in this study is shown in Figure 5.6. The peripheral leads are exposed at the package bottom for soldering to the board. Extra soldering under the center die pad and at diagonal corners is optional.

Currently there are very few publications available on board-level solder joint reliability modeling and testing of QFN packages [23-26]. In this thesis, QFN fatigue model with accurate life prediction capability is established. Many in-house thermal cycling test data are available for correlation with modeling.

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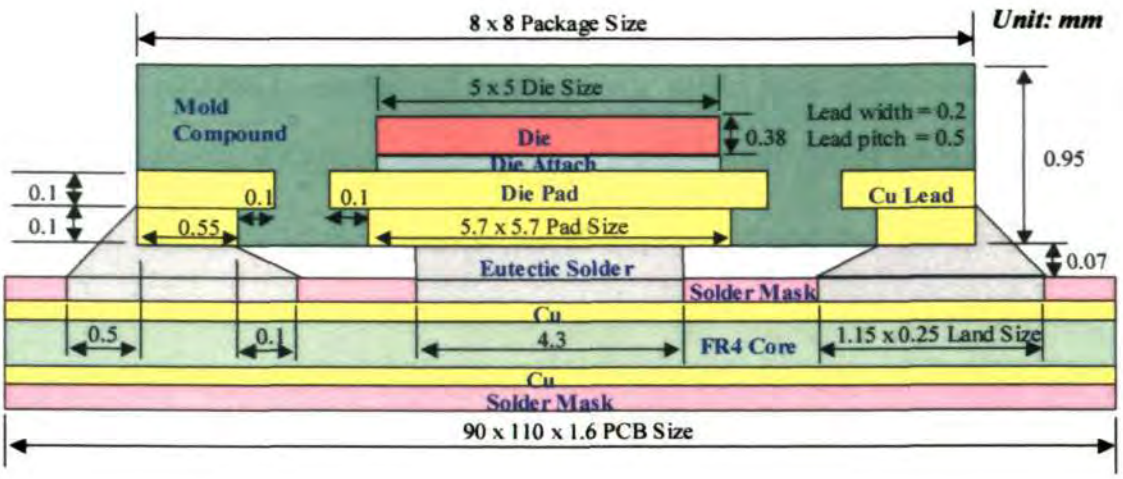

Figure 5.6. Schematic of QFN-8x8mm package on board

5.4.2 Solder Joint Fatigue Model

Figure 5.7 shows the 3D FEA sliced model used for QFN-8x8mm package. Half model is constructed due to symmetry. Only one row of lead with solder is simulated to reduce the computation time. Compared to full 3D model, the accuracy of sliced model is acceptable [79], and both models give the same trend of results, useful for relative comparison of solder joint fatigue life.

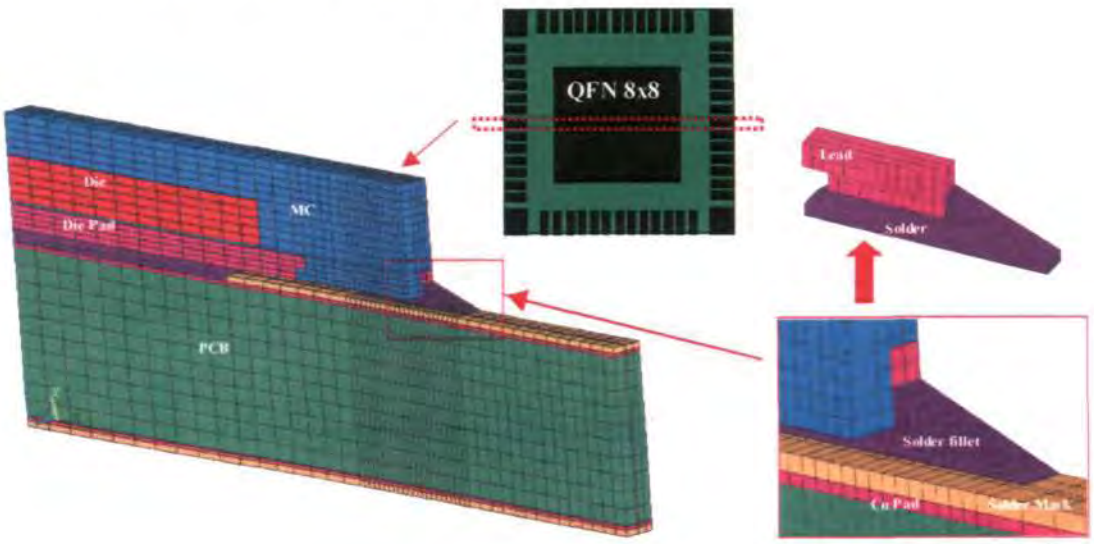

Figure 5.7. 3D sliced model for QFN-8x8

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The solder fillet is included, and constant element size is maintained in the parametric modeling, especially for viscoplastic solder joint (global element size of 35μm). Selection of solder element size is arbitrary (but should be consistent in all analysis), especially in the thickness direction [78], because the results will always vary with element size. The cutting surfaces are constrained to have the same displacement. Detailed PCB geometry dimensions such as land size, copper pad, and solder mask, are also considered in the model.

Temperature-dependent material properties are considered for the QFN packaging materials used. For solder material, Anand's model is used to describe the creep behavior. The rest of the materials are assumed to be linear elastic. Board is considered to be orthotropic. The thermo-mechanical material properties are listed in Table 5.4.

Table 5.4. Material properties applied in QFN model

Materials	**CTE_1 (ppm/°C)**	**CTE_2 (ppm/°C)**	**Tg (°C)**	**Modulus (GPa)**
Silicon Die	2.9	-	-	130
Cu Leadframe	16.9	-	-	128.9
Mold Compound	10	33	190	26.29
Die Attach	72	170	-10	0.86
Eutectic Solder Ball	24.5	-	-	45.5
Solder Mask	34.85	-	-	4.14
FR4 Board	17.6	-	-	19.51

* Sources: all from material suppliers. Modulus of MC and DA is storage modulus.

Modified Darveaux's method is applied to predict the fatigue life using SED per cycle accumulated along the critical failure interface, i.e. one layer of element along the top peripheral solder and lead interface. However, the structure of QFN package is very

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different from BGA. Therefore, the fatigue life correlation constants are unique and can be derived through in-house thermal cycling tests. C_1 *and* C_2 are 8.264E-7 and 0.78 respectively, and a is the lead length of QFN (see Eq. (5.2)). The SED per cycle used is calculated between the end of second and third thermal cycling cycles. Figure 5.8 shows that the hysteresis loops of modeling converge after three thermal cycling cycles, with less than 1% difference in SED. For the QFN-8x8 studied, the maximum SED is observed at the top corner of peripheral solder joint, close to the solder fillet. Solder joint under center of die pad has much lower SED.

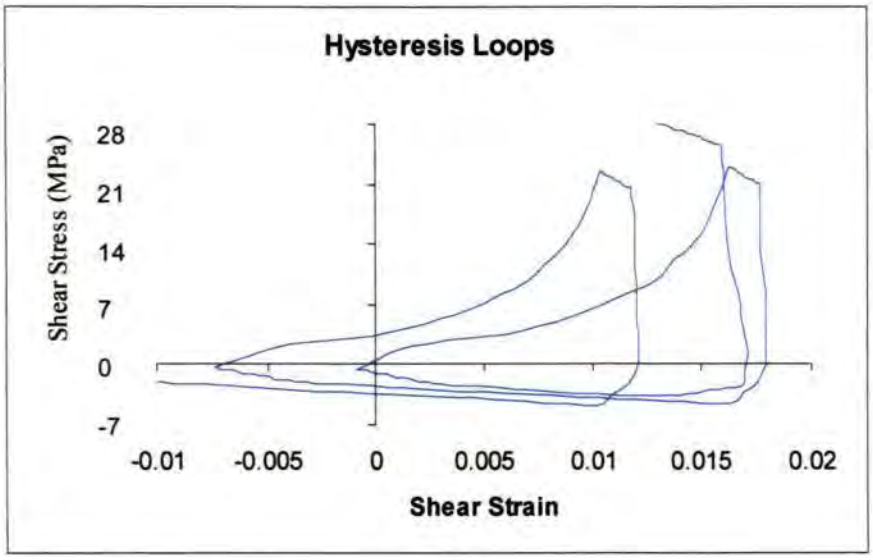

Figure 5.8. Convergence of hysteresis loops

5.4.3 FEA-Thermal Cycling Correlation

From the failure analysis (see Figure 5.9), it is clear that the peripheral solder joint cracks and propagates through the top interface. The failure mode and location agree well with the maximum SED predicted by modeling.

Eight different types of QFN packages were tested under thermal cycling tests. The cycles to failure, Weibull plots of these cases are obtained. The Weibull equation can

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be fully described with the availability of two Weibull parameters, β and η (see Eq. (5.1)). The results are listed in Table 5.5. In general, the experimental data shows that the solder joint fatigue life of QFN can be enhanced with:

1) Smaller QFN package size

- QFN-4x4 has longer fatigue life (about 2500 cycles) than QFN-8x8

2) More center pad soldering

- Solder coverage of 91% has longer fatigue life (176 cycles) than 75% coverage

3) Thinner die is better

- Die thickness of 0.24mm has longer fatigue life (1903 cycles) than 0.36mm

4) Mold compound with higher CTE

- Mold compound CTE of 16ppm/°C has longer fatigue life (1763 cycles) than 10ppm/°C

5) Package with solder high fillet is better

- 240 longer cycles

These relative trends of thermal cycling results correlate well the modeling studies (see later section).

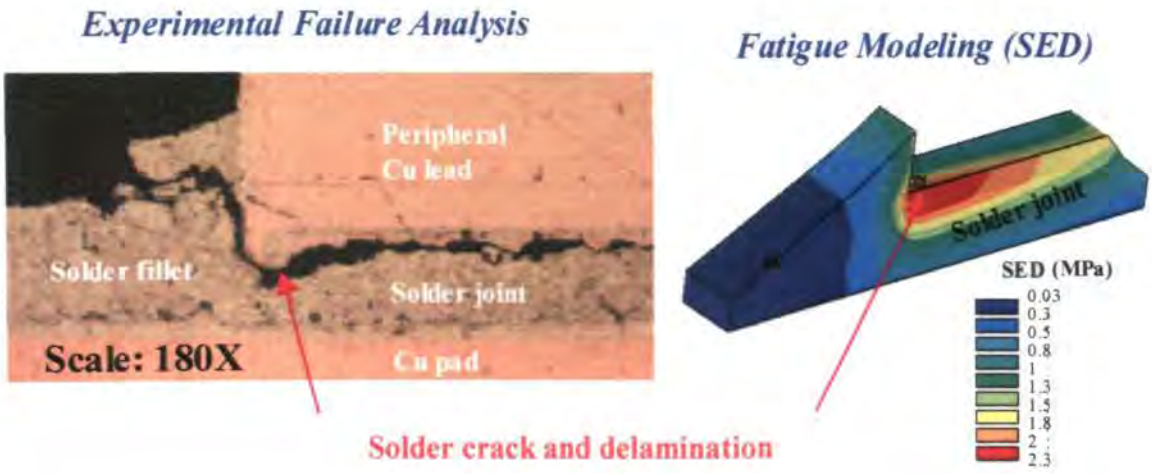

Figure 5.9. Correlation of failure analysis and SED of critical solder joint

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Table 5.5. Thermal cycling test results

Case	Package	Dominant Effect	β (slope)	η (cycles)
1	QFN-4x4	Mold compound CTE=10ppm/°C	3.92	3131
2	QFN-4x4	Mold compound CTE=16ppm/°C	7.57	4894
3	QFN-4x4	Die thickness = 0.24mm	5.40	4646
4	QFN-4x4	Die thickness = 0.36mm	1.66	2743
5	QFN-8x8	75% center pad soldering	4.94	1242
6	QFN-8x8	91% center pad soldering	4.85	1426
7	QFN-8x8	Without solder fillet	8.09	631
8	QFN-8x8	With solder fillet	5.85	871

For the eight correlation cases, SED per cycle can be obtained from modeling, and characteristic life is determined by experiment. Correlation constants (C_1 and C_2) in Eq. (5.2) are iterated such that the fatigue life differences between modeling and experiment data are minimized using least square fit method. Figure 5.10 shows that the FEA-thermal cycling correlation is within ±34% error, which is much better than ±2x error acceptable by Darveaux [78-79]. Similar modified constants are applied throughout the rest of parametric studies of package geometry and material properties, to obtain a consistent relative comparison of solder joint fatigue life.

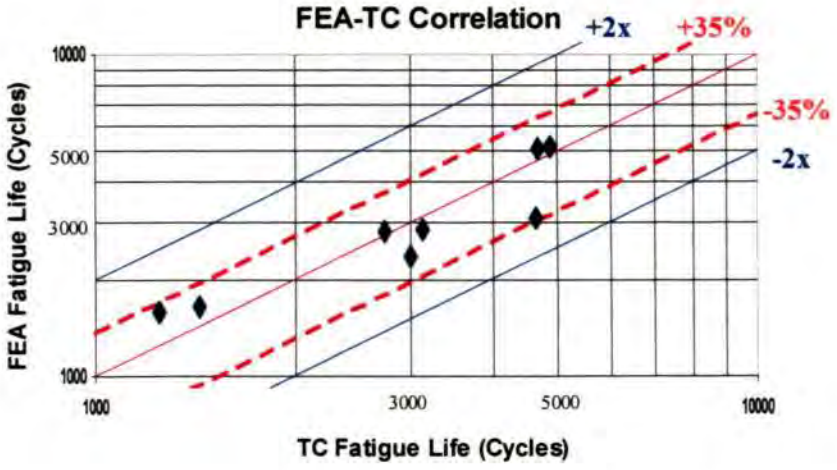

Figure 5.10. Correlation of modeling and thermal cycling tests for QFN

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5.4.4 Design Analysis

The validated QFN fatigue model is applied for parametric studies of package geometry and material properties, to enhance the board-level solder joint reliability. The package geometry of the control case, QFN-8x8, is shown in Figure 5.6. The predicted characteristic life is 1356 cycles. There are 17 effects studied relative to the control case (printed in bold font, one effect studied at a time), and results are tabulated in Table 5.6.

It is a comprehensive analysis on effects of type of QFN package, amount of center pad soldering, die size and thickness, die pad size, board thickness, land size, lead size, lead pitch, solder standoff, solder fillet, mold compound CTE and modulus, die attach materials, and temperature range of thermal cycling test. There are total of 30 different cases simulated (one variable at a time from the control case). Although the design analyses are studied relative to QFN-8x8, the effects of these design parameters on other QFN packages (QFN-4x4, 5x5, 6x6, and 7x7) are similar (magnitude may be different).

Effect of Type of QFN Package

The configurations of QFN-4x4 to 8x8 packages (package size, pad size, die size, and number of I/O) are listed in Table 5.7. Results from Table 5.6 show that smaller type of QFN package has longer fatigue life. The relative trend of this effect is consistent with thermal cycling test results. Smaller package size induces less warpage and smaller relative displacements in the critical solder joint. Smaller package also has smaller die size, which is good for solder joint reliability. QFN-4x4 has more than double longer fatigue life than QFN-8x8.

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Table 5.6. Summary of results for QFN design analysis

No	Design Variations	Values	Life (cycle)	% Difference
1	Type of QFN package	4x4mm (20L)	2928	115.6
		5x5mm (28L)	2165	59.7
		6x6mm (36L)	2015	48.6
		7x7mm (44L)	1635	20.6
		8x8mm (52L)	1356	-
2	Amount of center pad soldering	50%	1155	-14.8
		75%	1356	-
		100%	1739	28.3
3	Die size	2.5 x 2.5mm	2776	104.8
		5.0 x 5.0mm	1356	-
		5.5 x 5.5mm	1186	-12.5
4	Die thickness	0.25mm	1670	23.1
		0.38mm	1356	-
		0.50mm	1266	-6.7
5	Die pad size	5.2 x 5.2mm	1185	-12.6
		5.7 x 5.7mm	1356	-
6	Board thickness	0.8mm	2959	118.3
		1.6mm	1356	-
7	Land length	1.00mm	1329	-2.0
		1.15mm	1356	-
8	Lead/land length	0.40 / 1.00mm	769	-43.3
		0.55 / 1.15mm	1356	-
9	Lead/land width	**0.2 / 0.25mm**	1356	-
		0.3 / 0.35mm	2156	59.0
10	Lead pitch	**0.50mm**	1356	-
		0.65mm	1079	-20.4
11	Solder standoff	50μm	1126	-17.0
		70μm	1356	-
12	Solder fillet	***With***	1356	-
		Without	1129	-16.7
13	Fillet length (inner/outer)	**0.1/0.5mm**	1356	-
		0.3/0.3mm	1303	-3.9
14	MC CTE	**10 ppm/°C**	1356	-
		17.6 ppm/°C	2421	78.5
		24.5 ppm/°C	3475	156.3
		28 ppm/°C	3684	171.7
		32 ppm/°C	3551	161.9
15	MC modulus (MPa)	21032 (-20%)	1399	3.2
		26290	1356	-
		31548 (+20%)	1329	-2.0
16	DA materials	**Type-Q**	1356	-
		Type-A	1409	3.9
		Type-S	1446	6.6
17	Temp. range of thermal cycling test	-40 to 125°C	1922	41.7
		-40 to 150°C	1356	-

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Table 5.7. Configurations of QFN-4x4 to 8x8 packages

QFN	Leads	Pad Size	Die Size
4x4mm	20L	2.1x2.1mm	2x2mm
5x5mm	28L	2.7x2.7mm	2.5x2.5mm
6x6mm	36L	3.7x3.7mm	3x3mm
7x7mm	44L	4.7x4.7mm	4x4mm
8x8mm	52L	5.7x5.7mm	5x5mm

Effect of Amount of Center Pad Soldering

Additional soldering under the center die pad helps to enhance the fatigue life, because there is more solder material to support the plastic work induced during thermal cycling. Therefore, the SED of critical peripheral solder is reduced. For QFN-8x8 with 100% full coverage of center soldering, the fatigue life is 28% longer than the control case with 75% center soldering. The relative trend of this effect is supported by thermal cycling test results.

Effect of Die Size

Smaller die size has longer fatigue life, because the die edge is farther from the peripheral solder joint, resulting in less local CTE thermal mismatch. Compared with die size of 5x5mm, smaller 2.5x2.5mm die size improves the fatigue life by two times. Usually for the same package size, various die sizes may be chosen, depending on the applications.

Effect of Die Thickness

Thinner die has better solder joint performance, because there is less local CTE mismatch between die and solder joint. Thinner die implies that there is more mold

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compound material (higher CTE than die), resulting in less global CTE mismatch with the FR4 board (higher CTE than average package materials). QFN-8x8 with die thickness of 0.25mm has 23% longer life than the control case with 0.38mm die thickness. The relative trend of this effect is similar as thermal cycling test results.

Effect of Die Pad Size

Larger die pad size helps to enhance the fatigue life, but it is not as significant as the effect of die size. Larger pad size results in more copper material (and less mold compound), which has closer CTE to solder joint material. By varying the die pad size from 5.2x5.2mm to 5.7x5.7mm, the fatigue life is increased by 13%.

Effect of Board Thickness

In the model, one-layer board structure is assumed. For QFN-8x8, thinner board has much better solder joint reliability. This is because the FR4 board has larger CTE than mold compound (10ppm/°C) on the top, and thinner board helps to reduce global CTE mismatch between the package and the board. For the case with 0.8mm board thickness, the fatigue life is 118% longer than the typical 1.6mm board.

Effect of Land Length

When the land length is increased while the lead length remains the same, the fatigue life is not significantly affected. This is because the critical top pad interface remains the same, and only the solder fillet length is increased, which has little effect on fatigue life.

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Effect of Lead and Land Length

When both the lead and land length are increased, the fatigue life is enhanced, mainly due to increase in lead length (refer to Eq. (5.2)). The crack initiated takes longer time to propagate through the failure interface with extended length. QFN-8x8 with lead length of 0.55mm has 43% longer fatigue life than lead length of 0.4mm, assuming the number of leads and pitch remains unchanged (full 3D model is required for this combined effect).

Effect of Lead and Land Width

Lead and land width has similar effect as lead and land length, because there is larger pad interface, and more solder material which reduces the critical SED. The fatigue life is improved by 59% when the lead/land width of the control case is increased by 0.1mm.

Effect of Lead Pitch

The sliced model has thickness similar to lead pitch. Smaller lead pitch results in slightly better solder joint performance, when the number of leads and lead length/width remain the same. Smaller lead pitch implies that there is more percentage of solder material per slice of model, which helps to support the stress induced during thermal cycling. Lead pitch of 0.5mm has 20% longer life than lead pitch of 0.65mm. For more accurate modeling of effect of lead pitch, a full 3D model will be established in future study.

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Effect of Solder Standoff

Higher solder standoff has longer fatigue life. The larger separation distance of solder helps to reduce the SED induced during thermal cycling. QFN-8x8 with 70μm solder standoff has 17% longer fatigue life than the case with 50μm solder standoff.

Effect of With and Without Solder Fillet

QFN with solder fillet has slightly better solder joint reliability. With the additional solder material, the maximum SED of peripheral solder joint is reduced and redistributed (see Figure 5.11). The SED of center solder is not significantly affected.

This is assumed that the adhesion of solder fillet/lead edge is the same as the bottom lead/solder interface. From experiment, the solder fillet/lead interface usually fails first, and then the crack propagates inward along the pad interface (see Figure 5.9). QFN-8x8 with solder fillet has 227 longer cycles than the case without solder fillet, and this is close to the 240 cycles predicted by thermal cycling test, and the relative trend is similar.

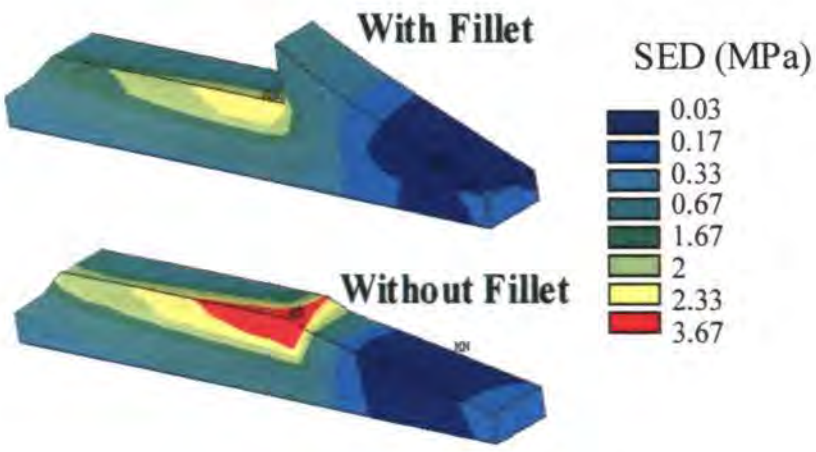

Figure 5.11. Effect of solder fillet on SED

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Effect of Solder Fillet Length (Inner/Outer)

The details of control case with inner solder fillet length of 0.1mm, and outer solder fillet length of 0.5mm are shown in Figure 5.6. The position of lead relative to land which determines the inner/outer fillet length of peripheral solder, has little effect on the fatigue life. The change does not affect the size of pad interface, and the impact on solder volume is not significant.

Effect of Mold Compound CTE

The mold compound CTE used in this analysis equals to CTE1, because the Tg of mold compound is 190°C, much higher than the maximum thermal cycling temperature of 150°C. Figure 5.12 shows that for the control case of QFN-8x8, higher mold compound CTE results in better solder joint reliability, and the optimum CTE is around 28ppm/°C, close to the CTE of eutectic solder. This trend is consistent with thermal cycling test results. At optimum mold compound CTE, both the local CTE mismatch (mold compound and solder) and global CTE mismatch (mold compound and PCB) are minimized. As mold compound CTE is increased, the distribution of high SED is partially shifted from the top corner of peripheral solder joint to the top corner of center solder joint, and the magnitude of maximum SED is reduced. The peripheral solder joint is still more critical, because if there is any failure in center solder joint (dummy connection), the electrical continuity will not be affected. For QFN with optimum mold compound CTE, the fatigue life can be improved by 172% compared with the control case CTE of 10ppm/°C.

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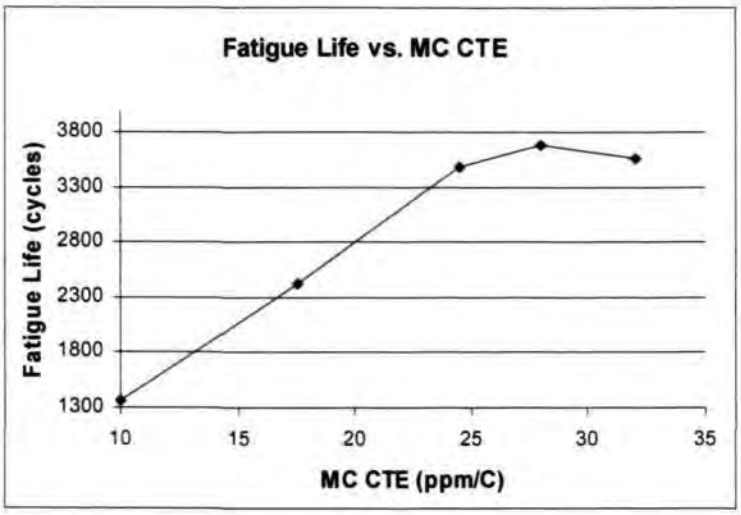

Figure 5.12. Graph of fatigue life vs. MC CTE

Effect of Mold Compound Modulus

The mold compound modulus has little effect on the solder joint reliability, within ±20% range from the control case. Mold compound with lower modulus has slightly longer fatigue life.

Effect of Die Attach Materials

The effect of die attach materials on the fatigue life is not significant. Three types of die attach materials have the following material properties:

- DA-Q (mean CTE = 154.5ppm/°C, E_1 = 0.86GPa)
- DA-A (mean CTE = 115.1ppm/°C, E_1 = 1.76GPa)
- DA-S (mean CTE = 24ppm/°C, E_1 = 31.0GPa)

DA-Q and DA-A are commercial die attach materials. DA-S is a type of soft solder material which has good electrical and thermal performance. Die attach material usually affects die stress, but not so much on board-level solder joint reliability, because the die attach layer is thin and located relatively further away from critical peripheral

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solder joint. Similarly for FCBGA packages, usually package-level underfill enhances solder bump reliability, but not the board-level reliability.

Effect of Temperature Range of Thermal Cycling

The effect of temperature range of thermal cycling on solder joint reliability is significant. Thermal cycling test with larger temperature difference results in lower fatigue life, due to larger thermal induced stress and strain. Test condition of –40°C to 125°C has 42% longer fatigue life than –40°C to 150°C temperature range.

5.4.5 Enhanced QFN Design - PowerQFN

PowerQFN is a variation of QFN package with longer lead length. The peripheral leads are extended out of the package by 0.37mm with a through hole of 0.15mm radius at the end of lead (see Figure 5.13). Extended lead length is designed to enhance the board-level solder joint reliability. The vertical edge of through hole in lead can be plated with tin, allowing better solderability. This feature is intended to reduce the stress induced along the lead/mold compound interface during the singulation process, and therefore better package level reliability. Soft solder is selected as the die attach for better electrical and thermal performance. PowerQFN can be used for medium-power automotive application.

Design analyses are performed to compare QFN-8x8 vs. PowerQFN-8x8, and the effect of special enhanced feature such as extended lead length. The control case of PowerQFN-8x8 has 0.59mm inner lead length and 0.37mm extended lead length. The results are summarized in Table 5.8. Other effects of PowerQFN-8x8 such as die size, die thickness, die pad size, board thickness, amount of center pad soldering, solder

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standoff, and mold compound CTE have the similar relative trends as design analysis studied earlier for QFN-8x8 (see Table 5.6).

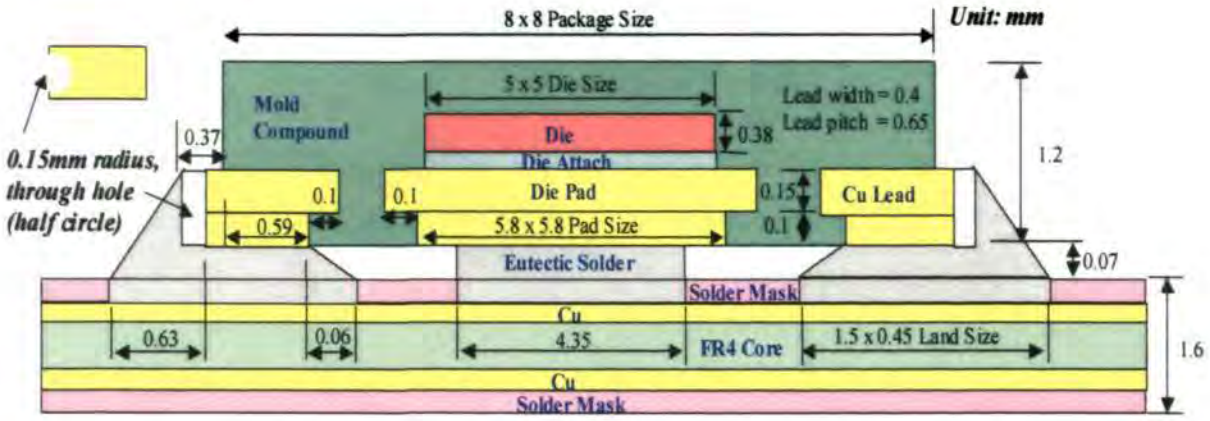

Figure 5.13. Schematic of PowerQFN-8x8mm package on board

Table 5.8. Results of PowerQFN design analysis

No	Design Variation	VALUES	Life (cycle)	% Difference
1	Package type	QFN-8x8	1356	-74.6
		PowerQFN-8x8	5331	-
2	Inner / extended lead length	0.18 / 0.37mm (total = 0.55mm)	1632	-69.4
		0.59 / 0.17mm (total = 0.76mm)	3727	-30.1
		0.59 / 0.37mm (total = 0.96mm)	5331	-

QFN vs. PowerQFN

The SED distributions of peripheral solder joint for PowerQFN-8x8 and QFN-8x8 are shown in Figure 5.14. PowerQFN has much lower SED than QFN, mainly due to extended lead length with more solder joint support, and better solder fillet adhesion around the plated through hole of lead. PowerQFN-8x8 has four times longer fatigue life than QFN-8x8 (see Table 5.8).

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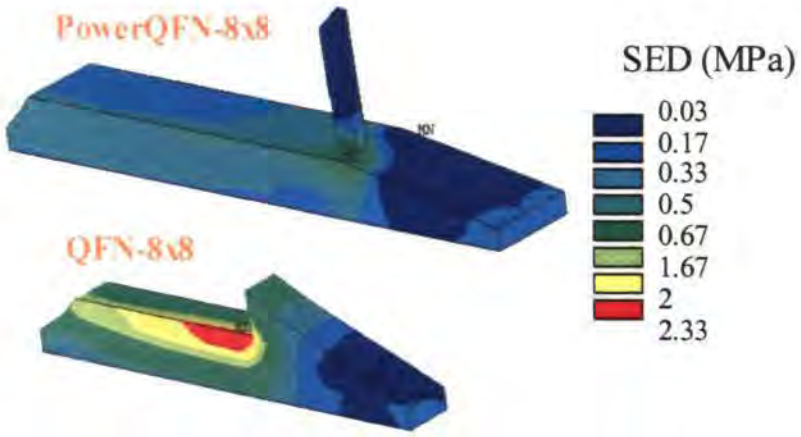

Figure 5.14. SED of QFN vs. PowerQFN

Effects of Total and Extended Lead Length

Similar to QFN, PowerQFN also has better solder joint reliability with longer total lead length. Control case of 0.96mm total lead length has more than three times longer fatigue life than the case with 0.55mm (similar length as QFN-8x8). Besides, the control case with extended lead length of 0.37mm also has 30% longer fatigue life than the case with shorter extended lead length of 0.17mm. The results show that most of the PowerQFN solder joint enhancement is resulted from the effect of longer total lead length (both inner and extended lead length).

5.5 WL-CSP FATIGUE MODEL

5.5.1 Background

Flip-chip (FC) CSP packages, also known as wafer-level CSPs (WL-CSP), are widely used in the low pin count telecommunication applications, e.g., mobile phones and PDAs, because of its high density and high performance interconnect technology. Underfill is usually not applied in WL-CSP assembly, therefore board level solder joint reliability during thermal cycling test is critical. Figure 5.15 shows the schematic

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diagram of 0.5mm bump pitch WL-CSP, 18 I/O, with 2.44x2.19mm die size. The staggered array allows more solder bumps to fit under the same die area.

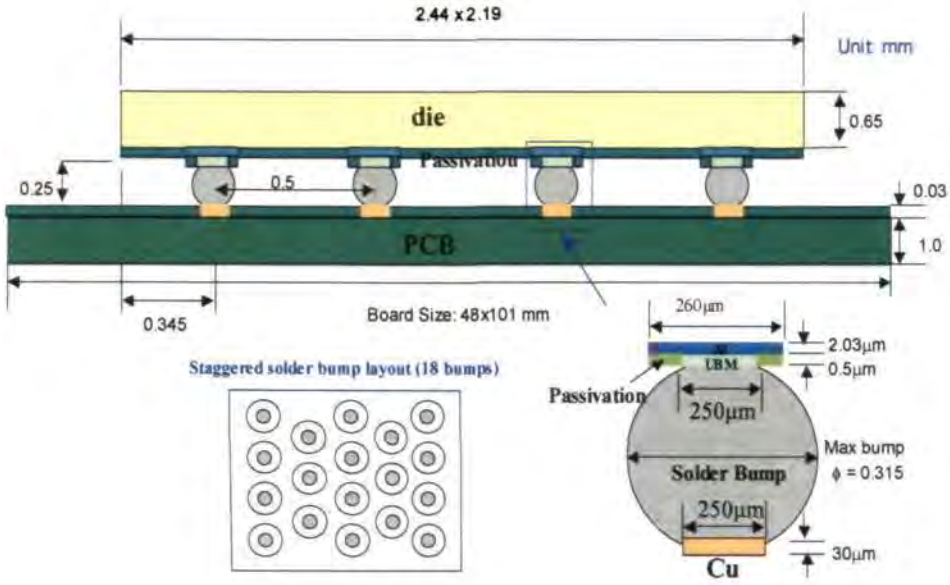

Figure 5.15. Schematic of WL-CSP with 18 staggered bumps

Solder joint fatigue modeling of WL-CSP or flip-chip on board (FCOB) has been studied by some researchers. Pitarressi et al. [17] established parametric model for WL-CSP and studied the variations of thermal cycling profile. Pang et al. [83] predicted the lives of FCOB based on several fatigue models, but no comparison or correlation is made with thermal cycling test data. Yang et al. [125] applied viscoelastic model to describe the curing process of underfill used in FCOB. As for Schubert et al. [126], they considered process-induced imperfections in FCOB assemblies, and compared with modeling. Kim et al. [127] studied the enhancement of solder joint performance using polymer reinforced WLP and Gonzalez et al. [128] applied silicon under the bump configuration. The performance of WL-CSP using lead-free solder [129] and thinner wafer [130] were also investigated. The thesis here provides detailed analysis of WL-CSP with 11 design parameters which were not previously investigated by other researchers.

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5.5.2 Solder Joint Fatigue Model

Here, the similar global/local modeling methodology used for TFBGA (see Section 5.3.2) is extended to the design analysis of WL-CSP, and the fatigue life prediction is correlated to the thermal cycling test data. The thermo-mechanical material properties are listed in Table 5.9.

Table 5.9. Thermo-mechanical material properties

Materials	**CTE (ppm/°C)**	**Modulus (GPa)**
Silicon Die	2.8	131
Copper Pad	17.7	117
Aluminium Pad	23.6	70.6
Passivation (Si_3N_4)	3	200
Eutectic Solder Bump	25	31.6
Solder Mask	95	5
FR4 Board	xy: 17.6 (in-plane) z: 64.1 (out-of-plane)	xy: 25.4 z: 11

* Sources: all from material suppliers

Firstly, global model with rough-mesh solder bumps is solved to identify the critical solder bump with the maximum plastic work or strain energy density (SED) per cycle. The solution time required is about half of detailed local model. The critical solder bump for WL-CSP studied is observed to be at the diagonal die corner (see Figure 5.16). Then, a local model with much finer mesh is established for the critical solder bump, and solved to obtain accurate SED along the top layer of solder bump, which is the potential failure interface for crack propagation.

For WL-CSP, only one set of thermal cycling test result (1014 cycles) is available. Therefore, the same correlation constants (C_1 and C_2) are extracted from the TFBGA

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package group which belongs to similar area-array type of package family. However, Darveaux's method tends to under-predict the fatigue life of WL-CSP, as it was originally formulated for BGA applications. Therefore, a factor of 8.41 is multiplied to the fatigue model to correlate with thermal cycling test data.

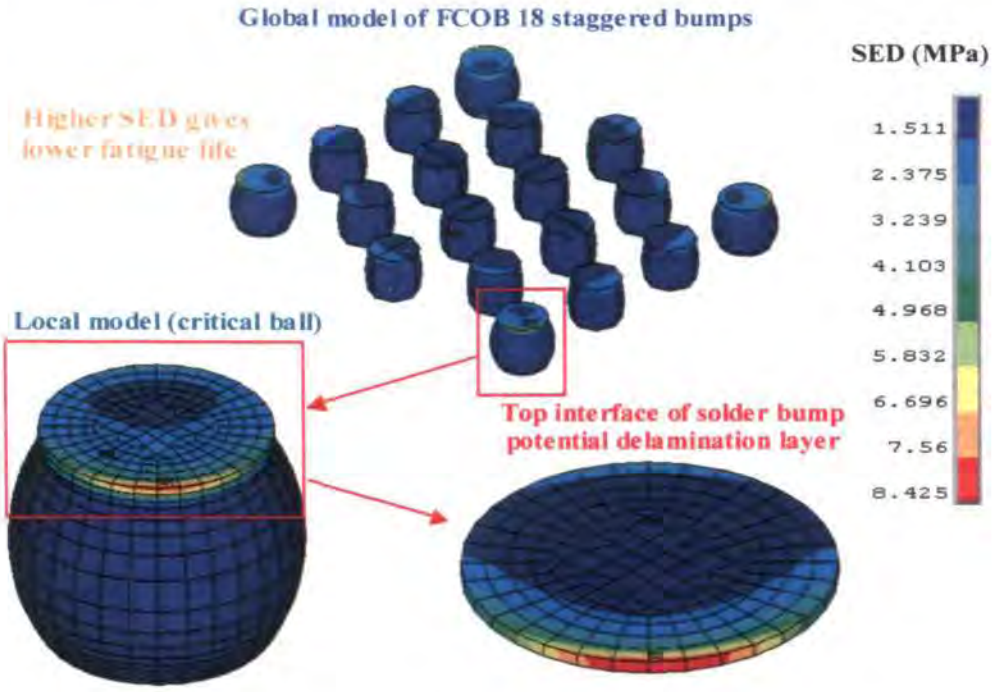

Figure 5.16. SED distribution of WL-CSP solder bumps

5.5.3 Modeling Solution Control

The accuracy of modeling solution depends on element size control and number of solution time steps. Table 5.10 shows the sensitivity results of these modeling variables. The number of time steps (±2x) during temperature ramping and dwelling have little effect on fatigue life prediction. Therefore, for faster solution, less time steps may be used.

It is known that modeling results are more accurate with smaller element size. In this model, the variation of in-plane solder bump element size (0.5x to 2x) has insignificant effect on fatigue life. It shows that the current element size has stabilized.

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However, for solder bump element size in thickness direction, the fatigue life difference is about 6% when coarser element mesh is applied. Therefore, it is important to control a consistent element size, especially in the thickness direction, for the subsequent parametric design analysis (see next section).

In the model, PCB size is assumed to be 3mm larger than die size. When bigger PCB sizes are used (actual board size is 48x101mm), there is little change in results. There is not much difference in result when all bumps are modeled with detailed mesh, compared with one critical bump. Therefore, the previous assumption of using smaller PCB size and detailed mesh for only critical bump to reduce the solution time is acceptable.

Table 5.10. Results of modeling solution control

Design Variations		**Life (Cycles)**	**% Difference**
Time Steps (Ramp/Dwell)	12 / 3 steps	1034	1.97%
	24 / 6 steps	**1014**	-
	48 / 12 steps	997	-1.68%
Bump Element Width	31.2 μm (2x)	1019	0.49%
	15.6 μm	**1014**	-
	7.8 μm (0.5x)	1013	-0.10%
Bump Element Thickness	50 μm	956	-5.72%
	30 μm	**1014**	-
PCB size	**5.44 x 5.19 mm**	**1014**	-
	8.14 x 8.19 mm	1015	0.10%
	15 x 15 mm	1018	0.39%
	20 x 20 mm	1018	0.39%
	48 x 101 mm	1020	0.58%
Detailed Bump Mesh	1 critical bump	**1014**	-
	All bumps	1042	2.75%

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5.5.4 Design Analysis

The critical solder bump of WL-CSP is at the outermost diagonal position, and the failure interface is along the die/solder bump interface (see Figure 5.16). The failure mode and location are consistent with the observation from failure analysis of thermal cycling test samples. WL-CSP is not molded, and therefore the DNP effect is dominant for solder joint reliability. Solder bump further away from die center has the highest SED.

The control case of WL-CSP model is correlated with thermal cycling test, which has a fatigue life of 1014 cycles. The package details of the control case is listed in Table 5.11. The validated WL-CSP fatigue model is then applied for parametric studies of package geometry, material properties and test condition, to enhance the board level solder joint reliability. For parametric studies, one design variable is changed at a time with respect to the control case.

Table 5.11. Package parameters for the control case

Design Parameters	Values
Die Size	2.44 x 2.19 x 0.65 mm
I/O	18 (staggered), 0.5mm pitch
PCB Thickness	1 mm
Bump Standoff	0.25 mm (eutectic solder)
Max. Bump Diameter	0.315 mm
UBM Opening Size	0.25 mm
PCB Pad Size	0.25 mm
TC Test Condition	-40 to 125°C

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There are 11 effects studied relative to the control case (printed in **bold font**, one effect studied at a time), and results are tabulated in Table 5.12. It is a detailed study on effects of PCB CTE (in-plane and out-of-plane) and modulus, PCB thickness, die size and thickness, solder bump standoff and maximum diameter, UBM opening size, PCB pad size, and thermal cycling temperature range.

Effects of PCB CTE, Modulus and Thickness

For PCB, the effect of in-plane CTE (xy) is much more significant than out-of plane CTE (z). The PCB thickness is only 1mm, therefore CTE-z has little effect. Lower PCB in-plane CTE results in less global CTE thermal mismatch with die on top, and therefore longer fatigue life. For WL-CSP, the choice of PCB type is critical. The effects of PCB modulus and thickness are insignificant.

Effects of Die Size and Thickness

Thinner die reduces the global CTE thermal mismatch between die and PCB, and fatigue life is enhanced. If the bump layout and pitch remain constant, the extension of die size (width and length) has little effect on fatigue life. If the bump layout and pitch are varied with bigger die size, the position of outermost corner solder bump will be further away from die center. The fatigue life will then be reduced because of larger DNP effect.

Effects of Bump Standoff and Diameter

It is desirable to have higher bump standoff and smaller maximum bump diameter during the board assembly. Higher bump standoff is known to reduce the interfacial shear stress accumulated during thermal cycling test.

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Table 5.12. Summary of WL-CSP parametric studies

Design Variations		Life (Cycles)	% Difference
PCB CTE-xy (in-plane)	13.0 ppm/°C	1295	27.7%
	17.6 ppm/°C	**1014**	-
PCB CTE-z (out-of-plane)	41 ppm/°C	1013	-0.1%
	64.1 ppm/°C	**1014**	-
PCB Modulus	-20%	1024	1.0%
	25400 MPa	**1014**	-
	+20%	1008	-0.6%
PCB Thickness	**1.0 mm**	**1014**	-
	1.6 mm	1022	0.8%
Die Thickness	0.35 mm	1153	13.7%
	0.65 mm	**1014**	-
Die Size	**2.44 x 2.19 mm**	**1014**	-
	2.70 x 2.45 mm	1002	-1.2%
Bump Standoff	**0.25 mm**	**1014**	-
	0.30 mm	1187	17.1%
Max. Bump Diameter	0.275 mm	1154	13.8%
	0.315 mm	**1014**	-
UBM Opening Size	**0.25 mm**	**1014**	-
	0.275 mm	1151	13.5%
PCB Pad Size	0.20 mm	1139	12.3%
	0.225 mm	1082	6.7%
	0.25 mm	**1014**	-
	0.275 mm	943	-7.0%
Thermal Cycling Temperature Range	-25 / 85 °C	1890	86.4%
	-40 / 85 °C	1238	22.1%
	-40 / 125 °C	**1014**	-

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Effect of UBM Opening Size

The size of UBM opening determines the interfacial crack length between solder bump and die. According to Eq. (5.2), larger UBM opening size requires longer time for crack to propagate through the failure interface, and therefore longer fatigue life. This effect is significant.

Effect of PCB Pad Size

Smaller PCB pad size is useful for solder bump reliability. It helps to redistribute the high stress from critical die/bump interface to PCB pad interface, and reduce the maximum SED.

Effect of Temperature Range of Thermal Cycling

The effect of temperature range of thermal cycling on solder joint reliability is significant. Thermal cycling test with lower temperature difference results in higher fatigue life, due to less thermal induced stress and strain. Test condition of -25°C to 85°C has almost two times longer fatigue life than –40°C to 125°C temperature range. Therefore, it is important to set a standard test condition for thermal cycling test. Modeling can be useful to convert the past experimental data obtained from different sources or at various test conditions, and used for direct comparisons.

5.6 SUMMARY

Detailed solder joint fatigue models with life prediction capability are established for TFBGA, QFN, and WL-CSP. Modified Darveaux's approach is applied with unique correlation constants for each type of CSPs. The validated models have excellent correlation with thermal cycling test results.

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For TFBGA, comprehensive design analyses are performed to study 14 effects, consisting of package geometry, material properties, and thermal cycling test condition. Generally, for enhanced solder joint reliability of TFBGA, it is recommended to have smaller die size, higher solder ball standoff, smaller maximum solder ball diameter, bigger solder mask opening, thinner board, higher mold compound CTE, smaller thermal cycling temperature range, and depopulated array type of ball layout pattern. The effects of die thickness, board size, substrate thickness, mold compound thickness, mold compound modulus, and number of solder balls are relatively insignificant.

For QFN, detailed design analyses are performed to study 17 effects, which consist of package geometry, material properties, and thermal cycling test condition. The relative fatigue life predictions are consistent with experimental observations. Generally, for enhanced solder joint reliability of QFN, it is recommended to have smaller package type, more center pad soldering, smaller die size, thinner die, bigger die pad size, thinner board, longer lead length/width, smaller pitch, higher solder standoff, solder with fillet, higher mold compound CTE, and smaller temperature range of thermal cycling test. The effects of land size, mold compound modulus, and die attach material are not significant. For PowerQFN, the extended lead length is the key feature for significant enhancement in solder joint reliability. For material selection, mold compound with optimum CTE of 28ppm/°C can increase the fatigue life greatly. Center pad soldering has significant effect on solder joint reliability, especially for bigger package size such as QFN-8x8 which has relatively lower fatigue life. Design optimization for both package geometry (e.g. center pad soldering, lead length, and solder standoff) and material properties (e.g. mold compound CTE) may enhance the fatigue life of QFN up to about 5 times.

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Detailed solder joint fatigue models with life prediction capability are established for WL-CSP. Both modeling and experiment show that the critical solder bump of WL-CSP is at the outermost diagonal position, and the failure interface is along the die/solder bump interface. Comprehensive design analyses are performed to study 11 effects, consisting of package geometry, material properties, and thermal cycling test condition. Generally, for enhanced solder joint reliability of WL-CSP, it is recommended to have lower in-plane PCB CTE, thinner die, higher solder bump standoff, smaller maximum solder bump diameters, bigger UBM opening size, smaller PCB pad size, and smaller thermal cycling temperature range. The effects of out-of-plane PCB CTE, PCB modulus, PCB thickness, and die size (same bump layout) are relatively insignificant.

For thermal cycling test, it is important to set consistent test conditions (e.g. temperature range and cycle time) and test board design (e.g. board thickness) for various cases. The standardization helps to make meaningful relative comparison among different cases. One set of thermal cycling test is recommended for each type of CSPs to determine more accurate correlation constants for fatigue modeling and life prediction.

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CHAPTER 6 APPLICATIONS OF SOLDER JOINT FATIGUE MODELING

6.1 INTRODUCTION

Based on the modeling methodology as mentioned in Chapter 5, finite element models are constructed for a few other CSPs to predict the board level fatigue life of solder joint during the thermal cycling test. Design analyses are performed on unique features of these advanced packages to assist in definition of package geometry and material selection.

The modified Darveaux's method is applied to investigate solder joint reliability of new CSPs which are getting popular recently, e.g., stacked die BGA, stacked die QFN, and thermally enhanced BGA package, under board level thermal cycling test. Stacked die CSPs are developed to reduce the footprint and total cost of package, and enable system-in-package (SiP) design through functions integration. Certain design rules learned from single die CSPs (see Chapter 5) may not be applicable for stacked die CSPs. The relationship between package warpage and solder joint fatigue life is also an area of research interest, as both parameters are sensitive to the temperature variation and CTE thermal mismatch. It is studied and reported for the first time in this thesis.

Besides, green package requires the usage of environmental-friendly material such as lead-free solder. The fatigue and creep behavior of lead-free solder is still not well understood by many researchers. A comparison between eutectic solder and lead-free solder (see Chapters 6-8) under thermal cycling test and drop test are investigated. The solder materials have different relative reliability performance as the failure modes and mechanisms are unique, i.e. CTE thermal mismatch for thermal cycling test, but mechanical shock and PCB bending under drop test.

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6.2 LEAD-FREE STACKED DIE BGA PACKAGE

6.2.1 Background

Stacked die or 3D packaging has become popular recently. There are several types of stacked die BGA available in the industry. An example for memory application is stacking of SRAM and Flash dice, which can reduce the total footprint by 28% [131]. Other applications are integrated passives and sensors that can be put together into a SiP with stacked dice. This is particularly useful for mobile phones or PDAs, which emphasizes on smaller and lighter products. Figure 6.1 shows several variations of stacked die interconnect, i.e. wirebond/wirebond (WB-WB), wirebond/flip-chip (WB-FC), and flip-chip/wirebond (FC-WB), being developed and industrialized for mobile electronic applications. The structure can be pyramidal (top die smaller than bottom die) or twin dice (equal in sizes). Mixing flip-chip technique with wirebonding leads to interesting and competitive solutions. In this study, flip-chip/wirebond structure is studied in detail, and comparisons are made with the other two interconnect methods. Besides, lead-free solder materials have been applied in stacked die BGA, to comply with the legislation to eliminate lead in "green" package.

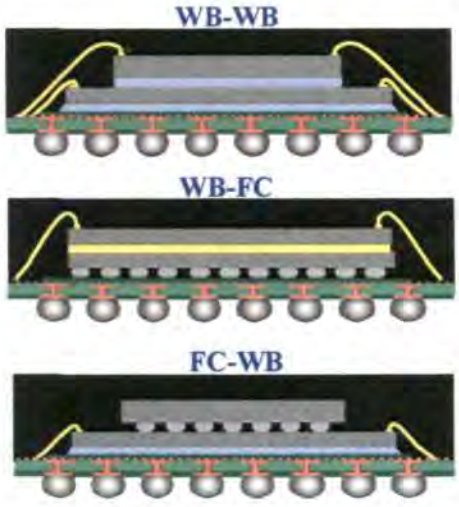

Figure 6.1. Different interconnect methods for stacked die BGA

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Solder joint fatigue modeling of stacked die CSP has been studied by some researchers [15-16]. Testing and modeling of lead-free CSPs (single die) are also investigated [132-133]. However, there are few publications available on lead-free stacked die BGA with mixed flip-chip/wirebond interconnect, and detailed analyses of design parameters. The behavior of critical solder joint in stacked die BGA is much more complex than in single die BGA. There is a need to analyze the stacked BGA design with a systematic and comprehensive approach.

6.2.2 Solder Joint Fatigue Model

3D FEA models are constructed for stacked die BGA to predict the fatigue life of solder joint during the thermal cycling test. Figure 6.2 shows the schematic diagram of 0.5mm ball pitch stacked die BGA, 88 I/O, with 3.6x3.5mm die on top and 5x5mm die on bottom. For lead-free (SnAgCu) and eutectic solder materials, Anand's model is applied to describe the creep behavior. The rest of the materials are assumed to be linear elastic. Board is considered to be orthotropic. The thermo-mechanical material properties are listed in Table 6.1.

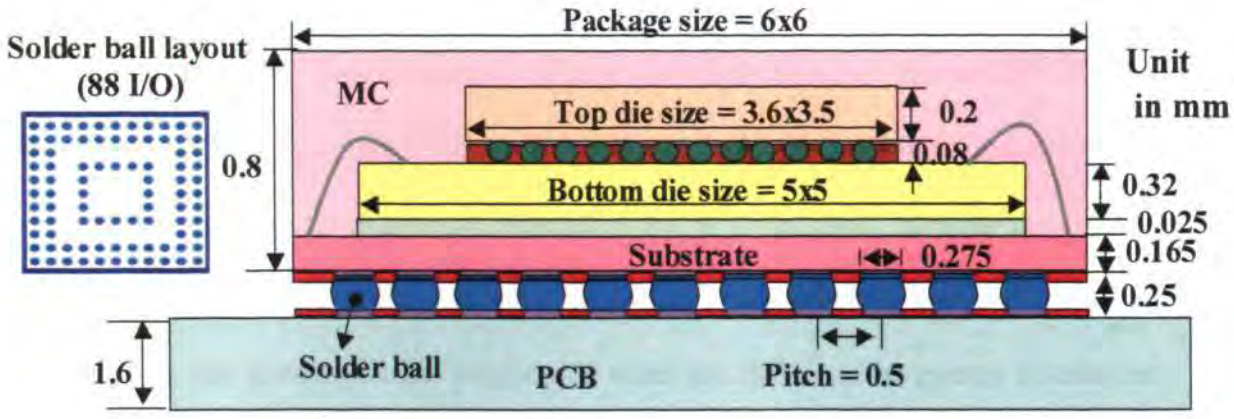

Figure 6.2. Schematic of stacked die mixed flip-chip/wirebond BGA

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Table 6.1. Thermo-mechanical material properties of stacked die BGA

Materials	CTE (ppm/°C)	Modulus (GPa)
Silicon Die	2.8	131
Copper Pad	17.7	117
SnAgCu Solder	17.6	46.4
Eutectic Solder	25	31.6
Solder Mask	95	5
BT Substrate	xy: 12.4 (in-plane) z: 57 (out-of-plane)	xy: 26 z: 11
PCB	xy: 16 (in-plane) z: 65 (out-of-plane)	xy: 16.5 z: 7.2
Die Attach	48 / 140 (Tg = 42°C)	0.64
Underfill	45 / 143 (Tg = 140°C)	5.6
Mold Compound	8 / 32 (Tg = 165°C)	25

* Sources: all from material suppliers. Storage modulus is used for DA, UF, and MC.

6.2.3 Design Analysis

The critical solder ball of stacked die BGA studied is at (4,4) position, between 3.6x3.5mm top die and 5x5mm bottom die (see Figure 6.3, quarter model), and the failure interface is along the top solder/pad interface, similar to single die BGA (see Figure 5.2). The localized die edge effect is more dominant than the DNP (Distance to Neutral Point) effect for solder joint reliability. The most critical solder ball is not at the outermost corner. The characteristic life predicted for this lead-free stacked BGA is 5097 cycles with 1.6mm board thickness, under –40 to 125°C (60 min/cycle) thermal cycling. This design configuration of stacked die BGA is good, because the critical load is nearly evenly distributed between (2,2) and (4,4) solder balls (see Table 6.2). The package can have optimum fatigue life when the SED can be evenly distributed among the solder balls, instead of concentrating at one critical solder ball.

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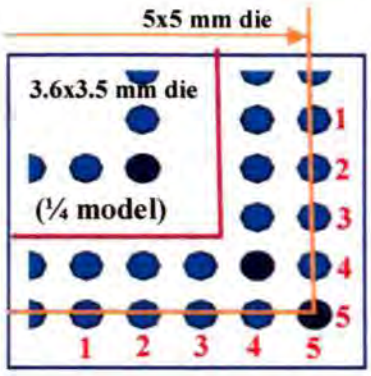

Figure 6.3. Position of solder balls and dice edges

Table 6.2. Effects of solder material and stacked die interconnect methods

Design Variations			Position (Life / cycles)			Critical (lowest)	% Diff.
			(2,2)	(4,4)	(5,5)		
Effects	**Descriptions**						
Solder Material	**Elastic**	**Fatigue**					
	Eutectic	Eutectic	1991	2133	4990	1991	-
	Lead-free	Lead-free	5696	5097	13754	5097	2.6x
	Lead-free	Eutectic	7428	7216	16771	7216	3.6x
	Eutectic	Lead-free	1411	1455	3405	1411	0.7x
Stacked die Interconnect Methods	**FC-WB**		**5696**	**5097**	**13754**	**5097**	-
	WB-WB		5966	4756	13227	4756	-6.7%
	WB-FC		5062	7822	14522	5062	-0.7%
Stacked vs. Single Die	**Stacked Die**		**5696**	**5097**	**13754**	**5097**	-
	Single Die		4576	7113	28984	4576	-10.2%

The stacked die BGA fatigue model is then applied for parametric studies of package geometry and material properties, to enhance the board level solder joint reliability. For parametric studies, one design variable is changed at a time with respect to the control case. The geometry of control case is given in Figure 6.2.

There are 10 effects studied relative to the control case (printed in **bold font**). Critical solder ball is one of (2,2), (4,4) and (5,5) diagonal balls, which has the lowest fatigue life. It is a detailed study on effects of solder material, stacked die structure, dice size and thickness, and mold compound and die attach materials.

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Lead-free vs. Eutectic Solder

Table 6.2 shows that stacked die BGA with lead-free (SnAgCu) solder has 2.6 times longer fatigue life than eutectic solder. The contribution of lead-free material is mainly from elastic mechanical properties (e.g. CTE and modulus) which affect the CTE thermal mismatch, and viscoplastic fatigue properties which govern the creep behavior of solder during thermal cycling. It was observed that the solder material has great performance (3.6 times longer life than eutectic solder), when lead-free elastic properties and eutectic fatigue properties are used. It implies that the elastic properties (mainly CTE) of lead-free solder is the main positive factor. SnAgCu has CTE of 17.6ppm/°C, much lower than CTE of eutectic solder (25ppm/°C). Lower solder CTE results in less CTE thermal mismatch with other main packaging materials, which have CTEs ranging from 2.8 to 17.7ppm/°C.

Effects of Interconnect Methods

Among three different stacked die interconnect combinations (see Figure 6.1), flip-chip/wirebond design has the highest fatigue life (see Table 6.2). The SED is more evenly distributed for flip-chip/wirebond design. The use of flip-chip interconnect between the two dice, creates an interfacial layer with compliant underfill to absorb the die stress.

Similarly, single die TFBGA-6x6mm (die size of 3.6x3.5x0.235mm and 0.6mm mold compound thickness) performs not as good as stacked die BGA package. For single die BGA, the SED is concentrated at innermost (2,2) solder ball, under single die corner. For stacked die, (2,2) and (4,4) solder balls are under the top die and bottom die corner respectively, therefore both are evenly loaded. The difference in dice length helps to redistribute the die stress.

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Effects of Dice Sizes and Thickness

It is desirable to have either larger top die size or larger bottom die size to enhance the fatigue life (see Table 6.3). The position of critical solder ball may shift with die size, because the distribution of stress induced by die edge is changed. When top and bottom dice sizes have the same length, larger die sizes of 5x5mm is better than 3x3mm, because the SED is more uniformly distributed in (2,2) and (4,4) balls. For 5x5mm dice sizes, outermost (5,5) ball (see Figure 6.3) also helps to share the load, therefore the performance is slightly better than control case with smaller top die size of 3.6x3.5mm. Selection of large and even length of top and bottom dice helps to improve fatigue life.

Thicker stacked dice helps to increase the fatigue life. Thickness of top die is more significant than bottom die. This trend is different from previous experience on single die BGA, which prefers smaller die size and thinner die (see Section 5.3.4). The same design guidelines learned from single die BGA may not be applicable for stacked die BGA, due to the complex behavior of multiple die layers.

Effects of Mold Compound and Die Attach Materials

Mold compound CTE has small effect on fatigue life within the range of 6-10 ppm/°C (see Table 6.4). The existing value of 8 ppm/°C is just nice because the SED is nearly evenly distributed between (2,2) and (4,4) balls. Increasing or decreasing the mold compound CTE will shift the critical load more towards one solder ball. For single die BGA, higher mold compound CTE is better for solder joint reliability (see Section 5.3.4). For die attach material, there is little effect on fatigue life, even when it is replaced with underfill material.

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Table 6.3. Effects of dice sizes and thickness

Design Variations			Position (Life / cycles)			Critical	% Diff.
			(2,2)	(4,4)	(5,5)		
Effects	**Descriptions**						
	Top Die	**Bottom Die**					
Top Die Size (mm)	2.5x2.5	5x5	8388	4896	19493	4896	-3.9
	3.6x3.5	**5x5**	**5696**	**5097**	**13754**	**5097**	-
	5x	5x5	5684	5973	13025	5684	11.5
Bottom Die Size (mm)	3.6x3.5	4x4	4889	10218	27006	4889	-4.1
	3.6x3.5	4.5x4.5	5476	8831	16868	5476	7.4
	3.6x3.5	**5x5**	**5696**	**5097**	**13754**	**5097**	-
	3.6x3.5	5.5x5.5	5715	5476	13054	5476	7.4
Top & Bottom Dice Sizes (mm)	3x3	3x3	4921	17965	37762	4921	11.4
	3.6x3.5	**3.6x3.5**	**4418**	**13418**	**26122**	**4418**	-
	5x5	5x5	5684	5973	13025	5684	28.7
Dice Thickness (mm)	**0.2**	**0.32**	**5696**	**5097**	**13754**	**5097**	-
	0.235	0.32	5543	5233	13699	5233	2.7
	0.2	0.335	5740	5110	13412	5110	0.3
	0.235	0.335	5596	5245	13346	5245	2.9

Table 6.4. Effects of mold compound and die attach material properties

Design Variations		Position (Life / cycles)			Critical	% Diff.
		(2,2)	(4,4)	(5,5)		
Effects	**Descriptions**					
MC-CTE	6 ppm/°C	4943	5412	12758	4943	-3.0
	8 ppm/°C	**5696**	**5097**	**13754**	**5097**	-
	10 ppm/°C	6519	4780	12117	4780	-6.2
MC-Modulus	20012.8 MPa	5509	5386	15925	5386	5.7
	25016 MPa	**5696**	**5097**	**13754**	**5097**	-
	30019.2 MPa	5858	4856	11977	4856	-4.7
DA Material	**No change in DA**	**5696**	**5097**	**13754**	**5097**	-
	E-DA = E-UF	5249	5487	12098	5249	3.0
	CTE-DA = CTE UF	5632	5108	13704	5108	0.2

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6.3 MEMS PACKAGE - STACKED DIE TQFN

6.3.1 Background

Accelerometer is a main application of Microelectromechanical Systems (MEMS), fabricated by surface-micromachining technique. When the device experiences a shock, the silicon mass connected by a cantilever will move between two fixed electrodes, resulting in a capacitance change, which can be correlated to linear acceleration. This is a highly sensitive 3-axis accelerometer, and the maximum acceleration is only a few G ($1G = 9.81 m/s^2$).

Traditionally MEMS accelerometer is packaged using small outline (SO) package. Stacked die TQFN (Thick Quad Flat No-lead) is an advanced new package introduced for accelerometer, mainly to reduce the footprint of package. TQFN is a dual and three-axis accelerometer, targeted for consumer products (eg. toys, healthcare, and PDA), industrial, automotive (eg. air bag), and telecommunication applications.

6.3.2 Solder Joint Fatigue Model

3D FEA model is constructed for stacked die TQFN to predict the fatigue life of solder joint during the thermal cycling test. Figure 6.4 shows the schematic diagram of TQFN with 32 leads, 0.65mm lead pitch with ASIC die on top and sensor die/cap on bottom, in a 7x7x1.8mm package. The wafer cap is to protect the sensor die, and they are bonded together by glass frit before the package assembly. The protection of the fragile micro-mechanical structures is achieved by wafer level packaging technique. As for ASIC die, it is used to make logical elaboration of sensor signal.

Similar to single die QFN (see Figure 5.9), the peripheral solder joint has much larger SED than center pad solder. The crack initiates and propagates through the peripheral top solder/pad interface.

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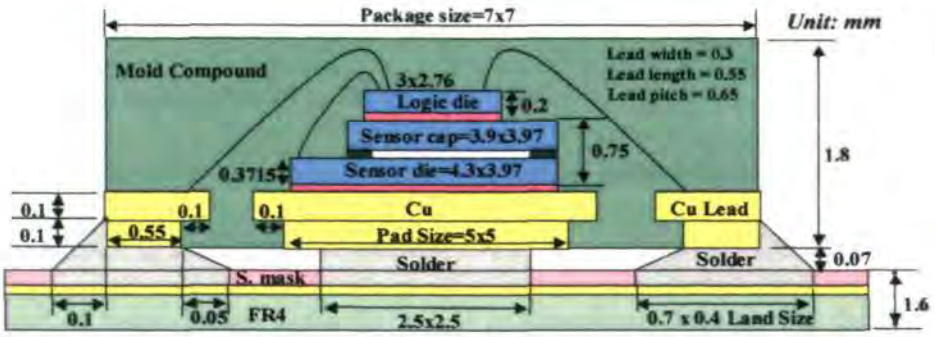

Figure 6.4. Schematic of stacked die TQFN-7x7mm

6.3.3 Design Analysis

The characteristic life predicted for this stacked die TQFN is 1560 cycles with 1.6mm board thickness, under –40°C to 125°C (1 hr/cycle) thermal cycling. The fatigue model is applied for parametric studies of package geometry and material properties, to enhance the board level solder joint reliability. For parametric studies, one design variable is changed at a time with respect to the control case. The geometry dimensions of the control case are given in Figure 6.4.

There are 12 effects studied relative to the control case (printed in **bold font**), and results are tabulated in Tables 6.5-6.8. It is a detailed study on effects of PCB thickness, package thickness, leadframe thickness, lead length, dice size and thickness, solder fillet, center pad solder coverage, solder standoff, modulus and CTE of mold compound.

Effects of Package and Board Geometry

PCB thickness is a critical design consideration. Thinner PCB of 0.8mm has 62% longer fatigue life than PCB with 1.6mm thickness (see Table 6.5). Thinner PCB results in smaller global CTE mismatch between package and board. For stacked die TQFN, it is important to keep the package thickness as thin as possible to enhance the

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fatigue life. It is inevitable that stacked die package has lower fatigue life than single die package, due to increase in package thickness.

As for leadframe, thicker one is better for solder joint reliability, as it increases the mean package CTE, and therefore smaller CTE mismatch with PCB. For package with longer lead, it takes longer time for crack to propagate through the failure interface, therefore the fatigue life is enhanced (according to Eq. (5.2)).

Table 6.5. Effects of package and board geometry

Design Variations		**Life (cycle)**	**% Diff.**
PCB Thickness	0.8 mm	2532	62.3
	1.6 mm	**1560**	-
Package Thickness	**1.8 mm**	**1560**	-
	2.1 mm	1317	-15.6
Leadframe Thickness	**0.2 mm**	**1560**	-
	0.3 mm	3002	92.4
Lead Length	**0.55 mm**	**1560**	-
	0.65 mm	2274	45.7

Effects of Dice Sizes and Thickness

It is desirable to have smaller sensor die size to enhance the fatigue life (see Table 6.6). When die size is reduced, the fatigue life becomes higher due to smaller local CTE mismatch between die edge and the critical solder joint. The effect of logic die size is not significant, as its position is further away from the peripheral solder joint. Thicker sensor and logic dice help to increase the fatigue life. This trend is different from previous experience on single die QFN, which prefers thinner die (see Section 5.4.4).

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Table 6.6. Effects of dice sizes and thickness

Design Variations		Life (cycle)	% Diff.
Die Thickness	Logic = 0.15 mm Sensor = 0.5 mm	1517	-2.8
	Logic = 0.2 mm **Sensor = 0.75 mm**	**1560**	-
Sensor Die Size	Sensor die = 3.9 mm Sensor cap = 3.5 mm	1847	18.4
	Sensor = 4.3 mm **Sensor cap = 3.9 mm**	**1560**	-
Logic Die Size	2.7 mm	1555	-0.3
	3.0 mm	**1560**	-

Effects of Solder Geometry

TQFN with solder fillet has better solder joint reliability than package without solder fillet (see Table 6.7). With the additional solder material, the maximum SED of peripheral solder joint is reduced and redistributed. It is assumed that the adhesion of solder fillet/lead edge is the same as the bottom lead/solder interface. From experiment, the solder fillet/lead interface usually fails first, and then the crack propagates inward along the pad interface.

Additional soldering under the center die pad helps to enhance the fatigue life, because there is more solder material to support the plastic work induced during thermal cycling. Therefore, the SED of critical peripheral solder is reduced. Package with higher solder standoff has longer fatigue life. The larger separation distance of solder helps to reduce the shear strain induced during thermal cycling.

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Table 6.7. Effects of solder geometry

Design Variations		Life (cycle)	% Diff.
Solder Fillet	**With**	**1560**	-
	Without	1432	-8.2
Center Pad Solder Coverage	0 %	1348	-13.6
	50 %	**1560**	-
	75 %	1777	13.9
	100 %	2083	33.5
Solder Standoff	**0.07 mm**	**1560**	-
	0.10 mm	1975	26.6

Effects of Mold Compound Material Properties

For the case studied, mold compound (MC) modulus and CTE are important to solder joint reliability (see Table 6.8). Lower mold compound modulus induces lower stress, and therefore longer fatigue life. Higher mold compound CTE increases average package CTE, resulting in lower CTE mismatch with PCB, and therefore longer fatigue life. For TQFN with fixed package geometry, the fatigue life can be increased easily through proper material selection such as mold compound.

Table 6.8. Effects of mold compound material

Design Variations		Life (cycle)	% Diff.
MC Modulus	17600 MPa (-20%)	1778	13.9
	22000 MPa	**1560**	-
	26400 MPa (+20%)	1406	-9.9
MC CTE	7 ppm/°C	1479	-5.2
	9 ppm/°C	**1560**	-
	11 ppm/°C	1645	5.4

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6.4 C^2BGA THERMALLY ENHANCED PACKAGE

6.4.1 Background

The increasing demand of package miniaturization and better thermal management has prompted the design of thermally enhanced BGAs. They have attractive features of better thermal performance with minimum added cost, and required I/O counts with small footprint, which cannot be achieved with conventional BGA packages. This has increased its usage in power applications, such as hard disk drive, automotive and telecommunication.

With C^2BGA (Conduction Cooled BGA) mounted on a PCB as an example (see Figure 6.5), the primary thermal path is: die ⇒ die attach ⇒ heat slug ⇒ thermal solder joints ⇒ PCB ⇒ ambient. The heat is mainly conducted from the die to the copper heat slug and to the PCB. Due to the high thermal conductivity of the copper heat slug, heat can be dissipated effectively from the package to the ambient. In addition, the thermal resistance due to the substrate along the primary thermal path is eliminated. This offers the lowest junction to board thermal resistance and results in a very low junction-to-ambient thermal resistance, θ_{ja}.

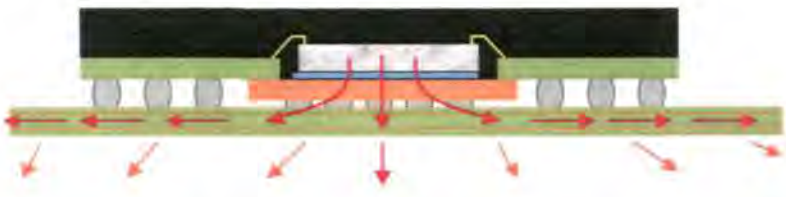

Figure 6.5. Primary thermal path for C^2BGA on a PCB

Figures 6.6 and 6.7 show the schematic of C^2BGA and the conventional TFBGA to be investigated later. Both BGAs have the same package size of 16x16mm, die size of 5x5mm, 0.8mm ball pitch and 240 I/O (same ball layout). The C^2BGA has a cavity with heat slug at the bottom of the package and five thermal solder joints.

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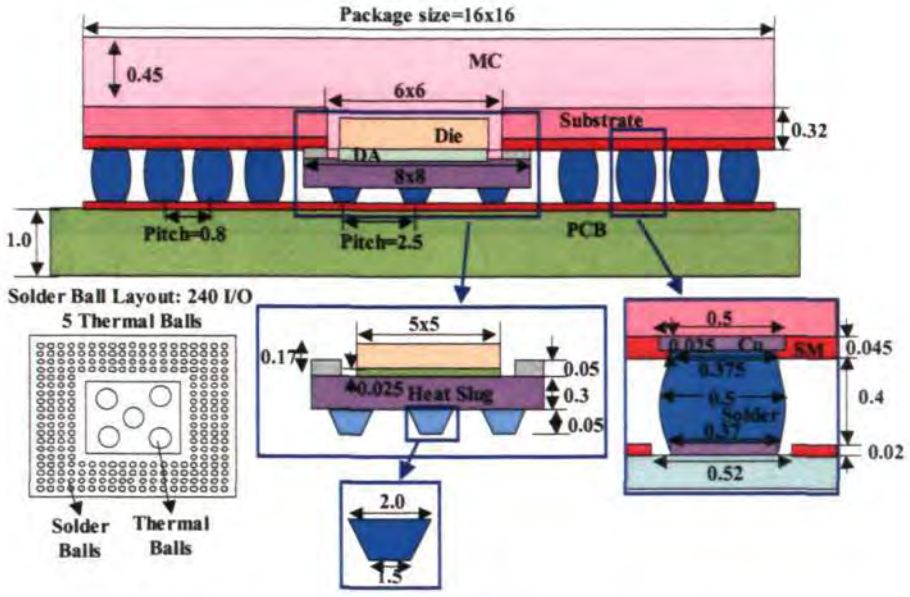

Figure 6.6. Schematic diagram of C^2BGA

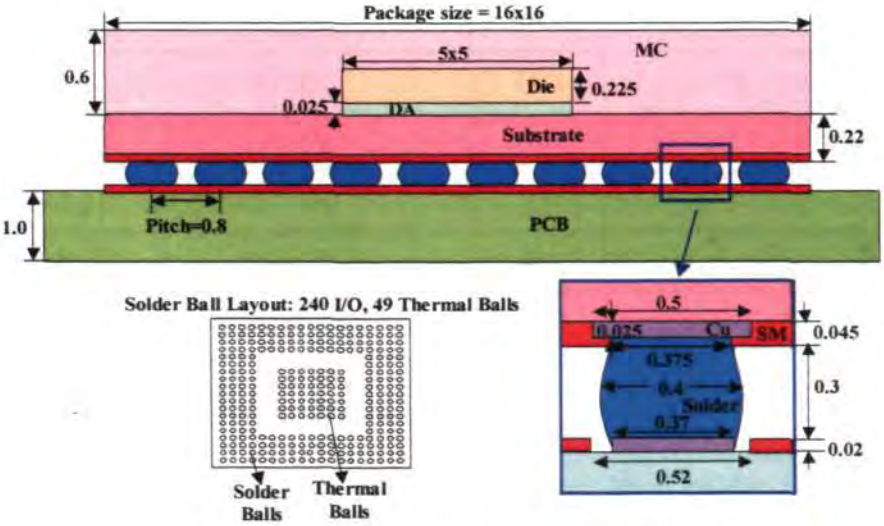

Figure 6.7. Schematic diagram of TFBGA

6.4.2 Solder Joint Fatigue Model

Both global and local 3D FEA models are constructed for C^2BGA and TFBGA, to predict the fatigue life of solder joint during thermal cycling test. The thermo-mechanical properties are listed in Table 6.9.

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Table 6.9. Thermo-mechanical material properties

Materials	CTE_1 / CTE_2 (ppm/°C)	Tg (°C)	Modulus (GPa)
Silicon Die	2.8	-	131
Copper Pad	17	-	117
Eutectic Solder	24	-	31.6
Solder Mask	95	-	5
BT Substrate	xy: 17 (in-plane) z: 55 (out-of-plane)	-	xy: 26 z: 11
PCB	xy: 16 (in-plane) z: 63 (out-of-plane)	-	xy: 25 z: 11
Die Attach A	25 / 75	80	5.1
Die Attach B	29 / 102	80	1.73
Die Attach C	72 / 145	24	0.5
MC-A	11 / 37	160	17
MC-B	8 / 32	165	25
MC-C	9 / 32	150	19
MC-D	12 / 59	160	14.9
Slug Attach A	40 / 140	75	7
Slug Attach B	25 / 75	80	5.1

* Sources: all from material suppliers

6.4.3 Effect of Thermal Solder Joints

The fatigue models are applied to compare board level solder joint reliability of C^2BGA and TFBGA packages. The location of the critical solder ball (see Figure 6.8) for both C^2BGA and TFBGA is at (7,7) position. With the same package size, solder ball layout, and mold compound material, C^2BGA have better fatigue performance than TFBGA (see Table 6.10). This is mainly due to additional enhancement of thermal solder joints below the center of C^2BGA package.

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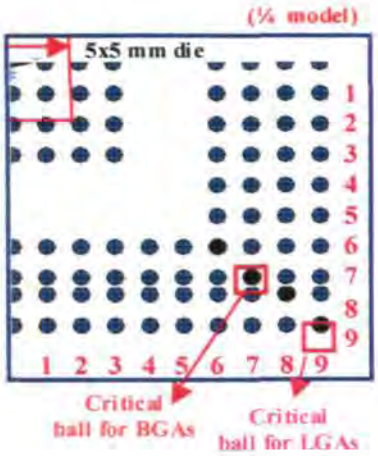

Figure 6.8. Position of critical solder balls and die edge

Table 6.10. Solder joint fatigue lives of C^2BGA and TFBGA

Design Variations	Position / Life (cycles)		Critical Life (cycles)	% Diff.
	(7,7)	(9,9)		
TFBGA	1941	5615	1941	-
C^2BGA	2238	3881	2238	15.3

Thermal solder joints connect the slug to the ground. Since they are not part of daisy-chain connection, thermal cycling test usually is unable to determine their actual reliability. However, it can be easily studied through modeling. The main function of the C^2BGA thermal solder joints is to conduct heat effectively away from the die to the PCB, without having pass through the substrate, and therefore junction-to-ambient thermal resistance, θ_{ja}, can be minimized. Here, the effect of the thermal solder joints on thermal performance and solder joint reliability of C^2BGA is investigated. Table 6.11 shows the schematic thermal solder joints designs and results. The worst case, which has all thermal solder joints removed (C2), the best case, which has all thermal solder joints intact (Control), and in-between case, which has only center thermal solder joints intact (C1), are studied.

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Table 6.11. Effect of thermal solder joint pattern

Cases	*Control*	C1	C2
Thermal Solder Joint Pattern			
θ_{ja} Increase (°C/W)	-	1.6	5
Critical Solder Ball Life (cycles)	**2238**	2243	1863
Thermal Solder Joint Life (cycles)	**35824**	34379	-

Reduction in number of thermal solder joints tends to increase the thermal resistance. For consistent thermal performance, the integrity of thermal solder joints is important. The fatigue life of the thermal solder joint is 35824 cycles, which is much longer than fatigue life of the critical solder ball. This is proven by failure analysis, which shows that thermal solder joints are still intact for C^2BGA sample after 2000 cycles of thermal cycling test.

The existence of thermal solder joints also enhances the reliability of critical solder ball. If there is no thermal solder joint at all, fatigue life of critical solder ball is reduced, and thermal resistance is increased. However, the number of thermal solder joints existing does not have significant impact on the fatigue life of critical solder ball.

6.4.4 Correlation of Fatigue Life and Package Warpage

The relationship between solder joint fatigue life and package warpage during thermal cycling can be established. For correlation, six design variations for TFBGA and 10 design variations for C^2BGA are studied for 16x16mm package size. The six design variations for correlation for TFBGA include die size, two die attach materials, and three mold compound materials. As for C^2BGA, it includes die size, mold compound and die thickness, substrate thickness, solder ball diameter and height, two

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die attach materials, three mold compound materials, and slug attach material. The focus of this section is not on design analysis, and therefore detailed results of each case are not provided. Package warpage change from –40°C to 125°C is calculated.

There is a general correlation between fatigue life and package warpage for both C^2BGA and TFBGA (see Figures 6.9 and 6.10). The correlation can be described by power law equations. It is shown that lower package warpage leads to higher fatigue life. This is because both parameters are sensitive to CTE mismatch during thermal cycling. Lower package warpage results in a smaller displacement change along the critical solder interface, and smaller shear strain is induced. This in turn enables longer fatigue life to be achieved. Therefore, it is possible to apply a simpler package warpage model for quick estimation of solder joint reliability performance.

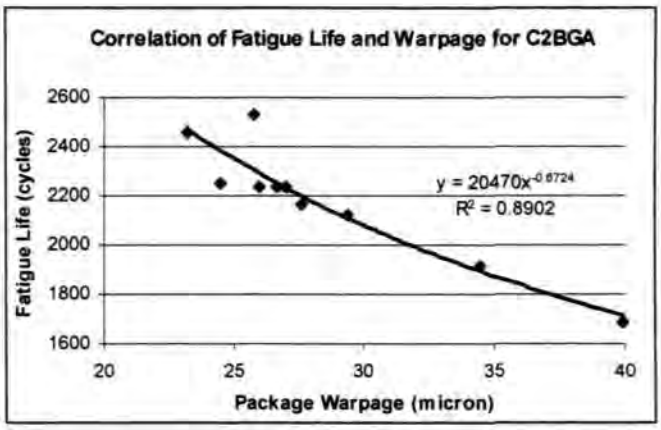

Figure 6.9. Correlation of warpage and fatigue life for C^2BGA

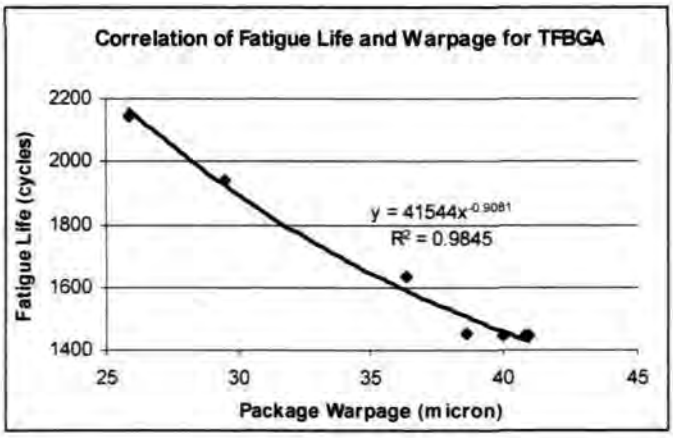

Figure 6.10. Correlation of warpage and fatigue life for TFBGA

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There is no need to apply a complex warpage model with consideration of process residue stress, as the difference in results will be adjusted during the numerical correlation with fatigue life.

6.5 SUMMARY

Fatigue modeling using modified Darveaux method is applied on design analysis of various advanced CSPs with stacking dice, lead-free solder, MEMS, and power applications. Detailed solder joint fatigue model with life prediction capability is established for lead-free stacked die with mixed flip-chip and wirebond BGA. The critical solder ball of stacked die BGA studied is between the top and bottom dice, and the failure interface is along the top solder/pad interface. Comprehensive design analyses are performed to study effects of package geometry and material properties. Generally, for enhanced solder joint reliability of stacked die BGA, it is recommended to have larger top or bottom dice sizes, and thicker top die. Lead-free solder with lower CTE is desired. SnAgCu solder has more than two times longer life than eutectic solder. Large and even length of stacked die are preferred to redistribute the SED more uniformly among the solder balls, instead of concentrating at one critical solder ball.

Certain design rules learned from single die BGA may not be applicable for stacked die BGA. The position of critical solder ball is a variable, so the common practice of using dummy balls for outermost corner position may not improve the fatigue life. Effects of design variables are case-dependent, so fatigue modeling is efficient to assess the solder joint reliability of new package design, with saving in cost, time, and manpower in performing the actual thermal cycling tests.

As for MEMS package, stacked die TQFN, the failure interface of peripheral solder joint is along the top solder/pad interface. Generally, for enhanced solder joint reliability of stacked die TQFN, it is recommended to have thinner PCB, thinner

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package, thicker leadframe, longer lead, smaller sensor die size, solder fillet, more center pad solder coverage, higher solder standoff, and mold compound with lower modulus and higher CTE.

Design comparison between thermally enhanced C2BGA and conventional TFBGA is studied. C^2BGA has better solder joint performance compared to conventional TFBGA. Integrity of C^2BGA thermal solder joints is excellent. Thermal solder joints help to reduce the thermal resistance and enhance the solder joint reliability at the same time. There is a good correlation between solder joint fatigue life and package warpage for both TFBGA and C^2BGA. Smaller package warpage leads to longer fatigue life.

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CHAPTER 7 BOARD LEVEL DROP IMPACT MODELING

7.1 INTRODUCTION

The reliability performance of IC packages during drop impact has become a great concern, due to increasing demand and popularity of handheld or portable telecommunication devices such as mobile phones and PDAs. The mechanical shock resulted from mishandling during transportation or customer usage may cause solder joint failure of IC package, which leads to malfunction of product. Therefore, it is important to design a more robust package and board with better reliability performance during the drop impact. Normally, mobile phones are designed to withstand a few accidental drops to floor from a height of 1.5m, without causing major mechanical or functional failures.

Product level drop test is complicated because it depends on many factors such as drop height, drop orientation, components layout on PCB, and product design. Board level drop test is convenient to characterize the solder joint performance, because it is more controllable than product level drop test. A few JEDEC test standards [134-136] provide guidelines to conduct board level drop test.

Traditionally, board level reliability usually refers to solder joint fatigue strength during the thermal cycling test. There are many researchers who have applied viscoplastic modeling to give accurate fatigue life prediction. However, there are few publications [113-114] related to drop test and simulation of its solder joint reliability, although drop test should be as important as thermal cycling test, especially for telecommunication industry. Researchers are beginning to pay more attention to drop test studies and analyses, due to high industrial demand to understand the failure

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mechanism. Most of the limited research work is either purely numerical or experimental, with very little study on correlation between simulation and testing. This is partly because dynamic simulation and drop testing are highly specialized, expertise and capabilities in both areas are required.

Dynamic responses, such as input acceleration, output acceleration, deflection, velocity, and strains, are very important to monitor the repeatability of drop test and investigate the failure mode and failure mechanism of solder joints. It is known that the dynamic strains and stresses of solder joints directly affect the solder joint reliability during drop impact. However, there is no suitable sensor to measure them directly. Alternatively, the dynamic responses of PCB are good measurable indicators which are closely related to solder joint strains and stresses. Some research work was done on dynamic responses at board level [114] and product level [110] drop test. However, currently there is no comprehensive study on dynamic responses of PCB and its corresponding solder joint reliability by both experiments and modeling. This issue will be addressed here. The dynamic responses of PCB under drop impact loading is studied using dynamic model, and excellent correlation has been achieved. This method is extended to investigate the solder joint reliability, solder joint failure mode, and root cause of solder joint failure which are closely related to dynamic responses of PCB.

There has been a lack of life prediction model in the area of research on board level drop test, and it will be addressed for the first time in this thesis. Due to uncertainty in drop test and lack of accurate drop test model, it has been a great challenge to apply modeling for quantitative evaluation of impact life, i.e. to estimate number of drops to failure. Modeling is usually applied to compare the relative drop test performance of various package designs. Variations in package and board geometry (e.g. package size, board size, solder ball size), materials (mechanical properties), and test conditions (drop

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height, orientation, impact duration) may be studied conveniently with drop test modeling. Modeling is more efficient than performing actual drop test, which is expensive, time-consuming, and requires a lot of manpower in measurement and failure analysis. Validated drop test model can be a useful design analysis tool for the competitive telecommunication industry, which emphasizes on short time-to-market. For some mobile phone manufacturers, they have to introduce new product models to the market every few months. Time is limited for them to conduct detailed reliability tests at board and product levels.

7.2 EXPERIMENTAL SETUP OF DROP TESTING

JEDEC (Solid State Technology Association) has developed a standard test procedures and board design for board level drop test of components used in handheld electronic products [134]. The current test standards [135-136] for mechanical shock of component and subassembly are not detailed enough, insufficient for direct comparison of board level drop test performance among various packages, produced by different manufacturers. In addition, the 1500G and 2900G input peak accelerations suggested by JEDEC may not be sufficient for certain packages to induce enough solder joint failures within 50 drops in the critical orientation, i.e. component face-down. This test standard is more useful for product qualification, rather than to understand the actual impact strength and weakness of IC packages at board level, which usually requires much higher peak acceleration. At the moment, the researchers have mostly used their own test boards and test procedures, and the data is only useful for in-house package comparison, due to lack of a comprehensive drop test standard.

Typical setup of board level drop tester is shown in Figure 7.1. The packages (2x5 matrix) are mounted on test board, which is connected to fixture (140x76.2x15mm) and

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solid aluminum drop block (210.5x210.5x70mm) with screws. Between board and fixture, 10mm spacer is added to allow PCB bending. The block is dropped from a height of 1.5m along the two guiding rods, onto a rigid surface covered with a layer of felt (5mm thickness). The board is tested until all components have failed, or up to the maximum of 50 drops. If necessary, the test can be extended to 100 drops, but the resistance measurement interval can be larger. Drop test level [135] is classified by the input acceleration or impact pulse (peak acceleration and pulse duration), and usually is a function of drop height, friction of guiding rods, strike surface, and felt materials.

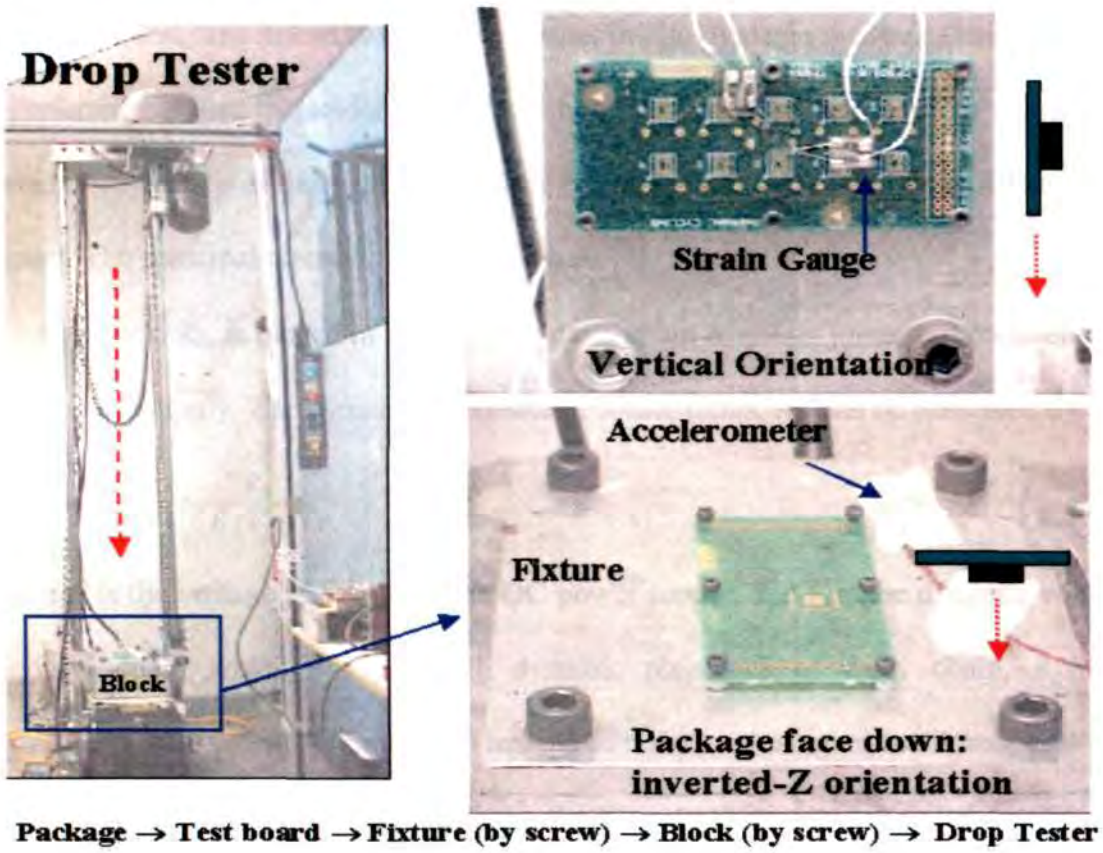

Figure 7.1. Setup of board level drop tester

During drop test, the dynamic responses of PCB and solder joints are crucial because they reflect the PCB behaviors which are closely related to solder joint failure during drop impact. A multi-channel real-time electrical monitoring system is setup to record

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down the input acceleration of PCB, in-plane strains at PCB center, and dynamic resistance of solder joints. The repeatability of the drop tester is excellent with acceleration and strains measurements within ±3%.

Two strain gauges connected to strainmeters, are mounted at the center of PCB (non-component side) to measure the dynamic strains induced in PCB length and width directions. The signals from strainmeters are linked to an oscilloscope. One accelerometer is mounted near to a corner PCB mounting screw to measure the impact pulse (input acceleration to PCB). The acceleration signal is processed by signal conditioner and then linked to the oscilloscope. In-situ dynamic resistance measurement is preferred because the solder joint crack induced by impact may close up again. The dynamic resistance of daisy-chained solder joints is measured in real-time during drop impact. The principal circuit is shown in Figure 7.2.

A resistor, R_o, is placed in series to the daisy chain of solder joints and connected to a DC power supply. The dynamic resistance of solder joints, R_x, can be described by

$$R_x = \frac{R_o V}{E - V} = \frac{R_o}{E/V - 1} \tag{7.1}$$

where E is the voltage (1.8 volt) of the DC power supply, and V is the dynamic voltage of daisy chain which changes with dynamic resistance of daisy chain, R_x. For convenience, the voltage is monitored instead of resistance using an oscilloscope. When $V \to E$, $R_x \to \infty$ (open circuit), indicating the critical solder joint has failed.

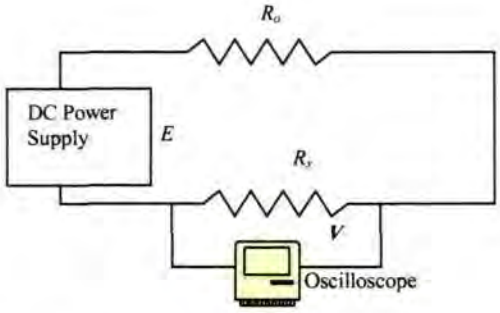

Figure 7.2. Dynamic resistance monitoring system

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7.3 EXPERIMENTAL ANALYSIS OF SOLDER JOINT RELIABILITY

7.3.1 Dynamic Resistance

The dynamic resistance of daisy-chained solder joints which reflects the solder joint reliability is monitored as well as the corresponding impact pulse and dynamic strains. The package is located at PCB center. The dynamic strains are also measured at PCB center on reverse side. Figure 7.3 shows typical dynamic resistance and strains after certain number of drops during drop impact, where positive peak of dynamic strain in PCB length direction implies PCB bending up and negative peak means PCB bending down. Peak value of dynamic resistance indicates that the solder joint crack opens, and the minimum value means that the solder joint crack closes up.

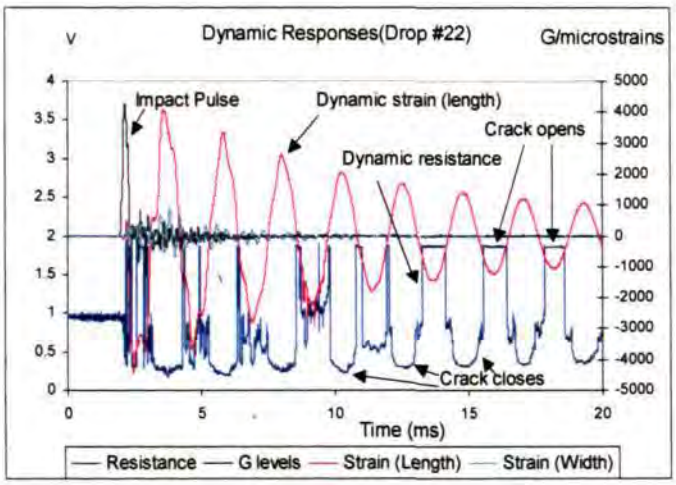

Figure 7.3. Typical dynamic responses

Coincidence of cyclic change of dynamic resistance and dynamic strains indicates that the solder joint crack opens and closes when PCB bends down and up. Figure 7.4 shows the PCB bending downwards and upwards after the impact. Due to the bending stiffness difference between PCB and TFBGA package, the outermost corner solder joints are under tensile normal stress when PCB bends downwards, causing the crack to open. On the other hand, when PCB bends upwards, they are under compressive stress,

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and the crack is closed. It proves experimentally that the solder joint reliability is closely related to the dynamic responses of PCB, and cyclic PCB bending or vibration is the major root cause of solder joint failure during drop impact.

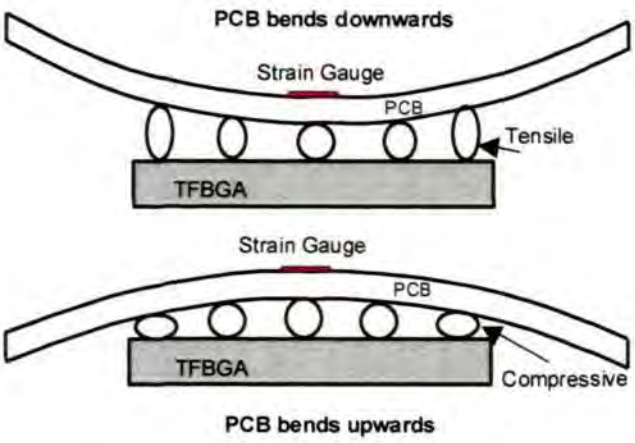

Figure 7.4. Effect of PCB bending direction

7.3.2 Solder Joint Failure Process

From the evolution of the dynamic resistance, the solder joint failure process can be divided into three main stages (see Figure 7.5), i.e. crack initiation (stage 1), crack propagation (stage 2), and crack opening (stage 3). In stage 1, both static and dynamic resistances increase gradually with number of drops. It implies that an initial crack is initiated, and the cross-sectional area of the critical solder joint is reduced gradually. In stage 2, there are a few peaks start to appear in dynamic resistance curve, as the crack is propagated, the cross-sectional area of solder joint is reduced, and thus the resistance is increased. The impact life at the first dynamic resistance peak is N_1. In the subsequent drops and PCB bending cycles, the amplitude of dynamic resistance peak increases until an intermittent failure ($R \rightarrow \infty$) occurs at impact life, N_2. At this moment, the crack is just propagated through the entire solder joint interface and there is an electrical discontinuity happened in a very short duration. The crack usually closes back after the

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impact testing, and the resistance is dropped. In stage 3, the process continues, and the duration of dynamic resistance peak increases with number of drops, as the crack opening gap is getting larger. The crack is harder to close up again during PCB bending, and the resistance goes to infinity most of the time. Finally, both the static and dynamic resistance go to infinity permanently at impact life, N_3. This is a permanent solder joint failure.

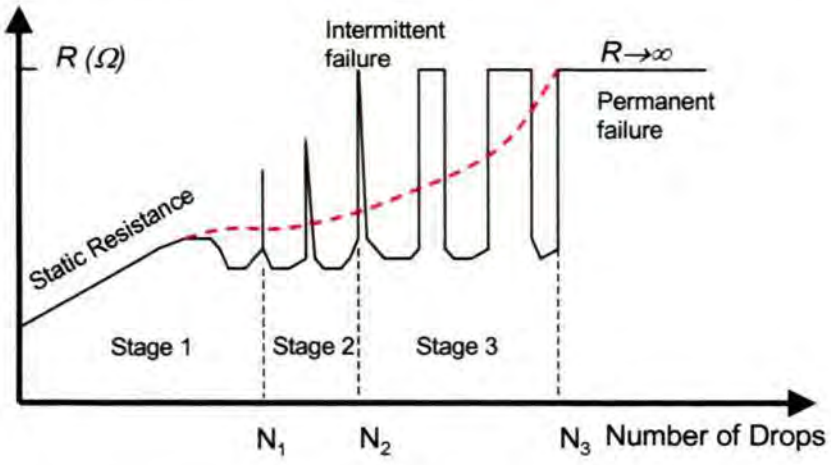

Figure 7.5. Solder joint failure process

Therefore, there should be three different solder joint impact lives, i.e. crack initiation life (N_1), intermittent failure life (N_2), and permanent failure life (N_3), depending on the definition of solder joint failure criteria. The real-time dynamic resistance method is able to record down all the three impact lives and display the three stages of solder joint failure process.

Compared with event detector, this method is much cheaper, easier to setup, and able to measure the actual value of dynamic resistance at real-time, which reflects the in-situ crack initiation and propagation of solder joints during drop impact. Event detector usually sets a threshold resistance (e.g., 300Ω) for failure to occur, and this simple pass/fail criteria is unable to describe the trend of solder joint reliability, and

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provide insufficient details for further analysis. Due to high frequency and short duration of PCB bending, event detector may fail to capture all the continuous intermittent failures because of its long data acquisition period (minimum is 2 seconds/poll) and channel resetting. On the other hand, manual probing can only check the static resistance of solder joints after drop impact. At this moment, the crack may close up again and the resistance measured is lower.

7.4 DROP IMPACT MODEL

It usually takes more than three months (including board design, fabrication, assembly and testing) and involves significant amount of cost to conduct an actual drop test for package qualification or design analysis. Due to pressure of short time-to-market, testing has become a bottleneck for semiconductor and telecommunication industry. Therefore, there is a need for a faster and cheaper solution, i.e. validated drop impact model, which is accurate, reliable, and enables understanding of physics-of-failure for design improvement.

In general, a validated drop impact model can be classified into three levels: 1) good correlation of dynamic responses of PCB (system's structural behavior), 2) good correlation of trend of solder joint stress/strain (qualitative), and 3) good correlation of impact life (quantitative). Due to lack of suitable sensor for measuring stress/strain in solder joint without affecting solder joint performance, correlation in the second level is difficult. Quantitative impact life prediction requires sophisticated material model, and thus, correlation in the third level is very challenging. Therefore, good correlation of drop impact model with dynamic responses is a prerequisite to accurate solder joint reliability analysis and impact life prediction.

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In this study, board level drop test simulation of 0.75mm pitch TFBGA46 (see Figure 7.6) is performed. Quarter 3D model is established to reduce model size due to symmetry (horizontal drop, component faced down). The package size is 6.39x6.37mm, die size is 4.6x3.5x0.235mm, and board size is 100x48x1.6mm with 46 I/O. Detailed package geometry, solder balls, and pad design are included in the model. For simplicity, the 46 solder balls are modeled as full array using a quarter model. The test board is fixed by four screws with one package (facing down) mounted at PCB center. This configuration is good for correlation and model validation because most measurements are performed at PCB center. The pad design is SMD on component side, and NSMD on PCB side. The screws were modeled as simple 3D cylindrical blocks, linking between the PCB and drop block with perfect adhesion assumed.

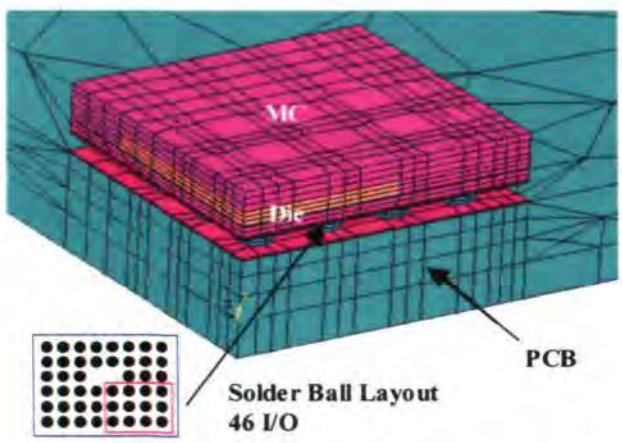

Figure 7.6. Finite element model of TFBGA package on board

ANSYS/LS-DYNA with drop test module is applied for pre/post-processing and solution of dynamic drop test simulation. The explicit solver is conditionally stable, compared with implicit solver which is unconditionally stable, but it is more efficient for drop test solution because usually the impact duration is very short, less than 1ms. The explicit solver usually requires less computational time than implicit solver due to its unique solution algorithm. Dynamic modeling using implicit solver is more

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challenging than explicit solver, especially for impact type of contact modeling. The critical time step, Δt, required for stable solution can be computed by

$$\Delta t = l\sqrt{\frac{\rho}{E}} \tag{7.2}$$

where l is the characteristic length of the smallest element, ρ is the density, and E is the modulus. Normally, a factor of 0.9 is applied to the critical time step to ensure a stable solution. The time step depends strongly on the smallest element size. For board level package model, there is a large variation of element sizes for different materials, the minimum time step usually is in the order of 1E-9s, and the total solution time may take from a few hours to a few days, depending on the complexity of model. Mass-scaling technique can be applied to shorten the solution time, and it will be discussed later.

Figure 7.7 shows the initial and boundary conditions of dynamic model (quarter 3D). To save processing time for solution, usually a near-impact velocity (according to Eq. (2.21)) is applied as an initial condition for object under drop test. For a drop height of 1.5m used in TFBGA drop test, the theoretical impact velocity is 5.425m/s. Gravitational acceleration of 9.81m/s^2 is applied during the free-fall.

The basic material properties required for linear elastic dynamic impact model are modulus, density and Poisson's ratio (see Table 7.1). Dynamics material properties with high strain effect are not considered in the model. For the TFBGA drop test model studied, there are total of 5183 elements and 5483 nodes.

Contact surface is defined between the drop object and the rigid impact surface. A layer of felt (nylon material) is added in between the contact surfaces to generate sinusoidal type of acceleration curve. The felt is modeled as a material layer attached with perfect adhesion to the drop block, and the entire system is dropped freely onto the striking surface. There is only one contact interface modeled.

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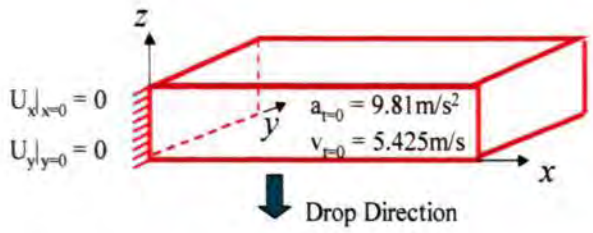

Figure 7.7. Initial and boundary conditions of dynamic model

Table 7.1. Material properties used in model

Materials	Modulus (MPa)	Poisson's Ratio	Density x 10^{-9} (Mg/mm^3)
Die	131000	0.3	2.33
Die Attach	5000	0.3	2.2
Mold Compound	25506	0.3	1.97
Cu Pad	117000	0.3	8.94
PCB	16850	0.11	1.82
Al Block	70000	0.33	2.7
Steel Screw	200000	0.3	7.8
Eutectic Solder	34000	0.363	8.41
Solder Mask	5000	0.3	1.15
Nylon Felt	1600	0.3	1.14

* Sources: all from material suppliers. Modulus of MC and DA are storage modulus.

7.5 INTEGRATED EXPERIMENTAL AND NUMERICAL ANALYSIS

7.5.1 Correlation of Dynamic Responses

The time-dependent input acceleration curve predicted by modeling on the top corner of the drop block is shown in Figure 7.8.

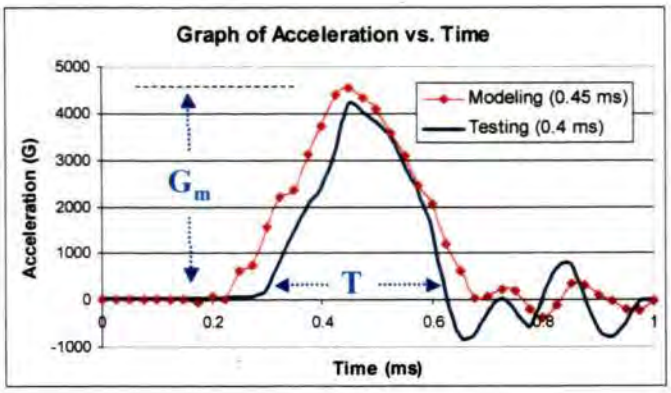

Figure 7.8. Input acceleration curve

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The peak acceleration (G_m) is 4500G (1G = 9.81m/s^2), slightly larger than the typical 4200G measured from experiment. The impact duration (T) predicted by modeling is 0.45ms, also slightly larger than the experimental value of 0.4ms. The difference is mainly due to friction experienced in actual drop test, along the guiding rods.

The area under the acceleration curve, or impact energy, for first positive peak is slightly smaller for experimental measurement. Actual impact velocity measured using high-speed camera is 4780mm/s, lower than the theoretical impact velocity (5425mm/s) predicted by Eq. (2.21) at 1.5m drop height. Since kinetic energy is proportional to square of velocity, the actual impact velocity can be estimated by

$$V_a = V_t \sqrt{\frac{A_a}{A_t}} \tag{7.3}$$

where V_a is actual impact velocity, V_t is theoretical impact velocity, A_a is area under acceleration curve measured by experiment, and A_t is area under acceleration curve predicted by modeling. The actual impact velocity calculated by Eq. (7.3) is 4637mm/s, and it is within the range of impact velocity values measured by high-speed camera (4780±200mm/s).

The reduction of kinetic energy is due to friction generated along the guiding rods during drop test. This effect can be minimized with the application of lubrication, and regular checking of tester's vertical alignment. Nevertheless, this friction effect is acceptable, as long as it is consistent for all the tests done. Friction effect is not considered in the model, but it can be compensated by the correlation constants used in life prediction model (see later Section 7.6).

The first half-sine acceleration curve can be approximated by

$$G(t) = G_m \sin \frac{\pi t}{T} \tag{7.4}$$

where $G(t)$ is the acceleration at time t, G_m is the peak acceleration or maximum shock level, and T is the impact duration. The acceleration curves given by testing and

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modeling are not perfectly sinusoidal (see Figure 7.8), but closer to triangular shape. With the same impact energy or area under the acceleration curve, theoretical sinusoidal curve given by Eq. (7.4) usually predicts lower peak acceleration with the same impact duration, or shorter impact duration when peak acceleration is fixed.

When the potential energy is fully converted into kinetic energy, the peak acceleration, G_m, for perfectly plastic case (no rebound) may be defined as

$$G_m = \frac{\pi\sqrt{gH}}{T\sqrt{2}} \tag{7.5}$$

where g is gravitational acceleration (9.81m/s^2), H is the drop height, and T is the impact duration. For perfectly elastic case (full rebound), G_m is two times larger than values given in Eq. (7.5). The effect of striking surface is not considered in this equation, and it must be determined experimentally. At fixed drop height, the product G_mT is a constant,

$$G_{m1}T_1 = G_{m2}T_2 \tag{7.6}$$

because the impulse remains the same. Usually there is a need to fine-tune the felt thickness, drop height, and impact surface conditions (type of material, shape and flatness), so that desired sinusoidal shape of acceleration curve (G_m and T values) can be achieved. Thicker felt generates lower peak acceleration and longer impact duration, due to decrease in contact stiffness.

The time-dependent dynamic strain in PCB length direction predicted by modeling is shown in Figure 7.9. It correlates very well with the experimental measurement (repeatable). The amplitude of PCB bending or vibration decreases gradually with time with the application of mass damping. The period or frequency of vibration is almost the same for both experiment and modeling. Currently, there is no other publication which has reported the same degree of correlation with experiment. Excellent

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correlation in dynamic responses of PCB is a prerequisite to good correlation of solder joint reliability and impact life.

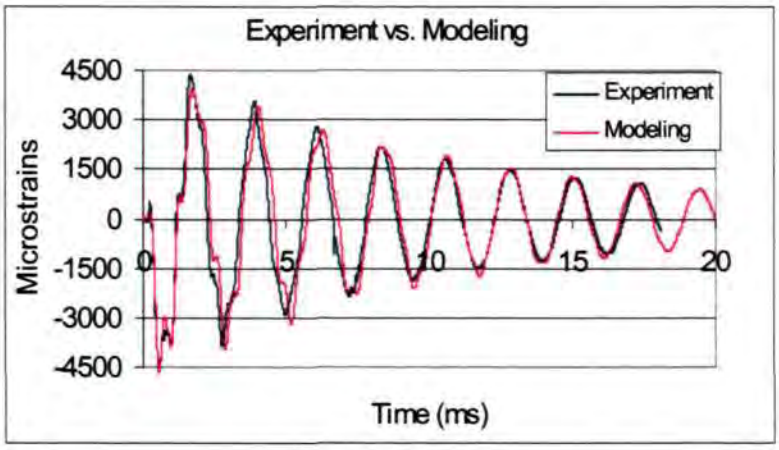

Figure 7.9. Comparison of strain curve (modeling vs. experiment)

7.5.2 Failure Criteria

Minimum requirement of a drop impact model is to have a good relative correlation between modeling and testing, so that the impact performance of other package designs can be evaluated qualitatively, i.e., better or worse. The reliability of solder joints during the drop impact is the main concern, as it affects the functionality of product. Figure 7.10 shows the variation of stresses in the critical solder joint with impact time, including normal stress in PCB length direction (S_x), first principal stress (S_1), vertical normal stress or peeling stress (S_z), shear stress (S_{xz}), and Von Mises stress (S_{eqv}). All the stresses vary cyclically under PCB vibration, corresponding to the measured dynamic strain of PCB. Among them, the peeling stress has close amplitudes in positive and negative directions. It looks like amplitude-declining cyclic fatigue stress. Comparing the five stresses at the same point, the first principal stress follows the same pattern as the peeling stress, especially during the periods of positive peaks, indicating that the peeling stress is the dominant stress component. The Von Mises stress also

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mainly reflects the trend of the peeling stress. The remaining horizontal normal stresses and shear stresses are much lower in magnitude.

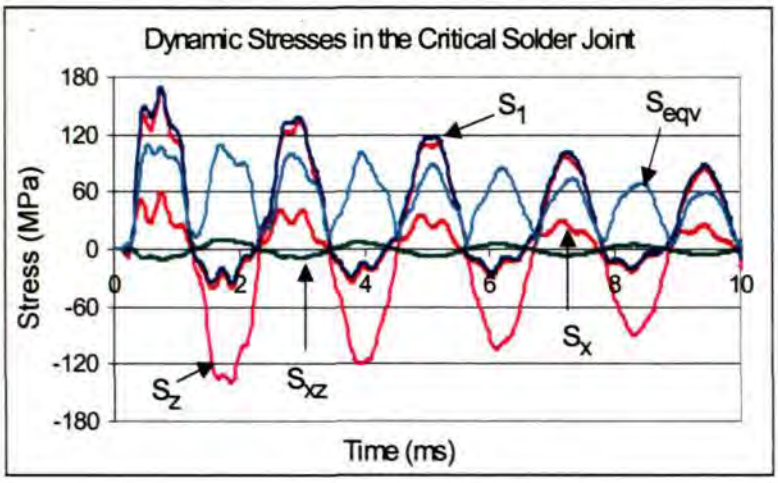

Figure 7.10. Dynamic stresses during drop impact

Therefore, the solder joint peeling stress is critical during drop impact and can be used as a failure criteria for the purpose of design optimization. Since the peeling stress is induced mainly by PCB bending or vibration, it can also be concluded that the PCB bending is the major failure mechanism of PCB subassembly under drop impact, especially for component mounted at PCB center with 4-screw fixation.

Results of input acceleration, dynamic strain in PCB length direction, dynamic resistance, and peeling stress in the critical solder joint are super-imposed and compared in Figure 7.11, where the peeling stress is predicted by modeling and the other three dynamic responses are measured by experiments. Since strain gauge is mounted at the backside (non-component side) of PCB, the negative peak of strain means PCB bending downwards. The peeling stress has a positive peak and the solder joint is subjected to tensile stress when PCB bends downs. It proves the remarks concluded in previous section by pure experiment (see Figure 7.4). At the same time, the dynamic resistance has a positive peak, indicating opening of crack. On the other

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hand, when the dynamic strain is positive and the PCB bends up, the critical solder joint is subjected to compressive stress. At this moment, the solder joint crack closes up and the dynamic resistance is low.

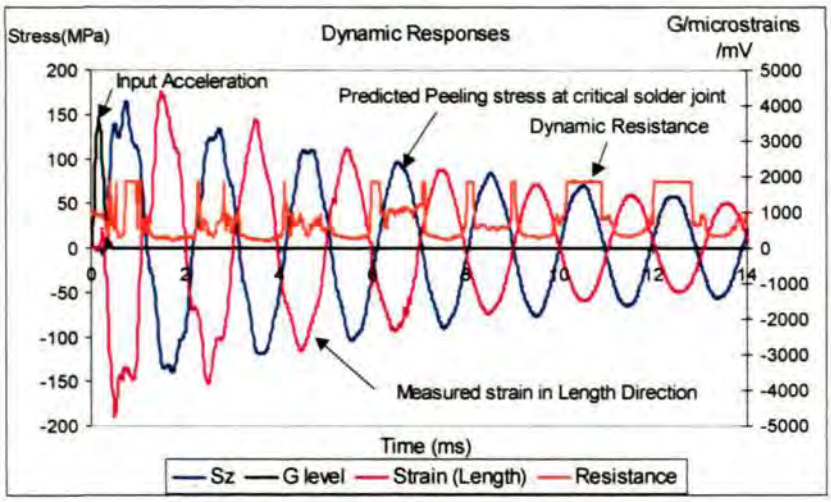

Figure 7.11. Dynamic responses during drop impact

This comparison shows the most important evidence that the peeling stress is the dominant stress component affecting the solder joint reliability. Coincidence of cyclic changes among peeling stress, dynamic strain of PCB, and dynamic resistance of solder joints indicates that the solder joint crack initiation, propagation, and opening are induced by cyclic PCB bending or vibration fatigue.

7.5.3 Failure Analysis

The maximum solder joint stress doesn't occur during the maximum input acceleration at 0.2ms as indicated in Figure 7.8. Instead, the stress level is the highest at 0.74ms, and the critical solder ball is at the outermost corner, with stress concentration along the solder/PCB pad interface (see Figure 7.12, quarter model shown). This is the moment when PCB has the largest warpage and bending stress, induced by the inertia force after impact.

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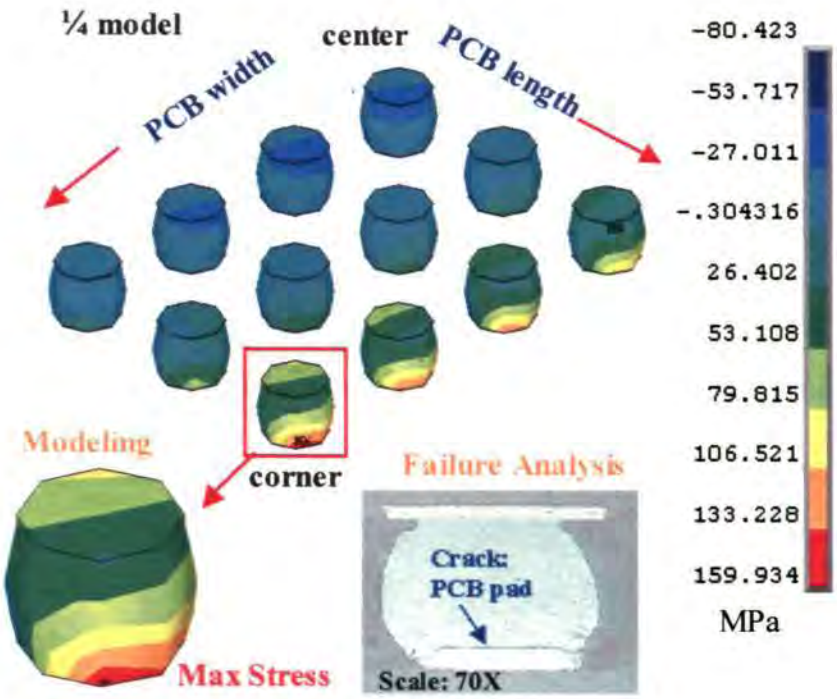

Figure 7.12. Critical solder ball and failure interface

The stress concentration predicted by modeling correlates well with actual failure mode and the critical solder ball location observed in experiment. For the failed TFBGA46 sample, all the solder balls are cross-sectioned row by row, and only the outermost corner solder ball is observed to have failure, a brittle crack in solder intermetallic, along the PCB pad interface. The failure mode is peel-dominant, and this validates the earlier modeling assumption, and supports that the maximum normal peeling stress can be regarded as a failure criteria for the solder joints under drop impact. In addition, the brittle crack also implies that the vibration fatigue is stress-controlled.

The failure location, failure interface, and failure mode can also be verified by dye penetration test. In dye penetration test, red dye is injected into the test sample, which will diffuse into any crack in solder joints. After dye and pry, good solder joints show

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shiny fracture surface while failed solder joints are stained with red ink. A combination of dye penetration test and cross section technique provide a full picture of solder joints failures. Drop testing of another two PCBs mounted with single package is performed for validation till the first failure has just occurred. The failed units are then studied under dye penetration test. Figure 7.13 shows that the critical solder joint is at diagonal corner, along solder/PCB pad interface. The intermetallic failure is confirmed to be a brittle crack.

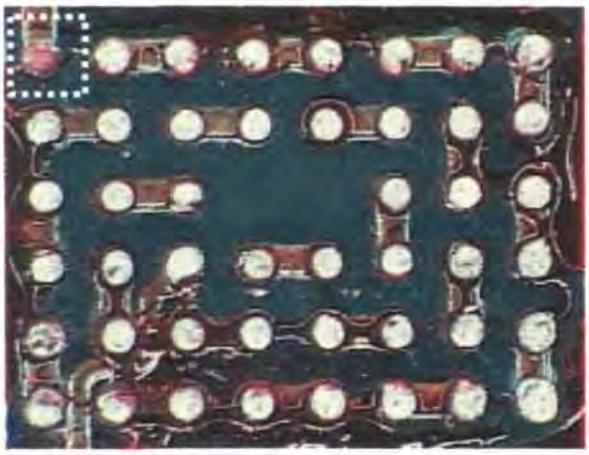

Figure 7.13. Failure location/interface by dye penetration test

The solder ball interfacial failure is induced by a combination of mechanical shock and PCB bending. The bending stress is critical to solder joint reliability. Figure 7.14 shows the warpage distribution of PCB during bending. The PCB has much larger warpage in the length direction (3.35mm) than in the width direction (0.33mm). As a result, the outer row of solder balls in the PCB length direction warps more and has higher bending stress level (see Figure 7.12). Therefore, the DNP (Distance to Neutral Point) effect is an important design consideration for components under drop impact.

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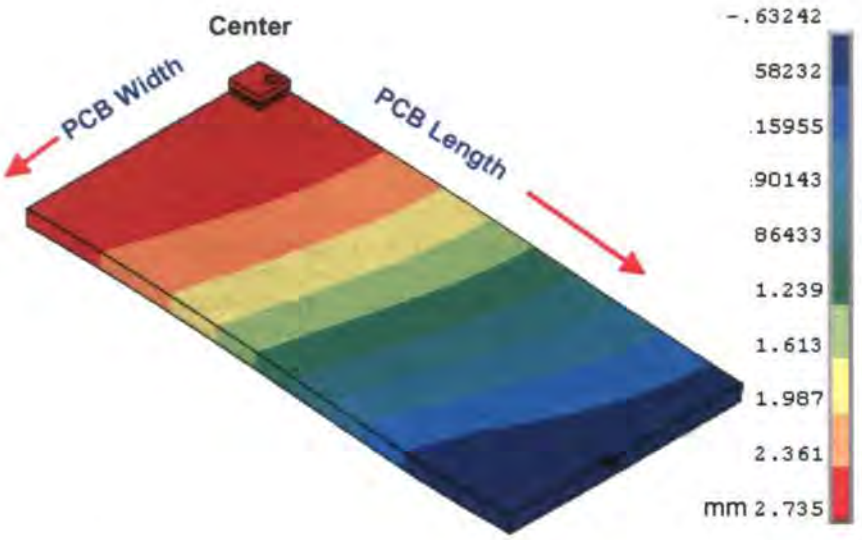

Figure 7.14. PCB warpage distribution at maximum bending

7.6 IMPACT LIFE PREDICTION MODEL

The next step of more in-depth modeling is to evaluate the impact performance quantitatively, using a life prediction model. There should be good correlation between modeling predicted impact lives and actual impact lives measured.

Experimentally (see Table 7.2), there are six different cases of TFBGA46 and VFBGA46 (Very thin-profile Fine-pitch BGA) packages tested with different drop orientation (up/down), with/without PCB bending, numbers of screws (4/6) mounting the board to fixture, and type of solder material (eutectic/SnAgCu). There are 10 packages (2x5 matrix) per board. Cases 5 and 6 have no spacer in between board and fixture, therefore there is no PCB bending. VFBGA46 has the same package size, die size, and ball layout as TFBGA46, except the package profile is lower.

Since Cases 5 and 6 have no failure at all after 50 drops, the results cannot be quantified, therefore only Cases 1-4 are correlated. Cases 5 and 6 will be applied for relative comparison. The experimental impact lives (number of drops to failure) for Cases 1-4 are given in Figure 7.15, and results will be discussed in detail in Section 7.7.

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Table 7.2. Details of correlation cases

Case	Package Type	Component Orientation	Number of Screws	Solder Material
1	TFBGA	Face-down	4 screws	Eutectic
2	TFBGA	Face-down	*6 screws*	Eutectic
3	TFBGA	Face-down	4 screws	*SnAgCu*
4	*VFBGA*	*Face-up*	4 screws	Eutectic
5	TFBGA	Face-up *(no bending)*	6 screws	Eutectic
6	*VFBGA*	Face-up *(no bending)*	6 screws	Eutectic

The percentage of failure (out of 10 components on board) and impact life shown in Figure 7.15, can be related by

$$F_r = \beta \ln(N) + \alpha \tag{7.7}$$

where N is impact life at corresponding failure rate (F_r, %), β is the slope (rate of change), and α is a constant. These experimental results are given in Table 7.3. Higher impact life means the package has stronger impact performance, and is able to sustain more number of drops before failure. For larger slope (β), the rate of failure is faster, once the failure is initiated. Failure-free life (N_f) is the number of drops without any failure. It is an important design consideration as it provides a safety zone for the product. Eq. (7.7) may be rewritten, by setting $F = 0$ for failure-free life:

$$N_f = e^{-\frac{\alpha}{\beta}} \tag{7.8}$$

For Case 3, since 80% failure occurs after 1 drop, both mean and failure-free impact lives are less than 1 drop (no physical meaning), so they are rounded up to 1 drop. The slope is assumed to be an average experimental slope of 40.3.

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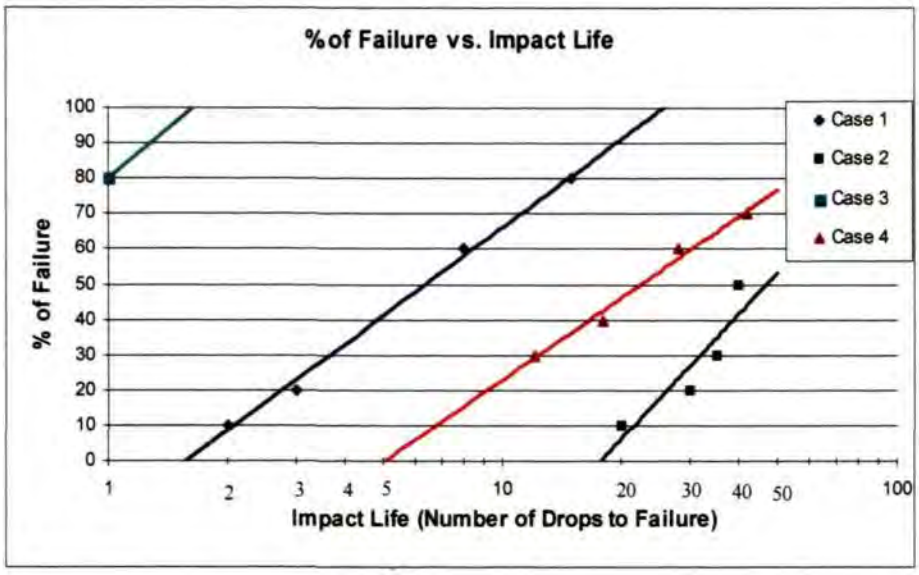

Figure 7.15. Experimental results of impact life

From the previous dynamic model established, the maximum peeling stress of critical solder can be calculated (see Table 7.3). Figure 7.16 shows that the relative stress results match very well with the actual impact life measured. A life prediction model is formulated using power law to relate the maximum peeling stress and mean impact life

$$N_{50} = C_1 \sigma_z^{C_2} \tag{7.9}$$

where N_{50} is the mean impact life (number of drops to failure at 50% failure rate), σ_z is the maximum peeling stress (MPa) in the critical solder ball, C_1 and C_2 are the correlation constants, 1.061E7 and –3.078 respectively. There is good correlation between mean impact lives predicted by modeling and measured by experiment (see Figure 7.17). The uncertainty of impact life prediction is within ±4 drops, for a typical test of 50 drops.

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Table 7.3. Results of modeling-testing correlation

Case	Solder Stress (MPa)	Mean Impact Life N_{50} (# Drops)		Failure-free Life, N_f (# Drops)		Slope (β)
1	141.20	6		2		35.94
2	53.64	47		18		51.57
3	152.50	1		1		40.30
4	73.20	22		5		33.41
5	28.82	>50	(341)	>50	(99)	-
6	29.60	>50	(314)	>50	(91)	-

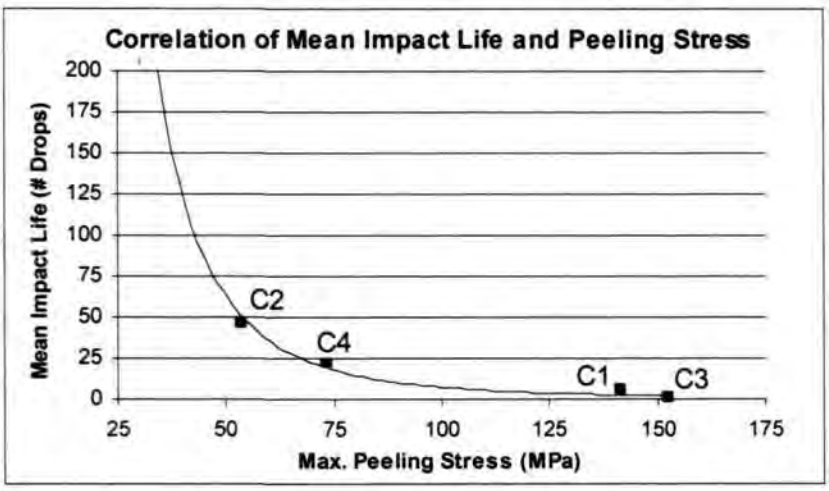

Figure 7.16. Experimental impact life vs. peeling stress

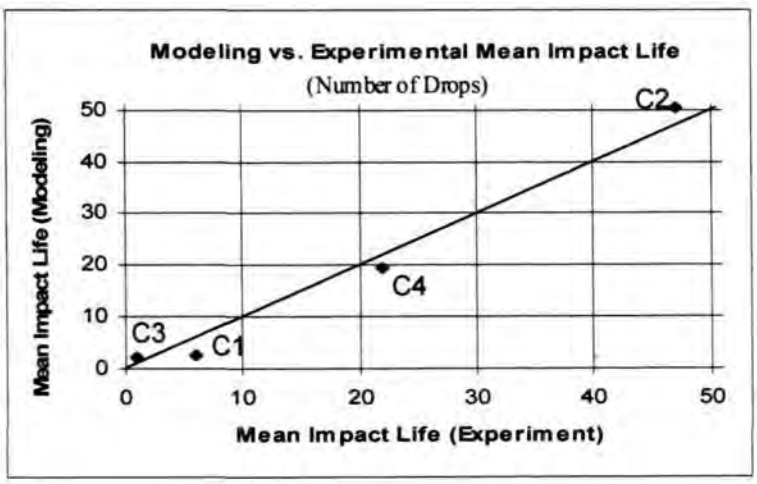

Figure 7.17. Impact life of modeling vs. experiment

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Figure 7.16 shows that impact life increases steeply when the solder peeling stress is low. When the peeling stress is less than about 50MPa, the mean impact life is higher than 50 drops. With this new model, a failure-free state can be determined, and drop test performance of new package design can be quantified, and further enhanced through modeling. This quantitative approach is different from traditional qualitative modeling, as it provides both accurate relative and absolute impact life prediction.

Similar to most finite element models, the value of peeling stress obtained from dynamic model depends on the element size, and other modeling assumptions (material model and contact condition). The drop test measurements also depend on type of tester, failure criteria, and other testing variables. Therefore, the correlation constants used for impact life prediction are model and tester dependent. This is similar to board level thermal cycling test, there are no universal correlation constants. However, even if different models and testers are used by other researchers, the relative comparison of impact performance should still be valid, and this may be sufficient for design analysis of new packages. For absolute impact life prediction, both modeling and testing require detailed considerations, as mentioned throughout this chapter.

7.7 DESIGN ANALYSIS

7.7.1 Integrated Experimental and Numerical Analysis

The drop test results are given in Figure 7.15 and Table 7.3, and several effects can be studied. The testing results are analyzed and compared with modeling, to gain a more in-depth understanding on physics of these dynamic failures. The control case used for design comparison is Case 1 (see Table 7.2), TFBGA46 tested in component face-down direction with four PCB mounting screws and eutectic solder.

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Effect of Component Position

A more detailed model is constructed with one package on center of board and four packages on corner of board to study the relative solder joint stress level between center and component. For Case 1 (4 screws), compared with center component, the maximum solder peeling stress level of corner component is about five times lower. As for Case 2 (6 screws), stress at corner component is about half of center component. These two results show that center component has much higher stress level than corner component, especially for the case with four PCB mounting screws, due to more PCB bending. Therefore, components positioned at board center are more susceptible to failure than corner components for Case 1.

The modeling results correlate well with experimental observations. Figure 7.18 shows that for Case 1, there are six failures out of total of 10 packages (number of drops to failure is printed on top of package). The center packages fail first after five drops, and the four corner packages have no failure at all after 50 drops. For Case 4 (component face-up, 4 screws), the trend is similar (see Figure 7.19), and corner components have stronger impact performance. As for Case 2 (component face-down, 6 screws), there is no clear trend of position effect, failures occur randomly as the PCB warpage distribution is more complicated.

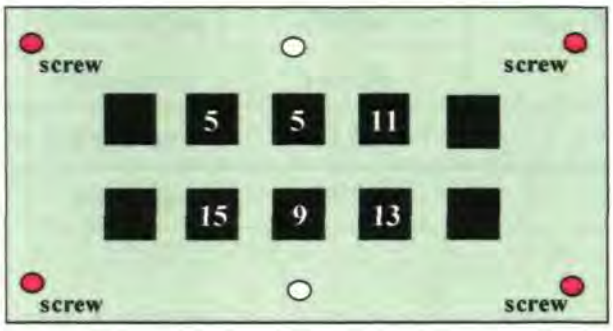

Figure 7.18. Impact life vs. position (Case 1, face-down)

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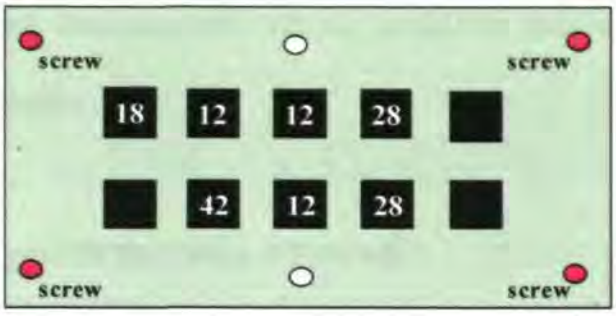

Figure 7.19. Impact life vs. position (Case 4, face-up)

Effects of Drop Orientation

Case 4 is tested with component face-up, but the package type is VFBGA46, therefore cannot be compared directly with Case 1 (TFBGA46, component face-up) on effect of drop orientation. Intermediate result (Case 7) is calculated by modeling for TFBGA46 with component face-up, so that the effect of drop orientation can be compared with the same package type, and impact life of TFBGA can be compared with VFBGA (see Table 7.4). Comparing Case 1 and Case 7 with the same TFBGA46 package, component tested in face-down direction is found to be more severe than in face-up direction.

Table 7.4. Results of drop orientation and package type effects

Case	Package Type	Drop Orientation	Solder Stress (MPa)	Mean Impact Life, N_{50} (# Drops)
1	TFBGA	Face-down	141.20	6
7	TFBGA	Face-up	63.65	30
4	VFBGA	Face-up	73.20	22

PCB is allowed to bend for both drop orientations. When component is in face-down orientation, the solder joints experience additional package inertia force, besides the critical PCB bending stress. Therefore, the recommended test of 50 drops in

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component face-down direction with 4200G, is able to induce enough solder joint failures for most packages.

Effect of Package Type: TFBGA46 vs. VFBGA46

VFBGA46 is a lower-profile version of TFBGA46, with lower solder standoff (0.25mm vs. 0.3mm), thinner mold compound (0.45mm vs. 0.6mm), and thinner die (0.17mm vs. 0.235mm). Comparing results of Case 4 and Case 7 (see Table 7.4) with the same drop orientation, TFBGA46 has slightly better impact performance than VFBGA46. From previous in-house board level thermal cycling test, both packages also have very close solder joint fatigue lives. The board level reliability tests (impact and thermal cycling) performance of TFBGA and VFBGA packages are close, as there is little difference in package structure and geometry dimensions.

Effect of Number of Screws Mounted on PCB

Comparing Case 1 and Case 2 (see Tables 7.2 and 7.3), PCB mounted with four corner screws has lower impact life than PCB with six screws (additional two screws at center of PCB edge in length direction, see Figure 7.18), due to larger PCB warpage. PCB bending stress can be reduced with more number of screws mounting the PCB to the fixture.

Effect of PCB Bending

The PCB in Cases 5 and 6 (component face-up) is not allowed to bend, as the PCB is mounted closely to the fixture with 6 screws without any spacer. Compared to other cases with PCB bending (e.g. Cases 1, 2 and 4), Cases 5 and 6 have much lower solder peeling stress (see Table 7.3) and therefore much longer impact lives.

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For Cases 5 and 6, the modeling predicted mean and failure-free impact lives are more than 90 drops (see Table 7.3). This life prediction explains why in the actual testing, there is no failure at all within the first 50 drops for these two cases. This is additional proof on the accuracy of life prediction model established.

Therefore, in board level drop test, PCB should be allowed to bend to induce higher peeling stress in the solder joint. Mechanical shock without PCB bending is not able to evaluate the true impact performance of the package. However, in the design of actual products (e.g. mobile phone), PCB bending should be minimized. This may be achieved by mounting the PCB to a thicker metal layer without any gap in between, or more screws may be used to mount the PCB to fixture.

Effect of Solder Material

Comparing Case 1 and Case 3 (see Tables 7.2 and 7.3), TFBGA46 with lead-free (SnAgCu) solder is found to have weaker impact life than conventional package with eutectic solder. SnAgCu has larger modulus, therefore the peeling stress induced in solder material is higher, for a given strain level. The trend of drop test results is different from the board level thermal cycling results (see Section 6.2) which show that TFBGA46 with SnAgCu solder has more than two times longer fatigue life than the same package with eutectic solder. The results are consistent with another experimental findings [137] that SnPb solder performs better than SnAgCu solder.

7.7.2 Extended Simulations Analysis

The validated dynamic model can be applied to study other effects, to save the time, manpower, and cost in performing the actual drop tests. The focus of this chapter is on the effects of testing and modeling variables. Peak acceleration, mean and failure-free

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impact lives computed in this section are based on modeling. The control case used for comparison is similar to the settings of previous Case 1, i.e. TFBGA46, component face-down, 4 screws, 1.5m drop height, and 100x48mm PCB size. The design variables studied are varied one at a time with respect to the control case.

Effect of Drop Height

Table 7.5 shows that higher drop height results in stronger peak acceleration. This effect is also stated in the Eq. (7.5). By varying the drop height from 1.5m to 0.5m, the mean impact life can be extended by 16 drops.

Table 7.5. Simulation results of drop height effect

Height (m)	**Peak Acc. (G)**	**Solder Stress (MPa)**	**Mean Impact Life N_{50} (# Drops)**	**Failure-free Impact Life, N_f (# Drops)**
0.5	2038	73.54	19	5
1.0	3516	112.5	5	1
1.5	4532	141.2	3	1
0.36	**1500**	57.26	42	12
0.80	**2900**	95.01	9	3

Another application of this life prediction model is quick evaluation of impact life of package under standard test conditions (e.g. 1500G and 2900G recommended by JEDEC). The desired acceleration level may be achieved by varying the drop height, using a simple dynamic model with only the drop block, and solution can be ready within a few minutes. The equivalent drop height values (0.36m and 0.80m) computed by modeling, are close to experimental measurements of 0.32m and 0.77m, for 1500G and 2900G respectively (see Table 7.5). For the most stringent JEDEC standard of 2900G, the mean impact life of TFBGA46 is predicted to be 9 drops, tested in

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component face-down direction (JEDEC's actual requirement is more relaxed, tested in different x, y, and z directions). The life prediction model can help to reduce the DOE matrix required for drop test qualification.

Effects of PCB Size and Shape

In Figure 7.12, it was shown that solder joints in the PCB length direction have higher peeling stress, especially along the outer row. When the PCB alignment is rotated by 90 degree (orientation of package and solder balls remain unchanged), the maximum solder stress is again shifted to the outer row of solder balls in the new PCB length direction. In this direction, there are four solder balls (compared to the previous case with three solder balls, see Figures 7.6 and 7.12), the DNP (Distance-to-Neutral-Point) is larger, therefore the solder stress is larger, and mean impact life is shorter (see Table 7.6). Comparing square PCB to rectangular PCB, larger square PCB has higher warpage, and therefore larger solder stress. Similarly for square PCB with different sizes, smaller PCB size induces less bending stress, and therefore better impact performance.

Table 7.6. Results of PCB size and shape effects

PCB Size/Shape (mm)	**Solder Stress (MPa)**	**Mean Impact Life N_{50} (# Drops)**
100x48	141.20	3
48x100 (90° rotation)	192.8	1
48x48	99.85	7
100x100	197.6	1

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Effect of Flatness of Contact Surface

The mode of impact between two surfaces is critical. It is interesting to note that flatness of contact surface has significant effect on peak acceleration and impact duration (see Table 7.7). This effect can be studied by modeling with impact of a block onto a slightly curved surface, e.g. top of a big sphere (see Figure 7.20).

Table 7.7. Results of contact surface flatness effect

Sphere Radius (mm)	Flatness (mm)	Peak Acc. (G)	Solder Stress (MPa)	Mean Impact Life N_{50} (# Drops)
5000	2.22	4532	141.2	3
10000	1.11	5514	148.6	2
∞ (flat)	0	7649	168.2	1

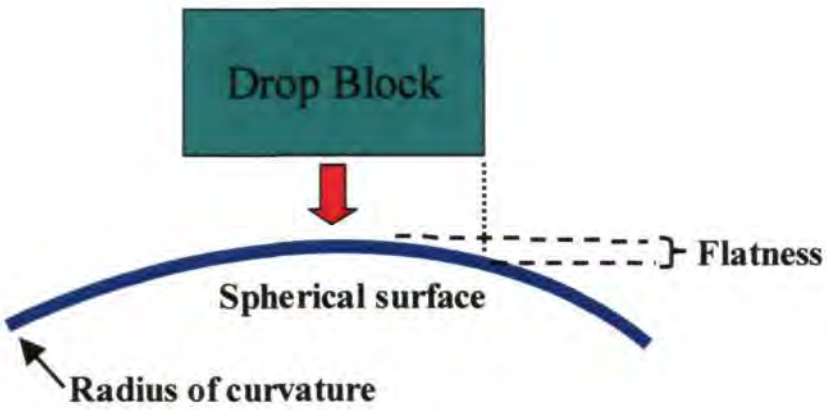

Figure 7.20. Impact on uneven surface

When radius of curvature is smaller, the peak acceleration is reduced, and impact duration becomes longer (see Table 7.7). This is because the block hits the center point of curvature first, and there is more time for the block to deform and have contact with other curved surface before rebounding. Flat-to-flat surface contact is a special case with infinite radius of curvature, as there is little room for deformation, the block has to

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rebound within a very short impact duration, therefore higher peak acceleration is generated (according to Eq. (7.6)). Naturally, when peak acceleration is higher, the solder peeling stress is also larger, and impact life is reduced.

Effect of Mass-scaling

Mass-scaling is common technique used in dynamic simulation to increase the minimum solution time step, in order to shorten the solution time. Eq. (7.2) shows that the minimum time step is dependent on the minimum element length, density and modulus. After fine-tuning in element meshing, usually there is little change can be done on length of element, especially in thin material layers such as solder mask, copper pad, and die attach. Mass-scaling increases density of elements with the smallest time step (computed by Eq. (7.2)). The additional mass is usually negligible (less than 1E-5%) compared to the total mass of system, therefore won't affect the acceleration distribution.

Table 7.8 shows that the solution time can be reduced by about 2 or 4 times, when the minimum time step is increased by 2 or 4 times. For a typical case without mass-scaling, the solution time is about 8 hours. Within 4 times of increment in the minimum time step, the percentage of difference is insignificant. When the time step is too large (e.g. 10 times), density of critical solder elements is affected, and therefore the accuracy of solder peeling stress is compromised. Mass-scaling is acceptable, as long as the density of elements modified is not in the solder material, which is the area of concern. The largest solution time step that can be adjusted by mass-scaling may be calculated based on the smallest element length of solder material.

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Table 7.8. Results of mass-scaling effect

Mass-scaling Factor	Min. Time Step (s)	Solution Time (hr)	Solder Stress (MPa)	% Diff.
1	2E-9	8	141.2	-
2	4E-9	4	139.1	-1.5
4	8E-9	2	138.0	-2.3
10	2E-8	0.8	149.7	6.0

Effect of Element Size

The accuracy of modeling solution usually depends on element size control. Table 7.9 shows the sensitivity results of solder element size. The control case uses solder element size of 60μm. When the element size is reduced by half, the maximum solder stress is increased by 6%, and the difference in mean impact life is less than 1 drop (using Eq. (7.9)). Therefore, it is advisable to apply a consistent element size throughout the model, especially when there is any change in package or board geometry dimensions.

Table 7.9. Results of element size effect

Element Size (μm)	Solder Stress (MPa)	% Diff.
60	141.2	-
40	147.1	4.2
30	150.0	6.2

7.8 APPLICATION IN QFN PACKAGE

7.8.1 Background

The same drop impact modeling methodology developed earlier for TFBGA package is applied for QFN package. A schematic of QFN-4x4mm package used in this study is

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shown in Figure 7.21. The peripheral leads are exposed at the package bottom for soldering to the board. Extra soldering under the center die pad and at diagonal corners is optional.

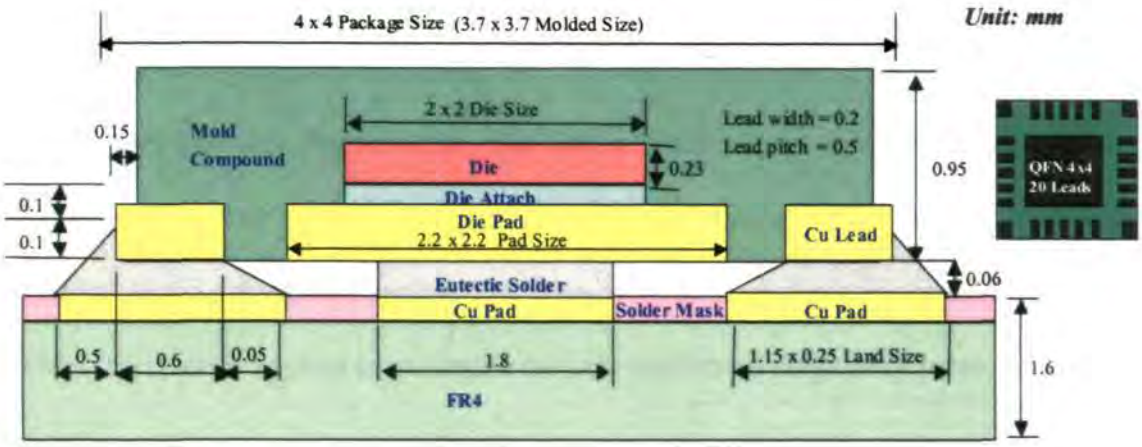

Figure 7.21. Schematic of QFN-4x4mm with 20 leads

7.8.2 Finite Element Model

In this study, board level drop test simulation is performed on a 0.5mm pitch QFN-4x4mm (see Figure 7.21). Quarter 3D model is established due to symmetry (horizontal drop, component faced down). The package size is 4x4mm (20 leads), die size is 2x2mm, and board size is 140x125x1.6mm. Detailed package geometry, solder joints, and pad design are included in the model. There are 16 packages (4x4 matrix) on board, but it is modeled as single package on board center, to reduce the computational time. The discussions below are based on QFN-4x4mm package tested in component face-down direction, and PCB mounted by four corner screws to the fixture.

The critical solder joint is at the corner, with stress concentration along the top peripheral solder/lead interface and the edge of solder fillet (see Figure 7.22, quarter model shown). Vertical normal peeling stress (σ_z) is responsible for failure along top solder/lead interface, whereas horizontal normal peeling stress (σ_x or σ_y) induces

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opening along the vertical edge of solder fillet and lead. The stress concentration correlates well with actual failure mode and critical solder joint location observed from experiment. For the failed QFN-4x4mm sample, all the solder joints are cross-sectioned row by row, and the corner solder joint is observed to have failure, a brittle crack in solder intermetallic, along the top solder/lead interface and vertical edge of solder fillet/lead (see Figure 7.22). The failure mode is peel-dominant, and this further validates the earlier modeling assumption, using the normal peeling stress as the failure criteria. In the subsequent analysis, volume-average normal peeling stress along the top solder interface is applied to minimize the potential stress singularity issue.

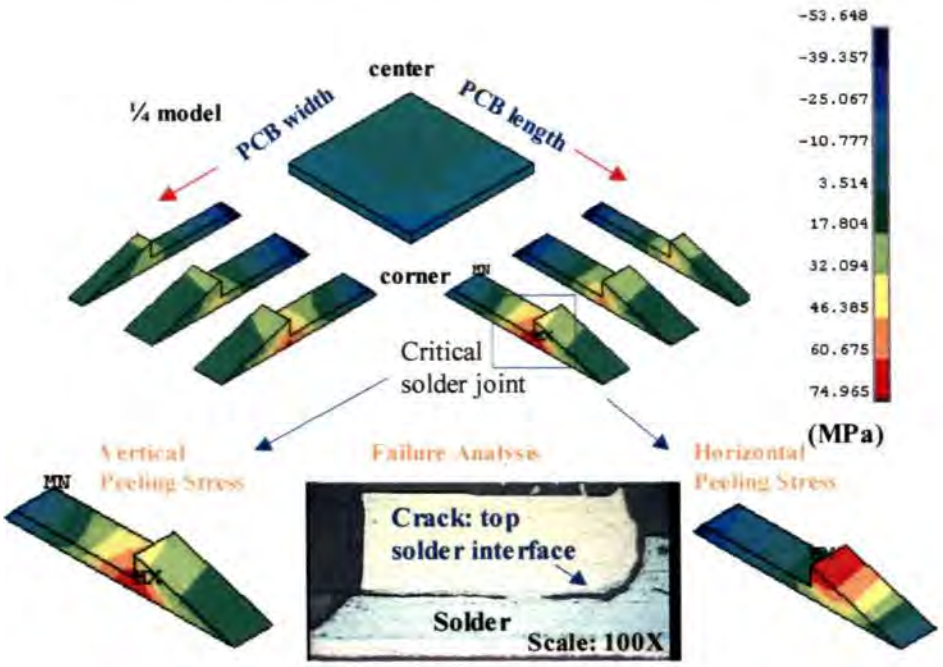

Figure 7.22. Critical solder joint and failure interface

7.8.3 Impact Life Prediction Model

The next step of more in-depth modeling is to evaluate the impact performance quantitatively, using a life prediction model. Experimentally (see Table 7.10), there are three different cases of QFN-4x4mm tested with different drop orientation (up/down),

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and with/without PCB bending. There are 16 packages (4x4 matrix) per board. Case 3 has no spacer in between board and fixture, therefore there is no PCB bending.

Table 7.10. Results of modeling-testing correlation for QFN

Case	Component Orientation	Solder Stress (MPa)	N_{50} (# Drops)		N_f (# Drops)	
1	Face-down	24.18	1		1	
2	Face-up	9.21	36		20	
3	Face-up (no bending)	2.87	>50	2726	>50	71

Since Case 3 has no failure at all after 50 drops, the results cannot be quantified, therefore only Cases 1-2 are correlated. The experimental impact lives (number of drops to failure) for Cases 1-2 are given in Figure 7.23, and results will be discussed in detail later.

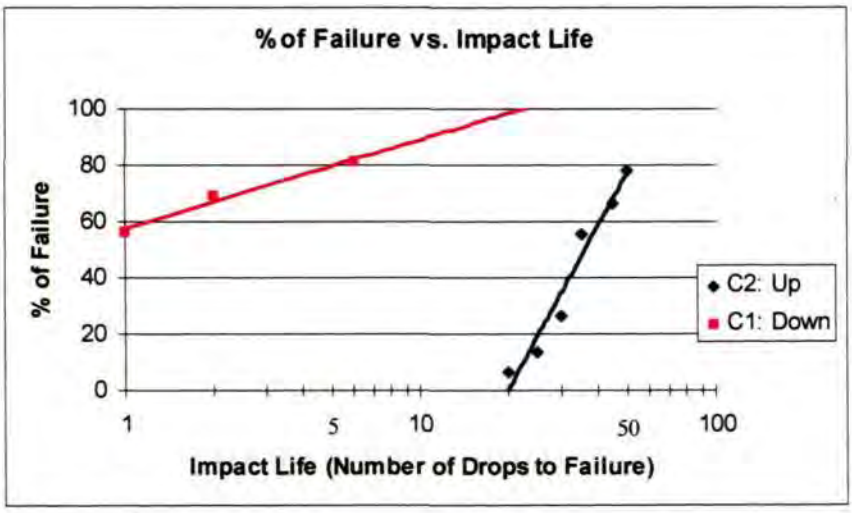

Figure 7.23. Experimental results of impact life

Following the same methodology as TFBGA package (see Section 7.4), an impact life prediction model is formulated for QFN package using power law to relate the average peeling stress and mean impact life (see Figure 7.24). The correlation

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constants used in Eq. (7.9), C_1 and C_2, are 136471 and –3.7117 respectively. The impact life increases steeply when the solder peeling stress is low. When the peeling stress is less than about 8MPa, the mean impact life is higher than 50 drops. Since there are only two exact experimental data, the uncertainty of impact life prediction is not applicable (curve-fitted exactly by the power law). However, Case 3 (no PCB bending) which has no failure within 50 drops, can be used for model validation later. In future, the model can be fine-tuned with more experimental cases. Power law may not be the best curve fit for this case due to limited testing data. However, it is a logical assumption based on prior modeling and testing experience of CSPs.

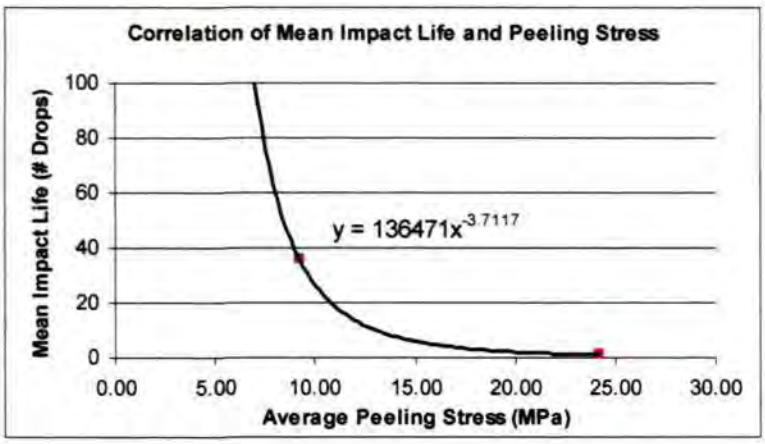

Figure 7.24. Experimental impact life vs. peeling stress

7.8.4 Design Analysis

The drop test results are given in Figure 7.23 and Table 7.10, and several effects can be studied. The testing results are analyzed and compared with modeling, to gain a more in-depth understanding on physics of these dynamic failures. The validated dynamic model can be applied to study other effects, to save the time, manpower, and cost in performing the actual drop tests. The focus of this section is on the effects of testing and modeling variables. The control case used for design comparison is Case 1 (see Table 7.10), QFN-4x4mm with solder fillet, tested in component face-down

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direction (PCB bending allowed) from 1.5m drop height. The design variables studied are varied one at a time with respect to the control case. Most effects are similar to board level drop test of TFBGA package (see Section 7.7).

Effect of Component Position

A more detailed model is constructed with one package on center of board and four packages on corner of board to study the relative solder joint stress level between center and component. For Case 1 (component face-down), compared with center component, the average solder peeling stress level of corner component is 20% lower. This result shows that center component has much higher stress level than corner component, due to more PCB bending. Therefore, components positioned at board center are more susceptible to failure than corner components for component face-down orientation. The modeling results correlate well with experimental observations (see Table 7.10). For Case 1, there are 12 failures, out of total of 16 components. The center packages fail first after 1 drop, and only the four corner packages have no failure at all after 50 drops.

Effect of Drop Orientation

Table 7.10 shows that for QFN package, component tested in face-down direction is found to be more severe than in face-up direction. However, for face-up drop orientation, once the failure is initiated, the failure rate is faster (see Figure 7.22, steeper slope). It does not mean that QFN has worse drop test performance compared with TFBGA, since different board size and design are used. For this QFN study, the board size used is much larger than TFBGA, therefore the bending stress is larger, and impact life is shorter.

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PCB is allowed to bend for both drop orientations. When component is in face-down orientation, the solder joints experience additional package inertia force, besides the critical PCB bending stress. Besides, there is a possibility that due to excessive PCB warpage, the components mounted in face-down orientation have contact with the fixture below, and additional contact stress is induced. The recommended test of 50 drops in component face-down direction with 4200G, is able to induce enough solder joint failures for most packages.

Effect of PCB Bending

The PCB in Case 3 (component face-up) is not allowed to bend, as the PCB is mounted closely to the fixture with four screws without any spacer. Compared to other cases with PCB bending (e.g. Cases 1 & 2), Case 3 has much lower solder peeling stress (see Table 7.10) and therefore much longer impact life.

For Case 3, the modeling predicted mean and failure-free impact life is 71 drops. This life prediction explains why in the actual testing, there is no failure at all within the first 50 drops for these two cases. This is additional proof on the accuracy of life prediction model established.

Effect of Solder Fillet

Figure 7.25 shows QFN designs with different solder fillet height (control case is mid fillet height). Table 7.11 shows that the case with mid solder fillet has much lower peeling stress than either low or no solder fillet. Additional solder fillet helps to strengthen the solder joint against impact failure, because the solder fillet/lead edge has to crack first, before propagating through the top solder interface (see Figure 7.22).

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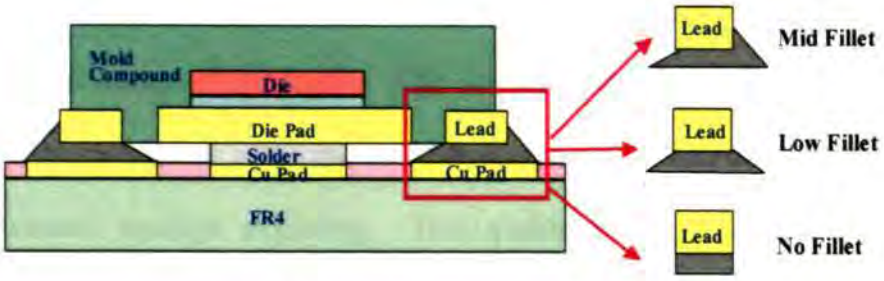

Figure 7.25. Different solder fillet designs

Table 7.11. Results of solder fillet effect

Solder Fillet Height	Solder Stress (MPa)	% Diff.
No Fillet	42.00	73.7
Low Fillet	39.27	62.4
Mid Fillet	24.18	-

7.9 SUMMARY

Comprehensive drop tests, failure analyses, and simulations are performed on TFBGA and VFBGA packages at board level. The solder joint failure is induced by the combined stress of mechanical shock and PCB bending. The critical solder ball is observed to occur at the outermost corner solder joint, and fails along the solder and PCB pad interface under peeling mode. Normal peeling stress is confirmed as the major stress component of solder joint, and the PCB cyclic bending or vibration fatigue is the main failure mechanism of solder joints during drop impact. This failure mechanism and location of critical solder joint are supported by same observations in both drop test and simulation.

For the first time, an accurate life prediction model is established for board level drop test to estimate the number of drops to failure for a package. For the correlation cases studied, the maximum normal peeling stresses of critical solder joints correlate

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well with the impact lives measured during the drop test, within uncertainty of ±4 drops, for a typical test of 50 drops. With this new model, a failure-free state can be determined, and drop test performance of new package design can be quantified, and further enhanced through modeling. This quantitative approach is different from traditional qualitative modeling, as it provides both accurate relative and absolute impact life prediction.

The focus of this combined testing and simulation analysis is to study the effects of drop testing variables on impact life. Component mounted on board center experiences larger bending stress than components mounted on board corner, near the PCB mounting screws. Drop orientation with component face-down is found to be more stringent than component face-up. During the drop test, the PCB must be allowed to bend in order to induce larger stress to the solder joints. It was shown that solder joints in the outermost PCB length direction usually have relatively larger stress, and smaller PCB size is useful to enhance the impact life. Besides, flatter contact surface induces higher peak acceleration, and therefore shorter impact life.

Detailed drop tests, failure analyses, and simulations are also performed on QFN-4x4mm packages at board level. The critical peripheral solder joint is observed to occur at the corner lead. Failure is in peel mode, initiated along the solder fillet/lead edge, propagating through the top solder/lead interface at the component side. QFN design with higher solder fillet is recommended to enhance the impact performance.

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CHAPTER 8 INTEGRATED SOLDER JOINT RELIABILITY MODELING

8.1 INTRODUCTION

Board level solder joint reliability of various CSPs during thermal cycling test and drop test are well investigated in Chapters 5-7, but they are discussed separately. Here, the same modeling methodology is applied to perform integrated design analysis of solder joint reliability. The effects of package parameters on solder joint reliability of both thermal cycling test and drop test are studied at the same time for BGA CSP and Integrated Passives Device (IPD).

8.2 BOARD LEVEL MODELING OF BGA CSP

8.2.1 Background

The demand for fine-pitch CSP is becoming higher as it fills the need for low cost, miniaturization, and high performance requirements of mobile phones, notebooks, PDAs, and other handheld electronic products. For such device, board level solder joint reliability due to drop test, bend test and thermal cycling test is a great concern to the manufacturers. The mechanical shock resulted from mishandling during transportation or customer usage may cause solder joint failure, which leads to malfunction of product. PCB bending induced by accident drop of mobile phones or pressure applied on key pad may also result in reliability concern. Besides, the device may be operated under extreme temperature conditions. Under different combined loadings of operating conditions, the field life of CSP may be limited.

Over the past few years, there has been increasing interest in board level testing and modeling related to drop, bend, and thermal cycling due to industrial demand. However,

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most researchers only investigate on reliability of one particular test, and there are limited publications related to integrated design analysis of all three types of board level tests using both experimental and numerical methods. This chapter presents a comprehensive solder joint performance analysis of a fine-pitch CSP under board level drop test, bend test, and thermal cycling test. Both testing and modeling under all three board level tests are performed, and the relative solder joint reliability as well as the failure modes are analyzed. The effect of underfill on solder joint performance under various board level tests is also investigated.

8.2.2 Drop Test, Bend Test, and Thermal Cycling Test

For drop test, the modeling and testing procedures are given in Chapter 7. Here, an impact pulse with peak acceleration of 3700G and impact duration of 0.4ms is applied. As for thermal cycling test, the modeling and testing details are explained in Chapter 5. A temperature cycle test condition of -40 to 125°C at 40mins/cycle is applied.

Board level bend test is a new analysis to supplement the drop test, as it was known that cyclic PCB bending is resulted after the drop impact. The 3-point bending test is usually carried out using Instron universal tester. The board with packages facing down is placed on two supports with a span of 105mm, and a cyclic displacement-controlled load is acted on the top of PCB center such that downward displacement of 4 mm (speed of 400 mm/min) is achieved. Then, the PCB springs back by itself in the upward direction to the original starting position. Viscoplastic model is applied for solder joint reliability analysis under bend test. Volume averaging of the elements at the critical solder joint interface is used to calculate the strain energy density (SED) accumulated per cycle. Larger SED leads to shorter solder joint fatigue life.

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8.2.3 Finite Element Model

The geometry for the CSP is shown in Figure 8.1. It is a 0.5mm pitch BGA with 7x7mm package size, 4x4mm die size, and 84 solder balls. The thermo-mechanical material properties used are listed in Table 8.1. Temperature-dependent material properties are considered. PCB and substrate are considered to be orthotropic. For solder material, viscoplastic model is applied for both thermal cycling test and bend test. The rest of the materials are assumed to be linear elastic.

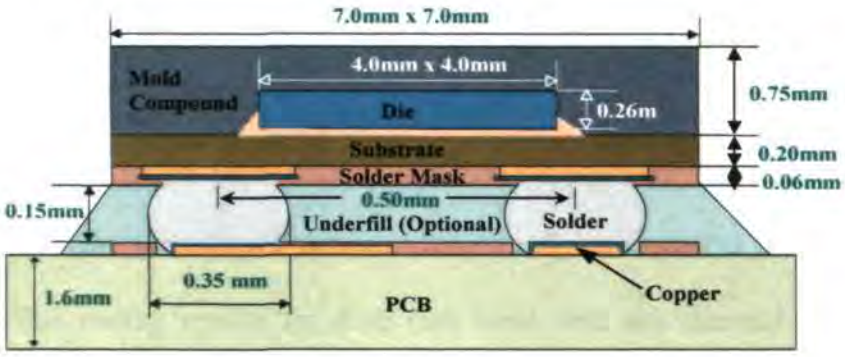

Figure 8.1. Schematic of BGA CSP package

Table 8.1. Thermo-mechanical material properties

Materials	CTE (ppm/°C)	Modulus (GPa)	Density (Mg/mm^3)
Silicon Die	2.8	131	2.33e-9
Copper Pad	17.7	117	8.96e-9
Mold Compound	8	25.02	2.00e-9
Die Attach	72	0.5	1.75e-9
Underfill	31	4	1.75e-9
Eutectic Solder	25	31.6	8.4e-9
Solder Mask	95	5	1.15e-9
PCB	xy: 17 z: 60	xy: 25 z: 11.0	2e-9
Substrate	xy: 17 z: 55	xy: 26 z: 11.0	2e-9

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3D finite element models are constructed for CSP to compare the relative performance of solder joints and the failure modes under various board level tests. For thermal cycling test model, a board size of 3mm larger than package size is assumed to reduce computational time with minimal effect on the result. However, for drop test and bend test models, a full board size of 115x77mm has to be modeled as it has significant effect on solder joint reliability. Experimental results are compared to verify the modeling results for all three board level tests.

8.2.4 Discussion of Results

There are 10 packages (2x5 matrix) mounted on the PCB (see Figure 8.2). Three boards are used for thermal cycling test, whereas only one board is tested for drop and bend tests. The testing results for drop test, bend test, and thermal cycling test are shown in Table 8.2.

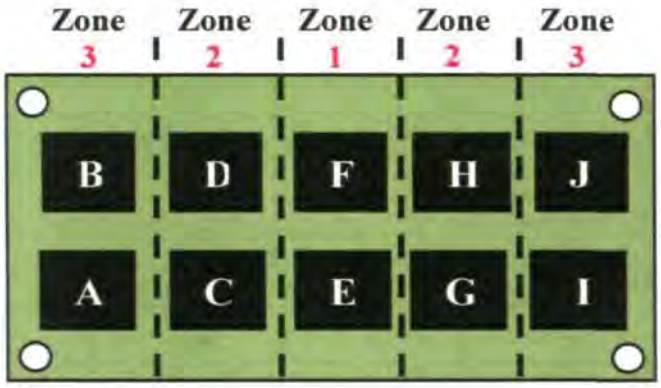

Figure 8.2. Package position on test board

For board level drop test, solder joint failures are induced by shock and PCB bending. Therefore, packages at PCB center (*E* and *F*) are more likely to fail first as PCB center has the maximum bending. The other packages away from PCB center (*A*, *B*, *C*, *D*, *G*, *H* and *I*) can withstand higher number of drops (>50 drops) before failure.

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Package *J* may have assembly defects, thus resulting in low number of drops to failure. In the subsequent drop tests at different height (unreported here), package *J* is never the first failure, and its impact life is much stronger than packages on PCB center. PCB length (115mm) is larger than width (77mm) direction, thus packages will fail along PCB length rather than width direction, according to three Zones 1, 2 and 3. Packages located in the same zone will fail around the same time.

For board level bend test, package position effect is also significant as solder joint failures are also induced by PCB bending, though at lower strain rate than drop test. Packages in Zone 1, which are near the package center, are the most susceptible to failure, and those in Zone 3 (furthest away from PCB center) can withstand a very large number of bending cycles without failure.

For board level thermal cycling test, package position effect is not significant. Packages fail randomly at any position on board. Solder joint failures are induced by CTE mismatch among solder joints, package, and PCB during thermal cycling. The failure mechanism is different from drop test and bend test.

Table 8.2. Summary of board level test results

Drop Test (Number of Drops)										
Zone	**3**		**2**		**1**		**2**		**3**	
Package	***A***	***B***	***C***	***D***	***E***	***F***	***G***	***H***	***I***	***J***
W/O U/F	67	57	N/A	>80	30	33	52	>80	56	25
With U/F	N/A	>250	>250	N/A	35	70	162	>250	>250	82
Bend Test (Cycles)										
Zone	**3**		**2**		**1**		**2**		**3**	
Package	***A***	***B***	***C***	***D***	***E***	***F***	***G***	***H***	***I***	***J***
W/O U/F	>50000	>50000	1343	3353	987	882	4197	3960	>50000	>50000
With U/F	>200000	>200000	85009	>200000	917	2410	29798	35003	>200000	>200000
Thermal Cycling Test (Cycles)										
Zone	**3**		**2**		**1**		**2**		**3**	
Package	***A***	***B***	***C***	***D***	***E***	***F***	***G***	***H***	***I***	***J***
W/O U/F	488	605	551	537	494	516	505	548	459	531

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8.2.5 Failure Analysis

Dye penetration test and cross-sectioning of solder joints are performed for drop test, bend test, and thermal cycling test (see Figures 8.3, 8.4 and 8.5 respectively) to determine the failure locations, failure interfaces, and failure modes. A combination of dye penetration test and cross section technique provide a full picture of solder joints failures.

For drop test and bend test, solder joints fail at the outermost row along the PCB length direction. The first solder joint failure is at the corner solder ball, cracking along the solder/component pad interface. Failures of several non-critical solder joints are observed along solder/PCB pad interface. Distance-to-neutral point (DNP) effect is dominant for both drop test and bend test, as the PCB bends and induces high tensile stress to solder joints. For thermal cycling test, solder balls under the die edge is more likely to fail. Local CTE mismatch between die and solder balls has more significant effect than DNP (global CTE mismatch between package and board) on solder joint failures, which are along solder/component interface.

For drop test, the solder joint is observed to have a smooth fracture surface (see Figure 8.3). This is a brittle type of failure, usually induced by stress-controlled high-cycle fatigue. Therefore, solder joint peeling stress can be used as the failure criteria in the drop test simulation. As for bend test and thermal cycling test, a dimpled solder joint failure interface is observed (see Figures 8.4 and 8.5 respectively). This is a ductile type of failure, corresponding to strain-controlled low-cycle fatigue. Therefore, SED is usually used as the failure criteria in bend test and thermal cycling test simulation with consideration of plastic and creep deformation.

Figures 8.6, 8.7 and 8.8 show the peeling stress distribution of solder joints during drop test, and SED distribution of solder joints during bend test and thermal cycling test

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simulation respectively. The simulation results are able to correlate with experimental observations related to the failure location and failure interface. The stress or SED concentration is along the solder/component interface, where actual failures are observed in testing. In the drop test model (see Figure 8.6), four corner solder joints have the highest peeling stress, due to strong DNP effect. As for bend test model (see Figure 8.7), solder joints along the outer rows in PCB length direction have relatively higher SED, and therefore lower bending fatigue life, correlating well with experimental observations (see Figure 8.4). In the thermal cycling test model (see Figure 8.8), SED is higher in the four solder joints under the die corner, corresponding to the same critical solder joint locations found in failure analysis (see Figure 8.5).

The differences in failure modes are due to unique loading and failure mechanism of each board level test. For both drop test and bend test, the solder joint failures are predominantly induced by PCB bending while for thermal cycling test, the failures are mainly due to CTE mismatch of packaging materials during temperature change. Therefore, drop and bend tests fail mainly in peeling mode for critical solder joint during PCB bending while thermal cycling test usually fails in shearing mode. For both drop test and bend test, the packages located at the PCB center are more critical while for thermal cycling test, results are not sensitive to package position on the PCB. Therefore, to enhance the solder performance for drop test and bend test, detailed consideration of board design is required. PCB should be designed to minimize the PCB bending, such as using smaller PCB size, square PCB shape, stiffer PCB, or adding more mounting screws to the fixture. As for enhancement of thermal cycling test performance, one should look at reducing CTE mismatch among the solder joint, package, and PCB.

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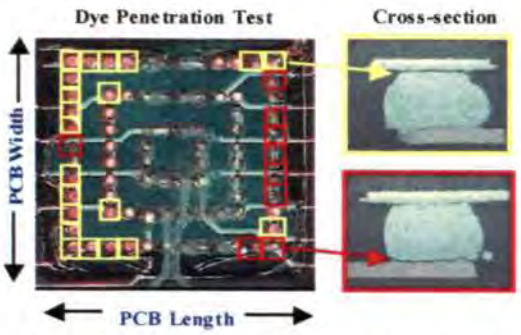

Figure 8.3 Failure analysis of drop test

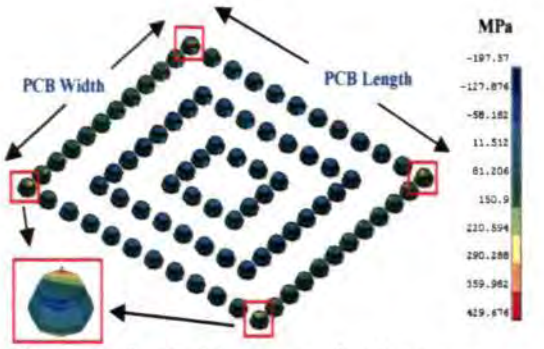

Figure 8.6. Solder stress in drop test

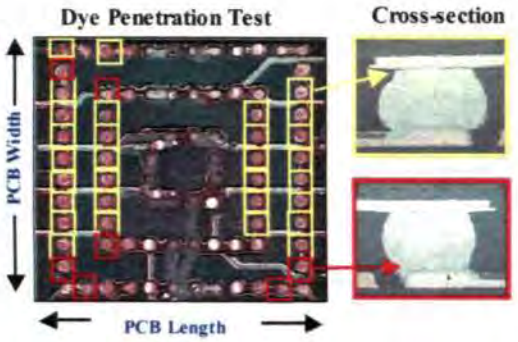

Figure 8.4. Failure analysis of bend test

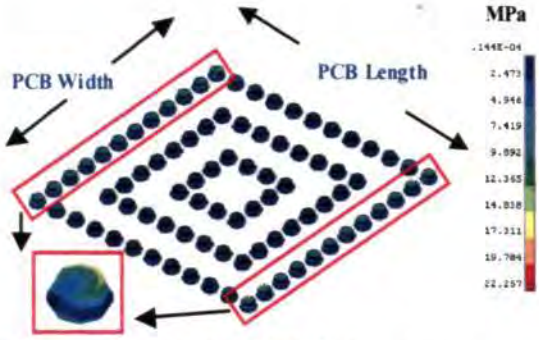

Figure 8.7. Solder SED in bend test

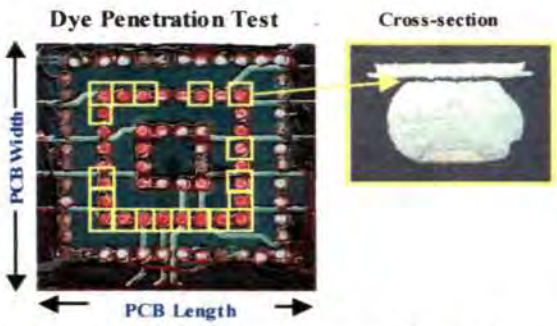

Figure 8.5. Failure analysis of thermal cycling test

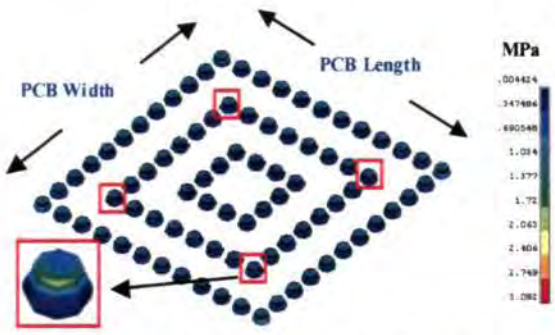

Figure 8.8. Solder SED in thermal cycling test

Depending on end applications and customer requirements, package and board designs have to be compromised to optimize the performance of particular test, while maintaining an acceptable reliability level for other less critical tests. For example, mobile phones require packages to have strong impact performance as the product may fail with accidental drop onto the floor. However, as the product usage life is short (a few years before changing to a new model), the requirement of thermal cycling test is relatively less significant.

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8.2.6 Effect of Board Level Underfill

Board level underfill is a more general and practical design enhancement, when the effects of other package and board parameters are limited. The effects of underfill enhancement on drop test and bend test are shown in Figures 8.9 and 8.10 respectively.

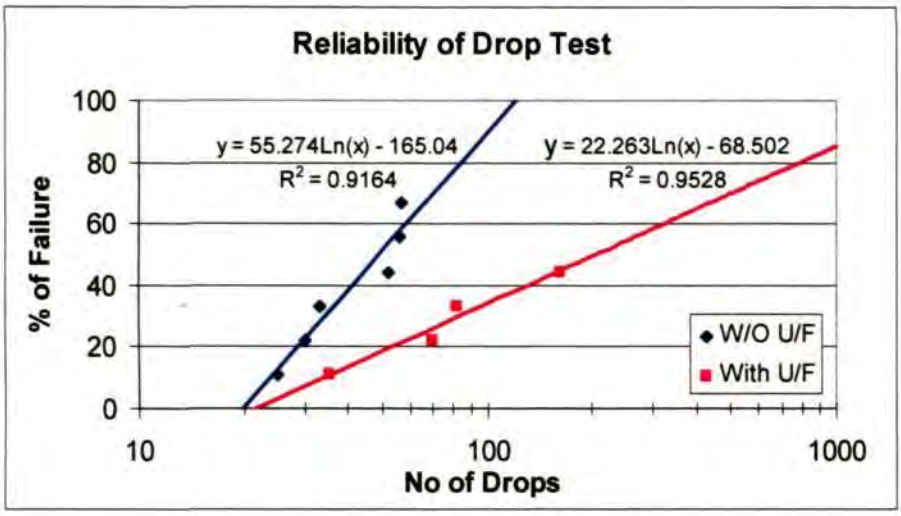

Figure 8.9. Reliability results of drop test

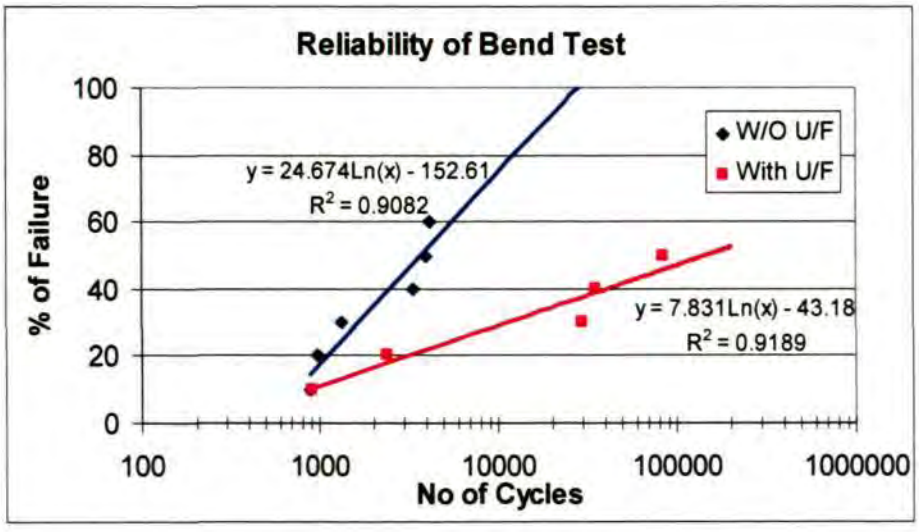

Figure 8.10. Reliability results of bend test

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The mean impact life (at 50% failure rate) and the first-failure life are summarized in Table 8.3. Similarly, Weibull plot can be obtained for thermal cycling test results (only two failures recorded for underfilled CSP) and the characteristic life at 63.2% failure rate is listed in Table 8.3.

Table 8.3. Mean life and first-failure life

Tests	Drop Test (# Drops)		Bend Test (Cycles)		Thermal Cycling Test (Cycles)	
Lives	Mean Life	First Failure	Mean Life	First Failure	Char. Life	First Failure
W/O U/F	49	30	3683	882	556	358
With U/F	205	35	147099	917	6700	2254
Factor	4.18	1.17	39.94	1.04	12.05	6.30

Figure 8.11 shows the mean impact life of drop test correlated to the maximum normal peeling stress of solder joint obtained from modeling. An impact life prediction model is formulated using power law approach to relate the maximum peeling stress of critical solder joint and mean impact life, according to Eq. (7.9) with correlation constants, C_1 and C_2, computed as 174052 and –1.328 respectively. Power law may not be the best curve fit for this case due to limited testing data. However, it is a logical assumption based on prior modeling and testing experience of CSPs.

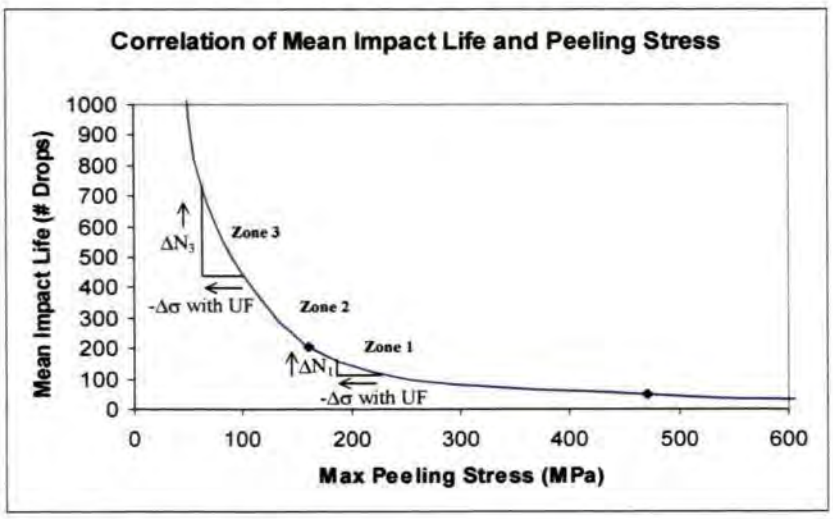

Figure 8.11. Impact life prediction model for CSP

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The use of underfill always enhances the board level solder joint reliability. For thermal cycling test, underfill has great improvement on both characteristic life and first-failure life (see Table 8.3). However, for drop test and bend test, underfill has great improvement on mean impact life, but only slight improvement on first-failure life.

The effect of package position on PCB is significant for drop test and bend test. Packages located near the board center (Zone 1) are more likely to fail than those away from PCB center (Zone 2 and 3). Similarly, underfill has more improvement on reliability of packages in Zone 3, following by Zone 2, and minimal effect in Zone 1. As illustrated in Figure 8.11, the use of underfill reduces the stress in the solder joint. Since the mean impact life correlates to the maximum peeling stress by power law, with the same reduction of stress, improvement in impact life is greater in Zone 3 compared to Zone 1 ($\Delta N_3 > \Delta N_1$). As packages on board center usually fail first, there is only slight improvement in reliability when underfill is applied. Therefore, it is important where packages are placed on the PCB. For board with four corner mounting screws, bending is significant, therefore critical packages should not be placed near the center, as using underfill only has little improvement on the first-failure life of board level drop test and bend test. However, it should be pointed out that usually the solder joints under field condition has much lower stress compared with accelerated board level tests. Thus, in actual product applications, board level underfill is still useful to improve both first-failure life and mean life of components.

As for thermal cycling test, package position on board is not significant on the reliability result. There is no concentrated stress near board center as in drop test and bend test, and the stress level is more evenly distributed. Therefore, use of underfill will have large improvement on solder joint reliability during thermal cycling test regardless of package position on board.

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8.3 BOARD LEVEL MODEL OF IPD

8.3.1 Background

IPD is a new solution for miniaturized system integration, in which the passive components are embedded into the substrate. The embedded passive technology [138-139] offers great advantages of package efficiency, reduced assembly cost, and improved system performance. This will become more crucial in the coming years with package miniaturization as the ratio of passive components to active components will be increasing in electronic products. IPD is mainly used for RF applications in handheld or portable telecommunication devices such as mobile phones and PDA. For such device, board level solder joint reliability due to drop test and thermal cycling test is a great concern.

8.3.2 Finite Element Model

3D FEA models are constructed for IPD on board to predict the solder joints fatigue life during the thermal cycling test and impact life under the drop test. Figure 8.12 shows the schematic diagram of IPD-2.51x2.51mm with 0.5mm ball pitch and 25 I/O.

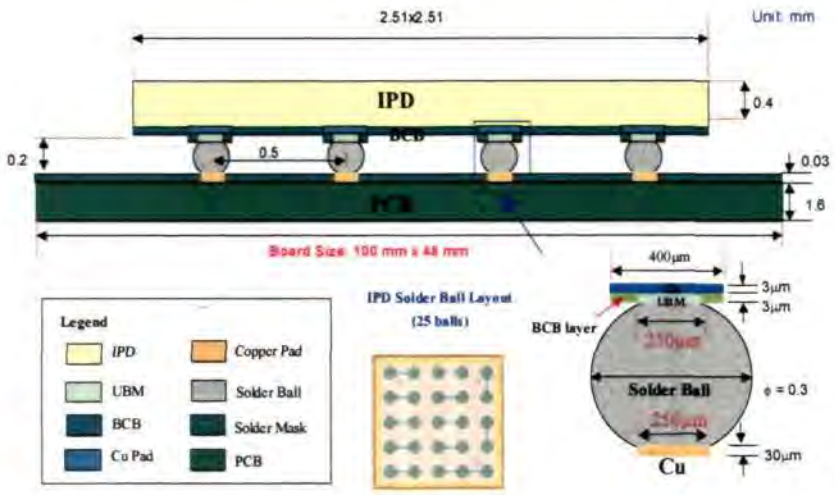

Figure 8.12. Schematic of IPD mounted on board

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8.3.3 Simulation Results

Drop Test Simulation

Figure 8.13 shows the warpage distribution of PCB during bending. The PCB has much larger warpage in the length direction (0.238mm) than in the width direction (0.002mm). The bending stress induced is determined by relative vertical displacement (warpage) of the solder joint position with respect to the package or PCB center, which is a neutral point (see Figure 7.4). As a result, the outer row of solder balls in the PCB length direction warps more relative to the PCB center and has higher bending stress level (see Figure 8.14). This row of solder balls is more likely to fail first. High stress concentration is observed along both the solder/PCB pad interface and solder/IPD pad interface. Therefore, both of these two interfaces are likely to fail, depending on the adhesion strength of the interfaces. The failure of critical solder joint under drop impact is mainly in peeling mode.

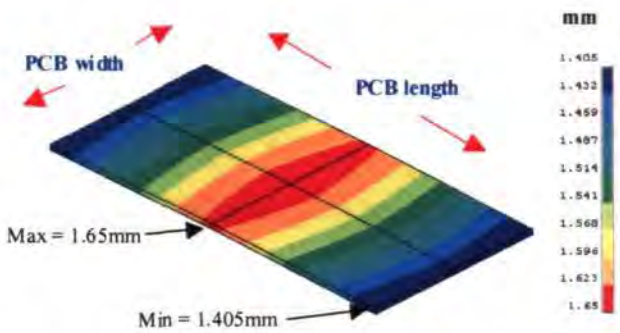

Figure 8.13. PCB warpage distribution during maximum bending

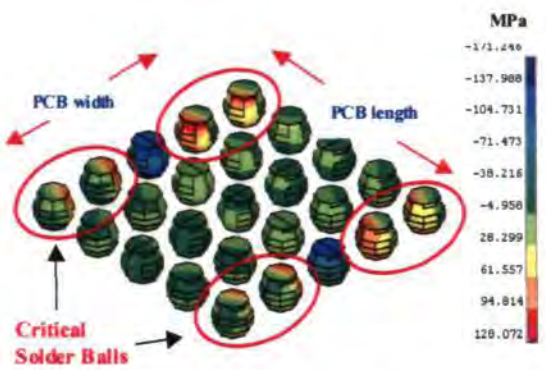

Figure 8.14. Stress distribution of solder joints during maximum PCB bending

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Thermal Cycling Test Simulation

Due to DNP (distance to neutral point) effect, the critical solder ball for IPD studied is observed to be at the outermost corner (see Figure 8.15), along the top layer of solder ball, which is the potential failure interface for crack propagation. The failure of critical solder joint under thermal cycling test is mainly in shearing mode due to CTE thermal mismatch.

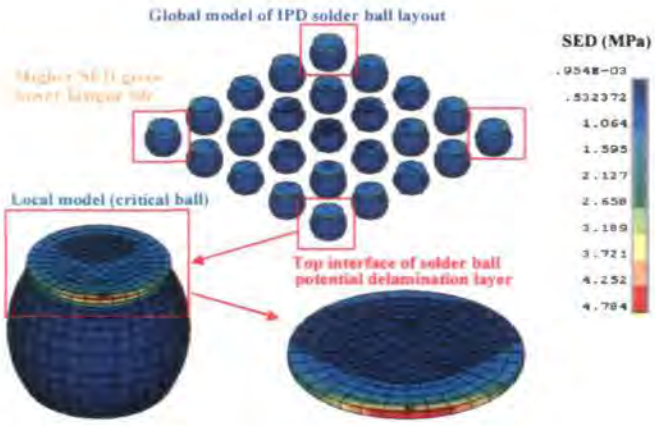

Figure 8.15. SED distribution of solder joints during thermal cycling test

8.3.4 Integrated Design Analysis

The board level solder joint reliability under drop test and thermal cycling test for eight different IPD design variations are studied and analyzed. The design parameters are IPD shape, IPD size, IPD thickness, IPD material properties, solder material, solder ball layout, PCB size, and PCB material properties. The results to be discussed are summarized in Table 8.4. Absolute solder joint fatigue lives are compared for thermal cycling fatigue test while for drop test, only the solder joint peeling stresses are studied for relative impact life performance.

The structure of IPD on board can be treated as a simple bi-material (IPD/PCB) connected by solder joints. The shear strain range, $\Delta\gamma$, of solder joints induced during

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thermal cycling, can be approximated by

$$\Delta\gamma = \frac{\Delta\alpha \cdot \Delta T \cdot DNP}{h} \tag{8.1}$$

where $\Delta\alpha$ is the CTE difference between IPD and PCB, ΔT is the thermal loading, DNP is the distance to neutral point (from IPD center to position of outermost corner solder joint), and h is the solder ball standoff. Shear strain range behaves likes SED, and the value should be minimized to enhance the fatigue life. This simple equation implies that CTE mismatch, thermal loading, and DNP should be minimized while solder standoff should be maximized, to increase the solder joint fatigue life.

IPD Shape

Comparing the shape of package (see Figure 8.16) with close area size, square IPD performs better than rectangular IPD in both drop test and thermal cycling test (see Table 8.4). With square design, the stress or SED can be distributed evenly in in-plane directions (see Figures 8.14-8.15). On the other hand, for rectangular IPD, the stress is higher in the length direction, and concentrated at the four corner solder joints.

DNP effect of rectangular IPD is larger than square IPD, and it gives lower fatigue life, according to Eq. (8.1). Larger DNP also results in larger PCB bending stress during drop impact. In addition, there are more solder balls under the square IPD (25 I/Os for 2.51x2.51mm IPD) than rectangular IPD (20 I/Os for 1.01x5.01mm IPD), to redistribute the stress induced.

Figure 8.16. Square and rectangular IPD

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Table 8.4. Simulation results of drop test and thermal cycling test

Design Variations		Drop Test		Thermal Cycling Test	
		Peel Stress (MPa)	% Diff.	Fatigue Life (Cycles)	% Diff.
IPD Shape	Square (2.51x2.51mm)	82.07	-	1749	-
	Rectangular (1.01x5.01mm)	105.79	16.3%	1081	-38.2%
IPD Size	2.51x2.51mm	82.07	-	1749	-
	5.01x5.01mm	84.72	2.5%	704	-59.8%
IPD Thickness	0.4 mm	82.07	-	1749	-
	0.7 mm	89.21	6.6%	1317	-24.7%
Solder Material	Lead-free	82.07	-	1749	-
	Eutectic	68.52	-16.5%	1459	-16.6%
PCB Modulus	25400 MPa	82.1	-	1749	-
	76200 MPa	59.8	-27.2%	1600	-8.5%

IPD Size

The size of IPD (see Figure 8.17) has no significant effect on drop test but smaller IPD enhances the solder joint reliability under thermal cycling test (see Table 8.4). The behavior of IPD package is similar to WL-CSP package in which there is a fundamental limit in package size (see Section 5.5.4). When the IPD size increases, the position of the outermost corner solder ball is further away from the IPD center, resulting in larger DNP, and therefore, lower fatigue life.

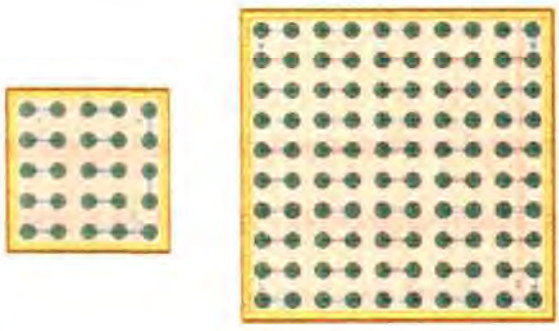

Figure 8.17. Different IPD size and number of solder balls

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IPD Thickness

Thinner IPD is preferred for both drop test and thermal cycling test (see Table 8.4). Thinner IPD is more compliant, and therefore induces lower solder joint stress during drop impact and under thermal cycling test. With technology advancement, IPD substrate thickness can be made thinner. This can greatly help to improve both drop and thermal cycling performance.

Solder Material

Lead-free solder is found to perform better in thermal cycling test, but poorer under drop test, compared to eutectic solder (see Table 8.4). Therefore, not all design changes are good for both drop and thermal cycling test. This is because the failure modes and mechanisms for drop test and thermal cycling test are totally different, i.e. one fails by sudden peeling stress while the other one fails by fatigue loading in shear mode. It is important to identify which test is more important for the package application. For IPD packages which are used mainly in handheld or portable telecommunication devices, drop test is usually more critical than thermal cycling test. If lead-free solder must be applied as a design constraint, other design parameters should be optimized towards better drop impact performance.

PCB Modulus

PCB with higher modulus is better for drop test but it leads to poorer thermal cycling test performance (see Table 8.4). Higher PCB modulus results in a stiffer PCB, and thus lower PCB bending stress during drop impact. As for thermal cycling test, PCB with larger modulus is less compliant, and induces larger stress in the solder joints. The modulus of PCB material should be formulated according to the end applications.

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8.4 SUMMARY

Board level drop test, bend test, and thermal cycling test have been analyzed experimentally and numerically for a fine-pitch BGA CSP. The modeling results correlate well qualitatively with actual testing results for all the board level tests on failure mode, failure location, and failure interface of critical solder joint.

Package position on board is found to be critical for both drop and bend test but not significant for thermal cycling test. For drop test and bend test, packages located near PCB center are more likely to fail first under high stress, and the enhancement of underfill on solder joint reliability is less effective, compared with those away from the board center. As for thermal cycling test, use of underfill has large improvement on solder joint reliability regardless of package position on board.

Since the failure mechanism and locations are different for drop test, bend test, and thermal cycling tests, it is important to identify which test is more important for the package end application, and compromise in design is required.

Detailed solder joint reliability models are also established for IPD package under drop test and thermal cycling test. DNP effect is dominant for IPD structure under drop test and thermal cycling test. However, drop test performance is more dependent on PCB geometry, compared with thermal cycling test. It is found that both drop test and thermal cycling test performance can be enhanced by having square and thinner IPD. Design with stiffer PCB, helps to improve the drop test performance more than the thermal cycling fatigue life. However, design with smaller IPD size can have great improvement on reliability under thermal cycling test but relatively insignificant effect on drop test performance. IPD design with lead-free solder has better thermal cycling test performance but poorer reliability under drop impact. Solder material and PCB modulus have totally different effects under drop test and thermal cycling test.

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CHAPTER 9 CONCLUSIONS AND RECOMMENDATIONS

9.1 CONCLUSIONS

The objectives of the thesis have been achieved successfully through extensive research work. Various types of package and board level reliability models are established for virtual prototyping of advanced CSPs, e.g., TFBGA, QFN, and WL-CSP, which are used in telecommunication applications. The original scope of research is even exceeded to consider more recent CSPs in the design analysis. The main contributions of this thesis research are on novel integrated package stress model using multiphysics approach and accurate solder joint fatigue life prediction models under board level thermal cycling test and drop test for CSPs. The modeling results correlate well with in-house reliability tests conducted. The validated models help electronic industry to save significant amount of cost, time, and manpower in performing the actual reliability tests for CSPs. In addition, the physics of failures (failure mechanism and failure mode) of these advanced IC packages are well understood, and the quality of products is enhanced through design for reliability. Comprehensive package and board design guidelines are provided for these CSPs under various reliability tests.

The actual CSP package failure mechanism during reflow is complex, contributed by combined effects of process defects, interfacial adhesion strength, moisture, vapor pressure, thermo-mechanical stress, and hygro-mechanical stress. Therefore, there is a need for comprehensive multiphysics studies on moisture diffusion, thermal, hygro-mechanical stress, thermo-mechanical stress, and vapor pressure modeling. An integrated stress model with interfacial fracture mechanics is established to study the QFN package stress, and compute the strain energy release rate when delamination is initiated. It is an useful tool to analyze and enhance the reliability of package, minimizing the delamination and popcorn failures encountered during reflow.

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Detailed solder joint fatigue models with life prediction capability are established for various types of CSPs. Novel combined local/global geometry modeling methodology is created to reduce the computational time of 3D fatigue model from days to hours. Modified Darveaux's approach is applied with addition of unique correlation constants for life prediction of TFBGA, QFN, and WL-CSP package families. The correlation between the fatigue model and actual thermal cycling test is excellent on both failure location and number of cycles to failure. The relative fatigue life predictions and design trends are also consistent with experimental observations. Generally, for enhanced solder joint reliability of CSPs, it is recommended to choose smaller die size, thinner die, higher solder joint standoff, bigger solder pad opening size, and thinner board.

The same fatigue modeling methodology is also applied to investigate solder joint reliability of other CSPs which are getting popular recently, e.g., stacked die BGA, stacked die QFN (MEMS package), and thermally enhanced BGA package, under board level thermal cycling test. Certain design rules learned from single die CSPs may not be applicable for stacked die CSPs. The relationship between package warpage and solder joint fatigue life is also established.

Comprehensive drop tests, failure analyses, and simulations are performed on CSPs (TFBGA and QFN) at board level. The solder joint failure is induced by the combined stress of mechanical shock and PCB bending. The critical solder ball is observed to occur at the outermost corner solder joint, and fails along the solder and PCB pad interface under peeling mode. Normal peeling stress is confirmed as the major stress component of solder joint, and the PCB cyclic bending or vibration fatigue is the main failure mechanism of solder joints during drop impact. This failure mechanism and location of critical solder joint are supported by same observations in both drop test and

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simulation. For the first time, an accurate life prediction model is established for board level drop test to estimate the number of drops to failure for a package. For the correlation cases studied, the maximum normal peeling stresses of critical solder joints correlate well with the impact lives measured during the drop test, within uncertainty of ±4 drops, for a typical test of 50 drops. With this new model, a failure-free state can be determined, and drop test performance of new package design can be quantified, and further enhanced through modeling. This quantitative approach is different from traditional qualitative modeling, as it provides both accurate relative and absolute impact life prediction.

In addition, integrated board level drop test and thermal cycling test have been analyzed for CSPs. Package position on board is found to be critical for drop test but not significant for thermal cycling test. Besides, lead-free solder is found to be useful for thermal cycling test but degrade the performance in drop test. Since the failure mechanism and failure mode are different for drop test and thermal cycling test, it is important to identify which test is more important for the package end application, and compromise in design is required. For telecommunication application, drop test is more critical than thermal cycling test.

IC packaging has evolved towards "4-Dimensional" packaging, i.e. design of the cheapest and most reliable package in the shortest time possible. Traditional design-build-test-redesign type of package development cycle is no longer efficient for competitive semiconductor and telecommunication industries which emphasize on short time-to-market. Design for reliability using modeling is the key element for success in new package development of CSPs.

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9.2 RECOMMENDATIONS

Recommendations for future work include further studies in the following areas:

1) Conduct JEDEC moisture sensitivity test for CSPs and correlate the results with integrated package stress model.
2) Measure interfacial fracture toughness of various materials, e.g. leadframe/mold compound, die/underfill, and substrate/mold compound, to establish an accurate predictive popcorn model.
3) Measure temperature-dependent CME for hygroswelling modeling, using only one pair of samples to minimize the material characterization time.
4) Consider mass "convection" type of boundary condition for moisture diffusion modeling by performing detailed moisture weight gain measurements at both material and package levels.
5) Perform viscoelastic warpage modeling of CSPs, especially for matrix BGA, as it is a main concern for manufacturability.
6) Consider non-uniform temperature distribution during thermal cycling fatigue modeling using coupled thermal and mechanical simulation.
7) Perform solder joint fatigue modeling under board level bend test, comparing failure mechanism and failure mode with thermal cycling test and drop test.
8) Establish vibrational fatigue model with modal analysis and spectrum analysis for drop test.
9) Consider strain rate-dependent material properties of solder joints under impact using Hopkinson bar test.
10) Extend the package and board level modeling analysis to other latest CSPs, e.g. multi-chip BGA module, as well as perform design optimization.

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APPENDIX

DESCRIPTION OF ANAND'S MODEL [79]

Since solder is above half of its melting point at room temperature, creep processes are expected to dominate the deformation kinetics. Steady-state creep of solder can be described by Eq. (2.11). Steady-state creep is not generally achieved immediately when stress is applied. A certain amount of transient creep occurs before attaining steady state. Transient creep at constant stress and temperature can be described by

$$\varepsilon_c = \frac{d\varepsilon_s}{dt}t + \varepsilon_T(1 - \exp(-B\frac{d\varepsilon_s}{dt}t)) \qquad \text{(A.1)}$$

where ε_c is the creep strain, $d\varepsilon_s/dt$ is the steady-state creep rate, ε_T is the transient creep strain, and B is the transient creep coefficient. The following strain hardening law can be used to describe high stress deformation

$$\varepsilon_p = C_p\left(\frac{\sigma}{G}\right)^{m_p} \qquad \text{(A.2)}$$

where ε_p is the time-independent plastic strain, G is the shear modulus, and C_p and m_p are constants. The total inelastic strain is given by the sum of creep strain and plastic strain

$$\varepsilon_{in} = \varepsilon_c + \varepsilon_p \qquad \text{(A.3)}$$

Eqs. (2.11), (A.1), (A.2), and (A.3) can fit the deformation behavior of eutectic solder. The material constants were characterized [77]. Unfortunately, these relations are not available in ANSYS software as standard subroutine. However, it is possible to input user-defined constitutive relations in most codes.

ANSYS does have viscoplastic elements as a standard option using Anand's model [140]. The use of these elements is convenient since the user does not have to modify

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the source code. Anand's model is broken down into a flow equation and three evolution equations:

Flow Equation

$$\frac{d\varepsilon_p}{dt} = A\left[\sinh(\xi\sigma / s\right]^{1/m} \exp\left(\frac{-Q}{kT}\right) \tag{A.4}$$

Evolution Equations

$$\frac{ds}{dt} = \left\{h_o\left(|B|\right)^a \frac{B}{|B|}\right\}\frac{d\varepsilon_p}{dt} \tag{A.5}$$

$$B = 1 - \frac{s}{s^*} \tag{A.6}$$

$$s^* = s\wedge\left[\frac{d\varepsilon_p / dt}{A}\exp\left(\frac{Q}{kT}\right)\right]^n \tag{A.7}$$

where the material constants in the equations above are listed in Table A.1. These nine constants can be input directly into ANSYS built-in user subroutine for Anand's model to perform creep or viscoplastic modeling of solder joints fatigue.

Table A.1. Anand's model constants for ANSYS (eutectic solder)

ANSYS Input	Constants	Values	Definitions
C1	S_o	1800	Initial value of deformation resistance
C2	Q/k	9400	Activation energy / Boltzmann's constant
C3	A	4.0E6	Pre-exponential factor
C4	ξ	1.5	Multiplier of stress
C5	m	0.303	Strain rate sensitivity of stress
C6	h_o	2.0E5	Hardening constant
C7	s^	2.0E3	Coefficient for deformation resistance
C8	n	0.07	Strain rate sensitivity of deformation resistance
C9	A	1.3	Strain rate sensitivity of hardening