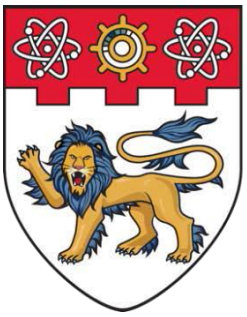

NANYANG TECHNOLOGICAL UNIVERSITY
SINGAPORE

DESIGN OF A POWER MANAGEMENT UNIT FOR A WIRELESS-POWER-TRANSFER-ENABLED WIRELESS SENSOR NODE

LUO HAO

SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

2019

DESIGN OF A POWER MANAGEMENT UNIT FOR A WIRELESS-POWER-TRANSFER-ENABLED WIRELESS SENSOR NODE

LUO HAO

School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

2019

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

29/07/2019

[Date Here]

[Student's Signature Here]

. . 29/07/2019. . . . . .

Date

. . . . . Luo Hao. . .. .

[Student's Name Here]

Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

[Date Here]	[Supervisor's Signature Here]
29/8/19	Liter Sick
Date	[Supervisor's Name Here]

Authorship Attribution Statement

This thesis contains material from 3 paper(s) published or to be published in the following peer-reviewed journal(s) where I was the first and/or corresponding author.

Chapter 3 is submitted for publication as H. Luo, and L. Siek, “A 0.7-V Supply-insensitive ΔV_{th}-based CMOS Voltage Reference with Proposed Trimming and Curvature-Compensation Techniques”, IEEE J. Solid-State Circuits, 2019 (submitted)

The contributions of the co-authors are as follows:

- A/Prof Siek Liter provided the initial project direction and edited the manuscript drafts.
- I prepared the manuscript drafts. The manuscript was revised by Dr Siek Liter.
- I designed the study and performed all the laboratory work at the School of Electrical and Electronic Engineering. I also analyzed the data.
- All topology development, schematic drawing, simulation, layout drawing, PCB design and testing were conducted by me in VIRTUS, IC Design Centre of Excellence.

Chapter 4 is to be submitted for publication as H. Luo, and L. Siek, “A 0.8-V Output-Capacitor-less Low Dropout Voltage Regulator Based on Load-Adaptive Negative-Resistance”, IEEE J. Solid-State Circuits, 2020 (to submit after all measurement results collected).

The contributions of the co-authors are as follows:

- A/Prof Siek Liter provided the initial project direction and edited the manuscript drafts.
- I prepared the manuscript drafts. The manuscript was revised by Dr Siek Liter.

- I designed the study and performed all the laboratory work at the School of Electrical and Electronic Engineering. I also analyzed the data.
- All topology development, schematic drawing, simulation, layout drawing, PCB design and testing were conducted by me in VIRTUS, IC Design Centre of Excellence.

Chapter 5 is published as H. Luo and L. Siek, "A 0.9-V input PWM DCM boost converter with low output ripples and fast load transient response based on a novel square-root voltage mode (SRVM) control approach," IEEE International Symposium on Circuits and Systems (ISCAS), 2017

The contributions of the co-authors are as follows:

- A/Prof Siek Liter provided the initial project direction and edited the manuscript drafts.
- I prepared the manuscript drafts. The manuscript was revised by Dr Siek Liter.
- I designed the study and performed all the laboratory work at the School of Electrical and Electronic Engineering. I also analyzed the data.
- All topology development, schematic drawing, simulation were conducted by me in VIRTUS, IC Design Centre of Excellence.

29/07/2019

[Date Here] [Student's Signature Here]

. . . 29/07/2019. . . . . Luo Hao. . . . . .

Date [Student's Name Here]

Acknowledgements

I would like to express my gratitude to A/Prof Siek Liter for offering me the opportunities of this PhD studies as well as the sponsorship from Broadcom Inc. for supporting my expenses and monthly stipends during the studies. The initial direction offered by A/Prof Siek Liter helped me to find the inspiration on the work developed in this thesis and interested me in conducting the work despite various obstacles encountered through the process. A/Prof Siek's support in component procurement, PCB fabrication and PCB assembly also help me set up the testing environment smoothly for the IC chips that I designed. In addition, yearly consultation and review of my research process by Broadcom colleagues also helped me refine my idea and let the concept mature.

Also, I would also thank our laboratory managers Ms Lim-Tan Gek Eng, Mr David Robert Neubronner, and Ms Quek-Gan Siew Kim for their consistent support and patience in helping me secure the testing equipment, processing POs and accepting deliveries while I was absence from the laboratory due to work. Without their help, much more time and effort will have to be spent in dealing with these works on my own.

Table of Contents

Abstract

Wireless Sensor Network (WSN) is one of the supporting technologies for the Internet of Things (IoT). However, a large-scale deployment of the WSN faces multifarious challenges. WSN node size and maintenance cost incurred by periodic energy source replacement are among them. From the perspectives of energy sources, these two challenges can be better addressed by Wireless Power Transfer (WPT) technologies in comparison with energy-scavengers or traditional energy-storages. Omnidirectional-Electro-Magnetic (EM)-Radiation WPT-technology appears to be a viable choice. Hence, this work proposes various circuit design techniques in developing the dedicated Power Management Integrated Circuit (PMIC) structures to facilitate implementation of such WPT technology.

In detail, this thesis describes (i) a sub-1-V CMOS Voltage Reference (VR) with novel trimming networks, (ii) a Capacitor-Less (OCL) Low Drop-Out Voltage Regulator (LDO) with load-adaptive negative-resistance at the input stage of an Operational Transconductance Amplifier (OTA), and (iii) a compensator-less Square Root Voltage Mode (SRVM) controller for a Pulse Width Modulation (PWM) Discontinuous Current Mode (DCM) Boost DC-DC Converter. To elaborate, the trimming networks aim at minimizing Temperature Coefficient (TC) against process variations and the finite resistance of the CMOS trimming switches in a CMOS Voltage Reference (VR). The load-adaptive negative-resistance helps to boost the DC-gain of the proposed OCL-LDO while improving the current efficiency and ensuring fast-settling and frequency stability. Lastly, the compensator-less SRVM controller is designed to minimize power and area from the discrete compensator circuits in conventional DC-DC converters.

Subsequently, structures of three key PMIC building blocks, such as a VR, an OCL-LDO and a boost DC-DC switching converter, are proposed with the aforementioned circuit design techniques. Trimming networks are proposed for a sub-1-volt CMOS VR implemented using the threshold-voltage-difference (ΔV_{th}) approach. Fabricated in 0.18-µm CMOS-technology, the trimmed CMOS VR consumes 0.4 µA with a supply voltage of 0.7 V. A TC of 45 ppm/°C and a

Power Supply Rejection (PSR) greater than -55 dB up to 10 MHz. The trimmed VR can also operate under supply voltages from 0.7 V to 1.5 V and operating temperature range from -40 °C to 80 °C.

A fast-settling OCL-LDO enhanced by a load-adaptive negative-resistance is proposed. Such load-adaptive negative-resistance resides at the EA input-stage, which incorporates a Partial-Positive-Feedback (PPF). No compensation capacitors is needed for frequency stability as a result. The overall OCL-LDO is manufactured in 0.18-µm CMOS-technology. It achieves a fast settling-time of 2.99 µs and 2.05 µs against a load step-up and –down respectively between 30 mA and 80 mA in 100 ns. The OCL LDO functions under supply voltages from 0.8 V to 1.5V. It consumes quiescent current of no more than 21 µA under no-load condition; it can source as much as 80 mA to the loading ICs.

In addition, a compensator-less PWM Boost DC-DC converter in DCM based on a SRVM controller is also proposed. The SRVM controller achieves voltage regulation by implementing analog-signal-processing unit to sense the load current and convert it into a PWM voltage-control-signals to drive the power switches. The block-level design of the proposed Boost DC-DC converter is simulated in MATLAB. It achieves output ripples of 0.42% of its steady-state output of 3 V. Output overshoots of 3 mV with 4-µs recovery-time are observed during step-down load-transients from 40 mA to 0 mA in 100 ns. Correspondingly, output undershoots during step-up load-transients are less than 10.8 mV with recovery-time of 8.9 µs. The boost converter can start up from a 0.9-V input autonomously based on a proposed two-phase start-up control-scheme. On top of this, a novel signal-boosting-technique is presented to ensure gate-driving voltages for MOSFET switches as high as attainable to minimize conduction losses. At the steady-state, the boost converter operates with a fixed 1-MHz switching-frequency with a 1-µH inductor and a 10-µF capacitor to source load current up to 40 mA.

All the proposed designs achieve supply- and load-independence as well as power- and area-efficiency in addressing the unique PMIC design challenges dedicated to the Omnidirectional-EM-Radiation WPT.

List of Figures

List of Tables

Chapter 1 Introduction

The Internet of Things (IoT) emerged from the need to share information in real time among computers for logistics management in 1999 [1]. The word “Internet” means the network to link autonomous objects or “Things”, such as computers, which share real-time information; and “things” refers to the elements that build up the information infrastructure. These elements are uniquely addressable; and they communicate among one another. In turn, such communication is supported by standards and protocols established by a network infrastructure. Simply put, IoT is an incorporation of the information and the network infrastructure.

During the implementation, the concept have evolved and described in various versions [2, 3]. It is also assessed from various perspectives [4-6]. Nonetheless, the consensus on IoT paradigm, at present, is an Internet-enabled network that facilitates knowledge integration by linking any objects in the physical, virtual and digital world. Alternatively speaking, knowledge from each linked objected is integrated via the Internet through interactions, which involve “identification, sensing, storage, actuating and other interfacing activities”. [2] To materialize these activities for practical use, supporting technologies have to be explored and studied.

1.1 Motivation

Wireless Sensor Network (WSN) is one of the supporting technologies for IoT implementation. It facilitates IoT by forming a constellation of wirelessly interconnected nodes. As a network of smart “things” with various dedicated functionalities, these nodes become the IoT information infrastructure. Specifically, a node that senses is a sensor node; a node that exchanges data with external networks is a sink node; a node that relays data is a router [2]. In this manner, this network of wireless nodes can realize multifarious IoT-related applications through peer-to-peer interactions.

The many fields of WSN applications are summarized in a tree diagram in

Figure 1.1. They can be categorized as either remote-tracking or remote-monitoring by functionalities. To differentiate the two categories from one another, remote-tracking relies on real-time interaction among the nodes, while remote-monitoring interrogates environment information periodically when invoked and stays in the standby mode otherwise. In either category, the WSN applications can be classified even further based on their indoor or outdoor implementations. [2]

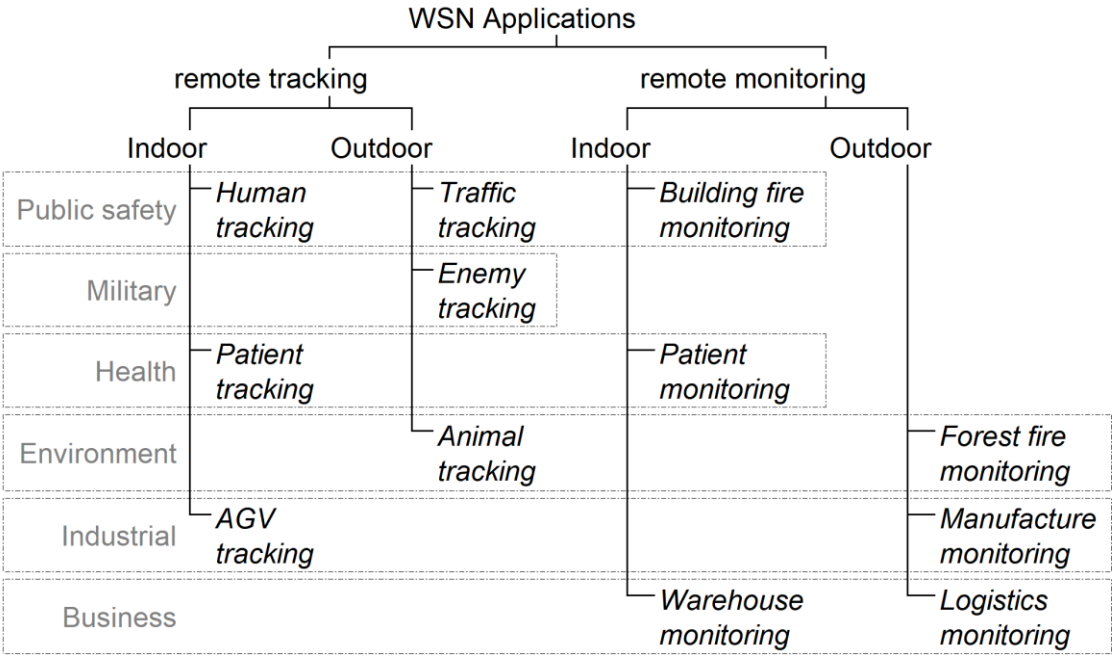

Figure 1.1 Summary of WSN applications [2].

To support the various applications summarized in Figure 1.1, the WSN sensor node is often built exclusively for its dedicated application. Nonetheless, it usually includes functional blocks, such as sensor, Analog-to-Digital Converter (ADC), microprocessor (µP), memory and Radio Frequency (RF) Transceivers, as grouped and labelled as “load” in Figure 1.2. In detail, a sensor acquires data from the environment. Depending on each application, it can be a light sensor, a temperature sensor, an accelerometer and so on. The sensor data is then digitalized through ADC and fed to the µP for analysis. The µP then formats the data and sends the data through the RF transceiver to a router or a sink node (also called base station). Alternatively, the RF transceiver also receives commands or data from a router or sink node and passes them to the µP. Such commands can be instructions to activate or deactivate the sensor for power

conservation purposes. They can also be request for data to the sensor node from its peers of the same WSN. Memories often operate together with the µP for arithmetic operations or data storage.

Such functional blocks within a sensor nodes are often considered loads to the Power Management Unit (PMU), which includes the Low Drop-Out voltage regulator (LDO), the Voltage Reference (VR) and the DC-DC Converter (DC-DC), as shown in Figure 1.2. The PMU functions to regulate its output voltage to meet the supply demand from its loads, such as sensor, µP, RF transceiver and memory. The PMU is often fed by the energy source, which can be energy harvesters, batteries and so on.

However, to deploy WSN applications, it is not without challenges. Major challenges can be summed up in the following as: 1) energy efficiency, 2) interference, 3) security, 4) data management, and 5) large-scale deployment. Detailed elaboration on each of these challenges can be found in [2]. Take the large-scale deployment for an instance. To effectuate WSN applications, a large amount of WSN sensor nodes over a large region are often inevitable. Consider the WSN deployed to monitor forest fire or earthquake. Wirelessly-networked sensors have to be spread out over a large geographical area as far as 1 km [7], for temperature or seismic data collection. Besides, relatively high node-density is required to ensure concerned events being detected with a suitable probability of success while maintaining a low probability of false alarm [8].

Yet, contradictions between node-size and cost hinders the large-scale deployment of WSN. On the one hand, small node-size demands small batteries to deploy sensor nodes in a large volume, but also ends up with low energy-capacity and short lifetime. This results in frequent battery-replacement, increased maintenance-cost and human-effort. On the other hand, to cut cost, a bulky battery may be desirable as it promises a long lifetime and avoids the costly maintenance. However, the large node-size resulted forbids the sensor nodes from being mounted at awkward locations, making it less ubiquitous [9].

In search of feasible power sources to enable WSN applications, [10] compares various power-source options in TABLE 1.1. Detailed descriptions on

these power sources are described in [10]. Primary and secondary batteries are exemplified by batteries for their relatively-large energy-densities.

TABLE 1.1 COMPARISON AMONG POWER SOURCES FOR WSN [10, 11]

	Power Source	Power Density ($\mu W/cm^3$)	Energy Density (J/cm^3)	Need for Secondary Storage	Need for Voltage Regulation	Commercial Availability
Energy-storage	Primary Battery	-	2880	No	No	Yes
	Secondary Battery	-	1080	-	No	Yes
	Micro-Fuel cell	-	3500	Maybe	Maybe	No
	Ultra-capacitor	-	50-100	No	Yes	Yes
	Heat Engine	-	3346	Yes	Yes	No
	Radioactive (^{63}Ni)	-	1640	Yes	Yes	No
Energy Scavenging	Solar Light	15000 [a]	-	Usually	Maybe	Yes
	Luminance Light	10 [a]	-	Usually	Maybe	Yes
	Thermal	40 [a,b]	-	Usually	Maybe	Soon
	Human Power	330	-	Yes	Yes	No
	Wind / Air Flow	380 [c]	-	Yes	Yes	No
	Pressure Variation	17 [d]	-	Yes	Yes	No
	Vibration	300	-	Yes	Yes	No
	Electro-Magnetism	< 60	-	Yes	Yes	No

a. The fundamental metric is $\mu W/cm^2$ rather than $\mu W/cm^3$.

b. The test result is based on a 5°C temperature differential.

c. Air velocity of 5 m/s and 5% conversion efficiency is assumed.

d. The test result is based on a 1 cm^3 closed volume of helium undergoing a 10 °C temperature change once per day.

Note that power-densities for energy-storage power-sources are deliberately ignored as they vary over time and offer little insights when relating their lifetime to their physical dimensions. Instead, energy-densities are quoted in TABLE 1.1. Apparently, high energy-densities are preferred under size-constraints as they increase the lifetime and extend replacement cycles. Hence, maintenance cost is lowered. Conversely, given identical energy-demand, they result in small node-sizes by assuming a fixed replacement-frequency. For an instance, micro-fuel cells and heat engines exhibit higher energy-densities than batteries. Such advantages render them seemingly more favorable than batteries. However, the complex conversion-process from thermal energy to electricity makes neither of them feasible energy-sources in small scales. Neither do radioactive materials, such as ^{63}Ni. They still require further research work to become available commercially. Moreover, the low energy-density of

typical ultra-capacitors makes them less attractive either. Despite recent development in compact and long-lifetime supercapacitors, such as Maxwell BCAP350 reported in [12], implementations for practical use is still rare due to the absence of dedicated and complex charging circuits. [12]

Alternatively, power sources generated by energy-scavengers in TABLE 1.1 reduce replacement cost when complemented with secondary or rechargeable batteries. Secondary batteries are generally required to store the harvested energy to budget for future consumption. This is due to the fact that energy scavenged from the environment is not always adequate instantaneously to drive node operations. This is due to the unpredictability from the environment. For an instance, the power harvested by solar-energy scavengers or solar panels, despite their high power-density, varies in daytime, weather, climate or even at the location where they are installed. Such variations can bring down the average power-density to be substantially lower than 15000 W/cm^2 shown in TABLE 1.1. In addition, the solar-energy-scavenger approach is suitable for outdoor implementations only.

Other types of energy-scavengers in TABLE 1.1 usually derive very low power-densities. Consider the electro-magnetism scavenger or Radio Frequency (RF) energy-scavenger. In between 25 m to 100 m, power densities derived by scavenging RF energy from a base station for Global System for Mobile communications (GSM) 900 are between 0.001 to 0.1 W/cm^2. Within the same distance, power densities integrated over the downlink band (935 to 960 MHz) are between 0.01 to 0.3 W/cm^2. Similarly, power densities obtained from GSM1800 are as low as those from GSM900. As a result, an antenna-area of 330 to 1000 cm^2 will be necessary to obtain incident RF-power of 0.1 mW based on measurement results. By taking into account the antenna-to-rectifier impedance-mismatch, the RF-to-dc conversion, and the rectifier-to-load impedance-mismatch, the predictable net-RF-power scavenged will be even smaller. [13] The relatively large antenna-size with limited RF-power scavenged makes such techniques incompetent. This is the case for the rest of the energy-scavengers listed in TABLE 1.1 also.

Fortunately, the deficiency in the RF-energy scavenged from the

environment may be improved by employing a dedicated RF-energy-radiator to power up the nearby sensor-node based on the same working principle of RF-energy scavengers. Such is the idea of Wireless Power Transfer (WPT). Indeed, the idea of WPT had been proposed and proved by Nicolas Tesla since 1900s. Since 1980s, several methods have been demonstrated [14], such as: 1) Inductive coupling, 2) Electro-Magnetic (EM) radiation, 3) magnetic resonant coupling, and 4) laser beam [15]. At present, WPT technologies [15] that support WSN applications can be summarized in TABLE 1.2.

TABLE 1.2 COMPARISON BETWEEN WSN-FRIENDLY WPT TECHNOLOGIES [15]

WPT Technology	Strengths	Weaknesses	Application Examples
Omnidirectional-EM-Radiation	Tiny receiver size	Decrease in efficiency over distance resulting in low-power reception	WSN for environmental monitoring
Magnetic Resonant Coupling	High efficiency over several meters	High efficiency only within several meters	Chargers for mobile devices and cars, implantable devices and WSNs

Despite the fact that both WPT technologies listed in TABLE 1.2 suffer from low-power reception due to efficiency drop over distances, the RF-power attainable via WPT is still considered more reliable than it being attained by energy scavenging. This is mostly attributed to the predictability and controllability of the power beamed to the node via WPT. In comparison with the RF-power scavenger, WPT approach can derive higher power-densities. Furthermore, it applies to a wider range of WSN applications when compared with solar scavengers as it facilitates both indoor and outdoor implementations.

In addition, the “tiny receiver size” enabled by the Omnidirectional-EM-Radiation WPT technology reduces manufacturing cost and makes it ideal to implement sensor nodes in a large volume. Specifically, the effective Receiving Antenna (Rx Antenna) area is estimated to be in the range of 10 to 50 cm^2 according to [13]. Such area-size corresponds to the Industrial, Scientific, Medical (ISM) operating-frequency-band of 2.45 GHz. The 2.45-GHz frequency-band is opted for EM-radiation WPT [16] as such frequency-band is internationally usable when compared with the regionally-usable lower ISM

frequency-bands, such as 868 MHz or 915 MHz [7]. In addition, higher frequencies also indicate higher data-rate and less frame-transmission time, less microcontroller idle-time, resulting in decreased overall energy consumption by the node [7].

Shown in Figure 1.2 is a hypothetical structure of a WSN sensor node powered through Omnidirectional-EM-Radiation WPT. A power source drives the Transmitting Antenna (Tx Antenna) that radiates EM power omnidirectionally. In case WSN applications are to be deployed over a large outdoor area, one or more of such power sources can be equipped with solar panels according to [17]. The rectenna, which is the acronym for “rectifying antenna”, at the front end of the WSN sensor node captures the radiated EM power and rectifies it from Alternating Current (AC) to Direct Current (DC). By following the definition in [13], the rectenna involves an Rx Antenna, an impedance matching network, and a rectifier. For the convenience of addressing design challenges in the DC domain as a whole, the boundary of the PMU in this research is delimited by grouping LDO, DC-DC and VR together while excluding the rectenna, the rechargeable battery and the charging circuit.

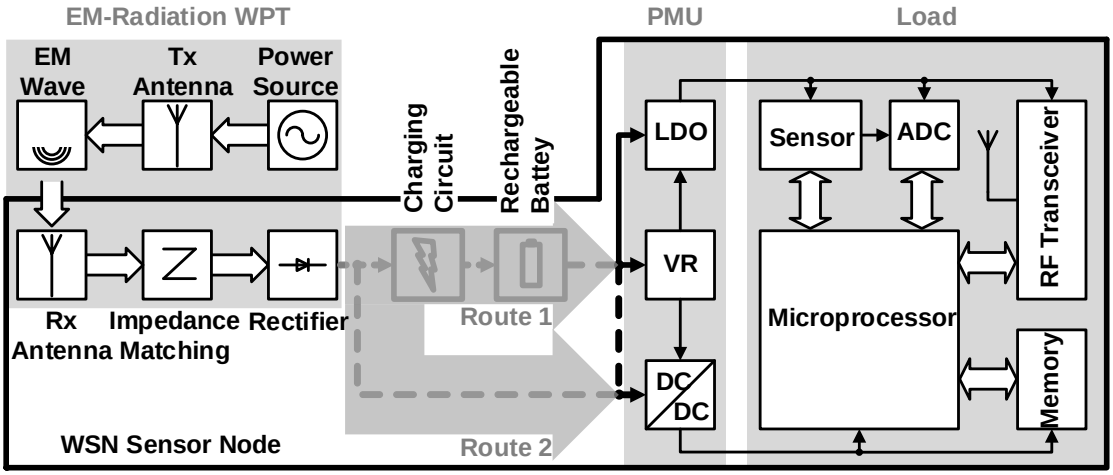

Figure 1.2 Block diagram of a WSN sensor node powered through Omnidirectional-EM-radiation WPT [12, 13].

Subject to the amount of power received, rectified power from the rectenna may be directed through Route 1 or Route 2 as shown in Figure 1.2. Route 1 is configured for a battery-equipped WSN sensor node, where incident RF power acquired through WPT is insufficient to support all node operations; whereas

Route 2 is for a battery-less WSN sensor node, where incident RF power acquired is sufficient or all intended node operations. Factors that determine whether Route 1 or 2 should be adopted will be reviewed in detail in Chapter 2.

From the hardware-design perspective, various performance requirements arise in developing PMU components for the two different types of node structures. In a battery-equipped node, the secondary battery exists to store the captured power and budget for future use. Indeed, such node-structure is similar to that adopted in the case of the RF-energy-scavenger power-source. Such structure may find its applications in patient- or logistics-monitoring listed in Figure 1.1. Under such scenario, the Dynamic Power Management (DPM) scheme [18] has to be employed to conserve energy. The main design challenge upon the PMU components, such as the LDO and the DC-DC converter, lies in the load-transient performance. To avoid malfunctions from loading ICs, it is critical to maintain stable supplies from the PMU with fast recovery to their nominal values upon sudden surge and decline of the load currents. The sudden load changes occur during mode-switching activities dictated by the DPM scheme.

On the contrary, a battery-less node can be necessitated by WSN applications for environmental monitoring on forest fire or seismic events, where periodic battery replacement is inconvenient or costly. By removing the battery, the PMU now have to regulate and condition the rectifier output directly to drive the loading ICs. In this case, good line-regulation and PSR performances are essential. This is due to: 1) the noisy and rippled rectifier output that is fed as the PMU input; 2) the noise-sensitive mixed-signal load, such as ADC, as well as the RF load, such as the RF transceiver, which all demand clean power supply to function properly.

1.2 Objectives

This work focuses on investigating the feasibilities to design a PMU that enables a WSN sensor node, be it battery-less or battery-equipped, powered by the Omnidirectional-EM-Radiation WPT. Objectives of the design work should involve the following features in specific.

1) Line Regulation

Supply independence is needed for both VR and LDO, be it battery-less or battery-equipped node. In case of a battery-less node, both VR and LDO are to maintain a steady supply or reference voltage when driven by the rectenna output that is fluctuating in both frequency and time domains.

For a battery-equipped node, the output of the secondary battery declines while it is being depleted. Besides, to ensure consistent performance, sub-1-V operability is desirable as the battery output might continue to drop below 1 V before enough wireless energy is received to charge it up.

Overall, good line regulation and fast line transient response down to sub-1-V are critical for both VR and LDO to regulate a fluctuating rectenna output or declining battery output. In addition, high PSR is also beneficial to the noise-sensitive loading-ICs, such as ADC and RF transceivers.

2) Load Regulation

Moreover, good load regulation and fast load transient response is critical to ensure steady performances for the LDO and the boost DC-DC converter in case of a battery-equipped node. This is due the DPM scheme that selectively turns on or off load components to conserve power. Known as mode switching, it causes the overall load current at the output of the PMU to vary in a very short instant.

It is essential to clarify that this research work concentrates on hardware technology to deploy WSNs by addressing power-management-related challenges. Also, it is assumed that challenges are very well addressed from other aspects, such as DPM scheme, physical layer design, signal processing algorithm, Medium Access Control (MAC), network structure, and communication protocol [8, 19-22].

3) Area and Power Efficiency

Furthermore, to facilitate large-scale deployment of WSN sensor nodes, a small

node size is advantageous. Within a PMU, the DC-DC converter often occupies the largest physical size. The compensator-based Pulse Width Modulation (PWM) controller is one of the main area- and power-consumers in a conventional DC-DC converter. Hence, a compensator-less boost DC-DC converter that offers comparable performance with its conventional counterparts can improve both power- and area- efficiency.

Moreover, by focusing on removing the compensator in the boost DC-DC, this work aims at addressing one of the main power and area consumers. Despite that a compensator-less boost DC-DC converter alone is sufficient to drive loads within a battery-less node, it will be incomplete for a battery-equipped node due to the lack of battery charging circuitries. A complete boost DC-DC converter for a battery-equipped WSN sensor node should embody a Multiple Inputs and Multiple Output (MIMO) structure. However, such structure will digress from the focus of this work.

1.3 Major Contribution of the Thesis

In this manner, the contributions of this research work revolve around the development of the PMU for a WSN sensor node that is powered through Omnidirectional-EM-Radiation WPT. Specifically, it is arranged in the following steps:

1) investigation and development of the circuit structure of a sub-1-V supply-independent low-power VR that is powered by a fluctuating rectenna output,
2) investigation and development of the circuit structure of a sub-1-V LDO that exhibits fast-settling load-transient-responses in addition to supply-independence and high current-efficiency, and
3) investigation and development of the circuit structure of a boost DC-DC that is compensator-less with fast-settling load-transient-responses and small output-ripples.

1.4 Organization of the Thesis

The thesis is organized in six chapters. With background and motivation listed in Chapter 1. Chapter 2 covers the relevant literature reviews in developing the

design work proposed. The literature review is laid out based on the IC components designed in this work, such as VR, LDO and DC-DC converters. A short conclusion is given after reviewing each of these IC components with directions on the proposed work. At the end of Chapter 2, all literature reviewed are summarized.

Chapter 3 concentrates on the development of the proposed CMOS VR. Theoretical background on the ΔV_{th}-based BVR-like CMOS VR is first introduced. It is followed by further investigation into the deficiencies of the original theories. Practical solutions, such as trimming networks, curvature-compensation circuits and start-up circuits, are proposed afterwards. They are listed and explained sequentially. Discussions on simulation and measurement results ensue. Performances of the proposed design are also compared against previous works to highlight strengths and weakness of the proposed work. Conclusion is drawn at the end of the chapter.

Chapter 4 explores the proposed OCL-LDO in detail. Relevant works conducted previously on PPF-incorporated G_m-cell-based OTA are first introduced. This is followed by impeding challenges when such OTA is implemented as the EA for an OCL LDO. Proposed solutions, such as load-adaptive negative resistance, process-tracking circuits and bulk-biasing techniques, are given afterwards. They are listed and illustrated sequentially. Simulation and measurement results are presented afterwards with discussions attached. The chapter is concluded by comparing the performance of the proposed OCL-LDO against previously reported counterparts.

The proposed concept of a compensator-less boost converter is presented in Chapter 5. Based on the literature review done previously in Chapter 2, the proposed control technique is listed on the block level. In-depth mathematical analyses on the proposed SRVM controller is conducted as well. Due to time constraint, the concept is simulated on the block level with MATLAB only. The simulated performances of the proposed SRVM controller are illustrated in waveforms and discussed.

Chapter 6 concludes the thesis by reviewing briefly all proposed designs

to develop a WPT-powered PMU for WSN sensor nodes. Relevant future work are also suggested for continual development and refinement of the proposed designs.

Chapter 2 Literature Review

Preliminary investigations on the adequacy of the RF-power acquired via Omnidirectional-EM-Radiation WPT to support WSN node operations are first conducted. A thorough power assessment is conducted on each typical load components within the node individually as well as on the overall performance of various popular WSN sensor nodes. Subsequently, metrics derived from the overall power assessment is compared against the estimated RF-power attainable. This is done by observing the international safety standards on EM radiation and it is to justify the adequacy of the amount of RF-power acquired through Omnidirectional-EM-Radiation WPT. Moreover, metrics derived from individual power assessment is utilized to specify performance targets on the PMU design, which includes a VR, an LDO, and a boost DC-DC. These are followed by detailed studies on relevant circuit structures of the three PMU components from previous works. The chapter concludes by a discussion on the pros and cons of previous designs on VR, LDO and DC-DC in developing a dedicated PMU for WSN sensor nodes.

2.1 Power Assessment on a WSN Sensor Node

Be it battery-less or battery-equipped, a typical WSN sensor node entails four subsystems [2] to realize its dedicated application. They are, namely: 1) computation subsystem, 2) communication subsystem, 3) sensing subsystem, and 4) power supply subsystems. The μP and memories constitute the computing subsystem; RF transceivers, which are an acronym for RF transmitter and receiver, form the communication subsystem; sensor and ADC make up the sensing subsystem; the rectenna and PMU become the power-supply subsystem. This section looks into each of these key components as well as the overall WSN sensor node for power assessment.

2.1.1 Microprocessor

Assisted by its peripheral components, such as memories, the μP carries out two major tasks: 1) hardware control and coordination of sensing and

communication subsystems, 2) execution of various power management schemes, signal processing algorithms as well as network protocols [19]. It is the most power-hungry element in the computation subsystem [2] as well as one of the most power-hungry components among all loads within a WSN sensor node.

DPM scheme is usually implemented to conserve power. Under DPM, more than one operating modes are scheduled by μPs. They often include active, idle, and sleep modes [19]. According to [19], a popular high-end μP, such as Intel's StrongARM μP consumes around 400 mW when active and 50 mW when idle; and a low-end μP, such as Atmel's AVR microcontroller, consumes around 16.5 mW when active and 0.16 mW when asleep. In addition, current consumption by Atmel's AVR microcontroller is 8 mA when active, 3.2 mA when idle, and 0.103 mA when powered down according to [23].

Other methods to conserve power involve lowering the operating voltage [2] or the operating frequency [19] of the μP by trading the computation performance. For an instance, 32-bit or 64-bit μPs that run conventional Operating Systems (OS) in hundreds or thousands of MHz with MBs or GBs of memory is often reduced into 16-bit or 8-bit with tailored OS as listed in TABLE 2.1. Their operating frequencies are reduced to tens of a few MHz.

TABLE 2.1 SOME POPULAR WSN SENSOR NODES WITH THEIR MICROPROCESSORS [7]

Node	μP	Data Path	Operating Frequency	Operating Voltage
MICA2	ATmega128L	16-bit	8 MHz	2.7 V ~ 5.5 V
Telos	TI MSP430	16-bit	8 MHz	2.5 V ~ 5.5 V
MICAz	ATmega128L	16-bit	8 MHz	2.7 V ~ 5.5 V
ez430-RF2500	TI MSP430	16-bit	16 MHz	2.5 V ~ 5.5 V
WSN430	TI MSP430	16-bit	8 MHz	2.5 V ~ 5.5 V
VirtualSense	TI MSP430	16-bit	25 MHz	2.5 V ~ 5.5 V
Pinoccio	ATmega128RFA1	8-bit	16 MHz	1.8 V ~ 3.6 V

Moreover, as [24] suggests, higher operating voltages result in higher power consumptions, whereas reduced operating voltages will decrease the maximum allowable operating frequencies and, subsequently, slow down computations. Thus, a compromise exists between power consumption and

computation performance when selecting optimum operating voltages. By observing the operating voltages of the popular µPs listed in TABLE 2.1, 3 V can be a reasonable choice for setting the DC-DC converter output, which powers up the µP.

2.1.2 RF Transceiver

The RF transceivers of the communication subsystem facilitate information sharing between the neighbouring WSN nodes and the physical world. [2] The preferred frequency band is 2.4 GHz as it is internationally available. This is exemplified by RF transceivers in WSN nodes, such as Telos, MICAz, ez430-RF250, VirtualSense, and Pinoccio in TABLE 2.1. A communication protocol, ZigBee, which is built upon the IEEE 802.15.4 physical and Media Access Control (MAC) layers [7], supports such information sharing.

When in operation, the RF transceivers drain the largest amount of current among all loads within a WSN node [8]. Various factors can be adjusted to reduce power consumption. They involve: 1) modulation scheme, 2) data rate or bandwidth, 3) transmitting power or transmission range, and 4) operating duty cycle divided and allocated into transmit, receive, idle, and sleep modes of operations. [2] By leveraging on the shrinking transistor geometries, recent developments have demonstrated Ultra-Low-Power (ULP) RF transceivers [25] that operates under sub-1-V supplies to support operations within WSN nodes. Some are compiled in TABLE 2.2. Thus, 0.7 V can be a reasonable supply voltage to operate such RF transceivers when setting the LDO output within the PMU.

TABLE 2.2 SOME RECENT WORKS ON SUB-1-V RF TRANSCEIVER

	Transceiver	Supply Voltage	Carrier Frequency	Data Rate	Power Consumption
[26]	Receiver	0.7 V	2.4 GHz	1.0 Mb/s	180 pJ/b
[27]	Transmitter	0.7 V	2.4 GHz	1.0 Mb/s	440 pJ/b
[28]	Transceiver	0.6 V	5.8 GHz	2.5 Mb/s	45.2 pJ/b
[29]	Transceiver	0.8 V	2.4 GHz	5.0 Mb/s	1.22 nJ/b

2.1.3 Sensor and ADC

The sensing subsystem constitutes the “eyes and ears” of a WSN sensor node. Generally, three main power consumers are involved: 1) the sensor itself, which samples and transduces physical signals to electrical signals, 2) the signal conditioning circuits, 3) and the ADC. Nonetheless, power consumption of various sensors varies significantly as listed in TABLE 2.3. For an instance, a temperature sensor reported in [30] consumes current of 1.1 mA during transmit mode under supply voltage of 1 V.

TABLE 2.3 POWER CONSUMPTION COMPARISON AMONG SENSORS [19]

Type of Sensor	Typical Application	Amount of Power Consumed
Passive sensor	Temperature, seismic sensing	Negligible
Active sensor	Sonar ranger	Large
Array sensor	Imager	
Narrow field-of-view sensor	Cameras with pan-zoom-tilt	

Moreover, as illustrated in [31], most energy-efficient ADCs of low to moderate resolution operate under sub-1-V supplies. They are typical choices for low-power WSN sensor nodes [25]. Some recent works on sub-1-V ADCs are compiled in TABLE 2.4. Again, 0.7 V can be chosen as the supply voltage to operate such ADCs.

TABLE 2.4 SOME RECENT WORKS ON SUB-1-V ADC

	Type	Resolution	Speed	Supply Voltage	Power Consumption
[32]	Pipeline	8 bits	10 MS/s	0.5 V	2.4 mW
[33]	Pipeline	12 bits	5 to 50 MS/s	0.5 to 1 V	0.237 to 4.07 mW
[34]	SAR	8 bits	0.2 to 40 MS/s	0.3 to 0.8 V	-
[35]	SAR	12 bits	10 MS/s	0.6 V	83 μW
[36]	SAR	11 bits	100 KS/s	0.7 V	0.6 μW

2.1.4 Rectenna

A rectenna resides at the front end of a WSN sensor node. It is one of the key element in the power supply subsystem. It functions to capture the incident EM-power through WPT. Structurally, it is usually made of an Rx Antenna, an

impedance matching network and a rectifier.

1) Rx Antenna

As a result of EM radiation from the Tx Antenna, power density S at a charging distance r is derived by [13, 37]

$$S = \frac{P_T G_T}{4\pi r^2} = \frac{EIRP}{4\pi r^2}, \quad \textbf{(2.1)}$$

where P_T is the transmitted power, G_T is the Tx Antenna gain and $EIRP = P_T G_T$ stands for Effective Isotropic Radiated Power (EIRP) from the Tx Antenna.

Moreover, effective aperture A_e of the Rx Antenna can be given as [37]

$$A_e = \frac{\lambda^2}{4\pi} D_r, \quad \textbf{(2.2)}$$

where λ is the wavelength of the 2.45 GHz EM wave, D_r stands for the directivity of the Rx Antenna. As a result, the incident power P_r at the Rx Antenna can be obtained by combing Equations (2.1) and (2.2) as [37]

$$P_r = S \cdot A_e = EIRP \cdot \left(\frac{\lambda}{4\pi r^2}\right)^2 \cdot D_r. \quad \textbf{(2.3)}$$

Furthermore, by considering the efficiency of the receiving antenna η_{er}, the captured power by the Rx Antenna can be derived as the Friis transmission formula as [37]

$$P_r = S \cdot A_e = EIRP \cdot \left(\frac{\lambda}{4\pi r^2}\right)^2 \cdot G_r, \quad \textbf{(2.4)}$$

where $G_r = \eta_{er} D_r$ is the gain of the Rx Antenna.

2) Impedance Matching Network

The impedance matching network within a rectenna is to match the output impedance of the Rx Antenna to the input impedance of the rectifier. [37] It is to improve the matching efficiency η_Z between the Rx Antenna and the Rectifier and, subsequently, to improve the RF-to-DC conversion efficiency $\eta_{RF\text{-}DC}$ of the rectenna. With the impedance matching network implemented, the matching

efficiency η_Z can be expressed as [13]

$$\eta_Z = 1 - |\Gamma|^2, \tag{2.5}$$

where Γ is the power wave reflection coefficient and can be expressed as [13]

$$\Gamma = \frac{Z_{IN\_rec} - Z_{ant}^*}{Z_{IN\_rec} + Z_{ant}}, \tag{2.6}$$

where $Z_{ant}^* = Z_{IN\_rec}$ is the matched impedance of the Rx Antenna, Z_{ant} is the impedance of Rx Antenna (, with the typical impedance R_{ant} being 50 Ω), and Z_{IN_rec} is the input impedance of the rectifier as shown in Figure 2.1.

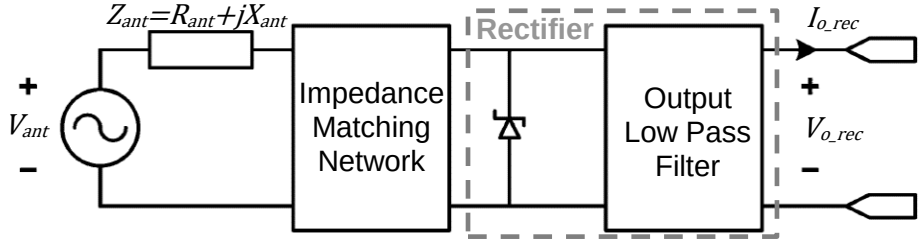

Figure 2.1 Block diagram of a typical rectenna [38].

Under the matched condition when $Z_{ant}^* = Z_{IN\_rec}$, by considering the antenna as a load to a transmission line [37], the received power P_r from the antenna delivered to the rectifier can be derived as

$$P_r = \frac{1}{2}\left(\frac{V_{ant}}{Z_{ant}^* + Z_{IN\_rec}}\right)^2 \cdot R_{ant} = \frac{V_{ant}^2}{8R_{ant}}. \tag{2.7}$$

Hence, the output voltage of the Rx antenna under the matched condition can be computed as

$$V_{ant} = 2\sqrt{2R_{ant}P_r}. \tag{2.8}$$

The accepted power by the rectifier at the rectifier input ports can be computed as

$$P_{acc\_rec} = \eta_Z P_r. \tag{2.9}$$

3) Rectifier

As demonstrated in [13], RF-to-DC conversion efficiency of a rectifier varies with respect to the load impedance of the rectifier is

$$\eta_{RF-DC} = \frac{P_{cap\_rec}}{P_{acc\_rec}} = \frac{V_{o\_rec}^2}{R_{L\_rec} P_{acc\_rec}}, \quad \textbf{(2.10)}$$

where P_{cap_rec} is the captured EM power by the rectenna, V_{o_rec} is the rectifier output and R_{L_rec} is the load impedance to the rectifier. As the rectifier output is often too low to drive loads, such as μPs or memories, a DC-DC converter is entailed to boost it to drive such loads. As $\eta_{\text{RF-DC}}$ varies with R_{L_rec}, an optimal R_{L_rec} that derives the highest η_{RF-DC} is advantageous. To do so, R_{L_rec} needs to be matched to the output of the rectifier.

Impedance matching for R_{L_rec} has to be achieved based on following considerations: 1) only slight variation exists in the amount of the incident EM power received at the Rx Antenna; 2) the captured EM power is relatively low and Discontinuous Conduction Mode (DCM) PWM control is sufficient for the DC-DC boost converter to drive the loads; 3) the rectenna can be modelled as an ideal DC source with a series resistance by designing it to operate within the first I-V quadrant shown in Figure 2.2 following the I-V relation as [38]

$$V_{o\_rec} = \frac{\pi}{4} V_{ant} - \frac{\pi^2}{8} Z_{ant} I_{o\_rec}, \quad \textbf{(2.11)}$$

where V_{o_rec} is the rectifier output voltage, I_{o_rec} is the rectifier output current, and V_{ant} is the antenna output voltage shown in Figure 2.1. In this manner, the Maximum Power Point (MPP) or the highest η_{RF-DC} occurs at the optimal load impedance [38]

$$R_{L\_rec,OP} = \frac{\pi^2}{8} R_{ant}. \quad \textbf{(2.12)}$$

In Figure 2.2, the I-V characteristics of a patch antenna is measured at three different incident EM power densities, as illustrated by the legends, against the corresponding emulated curves in the Cartesian coordinate quadrants. In the first quadrant, all measured curves exhibit relatively linear

relations between I_{o_rec} and V_{o_rec}, such that $R_{L\_rec} = \frac{V_{o\_rec}}{I_{O\_rec}}$. Thus, by matching the rectenna load resistance to $R_{L\_rec,OP}$, the allowed load current consumption I_{o_rec} and the resulted rectenna output V_{o_rec} can be automatically derived by Equation (2.11). However, as R_{L_rec} is represented differently in the battery-less sensor node from that in the battery-equipped sensor nodes, two possible matching implementations have to be considered at the rectenna output; and they have to be analyzed separately.

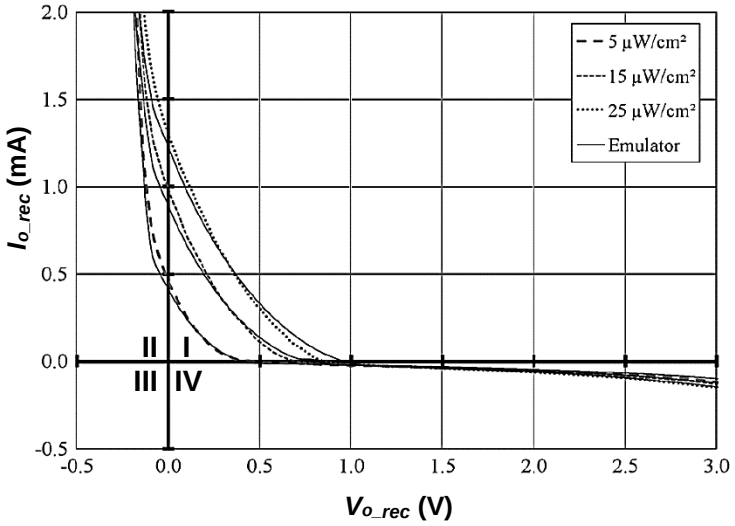

Figure 2.2 Experimentally measured I-V characteristics of a patch antenna [38].

For a battery-less sensor node, R_{L_rec} is the total input impedance of the DC-DC converter, LDO and VR. Two cases have to be considered for impedance matching at the rectenna output to maximize η_{RF-DC}:

- Case I: if the incident EM power P_r is kept constant by the power source driving the Tx antenna, V_{ant} will be constant with the impedance matching network implemented based on Equation (2.8). With $Z_{L\_rec,OP}$ determined by R_{ant} following Equation (2.12), V_{o_rec} and I_{o_rec} are both fixed based on Equation (2.11) and Ohm's law. To ensure constant load current consumption, power management schemes, such as DPM, can be employed and executed to turn on or off certain load components selectively upon various node operations. In case V_{o_rec} becomes too low to drive the PMU, voltage multiplication circuits can be implemented for the rectifier design to boost V_{o_rec}. This can be done by having several diodes connected

in cascade as demonstrated in [13]. Subsequently, dictated by Equations (2.11) and (2.12), R_{ant} and R_{L_rec} will have to be increased as well to ensure impedance matching at the rectenna output.

- Case II: if incident EM power P_r is adjustable by the power source that drives the Tx antenna, V_{ant} will vary according to Equation (2.8). With $R_{L\_rec,OP}$ determined by R_{ant} following Equation (2.12) and fixed, V_{o_rec} and I_{o_rec} will vary according to Equation (2.11) and Ohm's law. Such adjustability can be beneficial in terms of power saving such that I_{o_rec} can be lowered by lowering P_r when the node is idling. Additionally, it is worthwhile to note that a varying rectenna output voltage, V_{o_rec} , as determined by $V_{o\_rec} = I_{o\_rec}R_{L\_rec,OP}$, will entail a PMU with a good line regulation.

Next, for a battery-equipped WSN sensor node, R_{L_rec} becomes the input impedance of the charging circuit as illustrated in Figure 2.2. In this case, the incident EM power can be assumed constant since the captured EM power is too low to support node operation directly anyway. Therefore, η_{RF-DC} can be maximized by keeping constant the charging current to the secondary battery. However, with the secondary battery being the sole load component of the rectenna, the constant I_{o_rec} to maximize η_{RF-DC} can be in contradiction to the optimal charging current to maximize the charging efficiency of the secondary battery. Thus, a compromise between the charging efficiency and η_{RF-DC} will be inevitable. However, this is beyond the research scope of this work; and it will not be investigated in detail here.

2.1.5 PMU

In this work, the PMU consists of a DC-DC converter, an LDO, and a VR. It loads the rectenna; and it is another key component of the power supply subsystem. This section only assesses the power consumption of the PMU, whereas detailed circuit structures of each PMU component, such as DC-DC converter, LDO or VR, will be reviewed in the next sections.

1) DC-DC Converter

The power efficiency η_{DC-DC} of the DC-to-DC conversion varies with its input

power P_{in_DCDC}, which is a part of P_{cap_rec}. Hence, the output power P_{out_DCDC} of the DC-DC converter can be computed as

$$P_{out\_DCDC} = \eta_{DC-DC} P_{in\_DCDC} = V_{o\_DCDC} I_{o\_DCDC}, \quad \textbf{(2.13)}$$

where V_{o_DCDC} and I_{o_DCDC} are the output voltage and current of the DC-DC converter respectively. As a result, the load current I_{o_DCDC} facilitated by the DC-DC converter can be determined reversely by finding η_{DC-DC} and the available P_{in_DCDC}. With V_{o_DCDC} predetermined, it can be found that

$$I_{o\_DCDC} = \frac{\eta_{DC-DC} P_{in\_DCDC}}{V_{o\_DCDC}}. \quad \textbf{(2.14)}$$

Subsequently, for the case of a battery-less node, I_{o_DCDC} constitutes part of I_{o_rec}; for the case of a battery-equipped node, I_{o_DCDC} is supplied by the secondary battery.

2) LDO

Power efficiency η_{LDO} of the LDO can be expressed as [39]

$$\eta_{LDO} = \frac{I_{o\_LDO} V_{o\_LDO}}{(I_{o\_LDO} + I_Q) V_{IN}}, \quad \textbf{(2.15)}$$

where I_{o_LDO} is the LDO load current; V_{o_LDO} is the LDO output voltage; I_Q is the quiescent current dissipated within the LDO; and V_{IN} is the input voltage to the LDO. Therefore, for a WSN sensor node powered through WPT, $V_{IN} = V_{o\_rec}$. Similar to DC-DC converter, I_{o_LDO} constitutes part of I_{o_rec} for a battery-less node, whereas I_{o_LDO} is supplied by the secondary battery for a battery-equipped node.

As I_Q is usually kept small to minimize power loss, η_{LDO} can be simplified as

$$\eta_{LDO} \approx \frac{V_{IN} - V_{DO}}{V_{IN}}, \quad \textbf{(2.16)}$$

where $V_{DO} = V_{IN} - V_{o\_LDO}$ is the dropout voltage. Hence, a small V_{DO} will be beneficial to obtain a high η_{LDO} according to Equation (2.16).

Another parameter that is often considered is the current efficiency η_{I_LDO}, especially when minimum power consumption has to be determined. The minimum power consumption usually occurs when the loads are idling. Hence, it is useful in predicting battery lifetime for a battery-equipped node or the minimum power to be transferred through WPT for a battery-less node. Current efficiency η_{I_LDO} of an LDO can be expressed as [39]

$$\eta_{I\_LDO} = \frac{I_{o\_LDO}}{I_{o\_LDO}+I_Q}. \quad \textbf{(2.17)}$$

Moreover, in case of a battery-equipped node, the battery lifetime can be computed as [39]

$$\text{Life}[h] = \frac{\text{Capacity[Ah]}}{I_{\text{DRAIN(ave)}}} = \frac{\text{Capacity[Ah]}}{I_{o\_LDO}+I_Q+I_{o\_DCDC}+I_{VR}}, \quad \textbf{(2.18)}$$

where I_{VR} is the total current consumption of a VR and is usually constant under a given input voltage. As it is observable, when the node is idling and both I_{o_LDO} and I_{o_DCDC} are close to zero, I_Q becomes the total current drawn by the LDO. Hence, a smaller I_Q indicates a longer battery lifetime.

3) VR

As VR is usually not designed to drive loads, its total current consumption I_{VR} is the quiescent current consumed within the VR itself. Moreover, I_{VR} increases with the input voltage; and it is often minimized to save power.

2.1.6 WSN Sensor Node Overall

Due to the high cost of existing Commercial-Off-The-Shelf (COTS) solutions, WSNs are often developed in tailored version based on their dedicated applications. As a result, no standard solution to build a WSN sensor node as explained in [7].

Power profiles of various WSN sensor nodes are compiled in TABLE 2.5. Dictated by the DPM scheme, the node is only fully operational during the active mode when both µP and RF transceivers are on; during idle mode, power-hungry components, such as RF transmitters and the majority of µP operations,

are off to conserve power.

TABLE 2.5 POWER PROFILES OF VARIOUS WSN SENSOR NODES

WSN Sensor Node	μP	RF Transceiver	Active Mode [a]	Idle Mode [b]	Application
Rockwells WINS [19]	Intel StrongARM SA-1100	Conexant Systems	64 mW	1.08 mW	Acoustic and seismic sensing
UCLA MEDUSA-II [19]	Atmel AVR	Low-end RFM	24.58 mW	0.02 mW	SmartDust project
WSN [c,d] [19]	-	-	13 mW		-
Everlast [12]	PIC16LF747	2.4 GHz GFSK Nordic nRF2401	52.4 mW [e]	0.68 mW	MPPT for solar cells
WSN [f,d] [40]	TI MSP430F1611	MRF24J40MB	63.6 mW	1.48 μW	-
WSN [d] [13]	-	-	17.4 mW	~ 0 W	Temperature and humidity sensing
WSN [d] [9]	-	-	15.5 mW	1.55 μW	Temperature and humidity sensing [g]

a. The Active Mode refers to the DPM mode, when highest power is consumed by the WSN node.
b. The Idle Mode refers to the DPM mode, when lowest power is consumed by the WSN node.
c. The node was to demonstrate the benefits of 4-QAM scheme in energy-aware wireless communication.
d. The names of these WSNs were not given in the cited work.
e. The μP PIC16LF747 operates in 4 MHz during the active mode.
f. Component-aware Dynamic Voltage Scaling (DVS) is implemented in this WSN sensor node.
g. A COTS temperature and humidity sensor SHT21 is implemented for the application.

Take a WSN node demonstrated in [13], also listed in TABLE 2.5, for an instance. It is embodied by a battery-equipped configuration powered through WPT. The node is implemented to measure temperature and humidity. Its rectenna is made up of a 2.45 GHz rectangular micro-strip patch antenna (27.7 $\times$ 30.8 mm^2) that is 0-dBm-matched to a rectifier of an Avago HSMS-2852 Schottky diode voltage doubler. It is equipped with a rechargeable 3-V Lithium-ion battery and a COTS temperature and humidity sensor.

2.2 Power Assessment on Omnidirectional-EM-Radiation WPT

To determine the adequacy of the incident RF power with respect to the power consumption to execute operations, several factors have to be examined from the hardware technology perspective. From the transmitting end, the power density of the RF power being transferred is of main concern. It is restricted by

international safety standards on radiation. From the receiving end, various factors affect the adequacy of the RF power. They involve size of the Rx Antenna, charging distance r, conversion efficiencies of rectenna and PMU, size of the secondary battery (, if present), as well as the load consumption within the node. Consequently, the adequacy of the RF-power is determined by considering these factors holistically.

2.2.1 Safety Restrictions

Before adequacy of the RF-power can be determined, maximum RF-power that is allowed to be transmitted has to be determined. This is often limited by safety restrictions. Microwave radiation causes heating. It is due to dipole rotation. In the alternating EM field generated by the EM wave, molecules with electrical dipole moment will consistently reverse directions to stay aligned as EM field alternates. In the process, such molecules distribute energy to the adjacent ones in the form of heat. Though RF radiation is nonionizing and cannot cause cancer, long-term effects are still under research. [13] As a result, public concerns over potential health hazards due to the microwave heating of human tissues have initiated international commissions to set exposure limits under microwave radiation. The maximum power density from an intentional radiator operating at a frequency of 2.4 GHz is set by both U.S. Federal Communication Commission (FCC) standard for Maximum Permissible Exposure (MPE) (as averaged over 30 min) and International Commission on Non-Ionizing Radiation Protection (ICNIRP) standard for General Public Exposure [13, 41]; and both specify it as 10 W/m^2.

In addition, to prevent interference problems, FCC and European Radio-communications Commission (ERC) have also set restrictions on transmitting power. When transmitting 2.4 GHz EM energy, the currently most relaxed EIRP restrictions on the Tx Antenna is 4 W in North America and France (, where it is limited to indoor environment and cannot last for more than 15% of the duty cycle). [13]

TABLE 2.6 calculates maximum power reception at the Rx Antenna by assuming no path loss. To highlight the change of power reception with respect

to the charging distance and antenna size, the received power is integrated over difference effective antenna areas at different charging distances.

TABLE 2.6 MAXIMUM POWER AVAILABLE AT RX ANTENNA BASED ON INTERNALTIONAL SAFETY RESTRICTION ON EIRP [13]

Region	Max. EIRP (W)	Charging Distance	Power Density (mW/m^2)	Maximum Received Power Based on Rx Antenna Effective Aperture, A_e			
				50×50 cm^2		6×6 cm^2	
France	0.5[a]	1 m	39.79	9.98 dBm	9.9 mW	-8.44 dBm	0.14 mW
		10 m	0.40	-10.02 dBm	0.1 mW	-28.44 dBm	1.43 μW
	4[b]	1 m	318.31	19.01 dBm	79.6 mW	0.59 dBm	1.15 mW
		10 m	3.18	-0.99 dBm	0.8 mW	-19.41 dBm	11.5 μW
USA Canada	4	1 m	318.31	19.01 dBm	79.6 mW	0.59 dBm	1.15 mW
		10 m	3.18	-0.99 dBm	0.8 mW	-19.41 dBm	11.5 μW
Japan Korea	0.01	1 m	0.80	-7.01 dBm	0.2 mW	-25.43 dBm	0.003 mW
		10 m	0.0080	-27.01 dBm	0 mW	-45.43 dBm	0.03 μW

a. This is the maximum outdoor EIRP allowed in France.

b. This is the maximum indoor EIRP allowed in France; and the maximum duty cycle for it to last is 15%.

From Equation (2.1), it is noticed that, beyond 20-cm charging distance, maximum received power by an Rx Antenna is 250 mW with $A_e = 50 \times 50\ \mathrm{cm}^2$ and 3.6 mW with $A_e = 6 \times 6\ \mathrm{cm}^2$ when following the ICNIRP safety standards. These values are much larger than that of the maximum received power restricted by the ERC EIRP restrictions. For safety concerns, smaller values have to be chosen. As WSNs are usually widespread, separations wider than 20 cm are expected. Therefore, one should follow the ERC EIRP restrictions when determining the maximum power reception at Rx Antenna.

By comparing power consumption of popular WSN sensor nodes in TABLE 2.5 and the maximum power reception in TABLE 2.6, the RF power transferred through Omnidirectional-EM-Radiation WPT can be expected to be on the same level, i.e. tens of milliwatts, as the power consumption by WSN sensor nodes. Nonetheless, to ensure that sufficient RF power is captured to support node operations, several design parameters can trade with one another to achieve the dedicated WSN applications. These parameters include Rx Antenna size, charging distance r, conversion efficiencies within the rectenna

and the PMU, and the size of the secondary battery.

2.2.2 WPT-powered WSN Sensor Node Structure

Limited by ERC EIRP restrictions, a fixed amount of RF power can be predicted by Equation (2.1) with the given charging distance r. Thus, according to Equation (2.3), by building the Rx Antenna with a Micro-Strip Antenna (MSA) array, the RF power captured could be inadequate if r is large or the implemented MSA array is small. Other factors that will cause inadequacies are low conversion efficiencies of the rectenna and PMU components as well as the high power demand by the loads, such as the μP, RF transceivers, ADCs or so on. Under such scenario, a battery-equipped node is mandatory to budget the captured RF power for future use; and DPM has to be implemented. Therefore, good load regulation and fast load transient performance are the key concerns in PMU design as the load current consistently varies under DPM. In addition, good line regulation or Line Sensitivity (LS) is also necessary as the battery output voltage will slowly decline when it is dissipated.

In contrast, if the MSA array is sufficiently large or r is relatively small, the instantaneous RF power captured can be high enough to support all node operations. In a similar manner, high conversion efficiencies of the rectenna and PMU components or low power demand by the node loads will make the captured RF power adequate to satisfy power demand from loads. In this case, a battery-less node is sufficient to support the dedicated WSN application. Under such scenario, small output-ripples are the key concerns as the rectenna DC output is often fluctuating and noise-coupled. In VR and LDO design, such requirements are translated into good performances in line regulation and PSR. In boost DC-DC converter design, they are translated into noise-robustness and small output-ripples.

2.2.3 Performance Specifications on PMU Design

Despite diverse performance specifications on power management in the battery-equipped and battery-less node structures, this work aims at designing a PMU that is adoptable to both node structures. In other words, the PMU developed in this work are to encompass performance specifications demanded

by both node structures as much as possible. In this manner, the targeted performance specifications on the VR, LDO and boost DC-DC converter can be summarized in TABLE 2.7, TABLE 2.8, and TABLE 2.9 respectively.

TABLE 2.7 PERFORMANCE SPECIFICATIONS ON VR

$V_{DD,min}$ (V)	< 0.9
TC (ppm/°C)	< 50
Temp (°C)	-40 ~ 80
LS	< 0.2 %/V
PSR (up to 10 MHz) (dB)	< - 50

TABLE 2.8 PERFORMANCE SPECIFICATIONS ON LDO

$V_{DD,min}$ (V)	< 0.9
V_{DO} (V)	0.1
V_{OUT} (V)	0.7
$I_{L,max}$ (mA)	50
Load Reg. (mV/mA)	< 0.5
Line Reg. (mV/V)	< 1
Settling time, Δt_S (μs)	< 3
ΔI_{OUT} (mA)	50
Step time, t_r (ns)	100
PSR (up to 1 kHz) (dB)	< - 40

TABLE 2.9 PERFORMANCE SPECIFICATIONS ON BOOST CONVERTER

V_{DD} (V)	0.9
V_{OUT} (V)	3
Load Reg. (mV/mA)	< 0.5
Output Ripple (%)	< 1
T_{OS} (μs)	< 10
Overshoot (mV)	< 10
T_{US} (μs)	< 10
Undershoot (mV)	< 10
ΔI_{OUT} (mA)	40
Step time, t_r (ns)	100

2.3 Voltage Reference

Thanks to the controllability of the transmitting power-source and the presence of a rechargeable battery, the power constraint posed by a WPT-powered WSN sensor node can be more relaxed in comparison with that posed by energy-scavengers. Nonetheless, design challenges of a VR for a WPT-powered WSN sensor node still exist. They lie in the robustness of the design against variations in process parameters, supply voltage and temperature. More specifically, such robustness means low Temperature Coefficient (TC) over a wide temperature range, good LS over a wide supply range down to sub-1 V, and repeatable TC despite process deviations.

To achieve such robustness, process variations can be addressed by dedicated process-tracking or process-tolerance circuit structures [42, 43], or trimming circuitries when more precise TC is to be obtained [44]. Self-biased circuits and long-channel-length Metal Oxide Semiconductor Field Effect Transistors (MOSFET) are commonly used to overcome supply variations [45] so as to ensure a good LS.

Moreover, low TC can obtained by nullifying a Proportional-To-Absolute-Temperature (PTAT) term with a Complementary-To-Absolute-Temperature (CTAT) term derived by dedicated VR circuitries. In this manner, a VR output with a nearly-zero TC can be obtained. Various circuit topologies have been developed to implement such design principle. They include Bandgap Voltage Reference (BVR), CMOS VR derived from the Gate-Source Voltages (V_{GS}) or the weighted Difference between Threshold Voltages (ΔV_{th}) of two MOSFETs. To determine a viable VR structure dedicated to WPT-powered WSN sensor nodes, this section reviews each of these VR circuitries sequentially.

2.3.1 Bandgap Voltage Reference

The PTAT term derived from a BVR is ΔV_{BE}, which denotes the voltage difference between the base-emitter junctions of two Bipolar Junction Transistors (BJTs); the CTAT term is realized by V_{BE}, which denotes the BJT base-emitter voltage.

To illustrate, Figure 2.3 presents a typical BVR circuit topology. By assuming an ideal Error Amplifier (EA) in the BVR, it is inferred that $V_A(=V_{BE1}) = V_B$, where V_{BE1} is the base-emitter voltage of NPN BJT Q_1. Hence, apply Kirchhoff Current Law (KCL) at V_B to obtain

$$I_2 = \frac{V_B}{R_{1,2}} + \frac{V_B - V_{BE2}}{R_0} = \frac{V_{BE1}}{R_{1,2}} + \frac{\Delta V_{BE}}{R_0}, \quad \textbf{(2.19)}$$

where $\Delta V_{BE} = V_{BE1} - V_{BE2}$ and V_{BE2} is the base-emitter voltage of NPN BJT Q_2. Alternatively, PNP BJTs can be used for Q_1 and Q_2 instead as well to serve the same design requirements.

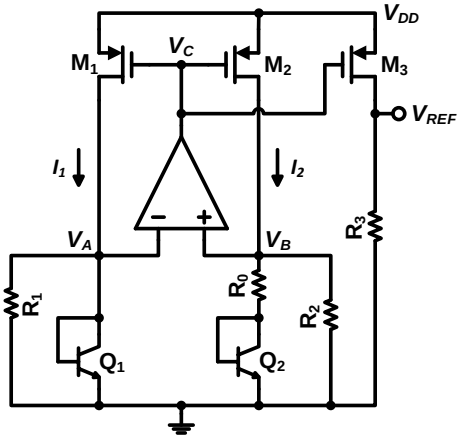

Figure 2.3 Circuit diagram of a typical current-mode BVR [46].

In Figure 2.3, $R_1 = R_2$ and P-channel MOSFETs (PMOS) M_1, M_2 and M_3 are identical by design. Resistors R_0, R_1, R_2 and R_3 are of the same material to ensure identical TCs of their resistance. In this manner,

$$V_{REF} = V_{BE1}\frac{R_3}{R_{1,2}} + \Delta V_{BE}\frac{R_3}{R_0}. \quad \textbf{(2.20)}$$

Moreover, by having both NPN BJT Q_1 and Q_2 operating in their active region,

$$I_{C1} = I_{S1}e^{\frac{v_{BE1}}{V_T}} = \frac{A_{E1}qD_n n_i^2}{N_A W}e^{\frac{v_{BE1}}{V_T}}; \quad \textbf{(2.21)}$$

$$I_{C2} = I_{S2}e^{\frac{v_{BE2}}{V_T}} = \frac{A_{E2}qD_n n_i^2}{N_A W}e^{\frac{v_{BE2}}{V_T}}, \quad \textbf{(2.22)}$$

where $I_{S1,2}$ are the saturation currents of Q_1 and Q_2; $V_T = \frac{kT}{q}$ is the thermal voltage; k is the Boltzmann constant; q is the electronic charge; T is the absolute temperature; D_n is the minority-carrier diffusion constant within the quasi-neutral

base region; N_A is the dopant concentration in the base; W_B is the width of the quasi-neutral base region; n_i is the intrinsic carrier density; $A_{E1,2}$ are the area of emitter-base junction of Q_1 and Q_2 respectively. [47] In addition, $A_{E2} = nA_{E1}$.

Furthermore, by combing Equation (2.21) and (2.22),

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = \frac{kT}{q}\ln(n). \quad \textbf{(2.23)}$$

In addition, according to [45], saturation current I_S of BJT can also be expressed as

$$I_S = bT^{4+m}e^{-\frac{E_g}{kT}}, \quad \textbf{(2.24)}$$

where b is a proportionality factor, $m \approx -1.5$ and $E_g = 1.12\,\text{eV}$ is the bandgap energy of silicon. Thus, V_{BE1} in Equation (2.20) can be expressed as

$$V_{BE1} = V_T \ln\left(\frac{I_{C1}}{I_{S1}}\right) = V_T \ln\left(\frac{I_{C1}}{b_1 T^{4+m} e^{-\frac{E_g}{kT}}}\right). \quad \textbf{(2.25)}$$

Consequently, from Equation (2.23) and (2.25),

$$\frac{d(\Delta V_{BE})}{dT} = \frac{k}{q}\ln(n); \quad \textbf{(2.26)}$$

$$\frac{d(V_{BE1})}{dT} = \frac{V_{BE1} - (4+m)V_T - \frac{E_g}{q}}{T} \approx -1.5\ {}^{mV}/_{\circ K}, \quad \textbf{(2.27)}$$

where it is estimated that $V_{BE1} \approx 750\,\text{mV}$ and $T = 300\,°\text{K}$. In this manner, based on Equation (2.20), by setting

$$TC = \frac{dV_{REF}}{dT} = \frac{dV_{BE1}}{dT}\frac{R_3}{R_{1,2}} + \frac{d(\Delta V_{BE})}{dT}\frac{R_3}{R_0} = 0, \quad \textbf{(2.28)}$$

$R_{1,2}$, R_3 and n can be derived.

As it is observable that sub-1-V supply, such as $V_{DD} = 0.9\,\text{V}$, is sufficient to ensure all BJT and PMOS transistors to operate in their active regions. Take the 180-nm CMOS process for example. This can be done by allocating $V_{CE} = V_{BE} = 0.7\,\text{V}$ and $V_{DS1,2,3} = 0.2\,\text{V}$. The main challenge to realize sub-1-V operations lies in the design of a sub-1-V EA. Topologies based on two distinct circuit

structures are investigated to bring down the affordable V_{DD} to sub-1 V.

1) Resistive-divider-based Topology

To ensure proper functionalities of a sub-1-V EA, [48] replaces R_1 and R_2 in Figure 2.3 with resistive dividers so as to bring down the input voltage to the PMOS input-pair within the EA. The circuit diagram is shown in Figure 2.4. In a similar fashion, V_{REF} can be computed using Equation (2.20), where $R_1 = R_{1A} + R_{1B}$ and $R_2 = R_{2A} + R_{2B}$.

However, input voltages to the EA in Figure 2.4 has dropped to $\frac{R_{1B}}{R_1}|V_{BE1}|$ from $|V_{BE1}|$ as in Figure 2.3. By implementing PMOS input-pair in the EA, the gate-source voltages, V_{SGp}, of the PMOS input-pair increase. Subsequently, the input transconductance g_{m_in} increases following

$$g_{m\_in} = \mu_p C_{ox}(\frac{W}{L})(V_{SGp} - |V_{thp}|), \quad \textbf{(2.29)}$$

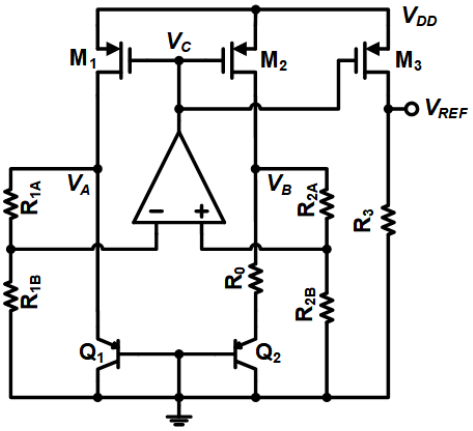

Figure 2.4 Circuit diagram of a current-mode BVR with resistive dividers [48].

where μ_p is the mobility of holes in PMOS; W is the channel width of the PMOS; L is the effective channel length of the PMOS; C_{ox} is the gate-oxide capacitance per unit area; V_{thp} is the threshold voltage of the PMOS. As a result, a high DC-gain $|A_{dc}| = g_{m\_in}R_{out}$ of the EA can be obtained, where R_{out} is the output impedance of the EA. A high DC-gain ensures that $V_A = V_B$.

Quantitatively, the minimum supply, $V_{DD,min}$, can be derived by ensuring that the PMOS input-pair of the EA operates in the saturation region from [48]

$$V_{DD,min} = \left(\frac{R_{1B}}{R_1}\right) V_{EB1} + |V_{thp}| + 2|V_{DS}|, \quad \textbf{(2.30)}$$

where V_{DS} refers to the drain-source voltages of the PMOS input-pair, M_4 and M_5, and the PMOS, M_{BP}, as the biasing current-source to the PMOS input-pair in the EA. Nonetheless, $V_{DD,min}$ is limited by $V_{EB1}(\approx 0.7\ \mathrm{V})$.

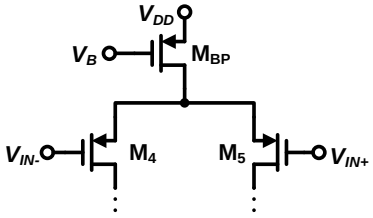

Figure 2.5 Circuit diagram of the EA input-stage for BVR with resistive dividers.

2) Grounded-input-pair-based Topology

Instead of a conventional PMOS input-pair sourced by a tail current-source, an EA with a grounded input-pair is introduced in [46]. The overall BVR in [46] follows exactly the same topology as that shown in Figure 2.3. In the same manner, V_{REF} can be computed by Equation (2.20) as well. The detailed circuit-diagram is displayed in Figure 2.6.

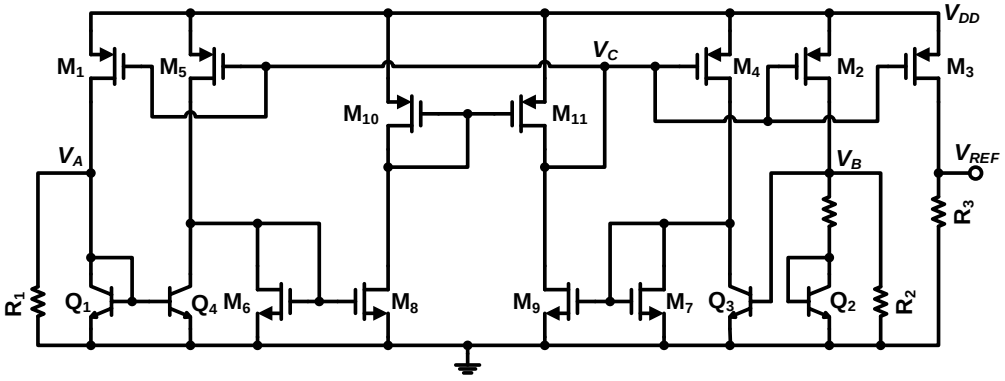

Figure 2.6 Circuit diagram of a BVR with grounded input-pair in its EA.

By implementing a grounded BJT input-pair Q_3 and Q_4, the resulted EA omits the tail current-sink. As a result, the current in the input stage of the EA can be controlled by the PTAT current of the BVR itself. This is achieved through current mirrors formed through diode-connected BJT, such as Q_1, and Q_4 instead of a tail current-sink conventionally. In addition, the biasing voltage for

the active loads, M_5 and M_4, of the EA's input-stage comes from the BVR circuit as well. Similar to any self-biased BVR design, a start-up circuit is needed in this design to initiate intended BVR operations.

It is apparent that there are maximally two transistors stacked along each branch of the EA. Hence, the minimum V_{DD} achievable is limited by the grounded input-pair only. In comparison with the PMOS input-pair in [48], the grounded input-pair reduces the minimum V_{DD} into the sub-1-V range as

$$V_{DD,min} = V_{BE1} + |V_{DS}|. \tag{2.31}$$

By assuming a 180-nm CMOS process, $V_{DD,min}$ can reach as low as $0.9\ \text{V}$ by allocating $V_{CE1} = V_{BE1} = 0.7\ \text{V}$ for Q_1 and $V_{DS} = 0.2\ \text{V}$ for M_1 to have both transistors operating in their active regions. Again, the large V_{BE1} to turn on the BJT is the main limiting factor to lower V_{DD} further. Besides, both the grounded input-pair and the push-pull second-stage formed by M_8 - M_{11} in the EA display inherent symmetry. It helps to minimize systematic offset of the EA and improves the BVR output-accuracy.

2.3.2 V_{GS}-based CMOS Voltage Reference

1) ΔV_{GS}-based Topology

To overcome the limitation on $V_{DD,min}$ imposed by V_{BE} ($\approx 0.7\ \text{V}$) to ensure that BJT operates in its active region, CMOS VRs are developed in attempts to lower $V_{DD,min}$ further. One type of them, such as the ΔV_{GS}-based VR derives the reference voltage, V_{REF}, based on the difference between the gate-source voltages of two MOSFETs operating in saturation regions. [49] Conventionally, this can be expressed in Equation (2.32) based on the circuit topology in Figure 2.7a:

$$V_{REF} = V_{GS2a} - V_{GS1a} = V_{th2a} - V_{th1a} + \sqrt{2I}\left(\sqrt{\frac{1}{k_{2a}}} - \sqrt{\frac{1}{k_{1a}}}\right), \tag{2.32}$$

where V_{th2a} and V_{th1a} refer to the threshold voltages of M_{1a} and M_{2a}; I equals the drain current through M_{1a} and M_{2a}; $k_{1a,2a} = \mu_n C_{ox}(\frac{W_{1a,2a}}{L_{1a,2a}})$ with μ_n being the mobility of electrons in NMOS, $W_{1a,2a}$ as the channel width of the M_{1a} and M_{2a},

$L_{1a,2a}$ as the effective channel length of M_{1a} and M_{2a}.

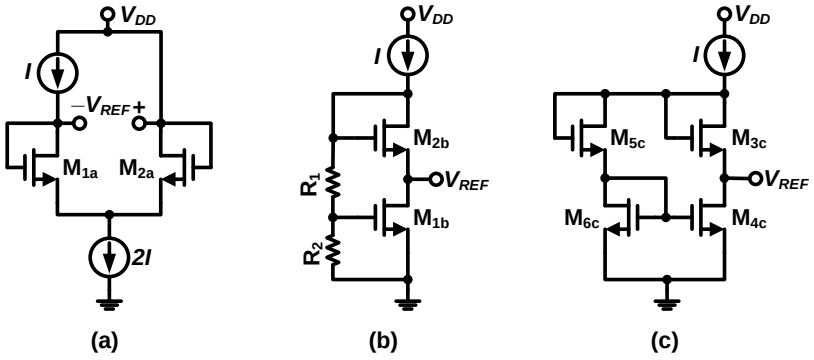

Figure 2.7 Circuit diagrams of ΔV_{GS}-based CMOS VRs.

Alternatively, V_{REF} can be derived by the weighted difference between the gate-source voltages of the two MOSFETs in saturation regions as expressed in Equation (2.33):

$$V_{REF} = \left(1 + \frac{R_1}{R_2}\right) V_{GS2b} - V_{GS1b} = \frac{R_1}{R_2} V_{th} + \sqrt{2I} \left[\left(1 + \frac{R_1}{R_2}\right) \sqrt{\frac{1}{k_{2b}}} - \sqrt{\frac{1}{k_{1b}}}\right], \quad \textbf{(2.33)}$$

where $V_{th} = V_{th1b} = V_{th2b}$. Subsequently, a zero TC can be derived by designing $I \propto \mu(T)T^2$ and neglecting non-ideal effects, such as channel-length modulation or body effects. The circuit structure to obtain I in (2.33) will be presented later as it is not the major concern in minimizing TC. The corresponding circuit topology is shown in Figure 2.7b. [49]

To minimize TC further by suppressing TC dependence on channel-length modulation and body effect, a circuit structure that replaces the passive resistive divider R1-R2 in Figure 2.7b with an active resistive divider M_{5c}-M_{6c} is shown in Figure 2.7c. By having all MOSFETs in saturation regions, it can be first derived that

$$V_{REF} = V_{th} + \left[\frac{1}{\sqrt{k_{4c}}}\left(1 + \sqrt{\frac{W_{6c}/L_{6c}}{W_{5c}/L_{5c}}}\right) - \frac{1}{\sqrt{k_{3c}}}\right] \sqrt{2I}, \quad \textbf{(2.34)}$$

where $V_{th} = V_{th3c} = V_{th4c} = V_{th5c} = V_{th6c}$; $k_{3c,4c} = \mu_n C_{ox}(\frac{W_{3c,4c}}{L_{3c,4c}})$; $W_{5c,6c}$ and $L_{5c,6c}$ are the channel width and channel length of M_{5c} and M_{6c} respectively [49, 50]. Therefore, TC dependence on channel length modulation and body effect

can be obtained respectively as in Equation (2.35) and Equation (2.36)

$$\frac{d}{dT}V_{REF}\Big|_{channel\_length\_modulation} \cong \frac{\lambda}{4}K_{t1}(2V_{th} - V_{REF}); \quad \textbf{(2.35)}$$

$$\frac{d}{dT}V_{REF}\Big|_{body\_effect} \cong \frac{\gamma}{2}\left(\frac{d\phi_f}{dT}\right)\left(\frac{1}{\sqrt{\phi_f - V_{BS5c}}} - \frac{1}{\sqrt{\phi_f - V_{BS3c}}}\right), \quad \textbf{(2.36)}$$

where λ is the channel-length-modulation coefficient; K_{t1} is the BSIM3v3 threshold-voltage temperature-coefficient; γ is the body-effect coefficient; ϕ_f is the work function of the silicon substrate; $V_{BS3c,5c}$ is the bulk-source voltage of M_{3c} and M_{5c}. Hence, by designing $V_{REF} = 2V_{th}$ and ensuring source terminals of M_{5c} and M_{3c} at the same voltage potentials, i.e., $V_{BS3c} = V_{BS5c}$. Despite a TC of 10 ppm/°C achieved [49], a minimum of 1.5 V is required as $V_{DD,min}$ to turn on such VR. This makes it not suitable for sub-1-V operations.

3) V_{GS}-based Topology

To bring down $V_{DD,min}$ below 1 V, a V_{GS}-based CMOS VR topology derived from the ΔV_{GS}-based CMOS VRs is shown in Figure 2.8. In this topology, M_1 and M_3 operate in the subthreshold region; whereas M_2 and M_4 operate in the saturation region. M_5 and M_6 are identical to form a set of current-mirror. M_7, M_8 and M_9 are identical to form another set of current-mirror. By having M_{10} in the saturation region, it can be given that

$$V_{REF} = V_{GS10} = V_{th10} + \sqrt{\frac{2I}{k_{10}}}, \quad \textbf{(2.37)}$$

where V_{th10} is the threshold voltage of M_{10} when $V_{BS10} = 0$ V; $k_{10} = \mu_n C_{ox}(\frac{W_{10}}{L_{10}})$.

Current I in Equation (2.37) retains the same characteristic of $I \propto \mu(T)T^2$ as it is in Figure 2.7. By ignoring the non-ideal effects, such as channel-length modulation and body effect, it is given that

$$I = \frac{\mu C_{ox} W_4/L_4}{2(N-1)^2} m_s^2 V_T^2 \ln^2(\frac{W_3/L_3}{W_1/L_1}), \quad \textbf{(2.38)}$$

where $N \equiv \sqrt{(W_4/L_4)/(W_2/L_2)}$ and m_s is the subthreshold slope-parameter. In addition, with

$$V_{th10}(T) = V_{th10}(T_0) - K_{tn}(T - T_0), \tag{2.39}$$

where K_{tn} is the threshold-voltage temperature-coefficient of a NMOS. Hence, TC can be derived as

$$\frac{dV_{REF}}{dT} = -K_{tn} + \frac{m_s}{N-1}\left(\frac{k}{q}\right)\sqrt{\frac{W_4/L_4}{W_{10}/L_{10}}}\ln\left(\frac{W_3/L_3}{W_1/L_1}\right). \tag{2.40}$$

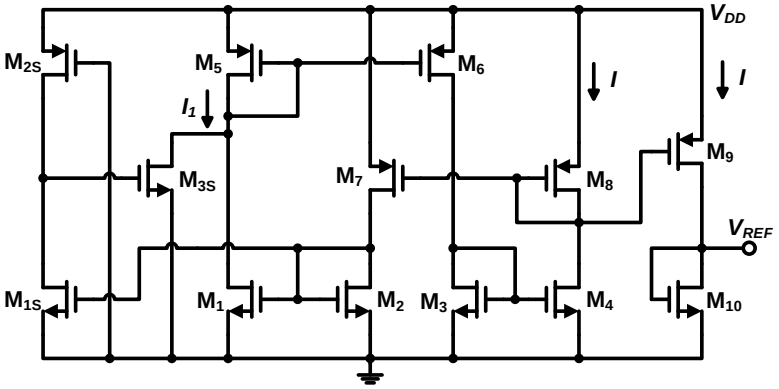

Figure 2.8 Circuit diagram of a V_{GS}-based CMOS VR.

Hence, by setting TC = 0, only following condition needs to be satisfied

$$\sqrt{\frac{W_4/L_4}{W_{10}/L_{10}}} = \frac{K_{tn}(N-1)}{m_s\left(\frac{k}{q}\right)\ln\left(\frac{W_3/L_3}{W_1/L_1}\right)}. \tag{2.41}$$

Despite the absence of body effect in such topology, channel-length modulation does exist and I in Equation (2.38) has to be re-computed as

$$I = \frac{m_s^2 V_T^2 k_4}{2}\left(\frac{1}{N-1/\sqrt{1+\lambda V_{DS4}}}\right)^2 \ln^2\left(\frac{W_3/L_3}{W_1/L_1}\right), \tag{2.42}$$

where $k_4 = \mu_n C_{ox}(\frac{W_4}{L_4})$ and V_{DS4} is the drain-source voltage of M_4. By considering the effect of channel-length modulation and substitute I from Equation (2.42) into Equation (2.37), TC of V_{REF} derived by the circuit in Figure 2.8 can be derived through the first-order Taylor series approximation as

$$\frac{dV_{REF}}{dT} = \frac{\lambda K_{tn}}{1-N}\left[V_{DD} - |V_{th8}| - (V_{REF0} - V_{th10}) \times \left(2\sqrt{\frac{W_{10}/L_{10}}{W_8/L_8}} - \frac{K_{tp}}{K_{tn}}\right)\right]. \tag{2.43}$$

From Equation (2.43), it is apparent that TC can be set as zero for a specific V_{DD} only. As V_{DD} deviates from the specific value, TC will become

nonzero. In other words, TC of V_{REF} obtained by the circuit topology in Figure 2.8 is supply-dependent. LS can be as large as 0.27%/V. Therefore, in spite of the sub-1-V operation achieved by this structure, supply-dependence is not a desirable trait for a VR powered by a fluctuating DC output from the rectifier through WPT.

2.3.3 ΔV_{th}-based CMOS Voltage Reference

1) 2-Transistor-based Topology

Another type of CMOS VR based on ΔV_{th} is introduced in Figure 2.9 [51]. It is in a simple form of a 2-Transistor topology. Both M_1 and M_2 operate in the subthreshold region. M_1 is a native NMOS whereas M_2 is a NMOS with thick gate-oxide for I/O applications. Hence, the threshold voltage, V_{th}, of M_1 and M_2 are inherently different from one another. In this manner, drain currents of M_1 and M_2 can be expressed as

$$I = I_1 = \mu_1 C_{ox1} \left(\frac{W_1}{L_1}\right) (m_{s1} - 1) V_T^2 \exp\left(\frac{0 - V_{REF} - V_{th1}}{m_{s1} V_T}\right); \quad \textbf{(2.44)}$$

$$I = I_2 = \mu_2 C_{ox2} \left(\frac{W_2}{L_2}\right) (m_{s2} - 1) V_T^2 \exp\left(\frac{V_{REF} - V_{th2}}{m_{s2} V_T}\right), \quad \textbf{(2.45)}$$

where $m_{s1,2}$ is the subthreshold slope-parameter. Further, by assuming that $V_{DS1,2} > 5V_T (= 5\,kT/q)$ and equating Equation (2.44) and Equation (2.45),

$$V_{REF} = \frac{m_{s1} m_{s2}}{m_{s1} + m_{s2}} (V_{th2} - V_{th1}) + \frac{m_{s1} m_{s2}}{m_{s1} + m_{s2}} V_T \ln\left(\frac{\mu_1 C_{ox1} W_1 L_2}{\mu_2 C_{ox2} W_2 L_1}\right). \quad \textbf{(2.46)}$$

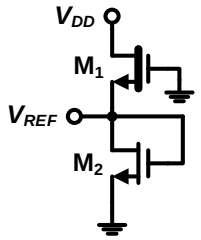

Figure 2.9 Circuit diagram of ΔV_{th}-based 2-Transistor CMOS VR.

Subsequently, by setting $TC = dV_{REF}/dT = 0$ and with reference to Equation (2.39), it is given that

$$\left(\frac{W_1}{W_2}\right)_{opt} = \frac{\mu_2 C_{ox2} L_2}{\mu_1 C_{ox1} L_1} \exp\left[\frac{q}{k}(K_{t2} - K_{t1})\right]. \quad \textbf{(2.47)}$$

The main drawback of this CMOS VR topology is the TC derived being highly sensitive to process variation. Even after trimming, the TC can vary from 5.3 ppm/°C to 47.4 ppm/°C across -20°C to 80°C over 25 dies.

2) BVR-like Topology

Alternatively, ΔV_{th} can be leveraged as shown in Figure 2.10 to derive V_{REF}. [52] Here, M_2 is implemented as a special high-V_{th} (hvt) NMOS provided by the foundry whereas its counterpart M_1 remains as a NMOS with normal-V_{th} (nvt). Similar to the conventional current-mode BVR, V_{REF} is derived as

$$V_{REF} = \frac{V_{GS2} - V_{GS1}}{R_1}(R_{0a} + R_{0b}), \quad \textbf{(2.48)}$$

where R_1, R_{0a} and R_{0b} are implemented with the same material.

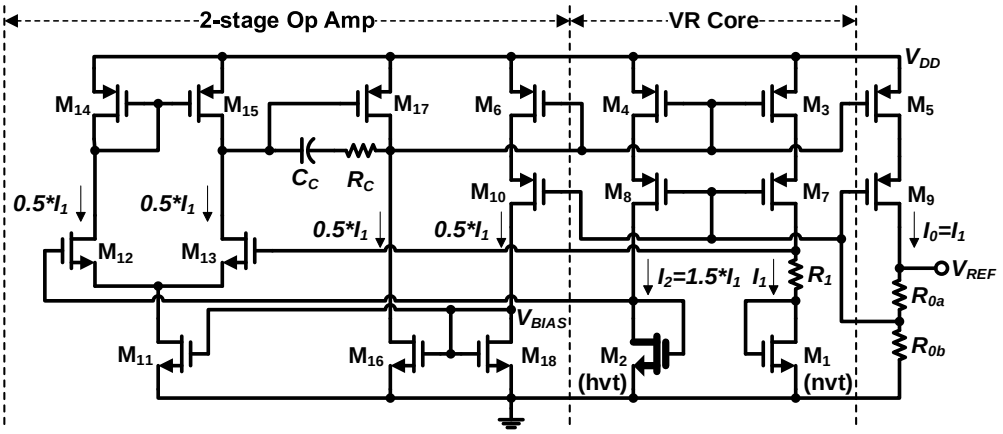

Figure 2.10 Circuit diagram of ΔV_{th}-based CMOS VR in a BVR-like topology.

In this manner, TC of this VR is linearly proportional to that of $(V_{GS2} - V_{GS1})$. By having M_1 and M_2 operate in subthreshold region and assuming that $V_{DS1,2} > 5V_T$ with $I_2 = 1.5I_1$, it can be shown that

$$V_{GS2} - V_{GS1} = V_{th,hvt} - V_{t,nvt} + \ln\left[\frac{I_2 \mu_{n1} C_{ox1}(W_1/L_1)}{I_1 \mu_{n2} C_{ox2}(W_2/L_2)}\right] m_s V_T, \quad \textbf{(2.49)}$$

where $V_{t,hvt}$ is the threshold voltage of M_2; $V_{th,nvt}$ is the threshold voltage of M_1; $m_s = m_{s1} = m_{s2}$. With reference to Equation (2.39) and by substituting Equation (2.49) into Equation (2.48),

$$\frac{dV_{REF}}{dT} = \frac{R_0}{R_1}\left\{\left(K_{t,nvt} - K_{t,hvt}\right) + m_s\left(\frac{k}{q}\right)\ln\left[\frac{I_2\mu_{n1}C_{ox1}(W_1/L_1)}{I_1\mu_{n2}C_{ox2}(W_2/L_2)}\right]\right\}, \quad \textbf{(2.50)}$$

where $K_{t,nvt} < K_{t,hvt}$. Hence, by setting $dV_{REF}/dT = 0$, an optimal ratio between W_1/L_1 and W_2/L_2 can be derived. Moreover, it is found out that, $V_{DD,min}$ for the VR core,

$$V_{DD,min,core} = V_{GS2} + V_{DS4} + V_{DS8}. \quad \textbf{(2.51)}$$

Hence, by choosing an EA whose $V_{DD,min}$ is less than $V_{DD,min,core}$, a sub-1-V CMOS VR can be obtained. The VR reported in [52] can operate with $V_{DD,min} = 0.65\ \mathrm{V}$.

2.3.4 Concluding Remarks

TABLE 2.10 compares all VR topologies reviewed in this section, where I_Q refers to the quiescent current consumption by the VR. As explained earlier, the main drawback of BVRs lie in their difficulties to achieve sub-1-V operations in spite of their relatively low TCs [48].

TABLE 2.10 PERFORMANCE COMPARISON AMONG VR TOPOLOGIES

		[48]	[46]	[50]	[49]	[51]	[52]
Topology		Resistive Divider	Grounded Input-pair	ΔV_{GS}	V_{GS}	ΔV_{th}, 2-T	ΔV_{th}, BVR-like
Tech.		0.6 µm CMOS	0.8 µm BiCMOS	0.35 µm CMOS	0.35 µm CMOS	0.13 µm CMOS	65 nm CMOS
VR Type		BVR	BVR	CMOS	CMOS	CMOS	CMOS
V_{DD} (V)		0.98 ~ 1.5	1 ~ 2	1.5 ~ 4.3	0.9 ~ 4	0.5 ~ 3.5	0.62 ~ 2
I_Q (µA)		< 18	92 @ 1 V	0.08 @ 1.5 V	0.04 @ 0.9 V	9.50E-05 @ 0.5 V	0.04 @ 0.62 V
				0.11 @ 4.3 V	0.055 @ 4 V		
V_{REF} (V)		0.63	0.54	0.891	0.67	0.175	0.39
TC (ppm/°C)		15 ~ 25	7.5	12 @ 3 V	10 @ 2.45 V	5.3 ~ 47.4	44 ~ 248
Trimming		yes	yes	no	no	yes	no
Temp (°C)		0 ~ 100	0 ~ 80	0 ~ 80	0 ~ 80	-20 ~ 80	-25 ~ 110
LS		0.73%/V	0.021%/V	0.46%/V	0.27%/V	0.036%/V	0.07%/V
PSR	100 Hz	-44 dB @ 0.98 V	-	-59 dB @ 1.5 V	-47 dB @ 0.9 V	-75 dB @ 0.5 V	-62 dB @ 0.62 V
	10 MHz	-17 dB @ 0.98 V	-	-52 dB @ 1.5 V	-40 dB @ 0.9 V	-122 dB @ 0.5 V	-
Area (mm^2)		0.24	3	0.015	0.045	0.0093	0.266

However, it is desirable to ensure good LS and line regulation for proper operation of the WSN node in case the output of its secondary battery slips into the sub-1-V region. In comparison with BVRs, CMOS VRs, free from limitations imposed by the bandgap voltage and V_{BE}, offer the potential to lower $V_{DD,min}$ further [49, 51, 52].

Nevertheless, due to non-ideal effects, such as channel-length modulation, TC of the V_{GS}-based CMOS VR is supply sensitive. The low TC derived is meaningful only under a specified V_{DD} [49]. In addition, CMOS VRs are process-sensitive in general. This results in bad repeatability in TC across dies [51, 52].

In contrast, the BVR-like topology implemented by the ΔV_{th}-based CMOS VR in [52] bridges the CMOS VR design with BVR design. As a result, various curvature-compensation techniques previously developed for BVRs are readily adoptable into a BVR-like CMOS VR as well. Such an advantage offers hope to reduce TC further in such CMOS VR. Moreover, with comprehensive trimming networks to address process variations and improve TC repeatability, such CMOS VR could be a viable solution to render stable reference voltages in a WPT-powered WSN sensor node.

2.4 Low Drop-Out Voltage Regulator

Twofold are the requirements on a supply-independent LDO to fit into a WPT-powered PMU for a WSN sensor node: namely, a low LS and a high PSR. To achieve both, a current-efficient sub-1-V structure with a high DC-gain is necessary. The Partial Positive Feedback (PPF) structure introduced in [53] displays potential. Variations of PPF are numerated and analyzed in the DC domain in [54] and, more recently, in [55, 56]. The amplifier incorporated with the PPF is current-efficient in boosting the input-transconductance (input-g_m) and the DC-gain. It does so by deriving source-degenerating negative-resistance at the input stage of the amplifier.

Moreover, fast load-transient-responses are to be assured upon sudden switching on or off the loading ICs orchestrated by the DPM scheme. Cross-

coupled input-structures are looked into in search of an effective approach to ensure fast-settling. [57] presents a fast-settling OCL-LDO with a pair of cross-coupled transconductance cells (G_m-cells) at the input stage of its EA. Similarly, a cross-coupled structure that makes use of Flipped Voltage Follower (FVF) is implemented in an OTA in [58] for the same purpose of transient acceleration.

Furthermore, various frequency compensation techniques to ensure stability are also explored in this section. These involve techniques, such as miller compensation and its derivatives as well as damping-factor-control compensation.

2.4.1 PPF-incorporated Input-stage

1) PPF Incorporated at the Source Terminals

Circuits in Figure 2.11a implements a PPF structure, consisting of identical transistors M_3 and M_4, as the Source Degenerating Resistance (SDR) to the input transistors M_1 and M_2 of an OTA [53]. To compute the resistance of the SDR, small-signal analysis is performed based on Figure 2.11b. By assuming i as the current going through M_3 and M_4 under voltage, v_d, across the PPF and attributing $v_d/2$ at the drain terminal of M_3 and $-v_d/2$ at the drain terminal of M_4, one may obtain

$$i = g_{m3}\left(-\frac{v_d}{2} - v_m\right) = -g_{m4}\left(\frac{v_d}{2} - v_m\right) \quad \textbf{(2.52)}$$

Subsequently, the PPF can be treated as two SDRs, such as r_3 and r_4, connected in series with M_1 and M_2 respectively with their value given below

$$r_{3,4} = (\frac{v_d}{2} - v_m)/i = -1/g_{m3,4} \quad \textbf{(2.53)}$$

The overall input-g_m of the OTA in Figure 2.11a can be computed based on the source-degenerated M_1 and M_2 [45, 53] as

$$g_{m,in} = g_{m3}/(1 - g_{m3}/g_{m1}) \quad \textbf{(2.54)}$$

Moreover, M_5 and M_6 in Figure 2.11a are necessary in preventing latch-up of the input stage. Specifically, M_6 helps to clamp the source voltage of M_4

to a sufficiently-high voltage to prevent M_{18} from shutting-off [53]. Furthermore, the ratio α of drain currents in M_1 or M_2 versus M_5 and M_6 is set as 3:1. Such value ensures good input-g_m boosting by a factor of 3 without additional current consumption. However, further increase in α can be prohibitive as it may sabotage the frequency stability of the OTA [53].

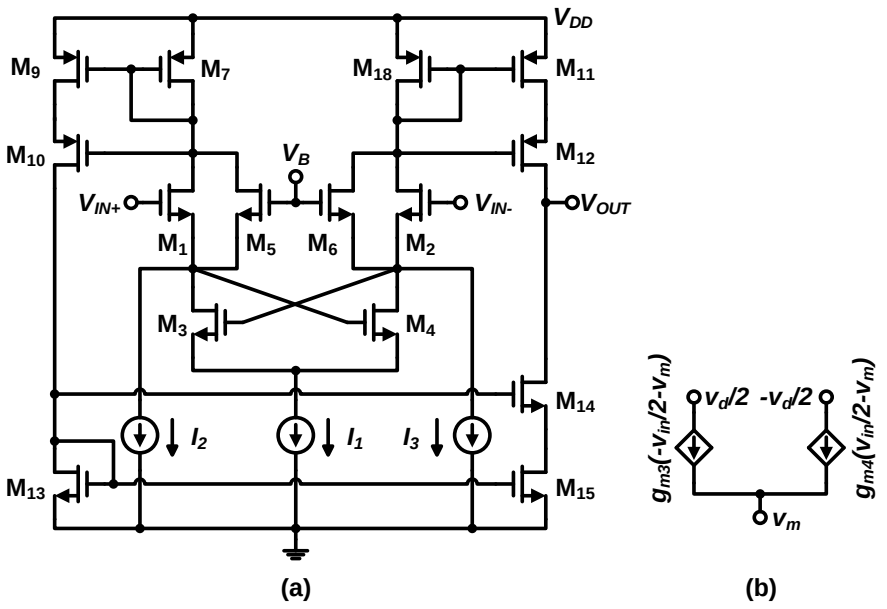

Figure 2.11 PPF incorporated as negative SDR in (a) the circuit diagram of an OTA [53] with (b) its small-signal diagram.

Therefore, despite a current-effective approach to raise input-g_m and DC-gain, the PPF-incorporated OTA in Figure 2.11a exhibits two disadvantages to qualify as a viable structure to build an LDO within a WPT-powered PMU. Firstly, the circuit structure is heavily stacked with transistors, which make it difficult to operate under a sub-1-V V_{DD}. Secondly, the frequency stability of the OTA is sensitive to the current ratio α. Indeed, such disadvantage affects the effectiveness of the PPF-incorporated structure reversely in boosting the input-g_m and DC-gain.

2) PPF Incorporated at the Drain Terminals

Variations in the PPF structure are listed in [54] and later implemented as negative load-resistance in both PMOS [55] and NMOS [56] at the input stage of an OTA for the same purpose as to boost input-g_m and DC-gain. Despite bulk-driven approach is implemented for input signals in both OTAs as shown in

Figure 2.12, the rationale to derive the input-g_m stays the same as the PPF-incorporated OTA in Figure 2.11. Take the OTA in Figure 2.12b for an instance. The input-g_m of the OTA can be derived through (2.53) and (2.54) [56] as

$$g_{m,in} = 2\,g_{mb1,3}g_{m9}/(g_{m7} - g_{m8} + g_{ds1} + g_{ds3} + g_{ds7} + g_{ds8}), \quad \textbf{(2.55)}$$

where $g_{mb1,3}$ is the bulk transconductance of identical transistors M_{1A}, M_{1B}, M_{3A} and M_{3B}; g_{m7}, g_{m8}, g_{m9} are the transconductance of transistors M_{7A}, M_{7B}, M_{8A}, M_{8B}, M_{9A} and M_{9B} respectively; g_{ds1}, g_{ds3}, g_{ds7} and g_{ds8} are the output conductance of transistors M_{1A}, M_{1B}, M_{3A}, M_{3B}, M_{7A}, M_{7B}, M_{8A} and M_{8B} respectively.

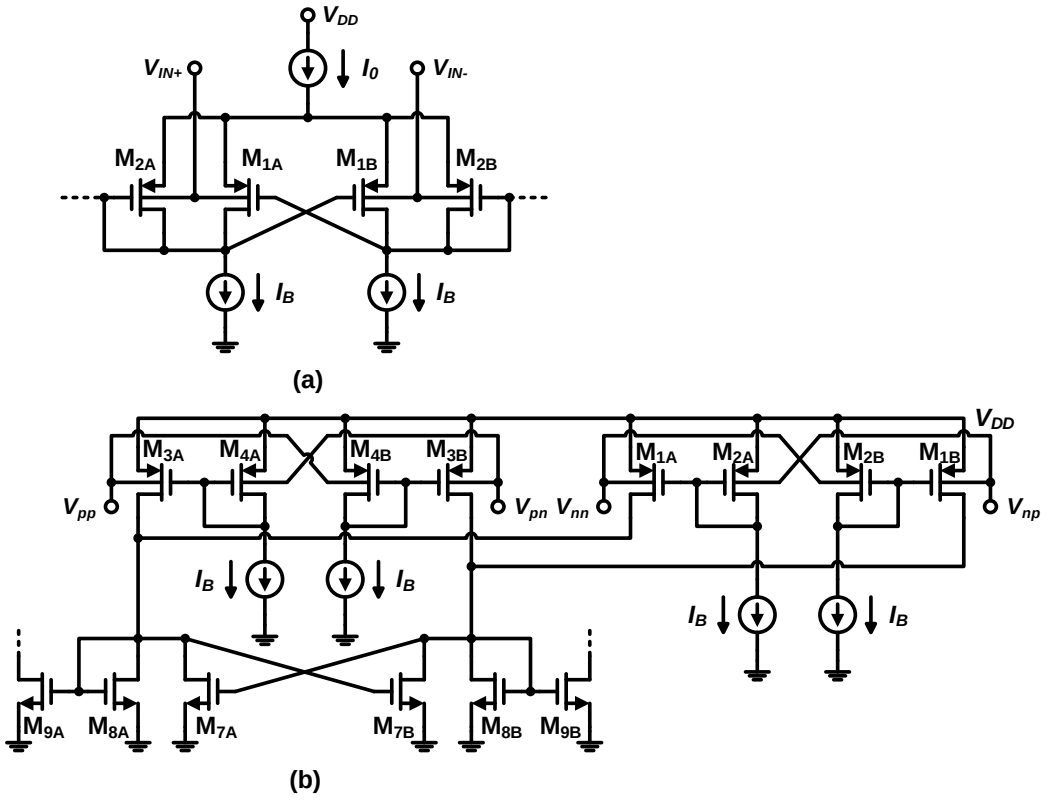

Figure 2.12 Circuit diagrams of PPF-incorporated as negative load-resistance (a) in PMOS in the OTA presented in [55] and (b) in NMOS in the OTA presented in [56].

In comparison with the OTA with PPF incorporated as the negative SDR in Figure 2.11, OTAs in Figure 2.12, especially in case of Figure 2.12b, offer potential to operate under sub-1-V V_{DD}. Consider 180-nm CMOS process technology, with $V_{DD,min} = |V_{GS}| + |V_{DS}|$, it is promising to obtain $V_{DD,min} < 1$ V as

the gate-source voltage, $|V_{GS}|$, needed to turn on the MOSFETs is likely to be less than 0.7 V, and the drain-source voltage, $|V_{DS}|$, can be set as around 0.2 V.

However, employing such OTAs as the EA for an LDO still face obstacles. Trade-off between the boosted input-g_m and deteriorated frequency-stability across loads is impeding. This is illustrated in Figure 2.13, where the dashed line refers to the bode plot of the OTA at zero load-current (I_L), i.e., I_L = 0, whereas the solid line refers to the bode plot at heavy load, such as I_L = 100 mA. $p_d = -1/(r_{o1}C_{o1})$ is the Left-Hand-Plane (LHP) dominant-pole, which appears at the gate of M_{PT}, where r_{o1} is the effective resistance at the node and C_{o1} is the lumped parasitic-capacitance at the node. Moreover, $p_o = -1/(r_{out}C_{out})$ is one of the non-dominant LHP-pole at the output node of the LDO, where r_{out} is the total resistance of the LDO itself in parallel with the effective load resistance derived from I_L; C_{out} is the lumped capacitance of the parasitic capacitance and the load capacitance, C_L. Furthermore, by adopting the PPF structure in Figure 2.13b, the non-dominant LHP-pole attributed by the PPF structure can be expressed as in (2.56) to be

$$p_N = -(g_{m8} - g_{m7} + g_{ds1} + g_{ds3} + g_{ds7} + g_{ds8})/C_N, \quad \textbf{(2.56)}$$

where C_N refers to the lumped parasitic-capacitance at the drain terminal of M_{8A} or M_{8B}. And p_N stays relatively stationary as the load varies.

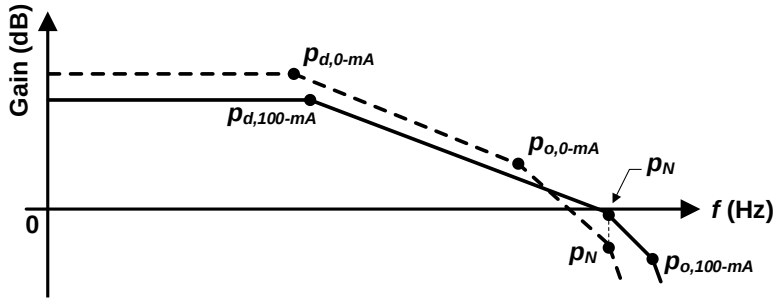

Figure 2.13 Bode plot of a PPF-incorporated LDO at no-load and 100-mA heavy-load.

At the heavy load, where the LDO is stable, it is inferable that $p_{o,100\text{-}mA}$ locates at relatively high-frequency or even beyond the cut-off frequency, f_t, as

shown in Figure 2.13. Under such scenario, $p_{o,100\text{-}mA}$ exerts negligible influence on the frequency stability, leaving p_N the first non-dominant-pole. Thus, it is relatively easy to ensure stability as the LDO can be approximated as a one-pole system. However, as the load decreases, the LDO become less stable. This is resulted from the emergence of the load-dependent $p_{o,0\text{-}mA}$ at low frequencies. In other words, $p_{o,0\text{-}mA}$ draws near to p_N. Essentially, the Phase Margin (PM) reduces to be close or even lower than zero, pushing the LDO to the verge of oscillation or instability. Therefore, effective approach to address the deteriorated frequency-stability while boosting input-g_m is still to be explored to make the PPF a useful element in an LDO design.

2.4.2 Cross-coupled Input-stage

1) FVF-based Topology

An OCL-LDO based on a pair of cross-coupled differential FVF [59] as the input stage of the EA [58] is listed in Figure 2.14. Such configuration is advantageous in accelerating the load transient response of an LDO. In other words, in comparison with conventional input-stage of an OTA without the cross-coupled configuration, such OTA achieves more-efficient pulling-down or pushing-up of the gate voltage, $V_{G,PT}$, of M_{PT}. This is due to the mutual enhancement between the two FVFs in the cross-coupled pair upon load transients.

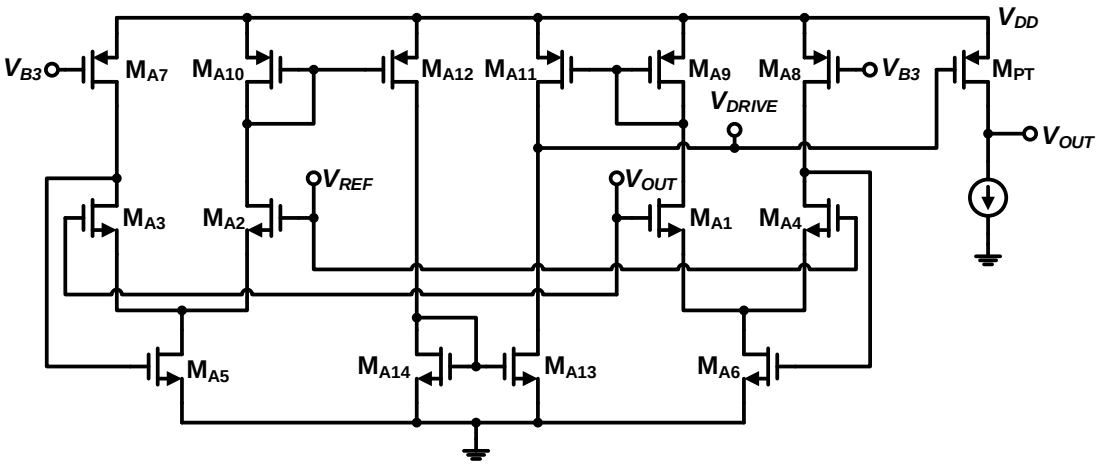

Figure 2.14 Circuit diagram of a FVF-based OCL-LDO [58].

To illustrate, assume a sudden increase of I_L at the LDO output-node. A drop in the gate voltage, $V_{G,A3}$ and $V_{G,A4}$ of M_{A3} and M_{A1} is immediately reflected

due to the undershoot of V_{OUT}. The drop in V_{OUT} is expected upon sudden increase in I_L as the OTA needs time to respond to the change in I_L by decreasing the gate voltage, $V_{G,PT}$, of M_{PT} to source more current to the load. As a result, I_L discharges the parasitic capacitances at the LDO output-node, resulting in a V_{out}-undershoot. The drop in $V_{G,A3}$ increases the on-resistance of M_{A3} and raises the gate voltage, $V_{G,A5}$, of M_{A5} subsequently as the current through M_{A3} is kept constant by a constant biasing voltage V_{B3}. The rise in $V_{G,A5}$ increases current through M_{A10}-M_{A2} and, in turn, increases current through M_{A13}. This helps to pull down $V_{G,PT}$ by discharging the parasitic capacitance at the gate of M_{PT}. Meanwhile, the drop in $V_{G,A1}$ helps to lower the current through M_{A9} and, subsequently, the current in M_{A11}. As a result, less current will be sourced to $V_{G,PT}$ to facilitate pulling-down of it by the current in M_{A13}. In this manner, M_{A11} enhances M_{A13} to shorten the undershoot-recovery time.

Similar mechanism can be derived upon a sudden decrease in I_L. The push-pull output-stage of the OTA operates to charge up $V_{G,PT}$ under such scenario to accelerate recovery from V_{OUT}-overshoot. In this manner, M_{A13} enhances M_{A11} in shortening the overshoot-recovery time.

Despite the fast-settling transient response, the OCL-LDO structure in Figure 2.14 can demand a relatively-high V_{DD} that makes it challenging to operate under sub-1 V. By assuming a 180-nm CMOS process, $V_{DD,min} = V_{GS} + 2*V_{DS} \approx 0.9$ V, where $V_{GS} \geq 0.5$ V and $V_{DS} = 0.2$ V. This is necessary to ensure all transistors operating in the saturation region. The LDO reported in [58] operates under V_{DD} no lower than 1 V despite a fast-settling time of 2.7 µs during load transient responses.

2) G_m-cell-based Topology

The cross-coupled differential-input transconductance cell (G_m-cell) presented in [57] operates in a similar manner to the FVF-based cross-coupled structure. The circuit diagram is shown in Figure 2.15.

To illustrate, upon a sudden increase in I_L, V_{OUT} undershoots due to the response delay of the OTA. The drop in V_{OUT} reduces the source voltage, $V_{S,PLa}$, and, subsequently, reduces the gate voltage, $V_{G,PLb}$, of M_{PLb}. This increases the

current through M_{N5} through the current-mirror M_{N3}-M_{N5} to discharge the parasitic capacitance and pulls down $V_{G,PT}$. Meanwhile, the drop in $V_{S,PHb}$ causes current through M_{P5} to decrease via current-mirrors, M_{N4}-M_{N6} and M_{P6}-M_{P5} as $V_{G,PHb}$ is fixed by the biasing condition. This enhances the pulling-down effort of the current through M_{N5} to ensure fast recovery.

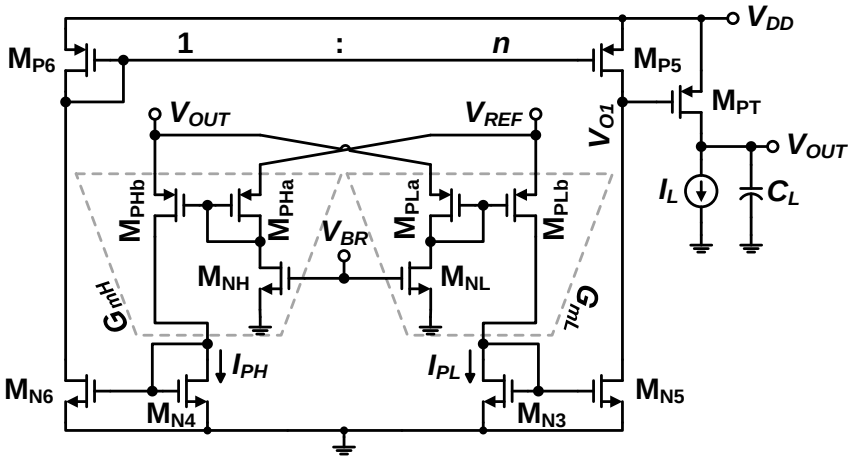

Figure 2.15 Circuit diagram of a G_m-cell-based OCL-LDO [57].

Likewise, a sudden drop in I_L raises V_{OUT} and $V_{S,PHb}$. Subsequently, current through M_{P5} increases via current-mirrors, M_{N4}-M_{N6} and M_{P6}-M_{P5}. Such current charges up $V_{G,PT}$. Meanwhile, the rise in $V_{S,PLa}$ raises $V_{G,PLb}$ and reduces current through M_{N5} via the current-mirror M_{N3}-M_{N5}. Reduction in current through M_{N5} enhances the pushing-up effort by the current through M_{P5}.

In comparison with the OCL-LDO shown in Figure 2.14, $V_{DD,min}$ for the LDO in Figure 2.15 is lower as $V_{DD,min} = |V_{GS}| + V_{DS} \approx 0.7$ V, where $V_{GS} \geq 0.5$ V and $V_{DS} = 0.2$ V for a 180-nm CMOS process. The reported LDO based on this structure [57] ensures a fast-settling of 4 µs upon a 50-µA-to-50-mA load transient with a low quiescent-current of 1.2 µA. However, the measurement result reported is obtained under 1.2-V V_{DD}, whereas performance under sub-1-V V_{DD} is not indicated. Modifications on such structure is shown in [60]. By enhancing the dynamic biasing current obtained from the G_m-cell, such modification boosts the load-transient-response further. A 20-ns settling time upon a 9-mA-to-40-mA load-transient is achieved. Nonetheless, the overall LDO is current-hungry and draws 158-µA quiescent current; and the reported

performance is not under sub-1-V V_{DD}, either. Moreover, the current-sourcing voltage reference required by [60] is unconventional but left unaddressed. Thus, to validate the G_m-cell-based OTA structure for a sub-1-V LDO, more investigation is necessary. This falls into the scope of this work.

2.4.3 Frequency Compensation

The stability analysis of an LDO usually includes the evaluation of two important poles in the frequency domain of the LDO loop-gain. One of the two poles, p_o, comes from the output node of the LDO; and the other, p_d, is from the gate of the pass transistor, M_{PT}.

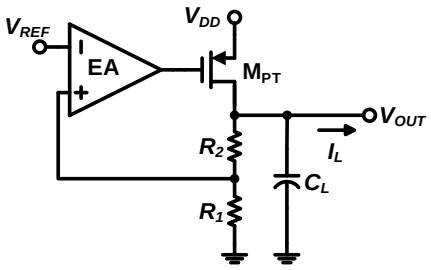

Figure 2.16 Block diagram of an LDO.

Typically, for a conventional LDO, which requires an output compensation capacitor at the output node, V_{OUT}, to guarantee frequency stability, p_o turns out to be its dominant pole and p_d the first non-dominant one. In contrast, for an Output-Capacitor-Less (OCL) LDO which relies on the internal on-chip compensation capacitors or no capacitor at all to ensure stability, p_d normally becomes the dominant pole and p_o the first non-dominant pole [61].

1) Equivalent Series Resistance (ESR) Approach

Dominant-pole compensation is one of the most straightforward compensations for a conventional LDO. It can be done by adding a shunt capacitor C_L at the output node, V_{OUT}. Besides, an additional LHP zero is created by C_L and its ESR as shown in Figure 2.17. The LHP zero is normally less than the cut-off frequency, f_t; and it helps to mitigate the effect of the first non-dominant-pole and improves the PM to maintain frequency stability.

Such approach suffers several weaknesses. Firstly, the inherent ESR of

C_L is not sufficiently large to create a strong LHP zero to achieve sufficient PM for stability. Secondly, even if the ESR becomes large enough, the load-transient responses can be sabotaged as the overshoot and overshoot at the LDO output will increases drastically [61, 62]. Thirdly, PSR is degraded with a large ESR also. In addition, the ESR varies with temperature. This will result in shifting of poles and zeros in the frequency domain such that the original objective of pole cancellation by the ESR can be forfeited [63].

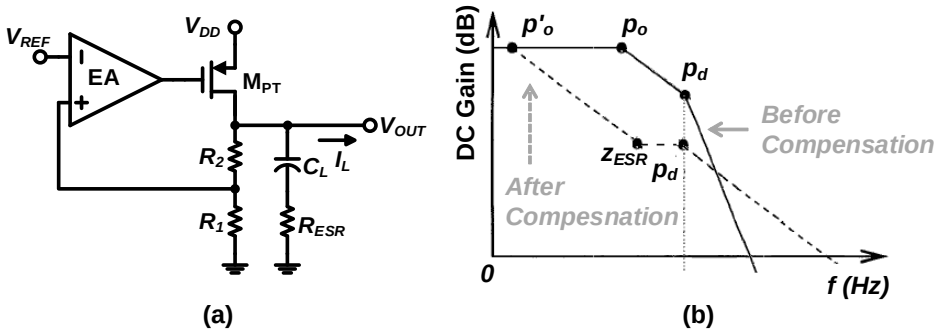

Figure 2.17 Dominant-pole compensation in (a) block diagram and (b) bode plot.

2) Gain-boosting Compensation

In an effort to derive sufficient open-loop DC-gain, a gain stage, A_2, can be inserted as the second-stage of the EA, consisting of stages A_1 and A_2, shown in Figure 2.18. Such frequency-compensation scheme is referred as the gain-boosting compensation. With a boosted open-loop DC-gain from the EA, M_{PT} can now be biased in the triode region without worries on DC-gain reduction at large I_L. As a result, a smaller transistor size of M_{PT} is allowed. [62]

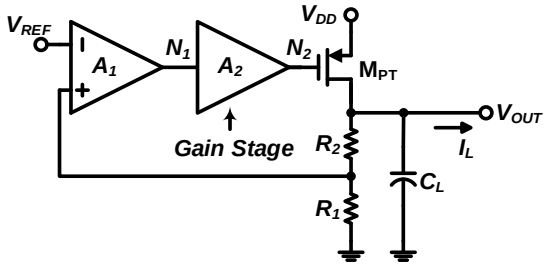

Figure 2.18 Gain-boosting Compensation in block diagram.

The gain-boosting compensation helps to reduce further $V_{G,PT}$ to lower the effective resistance and p_d at the gate of M_{PT} under a given I_L. PM can be

increased in this manner. Conversely, when PM becomes too large and slows down the transient responses, such compensation scheme can help to reduce PM to derive critically-damped response. This is achieved by increasing the DC gain to enlarge f_t, which can be estimated as the product of DC gain and the dominant-pole frequency for a single-pole system.

3) Nested-Miller-based Compensations

NMC shown in Figure 2.19a generally works fine in a closed-loop system when I_L is high. This is due to the large transconductance, $g_{m,PT}$, of M_{PT} and the high-frequency Right-Hand-Plane (RHP) zeros at heavy loads. However, as I_L decreases, $g_{m,PT}$ will decrease, which causes the RHP zeros shifting to lower frequencies to sabotage the stability.

To maintain stability at a low I_L, NMC with Null Resistor (NMCNR) is introduced first by inserting a null resistor to push the RHP zeros to high frequencies at the low I_L. In comparison with NMC, NMCNR allows smaller compensation capacitors to ensure stability, a higher voltage gain at high frequencies as well as a better PSR thanks to the null resistor [64]. The block diagram of NMCNR is similar to that shown in Figure 2.19a.

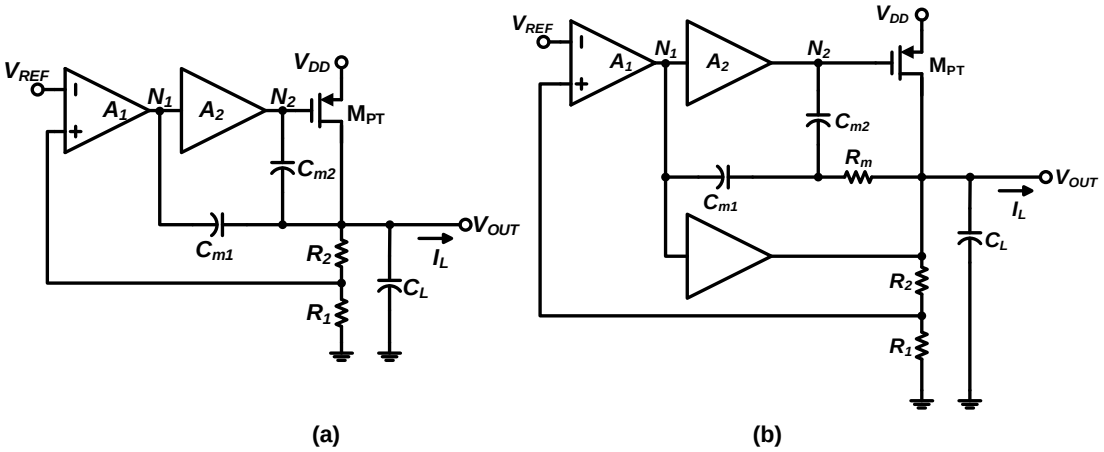

Figure 2.19 Block diagrams of NMC (a) in its original configuration and (b) with nulling resistor and feedforward transconductance stage.

To further enlarge f_t, NMCNR with the Feedforward Transconductance Stage (FTS), i.e., NMCNRF, is introduced by inserting FTS as shown in Figure 2.19b. The transconductance of FTS is designed larger than that of the second

gain-stage of the EA according to [64]. It is basically an integration of two stand-alone compensation techniques, namely, NMCNR and NMC with Feedforward Transconductance Stage (NMCF), both of which can be found in [64].

According to [63], the LDO is compensated when I_L = 0; as I_{OUT} increases, the LDO stays stable as its first non-dominant-pole always stays beyond f_t. The ESR zero coming from the output capacitor C_L does not affect the stability as it locates beyond the f_t as well. This is the case because the C_L does not need to be large with NMCNRF being implemented and so does its ESR. In addition, as all critical poles solely depend on the transconductance of the gain stages, which share the same temperature coefficient, stability of the LDO can be maintained across a wide range of temperatures.

Alternatively, the cut-off frequency, f_t of the LDO can be widened by removing the bandwidth-limiting compensation capacitor C_{m2} in the NMC. However, eliminating C_{m2} leads to the damping factor of the complex poles left uncontrolled since "complex-pole approach" [64] is adopted in the NMC. Subsequently, frequency peaking would occur due to the low damping factor or, equivalently, the high quality factor Q, which harms the frequency stability. Therefore, the Damping Factor Control (DFC) compensation approach is developed to lower the frequency peaking so as to retain the effectiveness of Miller compensation without C_{m2}. One way of doing so is by putting in a DFC block in the LDO structure as displayed in Figure 2.20.

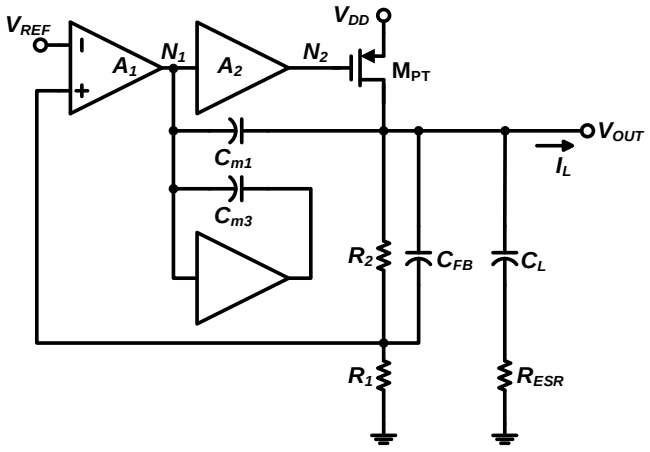

Figure 2.20 Block diagram of DFC compensation.

Now, the damping factor of the complex poles are effectively controlled by the transconductance of the negative gain stage of the DFC block and C_{m3}. Further, the damping factor should be properly controlled to be neither too small nor too large. In detail, when the damping factor is too small, the existing frequency peaking will still harm the stability; yet, when it is too high, the complex poles will become two separate poles to degrade the f_t. Thus, an optimum damping factor is typically set as $1/\sqrt{2}$. In addition, capacitive feedback C_{FB} is also incorporated into the structure to introduce an LHP zero, z_{FB}, for the purpose of PM improvement at medium-frequencies [65].

To further elaborate the DFC compensation approach, four cases are investigated in detail [65]. As it is noticed, frequency peaking due to complex poles only comes into play when I_L is low regardless of the presence of C_L at node V_{OUT}.

i) Conventional LDO (i.e., $C_L > 0$), $I_L = 0$ or $I_L > 0$ slightly only: As shown in Figure 2.21a, the resulted complex poles p_{COMP} are cancelled by z_{FB} and the z_{ESR} collectively. All other non-dominant-poles and the additional pole, p_{FB}, introduced by the capacitive feedback are beyond f_t and, hence, negligible.

ii) Conventional LDO (i.e., $C_L > 0$), $I_L >> 0$: The resulted complex poles are pushed beyond f_t and, hence, negligible. The first non-dominant-pole is cancelled by z_{FB}. All other non-dominant-poles are beyond f_t and, hence, negligible.

iii) OCL-LDO (i.e., $C_L = 0$), $I_L = 0$: As shown in Figure 2.21b, the LDO is unstable. It requires a minimum quiescent current to keep it stable.

iv) OCL-LDO (i.e., $C_L = 0$), $I_L > 0$: As shown in Figure 2.21c, it is similar to case 2) except that f_t is wider than that in case ii).

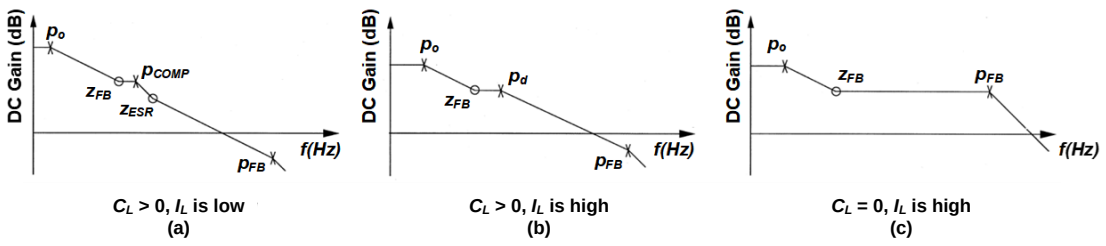

Figure 2.21 Bode plot of DFC compensation [65].

2.4.4 Concluding Remarks

TABLE 2.11 compares key performances of various LDO topologies with an emphasis on the load-transient responses. *K*-factor refers to the ratio between the measured settling-time over the smallest settling-time among all topologies in the table. In this manner, a load-transient-focused FOM is computed according to [60] as

$$FOM = K\left(\frac{\Delta V_{OUT} I_Q}{\Delta I_L}\right)\left(\frac{1}{L^2_{\text{technology}}}\right), \quad \textbf{(2.57)}$$

where ΔV_{OUT} is the maximum overshoot/undershoot during the load-transient response; ΔI_L is the transient step of I_L; $L_{technology}$ is the minimum channel-length of the process technology adopted to fabricate the reported LDO; K is the K-factor in the table.

TABLE 2.11 PERFORMANCE COMPARISON AMONG LDO TOPOLOGIES

	[66]	[67]	[57]	[58]	[60]
Technology (μm)	0.13	0.35	0.35	0.35	0.18
Active Area (mm²)	-	0.055	-	-	0.21
$V_{DD,min}$ (V)	1.15	1.6	1	1	1.6
V_{DO} (V)	0.15	0.4	0.1	0.2	0.2
V_{OUT} (V)	1	1.2	0.9	1	1.4
$I_{L,max}$ (mA)	50	12	50	100	50
$C_{OUT,max}$ (pF)	20	100	-	-	50
I_Q (@ no load) (μA)	37.32	28.6	1.2	1.4	130
Load Reg. (mV/mA)	0.0556	0.39	-	-	-
Line Reg. (mV/V)	8.1	0.31	-	-	-
Settling time (μs)	0.4	8	4	2.7	0.02
ΔV_{OUT} (mV)	56	~70	500	250	158
ΔI_L (mA)	50	12	50	100	31
PSR @ 1 kHz (dB) Full load	< -40	< -60	-	-	> -70
***K*-factor**	20	400	200	135	1
FOM (mV/μm²)	49	778	20	4	20

The FVF-based LDO topology in [58] displays the best FOM among all topologies. However, its $V_{DD,min}$ is too high to make it operate under sub-1 V as a viable solution for a WPT-powered WSN sensor node. So is the case with the LDO reported in [60]. Moreover, G_m-cell-based LDO topologies in [57] and [60]

offers equally good load-transient-responses according to their FOMs, but sub-1-V performances of [57] is left unknown whereas I_Q in [60] is too large to ensure a good current-efficiency. Notwithstanding relatively bad FOMs in [66] and [67], their performances are listed as a baseline for comparison only. Both topologies focus on PSR improvements with load-transient-responses left unaddressed.

As a result, the research work on LDO are prioritized in the following manner: 1) load-transient response, 2) current-efficiency, and 3) PSR. This is based on the consideration that trade-offs among fast-settling, PSR and current-efficiency is inevitable according to TABLE 2.11. On the one hand, to achieve both PSR and fast-settling, current-efficiency will drop significantly as in [60]; On the other hand, to guarantee fast-settling and current-efficiency, PSR of the LDO will be left unattended as in [57] and [58].

The load-transient response becomes the main focus to facilitate implementation of DPM, which aims at conserving power on the system-level. As DPM tends to switch on and off the loading ICs at various operation modes, fast-settling outputs from the PMU will be critical to ensure stable supplies to the loading ICs. Current-efficiency of the LDO becomes supplementary as it addresses power conservation on the component-level within the PMU. In addition, research on PSR performance only focus on low-frequency PSR, PSR_{LF}, which can be equally addressed by improving the DC-gain, A_{DC}, of the LDO [39] as

$$PSR_{LF} = \lim_{f \to 0\ Hz} \left[20 \log \left(\frac{dv_{dd}}{dv_{out}} \right) \right] = 20 \log \left(\frac{1}{A_{DC}} \right) \quad \textbf{(2.58)}$$

In other words, this work chooses to investigate the feasibility of incorporating PPF into an LDO to boost A_{DC}, while enhancing PSR_{LF} at the same time. In contrast, the high-frequency PSR, PSR_{HF}, is left unaddressed. After all, by considering the possibility to implement a noise-free rechargeable-battery as the power source to the LDO, high-frequency noise input to the LDO can be largely neglected.

2.5 Boost DC-DC Converter

When dedicated to drive digital loads, such as memories and µPs, from a

rectifier output, a boost converter often entails fast-settling load-transient-responses and small output-ripples. Firstly, a fast-settling load-transient-response ensures a stable supply to the loading memories and the µP upon sudden load-change as orchestrated by DPM. Moreover, small output-ripples ensure minimum supply-noises to the digital ICs. This helps in generating error-free outputs from the digital ICs. Furthermore, a low-output-ripple feature also serve as a safeguard in case of a fluctuating rectifier output in case such boost converter is powered by a rectifier directly under the scenario of a WPT-powered WSN sensor node.

Besides, area-efficiency will be preferred when the sensor node-size is concerned for the large-volume deployment of the WSN. This can be facilitated by minimizing the number of area-consuming discrete-components, such as capacitors and resistors that build the compensator within a conventional boost converter. In other words, a compensator-less design, such as the design rationale introduced in [68] is worth exploring.

2.5.1 Adaptive-Capacitance-based Transient Enhancement

Boost Converters reported in both [69] and [70] implement adaptive capacitance upon detection of a load-transient. In both cases, the load-transient is detected by a window comparator composed of COMP1 and COMP2 as shown in Figure 2.22. Such window comparator can be found in the Adaptive Capacitor Control (ACC) block in the boost converter in Figure 2.23.

In case of the WTE-based boost converter from [69], the load-transient-response is enhanced by turning off M_{P34} shown in Figure 2.24 upon the load-transient detection. In this manner, the effective capacitance in series with R_1 is reduced to two times of C_1 from six times of C_1 to boost the slew rate of the output voltage, V_{EA}, from the EA. Besides, during a light-to-heavy load-transient response, frequency stability of the boost converter is maintained by the WTE controller to increase the switching frequency, f_S. In a similar fashion, f_S is reduced by WTE controller upon a heavy-to-light load-transient for stability considerations.

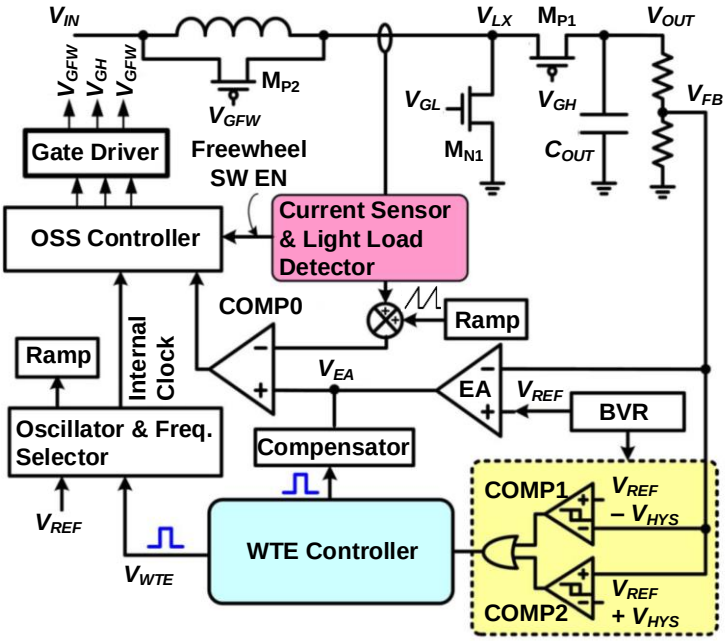

Figure 2.22 Block diagram of a current-mode boost converter with transient improvement by Window Transient Enhancement (WTE) and Overshoot Suppression (OSS) technique [69].

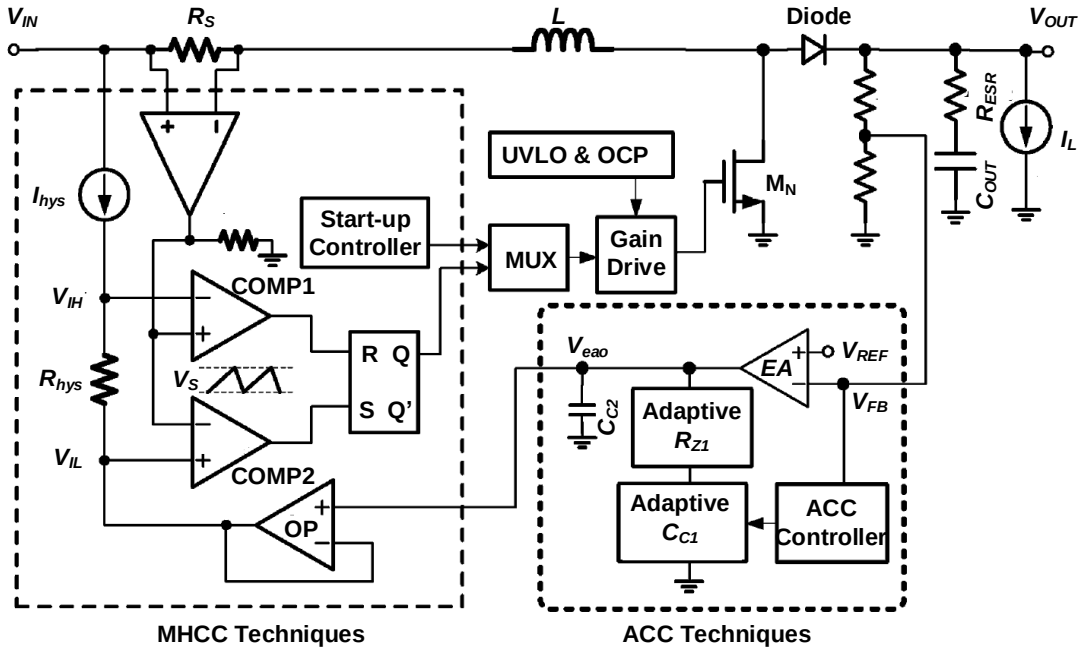

Figure 2.23 Block diagram of a boost converter with transient improvement by Modified Hysteretic Current Control (MHCC) [70].

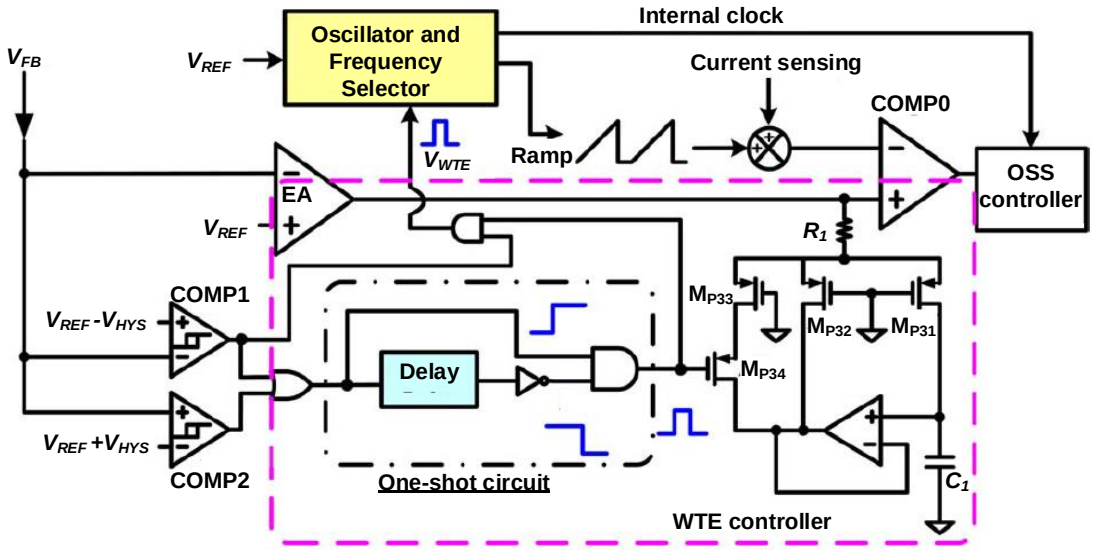

Figure 2.24 Block diagram of WTE controller [69].

In case of the ACC-based boost converter from [70], the adaptive capacitance C_{C1} shown in Figure 2.23 and Figure 2.25 is reduced to 2.1 pF within the duration of "Transient 1" labelled in Figure 2.25 upon detection of a load-transient. Subsequently, as V_{OUT} recovers, C_{C1} is increased to 6.4 pF during "Transient 2" to ensure enough PM and stability.

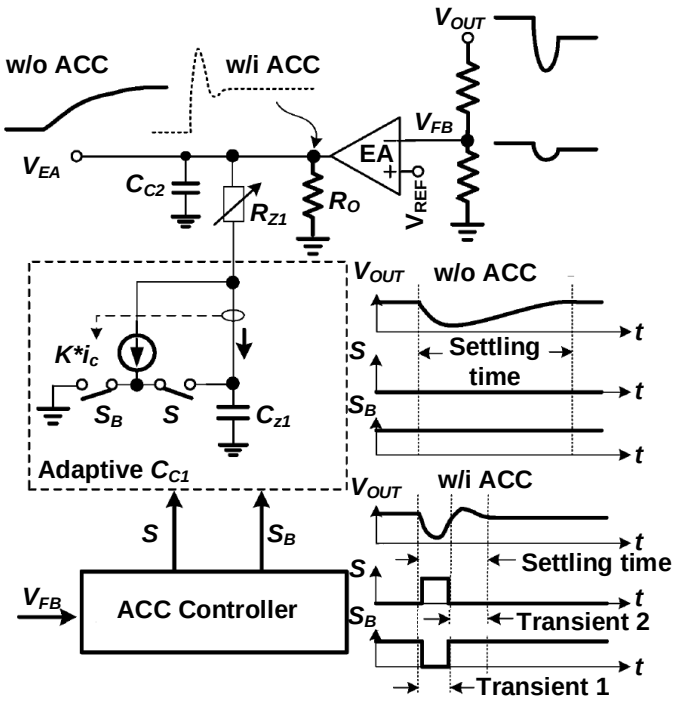

Figure 2.25 Working mechanism of the ACC controller [70].

2.5.2 Overshoot Suppression (OSS) Transient Enhancement

Other than adjusting the slew rate of V_{EA} to enhance load-transient-response, overshoot is also suppressed in [69] through the introduced OSS technique as shown in Figure 2.26.

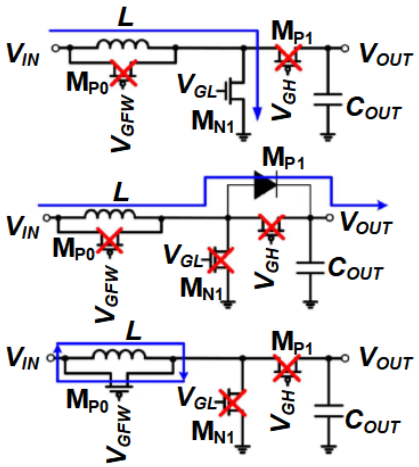

Figure 2.26 Working mechanism of OSS technique [69].

Upon detection of a V_{OUT}-overshoot during a heavy-to-light load transient, the OSS technique operates during the first time-interval as per conventional design based on the upper diagram in Figure 2.26. Here, input voltage, V_{IN}, ramps up the inductor current, I_{Ind}, through M_{N1} and stores energy in the inductor L. This is followed by the second time-interval based on the middle diagram, when all switches are off and L releases energy and extra charge to charge up the output capacitor, C_{OUT}. Different from the conventional approach, the duration of the second time-interval is fixed and set by design to limit the amount of extra charge being passed to the C_{OUT}. During the third time-interval as indicated by the lower diagram, the free-wheeling MOS-switch M_{P1} is on to dissipate extra energy within L itself and avoids any extra charge from being sent to C_{OUT}. In this manner, in both the second and the third time-interval, the OSS functions to limit the amount of extra charge discarded onto C_{OUT} to suppress the V_{OUT}-overshoot.

2.5.3 Dual-loop Compensator-less Control

To speed up the load-transient-response, the boost converter in [68] decouples

the current loop and the voltage loop by sensing i_{Ind} and v_{OUT} separately as shown in Figure 2.27a. The high-bandwidth current-loop implements peak-current-control by comparing the voltage across the inductor, $i_{Ind}*R$, with the reference voltage, V_{IREF}, which often equals V_{IPK} as long as $v_S < V_{REF1}$ as shown in Figure 2.27b, where R is the sensing resistance. In this manner, the output from comparator Q_2 derives the control signal, v_{GM}, to S_M. In fact, the undershoot recovery during the load-transient-response is carried out in the same manner, the speed of which solely relies on the bandwidth of the current-loop.

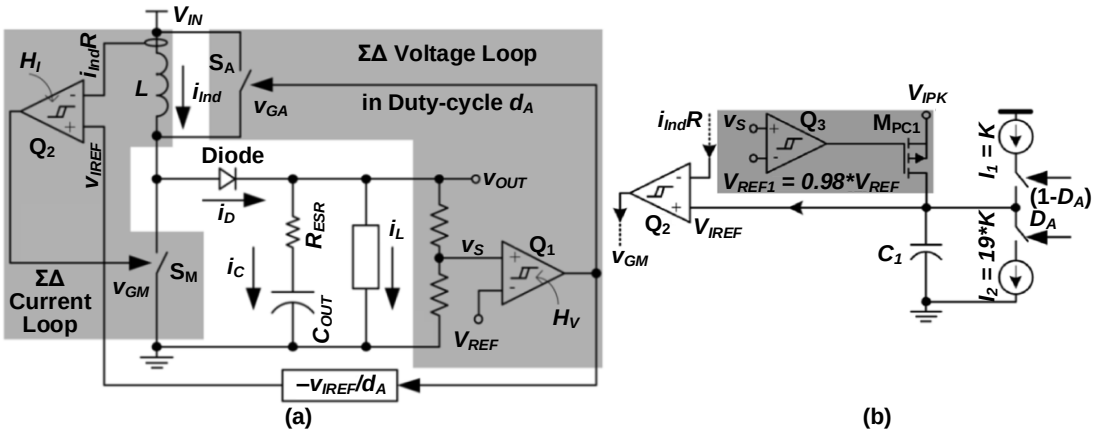

Figure 2.27 Block diagram of dual-loop control [68].

In comparison, the low-bandwidth voltage-loop only comes into play when $v_S > V_{REF1}$ according to Figure 2.27b, which illustrates how "$-v_{IREF}/d_A$" is implemented in Figure 2.27a. Upon such instance, it switches on S_A through v_{GA} to avoid further increase in v_{OUT}. Hence, the condition of $v_S > V_{REF1}$ can be treated as a boundary condition to detect overshoot during the load-transient-response as well. And it functions in a similar fashion to the OSS technique illustrated in the lower diagram in Figure 2.26. Thus, the low-bandwidth voltage-loop allows the inductor current, i_{Ind}, to react quickly against sudden overshoot and independently from current-loop.

2.5.4 Concluding Remarks

Both the WTE technique [69] and the ACC controller [70] implement adaptive capacitors in their PI compensators to boost the slew rate of V_{EA} from the EA output momentarily upon load transients. However, the capacitor-multiplication-

ratio-reduction method in [69] appears ineffective to speed up the overshoot recovery which still takes more than 100 µs, and the boost converter with ACC controller in [70] leads to a large 1.6% output ripple of its nominal value at the steady state.

On the one hand, addressing the EA output response upon transients help to speed up load-transient-responses. On the other hand, compensator-based design approaches do suffer a few disadvantages, such as: 1) trade-offs among recovery time, overshoot and undershoot ripples, and stability during load transients, and 2) potential large static power losses when high-speed circuits are involved.

As a result, compensator-less control approaches are investigated. The boost converter in [68] removes compensators by decoupling the inductor current and output voltage via two independent control loops instead. By eliminating bulky and power-consuming compensators, such approach offers a feasible framework to design boost converters for WSN PMUs considering the area constraints of WSN as well as the light-load power efficiency requirements. Nonetheless, output ripples as large as 1.7% of the nominal output-voltage are still observed.

Therefore, a compensator-less control approach with low output ripples is still in need while ensuring fast-settling load-transient-responses. In addition, a more effective approach to address the slew rate of V_{EA} is desirable to enhance the fast-settling.

2.6 Summary

Be it a battery-equipped or battery-less WSN node, an accurate and Process-V_{DD}-Temperature (PVT)-invariant VR is crucial. In this chapter, investigations on previous works have revealed that a BVR-like CMOS VR structure introduced in [52] is a good candidate. Firstly, in comparison with a BVR, a CMOS VR is more flexible and functional under a sub-1-V V_{DD}, which is inevitable for a WPT-powered WSN sensor node. Also, the BVR-like structure makes such CMOS VR feasible to adopt various curvature-compensation-techniques previously

developed for BVRs to minimize the relatively-large TC of CMOS VRs. In this manner, the only main obstacle that is left to overcome will be the process variations. Nonetheless, it is speculated that such process-induced inaccuracies can be effectively improved by dedicated trimming-networks. And this can be the design focus worth delving into.

Moreover, as power conservation measures, such as DPM, is often employed in a WSN sensor, fast-settling load-transient-response as well as steady load regulation are necessary requirements in PMICs, such as LDOs and DC-DC converters. Various studies on transient-enhancement structures and techniques for LDOs and boost DC-DC converters have been presented in this chapter. A G_m-cell-based OCL-LDO structure [57] is considered as the fundamental topology to ensure fast-settling behavior in an LDO. This is due to its capability to work under sub-1-V V_{DD} as well as the mutual-enhancing cross-coupled input stage and the class-AB output stage of its EA. However, to ensure good line and load regulations under sub-1 V, such structure alone is insufficient. Incorporating PPF into the G_m-cell-based structure is found to be current-efficient in boosting the DC-gain under low supplies. However, to make the stability-threatening PPF useful, frequency stability has to be maintained across the wide load-range. To solve such trade-off, a load-adaptive controller on the PPF-structure may be needed. And this can be a meaningful focus on the LDO design in this work.

Furthermore, in search of transient-enhancement controllers for boost converters, it is found out that the slew rate of V_{EA} from the EA output plays a critical role. Indeed, by temporarily increasing the slew rate of V_{EA}, the transient recoveries can be effectively enhanced as demonstrated in [69] and [70]. On top of this, a compensator-less controller [68] is also investigated by considering the node-size constraints in WSN to facilitate the wide-spread deployment. A compensator-less boost converter is attractive as the number of discrete components to build such a boost converter is reduced. Thus, the concept of a compensator-less controller that enhances the V_{EA} slew-rate can be advantageous to a WPT-powered WSN sensor node, if developed successfully in this work.

Chapter 3 A CMOS VR with Proposed Trimming Circuits and Curvature Compensation Techniques

Conventional BVR topologies are robust against process variations with relatively low TC. However, the Base-Emitter Voltage (V_{BE}) to turn on the BJT has to be no less than 0.7 V. It becomes a bottleneck to lower V_{DD} further below 1 V. A BVR with resistive dividers [48] can realize sub-1-V operations but with a V_{DD} no lower than 0.98 V. In comparison, CMOS VRs, free from limitations imposed by V_{BE}, enable a much lower V_{DD} from 0.5 to 0.9 V [49, 51, 52]. Yet, deficiencies in CMOS VRs are still to be addressed to reach its full potential. The TC of a sub-1-V V_{GS}-based CMOS VR reported in [49] is V_{DD}-dependent. A TC of 10 ppm/°C is attainable only at V_{DD} = 2.45 V. Its LS is as high as 0.27% over V_{DD} = 0.9 ~ 4 V. Moreover, TCs of CMOS VRs are usually large, ranging from 44 to 248 ppm/°C in case of ΔV_{th}-based CMOS VRs [52].

Notwithstanding large variations in TC, ΔV_{th}-based circuit structure in [52], shown in Figure 3.1b, displays potential for practical implementations. This is due to its BVR-like topology which allows reuse of curvature-compensation techniques previously developed for BVRs to minimize TC by addressing non-idealities due to second-order effects, such as channel-length modulation.

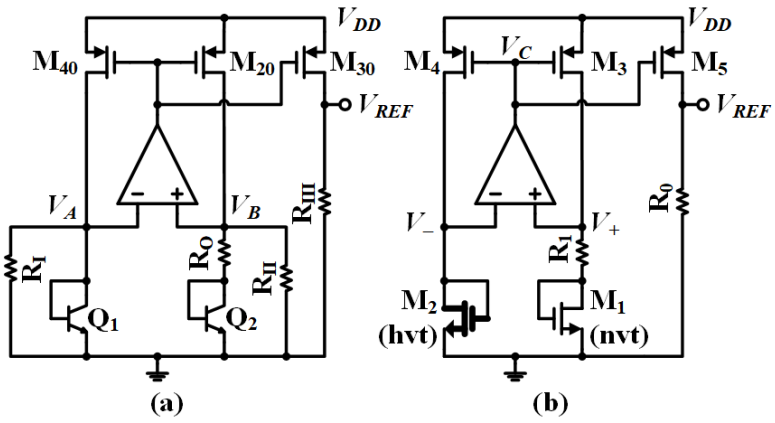

Figure 3.1 Circuit topologies of (a) conventional BVR and (b) ΔV_{th}-based BVR-like CMOS VR [52].

The main challenge, however, lies in achieving a stable TC over process

variations. Such is the case for most CMOS VRs. To address this, dedicated trimming-networks are proposed in this chapter. To improve TC further against secondary effects, such as channel-length modulation, curvature compensation techniques is proposed also. This chapter goes on to explain operations of the EA and start-up circuits adopted in the proposed design. In addition, a cost-effective implementation of the high-V_{th} NMOS is introduced in deriving the proposed BVR-like ΔV_{th}-based CMOS VR. Discussions on the simulation and measurement results of the design is covered afterwards. A conclusion is drawn towards the end of the chapter.

3.1 Derivation of Zero-TC Based on ΔV_{th}

As shown in Figure 3.1b, the ΔV_{th}-based CMOS VR derives a temperature-independent voltage across R_1 through the two NMOS transistors M_1 and M_2, both of which operate in the subthreshold region. However, M_2 is implemented with a high V_{th}, $V_{thn,hvt}$, whereas M_1 is with a normal V_{th}, $V_{thn,nvt}$.

Moreover, by assuming the drain-source voltage, V_{DS}, larger than $4V_T$, where $V_T = kT/q$ is the thermal voltage, the drain current, I_D, of subthreshold conduction can be calculated by (3.1) according to [52, 71]

$$I_D = I_{Do}(W/L)e^{(V_{GS}-V_{thn})/(m_s V_T)}, \tag{3.1}$$

where $I_{Do} = \mu_n C_{ox}(m_s\text{-}1)V_T^2$ [52]; μ_n is the electron mobility; C_{ox} is the gate-oxide capacitance per unit area; m_s is the subthreshold slope parameter; W and L are the channel width and length of the MOSFET respectively; V_{GS} is the gate-source voltage; k is the Boltzmann constant; T is the absolute temperature; q is the electronic charge. Subsequently, with the EA, EA1, to ensure that $V_- = V_+$ as shown in Figure 3.1b, the voltage across R_1, V_{R1} (= $V_{GS2} - V_{GS1}$), can be derived from (3.1) as

$$V_{R1} = \left(V_{thn,hvt} - V_{thn,nvt}\right) + m_s V_T \ln\left(\frac{I_{D2}\mu_{n1}C_{ox1}W_1L_2}{I_{D1}\mu_{n2}C_{ox2}W_2L_1}\right). \tag{3.2}$$

To verify the feasibility to achieve $d(\Delta V_{R1})/dT = 0$, we first examine the first term, ($V_{thn,hvt} - V_{thn,nvt}$), in (3.2). Conventionally, a high-V_{th} NMOS can be derived by implanting excessive acceptor dopants into the substrate to increase N_a,

which is the acceptor concentration in the p-type substrate of a normal-V_{th} NMOS. In this manner, the majority dopant concentration profile near the substrate surface becomes $N_{ai}(x)$, where x denotes the distance from the substrate surface [72]. This is illustrated in Figure 3.2, where the vertical axis denotes the dopant density; whereas the horizontal axis denotes the depth of the implant.

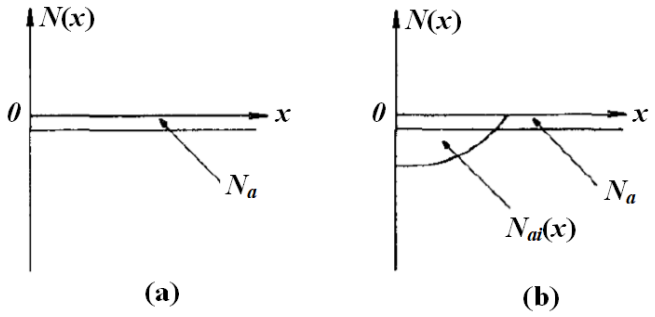

Figure 3.2 Illustration of dopant concentration profiles of (a) normal-V_{th} NMOS and (b) high-V_{th} NMOS. [72].

By ruling out body effect since source terminals of both M_1 and M_2 are grounded, the threshold voltage, V_{thn}, can be expressed according to [45] as

$$V_{thn} = V_{thn0} = |\Phi_{MS}| + 2|\Phi_F| + \frac{Q_{dep} - Q_{ss}}{C_{ox}}, \tag{3.3}$$

where $|\Phi_{MS}| = V_T \ln(\frac{N_{peak} N_a}{n_i^2})$ is the work-function difference between the n+-polysilicon gate and the silicon substrate [71]; Q_{SS} is surface-state charge density per unit area [71]; N_{peak} is the peak electron concentration in the channel at threshold [72]; $N_{peak} = N_a$ for an un-doped NMOS, and it equals N_{ai} for an implanted NMOS with N_{ai} being the average acceptor dopant concentration of the implanted NMOS; n_i is the intrinsic concentration of silicon; $|\Phi_F| = V_T \ln\left(\frac{N_a}{n_i}\right)$ is the Fermi potential of the substrate [73]; $Q_{dep} = 2\sqrt{q\epsilon_{Si}|\Phi_F|N_a}$ is the charge per unit area in the surface depletion-region; ϵ_{Si} is the dielectric constant of silicon. As a result, the first term on the right side of (3.2) becomes

$$\Delta V_{th} = V_{th,hvt} - V_{th,nvt} = \Delta|\Phi_{MS}| + \frac{\Delta Q_{dep}}{C_{ox}}, \tag{3.4}$$

where

$$\Delta\Phi_{MS} = \Phi_{MS,hvt} - \Phi_{MS,nvt}; \quad \textbf{(3.5)}$$

$$\Delta Q_{dep} = Q_{dep,hvt} - Q_{dep,nvt} = -q\int_0^{X_{hvt}}[N_{ai}(x) - N_a]dx + q\int_0^{X_{nvt}} N_a dx, \quad \textbf{(3.6)}$$

where X_{hvt} and X_{nvt} denote the edge locations of the implanted high-V_{th} NMOS and normal-V_{th} NMOS. In this manner, the TC of ΔV_{th} can be given by (3.7) based on [72]

$$\frac{d(\Delta V_{th})}{dT} = \frac{\epsilon_{Si}}{C_{ox}}\sqrt{\frac{qN_a}{2\epsilon_{Si}(\Phi_{MS,nvt})}}\cdot\left[\frac{1}{\sqrt{1-\frac{qN_{ai}X_i^2}{2\epsilon_{Si}\Phi_{MS,nvt}}}} - 1\right]\left(\frac{d\Phi_{MS,nvt}}{dT}\right), \quad \textbf{(3.7)}$$

where $\frac{d\Phi_{MS,nvt}}{dT} = \frac{1}{T}\left(\Phi_{MS,nvt} - 1.21\right) \approx -2.2\ \mathrm{mV/℃}$ at 300 K [72]. Hence, $d(\Delta V_{th})/dT < 0$, i.e. CTAT. As the second term in (3.2) remains the same as it is in [2106] and it is PTAT, a zero $d(\Delta V_{R1})/dT$ can be obtained by adjusting I_{D2}/I_{D1} and $W_1L_2/(W_2L_1)$ in (3.2) [52].

3.2 Proposed ΔV_{th}-based CMOS VR

The overall circuit-diagram of the improved VR is displayed in Figure 3.3b. The feasibility of the new high-V_{th} NMOS, such as M_2, in achieving the zero-TC reference output is first justified in this section. This is followed by a detailed illustration on the proposed R_1 and R_0 trimming networks as well as the curvature-compensation technique to minimize TC against PVT variation. The trimming networks are not only compatible with sub-1-V operations, but TCs of MOS switches involved also have to be minimized and compensated for not sabotaging the TC of the overall VR. The curvature-compensation technique, realized by EA2 and M_6, overcomes the channel-length-modulation effect in M_5 to guarantee that $I_{D3}/I_{D5} = W_3L_5/(W_5L_3)$. Besides, the EA structure shown in Figure 3.3a is also explained. It is implemented by both EA1 and EA2. Start-up circuits are presented towards the end of this section.

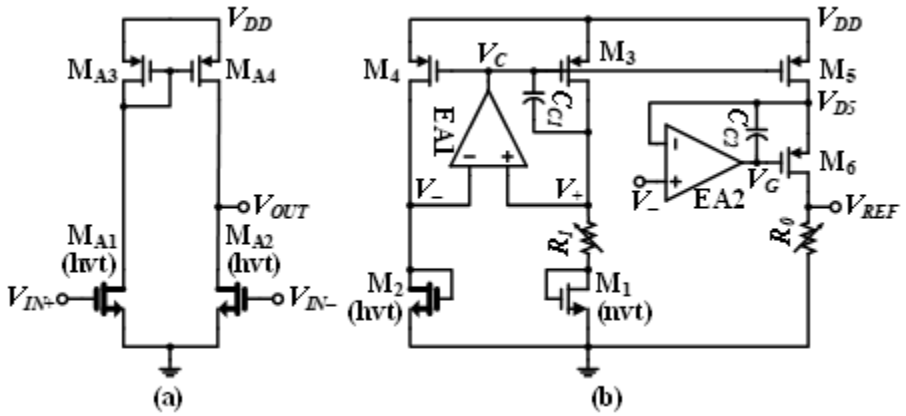

Figure 3.3 Circuit diagrams of (a) the EA implemented and (b) the proposed ΔV_{th}-based CMOS VR.

3.2.1 Derivation of the Zero-TC with Proposed 5-V NMOS

Other than the dopant implantation, a high V_{th} can also be derived by reducing C_{ox} in (3.3). This is achieved through increasing the gate-oxide thickness, t_{ox}, according to (8)

$$C_{ox} = \epsilon_r \epsilon_o / t_{ox}, \tag{3.8}$$

where $\epsilon_o = 8.85 \times 10^{-18}\,\mathrm{F/\mu m}$ is the absolute permittivity; ϵ_r = 3.97 is the relative permittivity of SiO_2; t_{ox} is the gate-oxide thickness. In this work, a NMOS with a higher voltage-rating such as a standard 5-V NMOS is proposed and implemented as the high-V_{th} NMOS. It is with a thicker t_{ox} than its standard 1.8-V counterpart, which is implemented as the normal-V_{th} NMOS in this work. The standard 5-V NMOS offers a more cost-saving solution in comparison with a high-V_{th} 1.8-V NMOS implemented in the previous work [52]. A high-V_{th} 1.8-V NMOS can be less desirable as it entails more expensive process steps, such as dopant implantation, to fabricate.

However, different from the high-V_{th} 1.8-V NMOS, a standard 5-V NMOS is usually derived by growing a thicker t_{ox} than that of a standard 1.8-V NMOS. This results in a higher V_{th}. Thus, it is necessary to re-evaluate (3.4) in a more general form by including the change in t_{ox}, Δt_{ox}, as shown in (3.9)

$$\Delta V'_{th} = \Phi_{MS,hvt} - \Phi_{MS,nvt} + \frac{Q_{dep,hvt}}{C'_{ox}} - \frac{Q_{dep,nvt}}{C_{ox}}, \tag{3.9}$$

where $C'_{ox} = \epsilon_r\epsilon_o/(t_{ox} + \Delta t_{ox}) < C_{ox}$; Δt_{ox} is the rise in the gate-oxide thickness. The meaning for the rest of the terms remain unchanged. Rearrange (3.9) to find the equivalent high-V_{th} 1.8-V NMOS counterpart (with the same t_{ox} as the standard 1.8-V NMOS but a higher V_{th}) for the standard 5-V NMOS to obtain

$$\Delta V'_{th} = \Phi'_{MS,hvt} - \Phi_{MS,nvt} + \frac{Q'_{dep,hvt}}{C_{ox}} - \frac{Q_{dep,nvt}}{C_{ox}} + \Phi_{MS,hvt} - \Phi'_{MS,hvt}, \quad \textbf{(3.10)}$$

where the equivalent surface-charge density in the depletion region is given as $Q'_{dep,hvt} = 2\sqrt{q\epsilon_{Si}|\Phi_F|N'_{ai}} = Q_{dep,hvt}(\frac{t_{ox}+\Delta t_{ox}}{t_{ox}})$, which removes Δt_{ox} and mathematically incorporates it into the acceptor dopant concentration, N_{ai}, to derive an equivalent N_{ai}' as $N'_{ai} = N_{ai}\left(\frac{t_{ox}+\Delta t_{ox}}{t_{ox}}\right)^2$. Moreover, with $\left|\Phi'_{MS,hvt}\right| = V_T\ln(\frac{N'_{ai}N_a}{n_i^2})$ given,

$$\frac{d(\Phi_{MS,hvt}-\Phi'_{MS,hvt})}{dT} = \frac{d\left[V_T\ln\left(\frac{N_{ai}}{N'_{ai}}\right)\right]}{dT} = \frac{2k}{q}\ln\left(\frac{t_{ox}}{t_{ox}+\Delta t_{ox}}\right) < 0. \quad \textbf{(3.11)}$$

Subsequently, the TC of $\Delta V'_{th} = V'_{th,hvt} - V_{th,nvt}$, where $V_{th,hvt}$ denotes the threshold voltage of the 5-V NMOS, becomes

$$\frac{d(\Delta V'_{th})}{dT} = \frac{\epsilon_{Si}}{C_{ox}}\sqrt{\frac{qN_a}{2\epsilon_{Si}(\Phi_{MS,nvt})}}\cdot\left[\frac{1}{\sqrt{1-\frac{qN'_{ai}X_i^2}{2\epsilon_{Si}\Phi_{MS,nvt}}}} - 1\right]\left(\frac{d\Phi_{MS,nvt}}{dT}\right) + \frac{d(\Phi_{MS,hvt}-\Phi'_{MS,hvt})}{dT} < 0. \quad \textbf{(3.12)}$$

Therefore, it can be proved, in a more general form, that the threshold voltage difference between a high-V_{th} NMOS and a normal-V_{th} NMOS is CTAT. It is regardless of how a high-V_{th} is obtained, be it dopant implantation or gate-oxide thickening. Hence, $d(\Delta V_{R1})/dT = 0$ can be achieved based on (3.2) by adjusting I_{D2}/I_{D1} and $W_1L_2/(W_2L_1)$ [52]. This is proved by simulation results of VR at the typical corner (in grey color) across the temperature range shown in Figure 3.4b. Subsequently, $d(\Delta V_{REF})/dT = 0$ can also be obtained through the current-mirror formed by M_3 and M_5 in Figure 3.3b according to

$$V_{REF} = \frac{V_{R1}}{R_1}\left(\frac{I_{D1}}{I_{D5}}\right)R_0 = \left(\frac{R_0}{R_1}\right)\left(\frac{I_{D3}}{I_{D5}}\right)(V_{GS2} - V_{GS1}), \quad \textbf{(3.13)}$$

where $I_{D3} = I_{D1}$ is the drain current through M_3; I_{D5} is the drain current through M_5. R_0 and R_1 are resistors implemented with the same type of material to cancel

out their inherent TCs.

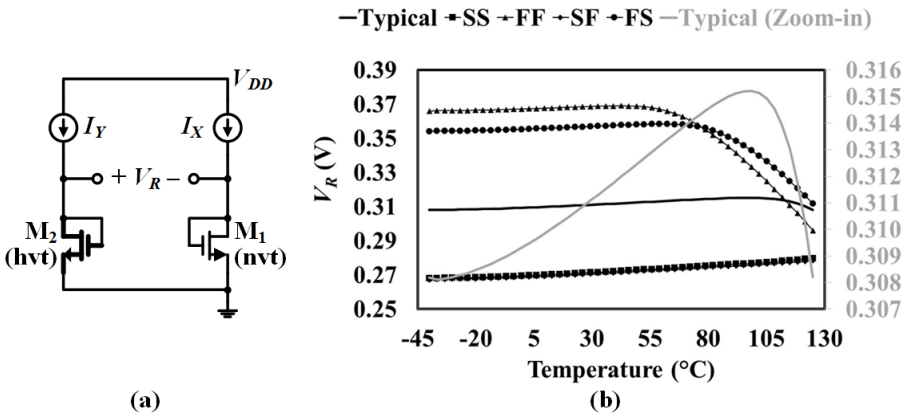

Figure 3.4 Zero-TC derivation in (a) circuit setup, where I_Y/I_X = 3:2, I_X = 66 nA and I_Y = 99 nA with (b) simulation results across all MOSFET process corners.

3.2.2 Proposed Trimming Networks for R_1

Failure caused by process variations in R_1 are twofold. On the one hand, thermal characteristics of MOSFET varies significantly as reflected in Figure 3.4b. By considering process variations in R_1 itself, it will result in a R_1 that is much larger than the drain-source resistance of M_1 at process corners with 'fast NMOS'; a large portion of V_{DD} along the branch of M_3-R_1-M_1 can be taken by R_1. It will squeeze down V_{DS1} till $V_{DS1} < 4V_T$, rendering the assumption to establish (3.1) invalid. Under such scenarios, (3.2) does not hold any more. This is due to the fact that V_{DS1} has to be included in (3.1) and (3.1) has to take a more general form [74] to become

$$I_{D1} = I_{Do}\left(\frac{W_1}{L_1}\right) e^{\frac{\left(V'_{GS1}-V_{thn}\right)}{m_S V_T}} \left(1 - e^{-\frac{V_{DS1}}{V_T}}\right), \tag{3.14}$$

where $V_{th,hvt}$ refers to the threshold voltage of the standard 5-V NMOS. By merely assuming $2V_T \leq V_{DS1} < 4V_T$ with $V_{DS1} = V_{GS1}$ since V_{G1} and V_{D1} of the NMOS are shorted, I_{D1} can be approximated as

$$I_{D1} \approx 0.78 \times I_{Do}\left(\frac{W_1}{L_1}\right) e^{\frac{(1+0.06m_S)V'_{GS1}-V_{thn}}{m_S V_T}}. \tag{3.15}$$

This is due to the fact that $\left(1 - e^{-\frac{V_{DS1}}{V_T}}\right) \approx 0.78e^{\frac{0.06V_{DS1}}{V_T}}$ for $2 \leq V_{DS1}/V_T \leq 4$ derived through MATLAB® approximation and plotted in Figure 3.5, where the

dotted line in grey color plots '1 - exp(-V_{DS}/V_T)', whereas the solid line plots '0.78exp(-0.06V_{DS1}/V_T)'.

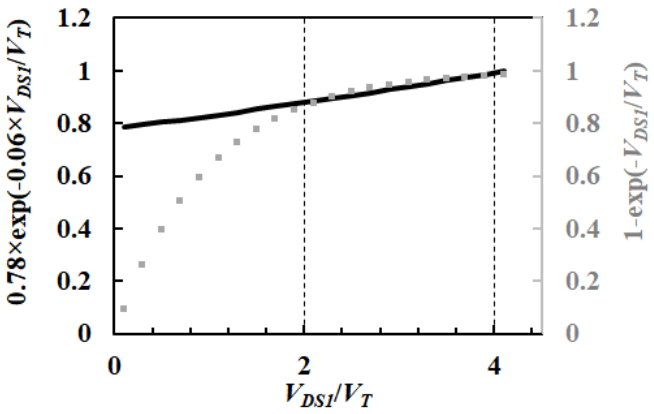

Figure 3.5 Approximation of '1 - exp(-V_{DS1}/V_T)' through MATLAB®.

As it is likely to maintain $V_{DS2} = V_{GS2} > 4V_T$ for M_2 due to the absence of a large resistor between M_4 and M_2, (3.1) is valid for computing V_{GS2}. Thus, (3.2) can be recalculated to become

$$\begin{aligned} V'_{R1} &= V_{GS2} - V'_{GS1} \\ &= \left[\left(V_{thn\_hvt} - V_{thn\_nvt}\right) + 0.06m_s V_{thn\_hvt}\right]/(1 + 0.06m_s) + \\ &\quad [m_s V_T/(1 + 0.06m_s)] \ln\left(\frac{0.78\times e^{1+0.06m_s} I_{D2}\mu_{n1}C_{ox1}W_1L_2}{I_{D1}\mu_{n2}C_{ox2}W_2L_1}\right). \end{aligned} \quad \textbf{(3.16)}$$

Since $dV_{thn\_hvt}/dT \approx -\frac{k}{q}\ln\left(N_{peak}/N_A\right) < 0$ [71], it is inferable that the first term on the right side in (3.16) is CTAT whereas the second term can be made PTAT through proper ratio-setting. With reference to (3.2) and (3.16),

$$\frac{dV'_{R1}}{dT} = \frac{k}{q}\frac{m_s}{1+0.06m_s}\ln\left(\frac{2\cdot e^{0.06m_s}N_A}{N_{ai}}\right). \quad \textbf{(3.17)}$$

Thus, unless dedicated implantation processes are implemented to have $N_{ai} = 2\cdot e^{0.06m_s}N_A$, it is more likely that $TC = \frac{dV_{REF}}{dT} = \left(\frac{R_0 I_{D3}}{R_1 I_{D5}}\right)\frac{dV'_{R1}}{dT} \neq 0$ in general. In other words, to ensure that (3.2) still holds, it will be more reasonable to trim R_1 to have $V_{DS1} > 4V_T$ than to control accurately the costly dopant-implantation to achieve $N_{ai} = 2\cdot e^{0.06m_s}N_A$. This is particularly critical under sub-1-V operations as V_{DS1} tends to be squeezed below $4V_T$ due to the low V_{DD}.

On the other hand, R_1 that becomes too small at certain process corners can result in a large drain current through M_1 and drive M_1 out of the subthreshold region into saturation region. Under such scenario, R_1 needs to be trimmed also to increase R_1 to validate (3.2) for M_1 and M_2.

In this work, I_{D1}/I_{D2} = 1.5 is chosen. Subsequently, M_1 and M_2 are sized accordingly to nullify TC for V_{REF}. They are implemented in large sizes to ensure good matching [52]. To compensate process variations, the proposed VR is simulated at 15 process corners.

TABLE 3.1 LIST OF OPTIMAL R_1 AND R_0 ACROSS PROCESS CORNERS

Process Corners			R_1 (kΩ)	R_0 (kΩ)
Resistor [a]	1.8-V MOSFET [b]	5-V MOSFET [b]		
SS	FF	FF	792	332
TYP	FF	FF	820	332
FF	FF	FF	877	360
SS	FS	FS	1018	445
TYP	FS	FS	1075	473
FF	FS	FS	1103	502
SS	TYP	TYP	2263	1294
TYP	TYP	TYP	2518	1407
FF	TYP	TYP	2942	1690
SS	SF	SF	2942	2029
SS	SS	SS	3169	2171
TYP	SF	SF	3395	2312
TYP	SS	SS	3536	2425
FF	SF	SF	3961	2680
FF	SS	SS	4102	2793

a. For resistor process corners, SS and FF refers to resistor slow case and fast case models accordingly; TYP refers to resistor typical case models.

b. FF, SS, FS, and SF refer to the process corner with fast NMOS and fast PMOS, slow NMOS and slow PMOS, fast NMOS and slow PMOS, and slow NMOS and fast PMOS accordingly; TYP refers to the typical NMOS and PMOS performances.

At each process-corner, the optimal R_1 that minimizes $d(\Delta V_{R1})/dT$ is recorded as shown in TABLE 3.1. Subsequently, the Least Significant Bit (LSB) resistance for R_1, R_{1_LSB} = 1%$R_{1,typical}$ is derived. $R_{1,typical}$ is the optimal R_1 at the typical process-corner. In addition, by considering the large R_1 variation across process corners and the area cost of a large trimming-network, this work implements the bit-dependent incremental resistance to trim R_1. Such

incremental resistance is to increase proportionally with the total resistance based on

$$\Delta R_{1,i} = \Delta R_{1,i-1}(R_{1,i}/R_{1,i-1}), \tag{3.18}$$

where $R_{1,i} = R_{1,i-1} + \Delta R_{1,i-1}$. $i \geq 1$ and it refers to the i^{th} bit of incremental resistance; and $\Delta R_{1,i} = R_{1\_LSB}$ when $i = 1$. Thus, the number of trimming bits, m, can be derived by solving (3.19)

$$R_{1,max} = R_{1,min} + \sum_{i=1}^{2^m} \Delta R_{1,i}, \tag{3.19}$$

where $R_{1,min}$ = 792 kΩ and $R_{1,max}$ = 4102 kΩ in this work. Subsequently, m = 6 is chosen. Hence, ($2^m = 2^6$ =) 64 segments of incremental resistances are connected in series to trim R_1 as shown in Fig. 4. V_{D1} refers to the drain of M_1, whereas V_{D3} refers to the drain of M_3. To illustrate, assume that ($R_{1,min} + \Delta R_{1,1}$) is the desired R_1. In Figure 3.4, $M_{TA1,2}$ and $M_{TB1,2}$ will be switched on by setting $V_{Trim1,2} = 0$. In this manner, I_{D1} flows from V_{D3} through $M_{TA1,2}$, $\Delta R_{1,1}$, and $R_{1,min}$ to V_{D1}. Moreover, through $M_{TB1,2}$, V_{D3} is passed to V_+, which is V_{IN+} of EA1. For matching purposes, additional PMOS transistors are inserted between V_- and V_{IN-} of EA1 to match $M_{TB1,i}$ as well as between V_{D4} and V_- to match $M_{TA1,i}$. They are not shown in Figure 3.3 for simplification.

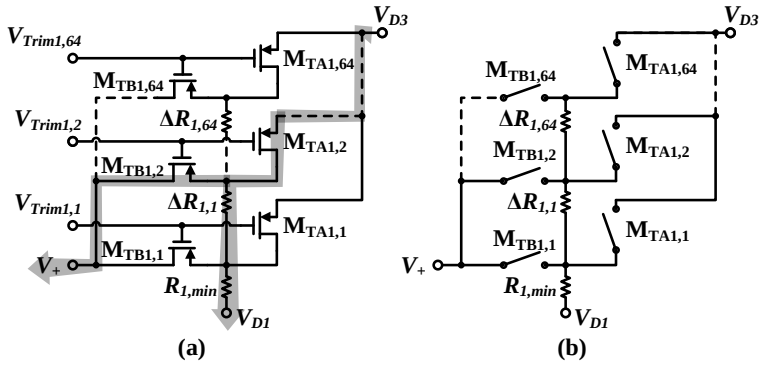

Figure 3.6 Resistance trimming networks for R_1 in (a) actual circuitries and (b) its conceptual diagram.

Trimming voltages $V_{Trim,1}$ to $V_{Trim,64}$ in Figure 3.6 are generated by the digital circuits in Figure 3.7. Altogether, Nine 3-to-8 'tree' decoders [71] are

implemented for this purpose. The decoder is enabled upon logic '0'. V_{R1_IN1} to V_{R1_IN6} are the input trimming bits, among which V_{R1_IN4} to V_{R1_IN6} function to select one of the eight cascading 3-to-8 decoders, whereas V_{R1_IN1} to V_{R1_IN3} turn on or off of the particular trimming voltage based on the decoder selected.

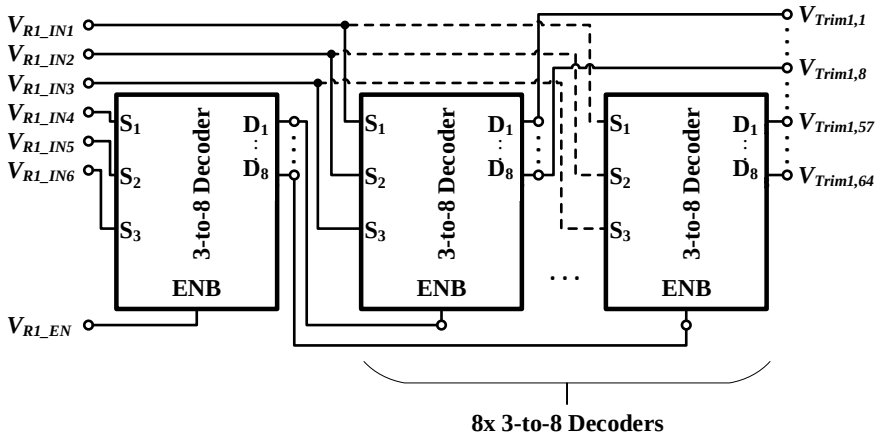

Figure 3.7 Digital circuits to derive $V_{Trim1,1}$ to $V_{Trim1,64}$.

3.2.3 Proposed Trimming Network for R_0

The main purpose to trim R_0 is to match R_1 as well as (V_{GS2} – V_{GS1}) in (3.13) to maintain V_{REF} at its nominal value, which is set to be 0.2 V in this work. To minimize effectively the undesired TC introduced by the resistance of MOS switches, the trimming network for R_0 is divided into upper and lower portions as shown in Figure 3.8. Moreover, the incremental resistance, $\Delta R_{0,Hj}$, of the upper portion is deliberately made large, whereas the incremental resistance, $\Delta R_{0,Lk}$, is made small.

To illustrate, take $R_0 = \Delta R_{0,H1} + R_{0,min} + \Delta R_{0,L16}$ as the desired R_0 for example. Only $M_{TB0,H2}$ and $M_{TA0,H2}$ needs to be on with $V_{Trim0,H2}$ = 0 V. The rest of trimming voltages in the upper portion are set as logic '1' to turn off their corresponding P-MOS switches. However, the resulted TC of V_{REF} could be corrupted if $\Delta R_{0,Hj}$ is not large enough. This is especially the case under sub-1-V operations. Since MOSFET as a switch operates in the triode region when turned on, the on-resistance, $R_{on\text{-}SW,H2}$, of $M_{TB0,H2}$ can be expressed as

$$R_{on-SW,H2} = \frac{1}{\mu_p C_{ox}(W_{H2}/L_{H2})(V_{D5}-|V_{thp}|-V_{SD,H2})}. \quad \textbf{(3.20)}$$

As V_{D5} is relatively low under sub-1-V operations, a low $V_{SG,TB0,H2}$ is resulted in, leading to a large $R_{on\text{-}SW,H2}$ comparable with the total off-resistance, $R_{off\text{-}SW}$, of all higher branches that consist of $M_{TB0,H3}$ till $M_{TB0,H7}$ in Figure 3.8a. Subsequently, significant amount of I_{D5} could flow through $R_{off\text{-}SW}$. As a result, (3.13) becomes

$$V''_{REF} = \left[\frac{(R_{0,min}+\Delta R'_{0,H1}+\Delta R_{0,L16})}{R_1}\right]\left(\frac{I_{D3}}{I_{D5}}\right)V_{R1}, \quad \textbf{(3.21)}$$

where $\Delta R'_{0,H1} = \Delta R_{0,H1} + R_{on\text{-}SW,H2}||R_{off\text{-}SW}$. Since R_0 is implemented with unsalicided n^+-poly resistor, which displays different TC from the MOS switches, $d(\Delta R'_{0,H1})/dT \neq d(\Delta R_{0,H1})/dT$. To minimize the effect of on-resistance, it is necessary to have $\Delta R_{0,H1} \gg R_{on\text{-}SW,H2}||R_{off\text{-}SW}$ such that $\Delta R'_{0,H1} \approx \Delta R_{0,H1}$. Subsequently, $\Delta R_{0,Lk}$ of the lower portion in Figure 3.8c has to be small to increase the trimming resolution for R_0.

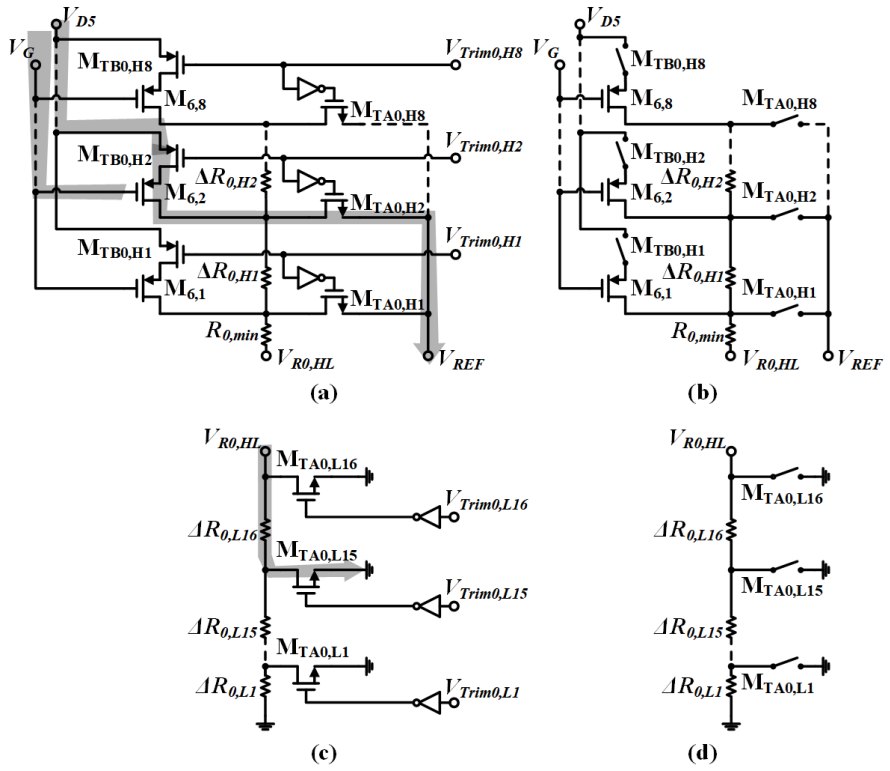

Figure 3.8 Resistance trimming networks for R_0 that consists of (a) the upper portion with (b) its conceptual diagram and (c) the lower portion with (d) its conceptual diagram.

Conversely, note that implementing the lower portion in Figure 3.8c alone

to trim R_0 is not feasible either. This is due to the situation when the desired R_0 becomes large enough and comparable with the off-resistance of the trimming MOS switches, such as $M_{TA0,Lk}$. Significant amount of current will flow through the off-resistances to sabotage the overall TC again following the same principle in (3.21).

By adopting $R_{0\_LSB} = R_{1\_LSB}$, a trimming resolution of $R_{0\_LSB}/R_{0,typical}$ = 2% can be obtained. $R_{0,typical}$ refers to the optimal R_0 at typical process corners for all components in TABLE 3.1. Thus, the trimming bits, n, for R_0 trimming-networks can be obtained as

$$n = \ln\left(R_{0,max}/R_{0\_LSB}\right)/\ln(2) \approx 7, \quad \textbf{(3.22)}$$

where $R_{0,max}$ = 2793 kΩ shown in TABLE 3.1. In Figure 3.8, $\Delta R_{0,Lk} = R_{0\_LSB}$, where k = 1 to 16. $\Delta R_{0,Hj} = 15 \times R_{0\_LSB}$, where j = 1 to 7. Trimming voltages $V_{Trim0,H1}$ to $V_{Trim0,H8}$ and $V_{Trim0,L1}$ to $V_{Trim0,L16}$ are generated by the digital circuits in Figure 3.9. The digital circuits are made up of three 3-to-8 decoders. The seven trimming-bits are $V_{R0H,IN1}$ to $V_{R0H,IN3}$, $V_{R0L,IN1}$ to $V_{R0L,IN3}$ and $V_{R0L,EN2}$. All decoders are enabled upon logic '0'.

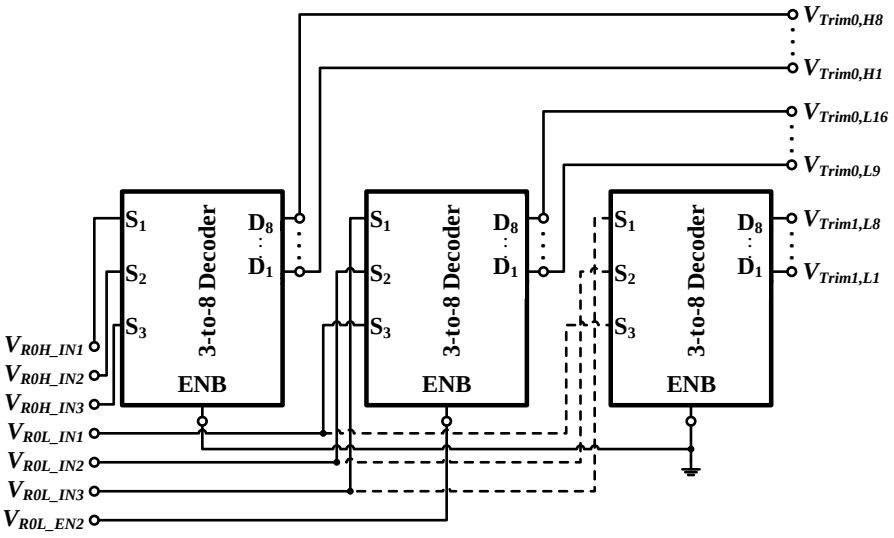

Figure 3.9 Digital circuits to derive $V_{Trim0,H1}$ to $V_{Trim0,H8}$ and $V_{Trim0,L1}$ to $V_{Trim0,L16}$.

3.2.4 Trimming Procedure

Making use of the proposed trimming networks, the CMOS VR is trimmed in the following manner. To start with, the R_1 trimming network is configured by assuming the typical process corners. Accordingly, R_0 trimming network is configured to derive a 200-mV V_{REF}.

In this manner, V_{REF} is recorded at -40 ℃, 25 ℃ and 80 ℃ to derive an estimated trend of V_{REF} over temperatures. Similarly, another two trends of V_{REF} will be recorded at R_1 values that is smaller and larger than its typical one. Thus, by comparing the slope of the three trends, the trimming direction can be determined, such as trimming R_1 up or down, to minimize the TC from -40 ℃ to 80 ℃. Once R_1 is determined, R_0 can be trimmed proportionally to ensure that V_{REF} = 200 mV.

3.2.5 Proposed Curvature-compensation Circuits

The proposed curvature-compensation serves two objectives. Primarily, it is to improve TC of the VR. Specifically, by considering the second-order effect of channel-length modulation, the drain current of a PMOS in the saturation region can be expressed according to [75] as

$$I_D = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)V_{eff}^2\left[1+\lambda_p(V_{DS}-V_{eff})\right], \tag{3.23}$$

where $V_{eff} = V_{SG} - |V_{thp}|$. Substitute (3.23) into (3.13) to obtain

$$V_{REF} = \left(\frac{R_0}{R_1}\right)\left(\frac{W_3L_5\left[1+\lambda_p(V_{SD3}-V_{eff,C})\right]}{W_5L_3\left[1+\lambda_p(V_{SD5}-V_{eff,C})\right]}\right)V_{R1}, \tag{3.24}$$

where $V_{eff,C} = V_{DD} - V_C - |V_{thp}|$. By having $\gamma = \frac{1+\lambda_p(V_{SD3}-V_{eff,C})}{1+\lambda_p(V_{SD5}-V_{eff,C})}$, it is apparent that $d\gamma/dT \neq 0$ as $\gamma \neq 0$ since $V_{SD3} \neq V_{SD5}$ and $d\lambda_p/dT \neq 0$, where λ_p is the output impedance constant [75]. It can be shown that

$$\frac{dV_{REF}}{dT} = \left(\frac{R_0}{R_1}\right)\left(\frac{W_3L_5}{W_5L_3}\right)\left[\frac{d\gamma}{dT}V_{R1} + \gamma\frac{d(V_{R1})}{dT}\right] \neq 0, \tag{3.25}$$

where $R_{on,5}$ is the on-resistance of M_5 in the saturation region. As R_0 is temperature-dependent, this indicates that $dV_{REF}/dT \neq 0$ with reference to (3.24)

due to the 2nd-order TC introduced by the temperature-dependent V_{SD5} even if dV_{R1}/dT can be nullified. To restore (3.23) to (3.13), a curvature compensation network that consists of EA2 and M_6 is proposed as shown in Figure 3.3b. With V_- sensed by V_{IN+} of EA2, the negative feedback from V_{IN-} of EA2 to V_{S6} ensures that $V_{D5} = V_-$ always. Subsequently, it guarantees that $V_{SD5} = V_{SD4} = V_{SD3}$ and $I_{D5}/I_{D3} = W_5L_3/(W_3L_5)$. Significant improvements on TC is illustrated by the simulation results shown in Figure 3.10 by the proposed curvature compensation techniques. The simulation setup is under V_{DD} = 0.7 V at typical process corners. TC improves by 68% from 19.3 ppm/°C (without curvature compensation) to 6.2 ppm/°C (with curvature compensation).

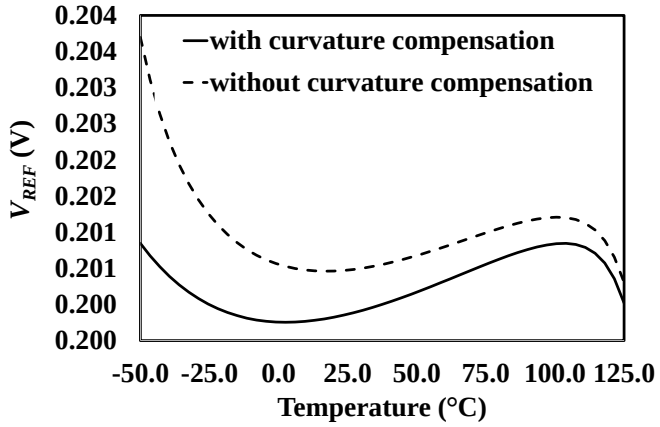

Figure 3.10 Effect of proposed curvature-compensation circuits on TC.

In addition, the curvature-compensation circuits also helps to improve the PSR of the proposed CMOS VR as verified by simulation results in Figure 3.11. The simulation setup is under V_{DD} = 0.7 V at typical process corners. No output capacitor is loaded at node V_{REF} to reveal the true PSR characteristics of the VR alone. PSR_{LF} improves by 28.5% from -48.9 dB (without curvature-compensation) to -62.8 dB (with curvature-compensation).

Improvements in PSR by curvature-compensation circuits are twofold. Firstly, the supply noise is weakened due to the additional impedance contributed by M_6 along the VR output branch. In detail, the low-frequency PSR, PSR_{LF}, is improved based on the impedance-division principle [76] as in

$$PSR_{LF} = 20\log\left(\frac{v_{ref}}{v_{dd}}\right) = 20\log\left[\frac{R_0}{R_0+|Z_5(s)|+|Z_6(s)|}\right] < 20\log\left[\frac{R_0}{R_0+|Z_5(s)|}\right], \quad \textbf{(3.26)}$$

where $Z_5(s)$ and $Z_6(s)$ are the impedance of M_5 and M_6 accordingly. Secondly, the compensation capacitor C_{C2}, which is inserted to constitute a dominant-pole compensation to ensure frequency stability, also improves the high-frequency PSR, PSR_{HF}. This is due to the fact that, at high frequency, $v_{s6} \approx v_{g6}$ since $\lim_{\omega\to\infty} Z_{CC2} = \lim_{\omega\to\infty} \frac{1}{j\omega C_{C2}} = 0$. This leads to $i_{d5} \approx 0$. Thus,

$$PSR_{HF} = 20\log\left(\frac{v_{ref}}{v_{dd}}\right) = 20\log\left(\frac{R_0 i_{d5}}{v_{dd}}\right) \approx -\infty. \quad \textbf{(3.27)}$$

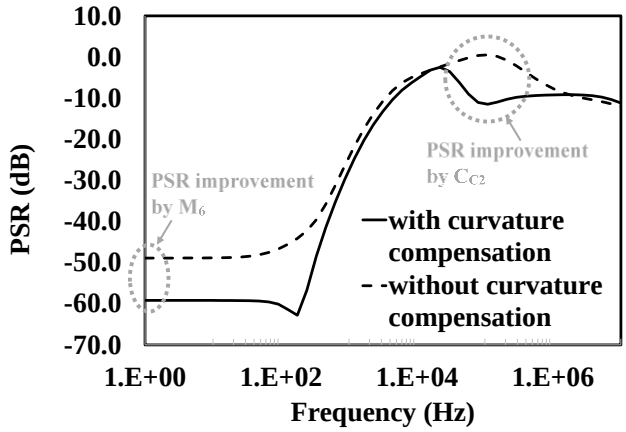

Figure 3.11 Effect of proposed curvature-compensation circuits on PSR.

3.2.6 Error Amplifier

The EA implemented in this work shown in Figure 3.3a adopts the amplifier structure introduced in [46] by replacing the grounded BJT input-pair with a grounded NMOS input-pair [77]. In this manner, no additional bias control is needed for the input currents of the EA since they are the exact replica of I_{D2} thanks to the current-mirror formed between M_2 and M_{A2} within the EA. Note that both M_{A1} and M_{A2} are 5-V NMOS' to match M_2. In addition, the inherent symmetrical structure ensures low input offset. Besides, the absences of a tail current-sink also facilitates sub-1-V operations. C_{C1} constitutes a miller compensation to ensure frequency stability of the proposed VR.

3.2.7 Start-up Circuits

To ensure that the proposed CMOS VR is functioning with designated amount

of current flowing through its core circuits to derive the targeted V_{REF}, a start-up circuit shown in Figure 3.12 is necessitated.

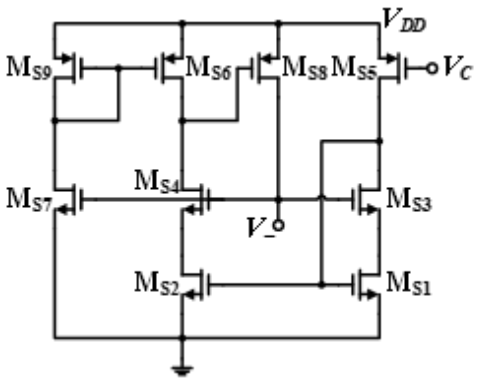

Figure 3.12 Start-up circuits for the proposed CMOS VR.

Upon power-up, no current flows through M_{S3} and M_{S1}. All transistors in the start-up circuits are off. However, the gate voltage of M_{S8} is designed in such a manner that, upon power-up, $V_{SG,S8}$ biases M_{S8} in the subthreshold region with a small amount of current leaking through M_{S8} from V_{DD}. Subsequently, the gate capacitances at V_- is slowly charged up. Thus, V_- is slowly raised. This leads to an increase in the drain current through M_2. Through the positive feedback from V_{IN-} of EA1 through M_4, V_- continues to increase and causing V_C to decrease accordingly through EA1. Subsequently, V_+ starts to get charged up through M_3 due to the lowering V_C. The complete VR will reach its stable state as long as the gain of the negative loop from V_{IN+} through M_3 to V_+ is larger than the gain of the positive loop from V_{IN-} through M_4 to V_-. As current in M_{S3} and M_{S1} increases, so does current through M_{S7} as well as M_{S6}, causing the on-resistance of M_{S6} to reduce and pushing the gate voltage of M_{S8} close to V_{DD} to turn off M_{S8}.

3.3 Results and Discussions

A micrograph of the proposed VR is shown below in Figure 3.13. The whole L-shaped chip, which involves both the main circuitries and the trimming networks occupies an area of 1.4 mm^2.

Figure 3.14 lists the TC of the proposed VR after trimming at the typical process corners. In comparison with previous works, such as the VR in [52], the

proposed VR exhibits relatively low TC 39.6 ppm/℃, 41.7 ppm/℃ and 39.7 ppm/℃ are obtained under V_{DD} at 0.7 V, 1.1 V and 1.5 V respectively. The resulted average V_{REF} across the temperature is 199.8 mV, 199.6 mV and 199.5 mV under V_{DD} at 0.7 V, 1.1 V and 1.5 V respectively.

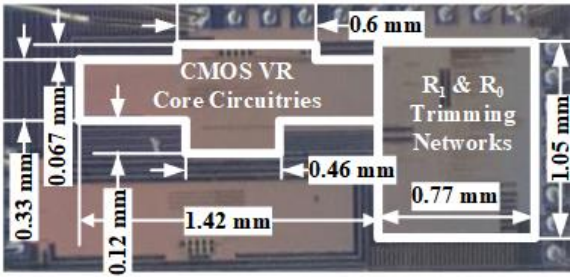

Figure 3.13 Micrograph of the proposed VR.

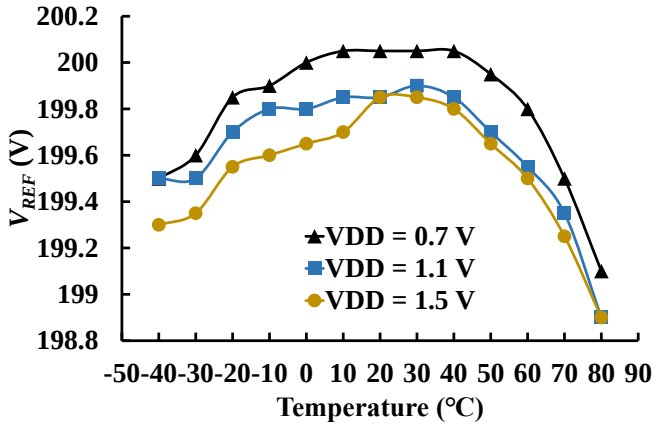

Figure 3.14 Measurement results of a typical V_{REF} versus temperature from one sample under V_{DD} at 0.7 V, 1.1 V and 1.5 V.

Moreover, TC repeatability is investigated in Figure 3.15, where V_{REF} of 10 samples under V_{DD} at 0.7 V, 1.1 V and 1.5 V are measured from –40 ℃ to +80 ℃. Altogether, 30 (= 3×10) sets of measurement data based on the 10 samples 3 supply inputs are collected. In Figure 3.15, all solid lines represent data collected under V_{DD} = 0.7 V; all dashed lines represent data collected under V_{DD} = 1.1 V; all dotted lines represent data collected under V_{DD} =1.5 V.

Statistical distributions of the 30 sets of data are analyzed in Figure 3.16. In Figure 3.16a, Gaussian distribution are plotted for the measured V_{REF} of the 10 samples under the 3 supply inputs accordingly. In general, the spread of V_{REF} is the narrowest under V_{DD} = 0.7 V with the smallest standard deviation (σ)

among the 3 sets of data under 3 supply inputs. The mean value (μ) of V_{REF} over temperature increases slightly by 0.2 mV as V_{DD} increases from 0.7 V to 1.5 V. Hence, the average LS for V_{REF} is computed to be 0.13%/V with the minimum at 0.06%/V and the maximum at 0.37%/V.

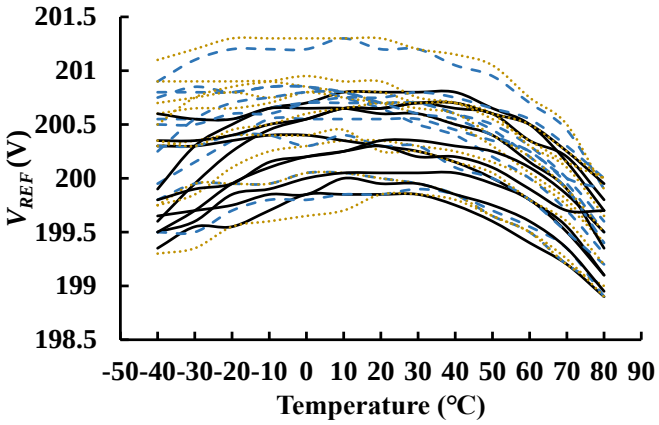

Figure 3.15 Measurement results of V_{REF} versus temperature from 10 samples after trimming.

Moreover, distributions of TC are summarized in Figure 3.16b. Based on the Gaussian distribution drawn under each V_{DD}, TC is more concentrated under V_{DD} = 0.7 V with the smallest σ among all data under the 3 supply inputs. The averaged TC varies slightly from 42.5 ppm/℃ under V_{DD} = 0.7 V to 48.5 ppm/℃ under V_{DD} = 1.1 V and 45.5 ppm/℃ under V_{DD} = 1.5 V. In comparison with the CMOS VR in a similar ΔV_{th}-based BVR-like topology in [52], the proposed trimming and curvature compensation techniques improve the TC by 2.54 times.

Furthermore, to reflect better the supply-sensitivity of TC, this work proposes TC's LS, $LS|_{TC}$, by taking the ratio between the largest TC-variation versus the range of the corresponding supply inputs as shown below:

$$LS|_{TC} = \frac{TC_{max} - TC_{min}}{V_{DD,max} - V_{DD,min}} \quad \textbf{(3.28)}$$

Different from the formula to compute the conventional LS for V_{REF} when the nominal value of V_{REF} is included in the denominator, the nominal value of TC is not involved in the denominator of Equation (3.28). Otherwise, a small TC with a relatively large (TC_{max} – TC_{min}) can result in a worse value than a large TC with the same variation. This will be nonsensical since TC variation around a

small nominal TC is more desirable than the same amount of variation around a large one. Hence, $LS|_{TC}$ will be in 'ppm/°C/V' rather than '%/V', which is the case for V_{REF}'s LS.

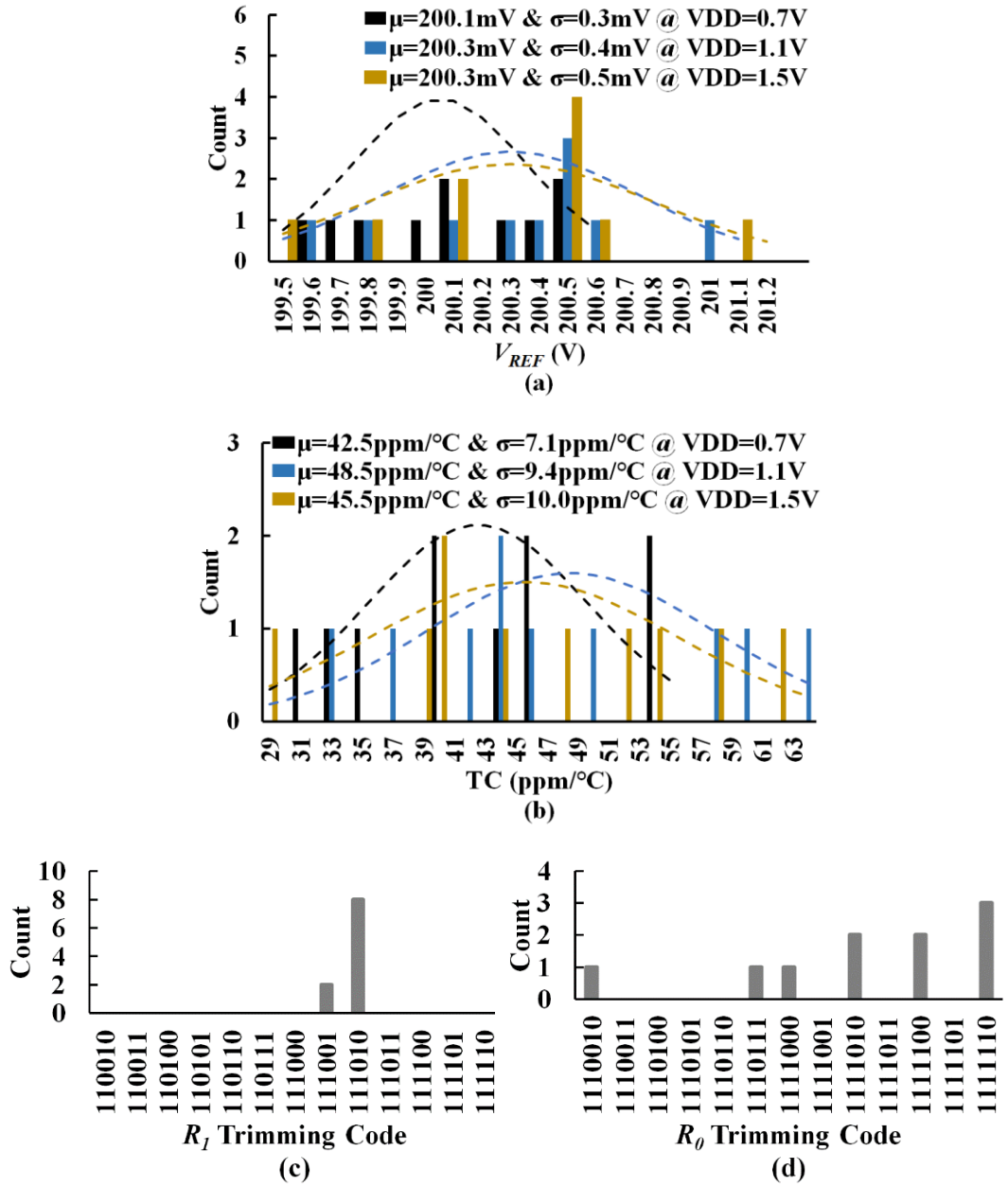

Figure 3.16 Distribution of (a) average V_{REF} at various V_{DD} after trimming, (b) TC, (c) trimming codes for R_1, and (d) trimming codes for R_0 from the 10 measured samples.

In this manner, $LS|_{TC}$ offers insight in characterizing the TC's supply-sensitivity for a given VR. It is a useful index as it is not rare that a VR can derive a good TC under a specified supply input but not so over its entire range of

supply inputs. In this work, the best $LS|_{TC}$ is measured as 2.65 ppm/°C/V among the 10 samples being measured; and its worst-case value is 15.4 ppm/°C/V. In addition, trimming code for R_1 and R_0 trimming network are summarized in Figure 3.16c and Figure 3.16d respectively.

Effectiveness of the proposed trimming networks is illustrated in Figure 3.17, where histograms in grey color represents TCs without trimming. Large variations in TC are notices over process deviations. They are most prominent at 'FF' and 'FS' corners, where TC deviates from its value at 'TYP' corner as much as 3000%! Such deviations are mostly attributed to the ineffectiveness of (3.1) by approximating $V_{DS} > 4V_T$ for the normal-V_{th} M_{N1} in Figure 3.1b in previous works.

The simulation results in Figure 3.17 have proved the effectiveness of proposed trimming networks. The results also implies the inadequacy of the curvature-compensation circuits alone in correcting TC over process variations despite its positive effect shown in Figure 3.10. TCs across all process corners are brought to be lower than 37 ppm/°C and close to their values at 'TYP' corners after trimming.

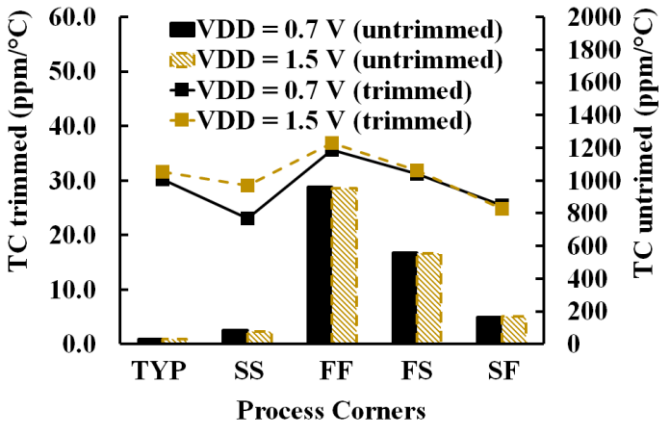

Figure 3.17 Simulation results of TC with and without trimming.

Moreover, the PSR reported in this work follows the definition of $PSR = 20\log(dv_{ref}/dv_{dd})$, which quantifies "the vulnerability of the circuit to noise injected through the input supply" [44]. PSR of the proposed CMOS VR under various supply inputs and with multiple values of output capacitor (C_L) is

measured and plotted in Figure 3.18a and Figure 3.18b respectively. As observed in Figure 3.18a, across all supply inputs, PSR deteriorates slightly from 100 Hz onwards with the worst PSR, being approximately -55 dB, occurring around 1 kHz. Such '1 kHz' corresponds to the -3-dB Band Width (BW) of the Low Pass Filter (LPF) formed by the 33-nF C_L and R_0. Beyond the '1 kHz', supply-induced noises are being filtered out by the LPF. Thus, PSR improves again. The significance of the -3-dB BW can be better illustrated by Figure 3.18b, where C_L increases from 0, 1 nF, 3.9 nF, 15 nF to 33 nF. As C_L increases, the mid-frequency PSR improves since the -3dB BW of the LPF shifts towards DC and the LPF filters out more low-frequency noises. R_0 is kept unchanged in this setup to ensure a 200 mV V_{REF}.

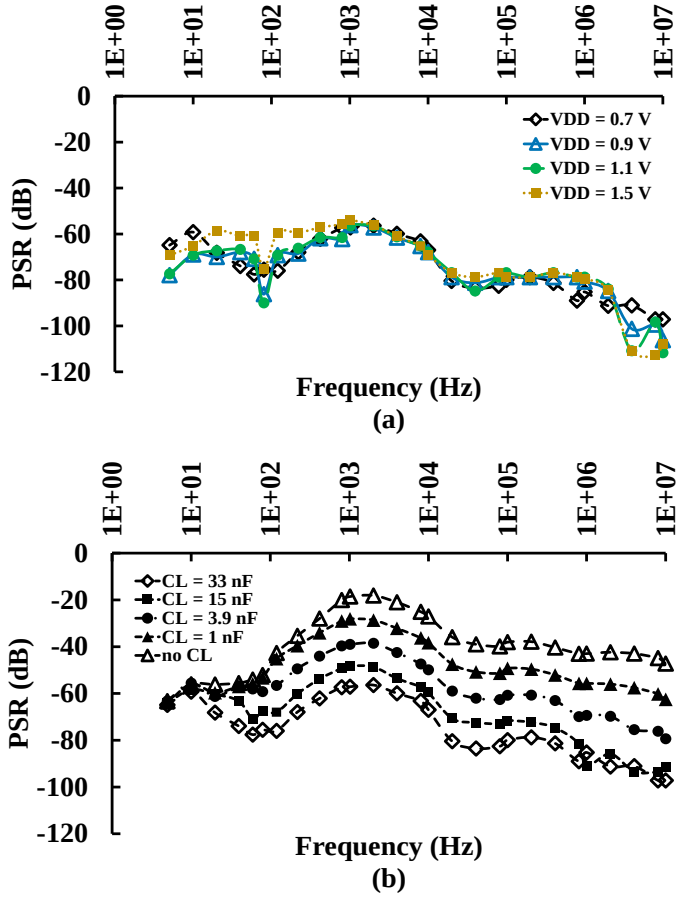

Figure 3.18 Measurement results of (a) PSR under various V_{DD} from 0.7 V to 1.5 V with 33-nF C_L and (b) PSR under V_{DD} = 0.7 V with various C_L from 0 to 33 nF.

The good supply-noise rejection at low frequencies can be attributed to the impedance-division principle [76] as the resulted V_{REF} (= 0.2 V) is relatively smaller in comparison with V_{DD} (> 0.7 V). To maintain a high PSR beyond 1

kHz, an output capacitor of 33 nF can be added at V_{REF}. In addition, the proposed curvature-compensation circuits also helps in improving the high-frequency PSR by forcing $v_{sg6} \approx 0$ which results in (3.27).

Furthermore, start-up performance is verified as well and shown in Figure 3.19. It takes longer time for the proposed VR to start up at low V_{DD}, such as V_{DD} = 0.7 V, due to the relatively low quiescent current available to charge up the parasitic capacitances of the internal nodes.

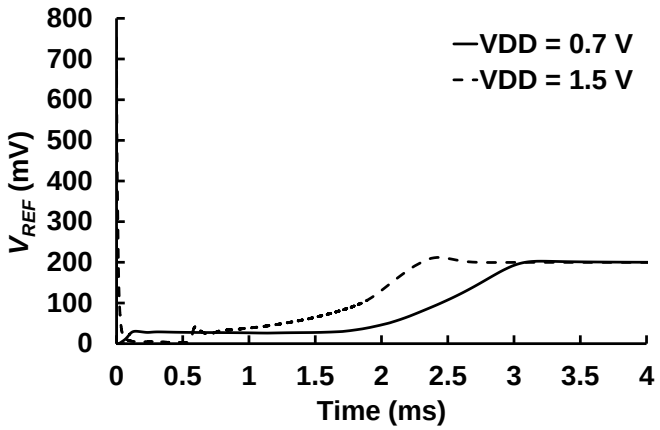

Figure 3.19 Simulation results of start-up performance.

Also investigated is the minimum supply-input, $V_{DD,min}$, of the VR. As it is shown in Figure 3.20a, the CMOS VR derives meaningful output with V_{REF} = 198.1 mV under V_{DD} from 0.63 V till 1.7 V by taking 200 mV as the targeted output and 1% as the targeted tolerance. Presented in Figure 3.20a is the quiescent current (I_Q) consumption measured across supply inputs. Noticeably, I_Q = 400 nA at V_{DD} = 0.7 V but increases with V_{DD} and reaches 3.25 μA at V_{DD} = 1.5 V. This is due to the increased current consumption of the digital logics that build the trimming networks under a higher V_{DD}. Temperature dependence of I_Q is listed in Figure 3.20b. As observed, I_Q is stable under sub-1-V V_{DD} and exhibits a slight decrease along the rising temperature under large supply inputs, such as 1.5 V.

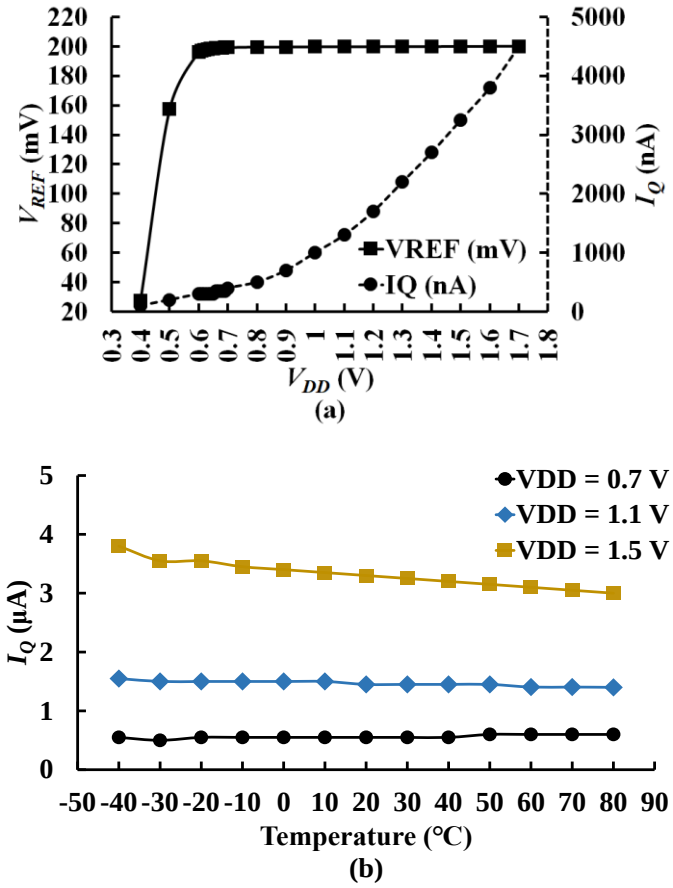

Figure 3.20 Measurement results of (a) V_{REF} and I_Q versus V_{DD} with the proposed trimming techniques at room temperature and (b) I_Q across temperature under V_{DD} of 0.7 V, 1.1 V and 1.5 V.

3.4 Concluding Remarks

Performances of the BVR-like CMOS VR with the proposed techniques are summarized and compared against prior works in in TABLE 3.2. In comparison with the ΔV_{th}-based CMOS VR in [52], the proposed trimming and curvature-compensation networks improve TC by 1.4 and 4.6 times in terms of the minimum and maximum TC respectively. In average, the proposed circuitries improve the TC by 2.54 times from 108 ppm/℃ as reported in [52] to 42.5 ppm/℃ as measured in this work. Thus, the proposed trimming and curvature compensation effectively offset process variations in such type of CMOS VR to derive a minimized TC.

Moreover, in terms of supply independence, V_{REF}'s LS and TC's LS of the proposed CMOS VR exhibits the second best performance among all listed works. This can be attributed to the 4-Transistor EA, shown in Figure 3.3a, which

inherently matches the VR core circuit as well as the curvature compensation to ensure accurate current mirroring between M_3 and M_5. This can be conducive when such VR is powered by a declining V_{DD} derived from a depleting battery output within a WSN sensor node.

TABLE 3.2 PERFORMANCE COMPARISON AGAINST PREVIOUS WORKS

	[48]	[51]	[52]	[78]	[79]	This Work
Year	2002	2012	2016	2016	2018	2019
Publication	JSSC	JSSC	JSSC	JSSC	TCASII	-
Technology (µm)	0.6	0.13	0.065	0.065	0.18	0.18
Type [a]	ΔV_{BE}	ΔV_{th}	ΔV_{th}	V_{GS}	ΔV_{GS}	ΔV_{th}
$V_{DD,min}$ (V)	0.98	0.5	0.62	0.8	0.6	0.7 [b]
I_Q (µA) @ $V_{DD,min}$	18	0.000059	0.0016	16.25	0.051	0.4
V_{REF} (mV)	603	175	390	428	218.3	200
Temperature range (°C)	0 ~ 100	-20 ~ 80	-25 ~ 110	-40 ~ 125	-40 ~ 125	-40 ~ 80
TC (ppm/°C) @ $V_{DD,min}$	15	13.5 ~ 47 [c]	44 ~ 248	3.2 ~ 9.8	8.4 ~ 34	31.2 ~ 54.1
TC's LS (ppm/°C/V)	19.2 [d]	1.21 [e]	-	-	-	2.65 [f]
Curvature Compensation	No	No	No	Yes	No	Yes
V_{REF}'s LS (%/V)	-	0.036	0.07	0.1	0.4	0.06 [g]
Trimming	No	Yes	No	Yes	Yes	Yes
PSR (dB) @ 100 Hz	-	-51	-62	-97	-	-60
PSR (dB) @ 10 MHz	-	-65	-	-65	-42.3	-97
Area (mm^2)	0.24	0.0093	0.077	0.0104	0.075	1.37

a. Type' refers to the key concept the VR relies on to derive a zero TC by cancelling PTAT and CTAT coefficients.
b. According to measurement results, the actual $V_{DD,min}$ is 0.63 V in this work. However, 0.7 V is taken to make the reported "TC @ $V_{DD,min}$" in this table tally with the rest of the works. In addition, 0.7 V is also the targeted $V_{DD,min}$ during design.
c. This is the TC of the digital trimmable 2T VR in [51].
d. This is measurement result from one sample according to [48].
e. This is the best-case measurement result according to [51].
f. This is the best-case measurement result. TC's LS range from 2.65 ppm/°C/V to 15.4 ppm/°C/V with an average at 9.02 ppm/°C/V.
g. This is the best-case measurement result. V_{REF}'s LS range from 0.06%/V to 37%/V with an average at 0.13%/V.

Despite inferior LS to that of the CMOS VR from [51], the proposed VR outperforms the VR in [51] in both PSR and the feasible temperature range. Indeed, PSR of the proposed work is much higher than that reported in [51] by 20 dB at low frequencies as listed in TABLE 3.2. This can be attributed to the effect of the on-resistance of M_6 and C_{c2} as explained earlier. The high PSR is advantageous when the supply input comes from a noisy rectifier-output as in

WPT-powered applications. Also surpassing the VR in [51], the proposed VR allows a wider temperature range. Indeed, it allows the widest feasible temperature range, from -40 ℃ to 80 ℃, among all prior works with an available $LS|_{TC}$ [48, 51]. The feasible temperature range of the proposed VR is 1.2 times wider than that of the VRs in [48] and [51].

With comparable TCs, a wider feasible temperature range implies a more robust V_{REF} against temperature variations and it is also more desirable. This is due to the fact that the local temperature gradient, dV_{REF}/dT, deteriorates more radically along the TC curve towards both cold and hot boundaries of the temperature range. Obviously, by narrowing down the temperature range, TC can be calculated smaller than it is done otherwise. However, a low TC under a narrow temperature range will become less meaningful as it will limit the practicality of the VR when the VR has to cope with large temperature variations. Therefore, as far as PVT-robustness is concerned, the proposed CMOS VR in this work still presents the best overall performance.

Admittedly, TCs reported in [78, 79] are low over a wide temperature range, their low TCs are valid only under specified supply inputs. Since no $LS|_{TC}$ is available to be deduced from these works, the practicability of these VRs is less convincing. In other words, the specific values of V_{DD} entailed to obtain the low TCs can be hard to guarantee due to inaccuracies and non-ideal setup in practice. Simply put, variations in V_{DD} may worsen their TCs considerably.

Nonetheless, the proposed VR is not without shortcomings. For an instance, the total area is relatively large. This is due to the overly designed trimming networks and the excessively placed dummies in empty areas to fulfil layout design rules. Even so, as far as product packaging is concerned, the VR faces no difficulties to fit into a Small Outline (SO) package, such as a 10.3×7.0×2.1 mm3 SO16 package. This is so even if it has to be packed together with a voltage regulator fed by its V_{REF}. Under such scenario, the R_0 trimming network can be replaced by a tunable resistive feedback loop of the regulator to save space as well.

Chapter 4 A Fast-settling OCL-LDO Based on Load-Adaptive Negative-Resistance

Despite the fact that an LDO dedicated to a WPT-powered WSN sensor node can be powered by a secondary battery, good LS is still necessary under the battery-output from 1.5 V down to sub-1 V. Moreover, fast-settling load-transient-response is to be assured upon sudden switching on or off the loading ICs orchestrated by the DPM scheme. Equally critical is the power efficiency since the power attainable under such scenario is limited. And the power efficiency will be translated into low Drop-Out Voltage (V_{DO}) in the range of 100 mV, and current efficiency above 99% in this work. Furthermore, an Output-Capacitor-Less (OCL) topology is favored as the absence of large and discrete compensation-capacitors at the LDO output-node saves the PMU package-size as well as the overall node-size of a WSN sensor.

Prior works in fast-settling sub-1-V OCL-LDOs [80-83] display a V_{DO} of 200 mV, which still leave room for improvement. An LDO reported in [84] features a V_{DO} as low as 50 mV but can source only 10-mA load current, maximum. This is inadequate when the LDO is loaded with both ADC [31, 32] and RF transceivers [28]. In contrast, this work develops an OCL LDO enhanced by load-adaptive negative-resistance at the input stage of its EA. In this manner, it targets at sourcing current up to 50 mA with high current-efficiency and fast-settling load-transient-response, even under sub-1-V V_{DD}.

In this manner, this chapter begins with an in-depth review on the inefficient power consumption of the original G_m-cell-based OCL-LDO to achieve fast-settling load-transient-response under sub-1-V input supplies. Benefits of PPF structure in raising the power efficiency are revealed subsequently. This is followed by listing obstacles faced when PPF is incorporated into the original G_m-cell OCL LDO. The chapter goes on by proposing the load-adaptive negative resistance to address those obstacles. The additional process tracking circuitries to correct process-deviation-induced errors in the proposed design is introduced afterwards. As a further improvement, a new bulk-biasing technique

is also covered in this chapter to accelerate the transient responses and PSR of the OCL LDO. The functionality of the proposed design is then examined and verified by small and large signal analyses. Simulation and measurement results are discussed afterwards with conclusions drawn at the end of the chapter.

4.1 Overview of Previous G_m-cell-based OCL-LDO

Despite a low quiescent-current of 1.2 μA, the load-transient performance of the original G_m-cell-based OCL-LDO under a sub-1-V V_{DD} is left unaddressed in [57]. To adapt its fast-settling feature into a battery-powered LDO implemented within a WSN sensor node, this work first delves into the sub-1-V performances of the original G_m-cell-based OCL-LDO in terms of its DC-gain and speed.

Shown in Figure 4.1a is the original OCL-LDO in [57] if removing transistors M_{N1} and M_{N2}. Transistors M_{PHa}, M_{PHb}, M_{PLa}, and M_{PLb} are identical. So are M_{NH} and M_{NL}. The current ratio of current-mirror M_{P6}-M_{P5} is 1:n; it is 1:1 for M_{N4}-M_{N6} and 1:n for M_{N3}-M_{N5} in [57]. The two G_m-cells are highlighted in dashed trapezoidal boundaries. Firstly, the total input-g_m, $g_{m,in}$, of the original OTA in [57] can be computed by (4.1) following [56]

$$g_{m,in} \cong \frac{2n g_{mp,HL} \cdot g_{mN,5\&6}}{g_{mN,3\&4} + g_{ds,HL} + g_{dsN,3\&4}}, \tag{4.1}$$

where $g_{m,HL}$ equals the transconductance shared by M_{PHa}, M_{PHb}, M_{PLa}, and M_{PLb}; $g_{ds,HL}$ is their output-conductance; $g_{mN,5\&6}$ refers to the transconductance shared by M_{N3} and M_{N4}; $g_{ds,HL}$ equals the output-conductance of M_{PHa}, M_{PHb}, M_{PLa}, and M_{PLb}; $g_{dsN,3\&4}$ refers to the output-conductance of M_{N3} and M_{N4}; all transistors concerned in (4.1) are operating in the saturation region.

Moreover, the settling time, Δt_S of an OCL-LDO is given by [39] as

$$\Delta t_S \approx \frac{0.37}{BW_{CL}} + \frac{C_{o1}\Delta i_L}{g_{m,PT} n I_{SR}} = \frac{0.37 C_{o1}}{g_{m,in} g_{m,PT} r_{out}} + \frac{C_{o1}\Delta i_L}{g_{m,PT} n I_{SR}}, \tag{4.2}$$

where $g_{m,PT}$ is the transconductance of M_{PT}; it is given as

$$g_{m,PT} = \mu_p C_{ox} (W_{PT}/L_{PT})\left(V_{DD} - V_{G,PT} - \left|V_{thp,PT}\right|\right), \tag{4.3}$$

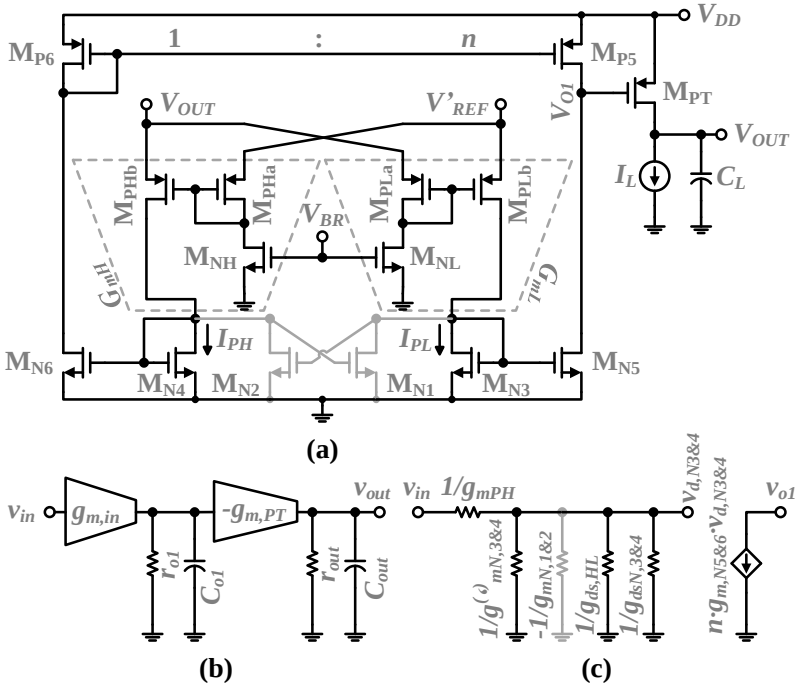

Figure 4.1 G_m-cell-based OCL-LDO in (a) its circuit diagram and (b) the small-signal diagram with (c) the small-signal diagram of the half-circuit of the OTA.

where $V_{G,PT}$ is the gate voltage of M_{PT}; $V_{thp,PT}$ is the threshold voltage of M_{PT}; W_{PT} is the channel-width of M_{PT}; L_{PT} is the channel-length of M_{PT}; $I_{SR} = nI_B\left[\Delta v_{out-}/\left(V_{SG,PLa} - |V_{thp,HL}|\right) - 1\right]^2$ is the discharging current [77] for Δt_S during an undershoot recovery upon a step-up load transient, whereas $I_{SR} = nI_B\left[\Delta v_{out+}/\left(V_{SG,PHa} - |V_{thp,HL}|\right) - 1\right]^2$ is the charging current [77] for Δt_S during an overshoot recovery upon a step-down load transient; Δv_{out-} and Δv_{out+} are the undershoot and overshoot magnitude of V_{OUT} during load transient responses $I_B = \mu_n C_{ox}\left(W_{N,HL}/L_{N,HL}\right)\left(V_{BR} - V_{thn,HL}\right)^2/2$ is the constant biasing-current through M_{NH} and M_{NL}; $V_{thp,HL}$ and $V_{thn,HL}$ are threshold voltages of $M_{PHa,b}$, $M_{PLa,b}$, M_{NH}, and M_{NL} accordingly; $W_{N,HL}$ is the channel-widths of M_{NH}, and M_{NL} accordingly; $L_{N,HL}$ is the channel-lengths of M_{NH}, and M_{NL} accordingly; V_{BR} is the bias voltage to generate the constant I_B; $BW_{CL} \approx A_{DC}p_d$ is the closed-loop bandwidth; $A_{DC} = g_{m,in}r_{o1}g_{m,PT}r_{out}$ is the open-loop DC-gain; $p_d = 1/(r_{o1}C_{o1})$ is the dominant-pole frequency; $r_{o1} = r_{ds,P5}//r_{ds,N5}$ and r_{out} are the output resistance of the OTA and the LDO accordingly; C_{o1} is the lumped parasitic capacitance at the gate of M_{PT}; Δi_L is the change of the I_L during transient response.

The cross-coupled differential-input G_m-cell presented in [57] ensures

fast settling of 4 μs upon a 50-μA-to-50-mA load transient with a low quiescent-current of 1.2 μA. However, the design requires a minimum of 1.2-V V_{DD}. Modifications on such structure is shown in [60]. By enhancing the dynamic biasing current obtained from the G_m-cell, it boosts the load-transient-response further. A 20-ns settling time upon a 9-mA-to-40-mA load transient is achieved. Nonetheless, the overall LDO is current-hungry and draws 158-μA quiescent current. Moreover, it is not under sub-1-V V_{DD}, either. In addition, its current-sourcing voltage reference circuit is unconventional but left unaddressed [60].

Now assume that V_{DD} falls under sub-1 volt and the output voltage, V_{OUT}, remains as 0.7 V. r_{out} will drop unavoidably if I_L is unchanged. Subsequently, I_{SR} has to increase to maintain Δt_S for fast settling based on (4.2). In turn, I_B has to increase if referred back through the current-mirrors. However, this leads to reduction in A_{DC} despite increase in $g_{m,in}$. It is so as the increase in $g_{m,in}$ is cancelled out by the corresponding decrease in r_{o1}. Thus, to restore A_{DC} for good line regulation and LS, $g_{m,PT}$ has to increase by raising W_{PT}/L_{PT}. However, a large W_{PT}/L_{PT} could result in M_{PT} pushed into triode region and reduce $g_{m,PT}$ unfavorably. Subsequently, Δt_S will drop further, implying an even-larger I_B needed to maintain Δt_S. Such iteration continues till an I_B that is considerably larger than its original value is allocated. As a result, the current efficiency of the original G_m-cell structure is reduced by the sub-1-V V_{DD}. Figure 4.2 shows the reverse effect of a lowering V_{DD} on A_{DC} and Δt_S of the original OCL-LDO. This calculation assumes that current consumption and I_L is kept constant across V_{DD} and V_{OUT} = 0.7 V. As it is illustrated, at V_{DD} = 0.8 V, A_{DC} drops as much as 95% of its value at V_{DD} = 1.2 V; besides, Δt_S also slows down to become 8.9 times of its value at V_{DD} = 1.2 V.

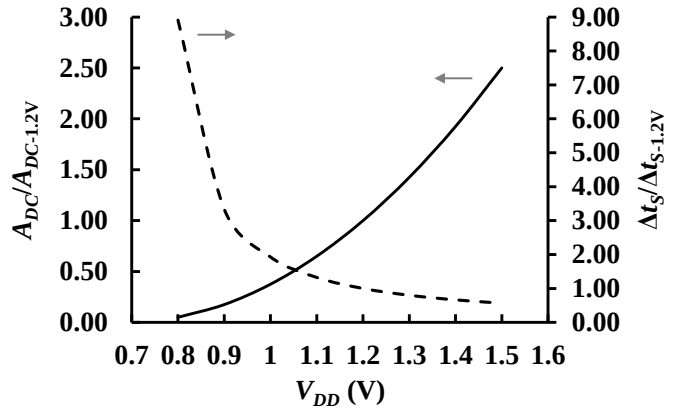

Figure 4.2 Plot of normalized A_{DC} and Δt_S of the original G_m-cell-based OCL-LDO from V_{DD} = 0.8 to 1.5 V with respect to A_{DC} and Δt_S at V_{DD} = 1.2 V.

4.2 Challenges in Incorporating PPF in OCL-LDOs

To boost $g_{m,in}$ without trading the load-transient-response, a cross-coupled pair, consisting of M_{N1} and M_{N2} is introduced by attaching them to M_{N3} and M_{N4} as shown in Figure 4.1a [54-56]. Such cross-coupled pair of M_{N1}-M_{N2} forms a PPF structure. As a result, the boosted input-g_m, $g'_{m,in}$, can be derived through small signal analysis as in Figure 4.1c and (4.4) [56]. Mathematically, it is as if a negative-resistance of value '$-1/g_{mN,1\&2}$' is connected in parallel with M_{N3} or M_{N4}.

$$g'_{m,in} \cong \frac{2ng_{mp,HL} \cdot g_{mN,5\&6}}{g'_{mN,3\&4} - g_{mN,1\&2} + g_{ds,HL} + g'_{dsN,3\&4} + g_{dsN,1\&2}} \tag{4.4}$$

By keeping current I_B constant and modifying the drain current through M_{N4} to be $I'_{N4} = (1-\alpha)I_{N4}$, $g'_{mN,3\&4} = (1-\alpha)g_{mN3,4}$, $g_{mN,1\&2} = \alpha g_{mN3,4}$ and $g'_{m,in}/g_{m,in} \approx 1/(1 - 2\alpha)$, where $0 < \alpha < 0.5$ is the current-allocation-factor. Note that $g_{ds,HL}$, $g'_{dsN,3\&4}$, and $g_{dsN,1\&2}$ are neglected as they are much smaller than $(1 - 2\alpha)g_{mN,3\&4}$. By adjusting the current ratio for current-mirror M_{N6}-M_{N4} to be 1 : $(1 - \alpha)$, the OTA output current, I_{o1}, which is through M_{P5} and M_{N5}, remains unchanged. In this manner, the PPF-incorporated OCL-LDO consumes identical quiescent current to the original. However, the modified DC-gain, A'_{DC} is boosted and related to the original DC-gain, A_{DC}, by

$$A'_{DC}/A_{DC} = g'_{m,in}/g_{m,in} = 1/(1-\alpha). \tag{4.5}$$

Thus, a larger α leads to a higher A'_{DC} as shown in Figure 4.3. The

calculation assumes that $V_{SG,PT}$ = 0.6 V at V_{DD} = 0.8 V and $|V_{thp,PT}|$ = 0.5 V. In addition, Δv_{out} is assumed unchanged and Δi_L is set as 100 mA. M_{PT} is assumed to be operating in the saturation region.

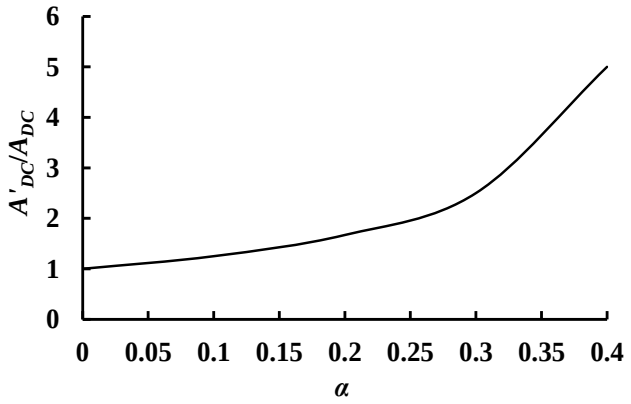

Figure 4.3 Plot of normalized A'_{DC} of the PPF-incorporated G_m-cell-based OCL-LDO with respect to A_{DC} of the original G_m-cell-based OCL-LDO.

In addition, the reduced settling time, $\Delta t'_S$, can be related to Δt_S as shown in Figure 4.4 using (4.2). Assumptions made for calculations to derive plots in Figure 4.4 follow those made in Figure 4.3. Moreover, the more current diverges into PPF from I_B, the faster the LDO responds. This becomes even more prominent under sub-1-V V_{DD}. Such are the characteristics in need by a battery-powered PMU within a WSN sensor node. Hence, in comparison with its original predecessor, the PPF-incorporated G_m-cell-based OCL-LDO is more current-efficient with better line-regulation due to the increased A'_{DC} and faster load-transient-response thanks to the reduced $\Delta t'_S$.

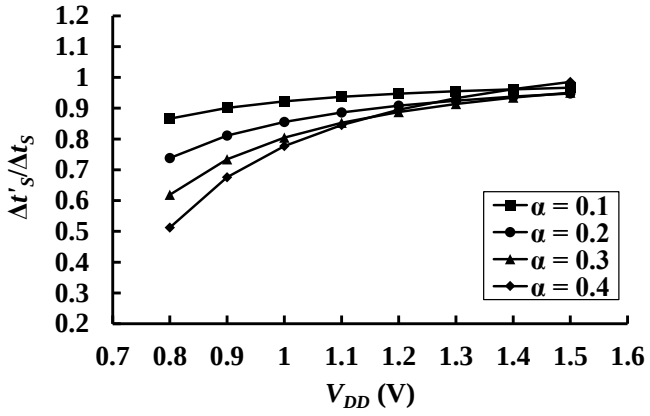

Figure 4.4 Plot of normalized $\Delta t'_S$ of the PPF-incorporated G_m-cell-based OCL-LDO with respect to Δt_S of the original G_m-cell-based OCL-LDO.

However, trade-off in developing a PPF-incorporated G_m-cell-based OCL-LDO does exist. Specifically, the improved DC-gain, A'_{DC}, and settling time, $\Delta t'_S$, threaten the frequency stability of the OCL-LDO across a wide load-range. This is due to the LHP pole associated with the negative load resistance [56]:

$$p_{N,1\&2} = -\frac{g'_{mN,3\&4} - g_{mN,1\&2} + g_{ds,HL} + g'_{dsN,3\&4} + g_{dsN,1\&2}}{C_{N,1\&2}}. \quad \textbf{(4.6)}$$

With the dominant-pole, p_d, derived at the gate of M_{PT}, the conventional first-non-dominant-pole of an OCL-LDO is the output pole, $p_o = 1/(r_{out}C_{out})$, where C_{out} is the lumped capacitance at the LDO output node. This may still hold at light load with PPF inserted into the LDO. However, at heavy load, the frequency of $p_{N,1\&2}$ can become lower than that of p_o, which shifts towards higher frequencies and leaves $p_{N,1\&2}$ as the new first-non-dominant-pole instead of p_o.

This is illustrated by simulation results in Figure 4.5. All dashed lines are plots under the light load when I_L = 0 mA; all solid lines are plots under the heavy load when I_L = 50 mA. The simulation setup is under V_{DD} = 0.8 V. The OCL-LDO is based on the proposed design except for the gate-biasing voltage of the active SDR being fixed at V_{SW} = 0.55 V to emulate a non-load-adaptive $g_{mN,1\&2}$. At heavy load, PM > 0 as labelled in Figure 4.5a. It indicates that the LDO is stable. This is due to the fact that $p_{o,50\text{-}mA}$ locates at relatively high-frequency or even beyond the cut-off frequency as shown in Figure 4.5b. Under such scenario, $p_{o,50\text{-}mA}$ exerts negligible influence on the frequency stability, leaving $p_{N,1\&2}$ as the first non-dominant-pole; and it is relatively easy to ensure stability as the LDO can be approximated as a one-pole system. However, as load decreases, the LDO become less stable. This is resulted from the emergence of the load-dependent $p_{o,0\text{-}mA}$ at low frequencies. In other words, $p_{o,0\text{-}mA}$ draws near to $p_{N,1\&2}$. The two closely-placed LHP poles can deteriorate the phase response drastically and pull down PM towards zero. Therefore, to leverage on the merits of PPF structure, the stability issue induced from the structure has to be resolved across the targeted load-range.

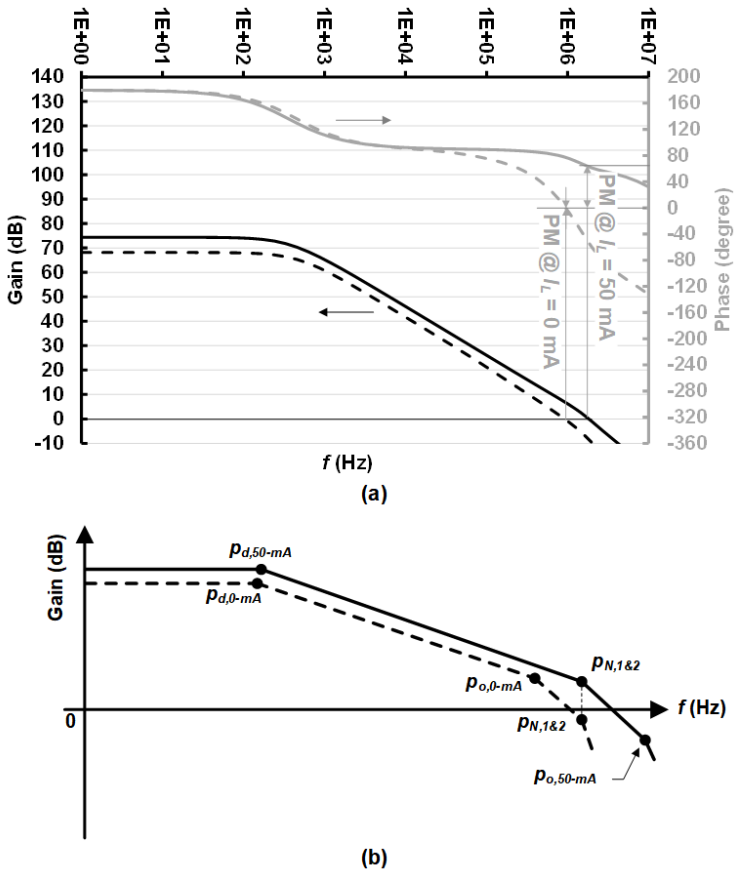

Figure 4.5 Frequency response of a PPF-incorporated OCL-LDO at heavy and light load in (a) simulation results and (b) bode-plot diagrams.

4.3 Proposed PPF-incorporated G_m-cell-based OCL-LDO

A conceptual diagram of the overall proposed OCL-LDO is displayed in Figure 4.6, whereas its detailed circuitries are shown in Figure 4.7. OTA1 is incorporated with PPF and cross-coupled G_m-cell at its input stage to boost its A_{DC} and Δt_S. The key element of OTA1 involves the proposed active load-adaptive negative-resistance and the control voltage. The control voltage, V_{SW}, is generated by the Load-Adaptive Controller (LAC). In addition, a Process-Tracking Current-Sink (PTCS) is also implemented within the LAC to ensure process-robustness. Besides, OTA2, M_{PR}, R_1, and R_2 forms an auxiliary low-power LDO as an adapter between a conventional VR and the current-sinking reference-input of OTA1. In this manner, it addresses the need for a current-sourcing VR from the G_m-cell-based input-stage.

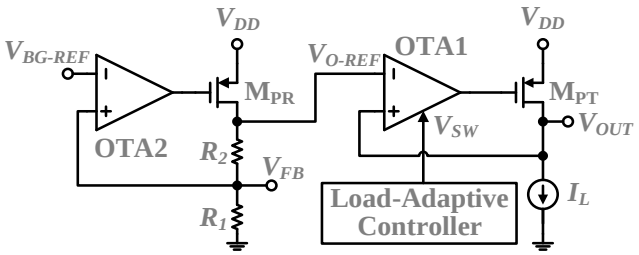

Figure 4.6 Conceptual diagram of the proposed OCL-LDO.

4.3.1 Proposed Load-adaptive Negative Resistance

The load-adaptive negative-resistance is achieved by attaching two active SDR at the source terminals of M_{N1} and M_{N2} respectively. Shown in Figure 4.7, the two SDRs are realized by two identical NMOS, M_{N1_D} and M_{N2_D}. By biasing M_{N1_D} and M_{N2_D} in the triode region, their effective resistance, R_{N_D}, can be estimated as $R_{N\_D} = 1/(\mu_n C_{ox}(W_{N\_D}/L_{N\_D})(V_{SW} - V_{th,N\_D}))$ by assuming deep-triode operation [45]. μ_n is the electron mobility; C_{ox} is the gate-oxide capacitance per unit area; W_{N_D} and L_{N_D} are the channel-width and channel-length of M_{N1_D} and M_{N2_D} accordingly; V_{SW} is the control voltage generated by the proposed LAC; V_{th,N_D} is the threshold voltage of M_{N1_D} and M_{N2_D}. In this manner, by viewing M_{N1} and M_{N1_D} together as an equivalent NMOS itself as well as for M_{N2} and M_{N2_D}, the effective transconductance of the degenerated M_{N1} and M_{N2} can be expressed as $g'_{mN,1\&2} = g_{mN,1\&2}/(1 + g_{mN,1\&2}R_{N\_D})$ [45]. Thus, the resulted negative resistance can be expressed as

$$r_{N,1\&2} = -\frac{1}{g'_{mN,1\&2}} = -\left[\frac{1}{g_{mN,1\&2}} + \frac{1}{\mu_n C_{ox}(W_{N\_D}/L_{N\_D})(V_{SW}-V_{thN\_D})}\right]. \quad \textbf{(4.7)}$$

Despite that $g'_{m,in}$ drops due to SDR as $g_{mN,1\&2}$ in (4.3) has to be replaced with $g'_{mN,1\&2}$ derived from (4.6), the negative-resistance $r_{N,1\&2}$ becomes adjustable by V_{SW}. In turn, V_{SW} is derived by the LAC to achieve load-adaptability. To derive V_{SW}, I_L is first sensed by the current sensing circuit shown in Figure 4.7. The current sensing circuit is made of M_{PS1}, M_{PS2}, M_{NS1} and M_{NS2}; it is constructed in a current-conveyor configuration. All MOSEFTs in the current sensing circuit operate in the subthreshold region. By ensuring $V_{DS} > 4V_T$ for M_{PS1}, M_{PS2}, M_{NS1} and M_{NS2}, the current-mirroring can still be guaranteed despite subthreshold operations as the drain current, I_D, under such scenario is governed by (4.8) according to [52, 71]

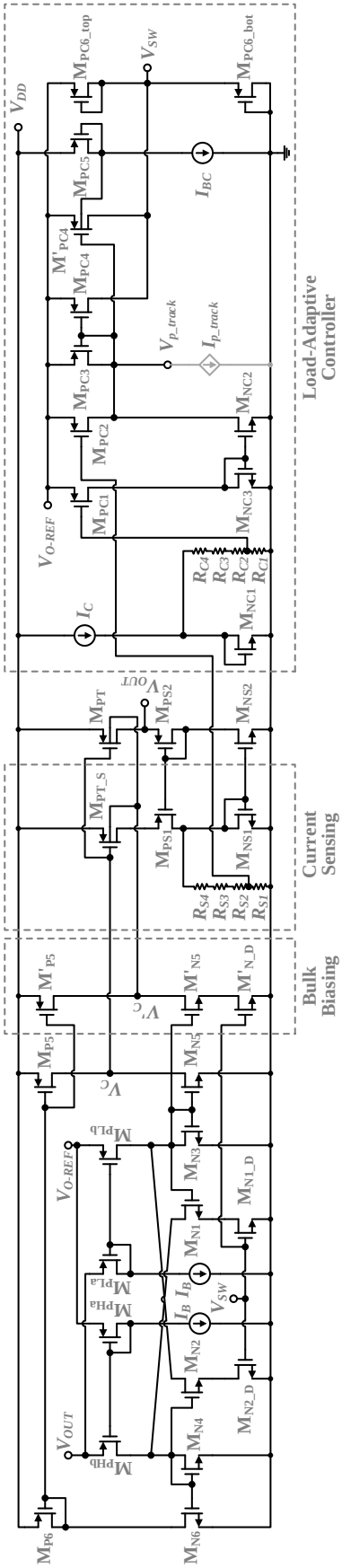

Figure 4.7 Circuit diagram of the proposed OCL-LDO.

$$I_D = I_{D0}(W/L)\exp[(|V_{GS}| - |V_{th}|)/(m_s V_T)], \quad \textbf{(4.8)}$$

where $V_T = kT/q$ is the thermal voltage; k is the Boltzmann constant; T is the absolute temperature; q is the electronic charge; $I_{D0} = \mu C_{ox}(m_s - 1)V_T^2$; μ is the charge carrier mobility, m_s is the subthreshold slope parameter; W and L are the channel width and length of the given MOSFET respectively. The sensed I_L is then converted into voltage $V_{G,PT2}$ at the gate of M_{PC2} by the resistive network of series-connected R_{S1}-R_{S4}. R_{S1}-R_{S4} are implemented with four identical MOSFETs in diode connections with high resistance, which ensures minimum current being diverted into the resistive branch with negligible effect on the current-mirror M_{NS1}-M_{NS2}.

The load-dependent $V_{G,PC2}$ is then compared with a constant reference biasing voltage, $V_{G,PC1}$ at the gate of M_{PC1}. $V_{G,PC1}$ is obtained from M_{NC1} and the resistive network of series-connected R_{C1}-R_{C4}, similar to that formed by R_{S1}-R_{S4}. The constant current-source I_C duplicates the current drawn from V_{OUT} when I_L = 0. M_{NC1} and M_{NS1} are identical; and by having $(W_{PT}/L_{PT}) : (W_{PT\_S}/L_{PT\_S}) = \alpha_I$, $I_C = (I_{D,PHb} + I_{D,PLa})/\alpha_I$ is a known value, which is also the output current from M_{PT} when I_L = 0. Subsequently, $V_{G,PC1} = V_{G,PC2}$ when I_L = 0. In other words, I_C sets a reference for comparison. Thus, as I_L increases, $V_{G,PC2}$ increases whereas $V_{G,PC1}$ stays constant. The voltage difference, ΔV_G, between $V_{G,PC1}$ and $V_{G,PC2}$ is then passed onto the simple OTA formed by M_{PC1}, M_{PC2}, M_{NC3} and M_{NC2}. Transistors M_{PC1} and M_{PC2} are identical, whereas transistors M_{NC3} and M_{NC2} are identical. The output current of the simple OTA, $I_d = I_{D,PC1} - I_{D,PC2}$, is then injected through current-mirrors into the resistive divider formed by two diode-connected MOSFETs, M_{PC6_top} and M_{PC6_bot} to derive V_{SW}. I_d can be calculated based on subthreshold-region operations of M_{NS1} and M_{NC1} via (4.8) as well as saturation-region operations of M_{PC1} and M_{PC2} via

$$I_D = \frac{1}{2}\mu_p C_{ox}(W/L)\left(V_{SG} - |V_{thp}|\right)^2. \quad \textbf{(4.9)}$$

It can be expressed in a quadratic polynomial of the varying parameter '$\ln(I_L)$' in (4.10)

$$I_d = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_{PC1,2} m_s V_T \alpha_V \cdot [-\alpha_V m_s V_T \ln^2(I_L) + (2V_{O-REF} - 2V_X\alpha_V)\ln(I_L) - (2V_{O-REF} - 2V_X\alpha_V)\ln(I_C) - \alpha_V m_s V_T \ln^2(I_C)], \quad \textbf{(4.10)}$$

where α_V = ¼ is the fraction of $V_{GS,NS1}$ or $V_{GS,NC1}$ from R_{S1}-R_{S4} or R_{C1}-R_{C4} respectively, $V_X = V_{thn,NS1,NC1} - m_s V_T \ln\left(\frac{\alpha_I I_C W_{NS1,NC1}}{L_{NS1,NC1}}\right)$; $V_{thn,NS1,NC1}$ is the threshold voltage of M_{NS1} and M_{NC1}; $W_{NS1,NC1}$ and $L_{NS1,NC1}$ are the channel width and length of identical transistors M_{NS1} and M_{NC1}.

Moreover, M_{PC6_top} and M_{PC_bot} are identical PMOS transistors in diode-connected configuration as resistors. Hence, at I_L = 0, I_d = 0, implying that no current is injected into M_{PC6_top}-M_{PC6_bot}. Hence, $V_{SW} = V_{O\text{-}REF}/2$. As I_L increases, I_d will increase, causing V_{SW} to increase. By having the same amount of I_d being mirrored and injected into M_{PC6_top}-M_{PC6_bot}, V_{SW} can be calculated and expressed in a quadratic polynomial of the varying parameter 'ln(I_L)' in (4.11)

$$V_{SW} = k_1 \ln^2(I_L) + k_2 \ln(I_L) + b, \quad \textbf{(4.11)}$$

where, by considering the fact that the threshold voltage of M_{PC6_top} and M_{PC6_bot}, $V_{th,PC6}$ > 0.4 V, k_1, k_2 and b in (4.11) are constants and given below:

$$k_1 = \begin{cases} -\dfrac{\mu_p C_{ox}\left(\frac{W}{L}\right)_{PC1,2} m_s^2 V_T^2 \alpha_V^2 (2V_{thp,PC6} - 0.7)}{4I_{D0}\left(\frac{W}{L}\right)_{PC6}}, V_{SW} \in [0.35, V_{thp,PC6}) \\ -\dfrac{\mu_p C_{ox}\left(\frac{W}{L}\right)_{PC1,2} \alpha_V^2 m_s^2 V_T^2}{2\left[I_X - I_{D0}\left(\frac{W}{L}\right)_{PC6}\right](0.7 - V_{thp,PC6})}, V_{SW} \in [V_{thp,PC6}, 0.7) \end{cases}$$

$$k_2 = \begin{cases} \dfrac{\mu_p C_{ox}\left(\frac{W}{L}\right)_{PC1,2} m_s V_T \alpha_V (V_{O-REF} - V_X\alpha_V)(2V_{thp} - 0.7)}{2I_{D0}\left(\frac{W}{L}\right)_{PC6}}, V_{SW} \in [0.35, V_{thp,PC6}) \\ \dfrac{\mu_p C_{ox}\left(\frac{W}{L}\right)_{PC1,2} m_s V_T \alpha_V (0.7 - V_X\alpha_V)}{\left[I_X - I_{D0}\left(\frac{W}{L}\right)_{PC6}\right](0.7 - V_{thp,PC6})}, V_{SW} \in [V_{thp,PC6}, 0.7) \end{cases}$$

$$b = \begin{cases} \dfrac{\mu_p C_{ox}\left(\frac{W}{L}\right)_{PC1,2} m_s V_T \alpha_V [(1.4 - 2V_X\alpha_V)\ln(I_C) + \alpha_V m_s V_T \ln^2(I_C)](0.7 - 2V_{thp})}{4I_{D0}\left(\frac{W}{L}\right)_{PC6}} + 0.35, \\ V_{SW} \in [0.35, V_{thp,PC6}) \\ \dfrac{\mu_p C_{ox}\left(\frac{W}{L}\right)_{PC1,2} m_s V_T \alpha_V [(1.4 - 2V_X\alpha_V)\ln(I_C) + \alpha_V m_s V_T \ln^2(I_C)] - 2I_{D0}\left(\frac{W}{L}\right)_{PC6}}{\left[I_X - I_{D0}\left(\frac{W}{L}\right)_{PC6}\right](1.4 - 2V_{thp,PC6})} + V_{thp,PC6}, \\ V_{SW} \in [V_{thp,PC6}, 0.7) \end{cases}$$

where $I_X = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_{PC6}(0.7 - V_{thp,PC6})^2$; $V_{thp,PC6}$ and $(W/L)_{PC6}$ are the threshold voltage and the aspect ratio of identical transistors M_{PC6_top} and M_{PC6_bot}. Note that k_1, k_2 and b are computed differently depending on the magnitude of V_{SW} or, alternatively, I_L. This is due to the consideration that both M_{PC6_top} and M_{PC6_bot} operate in the subthreshold region when $V_{O\text{-}REF}/2 \leq V_{SW} \leq V_{thp,PC6}$; M_{PC6_bot} drifts into the saturation region when $V_{SW} \geq V_{thp,PC6}$ while $M_{PC6,top}$ stays in the subthreshold region. In this work, $V_{O\text{-}REF} = V_{OUT} = 0.7$ V. A dedicated quadratic relation between V_{SW} and $\ln(I_L)$ is specifically configured to fit the simulated data on V_{SW}, shown in Fig 10b, to ensure that PM = 60°.

Furthermore, the current-mirror that mirrors and injects I_d into M_{PC6_top}-M_{PC6_bot} is formed by M_{PC3}, M_{PC4} and M_{PC5}. M_{PC4} and M'_{PC4} are identical except that the bulk terminal of M'_{PC4} is biased by a V_{DD}-tracking voltage, $V_{G,PC5}$. In other words, such current-mirror is made V_{DD}-dependent. To facilitate such feature, $V_{G,PC5}$ is derived from $V_{SG,PC5}$ of the diode-connected M_{PC5}, where $V_{SG,PC5} = V_{DD} - V_{G,PC5}$ is maintained constant by the constant-current-sink, I_{BC}, based on (4.9). Hence, as V_{DD} decreases, $V_{G,PC5}$ will decrease accordingly. Subsequently, the threshold voltage, $V'_{th,PC4}$, of M'_{PC4} decreases based on

$$V_{th} = V_{th0} + \gamma\left(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}\right), \quad \textbf{(4.12)}$$

where V_{th0} is the threshold voltage at $V_{SB} = 0$; γ is the body-effect coefficient; Φ_F is the work function of the silicon substrate; V_{SB} is the source-to-bulk voltage of a given MOSFET. In case of M'_{PC4}, $V_{SB} = V_{O\text{-}REF} - V_{G,PC5}$, where $V_{O\text{-}REF}$ is constant and regulated by the auxiliary LDO in Figure 4.6. In this manner, the V_{DD}-dependent current-mirror injects more current into M_{PC6_top}-M_{PC6_bot} to derive a higher V_{SW} at a lower V_{DD} for a given load condition. This is due to the

fact that, at sub-1-V V_{DD}, it is good to increase V_{SW} especially for heavy load conditions to ensure a high DC-gain, A''_{DC} by increasing $g''_{m,in}$ according to (4.4). In this manner, it compensates the inherently low DC-gain at sub-1-V V_{DD}. Specifically, the injected current, $I_{d,SW}$ (= $I_{D,PC4}$ + $I'_{D,PC4}$), into M_{PC6_top}-M_{PC6_bot} can be further computed based on (W_{PC3}/L_{PC3}) : (W_{PC4}/L_{PC4}) : (W'_{PC4}/L'_{PC4}) = 1 : 0.5 : 0.5 as

$$I_{d,SW} = I_d + \frac{\gamma\left(\sqrt{|2\Phi_F + V_{O-REF} - V_{G,PC5}|} - \sqrt{|2\Phi_F|}\right)\sqrt{2I_d\mu_p C_{ox}\left(\frac{W_{PC3}}{L_{PC3}}\right)}}{4}, \quad \textbf{(4.13)}$$

where $V_{G,PC5} = V_{DD} - |V_{thp,PC5}| - \sqrt{2I_{BC}L_{PC5}/\mu_p C_{ox} W_{PC5}}$.

4.3.2 Proposed Pass-Transistor Bulk-biasing

The proposed bulk-biasing for M_{PT} serves two purposes: firstly, to boost the DC-gain, A'_{DC}, further, the bulk voltage of M_{PT} is reduced and made adaptable with I_L as configured as V'_C in Figure 4.7. This is based on the consideration that $g_{m,PT}$ reduces as V_{DD} drops down, leading A'_{DC} to decrease according to Figure 4.3. To avoid raising W_{PT}/L_{PT}, which increases the chip area, this work proposes a reduced $|V_{thp,PT}|$ by bulk-biasing. This is achieved by duplicating the output branch M_{P5}-M_{N5} with M'_{P5}-M'_{N5} to have V'_C tracking V_C. Thus, as I_L increases, V_C is pulled down by the OTA and V'_C decreases accordingly. As a result, $g_{m,PT}$ and A'_{DC} increases.

Such effect is proved by simulation results in Figure 4.8. All dotted lines are DC-gains without bulk-biasing scheme by shorting the bulk to V_{DD}, whereas all solid lines are DC-gains with bulk-biasing implemented. As shown, it is more effective at moderate and heavy loads and less effective at light loads. Nonetheless, such improvement is sufficient to avoid a large W_{PT}/L_{PT} from catering for heavy loads and increasing chip area as it is conventionally when the bulk of M_{PT} is tied to V_{DD}.

Secondly, the bulk-biasing also speeds up the load-transient-response. It shortens Δt_S by increasing $g_{m,PT}$ according to (4.2). Take a low-to-high load transient for an instance. The G_m-cell-based OTA detects the change, ΔV_G, at its input and pulls down V_C and V'_C to cater for the heavy load. The decrease in

V_C increases $g_{m,PT}$ based on (4.3). This is similar to conventional cases when no bulk-biasing is implanted. However, with bulk-biasing, the decrease in V'_C speeds up the increase in $g_{m,PT}$ by adding into another factor of flexibility with a decreasing $V_{thp,PT}$ upon the load-transient. Similar explanation can be derived upon a low-to-high transient as well.

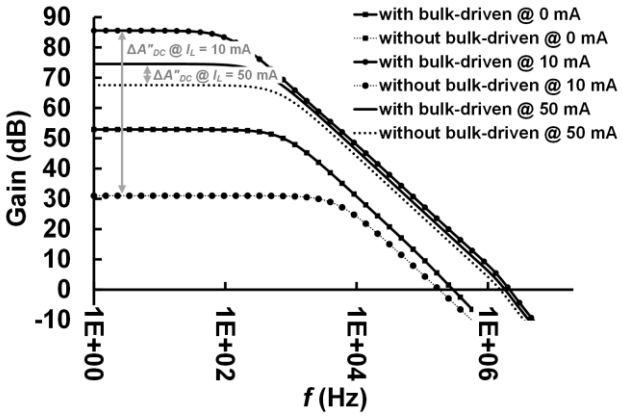

Figure 4.8 Simulation results to show the effect of M_{PT} bulk-biasing in raising the DC-gain, A'_{DC}, of the proposed OCL-LDO at I_L = 0 mA, 10 mA and 50 mA.

The improvements in load-transient-response by the proposed M_{PT} bulk-biasing are proved by simulation results and shown in Figure 4.9. All dashed lines are results without bulk-biasing scheme by shorting the bulk to V_{DD}, whereas all solid lines are results with bulk-biasing implemented. Moreover, the simulation results are collected under V_{DD} = 0.8 V by having I_L stepping up from 0 mA to 50 mA or stepping down from 50 mA to 0 mA. In this manner, by taking 1% deviation from the nominal value of 0.7 V as the settling condition, Δt_S is improved by 36.8% and the undershoot magnitude is improved by 30.9% in case of a 0-to-50-mA load-transient when the proposed bulk-biasing is compared with the conventional configuration when the bulk is tied to V_{DD}. It is improved by 29% in case of a 50-mA-to-0 load-transient.

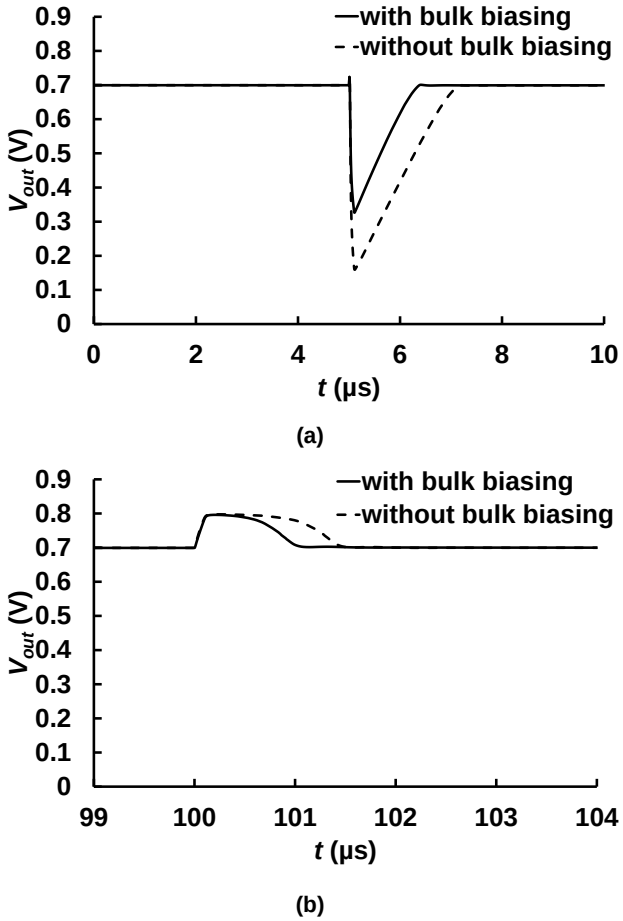

Figure 4.9 Simulation results to show the effect of M_{PT} bulk-biasing in speeding up the load-transient-response with ΔI_L = 50 mA.

4.3.3 Proposed Process-Tracking Current-Sink

A PTCS, denoted as I_{p_track} in Figure 4.7, is integrated into the proposed LAC to guarantee fast-settling of the proposed OCL-LDO against process variations. The detailed circuit-diagram of I_{p_track} is shown in Figure 4.10a. The need for such circuit is due to the finding that the desired V_{SW} at a given I_L varies with process fluctuations. In this work, the desired V_{SW} is chosen to ensure PM = 60°, which ensures fast-settling by approximating a critically-damped load-transient-response in a second-order system. This is indicated by the simulation data in Figure 4.10b, where I_{OUT} includes I_L and current sunk by OTA1 inputs. The simulation is performed with I_L = 0 to 100 mA and V_{DD} = 0.8 V. More specifically, the desired V_{SW} increases as process parameters deviate from the 'typ' process corner; and such trend becomes more significant at heavy loads.

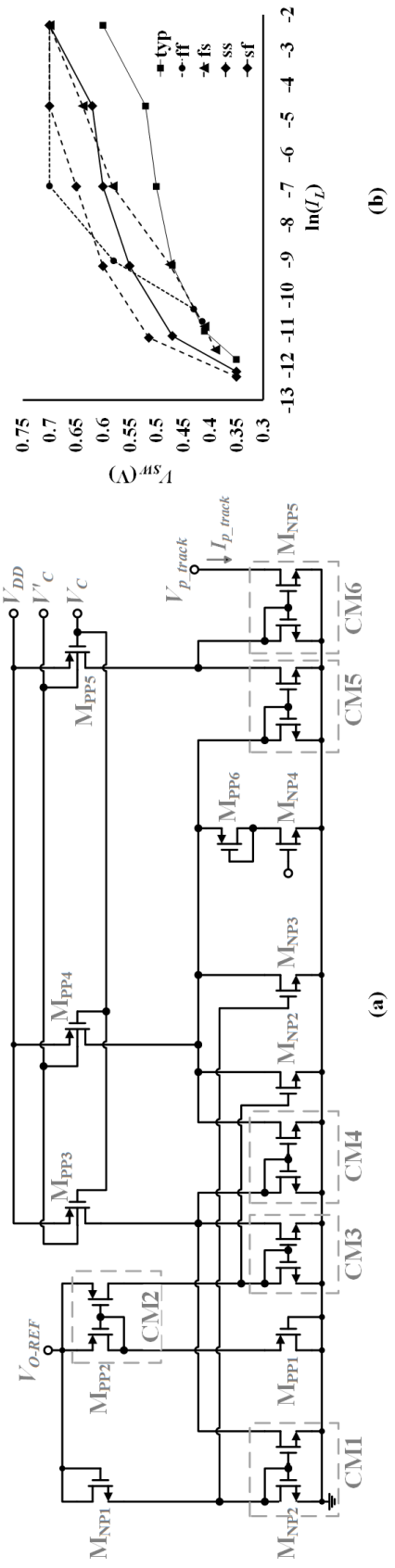

Figure 4.10 Proposed PTCS in (a) circuit diagram and (b) plot of V_{SW} based on simulation results to ensure PM = 60° across all loads and across all process corners.

To compensate process variations, the proposed PTCS sinks additional process-adaptive I_{p_track} at V_{p_track} in the LAC in Figure 4.7 to increase V_{SW}. This is achieved by implementing the process-tracking NMOS M_{NP1} and PMOS M_{PP1}. In this manner, upon a process corner with a 'slow NMOS', less current will be through M_{NP1}-M_{NP2}; similarly, upon a corner with a 'slow PMOS', less current will be through M_{PP2}-M_{PP1}. Moreover, M_{PP3}-M_{PP5} are load-adaptive current-sources similar to M_{PT_S}, which senses I_L. On top of the increase in I_d by a load-adaptive V_{SW} as I_L increases, such configuration ensures an increasing I_{p_track} being added into I_d to adjust V_{SW}. It ensures that V_{SW} tracks the 'ss'-corner where I_{p_track} will be increased if compared with its magnitude at the 'typ'-corner. Furthermore, at 'sf'-corner, I_{p_track} is compensated and raised through CM5-6 from M_{PP2}-M_{PP1}, CM3, and M_{NP2}; similarly, I_{p_track} is compensated and raised through CM5-6 from M_{NP1}-M_{NP2}, CM1, and M_{NP3} at 'fs'-corner. Lastly, at 'ff'-corner, I_{p_track} is compensated and raised from CM5-6 through both M_{NP2} and M_{NP3} from M_{PP2}-M_{PP1} and M_{NP1}-M_{NP2} as it does at 'sf'- and 'fs'-corner; in addition, it is also increased from M_{PP6}-M_{NP4}, which is dedicated to 'ff'-corner by considering V_{SW} entailed is the highest among all corners as illustrated in Figure 4.10b.

4.3.4 Frequency Stability

A small-signal diagram of the proposed OCL-LDO is shown in Figure 4.11, where OTA1 is circled in dashed line. The three poles concerned are the dominant-pole, $p'_d = -1/(C_{o1}r_{o1})$, at the gate of M_{PT}, where C_{o1} is the lumped parasitic capacitance, and r_{o1} is the output resistance of OTA1; the non-dominant-pole, $p'_o = -1/(C_{out}r_{out})$, is derived from the output node of the LDO, where C_{out} is the lumped capacitance involving all parasitic capacitances and the load capacitance, C_L; r_{out} is the effective resistance derived from the output of the LDO; $p'_{N,1\&2} = -\left(g''_{mN,3\&4} - g'_{mN,1\&2} + g_{ds,HL} + g''_{dsN,3\&4} + g'_{dsN,1\&2}\right)/C_{N,1\&2}$ is another non-dominant-pole, contributed by the PPF structure with the proposed load-adaptive negative-resistance; $C_{N,1,2}$ is the lumped parasitic-capacitances at drain terminals of M_{N2} or M_{N1}.

To ensure frequency stability across the loads, $g'_{mN,1\&2}$ is adjusted by V_{SW} according to I_L. Essentially, $g'_{mN,1\&2}$ is reduced as I_L drops, leading to a reduced

$g''_{m,in}$, according to (4.4), and subsequently, a slightly reduced A''_{DC} as illustrated by simulation results at I_L = 0 mA and V_{DD} = 0.8 V in Figure 4.12, where dashed lines refer to the conventional design; dotted lines refer to the proposed design.

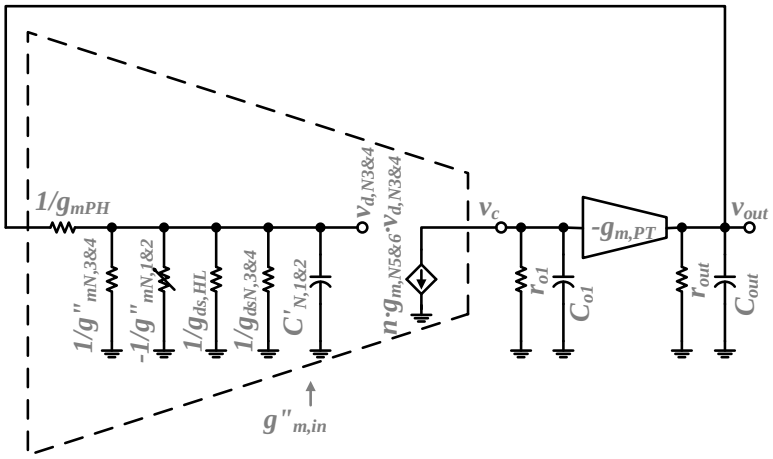

Figure 4.11 A closed-loop small-signal diagram of the proposed OCL-LDO.

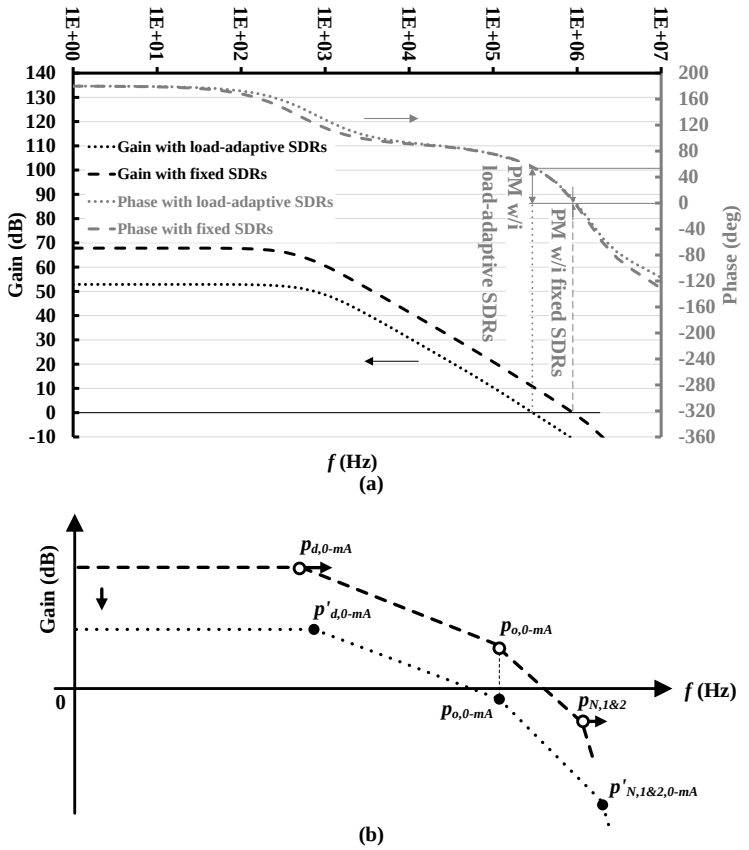

Figure 4.12 Frequency responses of the conventional PPF-incorporated LDO and the proposed LDO with load-adaptive negative-resistance in (1) simulation results and (b) bode plots.

In comparison with Figure 4.5, the cross-over frequency of the gain plot is lowered for the proposed design when I_L drops. As its phase plot stays relatively unchanged in comparison with the conventional design, a larger PM can be obtained [45] to ensure frequency stability as shown in Figure 4.12a.This is done by the proposed LAC to lower V_{SW} at light load in comparison with its value at heavy load. Besides A''_{DC} reduction, the reduction in V_{SW} also pushes $p'_{N,1\&2}$ to a higher frequency. This improves the phase response to increase PM further as shown in Figure 4.12.

4.3.5 Load Transient Response

The load-transient response is enhanced from three aspects. Firstly, from (4.2), the settling time, $\Delta t''_S$, is shortened by a boosted input transconductance, $g''_{m,in}$. Such effect is particularly prominent at heavy loads due to the relatively large V_{SW} derivable from (4.4), (4.7) and (4.11). In comparison, at light loads, the effect of $g''_{m,in}$ is mitigated due to the reduced V_{SW}.

Secondly, the proposed bulk-biasing for M_{PT} also speeds up the settling time by raising $g_{m,PT}$ in (4.2) due to the lowered $|V_{thp,PT}|$ in (4.3) according to (4.12). The proposed bulk-biasing configuration is more effective than shorting the bulk terminal to the gate of M_{PT} as it is in the Dynamic Threshold-voltage MOS (DTMOS). This is due to the duplicated branch M'_{P5}-M'_{N5}, which sources the sinking current to the bulk terminal and lessens the burden from branch M_{P5}-M_{N5}. In this manner, the branch M_{P5}-M_{N5} which only needs to source and sinks current to the parasitic capacitance at the gate of M_{PT} during the load-transient response.

Thirdly, the proposed PTCS ensures fast-settling despite process variations. The process-tracking I_{p_track} derives a larger V_{SW} in comparison with its value at ‘typ’ corner to maintain PM of the overall OCL-LDO around 60° across all loads. The increased V_{SW} not only helps to boost $g''_{m,in}$, but also shifts $p'_{N,1\&2}$ to lower frequencies at heavy loads to reduce the excessive PM, which can be higher than 76° for a second-order system and results in slow over-damped responses.

4.4 Results and Discussions

A micrograph of the proposed OCL-LDO is shown below in Figure 4.13. The chip takes an area of 0.16 mm^2. The proposed OCL-LDO can realize line regulation beyond V_{DD} = 0.72 V under no-load condition and V_{DD} = 0.8 V under full load of 80 mA as indicated in Figure 4.14 by taking 10 mV as the tolerance around the targeted 0.7 V. An average Line Regulation of 3.07 mV/V and 5.56 mV/V can be achieved under no load and full load respectively. These correspond to a 0.4%/V and a 0.8%/V in LS.

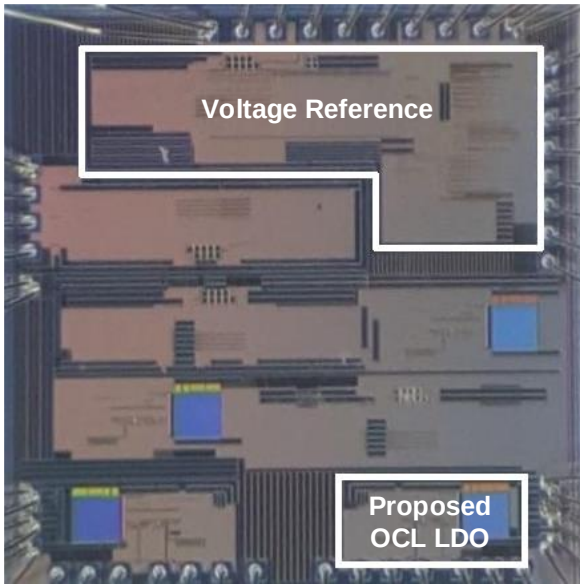

Figure 4.13 Micrograph of the proposed OCL-LDO.

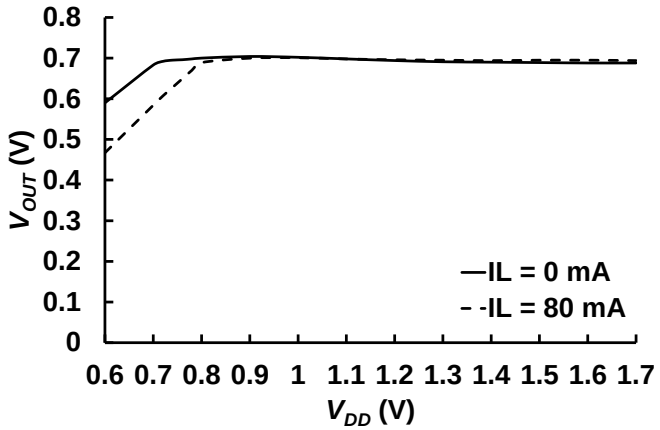

Figure 4.14 Measurement results of line regulation.

Moreover, by defining PSR as $PSR = 20\log(dv_{out}/dv_{dd})$ to characterize "the

vulnerability of the circuit to noise injected through the input supply" [39, 44] as well as "supply-induced variations in reference v_{REF}" [39], the PSR performance of the proposed OCL-LDO is shown in Figure 4.15 and Figure 4.16.

According to measurement results in Figure 4.15, a PSR around -34 dB can be achieved up to 1 kHz under no-load and V_{DD} of 0.8 V. Under V_{DD} of 1.5 V, PSR at 1 kHz is around -47 dB. These are slightly worse than simulation results at the typical process corner shown in Figure 4.16. This can be attributed to process variations. Nevertheless, by considering powering the LDO with a secondary battery within the WSN sensor node, such PSR can be sufficient to ensure a quiet supply to the loading ICs within the sensor node.

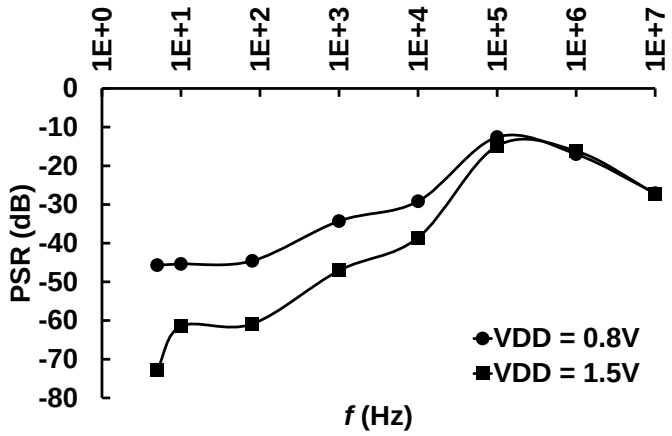

Figure 4.15 Measurement results of PSR under no load condition.

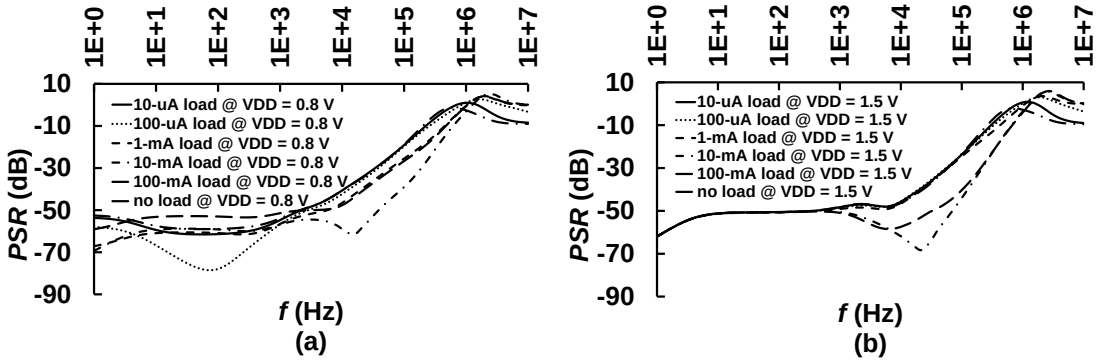

Figure 4.16 Simulation results of PSR at V_{DD} = 0.8 V and V_{DD} = 1.5 V.

The load transient responses are displayed in Figure 4.17. A transient step up and down of the load current, I_L, between I_L = 1 mA and I_L = 51 mA is measured in 100 ns to derived results in Figure 4.17. Under V_{DD} = 0.8 V, the

proposed OCL LDO takes $\Delta t_{S,undershoot}$ = 3.1 µs to recover from a 1-mA-to-51-mA transient and $\Delta t_{S,overshoot}$ = 1.51 µs from a 51-mA-to-1-mA transient. Similarly, from a 30-mA-to-80-mA transient, $\Delta t_{S,undershoot}$ = 2.99 µs is taken for output recovery and $\Delta t_{S,overshoot}$ = 2.05 µs for a 80-mA-to-30-mA output recovery. All data on the settling time are collected based on the timing difference between the onset of transient response and the instance when 1% of the nominal value is reached. The relatively larger overshoot and undershoot amplitude during load transient between 1 mA and 51 mA is attributed to the slower V_{SW} response time in comparison with that during the load transient between 30 mA and 80 mA.

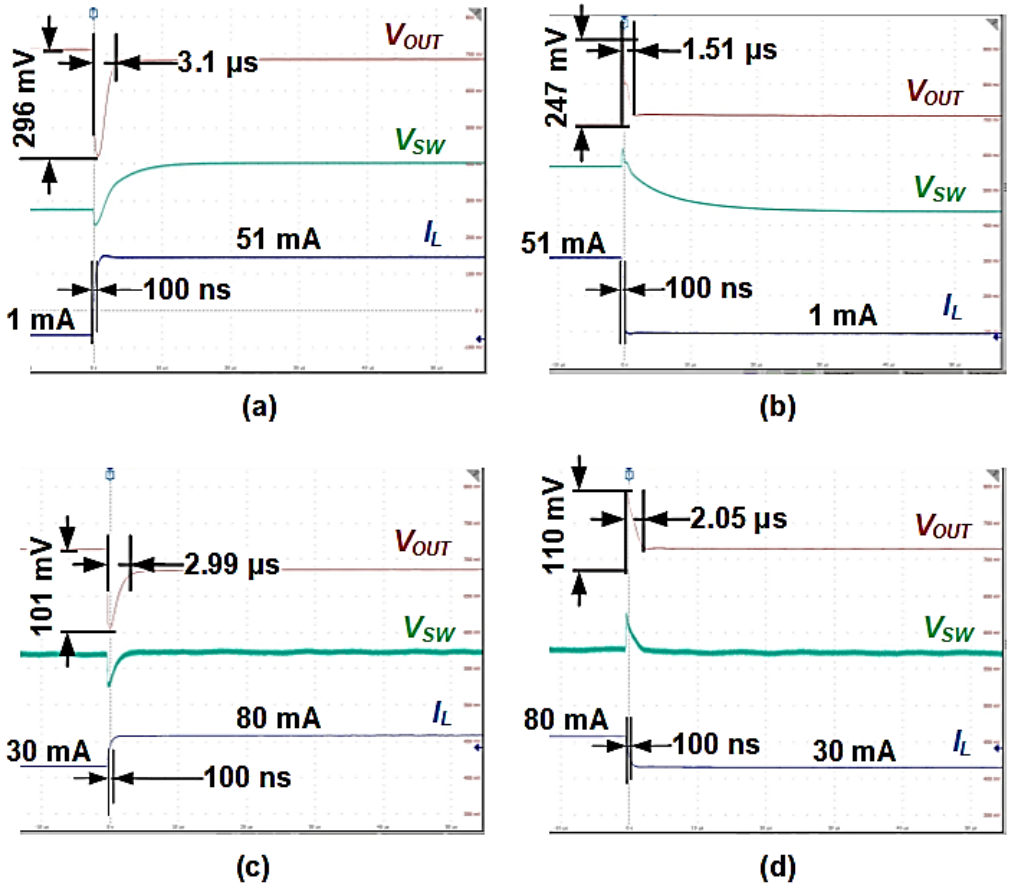

Figure 4.17 Measurement results of load transient responses under V_{DD} = 0.8 V with ΔI_L = 50 mA in (a) undershoot transient from 1 mA to 51 mA, (b) overshoot transient from 51 mA to 1 mA, (c) undershoot transient from 30 mA to 80 mA and (d) overshoot transient recovery from 80 mA to 30 mA.

The I_L-tracking capability of the proposed load-adaptive LAC is verified by measurement results in Figure 4.18, indicating approximately a quadratic relation between the derived V_{SW} versus I_L from 100 uA to 80 mA under various

V_{DD}. Moreover, as sought after, the derived V_{SW} across all I_L gets increasing larger at a higher V_{DD}. Note that the horizontal axis is plotted in logarithmic scale to reflect the dimension of ln(I_L) to demonstrate the intended relation between V_{SW} and I_L.

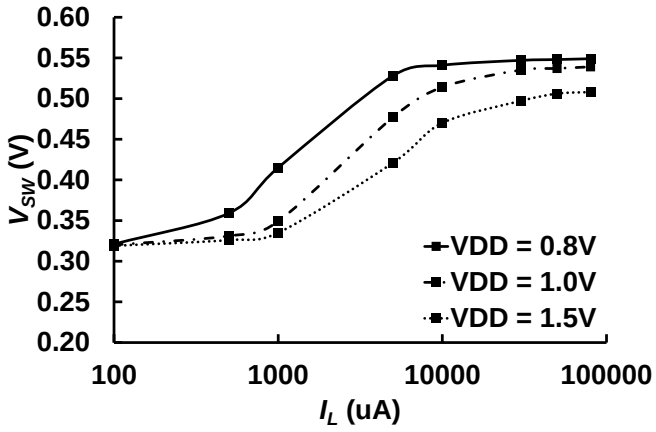

Figure 4.18 Measurement results of LAC output, V_{SW}, across I_L.

The effectiveness of the derived V_{SW} to ensure stability and fast-settling load transient response is displayed in Figure 4.19. Across all loads, PM between 50 to 80 degree can be achieved at V_{DD} = 0.8 V and V_{DD} = 1.5 V. Such PM is in the vicinity of 76 degree of a second-order control system for critical damped transient response.

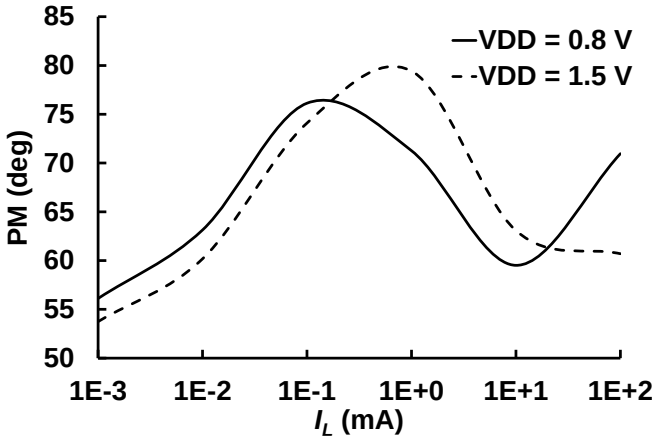

Figure 4.19 Simulation results of the resulted PM based on V_{SW}.

In addition, Figure 4.20 the overall quiescent current consumption of the proposed OCL-LDO involving the current sourcing VR-adapter circuits in Figure 4.6 under no-load conditions. Across the targeted V_{DD}, the proposed OCL-LDO

consumes quiescent current lower than 21 µA.

Detailed current distribution into each functional block of the proposed OCL LDO is illustrated in Figure 4.21. Specifically, the proposed circuitries consume only 2.6% of the total quiescent current. The majority of the quiescent current is consumed by the PPF-incorporated G_m-cell based structure. This is to ensure sufficient charging and discharging current for fast-settling load transient response according to (4.2) and enough input transconductance and DC gain for good line regulation according to (4.4).

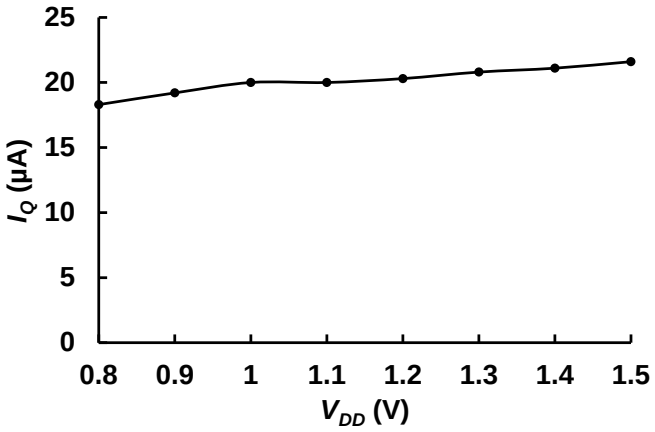

Figure 4.20 Measurement results of I_Q.

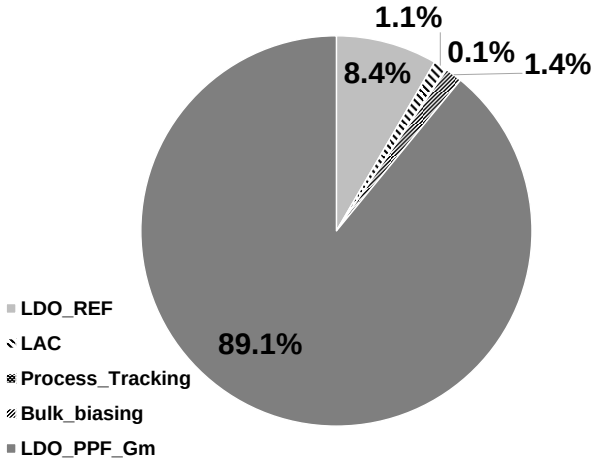

Figure 4.21 Current distribution of the proposed OCL LDO.

4.5 Concluding Remarks

TABLE 4.1 compares the overall performances of the proposed OCL-LDO against prior works, where *K*-factor refers to the ratio between Δt_S of the

particular work versus the best Δt_S among all works in the table [81] and FOM_1 characterize the load-transient behavior alone and follow the definition in (2.57).

Despite that fact that FOM_1 of the proposed OCL-LDO appears less competitive against some of the previous works, such criteria as FOM_1 is biased towards output ripple during transient response and quiescent current consumption only. Admittedly, such performance indices are critical, they insufficient to evaluate the strength of an LDO for a dedicated application, such as a WPT-powered WSN sensor node. In doing so, other critical factors, such as sub-1-V operations, response speed and power efficiency have to be considered as well. In this manner, a more dedicated criteria, such as FOM_2 has to be added upon FOM_1. In this manner, FOM_2 is defined as

$$FOM_2 = FOM_1 \Delta t_S V_{DO} V_{DD,min} \tag{4.14}$$

TABLE 4.1 PERFORMANCE COMPARISON AGINST PREVIOUS WORKS

	[81]	[85]	[80]	[83]	This work
Year	2010	2010	2018	2018	2019
Publication	JSSC	JSSC	TCASI	TPE	-
Technology (μm)	0.09	0.35	0.065	0.13	0.18
Active Area (mm^2)	0.019	0.155	0.0021	0.0046	0.16
$V_{DD,min}$ (V)	0.75	0.95	1	1.2	0.8
V_{DO} (V)	0.25	0.2	0.2	0.2	0.1
V_{OUT} (V)	0.5	0.7	0.8	1	0.7
$I_{L,max}$ (mA)	100	100	25	50	80
I_Q (@ no load) (μA)	8	43	24.2	42	21
Load Reg. (mV/mA)	0.1	0.4	0.28	0.01	0.088
Line Reg. (mV/V)	3.78	-	0.7	0.3	3
Settling time, Δt_S (μs)	4.9	3	3.6	0.24	2.05
ΔV_{OUT} (mV)	114	70	32	80	110
ΔI_{OUT} (mA)	97	99	25	50	50
PSR (dB) @ freq	-44@1kHz	-	-50@1kHz -26@1MHz -11@10MHz	-93@1kHz -64@1MHz	-34@1kHz -16@1MHz -27@10MHz
Edge time (ns)	100	100	100	100	100
K factor	1	1	1	1	1
FOM_1 ($mV/\mu m^2$)	1.16	0.25	7.33	3.98	1.36
FOM_2 ($ms \cdot V^3/m^2$)	0.84	0.14	5.28	0.23	0.22

The proposed design exhibits the second best FOM_2 among all works

listed in TABLE 4.1. Moreover, in spite of a better FOM_2 in [85], its PSR is unavailable. This can be problematic under the scenario when the LDO is powered directly through a fluctuating rectifier input. The lack of good power rejection will lead to a noisy supply output from the LDO and corrupt signal outputs of the loading ICs, such as the ADC and RF transceivers. In comparison, the proposed OCL LDO offers power supply rejection capability up to 10 MHz. This makes it more desirable in comparison with the LDO in [85].

In addition, despite a relatively large I_Q of 20 μA, it is the product $I_Q V_{DO}$ that matters when power efficiency is concerned according to Equation (2.15) and Equation (2.16). With an V_{DO} as low as 0.1 V, the proposed OCL LDO still exhibits the lowest $I_Q V_{DO}$ of 2 μA·V when compared with prior works.

Topologically, the proposed OCL-LDO offers a practical approach to make use of PPF-incorporated G_m-cell-based OTA as an EA for an OCL-LDO for a wide range of I_L. It addresses the trade-off between current-efficiency, frequency stability and fast-settling transient responses effectively with the proposed PV-invariant LAC.

Besides, in comparison with digital LDOs, which are well known for deriving low V_{DD}, the proposed LDO exceeds its digital counterparts in various factors, such as power efficiency, transient recovery as well as PSR. The proposed LDO displays both FOM_1 and FOM_2 that are far better than its digital LDOs listed in TABLE 4.2.

The main advantages of the proposed LDO versus its digital counterparts are its OCL feature and the low quiescent power consumption. The OCL feature saves space by eliminating bulky output capacitors, which are large and indispensable in case of digital LDOs for output ripple reduction. Quiescent power consumption and dropout voltage are both lower in the proposed design than the digital LDOs due to the absence of the power-consuming digital circuits. Also, the PSR of most digital LDOs are also unavailable as indicated in TABLE 4.2. This is also undesirable in case of a WSN sensor node implementations.

Therefore, the proposed LDO still presents the best features overall in

terms of power efficiency, transient recovery as well as supply noise rejection. These are the most desirable features to build a WPT-enabled PMU for a WSN sensor node.

TABLE 4.2 PERFORMANCE COMPARISON AGAINST DIGITAL LDOS

	[86]	[87]	[88]	[89]	This work
Year	2016	2018	2016	2019	2019
Publication	JSSC	JSSC	TCASII	ISCAS	-
Technology (μm)	0.028	0.065	0.065	0.065	0.18
Active Area (mm^2)	0.021	0.0374	0.01	0.17	0.16
$V_{DD,min}$ (V)	1.1	0.6	0.6	0.6	0.8
V_{DO} (V)	0.2	0.2	0.2	0.1	0.1
V_{OUT} (V)	0.9	0.4	0.4	0.5	0.7
$I_{L,max}$ (mA)	200	100	100	100	80
C_{out} (nF)	23.5	0.04	1	1	OCL
I_Q (@ no load) (μA)	110	100	82	34.6	21
Load Reg. (mV/mA)	0.1	0.64	0.06	0.11	0.088
Line Reg. (mV/V)	3.78	-	3	-	3
Settling time, Δt_S (μs)	44	1.24	0.7	3	2.05
ΔV_{OUT} (mV)	120	108	55	53	110
ΔI_{OUT} (mA)	180	50	88	100	50
PSR (dB) @ freq	-	-38@1MHz -16@10MHz	-	-	-34@1kHz -16@1MHz -27@10MHz
Edge time (ns)	4000	1000	100	1000	100
K factor	40	10	1	10	1
FOM_1 ($mV/\mu m^2$)	3741.5	511.24	12.13	43.40	1.36
FOM_2 ($ms \cdot V^3/m^2$)	36217	76.1	1.02	7.81	0.22

Chapter 5 A PWM DCM Boost Converter with Low Output Ripples and Fast Load Transient Response Based on Square-Root Voltage Mode (SRVM) Control Approach [90]

In a WPT-powered WSN sensor node, the input of the DC-DC converter for a battery-equipped WSN sensor node usually expects a rectenna-output of 0.21 V to 1 V [13]. Thus, this work assumes a 0.9-V input to the DC-DC converter, which loads the rectenna. With reference to Figure 2.2 and Equation (2.12), impedance network can be implemented as demonstrated in Figure 2.1 to derive the optimal load impedance to the rectenna, $R_{L\_rec,OP}$, to maximize $\eta_{RF\text{-}DC}$. Nonetheless, with a 0.9-V rectenna-output, the optimal load current to the rectenna, $I_{o\_rec,OP}$ to derive $R_{L\_rec,OP}$ could be in contradiction with the optimal charging efficiency for the secondary battery in case of a battery-equipped WSN sensor node. Hence, an inevitable compromise between $\eta_{RF\text{-}DC}$ and the charging efficiency might exist under such scenario as stated previously.

Moreover, based on Figure 1.2 and TABLE 2.1, the output of the DC-DC converter is specified as 3 V to power up the µP within the WSN sensor node. Thus, a boost DC-DC converter is needed to regulate a 0.9-V rectenna-output into a stable 3-V output as the supply voltage to the loads, such as µP and memories, within the sensor node. Subsequently, with reference to TABLE 2.5 and the active-mode power consumption of various WSN sensor nodes, the maximum output current, $I_{O,max}$, of the boost converter is set to be 40 mA.

Furthermore, the loading µPs often demand such boosted output to exhibit fast-settling load-transient-recoveries with small voltage ripples. Transient responses of conventional Continuous-Conduction-Mode (CCM) boost converters are limited by the RHP zero, the effect of which results in insufficient energy delivery to the converter output during load-transients. It causes contrary output responses against the controller expectations [91]. To overcome such effects, many solutions have been developed, such as WTE techniques [69], ACC controllers [69, 70], OSS techniques [69] and so on. The rationale of

boosting V_{EA} at the EA output from [69] and [70] upon load-transients offers insights in developing a fast-settling controller in this work. Also, the dual-loop controller for a boost converter introduced in [68] inspired the compensator-less design in this work. However, the large output ripples resulted from the aforementioned control techniques are still large. This has to be addressed in the proposed compensator-less controller in this work without losing the strength in accelerating the load-transient-responses.

To present such solutions, this chapter begins by proposing the two-phase dual-purpose start-up control approach. This is followed by the proposed compensator-free SRVM controller for DCM modulation to enhance load transient responses while minimizing output ripples. Accordingly, key design parameters, such as switching frequency f_S, inductor L, output capacitor C_{OUT} and so on, are derived afterwards. In addition, a signal booster is also proposed to minimize conduction losses from the main switches. Small-signal analysis is conducted afterwards to verify frequency stability of the design. Simulation results by MATLAB are presented also. A conclusion is drawn at the end of the chapter.

5.1 Proposed Control Techniques

A block diagram of the proposed boost converter is shown in Figure 5.1. The free-wheeling MOSFET switch M_{FW} reduces power losses from voltage oscillations at the drain nodes of M_P and M_N; it is on only when both MOSFET switches M_N and M_P are off. V_{Tm} is the peak amplitude of the saw-tooth waveform, V_T, for PWM control.

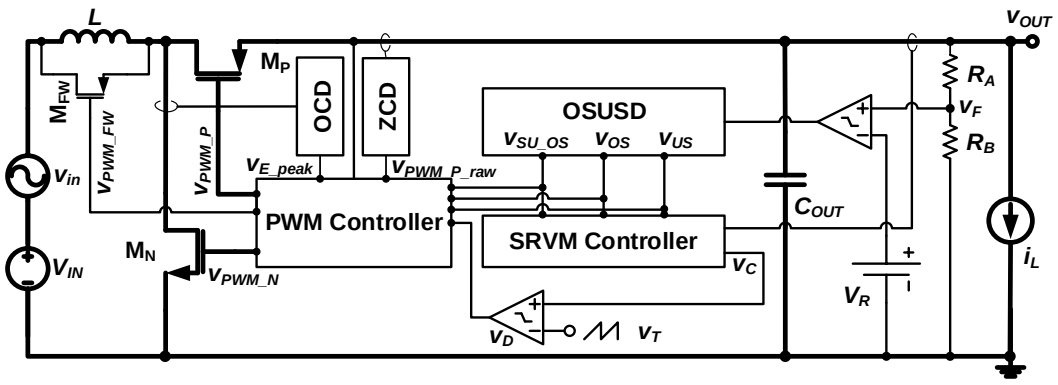

Figure 5.1 Block diagram of the proposed boost converter.

5.1.1 Proposed Two-phase Dual-purpose Start-up Control

The converter output is charged up from 0 V to its nominal steady-state value V_{OUT} through the proposed two phases. 1) In phase I, the output is charged up through charge sharing with the input. 2) Once the output reaches the vicinity of V_{IN}, phase II will start. In phase II, the controller invokes logics which is also utilized for transient undershoot recovery to initiate peak-current control in Boundary Conduction Mode (BCM) mode illustrated in Figure 5.2b. Phase II ends once the output reaches V_{OUT}.

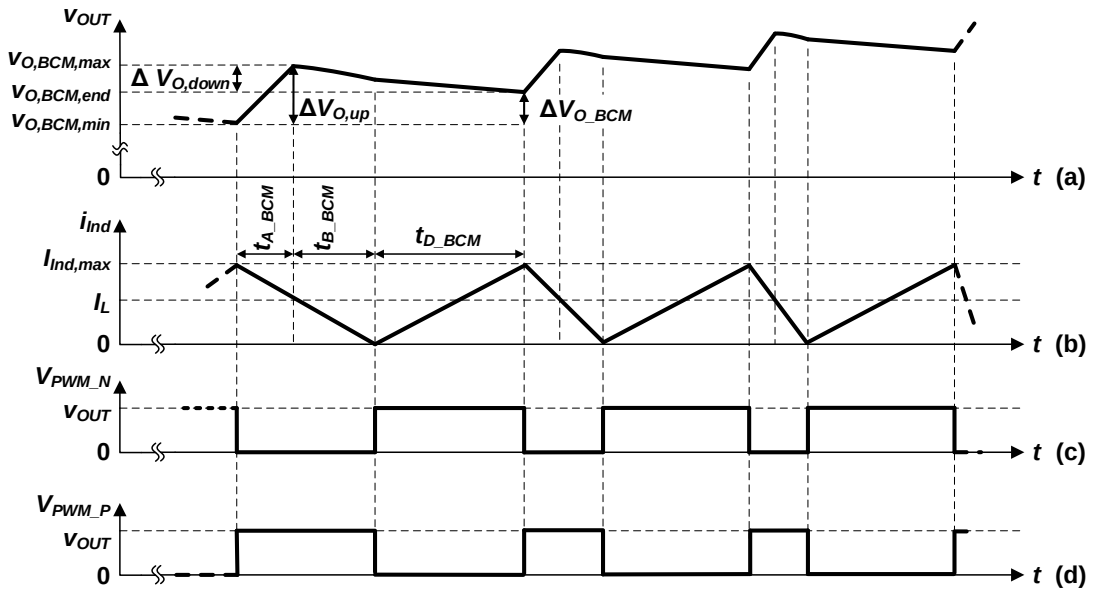

Figure 5.2 Illustrations on peak-current BCM mode start-up control. (a) Waveform of voltage v_{OUT}. (b) Waveform of inductor current i_{Ind}. (b) Waveform of control signals for M_N. (c) Waveform of control signals for M_P.

Thus, the converter operates in a frequency-varying manner with a fixed upward slope of $di_{Ind}/dt = V_{IN}/L$, and a steepening downward slope of $(V_{IN} - v_{OUT})/L$ due to the ramping v_{OUT}. Not only invoked during start-up, such control mechanism is also activated during low-to-high load-transient-recoveries. Details on transient recovery mechanisms will be explained in the next section.

Note that the boost converter under the proposed start-up controller is not susceptible to sub-harmonic oscillations. Thus, no closed-loop instability issue exists during start-up. This is due to the fact that the start-up controller operates in BCM modulation. In other words, any perturbation at the beginning

of the M_P on-time results in a phase delay in the inductor current waveform only. The next cycle is not forced to begin as it is in the case of constant-frequency modulation [92]. Rather, it only begins till the zero-current crossing is detected by the high-side Zero Current Detector (ZCD) in Figure 5.1. In doing so, the start-up controller operates in a frequency varying manner.

5.1.2 Proposed SRVM Controller

Analyses on power consumption in WSN µPs reveal an operational power interval between 16.5 mW to 400 mW [19], which falls into the light-load range for µPs under 3-V supply voltage [93]. This enables the use of DCM boost converters. Empirical studies on PWM DCM boost converters reveal that the duty ratio D, which is to turn on M_N, follows a square-root relation with respect to the load current, I_L, [94] as shown in (5.1)

$$D = \sqrt{\frac{2f_S L M_{V\_DC}(M_{V\_DC}-1)}{V_{OUT}}} \cdot \sqrt{I_L}\,, \tag{5.1}$$

where the conversion ratio $M_{V\_DC} = \frac{V_{OUT}}{V_{IN}}$; f_S is the switching frequency; $R_L = \frac{V_{OUT}}{I_L}$ is the equivalent load resistance; L is the inductance and V_{OUT} is the nominal output voltage at steady-state. All these are constants. The proposed SRVM controller leveraging on such concepts is shown in Figure 5.3, where $R_1 = R_2 = R_3 = R_4$, $R_5 = R_6$, and $R_7 = R_8$. The load current, I_L, is sensed and converted to voltage V_{SRVM_S} through the sense amplifier OP_{sense}. It is then conditionally topped up by V_{margin} according to v_{OS} by the sum amplifier OP_{sum}. The resulted V_{SR_I} is fed to the Square-Root (SR) circuit and multiplied by $(R_9 + R_{10})/R_9$ to obtain v_C. Therefore, D in (5.1) can also be expressed correspondingly as

$$D = D_1 = \frac{(R_9+R_{10})}{V_{Tm}R_9}\sqrt{R_{S\_SRVM}} \cdot \sqrt{I_L}. \tag{5.2}$$

However, due to power losses, energy delivered to C_{OUT} in duty ratio D given in (5.2) is insufficient and leads to consistent output dipping from V_{OUT} at the steady-state. To compensate such dipping, addition of V_{margin} into V_{SRVM_S} serves as a negative feedback to increase v_C, which equals DV_{Tm}. Such addition occurs whenever v_{OS} = '0', indicating $v_F < V_R$. The increased duty ratio D_2 can be computed to be

$$D_2 = \frac{(R_9+R_{10})}{V_{Tm}R_9}\sqrt{R_{S\_SRVM}I_L + V_{margin}}\ . \tag{5.3}$$

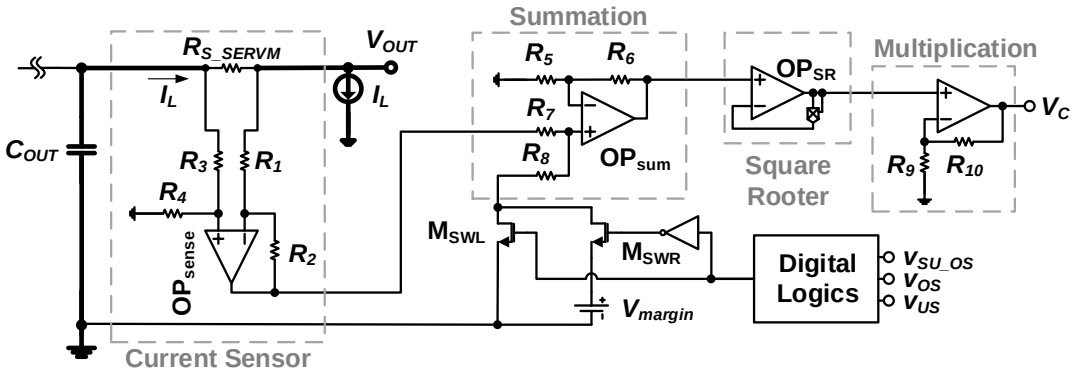

Figure 5.3 Block diagram of the proposed SRVM controller.

The dipping compensation by V_{margin} is illustrated in Figure 5.4. To ensure that the output is pulled back to V_{OUT}, which equals $[V_R(R_A + R_B)]/R_B$, the minimum of V_{O2}, $V_{O2,min}$, should satisfy

$$V_{O2,min} \geq \frac{V_R(R_A+R_B)}{R_B}(= V_{OUT}). \tag{5.4}$$

By the principle of charge conservation in the time interval t_{A2},

$$C_{OUT}\Delta V_{O,up} = C_{OUT}(V_{OP2} - V_{OUT} + nV_{r1}) = (I_{LP2} + I_L)\frac{t_{A2}}{2} - I_L t_{A2}, \tag{5.5}$$

where $I_{LP2} = \frac{D_2 T_S V_{IN}}{L}$, $t_{A2} = \frac{(I_{LP2}-I_L)L}{V_{OUT}-V_{IN}} = \frac{D_2 T_S V_{IN} - I_L L}{V_{OUT}-V_{IN}}$, $n = round\left(\frac{t_{dSVRM}}{T_s}\right) + 1$ is the number of cycles elapsed before v_{C2} emerging at the EA output. This is due to the loop delay, t_{dSRVM}, between the inception of output-dipping and the emergence of v_{C2}. For simplicity purposes, Figure 5.4 is drawn based on n = 1. By assuming $V_{O1,max} \approx V_{OUT}$, the value of V_{r1} is calculated as in (5.6) according to [95]:

$$V_{r1} \approx \frac{I_L}{C_{OUT}f_S} + \frac{LI_L^2}{2C_{OUT}(V_{OUT}-V_{IN})} - \frac{V_{OUT}\sqrt{2Lf_S V_{OUT}(V_{OUT}-V_{IN})}}{C_{OUT}f_S(V_{OUT}-V_{IN})}\left(\frac{V_{OUT}}{I_L}\right)^{-\frac{3}{2}}. \tag{5.6}$$

Similarly, on the time interval ($t_{B2} + t_{C2} + D_1T_S$),

$$C_{OUT}\Delta V_{O,down} = C_{OUT}(V_{OP2} - V_{OUT}) = (t_{B2} + t_{C2} + D_1 T_S)I_L - \frac{I_L t_{B2}}{2}, \tag{5.7}$$

where $t_{B2} = \frac{I_L L}{V_{OUT} - V_{IN}}$ and $t_{C2} = T_s - D_2 T_s - t_{A2} - t_{B2}$. Thus, combine (5.3) to (5.7) while ensuring DCM conduction. V_{margin} can be obtained as

$$V_{margin} = \frac{D_2^2 \, {V_{Tm}}^2 R_9^2}{(R_9 + R_{10})^2} - I_L \, R_{S\_SRVM}, \tag{5.8}$$

where $D_2 \in \left[L\,(V_{OUT} - V_{IN}) \left(\sqrt{{I_L}^2 \, {T_S}^2 + \frac{2\,{T_S}^2\,{V_{IN}}^2\,(C_{OUT}\,V_{r1} + D_1\,I_L\,T_S + I_L\,T_S)}{L\,(V_{OUT} - V_{IN})}} - I_L \, T_S \right) / (T_S \, V_{IN}) \, , (1 - V_{IN}/V_{OUT}) \right]$.

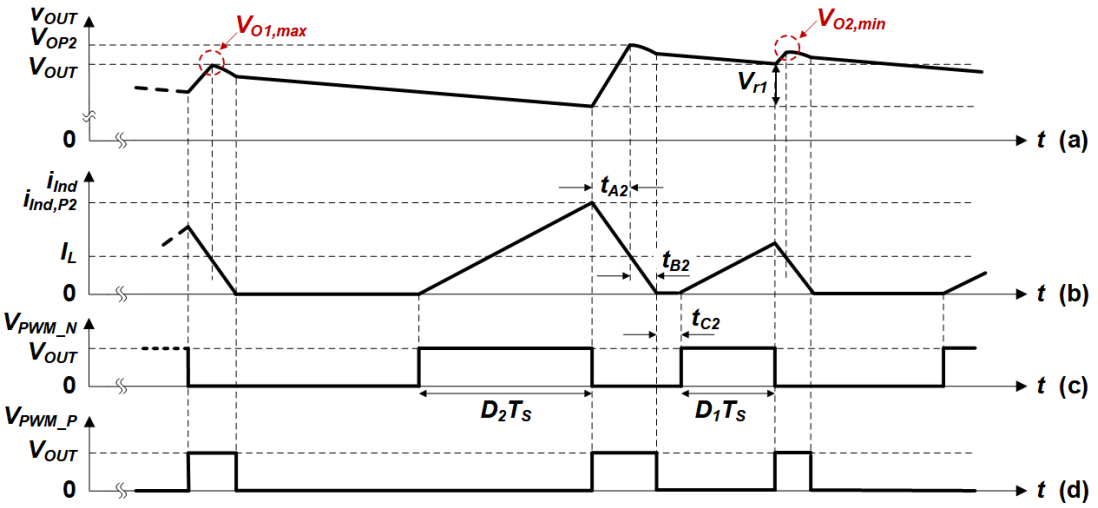

Figure 5.4 Waveforms at the steady state to determine V_{margin}. (a) Waveform of converter output v_{OUT}. (b) Waveform of inductor current i_{Ind}. (c) Waveform of control signals for M_N. (d) Waveform of control signals for M_P.

Thus, V_{margin} is chosen near the maximum of D_2 to leverage on the largest dipping compensation attainable. Further, the output ripple V_r can be estimated from (5.3) and (5.5) as

$$V_r = V_{OP2} - V_{OUT} + nV_{r1} = \frac{\left[\frac{(R_9 + R_{10}) T_S V_{IN}}{V_{Tm} R_9} \sqrt{R_{S\_SRVM} I_L + V_{margin}} - I_L L \right]^2}{2 C_{OUT} L (V_{OUT} - V_{IN})}. \tag{5.9}$$

The transient detection logics are designed to respond one T_S slower than the loop to avoid fs being varied in case of early activation. As for undershoot transient recovery by referring to Figure 5.2, the v_{OUT} jump, ΔV_{O_BCM}, within each cycle can be approximated by combing (5.5) and (5.6),

$$\Delta V_{O\_BCM} = \Delta V_{O,up} - \Delta V_{O,down} = \frac{(I_{Ind,max} - I_L - \Delta I) t_{A\_BCM} - (3 t_{B\_BCM} + 2 t_{D\_BCM})(I_L + \Delta I)}{2 C_{OUT}}, \tag{5.10}$$

where $t_{A\_BCM} = \frac{(I_{Ind,max} - I_L - \Delta I) L}{V_{OUT} - V_{IN}}$, $t_{B\_BCM} = \frac{(I_L + \Delta I) L}{V_{OUT} - V_{IN}}$, $t_{D\_BCM} = \frac{I_{Ind,max} L}{V_{IN}}$. By denoting

$t_{US,fall}$ as the duration when v_{OUT} falls and $t_{US,rise}$ when v_{OUT} rises, the undershoot recovery time t_{US} can be estimated as

$$t_{US} = t_{US,fall} + t_{US,rise} = (n+1)\left(1 + \frac{V_{r1}}{\Delta V_{O\_BCM}}\right) T_S \quad \textbf{(5.11)}$$

Similarly, upon detection of step-down load transients, both M_N and M_P will be turned off till v_{OUT} is pulled back down to V_{OUT}. The overshoot recovery time t_{OS} can be estimated as

$$t_{OS} = t_{OS,rise} + t_{OS,fall} = (n+1)(T_S + \frac{V_{r1}}{I_L - \Delta I}) \quad \textbf{(5.12)}$$

The maximum undershoot and overshoot ripples both equal $(n + 1)V_{r1}$.

5.1.3 Decision on Key Parameters

According to [92], boundary conditions between CCM and DCM modulation dictates that

$$I_{OB} = \frac{V_{OUT} D_{CCM} (1 - D_{CCM})^2}{2 f_S L}, \quad \textbf{(5.13)}$$

where I_{OB} is the inductor current at the CCM and DCM boundary; D_{CCM} is the duty ratio for CCM modulation by assuming $M_{V\_DC} = \frac{V_{OUT}}{V_{IN}} = \frac{1}{1 - D_{CCM}}$. Thus, substitute V_{OUT} and V_{IN}; it can be obtained that D_{CCM} = 0.7.

5.1.3.1 Switching Frequency f_S and Inductor-related Parameters

To ensure DCM modulation, it requires that $I_{OB} > I_{L,max}$. Hence, from Equation (5.13), it can be derived that $f_S L < 2.36\ \mathrm{Hz} \cdot \mathrm{H}$. In this work, $f_S L = 1\ \mathrm{Hz} \cdot \mathrm{H}$ is chosen. By considering the size constraint of a WSN sensor node, a small L is obviously beneficial as it is easier to be accommodated into the node than a large one.

However, it is unrealistic to reduce L indefinitely as it will result in a high switching frequency $f_S = 1/L$. This is due to the consideration that $t_{ON} = D/f_S$, where D is the duty ratio of DCM modulation at steady state. Note that t_{ON} is the on-time of M_N and it is limited by hardware configurations, such as rise and fall time of the gate drive signals at M_N and M_P, comparator delay in the ramp

generator and so on. And, with reference to Equation (5.1), t_{ON} cannot be reduced indefinitely with an increasing f_S. Therefore, f_S cannot be too high. In this work, f_S = 1 MHz is chosen with L = 1 µH.

Other parameters to consider when selecting the inductor involve DC resistance (DCR), Self-Resonant Frequency (SRF), saturation current, and Electro-Magnetic Interference (EMI). DC resistance measures the wire resistance of an inductor and contributes to the conduction loss. Lower DCR typically means larger wire and overall inductor size: it's a trade-off among power efficiency, allowed voltage drop and size. [96]

SRF refers to the natural resonant frequency of the parallel resonant tank formed by the inductor and distributed capacitances, C_w, associated to the inductor winding. Mathematically, $\mathrm{SRF} = 1/(2\pi\sqrt{LC_w})$. It is preferable to have an SRF much higher than f_S, such as being 10 times of f_S. [96]

Saturation current is the amount of current flowing through an inductor that causes the inductance to drop due to core saturation. Typically, it is desirable to operate with current peaks near the saturation rating. Thus, it allows the smallest possible inductor to be chosen. [96] In this work, the steady-state peak inductor current, $I_{Ind,P}$, can be calculated as $I_{Ind,P} = V_{IN}D_{max}/(f_S L) \approx 410\ \mathrm{mA}$ [92, 97], where $D_{max} \approx 45.5\%$ according to Equation (5.1) at $I_{L,max} = 40\ \mathrm{mA}$. The maximum inductor current during start-up and undershoot transient recovery is set to be around 600 mA. Thus, an inductor with a saturation current that is larger than 600 mA should be chosen.

Any inductor can be a potential source of radiation. EMI radiated from the inductor can pose additional noise to sensitivity loads in the WSN sensor node. In detail, ADCs and RF transceivers are the key loading ICs that is noise-sensitive. Thus, to suppress EMI, it would be preferable to use the inductor with a toroidal core and a distributed gap, such as the Murata Power Solutions' 3200 series recommended in [98].

5.1.3.2 Output Capacitance C_{OUT} and ESR

Derivation of C_{OUT} and its ESR is based on the output ripple, V_r. Mathematically, V_r can be expressed as $V_r = V_{Cpp} + V_{rcpp}$ [92], where V_{Cpp} denotes the portion of V_r contributed by C_{OUT} itself while V_{rcpp} denotes the portion contributed by the ESR of the output capacitor. Following [91], this work assumes that $V_{Cpp} = 20\% \cdot V_r$. Thus,

$$V_{Cpp} = 0.2V_r = \frac{V_{OUT}D_{max}}{f_S R_{L,min} C_{OUT,min}}, \tag{5.14}$$

where $R_{L,min} = \frac{V_{OUT}}{I_{L,max}}$. In this manner, by assuming that V_r = 10 mV, the minimum C_{OUT} required can be derived as

$$C_{OUT,min} = \frac{5V_{OUT}D_{max}}{f_S R_{L,min} V_r} \approx 9.11\ \mu\text{F} \tag{5.15}$$

Therefore, this work chooses a 10-µF output capacitor.

Moreover, the ESR of the output capacitor can be derived based on Equation (5.16) by Equation (5.17)

$$V_{rcpp} = 0.8V_r = \text{ESR} \cdot \frac{I_{L,max}}{1-D_{max}}. \tag{5.16}$$

$$\text{ESR} = \frac{0.8V_r(1 - D_{max})}{I_{L,max}} \approx 19.5\ \text{m}\Omega \tag{5.17}$$

5.1.4 Proposed Signal-boosting Gate Drive Circuit

To minimize conduction losses, voltage magnitudes of gate driving signals for MOSFET switches should be as large as affordable for their triode-mode operations. Thus, a novel signal boosted is proposed in Figure 5.5.

Take M_N for an instance. Upon logic '1' at $V_{PWM\_N\_VI}$, which equals V_{IN} as the control logics are powered from the input, charge sharing occurs between $V_{PWM\_N\_VI}$ and V_{PWM_N} though M_{NS5} to raise V_{PWMN_N} to V_{IN} first. As V_{PWM_N} ramps up to V_I, the gate of M_{NS2} is charged up through buffer BF_2 to turn on M_{NS2}. Consequently, through the current mirror M_{PS1} and M_{PS2}, $V_{PWM\_N\_M}$ are charged

up by v_{OUT}. Meanwhile, M_{NS1} is switched off to direct current through M_{PS2} and M_{NS4} to charge up V_{PWM_N} to v_{OUT}. Upon logic '0' at $V_{PWM\_N\_VI}$, M_{NS3} is turned on through inverter IN_2 to discharge V_{PWM_N} and $V_{PWM\_N\_M}$ and prepare the circuit for the next cycle of charging actions.

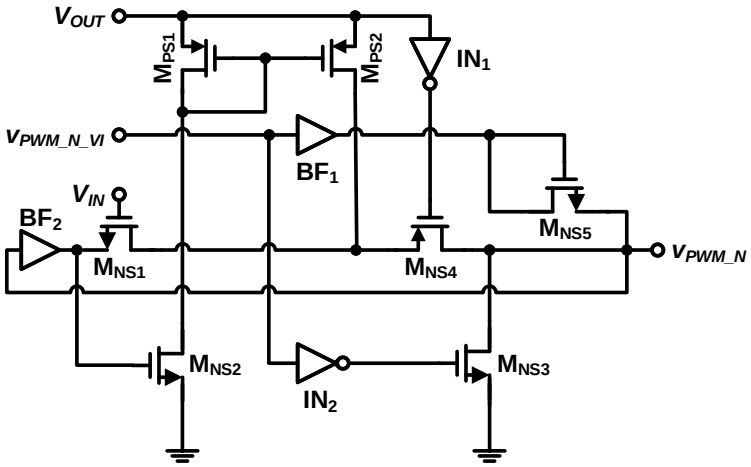

Figure 5.5 Circuit diagram of the proposed signal-boosting gate drive circuit.

5.2 Small-signal Model of the Proposed SRVM Controller

A small signal diagram [94] of the proposed PWM DCM boost converter is displayed in Figure 5.6. The loop gain of the converter is obtained as

$$T(s) = \frac{v_f(s)}{v_e(s)} = T_{mp}(s)\beta T_{comp}(s)T_{opsum\_cl}(s)T_{sr}(s)T_{opm\_cl}(s) \quad \textbf{(5.18)}$$

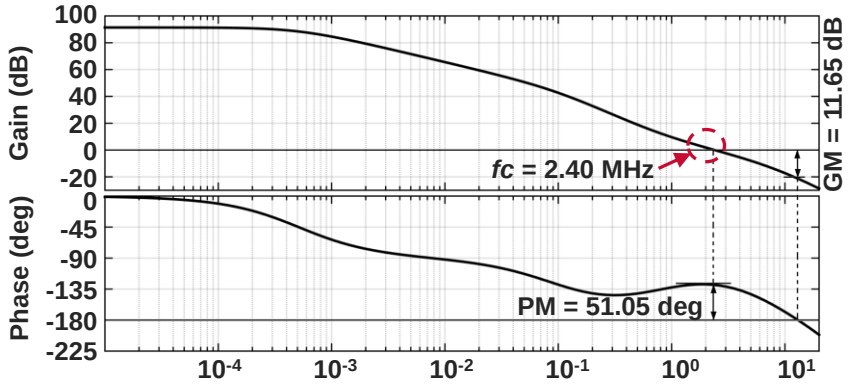

Figure 5.6 Bode plot of loop gain *T*(*s*) of the proposed boost converter.

The results are summarized in TABLE 5.1. Frequency responses are evaluated in Figure 5.7.

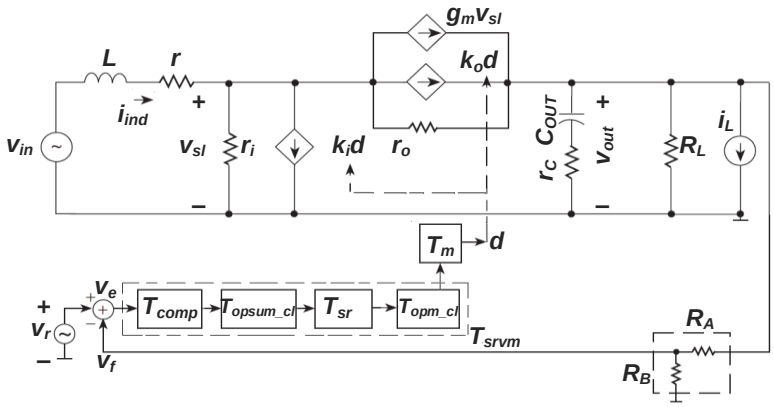

Figure 5.7 Small-signal diagram of the proposed boost converter.

TABLE 5.1 TRANSFER FUNCTIONS, ZEROS AND POLES OF THE CONVERTER

Description	Transfer Function	Zeros and Poles
$\frac{v_o(s)}{v_c(s)}$	$T_{mp}(s) = \frac{V_I}{V_{Tm}}\left(\frac{2}{2M_{V\_DC}-1}\right)\sqrt{\frac{M_{V\_DC}(M_{V\_DC}-1)R_L}{2Lf_s}}\left(\frac{1+\frac{s}{\omega_{z1}}}{1+\frac{s}{\omega_{p1}}}\right)$ [92, 99]	$\omega_{z1} = \frac{1}{r_C C}$ $\omega_{p1} = \frac{2M_{V\_DC}-1}{M_{V\_DC}-1}(\frac{1}{R_L C})$
$\frac{v_{srvm\_s}(s)}{v_e(s)}$	$T_{comp}(s) = V_{margin}\frac{T_c(0)}{1+\frac{s}{\omega_c}}$ [94]	ω_c: -3dB pole of CP_{OS}
$\frac{v_{sr\_i}(s)}{v_{srvm\_s}(s)}$	$T_{opsum\_cl}(s) = \frac{2}{1+\frac{s}{2T_{opsum}(0)\omega_{opsum}}}$	$\omega_{opsum\_cl} = 2T_{opsum}(0)\omega_{opsum}$
$\frac{v_{sr\_o}(s)}{v_{sr\_i}(s)}$	$T_{sr} \approx T_{opsr}(s) = \frac{T_{opsr}(0)}{1+\frac{s}{\omega_{opsr}}}$	ω_{opsr}: -3dB pole of OP_{SR}
$\frac{v_c(s)}{v_{sr\_o}(s)}$	$T_{opm\_cl}(s) = \frac{\frac{R_9+R_{10}}{R_9}}{1+\frac{s}{\frac{R_9+R_{10}}{R_9}T_{opm}(0)\omega_{opm}}}$	$\omega_{opm\_cl} = \frac{(R_9+R_{10})}{R_9}T_{opm}(0)\omega_{opm}$

As additional the transient recovery logics are implemented in this work, load transient responses are not limited by the PM in Figure 5.7 and the converter is stable at the steady state.

5.3 Simulation Results and Discussions

Due to time constraints, the concept of the proposed boost converter is only simulated without silicon results. This section lists key performances of the proposed control techniques based on simulation results in MATLAB.

5.3.1 Proposed Start-up Control

Performances of the start-up control is presented in Figure 5.8. After a brief charge sharing between the converter input and output initially, i_{lnd} conducts in

peak-current BCM mode till V_{OUT} is reached, fulfilling the objectives of the proposed design.

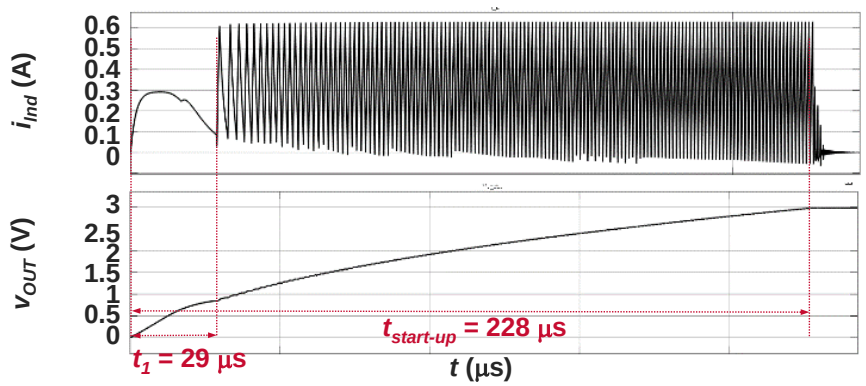

Figure 5.8 Simulated Waveform of i_{Ind} from start-up to steady state.

5.3.2 Proposed SRVM Controller

As shown in Figure 5.9, under the control of proposed SRVM technique, V_r at I_L = 40 mA is 12.5 mV, which is 0.42% of the nominal V_{OUT}. In the lower section of Figure 5.9, the solid line represents the boosted V_{PWM_N} control signal, the dashed line for EA output v_C, and the dotted line for the saw-tooth waveform.

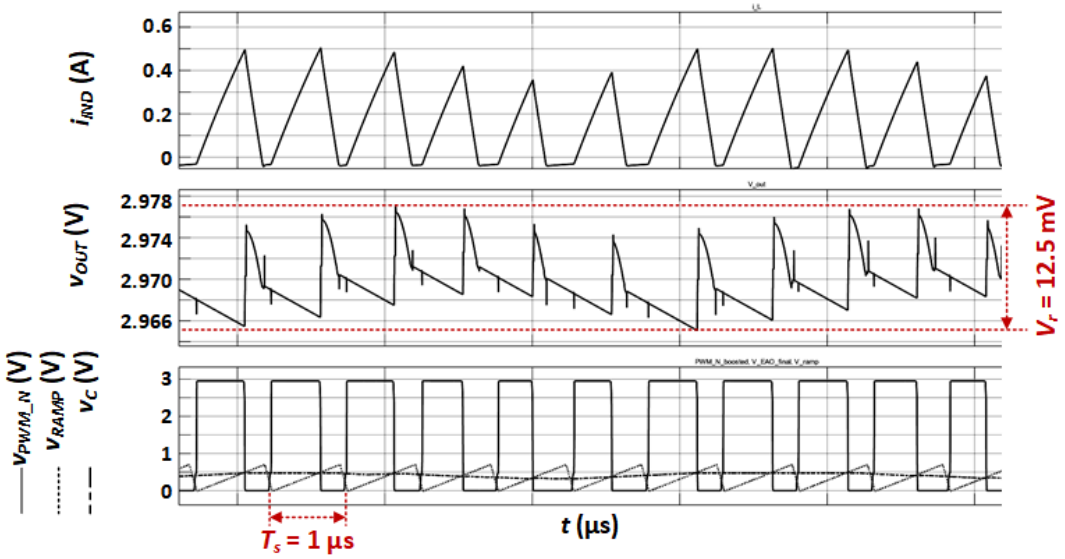

Figure 5.9 Simulated waveform of SRVM control at steady state.

Upon step-up and step-down load transients, the converter experiences 10.8 mV undershoot with recovery of 8.9 µs and 3.0 mV overshoot with a

recovery of 4 µs according to Figure 5.10.

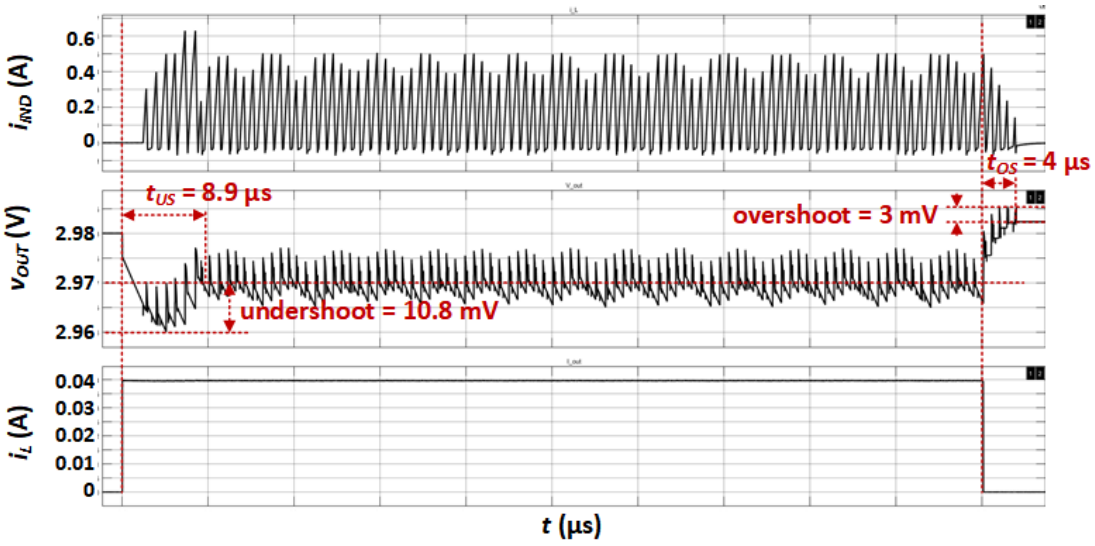

Figure 5.10 Simulated waveform of load transient response.

Hence, the transient recovery circuits are efficacious to boost the transient responses despite a relatively low PM at the steady state. Performance comparisons of the proposed SVRM controller against previous works are shown in TABLE 5.2.

TABLE 5.2 PERFORMANCE COMPARISON

	Proposed SRVM [a]	**ΣΔ [68]** [b]	**WTE [69]** [c]
f_s (MHz)	1	0.6	2
Control Mode	DCM	DCM	CCM
Output Ripple (%)	0.42	1.7	2.0
T_{OS} (µs)	4.0	400	120
Overshoot (mV)	3.0	230	54
T_{US} (µs)	8.9	50	≈ 7
Undershoot (mV)	10.8	292	90

a. Load transients: I_O switch between 0 and 40 mA in 100 ns.
b. Load transients: I_O switch between 0.1 and 1 A in 4 µs.
c. Load transients: I_O switch between 0 and 400 mA in 1 µs.

5.3.3 Proposed Signal-boosting Gate Drive Circuit

Performances of the signal boosting is displayed in Fig. 8(d) on the driving signal at the gate of M_N. The actual driving signal V_{PWM_N} traces closely with v_{OUT} during start-up as well as at the steady state.

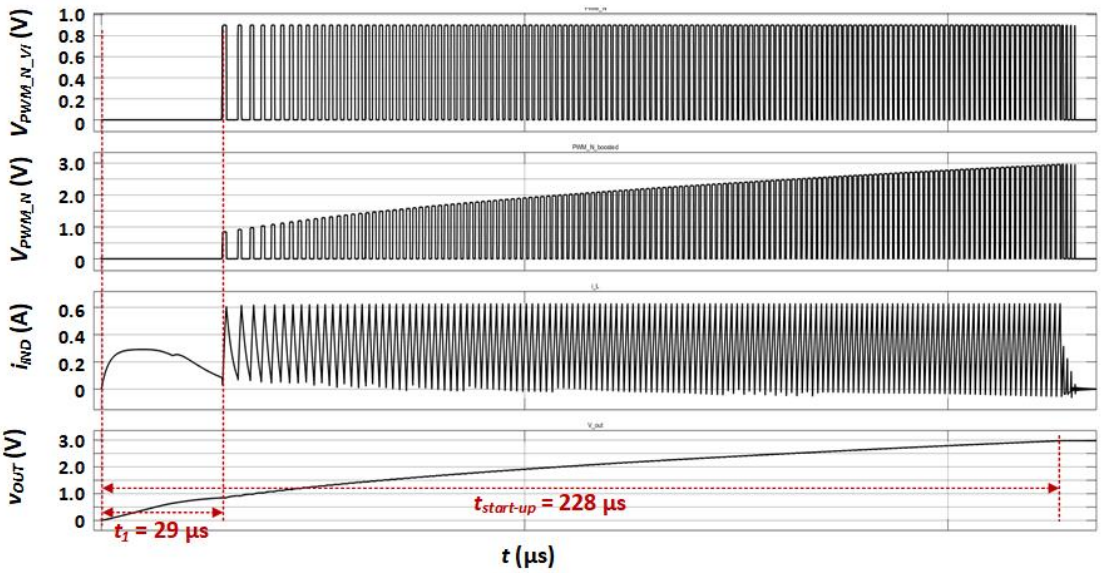

Figure 5.11 Simulated waveform of boosted PWM control signal V_{PWM_N} for M_N.

5.4 Concluding Remarks

In the effort to address the output ripples and load transient responses of boost converters in WPT PMUs for WSN, this work proposes a novel PWM DCM control to evade negative effects of the RHP zero. The proposed control approach 1) enhances steady-state and transient responses with the proposed SRVM controller, 2) ensures low conduction losses with the proposed signal booster, 3) and saves chip area with the dual-purpose start-up controller and analogue-processing-based control technique.

Chapter 6 Conclusions and Recommendations

To deploy WSN sensor nodes in a large volume and materialize the concept of IoT, various enabling energy-sources have been investigated. However, only limited options are adoptable due to cost and node-size constraints. WPT-powered solutions leverage on the advantages of both energy-storages in its controllability and energy-scavengers in its cost-saving features. Meanwhile, they avoid the drawbacks, such as frequent maintenance and unpredictability, of both. In this manner, WPT technologies, such as Omnidirectional EM-Radiation, emerge as a feasible approach to source energy to WSN sensor nodes.

As part of the effort to implement the WPT approach, a dedicated PMU has to be developed. Subsequently, all of key IC components, namely, VRs, LDOs and DC-DC converters, within such a PMU have to be investigated to identify design challenges from the perspective of IC design. Such is the scope of the work presented in this thesis.

6.1 Conclusion

In this work, concepts of a VR, an OCL-LDO and a boost DC-DC converter dedicated to WPT-powered WSN sensor nodes are developed. A BVR-like CMOS VR is designed to address the PVT-invariance. To address process variations, trimming networks on key resistive components within the VR are developed and proposed. Curvature-compensation circuits are also introduced to address supply variations from sub-1 V to 1.5 V. To improve its TC, the mathematical model of such topology is further explored to identify higher-order non-idealities such as the V_{DS} component of the normal-V_{th} NMOS in deriving the temperature-invariant V_{REF}. In comparison with its precedent counterpart [52], TC of the proposed VR improves by more than 5.5 times with a slightly-narrower operating temperature range. The proposed CMOS VR effectively addresses the unique requirements on a WPT-powered PMU, such as supply-independency, sub-1-V operations and high PSR.

Moreover, an OCL-LDO is also proposed to tackle the trade-off among its output accuracy, frequency stability and fast-settling transient responses due to the current-efficient PPF structure incorporated into the G_m-cell-based EA. In doing so, a process-robust LAC is developed. The proposed LAC effectively addresses the aforementioned trade-off. The resulted OCL-LDO offers superior overall performances among relevant previous works in terms of current-efficiency, speed, accuracy, loading capability and PSR as shown in TABLE 4.1. It renders as the best candidate to exist within a WPT-powered PMU for a WSN sensor node.

Furthermore, this work also promotes the concept of a compensator-less boost converter. Similar to the proposed OCL-LDO, such concept on the boost converter emphasizes the load-transient performances as well due to the DPM scheme, which is often implemented by the µP within the sensor node to conserve power. To boost the load-transient responses, the proposed boost converter adopts the rationale of accelerating V_{EA} response upon load transients as introduced by previous works. Upon steady state, the proposed design minimizes the output ripples which are left unaddressed in its previous counterparts. To do so, a compensator-less SRVM controller is introduced and developed. The resulted boost converter not only exhibits fast transient responses, small output ripples when sourcing loaded ICs, it also saves the node size of a WSN sensor by eliminating space-consuming discrete components that build the compensator in conventional designs.

By referring back to the WSN sensor node block diagram in Figure 1.2, the proposed VR, LDO and DC-DC are examined based on the two configurations, such as the battery-equipped and battery-less. By considering the high PSR at low frequencies and good LS, the proposed VR and LDO can be implemented into both configurations directly as illustrated in Figure 1.2. The feasible supply range of them allows variation from 0.8 V to 1.5 V, be the supply from the rectifier-output or the battery-output.

In addition, to fit the proposed DC-DC into the WSN sensor node, a few precautions are noteworthy. Firstly, to fit it into the battery-less WSN sensor node, DPM needs to be implemented in a manner to ensure that the total load

current to the rectifier output renders $Z_{L\_rec,OP}$ following Equation (2.12). This is to maximize $\eta_{RF\text{-}DC}$, the power conversion efficiency of the rectifier. It can be done by turn on or off certain load components selectively upon various node operations. Secondly, the proposed DC-DC structure can be adopted in the battery-equipped configuration as well. However, to maximize the charging efficiency of the secondary battery in the WSN sensor node, charging circuitries have to be added upon the proposed DC-DC structure. In reality, to achieve an optimal power efficiency under the battery-equipped configuration, the charging efficiency and $\eta_{RF\text{-}DC}$ may have to be considered together as maximizing one might trade-off the other. Thus, a compromise between the two efficiencies might be inevitable.

Therefore, by comparing the two configurations for a WPT-enabled WSN sensor node in Figure 1.2, the proposed VR, LDO and DC-DC fit better into the battery-less configuration. Nevertheless, power management is never sufficient from the hardware perspective alone. Effective DPM from the system level is also necessary to ensure an optimal power efficiency for a WSN sensor node.

6.2 Recommendations for Future Research

Future works from various perspectives can be derived based on current research efforts. To develop a full-CMOS VR, the resistive components within the proposed CMOS VR can be replaced with their active CMOS counterparts. Moreover, trimming networks can be further digitized to allow automatic trimming by involving the µPs within WSN sensor node. Furthermore, continual efforts can be dedicated on the BVR-like CMOS-VR structure in adapting curvature-compensation techniques previously developed for BVRs into the CMOS VR to better the TC. For the same purpose, a low-voltage high-gain EA can be developed as well.

With the process-tracking LAC clearing the obstacle to implement PPF in the proposed OCL-LDO, further efforts can be spent in raising the current efficiency by developing more current-saving VR adaptors and PTCS as well.

Lastly, the concept of the proposed boost converter should be implemented whenever opportunities allow. Nonetheless, several key

components that build the boost converter may have to be investigated and developed first, such as the fast response comparator that drives the control signal for the high-side main switch and the high-side current-sensor to feed the proposed SRVM controller. In addition, it will also be helpful to address the input variations to the boost converter while ensuring a good line-regulation.

Glossary of Abbreviated Terms

- AC: Alternating Current
- ACC: Adaptive Capacitor Control
- ADC: Analog-to-Digital Converter
- BCM: Boundary Conduction Mode
- BF: Buffer
- BG: Bandgap
- BJT: Bipolar Junction Transistor
- BR: Bias Reference
- BVR: Bandgap Voltage Reference
- BW: Bandwidth
- CCM: Continuous Conduction Mode
- CL: Closed-Loop
- CM: Current Mirror
- CMOS: Complementary Metal Oxide Semiconductor
- COTS: Commercial-Off-The-Shelf
- COMP, CP: Comparator
- DC: Direct Current
- DCM: Discontinuous Conduction Mode
- DFC: Damping Factor Control
- DO: Drop-Out
- DPM: Dynamic Power Management
- DS: Drain-Source
- DTMOS: Dynamic Threshold-voltage MOSFET
- DVS: Dynamic Voltage Scaling
- EA: Error Amplifier
- EIRP: Effective Isotropic Radiated Power
- EM: Electro-Magnetic
- EN, ENB: Enable
- ERC: European Radio-communications Commission
- ESR: Equivalent Series Resistance
- FB: Feedback

- FCC: Federal Communication Commission
- FF: Fast NMOS and Fast PMOS (Process Corner)
- FOM: Figure Of Merit
- FS: Fast NMOS and Slow PMOS (Process Corner)
- FTS: Feedforward Transconductance Stage
- FVF: Flipped Voltage Follower
- FW: Free Wheeling
- GB: Gigabyte
- GM: Gain Margin
- GS: Gate-Source
- HF: High Frequency
- HYS: Hysteresis
- IC: Integrated Circuit
- ICNIRP: International Commission on Non-Ionizing Radiation Protection
- ISM: Industrial, Scientific, Medical
- KCL: Kirchhoff Current Law
- LAC: Load Adaptive Controller
- LDO, LDR: Low Drop-Out Voltage Regulator
- LF: Low Frequency
- LHP: Left Hand Plane
- LS: Line Sensitivity
- MB: Megabyte
- MHCC: Modified Hysteretic Current Control
- MIMO: Multiple Inputs and Multiple Output
- MOSFET, MOS: Metal Oxide Semiconductor Field Effect Transistor
- MSA: Micro-Strip Antenna
- MUX: Multiplexer
- NMC: Nested Miller Compensation
- NMCF: NMC with Feedforward Transconductance Stage
- NMCNR: NMC with Null Resistor
- NMCNRF: NMCNR with the Feedforward Transconductance Stage
- NMOS: N-type MOSFET

- NPN: Negative-Positive-Negative type (BJT)
- OCD: Over Current Detector
- OCL: Output Capacitor-Less
- OP: Operational Amplifier
- OS: Overshoot
- OSS: Overshoot Suppression
- OTA: Operational Transconductance Amplifier
- PCB: Printed Circuit Board
- PI: Proportional and Integral (compensation)
- PK: Peak
- PM: Phase Margin
- PMOS: P-type MOSFET
- PMU: Power Management Unit
- PNP: Positive-Negative-Positive (BJT)
- PPF: Partial Positive Feedback
- PSR: Power Supply Rejection
- PSRR: Power Supply Rejection Ratio
- PTCS: Process Tracking Current Source
- PVT: Process-V_{DD}-Temperature
- PWM: Pulse Width Modulation
- REF: Reference
- RF: Radio Frequency
- RHP: Right Hand Plane
- RX: Receiving (Antenna)
- SAR: Successive Approximation Register (ADC)
- SC: Switched Capacitor
- SD: Source-Drain
- SDR: Source Degenerating Resistance
- SF: Slow NMOS and Fast PMOS (Process Corner)
- SG: Source-Gate
- SRVM: Square-Root Voltage Mode
- SS: Slow NMOS and Slow PMOS (Process Corner)

- SW: Switch
- TC: Temperature Coefficient
- TX: Transmitting (Antenna)
- TYP: Typical (Process Corner)
- ULP: Ultra Low Power
- US: Undershoot
- UVLO: Under Voltage-Lock Out
- VR: Voltage Reference
- WPT: Wireless Power Transfer
- WSN: Wireless Sensor Network
- WTE: Window Transient Enhancement
- ZCD: Zero Current Detector

Author's Publications

Journal papers:

[1] H. Luo, and L. Siek, "A 0.8-V Output-Capacitor-less Low Dropout Voltage Regulator Based on Load-Adaptive Negative-Resistance", *IEEE J. Solid-State Circuits*, 2020 (to be submitted)

[2] H. Luo, and L. Siek, "A 0.7-V Supply-insensitive ΔV_{th}-based CMOS Voltage Reference with Proposed Trimming and Curvature-Compensation Techniques", *IEEE J. Solid-State Circuits*, 2019 (submitted)

Conference papers:

[1] H. Luo and L. Siek, "An output-capacitor-less low-dropout voltage regulator with high power supply rejection ratio and fast load transient response using boosted-input-transconductance structure," *IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, 2015

[2] H. Luo and L. Siek, "A 0.9-V input PWM DCM boost converter with low output ripples and fast load transient response based on a novel square-root voltage mode (SRVM) control approach," *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2017

Bibliography

[1] K. Ashton, “That ‘internet of things’ thing,” *RFID journal,* vol. 22, no. 7, pp. 97-114, 2009.

[2] S. H. Yang, *Wireless Sensor Networks: Principles, Design and Applications*: Springer London, 2013.

[3] L. Atzori, A. Iera, and G. Morabito, “The internet of things: A survey,” *Computer networks,* vol. 54, no. 15, pp. 2787-2805, 2010.

[4] E. Fleisch, “What is the internet of things? An economic perspective,” *Economics, Management & Financial Markets,* vol. 5, no. 2, 2010.

[5] N. Gershenfeld, R. Krikorian, and D. Cohen, “The internet of things,” *Scientific American,* vol. 291, no. 4, pp. 76-81, 2004.

[6] O. Vermesan, P. Friess, P. Guillemin, S. Gusmeroli, H. Sundmaeker, A. Bassi, I. S. Jubert, M. Mazura, M. Harrison, and M. Eisenhauer, “Internet of things strategic research roadmap,” *Internet of Things-Global Technological and Societal Trends,* vol. 1, no. 2011, pp. 9-52, 2011.

[7] A. Moschitta, and I. Neri, "Power consumption assessment in wireless sensor networks," *ICT-energy-concepts towards zero-power information and communication technology*: InTech, 2014.

[8] C. Buratti, A. Conti, D. Dardari, and R. Verdone, “An overview on wireless sensor networks technology and evolution,” *Sensors,* vol. 9, no. 9, pp. 6869-6896, 2009.

[9] J. Lu, H. Okada, T. Itoh, T. Harada, and R. Maeda, “Toward the world smallest wireless sensor nodes with ultralow power consumption,” *IEEE Sensors Journal,* vol. 14, no. 6, pp. 2035-2041, 2014.

[10] S. Roundy, P. K. Wright, and J. M. Rabaey, *Energy Scavenging for Wireless Sensor Networks: With Special Focus on Vibrations*: Springer US, 2004.

[11] M. T. Penella-López, and M. Gasulla-Forner, *Powering Autonomous Sensors: An Integral Approach with Focus on Solar and RF Energy Harvesting*: Springer Netherlands, 2011.

[12] F. I. Simjee, and P. H. Chou, “Efficient charging of supercapacitors for extended lifetime of wireless sensor nodes,” *IEEE Transactions on power electronics,* vol. 23, no. 3, pp. 1526-1536, 2008.

[13] H. J. Visser, and R. J. M. Vullers, “RF Energy Harvesting and Transport for Wireless Sensor Network Applications: Principles and Requirements,” *Proceedings of the IEEE,* vol. 101, no. 6, pp. 1410-1423, 2013.

[14] S. Shreck, and S. Latifi, "Wireless Power Transmission." p. 1.

[15] L. Xie, Y. Shi, Y. T. Hou, and A. Lou, “Wireless power transfer and applications to sensor networks,” *IEEE Wireless Communications,* vol. 20, no. 4, pp. 140-145, 2013.

[16] B. Strassner, and K. Chang, “Microwave power transmission: Historical milestones and system components,” *Proceedings of the IEEE,* vol. 101, no. 6, pp. 1379-1396, 2013.

[17] G. Barrenetxea, F. Ingelrest, G. Schaefer, and M. Vetterli, "Wireless sensor networks for environmental monitoring: The sensorscope experience." pp. 98-101.

[18] A. Sinha, and A. Chandrakasan, “Dynamic power management in wireless sensor networks,” *IEEE Design & Test of Computers,* vol. 18, no. 2, pp. 62-74, 2001.
[19] V. Raghunathan, C. Schurgers, S. Park, and M. B. Srivastava, “Energy-aware wireless microsensor networks,” *IEEE Signal processing magazine,* vol. 19, no. 2, pp. 40-50, 2002.
[20] A. Chandrakasan, R. Amirtharajah, S. Cho, J. Goodman, G. Konduri, J. Kulik, W. Rabiner, and A. Wang, "Design considerations for distributed microsensor systems." pp. 279-286.
[21] D. Estrin, R. Govindan, J. Heidemann, and S. Kumar, "Next century challenges: Scalable coordination in sensor networks." pp. 263-270.
[22] J. M. Rabaey, M. J. Ammer, J. L. Da Silva, D. Patel, and S. Roundy, “PicoRadio supports ad hoc ultra-low power wireless networking,” *Computer,* vol. 33, no. 7, pp. 42-48, 2000.
[23] M. Gupta, and U. Singh, “A new flipped voltage follower with enhanced bandwidth and low output impedance,” *Analog Integrated Circuits and Signal Processing,* vol. 72, no. 1, pp. 279-288, 2012.
[24] K. Mikhaylov, and J. Tervonen, "Optimization of microcontroller hardware parameters for wireless sensor network node power consumption and lifetime improvement." pp. 1150-1156.
[25] P. P. Mercier, and A. P. Chandrakasan, *Ultra-low-power Short-range Radios*: Springer, 2015.
[26] P. M. Nadeau, A. Paidimarri, P. P. Mercier, and A. P. Chandrakasan, “Multi-channel 180pJ/b 2.4 GHz FBAR-based receiver,” 2012.
[27] A. Paidimarri, P. M. Nadeau, P. P. Mercier, and A. P. Chandrakasan, “A 2.4 GHz multi-channel FBAR-based transmitter with an integrated pulse-shaping power amplifier,” *IEEE Journal of Solid-State Circuits,* vol. 48, no. 4, pp. 1042-1054, 2013.
[28] A. Shirane, Y. Fang, H. Tan, T. Ibe, H. Ito, N. Ishihara, and K. Masu, “RF-powered transceiver with an energy-and spectral-efficient IF-based quadrature backscattering transmitter,” *IEEE J. Solid-State Circuits,* vol. 50, no. 12, pp. 2975-2987, 2015.
[29] Y. Zhang, R. Zhou, W. Rhee, and Z. Wang, "A 6.1 mW 5Mb/s 2.4 GHz transceiver with F-OOK modulation for high bandwidth and energy efficiencies." pp. 1-4.
[30] F. Kocer, and M. P. Flynn, “An RF-powered, wireless CMOS temperature sensor,” *IEEE Sensors journal,* vol. 6, no. 3, pp. 557-564, 2006.
[31] M. E. Sinangil, M. Yip, M. Qazi, R. Rithe, J. Kwong, and A. P. Chandrakasan, “Design of low-voltage digital building blocks and ADCs for energy-efficient systems,” *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 59, no. 9, pp. 533-537, 2012.
[32] J. Shen, and P. R. Kinget, “A 0.5-V 8-bit 10-Ms/s pipelined ADC in 90-nm CMOS,” *IEEE journal of solid-state circuits,* vol. 43, no. 4, pp. 787-795, 2008.
[33] S. Lee, A. P. Chandrakasan, and H.-S. Lee, “A 12 b 5-to-50 MS/s 0.5-to-1 V voltage scalable zero-crossing based pipelined ADC,” *IEEE Journal of Solid-State Circuits,* vol. 47, no. 7, pp. 1603-1614, 2012.
[34] K. Yoshioka, A. Shikata, R. Sekimoto, T. Kuroda, and H. Ishikuro, “An 8 bit 0.3–0.8 V 0.2–40 MS/s 2-bit/Step SAR ADC with successively activated threshold configuring comparators in 40 nm CMOS,” *IEEE*

Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, no. 2, pp. 356-368, 2015.

[35] W. Kim, H.-K. Hong, Y.-J. Roh, H.-W. Kang, S.-I. Hwang, D.-S. Jo, D.-J. Chang, M.-J. Seo, and S.-T. Ryu, “A 0.6 V 12 b 10 MS/s low-noise asynchronous SAR-assisted time-interleaved SAR (SATI-SAR) ADC,” *IEEE Journal of Solid-State Circuits,* vol. 51, no. 8, pp. 1826-1839, 2016.

[36] L. Chen, X. Tang, A. Sanyal, Y. Yoon, J. Cong, and N. Sun, “A 0.7-V 0.6-uW 100-kS/s Low-Power SAR ADC With Statistical Estimation-Based Noise Reduction,” *IEEE Journal of Solid-State Circuits,* vol. 52, no. 5, pp. 1388-1398, 2017.

[37] Y. Huang, and K. Boyle, *Antennas: from theory to practice*: John Wiley & Sons, 2008.

[38] A. Dolgov, R. Zane, and Z. Popovic, “Power management system for online low power RF energy harvesting optimization,” *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 57, no. 7, pp. 1802-1811, 2010.

[39] G. Rincon-Mora, *Analog IC design with low-dropout regulators (LDOs)*: McGraw-Hill, Inc., 2009.

[40] L. B. Hoermann, P. M. Glatz, C. Steger, and R. Weiss, "Energy efficient supply of wsn nodes using component-aware dynamic voltage scaling." pp. 1-8.

[41] R. A. Bercich, D. R. Duffy, and P. P. Irazoqui, “Far-field RF powering of implantable devices: Safety considerations,” *IEEE Transactions on Biomedical Engineering,* vol. 60, no. 8, pp. 2107-2112, 2013.

[42] A. Amaravati, M. Dave, M. S. Baghini, and D. K. Sharma, “A fully on-chip pt-invariant transconductor,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 23, no. 9, pp. 1961-1964, 2015.

[43] D. Wang, X. L. Tan, and P. K. Chan, “A 65-nm CMOS constant current source with reduced PVT variation,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 25, no. 4, pp. 1373-1385, 2017.

[44] G. A. Rincon-Mora, *Voltage References: From Diodes to Precision High-Order Bandgap Circuits*: Wiley, 2002.

[45] B. Razavi, *Design of Analog CMOS Integrated Circuits*: McGraw-Hill, 2001.

[46] P. Malcovati, F. Maloberti, C. Fiocchi, and M. Pruzzi, “Curvature-compensated BiCMOS bandgap with 1-V supply voltage,” *IEEE Journal of Solid-State Circuits,* vol. 36, no. 7, pp. 1076-1081, 2001.

[47] A. S. Sedra, and K. C. Smith, *Microelectronic Circuits*: Oxford University Press, 2004.

[48] K. N. Leung, and P. K. T. Mok, “A sub-1-V 15-ppm/C CMOS bandgap voltage reference without requiring low threshold voltage device,” *IEEE Journal of Solid-State Circuits,* vol. 37, no. 4, pp. 526-530, 2002.

[49] G. De, and G. Iannaccone, “A Sub-1-V 10 ppm/° C nanopower voltage reference generator,” *Solid-State Circuits, IEEE Journal of,* vol. 42, no. 7, pp. 1536-1542, 2007.

[50] G. Vita, G. Iannaccone, and P. Andreani, "A 300 nW, 12 ppm/C Voltage Reference in a Digital 0.35 um CMOS Process." pp. 81-82.

[51] M. Seok, G. Kim, D. Blaauw, and D. Sylvester, “A portable 2-transistor picowatt temperature-compensated voltage reference operating at 0.5 V,” *IEEE Journal of Solid-State Circuits,* vol. 47, no. 10, pp. 2534-2545,

2012.
[52] M. Liu, K. Pelzers, R. van Dommele, A. van Roermund, and P. Harpe, “A106nW 10b 80 kS/s SAR ADC with duty-cycled reference generation in 65 nm CMOS,” *IEEE Journal of Solid-State Circuits,* vol. 51, no. 10, pp. 2435-2445, 2016.
[53] R. Castello, A. G. Grassi, and S. Donati, “A 500-nA sixth-order bandpass SC filter,” *IEEE Journal of Solid-State Circuits,* vol. 25, no. 3, pp. 669-676, 1990.
[54] R. Wang, and R. Harjani, "Partial positive feedback for gain enhancement of low-power CMOS OTAs," *Low-Voltage Low-Power Analog Integrated Circuits*, pp. 21-35: Springer, 1995.
[55] H. G. Li, H. X. Bai, S. G. Xie, and D. L. Su, “Bulk-driven CMOS amplifier with high EMI immunity,” *IEEE Transactions on Electromagnetic Compatibility,* vol. 57, no. 6, pp. 1425-1434, 2015.
[56] F. Khateb, and T. Kulej, “Design and implementation of a 0.3-V differential difference amplifier,” *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 66, no. 2, pp. 513-523, 2018.
[57] T. Y. Man, P. K. T. Mok, and M. Chan, “A High Slew-Rate Push–Pull Output Amplifier for Low-Quiescent Current Low-Dropout Regulators With Transient-Response Improvement,” *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 54, no. 9, pp. 755-759, 2007.
[58] X. Qu, Z.-K. Zhou, B. Zhang, and Z.-J. Li, “An ultralow-power fast-transient capacitor-free low-dropout regulator with assistant push–pull output stage,” *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 60, no. 2, pp. 96-100, 2013.
[59] R. G. Carvajal, J. Ramírez-Angulo, A. J. López-Martín, A. Torralba, J. A. G. Galán, A. Carlosena, and F. M. Chavero, “The flipped voltage follower: A useful cell for low-voltage low-power circuit design,” *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 52, no. 7, pp. 1276-1291, 2005.
[60] C. Desai, D. Mandal, B. Bakkaloglu, and S. Kiaei, “A 1.66 mV FOM output cap-less LDO with current-reused dynamic biasing and 20 ns settling time,” *IEEE Solid-State Circuits Letters,* vol. 1, no. 2, pp. 50-53, 2018.
[61] C. K. Chava, and J. Silva-Martinez, “A frequency compensation scheme for LDO voltage regulators,” *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 51, no. 6, pp. 1041-1050, 2004.
[62] S. K. Lau, K. N. Leung, and P. K. Mok, "Analysis of low-dropout regulator topologies for low-voltage regulation." pp. 379-382.
[63] K. N. Leung, P. K. Mok, and W. H. Ki, "A novel frequency compensation technique for low-voltage low-dropout regulator." pp. 102-105.
[64] K. N. Leung, and P. K. Mok, “Analysis of multistage amplifier-frequency compensation,” *IEEE transactions on circuits and systems I: fundamental theory and applications,* vol. 48, no. 9, pp. 1041-1056, 2001.
[65] K. N. Leung, and P. K. Mok, “A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation,” *IEEE Journal of Solid-State Circuits,* vol. 38, no. 10, pp. 1691-1702, 2003.
[66] E. N. Y. Ho, and P. K. T. Mok, “Wide-Loading-Range Fully Integrated LDR With a Power-Supply Ripple Injection Filter,” *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 59, no. 6, pp. 356-360, 2012.
[67] C. Zhan, and W. H. Ki, “Analysis and Design of Output-Capacitor-Free

Low-Dropout Regulators With Low Quiescent Current and High Power Supply Rejection," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 61, no. 2, pp. 625-636, 2014.
[68] N. A. Keskar, G. A. Rinc, and M. n, "A Fast, Sigma-Delta Boost DC-DC Converter Tolerant to Wide LC Filter Variations," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 55, no. 2, pp. 198-202, 2008.
[69] Y. K. Luo, C. C. Chiou, C. H. Wu, K. H. Chen, and W. C. Hsu, "Transient Improvement by Window Transient Enhancement and Overshoot Suppression Techniques in Current Mode Boost Converter," *IEEE Transactions on Power Electronics,* vol. 26, no. 10, pp. 2753-2761, 2011.
[70] J. C. Tsai, C. L. Chen, Y. H. Lee, H. Y. Yang, M. S. Hsu, and K. H. Chen, "Modified Hysteretic Current Control (MHCC) for Improving Transient Response of Boost Converter," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 58, no. 8, pp. 1967-1979, 2011.
[71] R. J. Baker, *CMOS: circuit design, layout, and simulation*: Wiley-IEEE press, 2019.
[72] B.-S. Song, and P. R. Gray, "Threshold-voltage temperature drift in ion-implanted MOS transistors," *IEEE Journal of Solid-State Circuits,* vol. 17, no. 2, pp. 291-298, 1982.
[73] L. Vadasz, and A. Grove, "Temperature dependence of MOS transistor characteristics below saturation," *IEEE Transactions on Electron Devices*, no. 12, pp. 863-866, 1966.
[74] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and design of analog integrated circuits*: John Wiley & Sons, 2009.
[75] D. Johns, and K. W. Martin, *Analog integrated circuit design*: John Wiley & Sons, 1997.
[76] K. Wong, and D. Evans, "A 150mA low noise, high PSRR low-dropout linear regulator in 0.13 μm technology for RF SoC applications." pp. 532-535.
[77] H. Luo, and L. Siek, "An output-capacitor-less low-dropout voltage regulator with high power supply rejection ratio and fast load transient response using boosted-input-transconductance structure." pp. 447-450.
[78] J. Jiang, W. Shu, and J. S. Chang, "A 5.6 ppm/C Temperature Coefficient, 87-dB PSRR, Sub-1 V Voltage Reference in 65-nm CMOS Exploiting the Zero-Temperature-Coefficient Point," *IEEE Journal of Solid-State Circuits,* vol. PP, no. 99, pp. 1-11, 2016.
[79] C. Huang, C. Zhan, L. He, L. Wang, and Y. Nan, "A 0.6-V Minimum-Supply, 23.5 ppm/° C Subthreshold CMOS Voltage Reference With 0.45% Variation Coefficient," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 65, no. 10, pp. 1290-1294, 2018.
[80] S. Bu, K. N. Leung, Y. Lu, J. Guo, and Y. Zheng, "A Fully Integrated Low-Dropout Regulator With Differentiator-Based Active Zero Compensation," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 65, no. 10, pp. 3578-3591, 2018.
[81] J. Guo, and K. N. Leung, "A 6-uW Chip-Area-Efficient Output-Capacitorless LDO in 90-nm CMOS Technology," *IEEE Journal of Solid-State Circuits,* vol. 45, no. 9, pp. 1896-1905, 2010.
[82] T. Jackum, W. Pribyl, F. Praemassing, G. Maderbacher, and R. Riederer, "Capacitor-less LVR for a 32-Bit automotive microcontroller SoC in 65nm CMOS." pp. 329-332.

[83] F. Lavalle-Aviles, J. Torres, and E. Sánchez-Sinencio, “A high power supply rejection and fast settling time capacitor-less LDO,” *IEEE Transactions on Power Electronics,* vol. 34, no. 1, pp. 474-484, 2018.
[84] W.-C. Chen, Y.-P. Su, Y.-H. Lee, C.-L. Wey, and K.-H. Chen, "0.65 V-Input-Voltage 0.6 V-Output-Voltage 30ppm/degrees C Low-Dropout Regulator with Embedded Voltage Reference for Low-Power Biomedical Systems." p. 304.
[85] P. Y. Or, and K. N. Leung, “An Output-Capacitorless Low-Dropout Regulator With Direct Voltage-Spike Detection,” *IEEE Journal of Solid-State Circuits,* vol. 45, no. 2, pp. 458-466, 2010.
[86] Y.-J. Lee, W. Qu, S. Singh, D.-Y. Kim, K.-H. Kim, S.-H. Kim, J.-J. Park, and G.-H. Cho, “A 200-mA digital low drop-out regulator with coarse-fine dual loop in mobile application processor,” *IEEE Journal of Solid-State Circuits,* vol. 52, no. 1, pp. 64-76, 2016.
[87] S. Kundu, M. Liu, S.-J. Wen, R. Wong, and C. H. Kim, “A Fully Integrated Digital LDO With Built-In Adaptive Sampling and Active Voltage Positioning Using a Beat-Frequency Quantizer,” *IEEE Journal of Solid-State Circuits,* vol. 54, no. 1, pp. 109-120, 2018.
[88] M. Huang, Y. Lu, S.-W. Sin, U. Seng-Pan, and R. P. Martins, “A fully integrated digital LDO with coarse–fine-tuning and burst-mode operation,” *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 63, no. 7, pp. 683-687, 2016.
[89] G. Cai, C. Zhan, and Y. Lu, "A Fast-Transient-Response Fully-Integrated Digital LDO with Adaptive Current Step Size Control." pp. 1-4.
[90] H. Luo, and L. Siek, "A 0.9-V input PWM DCM boost converter with low output ripples and fast load transient response based on a novel square-root voltage mode (SRVM) control approach." pp. 1-4.
[91] C. P. Basso, *Designing control loops for linear and switching power supplies: a tutorial guide*: Artech house, 2012.
[92] M. K. Kazimierczuk, *Pulse-Width Modulated DC-DC Power Converters*: Wiley, 2015.
[93] G. A. Rincon-Mora, *Power IC Design-From the Ground up*: Lulu. com, 2015.
[94] P. E. Allen, and D. R. Holberg, *CMOS analog circuit design*: Elsevier, 2011.
[95] S.-l. Liu, J. Liu, and J. Zhang, "Research on output voltage ripple of boost DC/DC converters." pp. 1-5.
[96] B. Hauke, “Basic calculation of a boost converter's power stage,” *Texas Instruments, Application Report November*, pp. 1-9, 2009.
[97] C. P. Basso, *Switch-Mode Power Supplies: SPICE Simulations and Practical Designs*: BPB Publications, 2008.
[98] P. Lee, “Choosing Inductors for DC/DC Regulators,” no. 6, pp. 4, 2011.
[99] C. Basso, *Switch-mode power supplies spice simulations and practical designs*: McGraw-Hill, Inc., 2008.