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RESEARCH ARTICLE

Hybrid Duty Ratio Phase-Shift Modulation for a Si + SiC Neutral-Point-Clamped Dual-Active-Bridge Converter

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ABSTRACT The neutral-point-clamped (NPC) dual-active-bridge (DAB) converter with hybrid semiconductors (Si and SiC devices) is a promising topology for high-power energy storage systems. The triple-phase-shift (TPS) modulation can achieve high efficiency with zero-voltage switching (ZVS) by adjusting three phase shift angles. However, when applied to hybrid DAB topologies, switching and conduction losses are too high. In this paper, a hybrid modulation method using duty ratio and phase-shift is proposed to improve the efficiency of the hybrid NPC DAB converter. The Si and SiC devices on the primary NPC bridges work under different duty ratios with staggered switching instants so that the Si devices do not suffer from the high turn-off current, and the SiC devices benefit from less conduction time. The neutral current path is used to take over the negative current which flows through SiC body diodes under TPS. Switching and conduction losses under the proposed hybrid TPS modulation are compared. A 2-kW hardware prototype is built to verify the proposed hybrid modulation.

INDEX TERMS Dual-active-bridge converter, hybrid modulation, multilevel converter, switching loss analysis.

I. INTRODUCTION

Promoting the use of renewable energy instead of fossil-fuel-based sources is the key to mitigate global warming. Solar photovoltaic (PV) generation in 2021 is thirty times more than that in 2010 [1]. However, the introduction of renewable energy reduces system inertia, posing a serious challenge to power grid stability.

Thus, energy storage systems (ESSs) usually based on batteries, supercapacitors, and flywheels, are adopted to support the power grid when there are imbalances in the active power generated and consumed [2]. The battery-based ESSs require power electronic converters with good dynamic responses [3].

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As of now, the options for high-power battery ESSs are very limited because the high current and voltage levels challenge the semiconductor devices [4]. To circumvent the limitations of semiconductor manufacturing technology, series and parallel connections are used to reduce voltage and current stress, respectively. The input-series-output-parallel (ISOP) cascaded dual-active-bridge (DAB) converter and input-series-output-series (ISOS) cascaded DAB are studied in [4] and [5]. The neutral-point-clamped (NPC) three-level DAB is one candidate solution. A half-bridge NPC DAB is discussed in [6], and a full-bridge NPC DAB is used in [7]. In [8], a five-level NPC DAB converter was proposed. However, limitations associated with Si IGBT devices, such as restricted switching frequencies across the entire power converter and low utilization of input voltage, led to reduced power transfer capability.

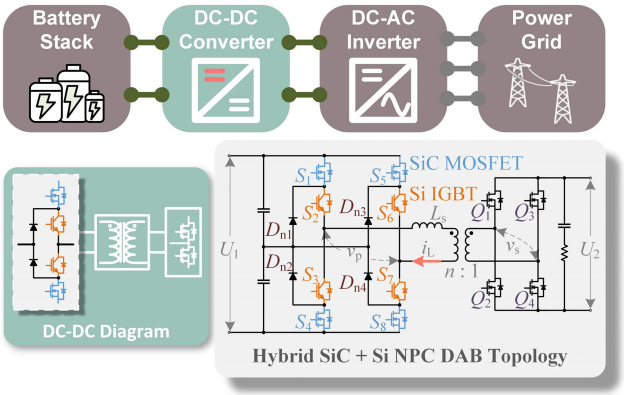


FIGURE 1. System configuration of hybrid NPC DAB converter.

To enhance the performance of the NPC DAB converter, SiC devices were introduced, resulting in a hybrid SiC and Si NPC DAB converter. This hybrid topology was initially introduced in [9], where SiC JFETs were connected in series with Si MOSFETs to optimize thermal performance. However, this approach required a total of 8 switches in each NPC module, comprising 4 SiC JFETs and 4 Si MOSFETs. This not only increased the cost of the switches but also raised the risk of system failure, as JFET overvoltage failures were common. Furthermore, the half-bridge structure was found to be unsuitable for high-power applications.

For applications requiring high voltage and power, the selection of semiconductors is limited. The considerable cost of high-power SiC MOSFETs makes it challenging to incorporate them into commercial power converters without compromising the overall system cost. In [10], a 1500-V, 150-kW battery ESS is studied. The input voltage ranges from 1165 V to 1498 V, and the output voltage rated at 140 V. The demanding requirements for both high voltage and power make it arduous to find a suitable SiC module for commercial products, even when the voltage stress on the semiconductors is halved in an NPC DAB topology. To address this issue, a novel hybrid NPC DAB topology is proposed, which combines the advantages of Si IGBTs and SiC MOSFETs, aiming to fulfil the system's demands for high efficiency and affordability. The performance of the hybrid NPC modules, illustrated in Fig. 1, is compared to that of NPC modules based solely on full Si IGBTs, full SiC MOSFETs, and another hybrid NPC configuration. Based on the conclusions drawn from [10], the hybrid NPC modules depicted in Fig. 1 achieve a good trade-off between efficiency and cost. The hybrid NPC DAB topology, as presented in Fig. 1, enables the utilization of SiC MOSFETs in high-power applications, such as solid-state transformers [11] and fast chargers for electric vehicles [12]. However, due to the limited research scopes discussed in one paper and the focus of reference [10] solely lies in the topological aspect, the modulation technique for this hybrid topology remains undiscussed. Consequently, this paper centers on a comprehensive modulation analysis for the hybrid NPC DAB topology, as well as the comparison of efficiencies across different modulation methods.

The modulation methods for DAB-based topologies can be classified into phase-shift modulation (PSM), duty ratio modulation (DRM), frequency modulation (FM), space-vector modulation (SVM), and hybrid modulation.

Under PSM, the two bridges in the DAB are modulated with a phase shift angle. By adjusting the phase difference between the bridges, the output power can be controlled. Single-phase-shift modulation is widely adopted because of its simplicity [13]. Extended-phase-shift and dual-phase-shift methods introduce an additional control degree to improve the performance [14], [15]. Finally, triple-phase-shift (TPS) modulation makes it possible to tune the phase-shift angles for the primary and secondary sides independently with three control degrees. It can be regarded as the general PSM method. Under TPS modulation, the primary and secondary sides can be optimized at different operating points to attain the best performance among the PSM methods [16]. TPS modulation can achieve performance optimization for peak current [17], [18], zero-voltage switching (ZVS) range [19], and efficiency [20] on both, the two-level DAB and the multilevel DAB converter. One of the main concerns with the PSM methods is that their efficiency under light load conditions may not be as good as their efficiency at rated power [21].

In DRM, the amplitude of the carrier signal for the modulation varies to achieve the desired output power [22]. Compared to PSM, DRM reduces the cost associated with high-precision sensors, while its performance under light load conditions remains satisfactory. However, it is not appropriate for high-frequency applications and usually requires a bulky filter, which inevitably reduces the power density of the converter.

The FM technique can achieve ZVS in a wide operating range, but its dynamic response is relatively poor [23]. Additionally, a bulky capacitor is required for filtering. As for SVM, it is highly praised for its high precision and low total harmonic distortion (THD) [24]. But its implementation complexity in DAB topologies limits its use.

Hybrid modulation attracts attention because it integrates the advantages of various modulation techniques [25]. The hybrid modulation improves efficiency under light load conditions. Furthermore, it requires a smaller filter, which is necessary for proper implementation of DRM.

In a hybrid Si + SiC NPC DAB topology, the primary side is combined with hybrid Si IGBTs and SiC MOSFETs. With the fixed duty ratio and synchronized switching command under PSM, the Si IGBTs turn off at the peak of the current, which results in a large switching loss due to the tail current effect of IGBTs [26]. Furthermore, the SiC MOSFETs suffer high conduction loss because of the high on-resistance [27]. According to the findings presented in [30], for high-power SiC MOSFET modules, despite the nearly consistent low resistance $R_{ds(on)}$ of the SiC MOSFETs, their conduction loss performance diminishes when the current surpasses 50% of the rated current, falling short of the performance demonstrated by Si IGBT modules with equivalent ratings. For the NPC DAB topology, there is no neutral current path under

PSM, which results in high conduction loss on SiC body diodes [28]. Besides, as the Si and SiC devices have different switching rates, the synchronized gate signals in PSM may cause overvoltage failure. Thus, the implementation of a fixed duty ratio is not appropriate for hybrid semiconductor topologies. A more detailed analysis is shown in Section II.

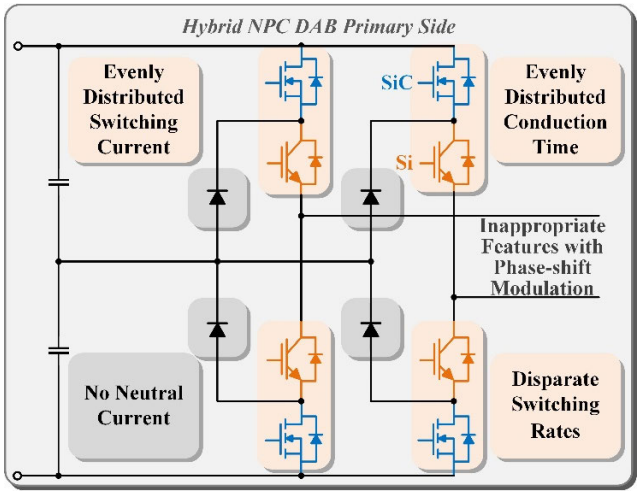


FIGURE 2. Inappropriate features with PSM.

A novel hybrid duty ratio PSM method for the hybrid NPC DAB converter is proposed in this paper aiming to solve the problems of conventional PSM. The primary side NPC bridges apply different duty ratios with a staggered switching sequence for the Si IGBTs and SiC MOSFETs. The Si IGBTs avoid high turn-off current and the SiC MOSFETs attain less conduction time with the proposed hybrid modulation. Besides, the neutral current path is used to reduce the conduction stress of the SiC body diodes. The potential overvoltage failure is also prevented because the staggered switching time is applied for different semiconductors. The proposed hybrid modulation can achieve higher efficiency than conventional PSM. A detailed theoretical analysis is provided, and experimental results from a 2-kW hardware prototype comprehensively validate the feasibility of the proposed hybrid duty ratio PSM.

The structure of the paper is as follows. The challenges of PSM are explained in Section II. The proposed hybrid duty-ratio PSM is analyzed in Section III, and simulation comparisons between the proposed hybrid modulation and TPS modulation are presented in Section IV. Experimental results are shown in Section V. Section VI concludes the paper.

II. CHALLENGES FOR THE PSM IN THE HYBRID NPC DAB CONVERTER AND PROPOSED SOLUTIONS

As the characteristics of Si IGBT and SiC MOSFET are different, the conventional PSM is not suitable for the hybrid topology for the following reasons.

A. CHALLENGES IN THE EXISTING PSM FOR THE HYBRID NPC DAB CONVERTER

1) HIGH SWITCHING LOSS DUE TO EVENLY DISTRIBUTED SWITCHING CURRENT

Evenly distributed switching current under PSM on the primary side leads to high switching loss of the Si switch and a large overvoltage spike on it. Under TPS modulation, because the Si and the SiC devices are in the same bridge arm (such as S_1 and S_2 in Fig. 1) and are still commuted concurrently, the switching currents for both devices are the same. In one aspect, due to the tail current, the Si device suffers great losses during the turn-off process. This switching-off loss shows a positive correlation to the switching current value. Under TPS modulation, the primary side Si switches S_2 andS_7 switch off the positive peak current of the leakage inductor, and Si switches S_3 and S_6 turn off the negative peak current. Thus, the switching loss of the Si device is excessive. Moreover, the high switching current results in high *di/dt*, which creates a large overvoltage spike that may destroy the device.

2) HIGH CONDUCTION LOSS DUE TO EVENLY DISTRIBUTED CONDUCTION TIME

Evenly distributed conduction time under PSM on the primary side results in high conduction loss of the SiC device. As mentioned above, the conventional PSM methods cannot change the duty ratio of the primary side of the hybrid NPC DAB converter. All switches share equivalent conduction time. However, the on-state resistances of the Si IGBT and the SiC MOSFET are not the same. In general, when the working current is high, the Si IGBT shows better performance in conduction loss than the SiC MOSFET due to the lower voltage drop of Si switches. The differences will be more significant with higher temperatures. Moreover, compared with the Si IGBT, the SiC MOSFET is more fragile to the long conduction time under high temperature, which may cause die-attach deterioration [29]. Hence, the PSM that applies the same duty ratio to both the Si IGBT and the SiC MOSFET is not a suitable strategy.

3) BODY DIODES CONDUCTION LOSS DUE TO NO NEUTRAL CURRENT PATHS

The advantages of neutral current paths are not fully revealed with pure PSM methods like TPS. Even though TPS modulation can generate three-level waveforms across the transformer, the zero-level voltage plateau is achieved by switching on either all upper switches or all lower switches in different NPC bridges. There is no current commutation loop passing through the clamping diodes. Thus, continuous current can only flow through the body diodes of the Si and SiC switches when the commutation state changes. However, as indicated by [28], the current that flows through the body diode of the SiC device results in high conduction losses.

4) POTENTIAL OVERVOLTAGE FAILURE DUE TO DISPARATE SWITCHING RATES

Disparate switching rates of Si and SiC devices induce high overvoltage risks for semiconductor switches. Under PSM, even though the gate signals for the switches in the same bridge arms are given simultaneously, the switches do not finish the state transition at the same time due to the different switching rates of Si switches and SiC switches, which increases the overvoltage risk.

B. PROPOSED SOLUTIONS: HYBRID DUTY RATIO PSM

This paper proposes a hybrid duty ratio PSM with a staggered switching sequence to solve the four problems described previously. There are three control freedoms; one control degree adjusts the duty ratio of the primary side switches, while the other two degrees control the inner phase angle among secondary side switches, and the outer phase angle between the primary side and the secondary side to regulate the power transfer.

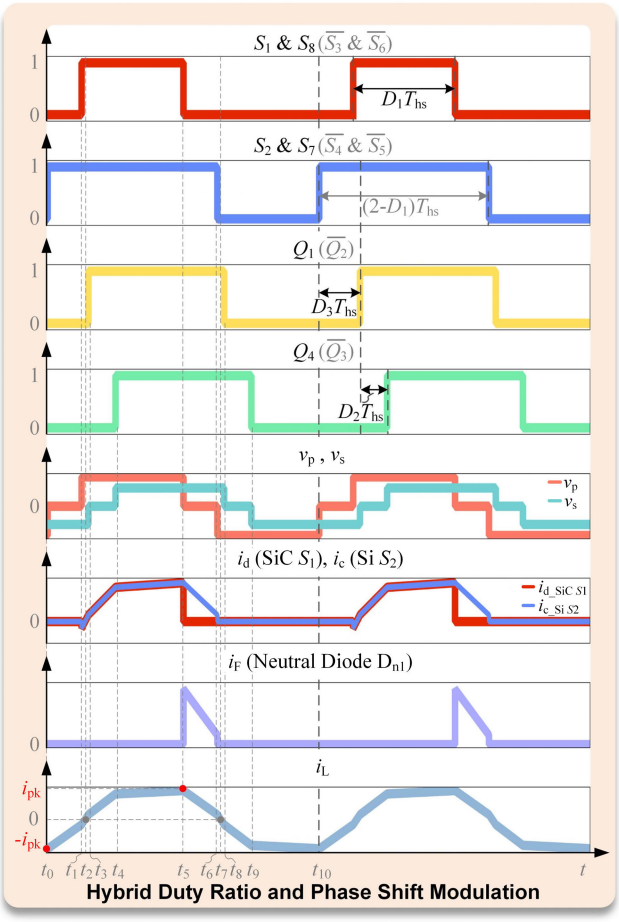


FIGURE 3. Waveforms of proposed hybrid duty ratio PSM.

Under the hybrid modulation method, the switching sequence for the primary side of the hybrid NPC DAB topology is modified. The duty ratio modulation on the primary side brings out the best performance of the hybrid NPC DAB converter. Firstly, the staggered switching sequence of Si and SiC devices mitigates the switching loss with unevenly distributed switching stress. The proposed hybrid modulation assigns a narrower driving signal to the SiC-based MOSFETs S_1, S_4, S_5, and S_8, and applies a wider signal to drive the Si-based IGBTs S_2, S_3, S_6, and S_7. Consequently, the Si devices are commuted at a lower current, which helps to mitigate the excessive switching loss caused by long tail current duration, while the SiC devices handle the peak current with low switching loss. Secondly, the SiC MOSFETs on the primary side are operated with less than 50% duty ratio under the hybrid modulation method, which helps reduce the total conduction loss. Thirdly, thanks to the staggered switching sequence under the hybrid modulation method, the Si device is still closed when the adjacent SiC device is turned off, allowing the continuous current flows through the neutral clamped diodes rather than the SiC body diodes, which also helps to smooth state transitions on primary side switches. Finally, because the Si devices and the SiC devices do not switch concurrently, the underlying overvoltage failure caused by different switching rates is avoided.

III. HYBRID DUTY RATIO PSM

A. WAVEFORMS OF THE PROPOSED HYBRID MODULATION

The waveforms of the proposed modulation method are shown in Fig. 3. On the primary side, the SiC MOSFET S_1 and Si IGBT S_2 follow the duty ratio modulation, and the same pattern applies to S_4 and S_3, S_5 and S_6, and S_8 and S_7. Within the on-state duration of S_2, the SiC MOSFET S_1 completes its switching process. Consequently, the on-state of S_2 is longer than that of S_1. While on the secondary side, the gate driving signals for Q_1 and Q_4 (or Q_2 and Q_3) follow the phase shift rules. Besides, the signals driving S_2 and Q_1 are phase-shifted. The switching cycle starts from the turn-on of the Si IGBT S_2. After the IGBT switch S_2 is activated, SiC switches Q_1 and Q_4 will turn on in a sequential manner and both conduct half switching cycle.

The definition of three control degrees is also shown in Fig. 3. The time that equals half switching time is defined as T_{hs}. The control freedom D_1 defines the duty ratio of the SiC MOSFET S_1. The on-state duration for S_1 is D_1T_{hs}, which is less than or equal to T_{hs}. This modulation parameter exerts a substantial influence on the conduction losses experienced by SiC MOSFETs. While the Si IGBT S_2 in the same arm keeps conducting for $(2\text{-}D_1)T_{hs}$. On the primary side, the SiC MOSFET S_1 and the Si IGBT S_3 receive complimentary driving signals, and so do SiC S_4 and Si S_2, SiC S_5 and Si S_7, and SiC S_8 and Si S_6. Thus, the switching sequences for the Si and SiC are staggered. The second control degree D_2 defines the inner phase angle between the secondary devices Q_1 and Q_4. The third control degree D_3 changes the outer phase shift angle between the primary S_2 and the secondary Q_1. The phase shift between the rising edge of S_2 and the rising edge of Q_1 is defined as D_3T_{hs}.

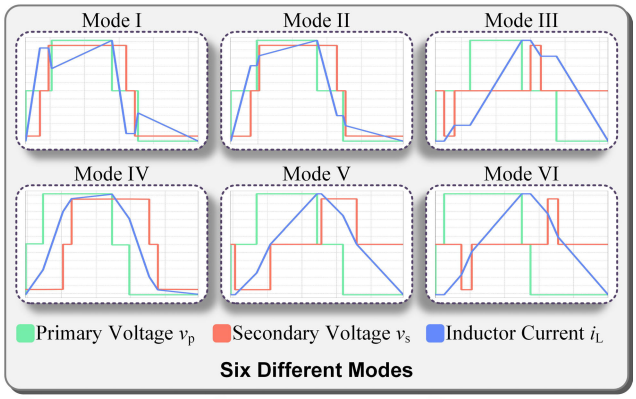


FIGURE 4. Six different modes under the hybrid modulation.

B. OPERATION MODE ANALYSIS

There are six different modes under the hybrid modulation method with three control degrees, D_1, D_2, and D_3. The six modes are displayed in Fig. 4. These modes represent different operating points and are distinguished by the boundary conditions of the modulation parameters D_1, D_2, and D_3, which are summarized in Table 1. The six modes have different power ranges, and Mode IV can cover the full range from zero to the maximum power. Since the methods and processes of analysis are similar, Only Mode IV will be analyzed in the following sections for illustrative purposes.

TABLE 1. Control parameters and power range with different modes.

MODE	RANGE OF D_1, D_2, D_3	MAXIMUM POWER OUTPUT
MODE I	$0<D_3<1-D_1<1$ $0<D_3+D_2<1-D_1<1$	$(-0.5P_{MAX}, 0.5P_{MAX})$
MODE II	$0<D_3<1-D_1<1$ $0<1-D_1<D_3+D_2<1$	$(0, 2/3P_{MAX})$
MODE III	$0<D_3<1-D_1<1$ $1<D_3+D_2<2-D_1<2$	$(0, 0.5P_{MAX})$
MODE IV	$0<1-D_1<D_3<1$ $1-D_1<D_3+D_2<1$	$(0, P_{MAX})$
MODE V	$0<1-D_1<D_3<1$ $1<D_3+D_2<2-D_1$	$(0, 2/3P_{MAX})$
MODE VI	$0<1-D_1<D_3<1$ $1<2-D_1<D_3+D_2<2$	$(-0.5P_{MAX}, 0.5P_{MAX})$

To better understand the relationship between the transferred power and three modulation parameters under Mode IV, voltages and currents are analyzed segment-by-segment using piecewise approach. Specifically, the voltage and current waveforms shown in Fig. 4 for Mode IV are divided into smaller segments, and the power transferred during each segment is analyzed separately. Based on the analyzed segments, the peak inductor current can be derived using equation (1), which is defined as follows:

$$i_p = \frac{U_1}{4f_sL_s}\left[D_1 + k\left(D_2 + 2D_3 - 1\right)\right], \tag{1}$$

TABLE 2. Peak current equations under different modes.

Mode	Peak Current
I	$i_p = \frac{U_1}{4f_sL_s}[D_1 + k(D_2 + 2D_3 - 1)]$
II	$i_p = \frac{U_1}{4f_sL_s}[D_1 + k(D_2 + 2D_3 - 1)]$
III	$i_p = \frac{U_1}{4f_sL_s}[D_1 + k(1 - D_2)]$
IV	$i_p = \frac{U_1}{4f_sL_s}[D_1 + k(D_2 + 2D_3 - 1)]$
V	$i_p = \frac{U_1}{4f_sL_s}[D_1 + k(1 - D_2)]$
VI	$i_p = \frac{U_1}{4f_sL_s}[D_1 + k(1 - D_2)]$

where U_1, f_s, L_s, and k represent the input voltage, switching frequency, leakage inductance and voltage conversion ratio respectively, and D_{1-3} are the modulation parameters. The peak current equations under all six modes are listed in Table 2.

As the output power P is the average of the instantaneous inductor voltage and current u_L and i_L integrated over time, P can be calculated by:

$$P = \frac{1}{2T_{hs}}\int_0^{2T_{hs}} u_L(t)i_L(t)dt. \tag{2}$$

From (2), the equation for the output power under Mode IV is:

$$P = \frac{kU_1^2}{2f_sL_s}\left[D_3\left(1 - D_3\right) - \frac{1}{2}\left(1 - D_1\right)^2 - \frac{1}{2}D_2\left(D_1 + D_2 + 2D_3 - 2\right)\right]. \tag{3}$$

C. COMMUTATION STATE ANALYSIS

The detailed commutation states under Mode IV are shown in Fig. 5. The current passing through the inductor from left to right is defined as positive. The first switching cycle starts at the time t_0 and ends at the time t_{10}.

Commutation state t_0: At the time t_0, the inductor current reaches the negative maximum value. The SiC MOSFETs S_4 and S_5 on the primary side turn off the negative peak current, and the Si IGBTs S_2 and S_7 turn on at the same time. On the secondary side, Q_2 and Q_3 are in the on state.

Commutation state (t_0, t_1): During the time between t_0 and t_1, the voltage across the inductor is nU_2, hence the negative current reduces. But it still reversely flows through the inductor. On the primary side, the current path consists of Si IGBT S_3, neutral diode D_{n2}, neutral diode D_{n3}, and Si IGBT S_6. There is no current running through the SiC MOSFET body diodes during this time. On the secondary side, the current flows through the body diodes of Q_2 and Q_3.

Commutation state t_1: At the time t_1, on the primary side, the Si IGBT S_3 and S_6 turn off, and the SiC MOSFET S_1 and

S_8 turn on. On the secondary side, Q_2 and Q_3 are in the on state.

Commutation state (t_1, t_2): During the time between t_1 and t_2, the voltage across the inductor is U_1+nU_2, hence the negative current reduces sharply. On the primary side, the current path changes to the body diodes of S_1, S_2, S_7, and S_8 for a short time. The voltages of S_1, S_2, S_7, and S_8 are clamped to zero with the negative current flowing through the body diodes. Therefore, ZVS of S_1, S_2, S_7 and S_8 is achieved. On the secondary side, the current flows through the body diodes of Q_2 and Q_3 so that ZVS is also ensured.

Commutation state t_2: At the time t_2, the negative inductor current reduces to zero. The switches S_1, S_2, S_7, S_8, Q_2, and Q_3 are activated at this time.

Commutation state (t_2, t_3): During the time between t_2 and t_3, the current direction changes to positive. The voltage across the inductor is $U_1+ nU_2$. The positive current keeps increasing. On the primary side, the current path changes to Si IGBTs S_2, S_7, SiC MOSFETs S_1, and S_8. On the secondary side, the current flows through Q_2 and Q_3.

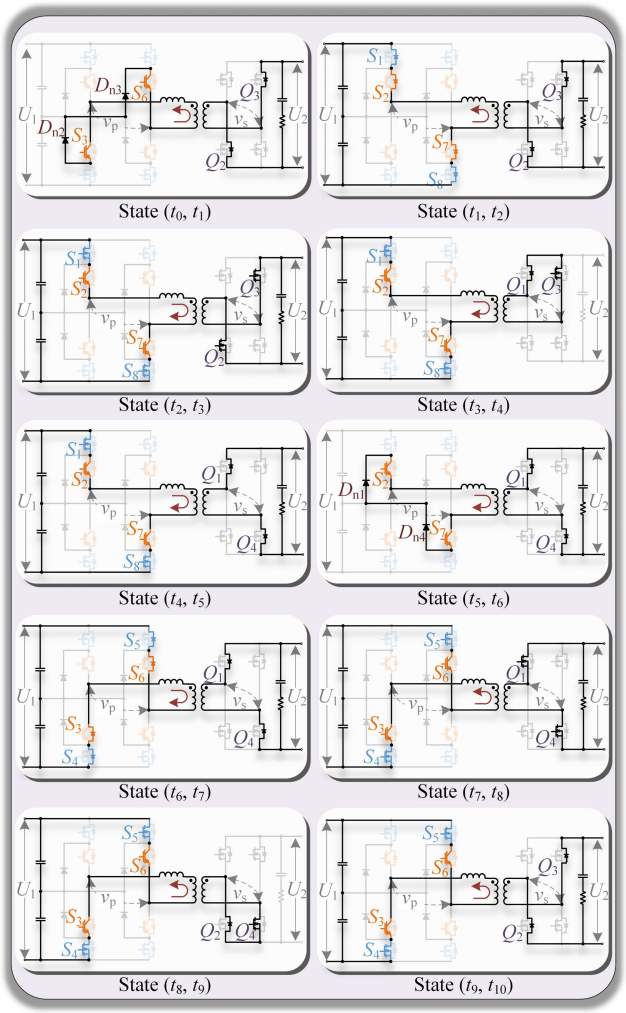


FIGURE 5. Commutation states under Mode IV.

Commutation state t_3: At the time t_3, on the primary side, the SiC MOSFETs S_1, S_8, Si IGBTs S_2, and S_7 are in conduction. On the secondary side, Q_2 turns off and Q_1 turns on, while Q_3 is still active.

Commutation state (t_3, t_4): During the time between t_3 and t_4, the voltage across the inductor is U_1, and the current increases. On the primary side, the current path is made by S_1, S_2, S_7, and S_8. On the secondary side, the current flows through Q_3 and the body diode of Q_1. The drain-to-source voltage of Q_1 is clamped to zero. ZVS of Q_1 is achieved.

Commutation state t_4: At the time t_4, on the primary side, the SiC MOSFETs S_1 and S_8, and the Si IGBTs S_2 and S_7 are in the on state. On the secondary side, Q_3 turns off, Q_4 turns, and Q_1 is activated.

Commutation state (t_4, t_5): During the time between t_4 and t_5, the voltage across the inductor is U_1-nU_2. The current continues rising but slowly. On the primary side, the current path is still made by S_1, S_2, S_7, and S_8. On the secondary side, the current changes to the body diodes of Q_1 and Q_4. The voltage across Q_4 is zero. Hence, ZVS for Q_4 is achieved.

Commutation state t_5: At the time t_5, the inductor current reaches the maximum value. On the primary side, the SiC MOSFETs S_1 and S_8 turn off the positive peak current, and the Si IGBTs S_3 and S_6 receive the driving signals at the same time. On the secondary side, Q_1 and Q_4 are active.

Commutation state (t_5, t_6): During the time between t_5 and t_6, the voltage across the inductor is -nU_2. The current drops from the peak. On the primary side, the current path is combined with the Si IGBT S_2, neutral diode D_{n1}, neutral diode D_{n4}, and Si IGBT S_7. There is no current passing through the SiC body diodes during this time. On the secondary side, the current flows through the body diodes of Q_1 and Q_4.

Commutation state t_6: At the time t_6, on the primary side, the Si IGBTs S_2 and S_7 turn off, and the SiC MOSFETs S_4 and S_5 turn on. On the secondary side, Q_1 and Q_4 are in the on state.

Commutation state (t_6, t_7): During the time between t_6 and t_7, the voltage across the inductor is -(U_1+nU_2). Hence, the current decreases. On the primary side, the current path changes to the body diodes of S_3, S_4, S_5, and S_6 for a short time. The voltages of S_3, S_4, S_5, and S_6 are clamped to zero with the negative current passing through the body diodes so that ZVS of S_3, S_4, S_5, and S_6 is achieved.

Commutation state t_7: At the time t_7, the positive inductor current reduces to zero. The switches S_3, S_4, S_5, S_6, Q_1, and Q_4 are active at this time.

Commutation state (t_7, t_8): During the time between t_7 and t_8, the current direction becomes negative. The voltage across the inductor is -(U_1+ nU_2). The negative current increases. On the primary side, the current path changes to Si IGBTs S_3, S_6, SiC MOSFETs S_4, and S_5. On the secondary side, the current flows through Q_1 and Q_4.

Commutation state t_8: At the time t_8, on the primary side, the SiC MOSFETs S_4 and S_5, and the Si IGBTs S_3 and S_6 are

in conduction. On the secondary side, Q_1 turns off, Q_2 turns on, while Q_4 is still active.

Commutation state (t_8, t_9): During the time between t_8 and t_9, the voltage across the inductor is -U_1. The negative current increases. On the primary side, the current path is made by S_3, S_4, S_5, and S_6. On the secondary side, the current flows through Q_4 and the body diode of Q_2.

Commutation state t_9: At the time t_9, on the primary side, the SiC MOSFETs S_4 and S_5, and the Si IGBTs S_3 and S_6 are in the on state. On the secondary side, Q_4 turns off, Q_3 turns on, while Q_2 is active.

Commutation state (t_9, t_{10}): During the time between t_9 and t_{10}, the voltage across the inductor is -(U_1-nU_2). The negative current continues increasing but slowly. It will reach the negative peak current and start another switching cycle. On the primary side, the current path is still made by S_3, S_4, S_5, and S_6. On the secondary side, the current changes to the body diodes of Q_2 and Q_3.

D. ZVS RANGE ANALYSIS OF THE HYBRID MODULATION METHOD

Similar to the analysis of ZVS range under TPS modulation method, a piecewise method has been employed for the investigation of the ZVS range pertaining to the hybrid duty ratio PSM. As shown in Fig. 6, the switching cycle is partitioned into eight segments under Mode IV.

Ensuring the ZVS range demands certain conditions at various time points. At time T_1, it is imperative for the inductor current to remain below zero to guarantee the ZVS operation of switches S_1, S_2, S_7, and S_8. Subsequently, at the time T_2, when the switch Q_1 turns on, the current must exceed zero, allowing it to pass through the body diode of Q_1, thereby ensuring the ZVS of Q_1. At time T_3, the current should surpass zero to ensure that it passes through the body diodes of Q_4 first, thus guaranteeing the ZVS. it must traverse zero between times T_5 and T_6 to ensure the ZVS of switches S_3, S_4, S_5, S_6, and Q_2. Finally, at time T_7, the current should be negative to secure the ZVS of Q_3.

To provide a succinct overview of the criteria for the six different modes, we have summarized them in Table 3.

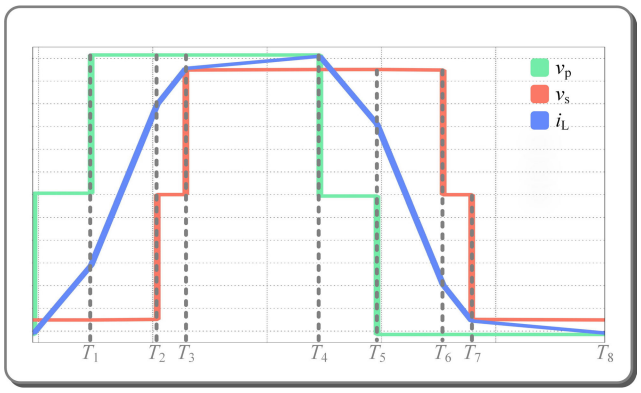


FIGURE 6. Time segments under mode IV for ZVS analysis.

TABLE 3. ZVS criteria under different modes.

Mode	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8
I	+	+	-	+	-	-	+	-
II	+	+	+	+	-	-	-	-
III	-	-	-	+	+	+	+	-
IV	-	+	+	+	+	-	-	-
V	-	-	+	+	+	+	-	-
VI	-	-	-	+	+	+	+	-

E. FEATURES OF THE HYBRID MODULATION METHOD

The proposed hybrid duty ratio PSM method overcomes the four challenges in the existing TPS modulation shown in Fig. 2.

Firstly, the duty ratio modulation on the primary side facilitates uneven switching stress, which significantly reduces switching loss and prevents large overvoltages. As shown in Fig. 3, the peak currents at t_0 and t_5 (red dots in Fig. 3) are all switched by the SiC MOSFETs. Due to the topological structure, the SiC devices do not suffer the tail current effects and the switching-off loss is small even with high switching current. The adjacent Si IGBTs do not turn off thanks to the staggered switching sequence. They continue conducting and turn off the current at t_1 (S_3 and S_6) and t_6 (S_2 and S_7). At time t_5, the peak current is switched by the SiC MOSFETs S_1 and S_8, while the negative peak current is switched by the SiC MOSFETs S_4 and S_5 at time t_0. As the current at t_1 (t_6) is near zero, the switching loss for the Si IGBTs is minimized. Compared to conventional TPS modulation, the switching stress for the SiC MOSFETs is not increased, but the switching stress for the Si IGBTs is reduced. Thus, the total switching loss is reduced. Moreover, the reduced switching current means low di/dt, which reduces the overvoltage spike during the turn-off process and increases the reliability of the NPC DAB converter.

Secondly, the duty ratio modulation on the primary side achieves uneven conduction stress, which greatly reduces the conduction loss. The Si IGBTs and SiC MOSFETs are arranged for different duty ratios so that the conduction time for Si and SiC can be different. As discussed above, the on-state durations for S_1 and S_2 are D_1T_{hs} and (2)-D_1)T_{hs}, respectively. Because the control degree D_1 is lower than one, the conduction time of the Si IGBT S_2 is longer than that of the SiC MOSFET S_1. When the operating temperature increases due to high load current, the Si IGBTs are more suitable for a longer conduction time compared to the SiC MOSFETs due to their lower voltage drop in high-temperature conditions. Thus, since the Si IGBT has a longer conduction time than the SiC MOSFET, the overall conduction loss of the switching devices is reduced.

Thirdly, the neutral current path under the hybrid modulation helps reduce the conduction loss caused by the body

diodes of the SiC devices. For example, during the commutation state (t_5, t_6), the inductor current passes through the neutral diodes because the Si IGBTs S_2 and S_7 are still activated. The SiC body diodes are bypassed with this neutral current path and do not suffer from this high current. Moreover, the inductor current greatly drops during this period. Hence, when the IGBTs S_2 and S_7 are about to turn off, the current is near zero, which greatly helps to reduce the switching-off loss of the IGBTs. Besides, even though the positive current can flow through the body diodes of the SiC switches during the commutation state (t_6, t_7), the conduction loss caused by the SiC body diodes can be neglected because the current is low and the duration is short.

Fourthly, disparate switching rates are avoided with the duty ratio modulation on the primary side because of the staggered switching sequence of the Si IGBT and the SiC MOSFET. The SiC MOSFETs S_1 and S_8 switch on and off at t_1 and t_5, respectively, while the adjacent Si IGBTs S_1 and S_8 switch at t_0 and t_6, respectively. The staggered moments help to avoid the different switching rates when switching different semiconductors, protecting both the Si and SiC switches from possible overvoltage failure.

Moreover, as shown in Figs. 3 and 5, ZVS can be achieved for all the switching devices under the hybrid modulation method. For the primary side switches, the current passes the body diodes of S_1, S_2, S_7, and S_8 during (t_1, t_2). The drain-to-source voltage of the MOSFETs and collector-to-emitter voltage of the IGBTs are clamped to zero. Then, the IGBTs and MOSFETs are activated at t_2. ZVS for S_1, S_2, S_7 and S_8 is achieved. Similarly, the current flows through the body diodes of S_3, S_4, S_5, and S_6 during (t_6, t_7), and drain-to-source voltage and collector-to-emitter voltage are clamped to zero. Hence, the IGBT and MOSFET turn on at t_7 with ZVS. For the secondary side, ZVS is also guaranteed. The MOSFETs turn on with zero drain-to-source voltage because their body diodes are active before turning on the switches. Hence, ZVS is achieved for all the switches in the analyzed operation mode.

Additionally, the hybrid duty ratio PSM does not introduce any additional transformer loss than TPS modulation. This is because the hybrid modulation can generate an inductor voltage waveform equivalent to that of TPS modulation. The detailed waveforms under hybrid modulation are shown in Fig. 4.

F. MODULATION PARAMETERS OPTIMIZATION

As the three modulation parameters are changing in range of the [0, 1], to find out the optimized operation parameters for minimum current stress and optimized ZVS range. The pairs are determined manually, and the corresponding results are records. This brute-force method chooses D_1 and D_2 with 0,002 step. The results are obtained from PLECS simulation with automatic python script.

IV. SIMULATION VERIFICATION

The hybrid modulation method has great advantages over the TPS modulation due to less switching stress and conduction stress on the power semiconductors. Simulation results based on a PLECS platform are obtained to validate the previous analysis, and the results are provided in this section. The simulation details are shown in Table 4. As the primary objective of this study is to verify the effectiveness of the proposed hybrid modulation method, the high-power systems have been downscaled for the purpose of simulations and experimental trials. The validation of the hybrid NPC topology at high power levels has been conducted and results can be found in [10].

TABLE 4. Simulation settings.

Parameters	Values
Battery voltage, U_1	300 V
DC-bus voltage, U_2	140 V
Turns ratio, n	2
Inductance, L_s	236 μF
Switching frequency, f_s	20 kHz
Primary side IGBT	IKW40N65ES5
Primary side MOSFET	UF3C065030K4S
Primary side neutral diode	APT30DQ60B
Secondary side MOSFET	UF3C065030K4S

A. SIMULATION WAVEFORMS OF THE PROPOSED HYBRID TPS MODULATION

The simulation waveforms shown in Fig. 7 validate the improvements of the hybrid modulation on the switching stress, conduction stress, and switching sequence of Si and SiC on the primary side compared to the TPS modulation. The drain-to-source voltage v_{ds} waveform shows that the switching-on time of the SiC devices under the proposed hybrid modulation is postponed compared to that under TPS modulation, which makes the turn-on process for Si and SiC devices different. The collector-to- emitter voltage v_{ce} waveform reveals the fact that the Si devices under hybrid modulation turn off later compared to that under TPS modulation, which makes the turn-off process for the Si and SiC devices staggered. The staggered switching sequence under the hybrid modulation method avoids the potential overvoltage failure caused by disparate switching rates among different semiconductors. The third waveform records the drain-to-source current i_d. Compared to the TPS modulation, the proposed hybrid modulation benefits from the shorter conducting time of SiC devices, which helps decrease conduction loss caused by the negative current i_d, as shown in Fig. 7. Besides, the turn-on current for the SiC devices also drops, which helps reduce turn-on loss. The collector-to-emitter current i_c waveform indicates two benefits that the hybrid modulation method brings to Si devices. One benefit

is that the turn-on loss for the Si devices is less compared to that under TPS modulation due to the lower turn-on current. The other benefit is that the turn-off current of the Si IGBT is not as high as that under TPS modulation, which results in a much lower turn-off voltage spike and lower turn-off loss. The neutral current i_n under hybrid modulation and TPS modulation is shown at the bottom of Fig. 7, which displays the neutral current path existing under hybrid modulation and no neutral current path with the TPS modulation.

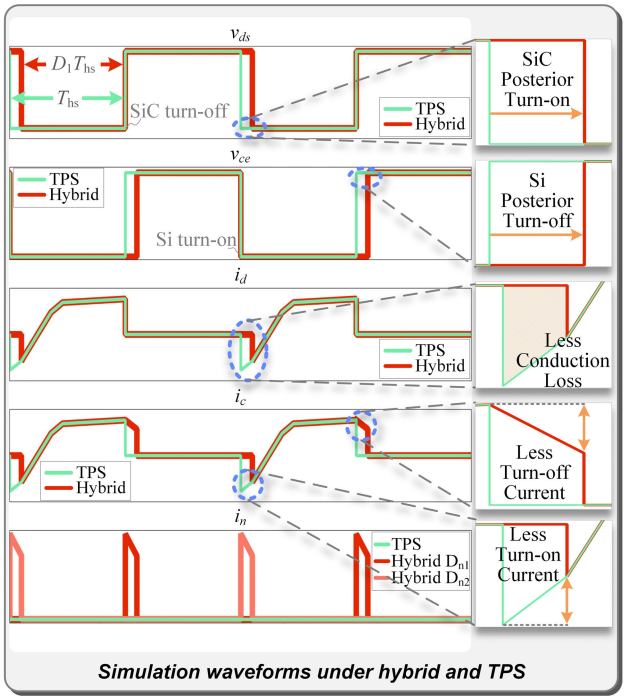


FIGURE 7. Simulation waveforms under the proposed hybrid modulation and TPS modulation.

B. SWITCHING LOSS COMPARISON BETWEEN THE PROPOSED HYBRID MODULATION AND TPS MODULATION

The switching loss under the proposed modulation reduces as indicated in Fig. 7 because of the lower switching current. The switching loss under the proposed hybrid modulation and TPS modulation is compared by simulation. The semiconductor models with practical thermal and loss behavior, as shown in the corresponding datasheets, are used to build the NPC DAB topology. As discussed in Section II, during the time interval $[t_5, t_6]$, the current descent rate is $-\frac{nU_2}{L_s}$, and the duration of this state is equal to $(1\text{-}D_1)T_{hs}$. The peak current under Mode IV is shown in Subsection III-B. As shown in (1), the IGBT switching off current varies with the changes in the control parameters D_1, D_2, and D_3. The switching loss at 2 kW, 1 kW, and 200 W is compared in Fig. 8. At each output power, there are four different pairs of (D_1, D_2). Category I is (D_1, D_2) = (0.96, 0.96), and Categories II to IV represent (0.90, 0.90), (0.80, 0.90), and (0.76, 0.84), respectively. As shown in Fig. 8, the switching loss reduces significantly with the help of the proposed hybrid modulation. When the output power is 2 kW with Category IV, the switching loss in the IGBTs reduces by 42.94%. For the same output power, if Category III is applied, the switching loss is 46.92% less than that with TPS modulation. Moreover, under light load conditions, the hybrid modulation attains both ZVS and zero-current switching (ZCS) simultaneously, reducing more than 0.8 W in each IGBT switching loss. Providing Category IV and $P = 1$ kW, the IGBT can achieve ZCS during the turn-off process, which proves the superiority of the proposed hybrid modulation. Under all load conditions, the switching loss of the proposed hybrid modulation is consistently better because it does not suffer from high switching current compared to TPS modulation. In addition, ZVS can be ensured under the hybrid modulation for the whole power range if the control parameters are properly adjusted.

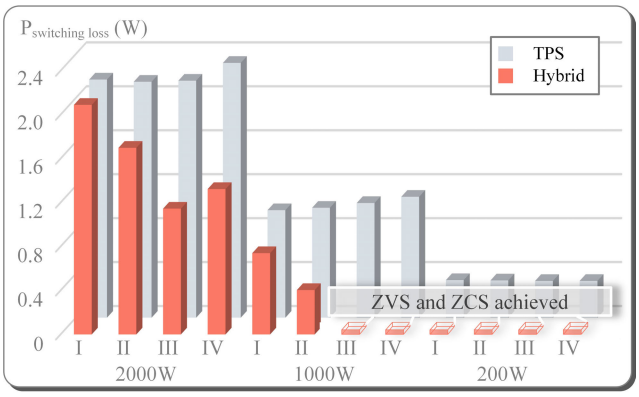


FIGURE 8. Switching loss of Si IGBT devices under the hybrid modulation and TPS modulation.

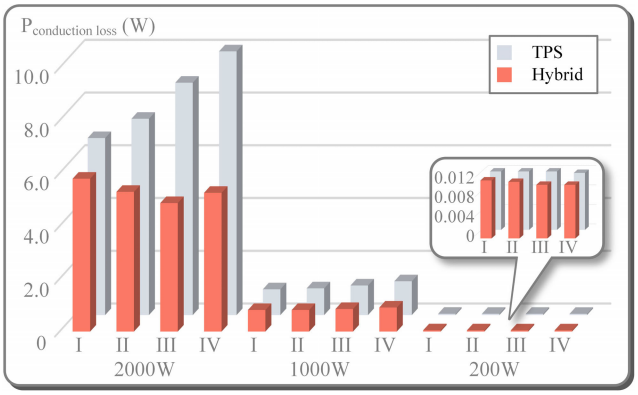


FIGURE 9. Conduction loss of primary SiC MOSFET devices under the hybrid modulation and TPS modulation.

C. CONDUCTION LOSS COMPARISON BETWEEN THE PROPOSED HYBRID MODULATION AND TPS MODULATION

As explained in Section II, the conduction loss of the SiC devices is reduced by the proposed hybrid modulation method. It is achieved by shortening the duty ratio of the SiC

MOSFET and bypassing the body diode of the SiC device with the help of a neutral current path. The conduction loss caused by the on-resistance of the SiC MOSFET is proportional to the integral of the drain-to-source current in the time domain. As shown in Fig. 7, the conduction time of the MOSFET is equal to D_1T_{hs}. Consequently, the smaller D_1, the lower the conduction loss. For the conduction loss caused by the body diode of the SiC devices during the zero-voltage stage of v_p, the neutral clamped diodes are utilized to make the neutral current path. The high current flows through neutral diodes rather than the SiC body diodes so that the conduction loss can be minimized.

The comparison of the conduction loss at different operating points is displayed in Fig. 9. The categories are as same as those defined in Fig. 8. At rated power of 2 kW, the hybrid modulation can reduce more than 5 W in total conduction loss with Category IV. At 1 kW, the conduction loss drops by more than 20% under the hybrid modulation compared to that under the TPS modulation. Operating with light load conditions, the performance under the hybrid modulation is 8% better than that under TPS modulation.

D. EFFICIENCY COMPARISON BETWEEN HYBRID SI + SIC NPC DAB, FULL SI NPC DAB AND FULL SIC NPC DAB

To effectively demonstrate the efficacy of the proposed hybrid modulation method, 150-kW simulation results were obtained using the same modulation parameters but different topologies. The SiC devices are Infineon FF3MR12KM1. Three scenarios were considered: one with a full Si NPC DAB, another with a full SiC NPC DAB, and the third with a hybrid Si + SiC NPC DAB. To assess the improvements in efficiency performance, certain variables were controlled. The modulation parameters were set to (D_1, D_2) values of (0.8, 1.0), (1.0, 0.8), and (0.8, 0.8), respectively. The outcomes of these simulations are presented in Figs 10-12.

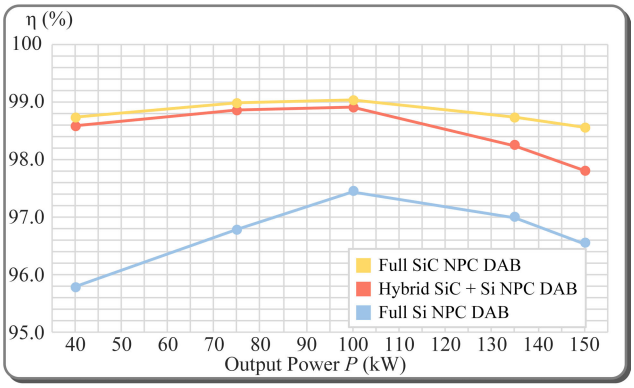


FIGURE 10. Efficiency Comparison among three different NPC modules under proposed hybrid duty ratio PSM with ($D1$, $D2$) = (0.8, 1.0).

As depicted in Figs 10 to 12, the proposed hybrid duty ratio PSM demonstrates its effectiveness in significantly enhancing the efficiency performance of the hybrid SiC + Si NPC DAB converter, optimizing its efficiency to the fullest extent.

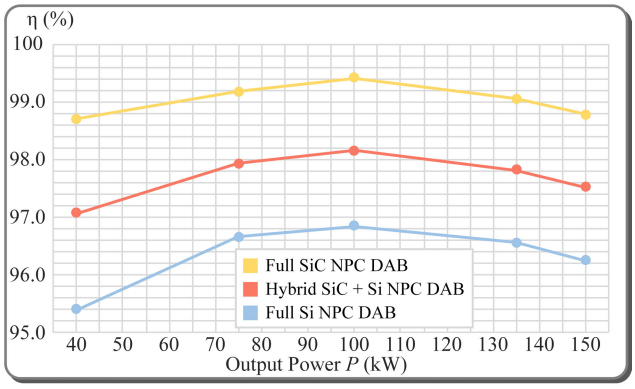


FIGURE 11. Efficiency Comparison among three different NPC modules under proposed hybrid duty ratio PSM with ($D1$, $D2$) = (1.0, 0.8).

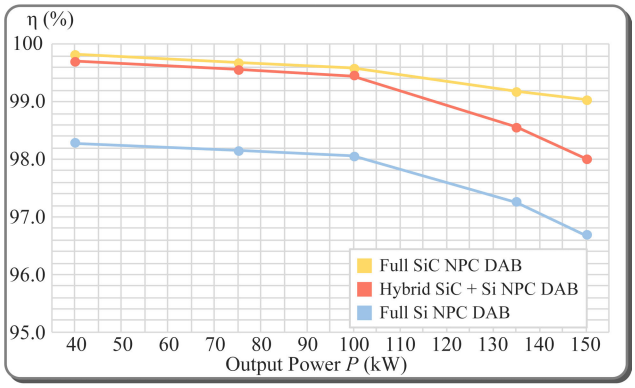


FIGURE 12. Efficiency Comparison among three different NPC modules under proposed hybrid duty ratio PSM with ($D1$, $D2$) = (0.8, 0.8).

Particularly in the context of light load conditions, the proposed hybrid duty ratio enables the hybrid SiC + Si NPC DAB to attain a similar level of efficiency as that of a full SiC NPC DAB, thereby maximizing cost-effectiveness.

V. EXPERIMENTAL RESULTS

A. HARDWARE SETTINGS

A 2-kW NPC-based DAB converter prototype using SiC MOSFETs and Si IGBTs has been built for experimental validation. The hardware platform is displayed in Fig. 13, and the experimental settings are summarized in Table 1. The controller is based on the dSPACE 1202 platform. The converter input voltage is provided by a Chroma programmable dc power supply 62150H-600S. the output side is connected to the dc load, which is provided by a Chroma dc programmable ac/dc electric load 6304. A Yokogawa precision power analyzer WT3000 is used for measuring the converter efficiency, and the oscilloscope used for capturing the waveforms is a Teledyne LeCroy WaveRunner 8058HD.

B. CONTROL DIAGRAM

Fig. 14 illustrates the control diagram. To maintain the output voltage and regulate power transfer, the third parameter D_3 is

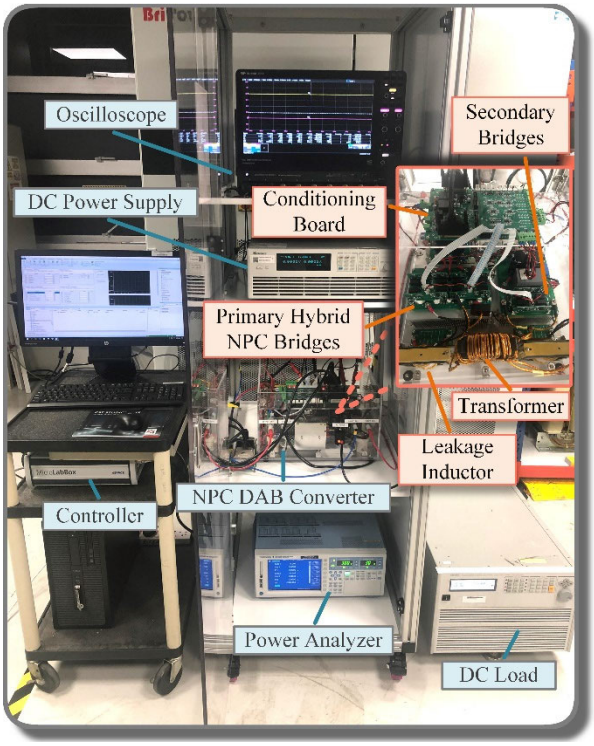


FIGURE 13. Hardware setup of the NPC DAB converter.

controlled by a proportional-integral (PI) controller, while the modulation parameters D_1 and D_2 are determined manually.

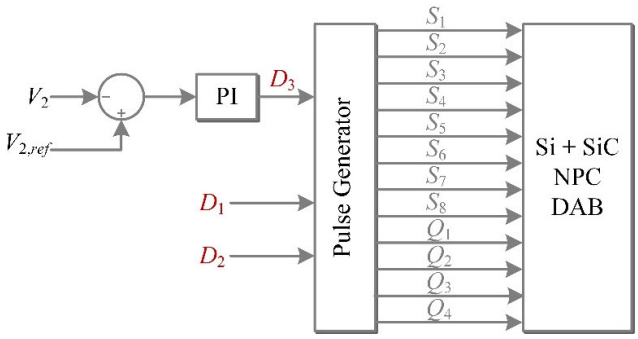


FIGURE 14. Control diagram of Si + SiC NPC DAB under the proposed hybrid duty ratio PSM.

C. MODULATION WAVEFORMS IN THE STEADY STATE

Experimental results at different output powers are shown in Figs. 15 to 17. Fig. 15 shows the waveforms at 2 kW with $(D_1, D_2) = (0.84, 0.90)$, Fig. 12 shows the waveforms at 1 kW with $(D_1, D_2) = (0.72, 0.88)$, and Fig. 17 shows the waveforms at 200 W with $(D_1, D_2) = (0.76, 0.86)$. The figures display different modes under the proposed hybrid modulation when the output power varies from 200 W to 2 kW. At 2 kW, the hybrid modulation is under Mode IV, at 1 kW, the hybrid modulation is under Mode II, and at 200 W, the hybrid modulation is under Mode I. The experimental waveforms match the theoretical analysis provided in Section III.

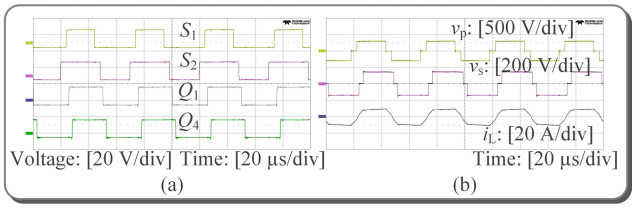


FIGURE 15. Hardware experiments of the proposed hybrid modulation at 2 kW with $(D_1, D_2) = (0.84, 0.90)$. (a) Gate signal waveforms and (b) v_p, v_s, and i_L waveforms.

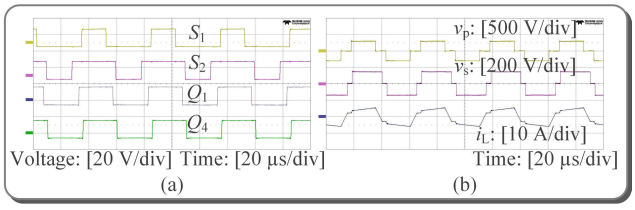


FIGURE 16. Hardware experiments of the proposed hybrid modulation at 1 kW with $(D_1, D_2) = (0.72, 0.88)$. (a) Gate signal waveforms and (b) v_p, v_s, and i_L waveforms.

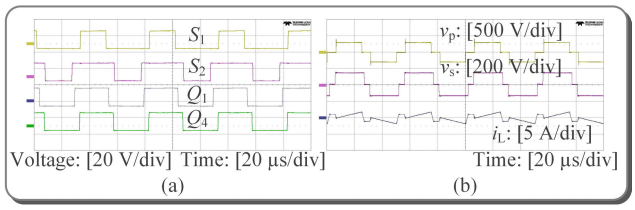
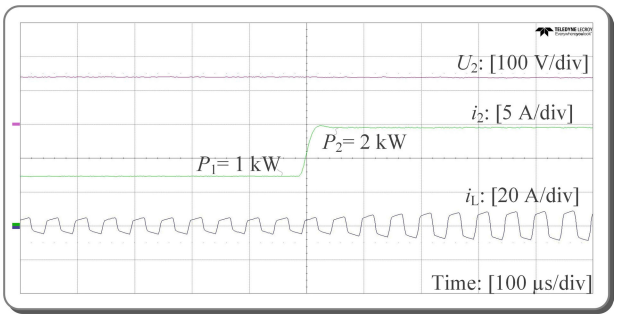


FIGURE 17. Hardware experiments of the proposed hybrid modulation at 200 W with $(D_1, D_2) = (0.76, 0.86)$. (a) Gate signal waveforms and (b) v_p, v_s, and i_L waveforms.

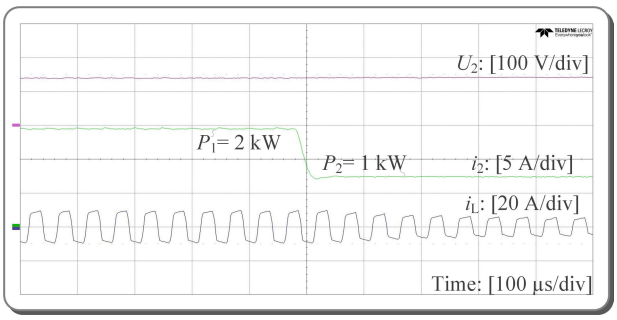
As shown in Figs. 15 to 17, the proposed hybrid modulation changes the duty ratio of the primary side SiC MOSFET S_1 and Si IGBT S_2, which reduces the S_1 on-state time and prevents S_2 from the high switching-off current. Besides, it shifts the inner phase angle between secondary bridges and the outer phase angle between the primary and secondary sides. The proposed hybrid duty ratio PSM is verified with these experimental results.

D. TRANSITION PERFORMANCE OF THE PROPOSED HYBRID MODULATION

The transition performance of the proposed hybrid modulation method is displayed in Fig. 18. The output voltage U_2, output current i_2, and inductor current i_L are presented when the output power changes from 1 kW to 2 kW and from 2 kW to 1 kW. The experiment results show that the hybrid modulation method can recover quickly from the load step, validating the fast dynamic response.



(a)



(b)

FIGURE 18. Hardware experiments of a transition performance with the proposed hybrid modulation method. (a) Load changes from 1 kW to 2 kW and (b) load changes from 2 kW to 1 kW.

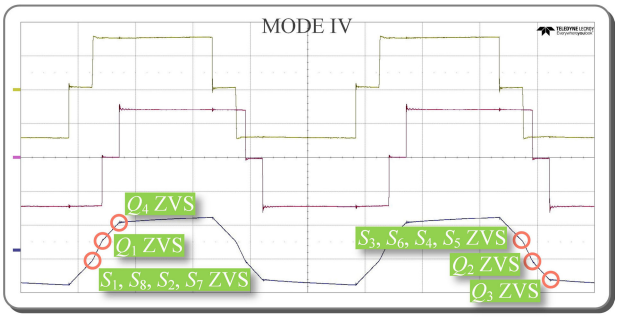


FIGURE 19. ZVS analysis at 2 kW with modulation Mode IV (0.84, 0.90).

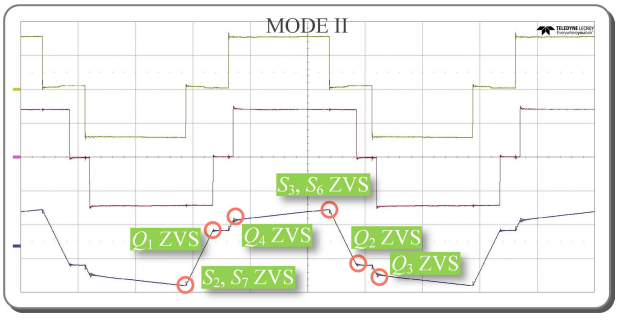


FIGURE 20. ZVS analysis at 1 kW with modulation Mode II (0.72, 0.88).

E. SOFT SWITCHING ANALYSIS OF PROPOSED HYBRID MODULATION

Figs. 19-21 show the ZVS operation for the primary Si IGBT, primary SiC, and secondary SiC devices. When the output power is 2 kW, the converter works under Mode IV. ZVS is achieved for all the Si IGBTs and SiC MOSFETs. The intervals when the current passes through the corresponding body diodes are marked in Fig. 19, which indicates ZVS operation. The Si devices S_2, S_7, SiC S_1, and S_8 achieve ZVS at the same moment and so do the devices S_3, S_6, S_4, and S_5. As shown in Fig. 20, under Mode II, the primary side Si IGBTs and the secondary side SiC MOSFETs can achieve ZVS conditions. At 200 W, the ZVS under modulation Mode I is analyzed. As shown in Fig. 21, the ZVS for all the SiC MOSFETs and all Si IGBTs is satisfied. The primary Si devices S_2 and S_7 achieve ZVS when they receive the gate signals. ZVS is ensured for the primary SiC S_1 and S_8 since the inductor current drops to negative. Hence, ZVS conditions can be ensured for all the primary Si IGBTs and secondary SiC MOSFETs under Modes I, II, and IV. For the primary SiC MOSFETs, ZVS can be achieved under Modes I and IV.

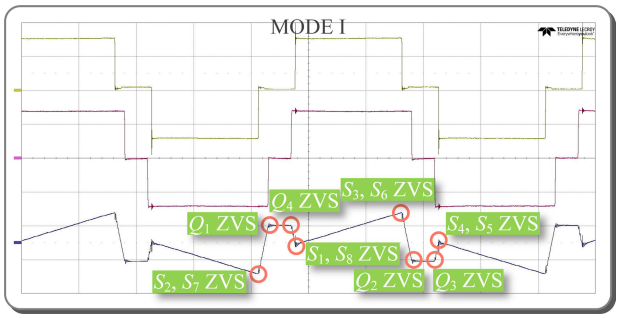


FIGURE 21. ZVS analysis at 200 W with modulation Mode I (0.76, 0.86).

F. EFFICIENCY COMPARISON WITH TPS MODULATION UNDER DIFFERENT VOLTAGE GAINS

Fig. 22 compares the efficiency performance of the hardware prototype under TPS modulation and the proposed hybrid modulation with the same settings shown in Table 2. There are 16 different pairs (D_1, D_2) for output powers ranging from 200 W to 2 kW. At 2 kW, the hybrid modulation method can achieve an efficiency of 96.7%, while TPS modulation can only achieve 96.4%. When the output power is 1 kW, the hybrid modulation can reach the highest efficiency of 97.9% with (D_1, D_2) = (0.88, 1.00). Compared to the performance with fixed duty ratio under TPS modulation, the different duty ratio applied on Si IGBT and SiC MOSFET under the proposed hybrid modulation achieves higher efficiency. Moreover, under light load conditions, the hybrid modulation can maintain the highest efficiency at 97.9%, which is 0.5% higher than TPS modulation.

These experimental results comprehensively verify the effectiveness of the proposed hybrid modulation method. The average efficiency improvement among all load conditions is 0.318% compared to TPS modulation.

Given the impact of voltage gain on the efficiency performance of the DAB-based topology, additional experimental

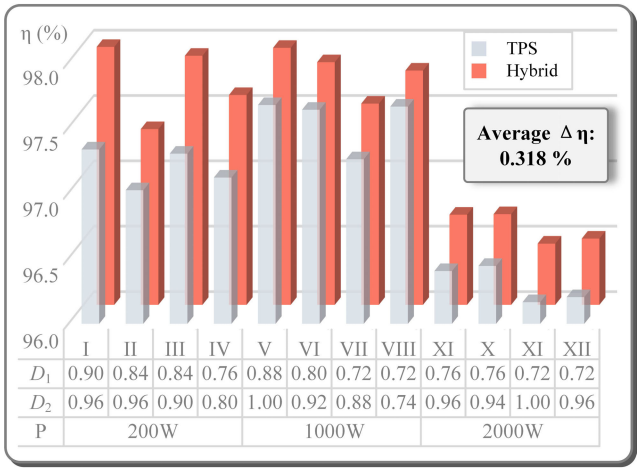


FIGURE 22. Hardware experiments of efficiency performance with the proposed hybrid modulation and TPS modulation (Input: 300 V; Output:140 V).

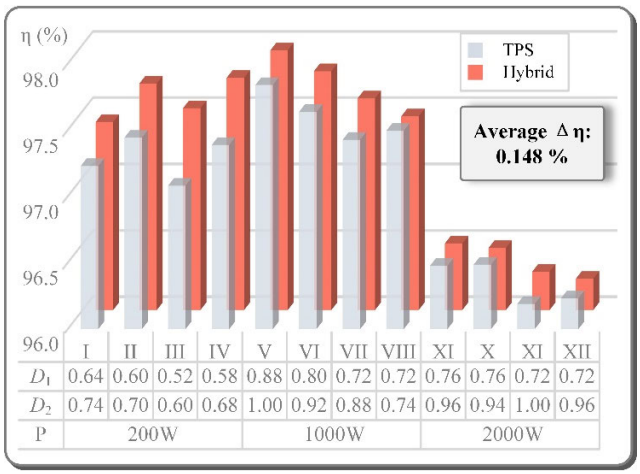


FIGURE 23. Hardware experiments of the efficiency performance with the proposed hybrid modulation and TPS modulation (Input:300V; Output: 130V).

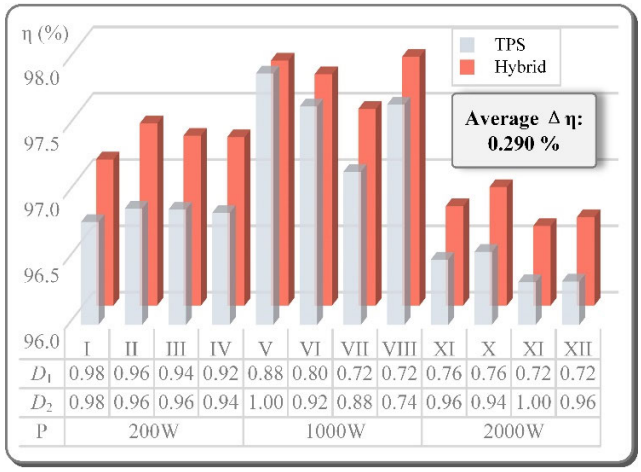


FIGURE 24. Hardware experiments of the efficiency performance with the proposed hybrid modulation and TPS modulation (Input:300V; Output: 150V).

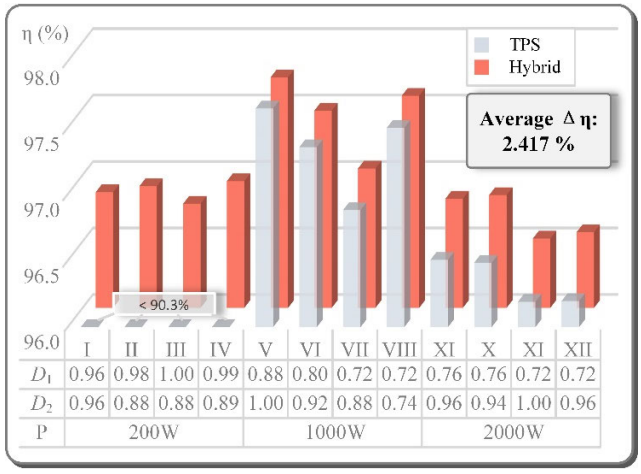


FIGURE 25. Hardware experiments of the efficiency performance with the proposed hybrid modulation and TPS modulation (Input:300V; Output: 160V).

data are shown in Figs. 23-25, which provide insight into the relationship between voltage gain and efficiency.

Fig. 23 compares the efficiency performance of the same hardware prototype under TPS modulation and the proposed hybrid modulation with a 300-V input voltage and 130-V output voltage. For output powers ranging from 200 W to 2 kW, there are sixteen different pairs of (D_1, D_2). The results show that the hybrid modulation method outperforms TPS modulation in terms of efficiency. Specifically, at 200 W, the hybrid modulation method achieves an efficiency of 97.7%, while TPS modulation can only achieve 97.4%. At 1 kW, the hybrid modulation reaches the highest efficiency of 98.0% with $(D_1, D_2) = (0.88, 1.00)$, whereas at 2 kW, the hybrid modulation maintains the highest efficiency at 96.5%. The average efficiency improvement across all load conditions is 0.148% compared to TPS modulation.

Fig. 24 compares the efficiency performance of the same hardware prototype under TPS modulation and the proposed hybrid modulation with a 300-V input voltage and 150-V output voltage. For output powers ranging from 200 W to 2 kW, there are sixteen different pairs of (D_1, D_2). The results show that the hybrid modulation method outperforms TPS modulation in terms of efficiency. Specifically, at 200 W, the hybrid modulation method achieves the efficiency of 97.4%, while TPS modulation can only achieve 96.8%. At 1 kW, the hybrid modulation reaches the highest efficiency of 97.9% with $(D_1, D_2) = (0.88, 1.00)$, whereas at 2 kW, the hybrid modulation maintains the highest efficiency at 96.9%. The average efficiency improvement compared to TPS modulation across all load conditions is 0.290%.

Fig. 25 compares the efficiency performance of the same hardware prototype under TPS modulation and the proposed hybrid modulation with a 300-V input voltage and 160-V

output voltage. As a result of the voltage conversion factor, k, being greater than 1 under this condition, the overall performance of the hybrid NPC DAB tends to be consistently lower compared to when the output voltage is set at 130 V, 140 V, or 150 V. For output powers ranging from 200 W to 2 kW, there are sixteen different pairs of (D_1, D_2). The results show that the hybrid modulation method outperforms TPS modulation in terms of efficiency. Specifically, at 200 W, the hybrid modulation method achieves the efficiency of 96.9%, while TPS modulation can only achieve 90.2%. At 1 kW, the hybrid modulation reaches the highest efficiency of 97.7% with $(D_1, D_2) = (0.88, 1.00)$, whereas at 2 kW, the hybrid modulation maintains the highest efficiency at 96.8%. The average efficiency improvements compared to TPS modulation across all load conditions is 2.417%. The substantial enhancement observed under light load conditions, when compared to TPS modulation, results in a greater average improvement compared to the conditions with 130-V, 140-V, and 150-V output voltages.

In conclusion, the hybrid modulation method achieves a higher efficiency performance than TPS modulation under different voltage gains, which validates the effectiveness of the hybrid duty ratio PSM.

VI. CONCLUSION

A novel hybrid duty ratio PSM has been proposed for a Si + SiC NPC DAB topology. It improves the efficiency of the converter by solving four problems associated with conventional PSM, like TPS modulation. The proposed modulation applies different duty ratios to the primary Si IGBTs and SiC MOSFETs. The primary Si IGBTs S_2, S_3, S_6, and S_7 have a larger duty ratio, while the primary SiC MOSFET S_1, S_4, S_5, and S_8 have a shorter duty ratio. As for the phase shift in hybrid modulation, the outer phase shift angle between the primary S_2 and secondary Q_1 and the inner phase shift angle between the secondary Q_1 and Q_4 can be changed. By adjusting the duty ratio of the primary devices, the switching loss of the Si devices is reduced with a lower turn-off current and the conduction loss of the SiC devices drops with less conduction time. The neutral current path is fully used for the current commutation loop. Meanwhile, the staggered switching time avoids the potential overvoltage failure because of the disparate switching rates. The hybrid modulation is comprehensively analysed and validated with PLECS simulation results. Furthermore, experimental results based on the 2-kW prototype prove that the hybrid modulation achieves higher efficiencies for all the tested operating conditions, which highlights the effectiveness and superiority of the hybrid duty ratio PSM method.

However, concerning the hybrid NPC DAB topology, this single paper's research scope does not encompass the optimization of circuit parameters, or the work related to balancing capacitor voltages. The discussion of the impact of the hybrid duty ratio PSM on the hybrid NPC DAB topology is primarily from a modulation perspective.

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