Study of Chip Scale Wireless Interconnect Systems and Their Antennas

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Summary

The traditional wire interconnects are approaching their fundamental material limits in the giga-scale integration (GSI). Intra- and inter- chip wireless interconnects become possible with high-frequency silicon technologies and ever-increasing integrated-circuit (IC) size. In this thesis, the chip scale wireless interconnect systems are analyzed in terms of bit error rate (BER) performance and studied in terms of their antennas, including on-chip antennas for intra-chip wireless interconnects and on-package antennas for inter-chip wireless interconnects.

A novel inter-chip RF-interconnect (RFI) system is first proposed and analyzed in terms of BER performance. It is still a 'wire' interconnect and uses coplanar waveguide (CPW), capacitive couplers, and ultrawide-band (UWB) radios that operate in 22-29 GHz. It is concluded that a high interconnect data rate of 3.33 giga bits per second (Gbps) with a low BER $< 10^{-5}$ up to an inter-chip interconnect distance of 3 cm is achievable with the average transmitted power less than -2.85 dBm.

An intra-chip wireless interconnect system is then studied in terms of BER performance. A method is presented to evaluate the system BER. The BER performance of

various digital modulation schemes in the system is evaluated at 25 GHz, including coherent MASK, MPSK, MQAM, GMSK and MSK, as well as noncoherent MFSK and MDPSK. It is concluded that by taking feasible measures a high data rate at 2 Gbps with a low BER $< 10^{-5}$ up to an intra-chip wireless channel of length 2 cm is achievable under the reasonable signal-to-noise ratio (SNR) budget.

On-chip antennas are suitable for intra-chip wireless interconnects. On-chip dipole pair's transmission mechanism is analyzed and its performance is simulated. Also, On-chip 60-GHz inverted-F and quasi-Yagi antennas are designed, fabricated, and characterized. Furthermore, on-chip monopoles are fabricated and measured up to 110 GHz. Finally, a novel intra-chip wireless interconnect system using on-chip meander monopole antennas and UWB radios that operate in 22-29 GHz is studied. It is shown that the system on the 10-Ω.cm substrate can support a data rate of 1.5 Gbps with a BER $< 10^{-5}$ up to an intra-chip wireless channel of length 10 mm with the average transmitted power of 0 dBm; while the system on the 5-KΩ.cm substrate can support a data rate of 3.5 Gbps with a BER $< 10^{-6}$ up to an intra-chip wireless channel of length 40 mm with the same transmitted power.

On-package antennas are suitable for inter-chip wireless interconnects. An LTCC-based discrete beveled monopole UWB antenna is fabricated and characterized. The LTCC-based UWB integrated circuit package antenna (ICPA) and 60-GHz ICPAs are also designed. Finally, a novel inter-chip wireless interconnect system using on-package beveled monopole antennas and UWB radios that operate in 3.1-10.6 GHz is studied.

SUMMARY

It is concluded that a high data rate of 1 Gbps with a low BER $< 10^{-7}$ over an inter-chip wireless channel of length 20 cm can be achieved with the radiated power spectral density less than -41.3 dBm/MHz.

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Chapter 1

Introduction

1.1 Background and Motivation

1.1.1 Traditional wire interconnects

Semiconductor technologies continuously scale down feature size to improve the speed of operation. Taking complementary metal oxide semiconductor (CMOS) technology as an example, the minimum feature size of MOS transistors has reduced to 90 nm and the speed of operation has exceeded 100 GHz [1]. Such rapid scaling has two profound impacts. First, it enables much higher degree of integration. Second, it implies much greater challenge of traditional wire interconnects and fundamental material limits are approaching [2].

To parallel with the trend of CMOS device scaling down, metal wire width and space together with via size in the traditional interconnect technology have to be scaled down accordingly. Constant metal resistance is maintained as both width and length have been scaled down, without affecting the metal thickness. Meanwhile, the wire

capacitance per unit length is increasing. Total capacitance is roughly constant, but with another distribution of different contributors: intra-metal contributors are becoming bigger than inter-metal ones. Contact and via resistances are scaling up, since their aspect ratio is becoming worse and worse (fixed height and smaller diameter). The limitation of the traditional interconnect can be viewed from four aspects, namely, interconnect resistance, interconnect capacitance, interconnect inductance, and bit-rate capacity [3, 4, 5, 6, 7, 8]. For interconnect resistance, it is calculated as

$$R_{interconnect} = R_{wire} + R_{contact} + R_{via} \tag{1.1}$$

The number of contacts is constant and the number of vias tends to increase with more metal layers and more complex circuits. For a given capacitance C and its driver there is a value of resistance R that makes that wire a transmission line [5]. With interconnect resistance increasing, more and more interconnect wires are becoming *RC* transmission lines with *RC* delay constant, which can be calculated as

$$\tau_{delay} = R_{interconnect} \times C_{interconnect} \tag{1.2}$$

Hence, the interconnect delay (the delay from the input of a 'line driver' to the output of a 'line receiver' with a transmission line in the middle, where a transmission line is composed of a simple or complex network of resistances and capacitances) is getting larger, as well as the voltage drop across the interconnect.

Next, for interconnect capacitance, its intra-metal capacitance component is increasing. Then the ratio between intra-metal capacitance ('sidewall component') and

inter-metal capacitance ('plate component'), which is related to signal integrity, is getting larger. However, for good signal stability, we have to maintain a small ratio (as long as the ratio is smaller than 1, the signal has a good stability; when the ratio is becoming greater than 1, the significant negative effects such as voltage bump happening and cross coupling effects will be observed). Hence, signal integrity cannot be too high due to the increasing intra-metal capacitance [5]. For the interconnect inductance, it leads to signal ringing, signal reflection and additional inductive crosstalk under fast input slew rate condition [6]. When a circuit frequency increases above 500 MHz, the on-chip inductance must be considered [6].

Finally, for bit-rate capacity, the traditional wire interconnect faces a limit. Once the bit-rate capacity exceeds $\sim 10^{16} A/l^2$ bps or $\sim 10^{17} A/l^2$ bps by equalizing the channels [7], wire interconnects become more difficult, where A is the cross-sectional area of the interconnect wire and l is the length of the wire. The dynamic power dissipation and the crosstalk of the wire become significant as well [7].

As pointed out in [3], for the microchip performance and cost,we are experiencing a epical shift from the transistor dominated age (from the inception of microelectronics in 1959 until the early 1990's) to the interconnect dominated age. Taking the clock distribution as a example, the global interconnect delay presents a particularly detrimental problem since these signals need to be distributed across the microprocessor with skews of less than 10 % of the global clock period. One dilemma is that the delay of a 1.0 mm interconnect devolves faster from one decade to two decades, e.g., it is

1 ps for late 1980's 1.0 μm technology but 100 ps for early 2000's 0.1 μm technology [3]. Concurrent with this dilemma, clock frequency is increasing by 100 times placing stringent new demands on the interconnects that implement the chip clock distribution network. This is in contrast to chip area and total delay through the clock distribution network, which are both increasing. Also with this trend chip-to-package input-output interconnect count increases by 10-20 times and the maximum total wire length per chip increases by 50 times. Hence, techniques are required to equalize the increasingly large delays of each distributed clock signal to even greater accuracies or lower clock skews. Another example for interconnect problem is the heavy burden of the power distribution network with supply current increasing by 60 times while supply voltage scaling downward by 5 times. Seen from the above examples as well as its profound and pervasive nature the interconnect problem demands commensurate response.

1.1.2 Chip scale wireless interconnects

Revolutionary interconnect methods and techniques must be pursued to carry on the fast progress of the future ULSI technology. Possibilities include 3D integration, optical interconnects, and RF/wireless interconnects. 3-D integration has been shown to reduce the number and average length of 2-D global wires by providing shorter 'vertical' paths for connection. However, it needs a new process technology and heat removal remains to be quite challenging [9]. Optical interconnect technologies have long been considered as attractive solutions to providing both inter or intra chip/package applica-

tions. However, the relative size of optical components is a big issue and they exhibit serious challenges to be fabricated in silicon [10]. RF/wireless interconnects become possible with high-frequency silicon technologies and ever-increasing integrated circuit (IC) size [11, 12, 13, 14, 15, 16, 17].

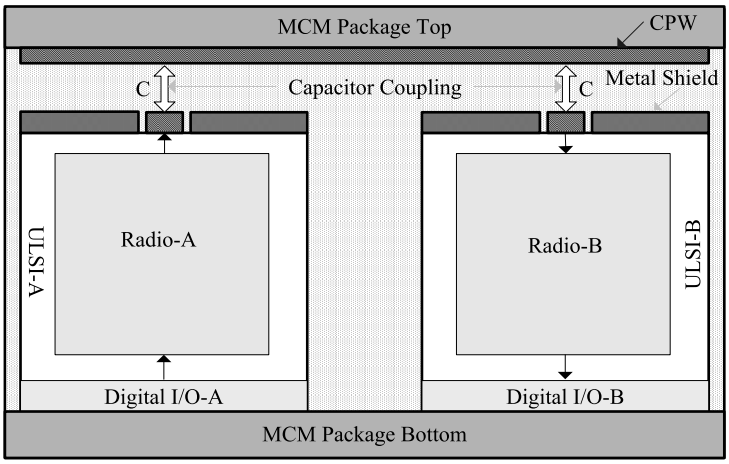


Figure 1.1: Inter-chip RF-interconnect system inside the MCM package.

An RF-interconnect (RFI) system inside a multi-chip-module (MCM) package is presented by Chang *et al.* as shown in Fig. 1.1 [11]. RF signals are up-linked to the shared broadcasting medium, coplanar waveguide (CPW) or microstrip transmission line (MTL) via transmitting capacitive couplers, then down-linked via receiving capacitive couplers to fulfill the interconnect function. Modern communication algorithms CDMA and/or FDMA have been demonstrated to effectively alleviate the undesired cross-channel interference within the shared medium. The RFI system can be very suitable to relay ultra broadband signals up to 150 GHz. It overcomes the limits of conventional digital interface systems using the direct-coupled interconnect (DCI) and

the capacitive coupled interconnect (CCI). It improves the signal-to-noise ratio and lowers the signal swing and output consumption while increases the transmission data rate [18]. For this RFI system structure it has been demonstrated a maximum data rate of 2.2 Gbps in 0.18-μm CMOS technology [18]. In [11, 12, 18, 19], the transceivers of these previous RFI systems are all based on traditional radio structure. As compared with conventional radios, the ultrawide-band (UWB) radio is much simpler and there is no reference oscillator, frequency synthesizer, voltage-controlled oscillator, mixer, or power amplifier, which directly translates to smaller circuitry overhead and power consumption [20]. The concept of integration of UWB transceiver into a chip for intra- and inter- chip wireless interconnect has been proposed in a novel configuration of wireless chip area networks (WCAN) as its physical layer [21]. The UWB radio is firstly proposed as the transceiver for the inter-chip RFI system using CPW and capacitive couplers by us [58]. Based on this idea, a novel RFI system structure is proposed in this thesis to offer an alternative solution for inter-chip interconnect problem.

It is true that the above RFI approach provides the solution for future interconnect. However, it uses 'active' capacitive coupling to CPW or MTL making it still a 'wire' interconnect method and its performance is limited by interconnect capacitors. Problems include the area required by a coupling capacitor, which is about 600 μm^2, and its impacts to interconnect delay time. At this point, the chip scale wireless interconnect systems using on-chip/on-package antennas have shown their advantages. The wireless interconnect system consists of integrated receivers and transmitters with on-chip/on-package antennas which communicates across a single chip or between

multiple chips at the speed of the light via electromagnetic waves. The interconnect delay is expected to be much smaller than that of the wire interconnect, because the signal can propagate at the speed of light, as with optical interconnects [2]. In addition, the system is easier to be integrated in CMOS ICs. Wireless interconnects should also provide an additional means for global communication, freeing up conventional wires for other users.

Chip scale wireless interconnect is a very new approach for intra- and inter- chip interconnects, although the techniques proposed are well developed for wireless communications applications. It faces the same fundamental issues related to component (transmitter, antenna, receiver) size and error correction. Before becoming a viable candidate to replace global wires and/or package interconnects it also has additional difficult challenges to overcome. First, for package applications, its implementation must be cost competitive with existing interconnects and must support the required form factors. Further, the power dissipated by its support circuits must be equal to or less than the power dissipated by the global interconnect wires, and the silicon area consumed by these RF circuits must be less than a few 100 μm^2 [2]. Also, its RF power dissipation cannot add a significant amount of heat to an already heavy thermal load. Finally, similar to optical interconnects, chip scale wireless interconnect systems will likely require adaptation of new system architectures to fully exploit the capabilities of RF interconnects [2].

The chip scale wireless interconnect systems are shown in Fig. 1.2. They can be

classified into two categories, intra-chip wireless interconnects and inter-chip wireless interconnects. They can be used for both data and clock signals. Compared with wireless interconnect for clock signal distribution, the one for data communication is much more complex as a modulation scheme is required.

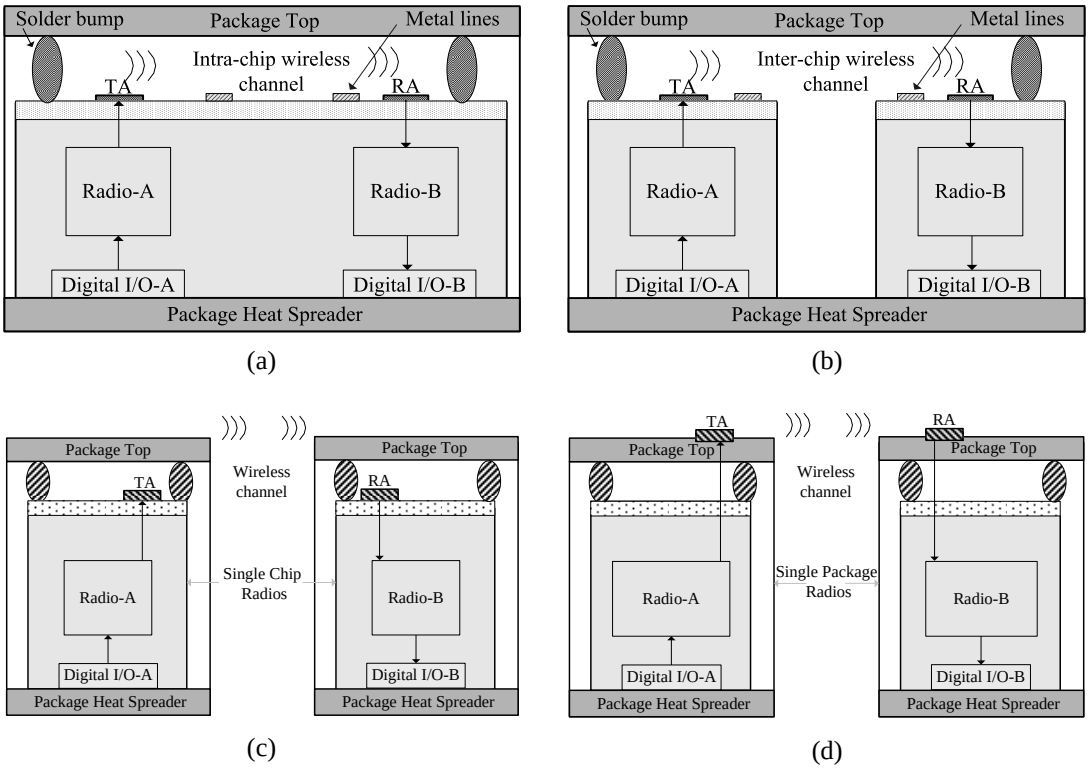


Figure 1.2: Chip scale wireless interconnects: (a) intra-chip wireless interconnect using on-chip antennas, (b) inter-chip wireless interconnect using on-chip antennas inside MCM package, (c) inter-chip wireless interconnect using on-chip antennas through air, and (d) inter-chip wireless interconnect using on-package antennas through air.

A. Intra-chip wireless interconnects

The intra-chip wireless interconnect system is illustrated in Fig. 1.2 (a), which fulfils the wireless interconnection between the digital I/O A and B. The system features on-chip antenna pairs, radios, and a unique intra-chip wireless channel on the same

substrate.

The system can be used for both clock and data signals. It has been demonstrated recently for clock distribution at 15 GHz in 0.18-μm CMOS technologies [13]. It has also received attention for data communication [17], which should be developed to further exploit the capacities of wireless interconnects. This will have great significance on providing the potentials to develop reconfigurable intra-chip wireless interconnect system using multi-access methods to meet the future ULSI interconnect system demands of extremely high data transmission rate, multi-I/O services, reconfigurable and fault-tolerant computing/processing architecture, and full capability with mainstream silicon CMOS and MCM technologies [11]. Unlike wireless clock, wireless data require a modulation scheme. Thus, the accurate analysis of bit error rates (BER) for different digital modulation schemes in intra-chip wireless channels will become increasingly important in system design. BER analysis will not only provide an understanding of the performance of each modulation scheme in the chip environment, but will also reveal the limits of data rate and intra-chip wireless channel capacity. A simple BPSK intra-chip wireless interconnect system for data communication is analyzed at 15 GHz in [17]. To optimally design intra-chip wireless interconnect systems, BER performance of various digital modulation schemes in intra-chip wireless channels should be fully evaluated at the system working frequency, such as 15, 25 or 60 GHz. We will study this issue at 25 GHz in the thesis.

The conventional radios were used in the previous studies for this system. As

compared with the conventional narrowband radios used in wireless clock and data [13, 17], the UWB radio is much simpler and has smaller circuitry overhead and power consumption. The novel intra-chip wireless interconnect system using UWB radios should be evaluated. This will be studied in the thesis.

B. Inter-chip wireless interconnects

The inter-chip wireless interconnect systems are illustrated in Fig. 1.2 (b), (c), and (d), which fulfil the wireless interconnection between the digital I/O A and B. The system features on-chip/on-package antenna pairs, radios on the different substrate and a unique inter-chip wireless channel. For Fig. 1.2 (c) and (d), the inter-chip wireless channel is though air. They realize the wireless communication through air between two single-chip radios or single-package radios, respectively.

60-GHz single chip/package radio has received great attention recently. This is because that a large bandwidth of 7 GHz is available at 60-GHz band for wireless personal area network (WPAN) applications [22]. The large bandwidth and millimeter wave frequency have indeed created many challenges, in particular, in the design of radio front-ends. The 60-GHz radio front-end implemented as an assembly of microwave monolithic integrated circuits (MMICs) in Gallium Arsenide (GaAs) semiconductor technology has proven feasible but rather expensive [23]. The 60-GHz radio front-end based on MMICs in Silicon Germanium (SiGe) semiconductor technology has been attempted. For instance, Renolds *et al.* demonstrated 60-GHz radio front-end circuits including a low noise amplifier (LNA), a direct down converter, a

power amplifier, and a voltage controlled oscillator (VCO) in SiGe technology [24]. Design towards realizing a low-cost fully-integrated SiGe 60-GHz radio front-end has been carried out [25]. As the high-frequency capabilities of CMOS technology improve through scaling, CMOS has become a viable technology for millimetre wave operation. Doan *et al.* has explored CMOS for 60-GHz applications and designed an LNA using a standard 0.13-μm CMOS process [26]. Luiz *et al.* demonstrated 64-GHz and 100-GHz VCOs in 90-nm CMOS [27]. Liu *et al.* demonstrated a 63-GHz VCO in a standard 0.25-μm CMOS [28]. In addition, CMOS technology that promises to integrate a complete 60-GHz system (radio front-end plus digital processor) on a single chip (SoC) further enhances its competitiveness.

UWB single chip/package radio has also received great attention recently. UWB has attracted significant interest for the implementation of high-speed wireless data rates up to 480 Mb/s in short range personal area network. With the development of the ULSI the highly integrated UWB transceiver has become the research focus of many semiconductor companies. It will be aimed to realize a single-chip UWB radio or single-package UWB radio [29, 30, 31, 32]. A novel inter-chip wireless interconnect system using UWB radios will be studied in the thesis.

1.1.3 Antennas for chip scale wireless interconnects

A. On-chip antennas for intra-chip wireless interconnects

On-chip antennas can be used for both intra- and inter- chip wireless interconnect

systems as shown in Fig. 1.2. They are more common to be used for intra-chip wireless interconnects on the same substrate. Here it should be mentioned that on-chip antennas on silicon substrates have been investigated for conventional wireless applications. For instance, Chan *et al.* developed planar inverted-F antennas of size 9.4 to 25 mm^2 on proton-implanted silicon substrate with high resistivity 1 MΩ.cm to resonate at 10 and 5.8 GHz, respectively [33] and Mendes *et al.* developed planar inverted-F antennas of 9 mm^2 on silicon substrate of high resistivity 10 KΩ.cm to resonate at 6 GHz [34]. Micromachining techniques, bulk fabrication, and etching process were employed to construct cavity-backed microstrip patch antennas of 144 mm^2 and 7 mm^2 on silicon substrates of high resistivity to resonate at 16 and 21 GHz, respectively [35, 36]. The on-chip antennas have also been investigated for intra-chip wireless interconnects. However, the previous studies focus more on the dipole. They show that wireless interconnects rely on transmission gains of on-chip antennas. The antenna transmission gain is defined as the ratio of the received power by the receive antenna to the transmitted power by the transmit antenna, where both antennas are conjugately matched. To characterize on-chip antennas, Kim *et al.* fabricated dipoles of axial length 2 mm on bulk, silicon on insulator (SOI), and silicon on sapphire (SOS) substrates and measured their transmission gains from 10 to 18 GHz. They found that the transmission gains of dipoles increase with frequency and they are higher on the SOS substrate than those on the bulk and SOI substrates. The lower transmission gains of the bulk and SOI dipoles are due to the conduction loss of the substrates [37]. To improve on-chip antennas, Rashid *et al.* fabricated dipoles of axial length 2 mm on proton-implanted silicon sub-

strates and measured their transmission gains from 6 to 26.5 GHz. They demonstrated that the proton implantation greatly increased the resistivity of the silicon substrates, so did the transmission gains. They confirmed that the transmission gains of dipoles increase with frequency and found that the transmission gains could be maximized for a given resistivity by optimizing the silicon substrate thickness [38].

On-chip dipoles are preferred in intra-chip wireless interconnects because they can adequately reject noise and interfering signals generated by other circuits on the same silicon substrate. To evaluate the on-chip dipole performance the previous studies are mainly focused on the experimental method [13, 38]. There are some simulation results based on the EM software such as HFSS, but it is time consuming to get the simulation results [39, 40]. The dipole antenna pair transmission mechanism should be further studied and efficient simulation should be further carried out. This issue will be studied in the thesis. In addition, dipole antennas are not compatible with most existing test facilities. They require using baluns to have the measurements done. It is known that baluns are narrow band devices, which partially explains why the reported integrated dipoles for wireless interconnects were measured below 26.5 GHz. To experimentally characterize integrated antennas on silicon substrates over a much broader bandwidth, on-chip monopoles will be designed in the thesis.

A 60-GHz antenna plays a key role in a 60-GHz radio. It has independent properties that affect the radio as a whole. Current antennas for 60-GHz radios are mainly discrete designs on conventional dielectric substrates [41, 42]. At 60 GHz the antenna

form factor is on the order of millimetres or less and opens up new integration options. Integration of millimetre-wave antennas on silicon substrates of high resistivity has been investigated [34, 36, 43]. The 60-GHz on-chip antenna design also becomes possible. However, the problems lie in the large loss due to low resistivity silicon substrate as the frequency increases to millimeter-wave range. The various techniques such as micromachining process and proton implantation have to be employed to combat this problem. The micromachining process removes the loss silicon substrate underneath the antenna radiating element [43], while the proton implantation increases significantly the resistivity of the silicon substrate underneath the antenna radiating element from 10 Ω.cm to 10^6 Ω.cm [33]. In our work, we adopt the post back-end-of-line (BEOL) process developed at Singapore Institute of Microelectronics for RF CMOS passives to overcome this problem. The 60-GHz on-chip inverted-F and quasi-Yagi antenna using this process will be presented in the thesis.

B. On-package antennas for inter-chip wireless interconnects

On-package antennas can be used for inter-chip wireless interconnect systems as shown in Fig. 1.2. On-package antennas have been investigated for the conventional narrow band single-package radio in [44, 45]. They have also been investigated in MCM technologies for 60-GHz radio [46]. Low-temperature cofired ceramic (LTCC) technology has recently become the choice of technology to realize compact RF/microwave modules due to its excellent RF performance [47]. We will design the 60-GHz integrated circuit package antennas (ICPAs) using this technology in the the-

sis. The designed ICPAs are not only as antennas but also as packages that can carry the single-chip 60-GHz radio transceivers for inter-chip wireless communications.

The antenna in a UWB radio plays a more unique role than it does in a conventional narrowband radio because it behaves like a bandpass filter and reshapes the spectra of the UWB pulses. It should be designed with care to avoid pulse distortions. Generally speaking, it is quite challenging to design a suitable antenna to fulfill all the critical requirements of UWB radios, including ultrawide bandwidth, omnidirectional patterns, and constant gain over the entire band, high-radiation efficiency, and low profile [48]. Driven by the development of UWB radios, many antennas for UWB applications have been designed to cover the single band or multi-band of 3.1∼10.6 GHz frequency range. Among them, the monopole antenna has become the choice of antennas for UWB radios due to its attractive merits, such as the ultra wideband characteristic, near omni directional radiation patterns, simple structure and low cost. The monopole antennas for UWB radios can be classified into three types according to their fabrication technology. The first type is in a metal-plate format perpendicularly mounted above a large ground plane. The typical designs can be found in [49] for a shorted metal-plate monopole with a bevel and for a square planar metal-plate monopole with a trident-shaped feeding strip [50]. The second type is in a planar format fabricated on PCB material substrates, such as FR4, RO4350B, and Rogers RT/Duroid 5880. The antenna can be a single or multi-layer structure. The typical designs can be found in [51] for a CPW-fed circular disc monopole antenna and in [52] for a microstrip feed beveled monopole antenna. The third type is in a planar format fabricated

on the LTCC substrates [53]. The typical designs can be found in [54] for a planar volcano-smoke slot monopole antenna and in [55] for a planar monopole antenna with ground plane on the bottom. It should also be mentioned that there are chip antennas fabricated in LTCC for UWB radios. The typical design can be found in [56]. The chip antenna has a radiating element as small as $8\times6\times1$ mm^3. However, a ground plane with almost 5 times larger than the radiating element is needed. This makes the effective antenna dimension still very large. Among above monopole antennas for UWB radios the planar LTCC type provides the great potential to be integrated and further provides the solution of single package UWB radio implementation. This advantage is based on its easily integrated characteristic of planar structure, the excellent RF performance of LTCC technology as well as its miniaturized antenna profile owing to the high dielectric constant of LTCC [47]. The planar monopole antenna fabricated in LTCC not only forms as an antenna but also as a package that can carry a single-chip UWB radio. However, the existing planar monopole antenna in LTCC with smallest dimensions still has radiating element footprint of 23×23 mm^2 on a $66\times50\times1$ mm^3 LTCC substrate. They meet the challenges to be miniaturized and further to be integrated. In [57], this miniaturization issue was detailed. Using circular and beveled planar monopole antennas as examples, we demonstrated through simulations that a 40% size reduction could be realized by simply exploiting their structural symmetry. We found that the miniaturized antennas exhibit wider impedance bandwidth, higher cross-polar radiation, and slightly lower gain as compared with their un-miniaturized counterparts. We confirmed these effects of miniaturization with measurements of

both un-miniaturized and miniaturized beveled monopole antennas. This LTCC-based miniaturized UWB antenna will be presented in the thesis. The LTCC-based UWB ICPA will also be designed in the thesis.

1.2 Objectives

The thesis focuses on two objectives. The first is to propose the structures and evaluate the performance of the intra- and inter- chip wireless interconnect systems. The second is to investigate the suitable antennas for intra- and inter-chip wireless interconnect systems.

1.3 Major Contributions of the Thesis

This thesis studies the chip scale wireless interconnect systems and their antennas. The major contributions are listed as follows. **The first contribution** is that we proposed a novel inter-chip RF-interconnect using CPW, capacitive couplers, and UWB radios and evaluated its performance; **the second contribution** is that we evaluated the BER performance of various digital modulation schemes in intra-chip wireless channels at 25 GHz; **the third contribution** is that we proposed a novel intra-chip wireless interconnect system using on-chip meander monopole antennas and UWB radios and evaluated its performance; **the fourth contribution** is that we proposed a novel inter-chip wireless interconnect system using on-package beveled monopole antennas and UWB radios and evaluated its performance; **the fifth contribution** is that we analyzed

the on-chip dipole antenna pair in theory and simulated it with various parameters. It can be used for intra-chip wireless interconnects; **the sixth contribution** is that we fabricated and characterized the on-chip monopoles, on-chip 60-GHz inverted-F and quasi-Yagi antennas. They can be used for intra-chip wireless interconnects; **the seventh contribution** is that we fabricated and characterized the LTCC-based beveled monopole UWB antenna. It can be used for inter-chip wireless interconnects; **the eighth contribution** is that we finished the initial design of LTCC-based UWB ICPA and 60-GHz ICPAs. They can be used for inter-chip wireless interconnects.

1.4 Organization of the Thesis

In the thesis, a intra- or inter- chip interconnect is treated as a system. The system consists of a transmission antenna (TA) and receiving antenna (RA), a wireless channel, and a modulation scheme which is used to accomplish the signal transmission between transmit/receive sites. This is the methodology used in the whole thesis.

This chapter has presented the background and main achievements of the project. The following chapters will be organized as follows.

Chapter 2 presents and analyzes a novel inter-chip RF-interconnect (RFI) system using CPW, capacitive couplers, and UWB transceivers that operate in 22-29 GHz.

In this chapter, the RFI interconnect is treated as a system, where the capacitive couplers act as TA and RA, CPW as channel and the UWB transceivers are used. We initially restricts considerations to characterization of the channel using transmission

line theory. This is done via HFSS EM simulations as well as MATLAB simulations. By having obtained the channel properties, the system performance is assessed in terms of BER only via simulations in MATLAB.

Chapter 3 evaluates the performance of an intra-chip wireless interconnect system using on-chip antennas at 25 GHz for various digital modulation schemes.

In this chapter, the intra-chip wireless interconnect is treated as a system, where the linear on-chip dipoles are used for TA and RA and the different modulation schemes are used. The focus is the evaluation of the system BER performance varied by the modulation schemes. We initially restricts considerations to characterization of the channel by measurement. By having obtained the channel properties, the system performance is assessed in terms of BER only via simulations in MATLAB.

Chapter 4 first studies on-chip antennas for intra-chip wireless interconnects, including dipole antennas, 60-GHz inverted-F and quasi-Yagi antennas, as well as monopoles. In addition, a novel intra-chip wireless interconnect system using on-chip meander monopole antennas and UWB radios that operate in 22-29 GHz is studied in terms of BER performance.

In this chapter, for the on-chip dipole pair, its transmission mechanism is obtained using theoretical analysis and its performance is simulated using IE3D. For the on-chip 60-GHz inverted-F and quasi-Yagi antennas, they are designed in IE3D, fabricated using BEOL process of silicon substrates of low resistivity, and characterized on wafer with Cascade Microtech coplanar probes and an HP8510XF network analyzer. For

on-chip monopoles they are fabricated and measured up to 110 GHz.

In this chapter, the intra-chip wireless interconnect using on-chip antennas is treated as a system, where on-chip meander monopole antennas are used for TA and RA and UWB radios are used. We initially restricts considerations to characterization of the channel by measurement. By having obtained the channel properties, the system performance is assessed in terms of BER only via simulations in MATLAB.

Chapter 5 first studies LTCC-based on-package antennas for inter-chip wireless interconnects, including a discrete beveled monopole UWB antenna, a UWB ICPA, and 60-GHz ICPAs. In addition, a novel inter-chip wireless interconnect system using on-package beveled monopole antennas and UWB radios that operate in 3.1-10.6 GHz is studied in terms of BER performance.

In this chapter, for the discrete beveled monopole UWB antenna, it is fabricated in LTCC technology and measured in terms of impedance bandwidth, radiation patterns, gain, and both frequency domain and time characteristics. For the UWB ICPA, only a design procedure and result in HFSS are presented. No fabrication and measurement are realized. For the 60-GHz ICPAs, they are also designed in HFSS. No fabrication and measurement are realized.

In this chapter the inter-chip wireless interconnect using on-package beveled monopole antennas is treated as a system, where on-package beveled monopole antennas are used for TA and RA and UWB radios are used. We initially restricts considerations to characterization of the channel by measurement. By having obtained the channel

properties, the system performance is assessed in terms of BER only via simulations in MATLAB.

As shown above, IE3D and HFSS are two EM softwares used mostly in the thesis. It is known that the IE3D is the 2.5D Method of Moments based EM analysis software. As it assumes, infinitely long layers of dielectrics, it provides approximations to the actual circuits and antennas investigated in the thesis, which are of finite dimensions. This is not the case of HFSS of Ansoft, being the Finite Element Method EM analysis software.

Chapter 6 presents the conclusions and recommendations.

Chapter 2

Inter-Chip RF-Interconnects

A novel inter-chip RF-interconnect (RFI) system using CPW, capacitive couplers, and ultrawide-band (UWB) radios that operate in 22-29 GHz is described in section 2.1 and analyzed in terms of system bit error rate (BER) performance in section 2.2.

2.1 System Description

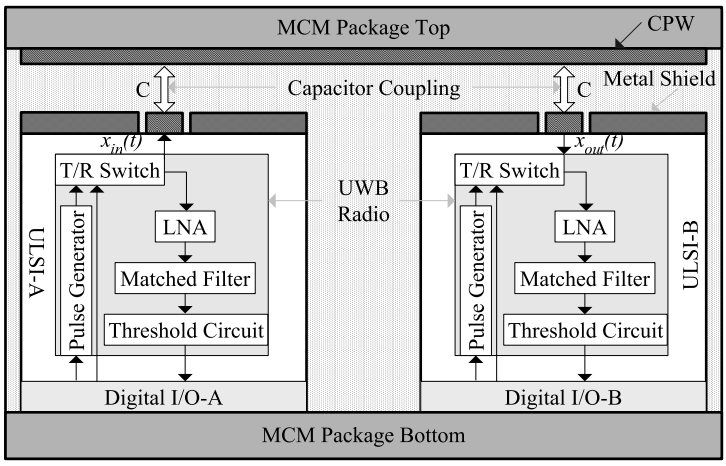


Figure 2.1: Inter-chip RF-interconnect system architecture.

The previous RFI systems are all based on traditional radio structure [11, 12, 18, 19]. The UWB radio is firstly proposed as the transceiver for the inter-chip RFI system by us [58]. The proposed system has the advantage of the small attenuation of CPW

and capacitive coupler channel as well as the advantage of the UWB radio for short range communication. Fig. 2.1 shows this novel inter-chip RFI system located inside a MCM package to fulfill the interconnect function between digital I/O A and B [58].

The system features a unique channel, composed by capacitive couplers and an off-chip but in-package passive CPW as a shared broadcasting medium. A transfer function $H(f)$ is defined as follows to characterize this channel,

$$H(f) = \frac{X_{OUT}(f)}{X_{IN}(f)} \tag{2.1}$$

where $X_{IN}(f)$ and $X_{OUT}(f)$ are the frequency domain representations of the channel input signal $x_{in}(t)$ and output signal $x_{out}(t)$ respectively as shown in Fig. 2.1. In our study $H(f)$ will be characterized by the theoretical method.

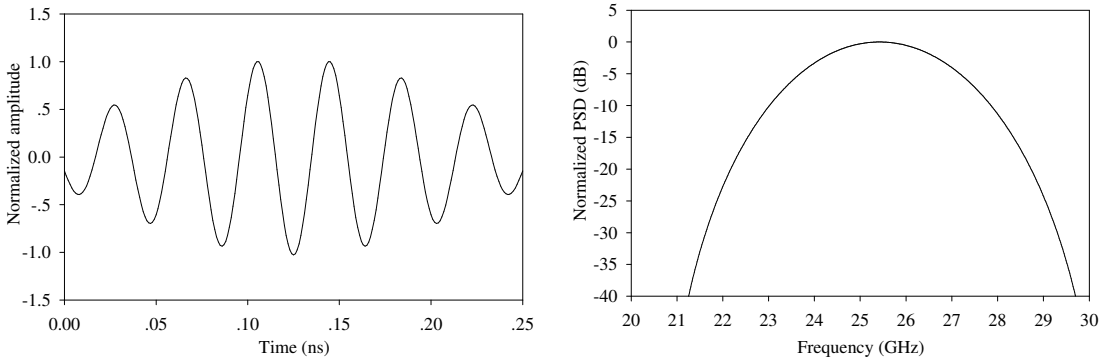
The system features UWB transceivers, which comprise a pulse generator, a transmit /receive (T/R) switch, a low noise amplifier (LNA), a matched filter, and a threshold circuit. The UWB radio can operate over either a 7-GHz bandwidth from 22-29 GHz or a 7.5-GHz bandwidth from 3.1-10.6 GHz. In this study the higher band is preferred for the lower channel loss. The UWB radio adopts the pulse position modulation (PPM) scheme. The PPM signal applied to the channel input $x_{in}(t)$ is then given as [58],

$$x_{in}(t) = \sum_{i=-\infty}^{+\infty} A \cdot g(t - iT_f - d_i\delta) \tag{2.2}$$

where $g(t)$ is the basic UWB pulse with 0.25 ns pulse duration to occupy the 7-GHz bandwidth from 22 to 29 GHz as shown in Fig. 2.2, designed using a novel algorithm proposed in [59]. T_f = 0.3 ns is the frame width that controls the interconnect data rate

R_b = 1/T_f = 3.33 Gbps, d_i is the transmitted data in ith frame. The peak amplitude A, which controls the transmitted energy per bit E_{tb}, is adjusted to meet a certain transmitted power P_t, e.g. when A is 0.03 V we obtain the E_{tb} value of -131.5 dB for 22-29 GHz bandwidth or the average transmitted power P_t less than -2.85 dBm. The PPM delay δ is optimized as 0.02 ns to obtain the best system BER performance according to the criterion,

$$\delta_{opt} = \arg\min_{\delta} \int_{-\infty}^{+\infty} g(t)g(t-\delta)dt \tag{2.3}$$



(a) (b)

Figure 2.2: Designed UWB pulse $g(t)$ and its normalized PSD.

As shown in eq. (2.1), given $x_{in}(t)$ and the theoretically characterized $H(f)$ the channel output signal $x_{out}(t)$ is easily obtained using the Fourier inverse transform.

2.2 System Performance Evaluation

2.2.1 Characterization of the interconnect channel

The channel comprises capacitive couplers and a shared CPW. The characteristic of this channel is first analyzed in [11] based on transmission line theory with some ap-

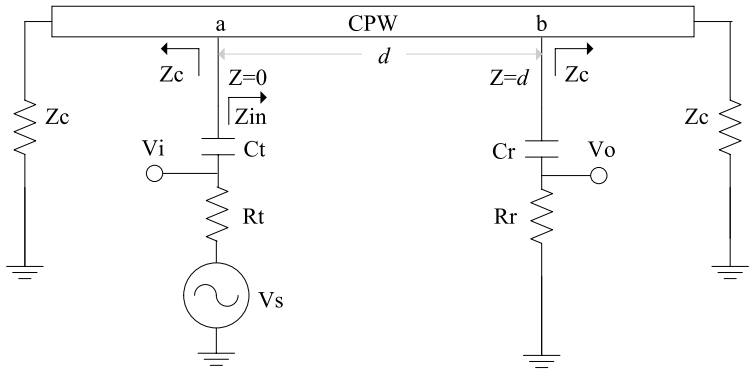


Figure 2.3: Channel model, where C_t is the transmitter's coupling capacitor, C_r is the receiver's coupling capacitor, R_t is the transmitter's output resistance, R_r is the receiver's input resistance, V_s is the source signal voltage, d is the distance between the transmitter and receiver, Z_{in} is the impedance looked into the CPW, V_i is the channel's input voltage, and V_o is the channel's output voltage.

proximation. Here, the channel's exact transfer function is derived in (2.4) based on transmission line theory using the channel model as shown in Fig. 2.3.

$$H(f,d) = \frac{X_{C_t} + Z_c//Z_{in}}{(R_t + X_{C_t} + Z_c//Z_{in})} \cdot \frac{[(Z_{in}+Z_c)\exp(-\gamma d) + (Z_{in}-Z_c)\exp(\gamma d)]}{2(R_t + X_{C_t} + Z_{in})} \tag{2.4}$$

where

$$X_{C_t} = -j\frac{1}{\omega C_t}, X_{C_r} = -j\frac{1}{\omega C_r}, Z_{in} = Z_c\frac{(R_r + X_{C_r})//Z_c + Z_c\tanh\gamma d}{Z_c + (R_r + X_{C_r})//Z_c\tanh\gamma d}, \tag{2.5}$$

$\gamma = \alpha + j\beta$ is the complex propagation constant of the CPW. Its real part α in NP/m represents the attenuation constant and its imaginary part β in rad/m represents the phase constant.

Based on the simulated frequency dependant α and β values in [58], we examined the parameters' effect on the amplitude of transfer function H as shown in Fig. 2.4 (a), (b), and (c). The parameters include the distance between the transmitter and receiver

2.2 System Performance Evaluation

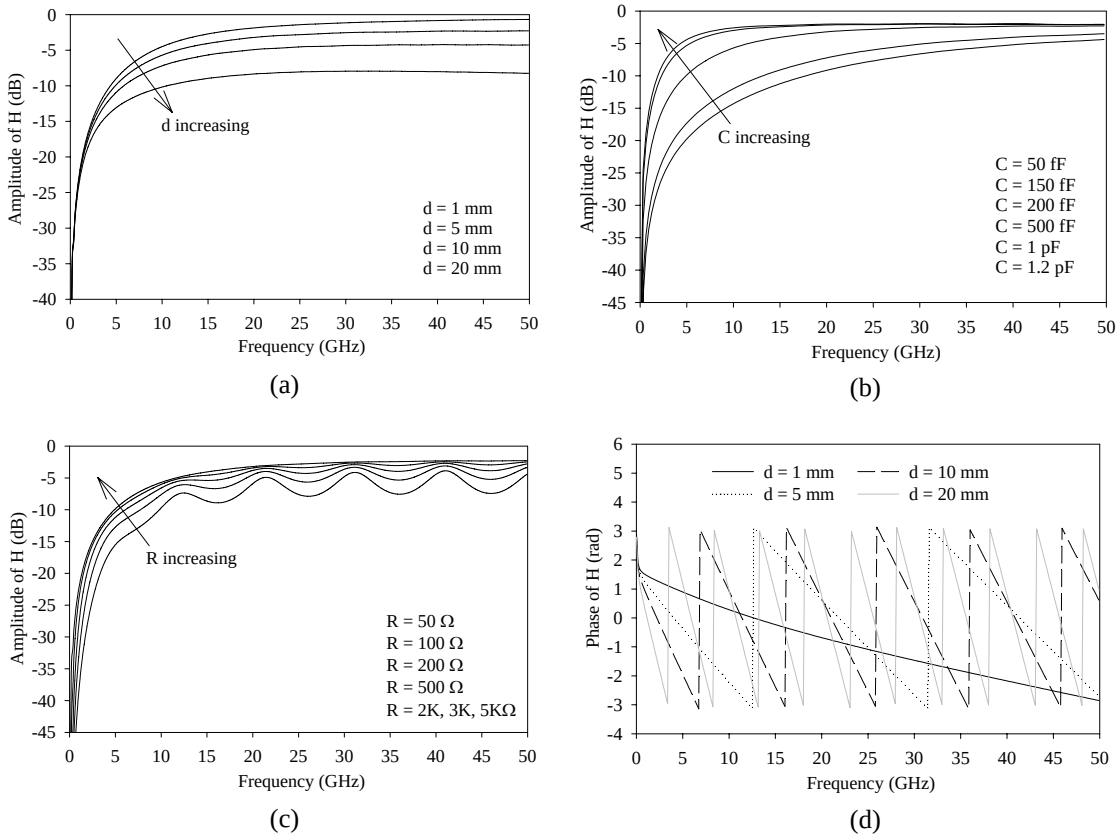


Figure 2.4: Amplitude and phase of H versus frequency: (a) effect of distance: C = 500 fF, R = 5 KΩ, (b) effect of coupler capacitance: d = 5 mm, R = 5 KΩ, (c) effect of resistance: d = 5 mm, C = 500 fF, (d) effect of distance: C = 500 fF, R = 5 KΩ.

d, the coupler capacitance $C = C_t = C_r$, and the resistance $R = R_t = R_r$. Note that the value of coupler capacitance C and resistance R is the same for the transmitter and receiver because of our system's bidirectional communication nature. As expected the amplitude of the transfer function shows the high pass characteristics. In addition, Fig. 2.4 (a) shows that the amplitude of H decreases with distance quickly. The longer distance has the larger attenuation. Fig. 2.4 (b) shows that coupler capacitance C has important effect on the amplitude of H. The smaller capacitance has the larger channel attenuation. Based on this simulation C = 500 fF is chosen for our system. Furthermore, it is found that output resistance R has certain effect on the amplitude of H. R

with small value will cause the fluctuation of the amplitude of H in high frequency as shown in Fig. 2.4 (c). Based on this simulation we choose R = 5 KΩ. The phase of the transfer function in terms of distance is also examined Fig. 2.4 (d). It shows the linear characteristics and the longer distance has the larger delay. Based on the above observation we conclude that the CPW and capacitive coupler channel can be regarded as a high pass filter which has linearly increased delay with interconnect length. This conclusion reconciles well with the measurement result in [60]. The channel characteristics also can be clearly observed in Fig. 2.5, which shows the transmitted data, channel input signal $x_{in}(t)$ and channel output signal $x_{out}(t)$ with normalized amplitude at d = 20 mm. As expected the channel output signal suffers from channel loss and delay. Fig. 2.6 shows their relationship with distance, computed using a time-domain waveform of the signal after the channel. As expected the channel loss L_c and delay both increase with interconnect distance.

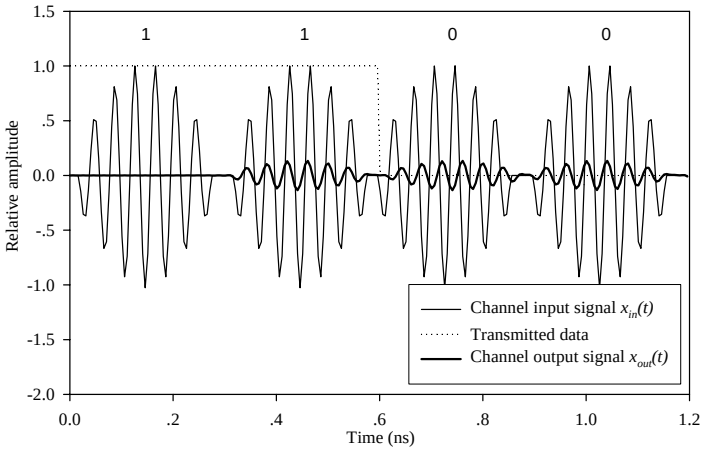


Figure 2.5: Channel input and output signal with normalized amplitude at d = 20 mm.

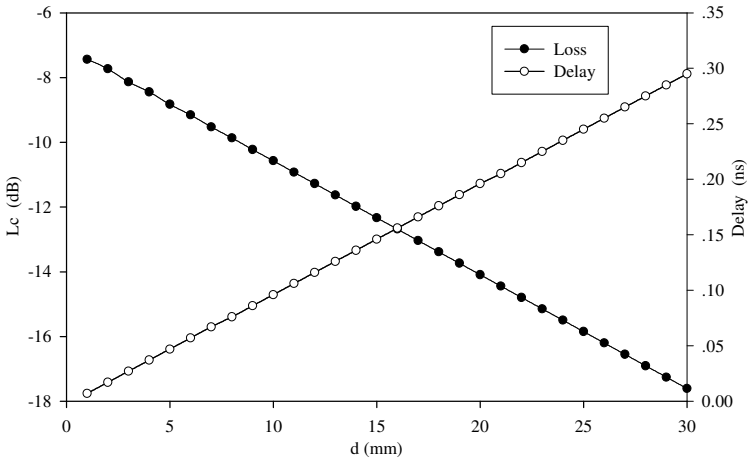


Figure 2.6: Channel delay and loss versus distance.

The highpass characteristics of the channel can greatly reduce the switching noise coupling from the on-chip digital circuitry into the channel at the transmitter end as illustrated in Fig. 2.7. It also explains why the higher UWB 22-29 GHz band is preferable than the lower band. However, for realistic condition switching noise will randomly couple to the CPW channel at any point. The more realistic switching noise model will be developed and the corresponding average noise power spectral density (PSD) will be presented in section 2.2.2.

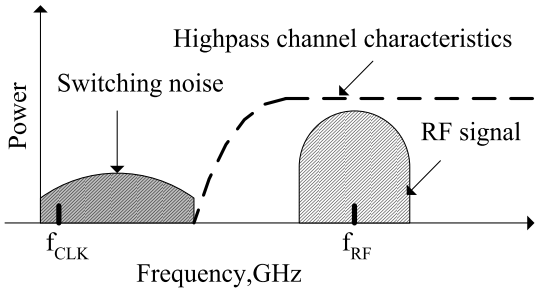


Figure 2.7: Suppression of switching noise at the transmitter end in RF-interconnect.

2.2.2 Switching noise attack model

For our system that integrates both the analog radio front end and digital baseband processing circuits, the switching noise produced by the digital circuits may be significant and impact the receiver performance. Two types of switching noise coupling can be considered. The first type is the noise generated by the transistors in digital circuits injecting currents into the common substrate. Its effect on the system can be modelled by capacitive coupling. The second is the noise capacitively coupled to the CPW in the same layer or from adjacent layers [61]. Therefore, the switching noise attack of both two types can be modeled based on capacitive coupling mechanism.

Fig. 2.8 shows the attack by a switching noise source V_n on a victim CPW through capacitive coupling at the point p. The more realistic attacker waveform $V_n(t)$ is proposed in [61] based on the Markov chain and low pass filter (LPF) model as shown in Fig. 2.9. The switching noise activity is modeled by the Markov chain producing $d(t)$ whose PSD is shown in (2.6), where a is the probability that a particular attacker switches and T is the shortest delay between state transition.

$$S_D(e^{j2\pi fT}) = \frac{a(1-a)}{1+(1-2a)^2-2(1-2a)\cos(2\pi fT)} \tag{2.6}$$

The realistic attack noise waveform $V_n(t)$ is obtained by making $d(t)$ pass through a first-order LPF having a gain V and a time constant τ. Its PSD is then derived as

$$S_n(f,V) = S_D(e^{j2\pi fT})\left|\frac{V^2}{(2\pi f\tau)^2+1}\right| \tag{2.7}$$

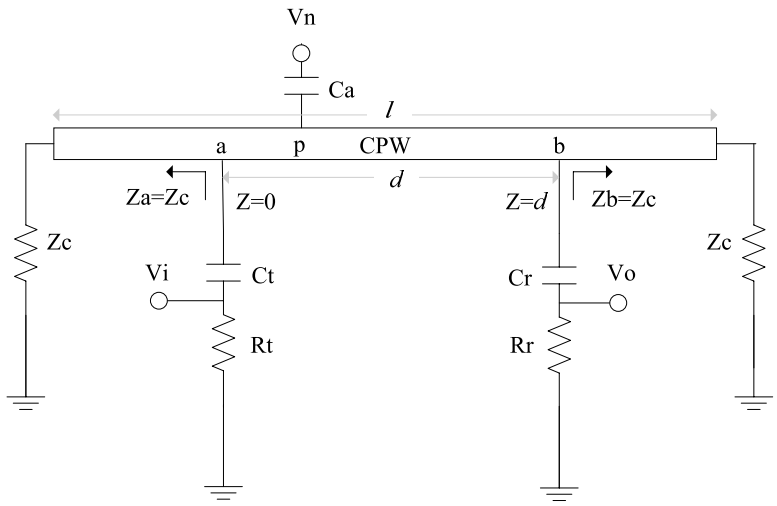


Figure 2.8: Switching noise attack model.

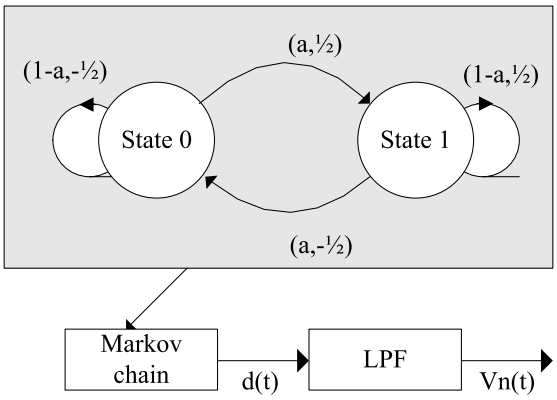


Figure 2.9: Markov chain model for the switching activity of attackers.

For switching noise attack model of Fig. 2.8 the transfer function $H_n(f, p)$ between V_0 and V_n can be exactly derived based on the transmission line theory according to three cases, $p < a$, $a \leq p \leq b$ and $b < p \leq l$. The received noise PSD at V_0 contributed by the single noise attacker V_n is then obtained by

$$S_0(f) = S_n(f, V) \left| H_n(f, p) \right|^2 \tag{2.8}$$

It is assumed that the position of the each attacker p is a random variable, which is

uniformly distributed in the range of 0 to the CPW's length l. The gain V is also assumed to be a random variable having uniform distribution in the range of 0 to 1. To consider the realistic case of many switching noise attackers to the victim CPW, the total PSD of the noise at V_0 is determined by superposing the contribution of each individual attacker. In MATLAB, we simulated the average PSD at V_0 at 5, 10 and 15 attackers, which is calculated by

$$S_{0,av}(f) = \frac{1}{N}\sum_{j=1}^{N}\sum_{i=1}^{5,10,15} S_n(f, V_{ij})\,|H_n(f, p_{ij})|^2 \tag{2.9}$$

where N is the total test number, j is the test index, and i represents the ith switching noise attacker. In every test, a noise source's coupling gain V_{ij} and coupling position p_{ij} is produced randomly according to their distribution. $H_n(f, p_{ij})$ is then calculated according to its position p_{ij}.

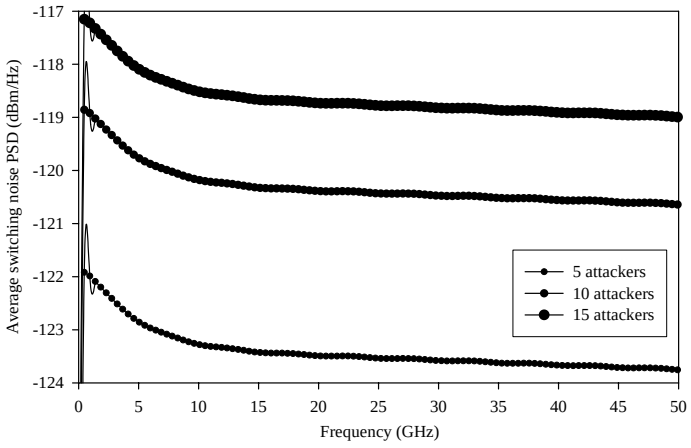


Figure 2.10: Average switching noise PSD versus frequency.

The simulated $S_{0,av}(f)$ at the attacker number of 5, 10 and 15 respectively is shown

in Fig. 2.10. As expected, the $S_{0,av}(f)$ increases with the number of attacker. It is also worth noting that the $S_{0,av}(f)$ has no DC component and is fairly flat in the frequency range 22-29 GHz. The average value in this frequency range S_0 will be used to estimate the average bit signal-to-noise ratio (SNR) at the receiver end in section 2.2.3. The exact transfer function and realistic switching noise attack model presented here makes it possible to realistically estimate the switching noise PSD on the victim line, which will provide important information to evaluate the system's performance.

2.2.3 System BER performance

The system performance is evaluated in terms of BER under the assumptions of perfect system synchronization. For inter-chip interconnect within a package the signal is only contaminated by thermal noise and switching noise. The expression of the thermal noise power spectral density N_0 has been presented in [58] based on the receiver noise figure F_r. It is shown that F_r is 6.6 dB in the lower band and 8.6 dB in the upper band for a CMOS UWB radio operating from 3.1 to 10.6 GHz [63, 64]. Thus, here F_r can be reasonably assumed to be 15 dB. The simulated average switching noise PSD is obtained in section 2.2.2 as S_0. Then the average bit signal-to-noise ratio (SNR) at the receiver end is shown as follows

$$\Gamma_b = \frac{E_{rb}}{N_0 + S_0} \tag{2.10}$$

$$E_{rb} = E_{tb} \cdot L_c \cdot G_r \cdot L_m \tag{2.11}$$

$$E_{tb} = \frac{P_t}{R_b} \tag{2.12}$$

where E_{rb} is the received average energy per bit, calculated based on the gain of the receiver G_r and the implementation margin L_m, which includes all kinds of marginal loss. BER of our system using PPM modulation is then obtained as [58],

$$P_b = \frac{1}{2} erfc\left(\sqrt{\frac{(1-\rho)\cdot\Gamma_b}{2}}\right) \tag{2.13}$$

$$\rho = \frac{\int_0^{T_f} g'(t)g'(t-\delta)dt}{\int_0^{T_f} g'^2(t)dt} \tag{2.14}$$

where $g'(t)$ is the received pulse corresponding to our designed pulse $g(t)$.

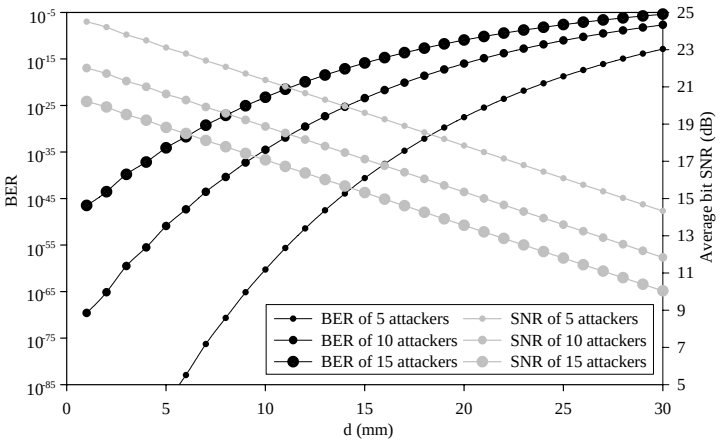


Figure 2.11: Average bit SNR and BER versus distance for the different number of attackers.

The average bit SNR Γ_b and BER versus distance for the different number of attackers are shown in Fig. 2.11. The parameters used in the simulations are L_m = −4 dB, G_r = 15 dB, F_r = 15 dB, and the peak amplitude of the transmitted pulse A is adjusted to 0.03 V. As expected, Γ_b decreases with distance and the attacker number. BER increases with distance and the attacker number. It is concluded that a high inter-

connect data rate of 3.33 Gbps with a low BER $< 10^{-5}$ up to an interconnect distance of 3 cm is achievable with the average transmitted power less than -2.85 dBm.

Chapter 3

Intra-Chip Wireless Interconnects

An intra-chip wireless interconnect system using on-chip antennas is described in section 3.1 and studied in terms of its bit error rate (BER) performance at 25 GHz in section 3.2 for various digital modulation schemes.

3.1 System Description

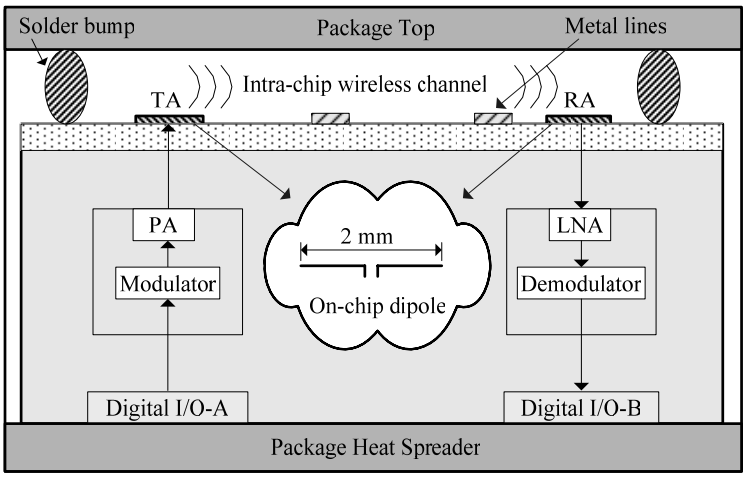


Figure 3.1: An intra-chip wireless interconnect system for data communication.

An intra-chip wireless interconnect system using an on-chip antenna pair for point to point data communication is shown in Fig. 3.1 [17]. Note that the transmitter comprises a modulator, a power amplifier (PA), and a transmit antenna (TA); while

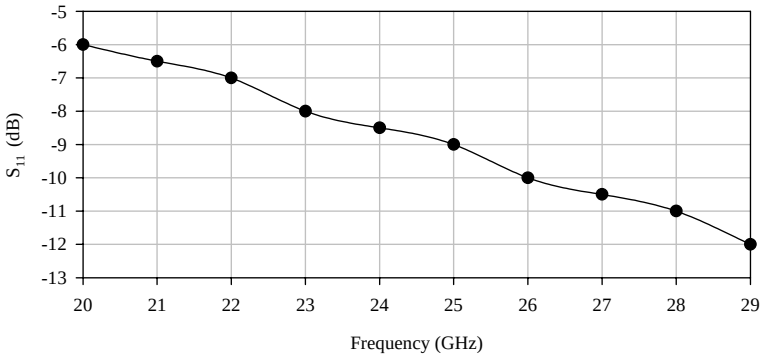
the receiver comprises a receiver antenna (RA), a low noise amplifier (LNA), and a demodulator. Also note that the wireless interconnect system features a unique intra-chip wireless channel.

The linear on-chip dipole antenna pair, each the mirror image of the other, is used for TA and RA. The antennas are 2 μm thick, 10 μm wide and 2 mm long. The dipole-balanced structure ensures an adequate rejection of noise and interfering signal travelling through the common silicon substrate. They are fabricated on a 3-μm thick oxide layer on a 20-Ω.cm silicon substrate of 633-μm thickness. The S_{11} of the on-chip dipole antenna versus frequency is shown in Fig. 3.2 (a). It is evident that S_{11} is lower than -6 dB from 20 to 29 GHz indicating an acceptable matching to a 50-Ω source. To measure the transmission performance between TA and RA, the antenna transmission gain (*TG*) is derived using *Friis transmission formula*

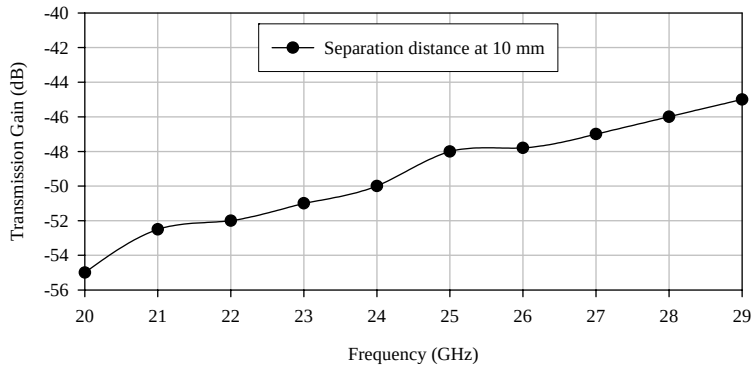
$$TG = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)} \tag{3.1}$$

TG is the ratio of the received power to the transmitted power when both on-chip antennas are conjugately matched. The average value of *TG* can be accurately obtained from an on-chip measurement or from a full wave electromagnetic simulator. Fig. 3.2 (b) and (c) show the average value of *TG* for the on-chip dipole antenna pair. It is found that the average value of *TG* increases with the frequency and decreases with the distance. It is -48 dB at 25 GHz at a separation distance of 10 mm.

3.1 System Description



(a)



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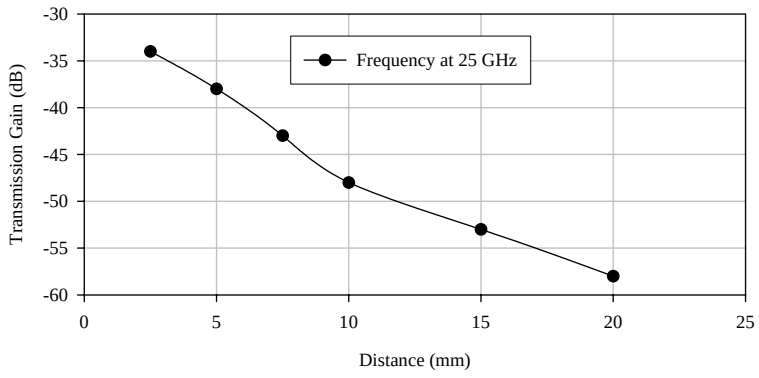


(c)

Figure 3.2: On-chip dipole antenna pair characterization: (a) S_{11}, (b) average TG versus frequency, and (c) average TG versus distance.

3.1 System Description

The system features a unique intra-chip wireless channel. The characteristics of this channel are analyzed around 15 GHz in [17] and 25 GHz in [21]. It is concluded that the channel can be regarded as a non-dispersive Rician fading channel for the data rate 2-5 Gbps considered here. The conclusion is based on the imperfect dielectric waveguide characteristics due to the intra-chip wireless channel not being designed primarily as a wave guiding structure, which supports the transmission of multi hybrid electromagnetic modes. This is particularly true in a package chip environment where exist a large number of metal lines and solder bumps. They will cause mode conversion and increase transmission loss. Similar to radio propagation via multipaths in an indoor wireless channel, radio signal transmission through multimodes in the intra-chip wireless channel exhibits fluctuations while still keep the dominant mode as analyzed in [17]. As a result, signal fluctuations over the intra-chip wireless channel follow a Rician distribution. This treatment of the intra-chip wireless channel as the Rician fading channel also agrees with the on-chip measurements of the radio signal transmission from 5 to 26 GHz. The measurements reveal that the signal fade depth never exceeds 10 dB [13]. In addition, as for the dispersive characteristics of the wireless channel, time delay is calculated to be negligible for the data rate range of 2-5 Gbps of interest [17]. As analyzed in [17], through this non-dispersive Rician fading intra-chip wireless channel the transmitted signal will be only corrupted by the thermal noise and switching noise.

3.2 System Performance Evaluation

3.2.1 Methods to evaluate BER

Based on the assumption that the intra-chip wireless channel is a non-dispersive Rician fading channel, the system SNR and BER performance will be evaluated under the assumptions of perfect system synchronization and signal corruption from thermal and switching noise.

The thermal noise power spectral density (PSD) N_0 is obtained using the method presented in [17] as

$$N_0 = kT_0F = kT_0(\frac{T_{ant}}{T_0} + F_r) \tag{3.2}$$

where k is the Boltzman constant, T_0 is the reference temperature (typically taken as 290 K), T_{ant} is the antenna temperature (taken as 330K) [17], and F_r is the receiver noise figure. As shown, N_0 increases with F_r.

For our system that integrates both the analog radio front end and digital baseband processing circuits, the switching noise produced by the digital circuits may be significant and impact the receiver performance. The switching noise PSD S_0 has been analyzed in [21]. The measured switching noise was also found to be 10 dB lower than the thermal noise [66]. Based on this measurement result the switching noise PSD S_0 can be reasonably assumed to be either 10 or 5 dB lower than the thermal noise as denoted as T in the following BER calculation.

The average bit SNR at the receiver end is then given as follows

$$\Gamma_b = \frac{E_{rb}}{N_0 + S_0} \tag{3.3}$$

where E_{rb} is the received average energy per bit, calculated as

$$E_{rb} = (1 + \frac{1}{K}) \cdot E_{tb} \cdot TG \cdot G_r \cdot L_m \tag{3.4}$$

$$E_{tb} = \frac{P_t}{R_b} \tag{3.5}$$

where E_{tb} is the transmitted energy per bit, P_t is the transmitted power, R_b is the interconnect data rate, TG is the transmission gain of on-chip antennas. G_r is the gain of the receiver, L_m is the implementation margin that includes all kinds of marginal loss. K is the specular-to-random energy ratio of the Ricain distribution of intra-chip wireless channel, and $(1 + 1/K)$ is the modified parameter for the received energy in Rician fading channel.

Considering the Rician fading effect, the instantaneous bit SNR x become a variable following a probability density function $p(x)$ as shown in (3.6) [67], which is determined by K and the non-fading bit SNR Γ_b of (3.3).

$$p(x) = \frac{1+K}{\Gamma_b} \exp(-\frac{(1+K)x + K\Gamma_b}{\Gamma_b}) I_0(2\sqrt{\frac{K(1+K)x}{\Gamma_b}}) \quad x \geq 0 \tag{3.6}$$

The BER of our system is then obtained by averaging $P_{b|x}$, the BER at a specific value of x, over the entire range of x [68], that is

$$P_b = \int_0^{+\infty} P_{b|x}\, p(x) dx \tag{3.7}$$

3.2 System Performance Evaluation

It is well known that the accurate computation of the above infinity integration in (3.7) is rather difficult. To circumvent this difficulty, we propose to use the following two formulas to transform the infinite integration to a finite one. The first is (3.8), which can be easily proved by using [69, eq. (7.4.11)] and making a variable change

$$\frac{1}{\pi}\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} e^{-r\sec^2\theta x}d\theta = erfc(\sqrt{rx}) \tag{3.8}$$

and the second is (3.9)

$$\int_0^{+\infty} e^{-\alpha x} I_0(2\sqrt{\beta x})dx = \frac{1}{\alpha}e^{\frac{\beta}{\alpha}} \tag{3.9}$$

which can be found from integration tables [70]. We finally get the BER expressions that are precise and easily computed numerically as follows, where $k = log_2 M$ is the number of bits per symbol.

$$P_{b,MFSK}(K,\Gamma_b) = \frac{2^{k-1}}{2^k-1}\cdot\frac{1}{M}\cdot\sum_{i=2}^{M}(-1)^i\begin{pmatrix} M \\ i \end{pmatrix}\frac{1+K}{1+K+(1-\frac{1}{i})\cdot k\Gamma_b}\cdot \exp\left(-\frac{K(1-\frac{1}{i})}{\frac{1+K}{k\Gamma_b}+1-\frac{1}{i}}\right) \tag{3.10}$$

$$P_{b,MDPSK}(K,\Gamma_b) = \frac{1}{k}\cdot\frac{\sin\frac{\pi}{M}}{2\pi}\cdot\frac{1+K}{k\cdot\Gamma_b}\cdot \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}}\frac{\exp\left(-\frac{K\left(1-\cos\frac{\pi}{M}\cos\theta\right)}{\frac{1+K}{k\cdot\Gamma_b}+1-\cos\frac{\pi}{M}\cos\theta}\right)}{\left(1-\cos\frac{\pi}{M}\cos\theta\right)\left(\frac{1+K}{k\cdot\Gamma_b}+1-\cos\frac{\pi}{M}\cos\theta\right)}d\theta \tag{3.11}$$

$$P_b(K,\Gamma_b) = a\cdot\frac{1}{k\pi}\cdot\frac{1+K}{\Gamma_b}\cdot\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}}\frac{1}{rk\sec^2\theta+\frac{1+K}{\Gamma_b}}\cdot\exp\left(\frac{-Krk\sec^2\theta}{rk\sec^2\theta+\frac{1+K}{\Gamma_b}}\right)d\theta \tag{3.12}$$

(3.12) is applied to the Gray coded coherent MASK, MPSK, MQAM, GMSK, and MSK with parameters a and r shown in Table 3.1 [71]. It should be noted that (3.12) can be applied to the $P_{b|x}$ with the general form as follows

$$P_{b|x} = a \cdot erfc(\sqrt{r \cdot x}) \qquad a, r > 0 \tag{3.13}$$

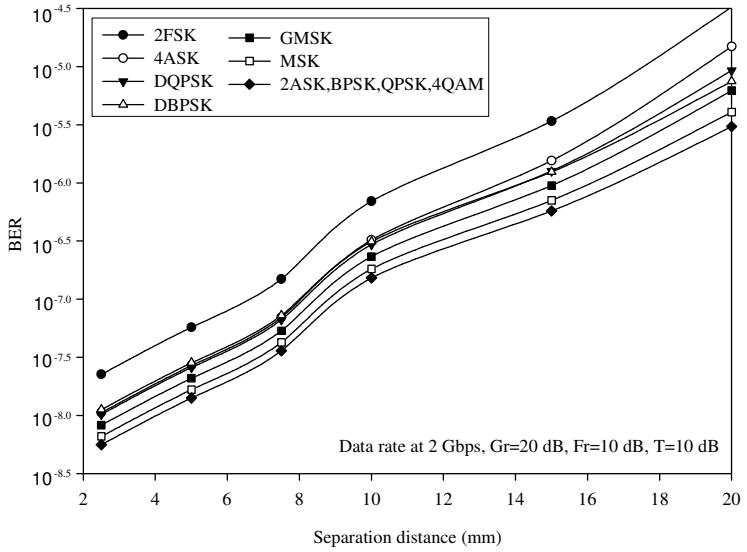
	MASK	MPSK	MQAM	GMSK (BT = 0.25)	MSK
a	$\frac{(M-1)}{M}$	$\begin{cases} 0.5 & M = 2 \\ 1 & M \neq 2 \end{cases}$	$\frac{2(\sqrt{M}-1)}{\sqrt{M}}$	0.5	0.5
r	$\frac{3}{M^2-1}$	$\sin^2(\pi/M)$	$\frac{3}{2(M-1)}$	0.68	0.85

Table 3.1: Parameters a and r in eq. (3.12) for Gray coded coherent MASK, MPSK, MQAM, GMSK, and MSK.

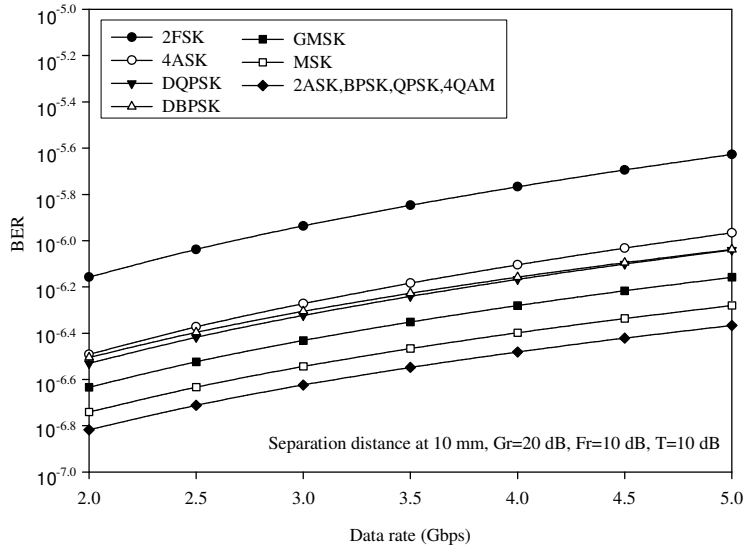
3.2.2 System BER performance

In BER calculation, F_r is assumed to be 10 dB or 15 dB at 25 GHz, which is supported by a recent study of CMOS implementation of a broadband software radio [21]. The switching noise is assumed to be T = 10 dB or T = 5 dB lower than the thermal noise according to the measured result [66]. L_m = $-$13 dB, including the loss of TG due to the inference structures between the TA and RA as well as the kinds of mismatch loss [66]. P_t = 0 dBm, K = 10 dB, and G_r is 20 dB or 15 dB. Fig. 3.3 shows the BER performance of different modulation schemes versus the separation distance and data rate at 25 GHz with the according parameters. As expected, for all modulation schemes their BER performance degrades with separation distance and data rate. It is

found that among simulated modulation schemes FSK shows the worst performance and (2ASK, BPSK, QPSK, 4QAM) shows the same best performance.



(a)



(b)

Figure 3.3: BER: (a) versus distance and (b) versus data rate.

In practice, factors of implementation complexity and power efficiency must be both considered for modulation schemes. i.e., as for the noncoherent 2FSK, with the

worst BER performance but easy to be implemented, it can be one of the candidates for intra-chip wireless data communication; as for the coherent BPSK, with the best BER performance but not feasible to realize the perfect synchronization for demodulation, especially in a fading intra-chip channel, it may not be a good scheme to be used in intra-chip wireless communication; as for DBPSK, it may be an attractive technique because of its simplicity of noncoherent demodulation and relatively better power efficiency.

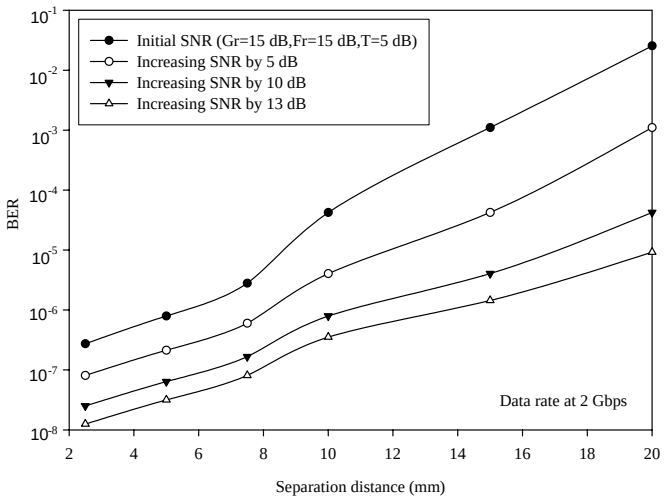


Figure 3.4: Feasibility study of FSK in terms of BER performance.

Provided that we choose 2FSK for its simplicity in implementation, the feasibility in terms of BER performance is studied in Fig. 3.4. We choose the initial parameters, that is P_t = 0 dBm, L_m = $-$13 dB, G_r = 15 dB, F_r = 15 dB, T = 5 dB. Using the initial parameters, we get BER $> 10^{-2}$ at 20 mm distance to achieve 2 Gbps. When we increase the SNR by 5 dB, the BER decreases to about 10^{-3}. When we further

increase the SNR by 13 dB, the BER decreases to about 10^{-5}. The increase of 13 dB in SNR budget is reasonable to be obtained. This can be achieved by exploiting the potentials of all parameters, namely, increasing the transmitted power P_t, receiver gain G_r and transmission gain TG as well as decreasing the inference structures loss in L_m and receiver noise figure F_r. Especially, TG has the potential to be improved by up to 10 dB using new process as reported in [38]. Also, the initial transmitted power of 0 dBm can be further increased to a value at which power consumption and generated extra heat cause no harm to the system realization. Finally, from the above analysis for 2FSK which has the poorest BER performance among the modulation schemes, namely, (2ASK, BPSK, QPSK, 4QAM), MSK, GMSK, DBPSK, DQPSK, 4ASK, and 2FSK, it is concluded that a high data rate at 2 Gbps with a low BER $< 10^{-5}$ up to a interconnect distance of 2 cm is achievable for all these modulation schemes under the reasonable SNR budget.

Chapter 4

On-Chip Antennas for Intra-Chip Wireless Interconnects

On-chip antennas for intra-chip wireless interconnects are studied, including on-chip dipole antennas in section 4.1, on-chip 60-GHz inverted-F and quasi-Yagi antennas in section 4.2, and on-chip monopoles in section 4.3. A novel intra-chip wireless interconnect system using on-chip meander monopole antennas and UWB radios that operate in 22-29 GHz is finally studied in section 4.4.

4.1 On-Chip Dipole Antenna Pair

4.1.1 Transmission theory

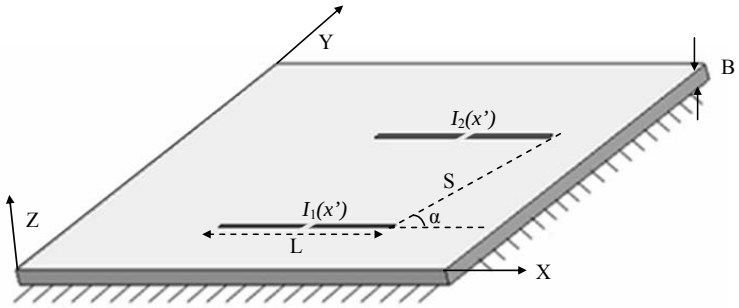


Figure 4.1: On-chip dipole antenna pair geometry.

Fig. 4.1 shows the simple geometry of the dipole antenna pair with vertical sep-

aration distance of S. The pair is on the surface of the grounded silicon substrate with thickness B and relative permittivity of ε_r. The on-chip dipoles are of length L and width a. It is assumed that the width is very small as compared to the free-space wavelength ($a \ll \lambda$), and therefore the thin-wire approximation can be used.

In the cylindrical coordinates, the components of the field in the air (z $\geq$ 0) generated by a horizontal on-chip dipole on the same substrate as shown in Fig. 4.1 with unit electric moment are shown as follows when $1 \leq f \leq 100$ GHz [72].

$$E_{0\rho}(\rho,\phi,z) = \frac{\omega\mu_0}{2\pi k_0}\cos\phi e^{ik_0 r}\left\{\begin{array}{l} \varepsilon\left(\frac{z}{r}\right)\left(\frac{ik_0}{r}-\frac{1}{r^2}\right)-\varepsilon^2 \\ \left[\frac{ik_0}{r}-\frac{1}{r^2}-\frac{i}{k_0 r^3}-k_0^2\varepsilon\left(\frac{r}{\rho}\right)\left(\frac{\pi}{k_0 r}\right)^{1/2}e^{-iP}F(P)\right]\end{array}\right\} \tag{4.1}$$

$$E_{0\phi}(\rho,\phi,z) = \frac{\omega\mu_0}{2\pi k_0}\sin\phi e^{ik_0 r}\left\{\begin{array}{l} \varepsilon\left(\frac{z}{r}\right)\left(\frac{ik_0}{r}-\frac{1}{r^2}\right) \\ -\varepsilon^2\left[\begin{array}{l}\frac{2}{r^2}+\frac{2i}{k_0 r^3}+\left(\frac{z}{r}\right)^2\left(\frac{ik_0}{r}-\frac{3}{r^2}-\frac{3i}{k_0 r^3}\right) \\ +ik_0\varepsilon\left(\frac{r^2}{\rho^3}\right)\left(\frac{\pi}{k_0 r}\right)^{1/2}e^{-iP}F(P)\end{array}\right]\end{array}\right\} \tag{4.2}$$

$$E_{0z}(\rho,\phi,z) = -\frac{\omega\mu_0\varepsilon}{2\pi k_0}\cos\phi e^{ik_0 r}\left[\left(\frac{\rho}{r}\right)\left(\frac{ik_0}{r}-\frac{1}{r^2}\right)-k_0^2\varepsilon\left(\frac{\pi}{k_0 r}\right)^{1/2}e^{-iP}F(P)\right] \tag{4.3}$$

$$B_{0\rho}(\rho,\phi,z) = -\frac{\mu_0\varepsilon}{2\pi}\sin\phi e^{ik_0 r}\left[\begin{array}{l}\frac{2}{r^2}+\frac{2i}{k_0 r^3}+\left(\frac{z}{r}\right)^2\left(\frac{ik_0}{r}-\frac{3}{r^2}-\frac{3i}{k_0 r^3}\right) \\ +ik_0\varepsilon\left(\frac{r^2}{\rho^3}\right)\left(\frac{\pi}{k_0 r}\right)^{1/2}e^{-iP}F(P)\end{array}\right] \tag{4.4}$$

$$B_{0\phi}(\rho,\phi,z) = \frac{\mu_0\varepsilon}{2\pi}\cos\phi e^{ik_0 r}\left[\frac{ik_0}{r}-\frac{1}{r^2}-\frac{i}{k_0 r^3}-k_0^2\varepsilon\left(\frac{r}{\rho}\right)\left(\frac{\pi}{k_0 r}\right)^{1/2}e^{-iP}F(P)\right] \tag{4.5}$$

$$B_{0z}(\rho,\phi,z) = \frac{\mu_0}{2\pi}\sin\phi e^{ik_0 r}\left\{\begin{array}{l}\varepsilon\left(\frac{\rho z}{r^2}\right)\left(\frac{ik_0}{r}-\frac{3}{r^2}-\frac{3i}{k_0 r^3}\right)-\varepsilon^2\left(\frac{\rho}{r}\right) \\ \left[\frac{1}{r^2}+\frac{3i}{k_0 r^3}-\frac{3}{k_0^2 r^4}+\frac{z^2}{r^2}\left(\frac{ik_0}{r}-\frac{6}{r^2}-\frac{15i}{k_0 r^3}\right)\right]\end{array}\right\} \tag{4.6}$$

where

$$r = \left(\rho^2 + z^2\right)^{1/2} \tag{4.7}$$

$$\varepsilon = -ik_0 B \tag{4.8}$$

$$P = \frac{k_0 r}{2}\left(\frac{\varepsilon r + z}{\rho}\right)^2 \tag{4.9}$$

$$F(P) = \frac{1+i}{2} - \int_0^P \frac{e^{it}}{(2\pi t)^{1/2}} dt \tag{4.10}$$

where the integral in $F(P)$ is the well-known and tabulated Fresnel integral.

Of particular interest are much simpler formulas when the point of observation is on the surface of the dielectric. With z = 0, the formulas are

$$E_{0\rho}(\rho,\phi,0) = -\frac{\omega\mu_0\varepsilon^2}{2\pi k_0}\cos\phi e^{ik_0\rho}\left[\frac{ik_0}{\rho} - \frac{1}{\rho^2} - \frac{i}{k_0\rho^3} - k_0^2\varepsilon\left(\frac{\pi}{k_0\rho}\right)^{1/2} e^{-iP}F(P)\right] \tag{4.11}$$

$$E_{0\phi}(\rho,\phi,0) = -\frac{\omega\mu_0\varepsilon^2}{2\pi k_0}\sin\phi e^{ik_0\rho}\left[\frac{2}{\rho^2} + \frac{2i}{k_0\rho^3} + \frac{ik_0\varepsilon}{\rho}\left(\frac{\pi}{k_0\rho}\right)^{1/2} e^{-iP}F(P)\right] \tag{4.12}$$

$$E_{0z}(\rho,\phi,0) = -\frac{\omega\mu_0\varepsilon}{2\pi k_0}\cos\phi e^{ik_0\rho}\left[\frac{ik_0}{\rho} - \frac{1}{\rho^2} - k_0^2\varepsilon\left(\frac{\pi}{k_0\rho}\right)^{1/2} e^{-iP}F(P)\right] \tag{4.13}$$

$$B_{0\rho}(\rho,\phi,0) = -\frac{\mu_0\varepsilon}{2\pi}\sin\phi e^{ik_0\rho}\left[\frac{2}{\rho^2} + \frac{2i}{k_0\rho^3} + \frac{ik_0\varepsilon}{\rho}\left(\frac{\pi}{k_0\rho}\right)^{1/2} e^{-iP}F(P)\right] \tag{4.14}$$

$$B_{0\phi}(\rho,\phi,0) = \frac{\mu_0\varepsilon}{2\pi}\cos\phi e^{ik_0\rho}\left[\frac{ik_0}{\rho} - \frac{1}{\rho^2} - \frac{i}{k_0\rho^3} - k_0^2\varepsilon\left(\frac{\pi}{k_0\rho}\right)^{1/2} e^{-iP}F(P)\right] \tag{4.15}$$

$$B_{0z}(\rho,\phi,0) = -\frac{\mu_0\varepsilon^2}{2\pi}\sin\phi e^{ik_0\rho}\left(\frac{1}{\rho^2} + \frac{3i}{k_0\rho^3} - \frac{3}{k_0^2\rho^4}\right) \tag{4.16}$$

where $P = (k_0\rho\varepsilon^2)/2$.

The fields excited by an on-chip dipole along the air dielectric interface can be

decomposed into the following components: a space wave ($1/\rho$ dependence), a higher order wave ($1/\rho^2$ dependence), a surface wave ($1/\rho^{1/2}$ dependence), and leaky waves ($\exp(-\lambda\rho)/\rho^{1/2}$ dependence) [74]. As ρ increases the surface waves constitute the dominant contribution because of their cylindrical wave character $\rho^{1/2}$ as opposed to the spherical behavior of the space wave [73].

For the dipole pair as shown in Fig. 4.1, its current distribution can be expressed as

$$J(x', y') = [I_1(x')\delta(y')P_1 + I_2(x')\delta(y' - S)P_2]\delta(z' - B)\hat{x} \tag{4.17}$$

where $I_1(x')$, $I_2(x')$ are the unknown currents and P_1, P_2 are two unit pulse functions which are zero everywhere except over the lengths of the dipoles L_1, L_2, respectively. The axial component of the electric field E_x is given at any point on the substrate by [73]

$$E_x = \int_{L_1, y'=0} I_1(x') \left[k^2 \Pi_x + \frac{\partial^2 \Pi_x}{\partial x^2} + \frac{\partial^2 \Pi_z}{\partial x \partial z} \right] dx' + \int_{L_2, y'=S} I_2(x') \left[k^2 \Pi_x + \frac{\partial^2 \Pi_x}{\partial x^2} + \frac{\partial^2 \Pi_z}{\partial x \partial z} \right] dx' \tag{4.18}$$

where the components of the Hertz vector Π_x and Π_z are given by

$$\Pi_x = \lim_{z \to B} 2K \int_0^\infty J_0(\lambda\rho) e^{-\mu(z-B)} \frac{\lambda d\lambda}{D_e(\lambda)} \tag{4.19}$$

$$\Pi_z = \lim_{z \to B} 2K(1 - \varepsilon_r) \int_0^\infty J_1(\lambda\rho) e^{-\mu(z-B)} \frac{\lambda^2 \cos\alpha d\lambda}{D_e(\lambda) D_m(\lambda)} \tag{4.20}$$

with

$$D_e(\lambda) = \mu + \mu_e \coth \mu_e B \tag{4.21}$$

$$D_m(\lambda) = \mu\varepsilon_r + \mu_e \tanh \mu_e B \tag{4.22}$$

$k = (2\pi)/\lambda$, $\mu = \sqrt{\lambda^2 - k^2}$, $\mu_e = \sqrt{\lambda^2 - \varepsilon_r k^2}$, $\rho = \sqrt{(x-x')^2 + (y-y')^2}$, and $K = -i/(4\pi\varepsilon_0\omega)$.

The dipoles are divided into N_1 and N_2 subsections respectively to solve for $I_1(x')$ and $I_2(x')$. For numerical convergence, sinusoidal functions have been chosen as expansion and testing functions. In addition, the appropriate principal value integration of the Sommerfeld-type integrals along the real axis is adopted. $I_1(x')$, $I_2(x')$ are then obtained by the matrix form [V]=[Z][I] as below with $M = N_1 + N_2 - 2$.

$$\begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_M \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & \cdots & Z_{1M} \\ Z_{21} & Z_{22} & \cdots & Z_{2M} \\ \vdots & \ddots & & \vdots \\ Z_{M1} & Z_{M2} & \cdots & Z_{MM} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_M \end{bmatrix} \tag{4.23}$$

where I is related to the currents on the subsections and V to the electromagnetic excitation column. Depending on the feeding point, the corresponding excitation voltage is set to unity in the excitation column. By using the knowledge of the current distribution over the pair the mutual impedance Z_c between the two on-chip dipoles is then easily obtained as presented in [73].

With different value of α, the dipole pair can be in collinear (α = 0°/180°), broadside (α = 90°) or echelon configurations (α = others). The substrate thickness B and relative permittivity ε_r determine the number of the supported surface wave modes. The TE and TM modes are zeros of the factors $D_e(\lambda)$ and $D_m(\lambda)$, respectively. The

lowest order mode is TM mode with a component of electric field parallel to the direction of propagation.

For a single propagating TM mode, the pair launches the surface wave with maximum efficiency in the collinear configuration while with minimum efficiency in the broadside configuration. This is because the TM mode has a launching spatial pattern cosα as shown in (4.20). Therefore, for the single propagating mode, the mutual coupling in the broadside configuration will be mainly due to direct, high order and leaky waves excited by the antenna. While the mutual coupling in the collinear configuration will be mainly due to the TM surface wave excited by the antenna. The mutual coupling in the echelon configuration will be the intermediate state. Fig. 4.2 (a) and (b) shows the mutual impedance as a function of separation distance S in the broadside case, which is commonly used in the intra-chip communication for dipoles. The silicon substrate has ε_r = 11.9. As shown the rapid fall in mutual impedance for small separation ($S < 0.4\lambda_0$) confirms that the coupling is mainly due to the higher order modes, while for ($S > 0.8\lambda_0$) the space wave takes over. In the intermediate zone ($0.4\lambda_0 < S < 0.8\lambda_0$) the leaky wave modes are dominant. It is also found that the longer antenna has the larger mutual impedance in the small separation zone by comparing the Fig. 4.2 (a) for $L = 0.3\lambda_0$ with (b) for $L = 0.35\lambda_0$.

For two propagating modes, the TE mode surface wave will be excited and dominated in the coupling of the broadside configuration, while in the collinear configuration the dominant coupling will be still due to the TM mode. The mutual coupling in

the echelon configuration will be the intermediate state. Fig. 4.2 (c) shows the mutual impedance in the broadside case. It is found that mutual impedance oscillates with a period of $0.68\lambda_0$ which is very close to the wavelength of the TE mode of the surface waves of $0.673\lambda_0$. TE mode surface wave is dominant in this case. In addition, the rapid fall in mutual impedance for small separation shows the effect of the higher order modes.

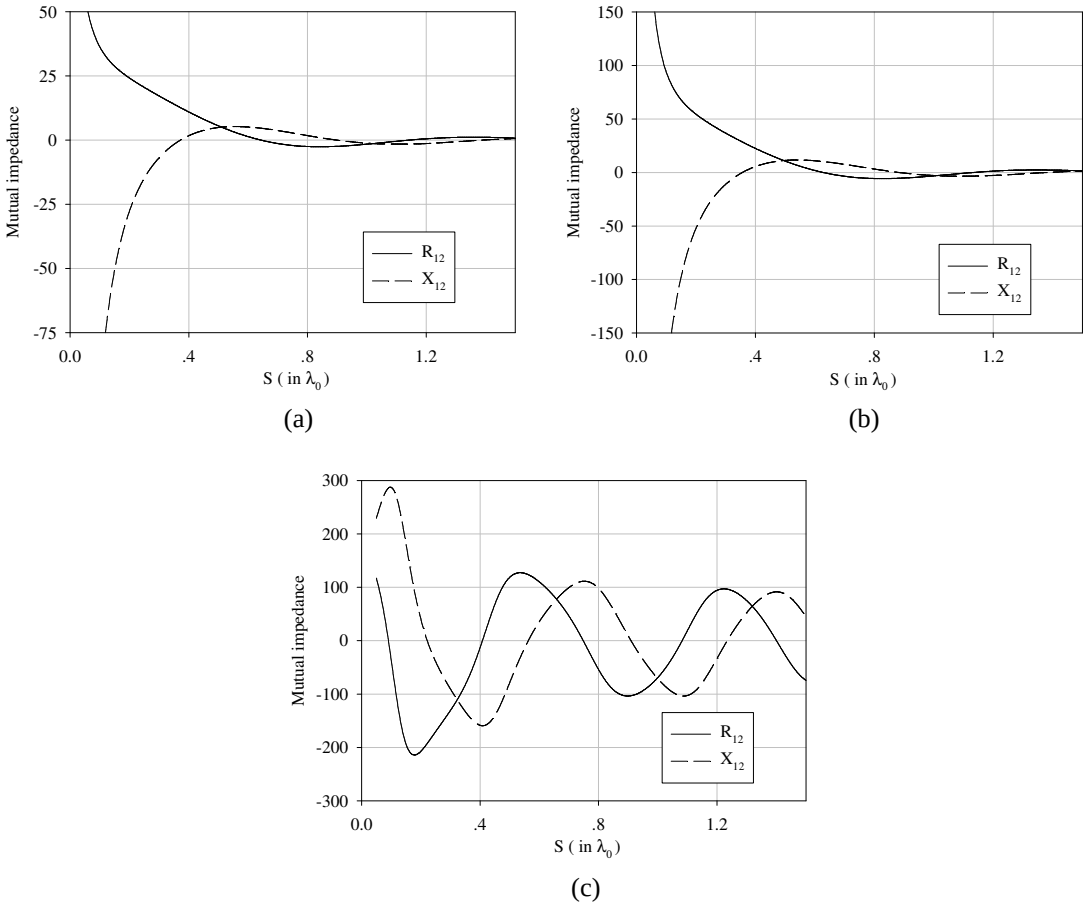
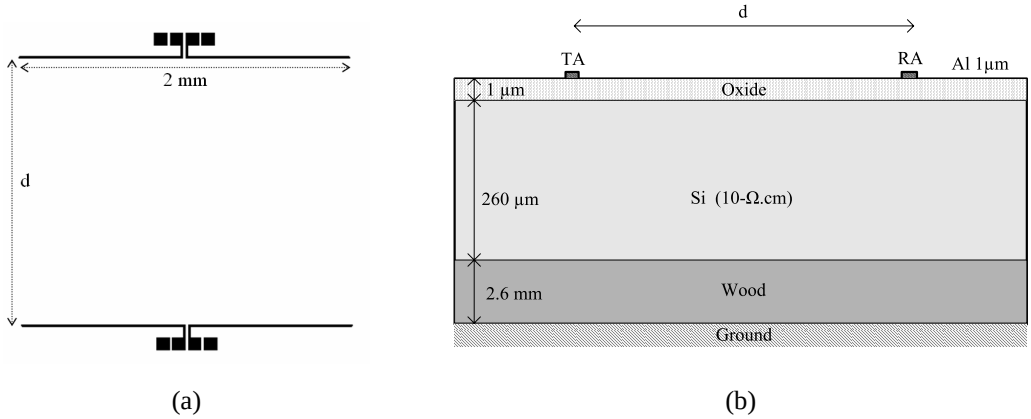


Figure 4.2: Mutual impedance between two broadside dipoles: (a) for a single propagating mode with B = $0.03\lambda_0$, ε_r = 11.9, and L = $0.3\lambda_0$, (b) for a single propagating mode with B = $0.03\lambda_0$, ε_r = 11.9, and L = $0.35\lambda_0$, and (c) for two propagating modes with B = 0.1016 λ_0, ε_r = 11.9, and L = 0.3 λ_0.

4.1.2 Simulation study



(a) (b)

Figure 4.3: On-chip dipole antenna pair: (a) layout and (b) cross-sectional view.

The simple analytical method is conducive to obtain the dipole transmission mechanism. However, it shows limit in analyzing the more complicated structure as shown in Fig. 4.3 for an on-chip dipole antenna pair with the separation distance of d. The axial length of the antenna is 2 mm. The test ground-signal-signal-ground (GSSG) pads are squares of 80 μm by 80 μm. The width of the line elements is 10 μm. Fig. 4.3 (b) shows the cross sectional view of the antenna pair. As shown, an oxide layer of thickness 1 μm is grown on the low resistivity silicon substrate (10 Ω.cm) of thickness 260 μm to increase isolation and an aluminum layer of thickness 1 μm is used to form the antennas. The block of wood (2.6 mm thick with ε_r = 2.15) is used to eliminate the effect of metal chuck of the probe station in accordance with the measurement set up condition in [39]. In this case we use the electromagnetic 2.5-D simulator Zeland IE3D to study the on-chip dipole antenna pair performance. It is based on the method of moments (MOM) and is quick and accurate to solve the planar dipole antenna pair

problem. Its features such as open box formulations and the differential MMIC port de-embedding scheme also make it efficient in simulation.

In the dipole antenna pair simulation, its performance with varied separation distance should be studied to investigate the interconnect potentials. In addition, one of challenges for on-chip antennas is the large loss due to low resistivity silicon substrate. It is the fundamental limitation of silicon operating at higher frequency. It becomes more serious as the frequency increases to millimeter-wave range. To improve the on-chip antenna transmission performance various techniques such as micromaching and proton implantation have been developed [33, 46]. The micromaching process removes the loss silicon substrate underneath the antenna radiating element, while the proton implantation increases significantly the resistivity of the silicon substrate underneath the antenna radiating element from 10 Ω.cm to 10^6 Ω.cm. Recently a BEOL process is adopted to combat substrate loss at Singapore Institute of Microelectronics for RF CMOS passives to fabricate the on-chip antennas for 60-GHz radios. The effect of these processes on the on-chip dipole pair performance should be simulated and their potentials to improve the antenna pair transmission performance should be investigated. Furthermore, inside an SOC or a ULSI there are many metal structures such as bus lines or power lines. Inevitably, they occur in between the transmitting and receiving antennas and certainly affect the transmission performance. The effects of these interference structures on the antenna pair performance should be investigated. In what follows the factors mentioned above with their effects on dipole pair performance will be simulated and analyzed.

4.1 On-Chip Dipole Antenna Pair

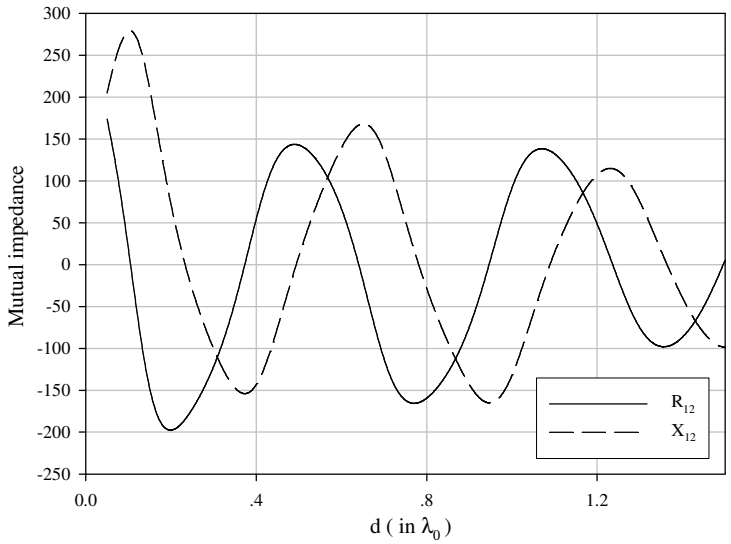


Figure 4.4: Simulated mutual impedance.

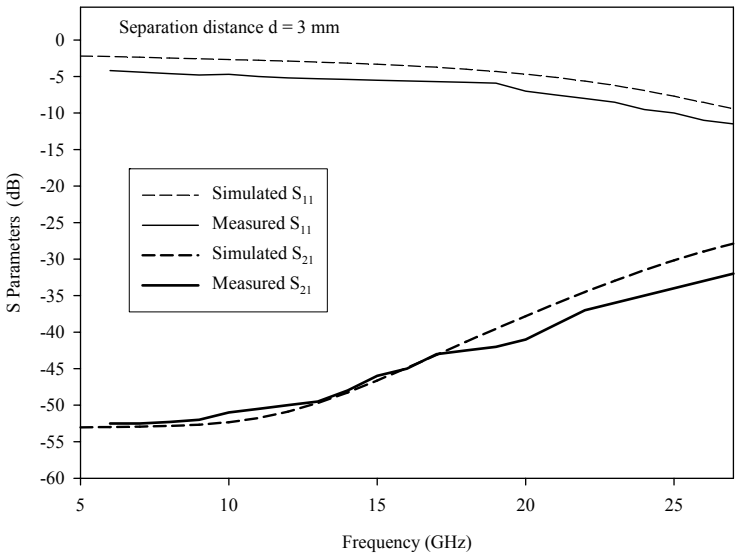


Figure 4.5: Simulated and measured S_{11} and S_{21}.

Fig. 4.4 shows the simulated mutual impedance. It is found that mutual impedance oscillates with a period. Its characteristics are very similar to Fig. 4.2 (c). The surface wave is expected to be dominant in this case. In addition, the rapid fall in mutual impedance for small separation shows the effect of the higher order modes. This plot is conducive to understand the dipole transmission mechanism. Fig. 4.5 compares the simulated S parameters with the measured ones from [39]. The separation distance of the dipole antenna pair is 3 mm. It is seen that the measured and simulated results agree well to some extent. It is noted that in S_{21} simulation the meshing frequency can greatly influence the simulation results. Therefore the point by point frequency meshing method is used in IE3D simulation.

Fig. 4.6 (a) shows the effect of the separation distance d on the dipole antenna pair performance. It is found that S_{11} results are insensitive to the separation distance of the antenna pair. They remain unchanged with d varied from 2 mm to 10 mm. It is also evident that S_{21} results decrease with the distance as expected.

Fig. 4.6 (b) shows the effect of the process on the dipole antenna pair performance. First, the simplified BEOL process is used to overcome the substrate loss. The oxide thickness is increased to 20 μm according to this process in our simulation. Compared with the original antenna pair performance, the S_{11} value becomes larger and the S_{21} performance becomes worse. It is concluded that using BEOL can not always increase the transmission ability and the design should be optimized to take the advantage of this process. Second, the proton implantation effect is studied. The 5-KΩ.cm high re-

4.1 On-Chip Dipole Antenna Pair

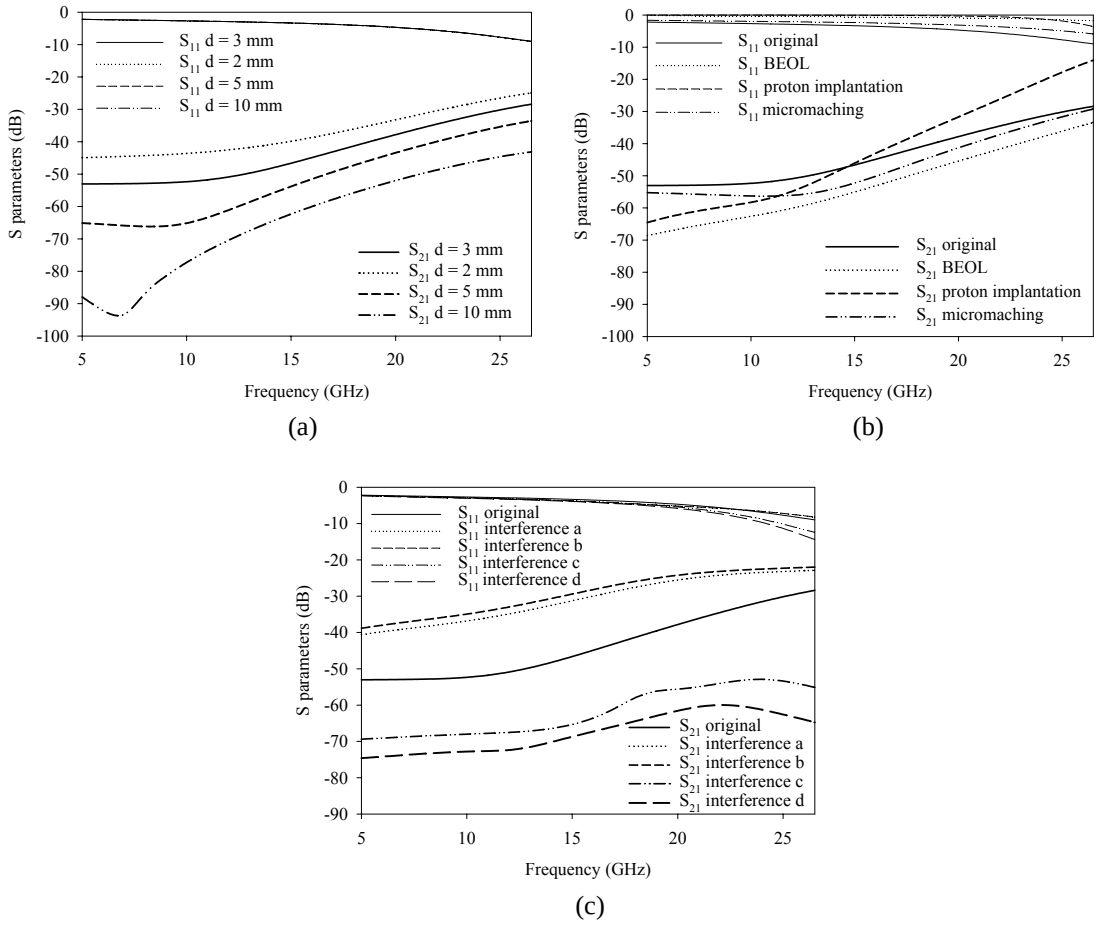


Figure 4.6: Simulated S_{11} and S_{21}: (a) effect of distance, (b) effect of the process, and (c) effect of the interference structures.

sistivity substrate is used to substitute the original substrate of 10-Ω.cm low resistivity. It is found that the S_{21} performance increases quickly in the higher frequency range as shown in Fig. 4.6 (b). This agrees well with the measured characteristics in [40]. Third, the micromaching technique is also studied. The substrate thickness is reduced from the original 260 μm to 100 μm. It is found that the S_{21} performance using micromaching shows no advantages. It is concluded that the design should be optimized to take the advantage of this process.

Fig. 4.6 (c) shows the effect of the interference structures (Fig. 4.7) on the dipole antenna pair performance. It is found that the S_{11} results are changed for all four interference structures. It can be seen that the interference structures a and b can greatly improve the S_{21}, behaving like transmission lines. While the interference structures c and d decrease the S_{21} performance. This characteristic can be used wisely to improve the antenna gain performance as suggested in [75].

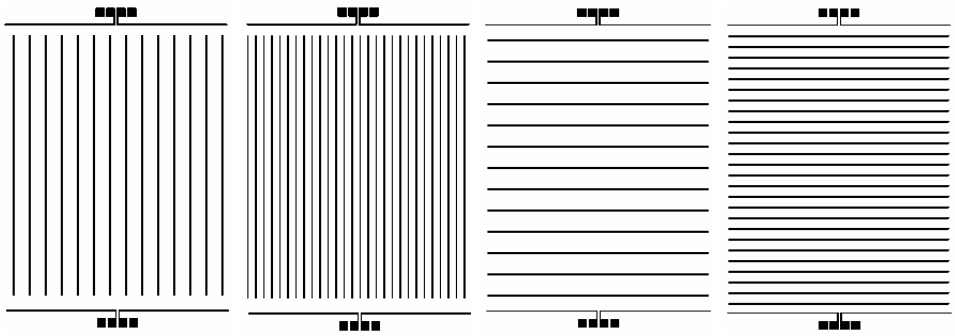


Figure 4.7: Interference structures layout with separation distance d = 3 mm.

4.2 On-Chip 60-GHz Inverted-F and Quasi-Yagi Antennas

Antennas for 60 GHz applications should feature the following properties: 1) low fabrication cost and readily amenable to mass production, 2) light weight and small size, 3) high efficiency and broad bandwidth, and 4) integratable with other radio front-end circuitry [22]. Most antennas on silicon substrates are microstrip antennas, planar inverted-F antennas and Yagi-Uda antennas [34, 36, 43]. Considering the potential that the microstrip patch and the planar element may cause micro fracture to the silicon

substrate, we chose linear inverted-F and quasi-Yagi antennas for our work.

The linear inverted-F antenna consists of a horizontal line, a short-circuited vertical line, and a signal-driven vertical line. It is well known that the inverted-F antenna originated from the modification of the inverted-L antenna. The modification is very important because the input impedance of an inverted-F antenna can be arranged to have an appropriate value to match the source impedance, without using any additional circuit between the antenna and the source. An inviting property of the inverted-F antenna is a radiation with both vertical and horizontal polarizations. This would be very useful for WPAN applications. In a WPAN environment, the radio signal has random fluctuating distributions, compounding of the vertical polarization and the horizontal polarization can provide a diversity effect and improve the reception. Another advantage of the inverted-F antenna is its small vertical dimension, which enables it to be favourable for on-chip integration as it can be designed at one of chips' edges. Taking these facts into account it can be said that the inverted-F antenna is an especially attractive antenna for WPAN applications.

The Yagi-Uda antenna has found wide applications in the HF-UHF band. For frequencies up to millimeter-wave range, microstrip-fed quasi-Yagi antennas have been built on conventional dielectric substrate (ε_r = 9.8) [76]. The Yagi-Uda is based on the principles of parasitic elements that are not directly fed by an energy source. These elements focus the radiation pattern using currents induced in them by radiation from the driven element. According to their length and spacing from the driven element, the

parasitic elements become either directors or reflectors. Directors are shorter than the driven element and result in the radiation pattern being sharply focused in the direction of the directors. Reflectors are longer than the driven element and result in a radiation pattern directed away from them. The overall result is an endfire radiation pattern, which is an attractive property for point-to-point radio communications [43].

4.2.1 Design

The inverted-F and quasi-Yagi antennas were designed using the electromagnetic simulator Zeland IE3D.

A. Design of on-chip inverted-F antenna

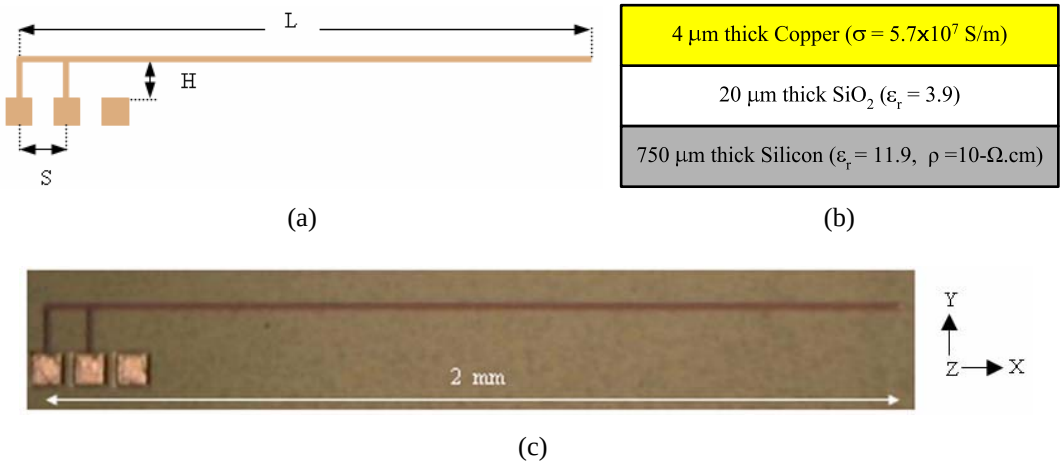


Figure 4.8: On-chip inverted-F antenna: (a) layout, (b) cross sectional view, and (c) top view photograph.

The layout, cross-sectional view, and top view photograph of the on-chip inverted-F antenna are illustrated in Fig. 4.8. The test ground-signal-ground (GSG) pads are squares of 80 μm by 80 μm. The width of the line elements is 10 μm. Given the

technology, the design parameters are L, H, and S. The effective length $(L + H)$ controls the frequency of resonance, while the separation distance S can adjust the antenna impedance to match to the source. To ease our design H and S are fixed as 100 μm, respectively.

The simulated S_{11} of the inverted-F antenna for the parameter L variation is shown in Fig. 4.9. It is evident from the figure that when L reaches 2 mm, the return loss drops to 17 dB indicating good matching to the 50-Ω source at 60 GHz. We know that for conventional inverted-F antenna the resonance occurs at

$$(L + H) = n\lambda/4 \tag{4.24}$$

where λ is the wavelength and n is the mode order. At 60 GHz, the wavelength in CMOS silicon substrate of low resistivity of Fig. 4.8 (b) is about 2.2 mm. Thus, it seems that $(L + H)$ should be 0.55 mm for the first-order mode to resonate at 60 GHz. However, our simulation shows in Fig. 4.9 that the resonance does not occur for the first-order mode with this length. The resonance occurs near 60 GHz when $(L + H)$ reaches 2.1 mm, which indicates that the fourth-order mode is excited.

The simulated radiation patterns of the inverted-F antenna in the azimuth and elevation planes at 60 GHz are shown in Fig. 4.10, where L, S, and H are taken as 2 mm, 100 μm, and 100 μm, respectively. In the azimuth plane: as expected, the maximum radiation occurs in the 0° direction for the co-polarization radiation and the radiation is stronger in the upper hemisphere. The cross-polarization radiation is much

weaker than the co-polarization radiation, for example, in the 0° direction the cross-polarization radiation is 32 dB weaker. In the elevation plane: the radiation patterns, both co- and cross-polarizations can only be obtained for the upper hemisphere because the electromagnetic model assumes infinite extension of the ground plane. The co-polarization radiation pattern becomes asymmetric because of the shorted-circuit line element. The radiation gets stronger in the directions away from the shorted-circuit line element. The cross-polarization radiation is stronger as compared with that in the azimuth plane. The cross-polarization radiation is only about 9 dB weaker than the co-polarization radiation in the 0° direction in the elevation plane.

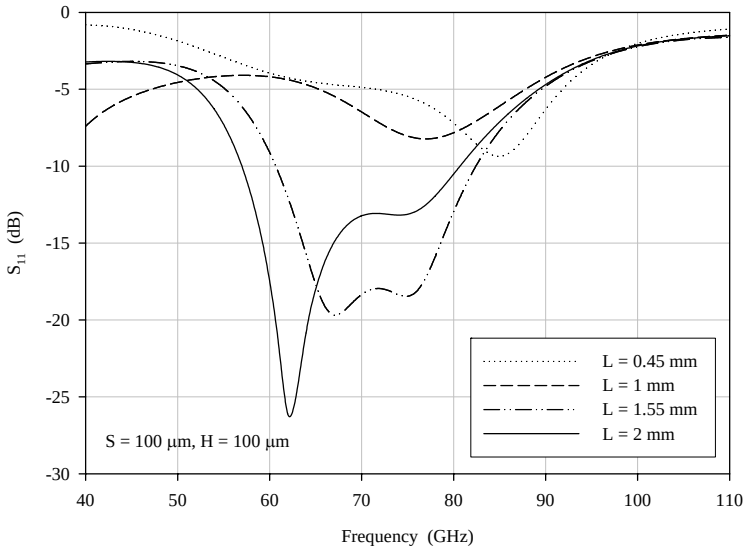


Figure 4.9: S_{11} of the inverted-F antenna for L variation.

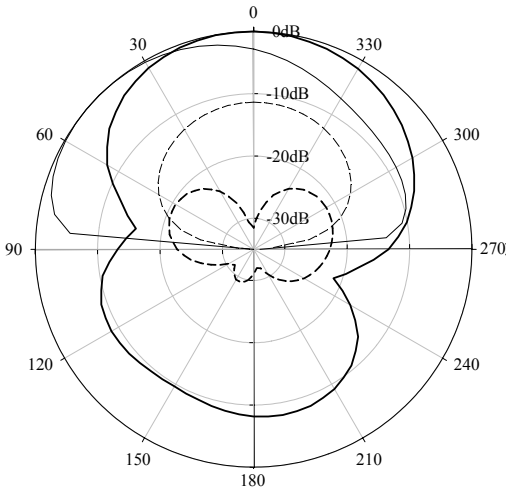
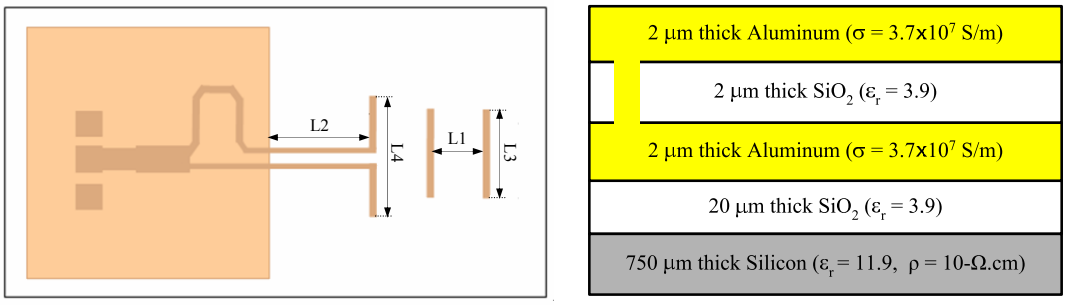


Figure 4.10: Radiation patterns of the inverted-F antenna with solid lines for co-polarization components, short dash lines for cross-polarization components, normal lines for elevation plane (ϕ = 0°), and thicker lines for azimuth plane (θ = 85°).

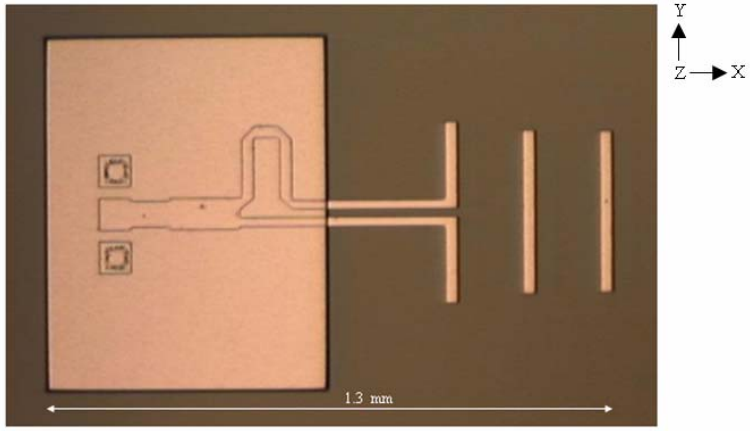
B. Design of quasi-Yagi antenna

Fig. 4.11 shows the layout, cross-sectional view, and top view photograph of the on-chip quasi-Yagi antenna. It consists of one driver, two directors, and a truncated ground plane that acts as reflector. The antenna is fed by a microstrip line. It should be mentioned that the ground-signal-ground (GSG) probes require the testing pads being squares of 80 μm by 80 μm with a pitch of 100 μm. As a result, the impedance between the signal pad and the ground plane with 2-μm thick silicon oxide separation is small. This small impedance of a few ohms avoids the short circuit and a part of the signal reach the antenna to radiate.

It is known that the quasi-Yagi antenna has significantly more gain and a better-controlled front-to-back ratio when it employs at least three elements. We chose four elements for our design [76]. As shown in Fig. 4.11 (a), parameters considered to



(a) (b)



(c)

Figure 4.11: On-chip quasi-Yagi antenna: (a) layout, (b) cross sectional view, and (c) top view photograph.

optimize the design are $L1$, $L2$, $L3$, and $L4$. Parameter $L1$ is the distance between the driver and the first director, which equals the distance between the first director and the second director to simplify the design. Parameter $L2$ is the distance between the driver and the ground plane, parameter $L3$ is the length of the director, and parameter $L4$ is the length of the driver. The optimized parameters are $L1$ = 146 μm, $L2$ = 270 μm, $L3$ = 382 μm, and $L4$ = 426 μm. It is found that the return loss is insensitive to the variation of parameters $L1$ and $L3$. When $L1$ is varied by 30 μm from 116 μm to 176 μm and $L3$ by 30 μm from 352 μm to 412 μm, respectively, the return loss remains unchanged. It is also found that the return loss is sensitive to the variation of parameters

$L2$ and $L4$ as shown in Fig. 4.12. They affect both impedance bandwidth and resonant frequency. The resonant frequency increases when the parameter $L2$ increases from 190 μm to 350 μm by 80 μm. The resonant frequency decreases when the parameter $L4$ increases from 376 μm to 476 μm by 50 μm. The final optimized parameters for the quasi-Yagi antenna yield the axial length of the quasi-Yagi antenna 1.3 mm and a broad 10-dB return loss bandwidth from 55 to 65 GHz.

The simulated radiation patterns of the quasi-Yagi antenna in the azimuth and elevation planes at 60 GHz are shown in Fig. 4.13. Note that the quasi-Yagi antenna results in low cross-polarization radiation. They are 18.7 dB lower in the azimuth plane and 29.7 dB lower in the elevation plane as compared with co-polarization radiation. The poor front-to-back ratio is due to the lossy substrate configuration.

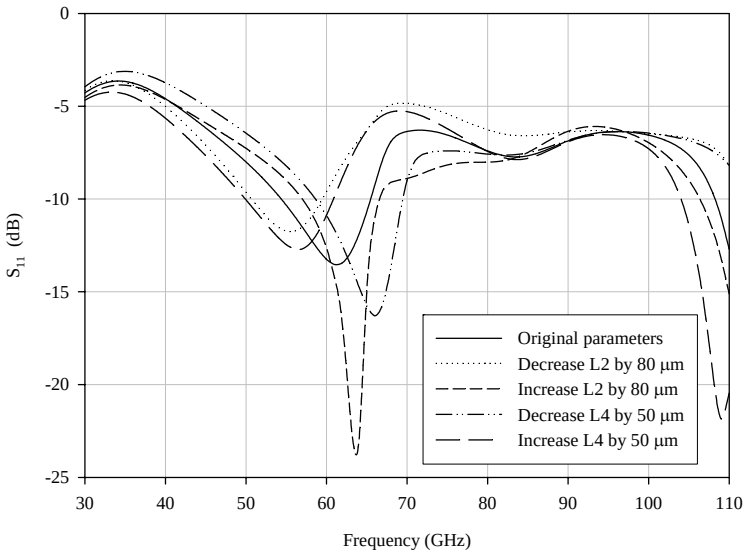


Figure 4.12: S_{11} of the quasi-Yagi antenna for parameter variation.

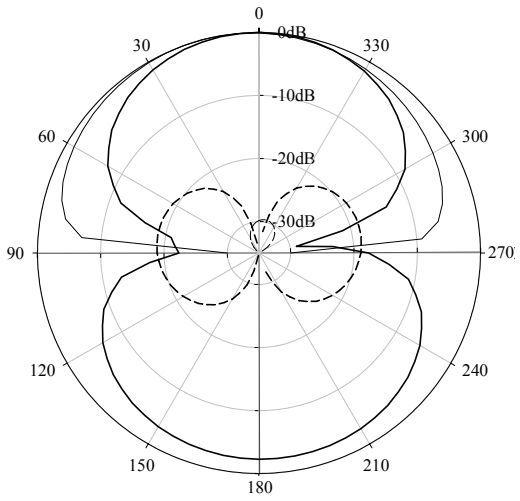


Figure 4.13: Radiation patterns of the quasi-Yagi antenna with solid lines for co-polarization components, short dash lines for cross-polarization components, normal lines for elevation plane ($\phi = 0°$), and thicker lines for azimuth plane ($\theta = 85°$).

4.2.2 Fabrication

The post BEOL process is illustrated in Fig. 4.14. Note that a standard low resistivity silicon wafer of diameter 8 inches and thickness 750 μm is used. First, a 6-μm thick SiO_2 layer is grown on the wafer to simulate the insulator used for on-chip interconnect in standard CMOS process and over it a 7.5 KÅ thin Aluminum pattern is deposited, which is equivalent to the Al pad used in standard CMOS ICs. Then, a 20-μm thick SiO_2 layer is grown to enhance the isolation of the RF passives from the silicon substrate of low resistivity. The 20-μm thick SiO_2 layer and the associated deep via capability are two important features of this BEOL process. Next, a 1 KÅ thin Si_3N_2 layer is grown. After this process, we proceed to grow a 4-μm thick SiO_2 layer. In the 4-μm thick SiO_2 layer the Copper passive pattern is embedded. Deep vias are formed to connect the Aluminum with the Copper layers. This is followed by growing

a 3 KÅ thin Si_3N_2 layer and a 3 KÅ thin SiO_2 layer for passivation sequentially. The Aluminum test pads are finally formed for testing.

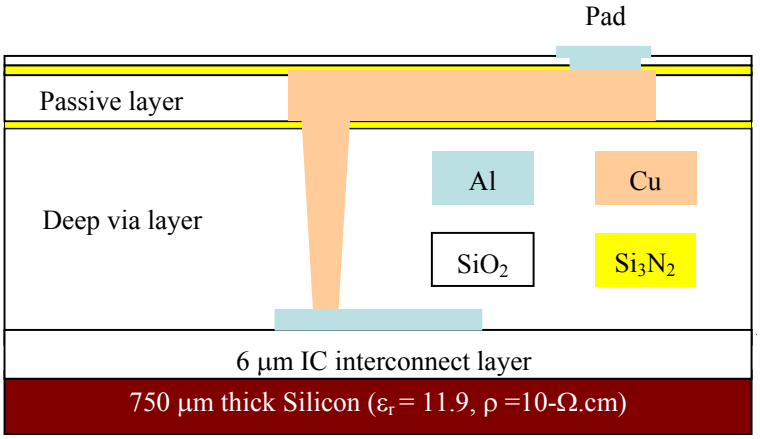


Figure 4.14: The BEOL process

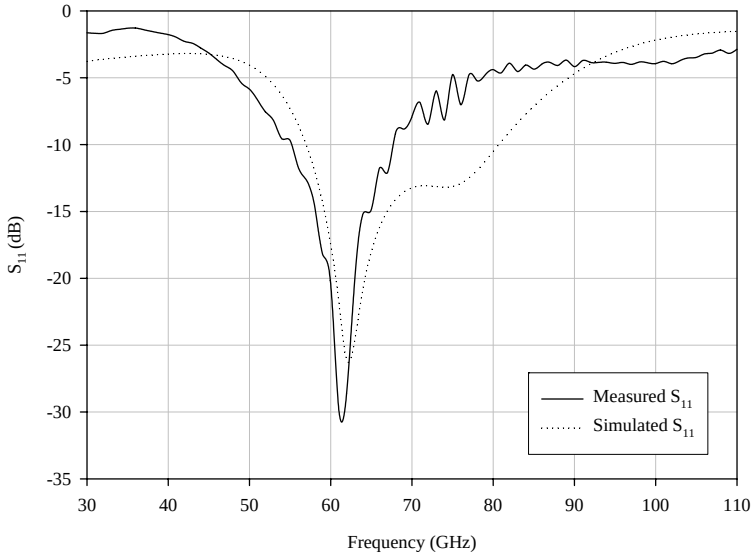
The inverted-F antenna was fabricated with the simplified post BEOL process. This can be seen from Fig. 4.8 (b) where no Aluminum layer is deposited and no deep via is formed. The inverted-F antenna is separated from the silicon substrate by a 20-μm thick SiO_2 layer. The quasi-Yagi antenna was fabricated with the modified post BEOL process. As seen from Fig. 4.11 (b), the antenna is formed by two 2-μm Aluminum layers separated by a 2-μm SiO_2 layer. The driver, two directors, and its feeding structure are etched on the top Aluminum layer, while the truncated ground plane used as the reflector is etched on the bottom Aluminum layer. The ground pads are connected to the truncated ground plane by vias to eliminate the capacitance effect between the two Aluminum layers. The whole antenna structure is separated from the silicon substrate by a 20-μm thick SiO_2 layer. It is obvious that the antennas can be built on CMOS IC chips using the post BEOL process if they are proved to be

successfully fabricated with the simplified post BEOL process discussed here.

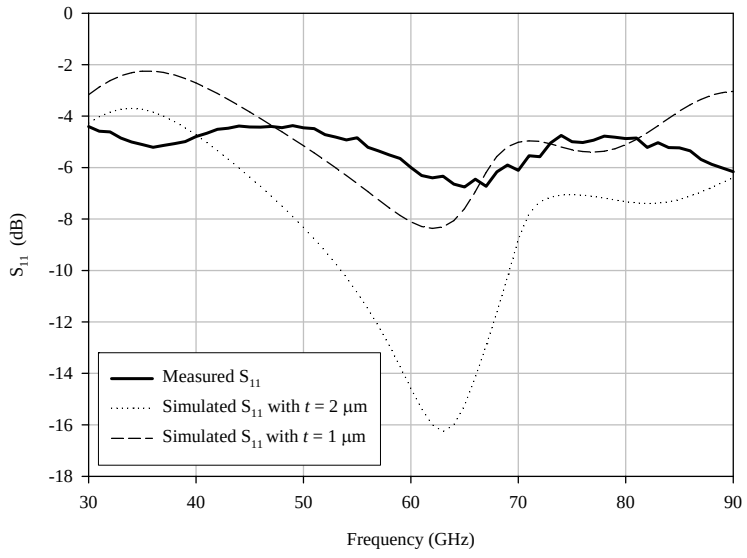
4.2.3 Characterization

The measurements were performed on-wafer with Cascade Microtech coplanar probes and an HP8510XF network analyzer. The S-parameters were measured for both antennas up to 110 GHz.

Fig. 4.15 (a) shows the measured and simulated S_{11} of the inverted-F antenna. It is evident from the figure that the measured result agrees well with the simulated one. It is more important to note from the measurement result that a sharp dip exists at 61 GHz, which indicates excellent antenna quality and good matching to the 50-Ω source. Using a threshold of -10 dB, the measured bandwidth for the inverted-F antenna covers from 55 to 67.5 GHz. Fig. 4.15 (b) shows the measured and simulated S_{11} of the quasi-Yagi antenna. Note that a resonance null occurs at 65 GHz. Using a threshold of -6 dB, the measured bandwidth covers from 61 to 70 GHz. The measured resonant frequency agrees with the simulated one. However, the matching is not good to achieve the lower return loss at the resonant frequency. It might be the reason of fabrication tolerance that makes the fabricated antenna not as fine as the designed. Fig. 4.15 (b) also shows the tolerance influence of the thickness t of the silicon oxide layer between the top antenna structure and the truncated ground plane on the return loss. This can give one important possible reason why the measured return loss is so low at the resonant frequency.



(a)



(b)

Figure 4.15: Measured and simulated S_{11} of (a) the inverted-F antenna and (b) the quasi-Yagi antenna.

The gains of both inverted-F and quasi-Yagi antennas were measured with the technique presented in [77]. The technique requires two identical antennas placed face-to-face and separated by a distance d. The distance d measures the separation between the reference planes used for far-filed measurements. One antenna functions as a transmit antenna, the other as a receive antenna. From transmission measurements the antenna gain can be estimated by

$$G^2 = |S_{21}|^2 \left[\frac{4\pi d}{\lambda}\right]^2 \quad . \tag{4.25}$$

The technique does not permit one to determine the radiation pattern. However, the goal of this work was to validate the design method and to optimize the process in order to integrate a complete 60-GHz radio front-end. The antenna gain is extracted from the measurements with d = 20 mm. In our measurement a gain of -19 dBi is obtained at 61 GHz for the inverted-F antenna; while a gain of -12.5 dBi at 65 GHz for the quasi-Yagi antenna.

4.2.4 High transmission gain inverted-F antenna pair on low resistivity Si

60-GHz on-chip antenna pair can be used for the intra-chip wireless communication. The wireless interconnects rely on transmission gains of on-chip antenna pair as defined in (3.1). In what follows we demonstrate the high transmission gain performance of the on-chip inverted-F antenna pair .

The layout and top view photograph of the on-chip inverted-F antenna are illustrated in Fig. 4.8. To characterize the antenna pair transmission performance, a test

vehicle is layout as shown in Fig. 4.16, including transmit antenna 00 and receive antennas 01, 02 and 03.

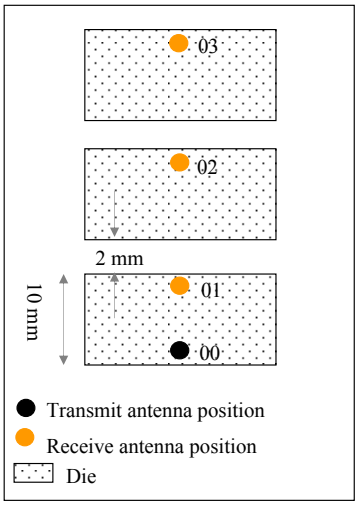


Figure 4.16: Top view of the tested die.

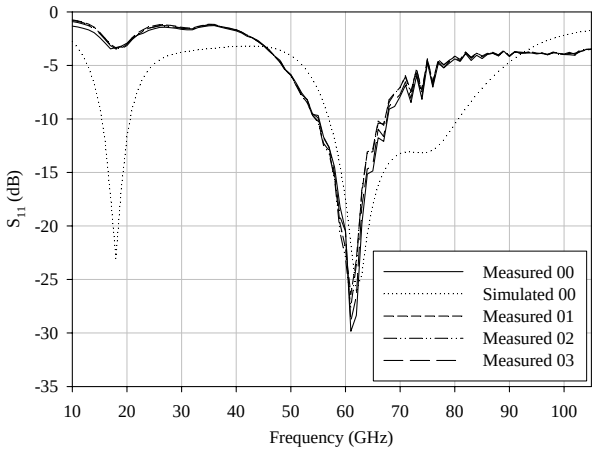


Figure 4.17: S_{11} versus frequency for the on-chip inverted-F antenna pair.

Fig. 4.17 shows the measured S_{11} results of receive antennas 01, 02, and 03 of Fig. 4.16 located at the three different dies, respectively. It is evident that their S_{11} results are insensitive to their location on the wafer. They show the same characteristics as

the Fig. 4.15 (a). A sharp resonance dip occurs at 61 GHz which comes from the one-wavelength resonance as already explained. Using the threshold of -10 dB, a broad 12.5-GHz bandwidth can be achieved at 61 GHz. In addition, Fig. 4.17 compares the measured and simulated S_{11} results of the transmit antenna 00 of Fig. 4.16. The simulation was run using a full-wave solver IE3D. It is seen that the measured and simulated locations of the resonance dips agree well. However, the measured and simulated S_{11} values do not agree well. It might be the reason of fabrication tolerance.

The transmission gain TG defined in eq. (3.1) is calculated from the measured S-parameters. It is valid only for the case that $|S_{11}| << 1$. It is seen from Fig. 4.17 that the measured S_{11} results are lower than -10 dB in the frequency range of 56-67 GHz. Fig. 4.18 shows the calculated transmission gain results in this frequency range between the transmit antenna 00 and receive antennas 01, 02, and 03 of Fig. 4.16. A transmission gain of -46.3 dB at 61 GHz is achieved from the pair of inverted-F antennas at the separation of 10 mm on the standard 10-Ω.cm silicon substrate of thickness 750 μm. It should be mentioned that a transmission gain of -56 dB was measured for a pair of 2-mm long and 10-μm wide dipoles at a separation of 10 mm on the standard 10-Ω.cm silicon substrate of thickness 500 μm at 18 GHz [13]. This is very near to the -56.3 dB gain at 18 GHz obtained for the same size dipoles at the same separation on the standard 10-Ω.cm silicon substrate of thickness 260 μm [38]. It is interesting to note from Fig. 4.18 that the transmission gain decreases slowly with the separation distance between the transmit and receive antennas in the far-field region at 61 GHz. An approximate decreasing rate of 0.16 dB per mm reveals that the

propagation of guided waves plays a dominant role. Fig. 4.18 also shows the measured phase delay between receive antennas 01 and 02 with respect to the transmit antenna. It is observed that the phase delay changes with frequency rapidly, which indicates that the signal in this frequency range suffers from the multipath fading due to the propagation of multiple guided modes or paths.

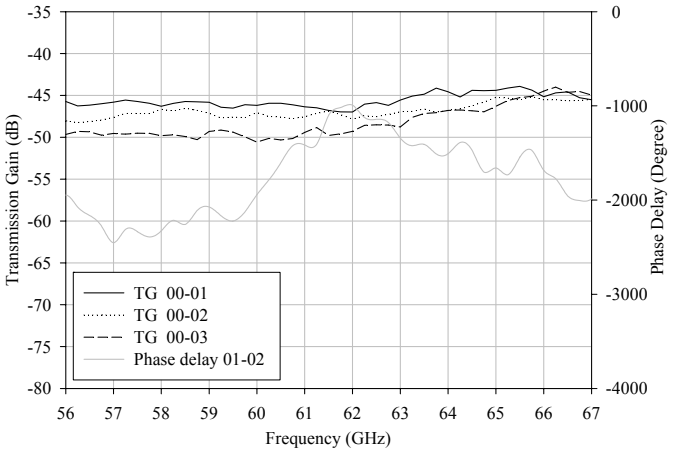


Figure 4.18: Transmission gain and phase delay versus frequency for the on-chip inverted-F antenna pair.

4.3 On-Chip Monopole Antennas

4.3.1 Layout and fabrication

Fig. 4.19 shows the on-chip monopole structures. They are zigzag 30°, meander, T-linear, T-meander, T-zigzag up, T-zigzag down, T-zigzag 30°, and T-zigzag 120°. The axial length of the antenna is 1 mm. The test ground-signal-ground (GSG) pads are squares of 80 μm by 80 μm. The width of the line elements is 10 μm. The T-linear monopole is easily designed due to its simple structure. Other monopoles are similar

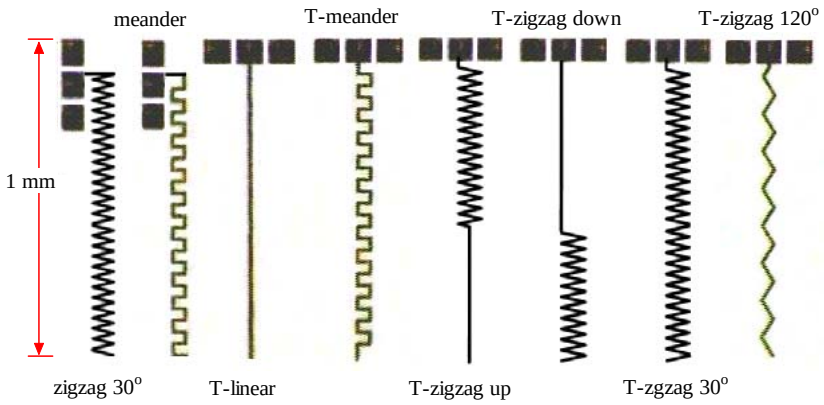
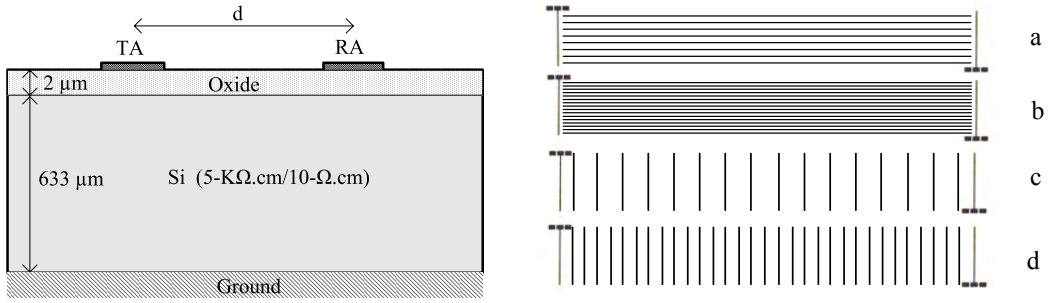


Figure 4.19: On-chip monopole antennas.

in that resonance is obtained in a compact space by compressing the wire in different ways. With the wire folded back and forth the antenna resonance is found in a much more compact structure than can otherwise be obtained.

The antennas were layout in a test vehicle and fabricated using the NTU 1.2-μm CMOS process on silicon wafers of high resistivity 5 KΩ.cm and low resistivity 10 Ω.cm, respectively. Fig. 4.20 (a) shows the test vehicle cross sectional view. As seen an oxide layer of thickness 2 μm was grown on the silicon substrate of thickness 633 μm to increase isolation and an aluminum layer of thickness 2 μm was used to form the antennas. The test vehicle contains the transmit and receive antenna pairs, each the mirror image of the other, with the separation distance d varied from 2.5 to 40 mm as shown in Fig. 4.20 (a). The test vehicle also contained interference structures. These structures were designed to estimate interference effects of metal lines between the transmitting and receiving monopoles on their performance. The interference structures as shown in Fig. 4.20 (b) include metal lines parallel to the

monopoles and metal lines perpendicular to the monopoles.



(a) (b)

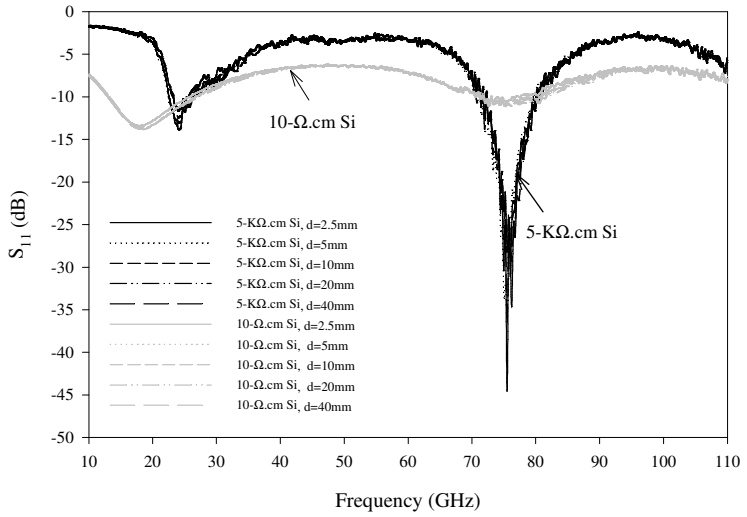
Figure 4.20: Test vehicle: (a) cross sectional view and (b) interference metal line structures.

4.3.2 Characterization

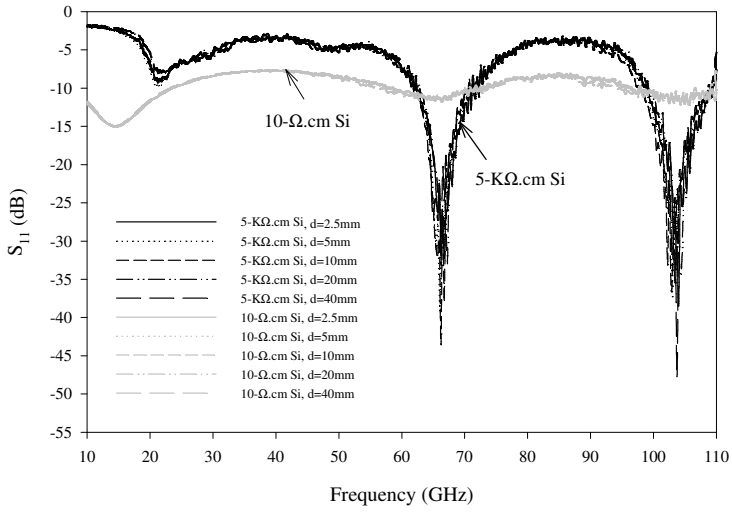
The on-chip monopoles were measured on wafer using a MicroTech probe station and an HP8510XF network analyzer to get the S-parameters in the frequency range of 10-110 GHz at the NTU wireless technology center. The reflection measurements were to obtain S_{11} and S_{22}, while the transmission measurements were to obtain S_{12} and S_{21}. The transmission gain TG is calculated from the S-parameters as defined in (3.1) [17].

The meander and zigzag 30° monopole pair performance are first evaluated. The results of reflection measurements are displayed in Fig. 4.21. It is evident from the figure that their S_{11} results are insensitive to the separation distance. Compared with the 5-KΩ.cm silicon substrate, the 10-Ω.cm silicon substrate has larger loss over the whole frequency range and there is no sharp resonance dip observed. In contrast, a sharp resonance can be seen at 75 GHz for the meander monopole and two at 67 and 104 GHz for the zigzag 30° monopole on the 5-KΩ.cm silicon substrate. Using the

threshold of −20 dB, a broad 5-GHz bandwidth can be achieved at all these resonant frequencies.



(a)



(b)

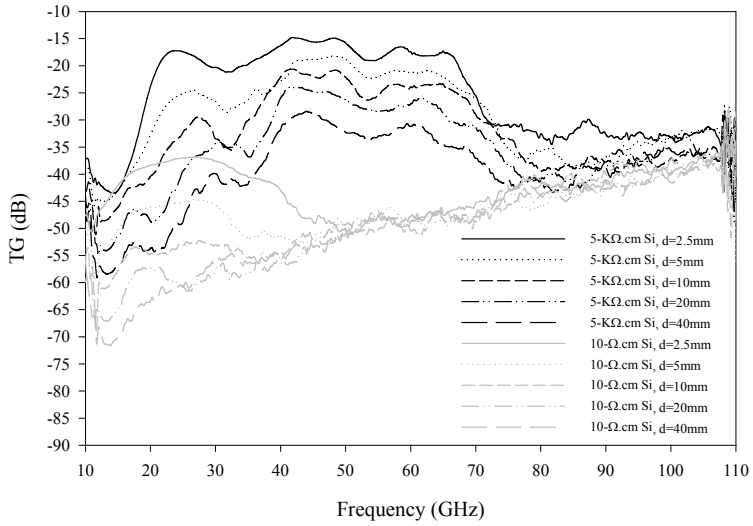
Figure 4.21: The measured S_{11}: (a) the meander pair and (b) the zigzag 30° pair.

The results of transmission measurements are exhibited in Fig. 4.22. It should be noted that the transmission measurement results around 110 GHz show large swings due to the test system problem around this frequency. Firstly, it is seen from the figure that the pattern of the transmission gain is quite similar for both meander and zigzag 30° monopole pairs. This is because the transmission gain reflects the propagation characteristics of the on-chip channel. Once the signal is excited by a monopole, the transmission of the signal is mainly controlled by the propagation characteristics of the on-chip channel. Secondly, there exists a high gain window. For the 5-KΩ.cm silicon substrate, the high gain window locates between 13 to 65 GHz. It first increases rapidly from 13 GHz, then maintains high with small fluctuations up to 60 GHz, and finally decreases slowly from 65 GHz. For the 10-Ω.cm silicon substrate, the high gain window becomes narrow and separation-dependent. Taking the separation of 5 mm as an example, the high gain window starts at 13 GHz and ends at 33 GHz. Finally, it is more interesting to note that the transmission gain increases slowly with frequency and becomes insensitive to separation after 45 GHz for the 10-Ω.cm silicon substrate.

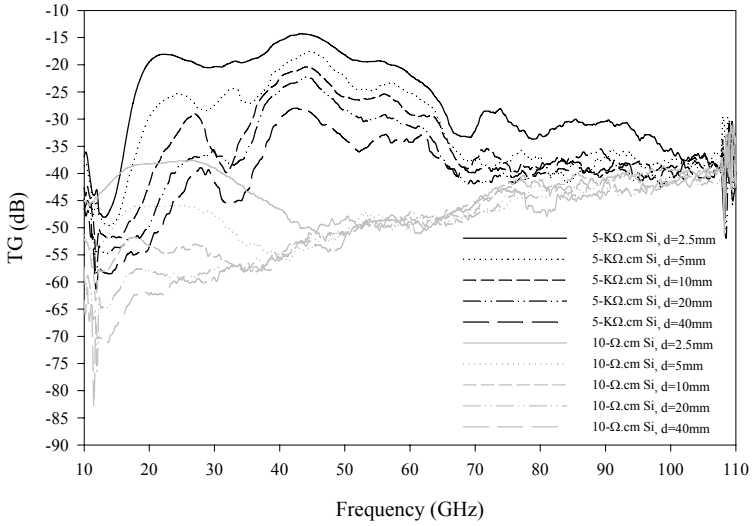
The distinction between the high gain window area and after the high gain window area can be clearly identified in the measured phase of S_{21}. Fig. 4.23 shows the measured phase of S_{21} for the meander monopole pair with a separation of 5 mm. Note that within the window area the phase exhibits linear or nearly linear characteristic with frequency, which illustrates that the signal transmission between the monopoles occurs through the propagation of a dominant mode or path. The signal in this frequency range can be expected to be received easily. While in the after-window area

the phase changes with frequency rapidly, the signal in this frequency range suffers from the multipath fading due to the propagation of multiple modes or paths. This multipath fading effect occurs more easily for lower resistivity silicon substrate and larger distance. This explains why the window width decreases with distance.

The finding of the high gain window is important and useful. It suggests that the operating frequency of wireless interconnects be allocated within the high gain window for good performance. For instance, the frequency of 18 GHz is a proper band for wireless interconnects on standard 10-Ω.cm silicon substrates. At 18 GHz, a transmission gain of -56 dB was measured for a pair of 2-mm long and 10-μm wide dipoles at a separation of 10 mm on the standard 10-Ω.cm silicon substrate of thickness 500 μm [38].This is very near to the -56.3 dB gain at 18 GHz obtained for the same size dipoles at the same separation on the standard 10-Ω.cm silicon substrate of thickness 260 μm [33]. As can be seen from Fig. 4.22, a transmission gain of -54 dB at 18 GHz are achieved from either the pair of meander or zigzag 30° monopoles at the separation of 10 mm on the standard 10-Ω.cm silicon substrate of thickness 633 μm. We enhanced the gain by 2 dB with a 50% reduction in antenna axial length. The reduction of antenna length directly helps to save the die area.

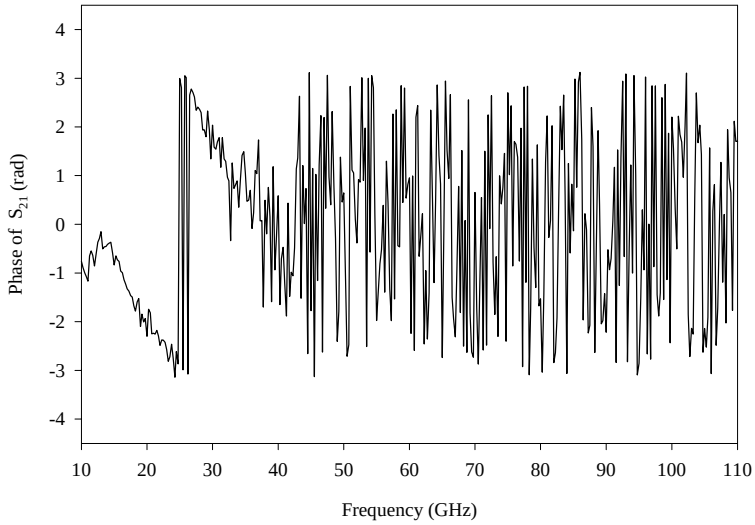


(a)

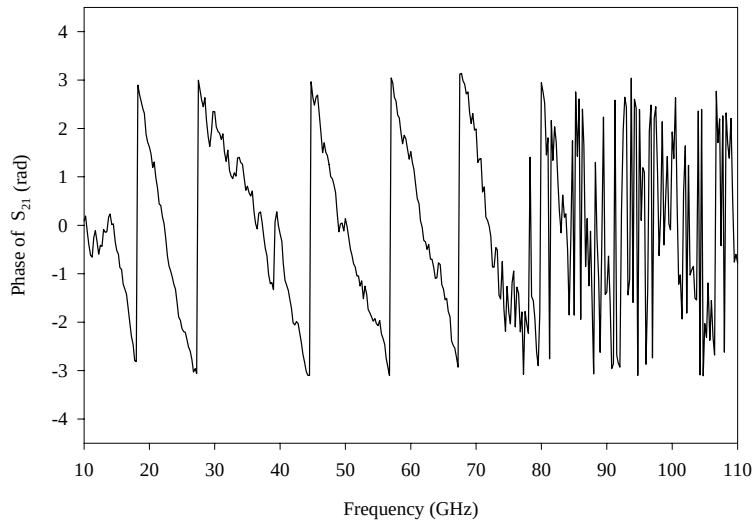


(b)

Figure 4.22: The measured transmission gain: (a) the meander pair and (b) the zigzag 30° pair.



(a)



(b)

Figure 4.23: The measured phase of S_{21} of the meander pair at d = 5 mm on (a) 10-Ω.cm and (b) 5-KΩ.cm silicon substrate.

4.3 On-Chip Monopole Antennas

Inside an SoC or an ULSI, there are many metal structures such as bus lines or power lines. Inevitably, they occur in between the transmitting and receiving antennas and certainly affect the performance of the antenna pair. To study their effects, we measured the transmission gain over a distance of 5 mm between a pair of T-linear monopoles with and without metal lines as shown in Fig. 4.20 (b). Fig. 4.24 shows the measurement results. It is observed from the figure that the existence of metal lines improves the highest gain of the window area. This is because the periodic layout of the metal lines enhances the band pass characteristic of the on-chip channel. This characteristic can be used wisely to improve antenna gain performance.

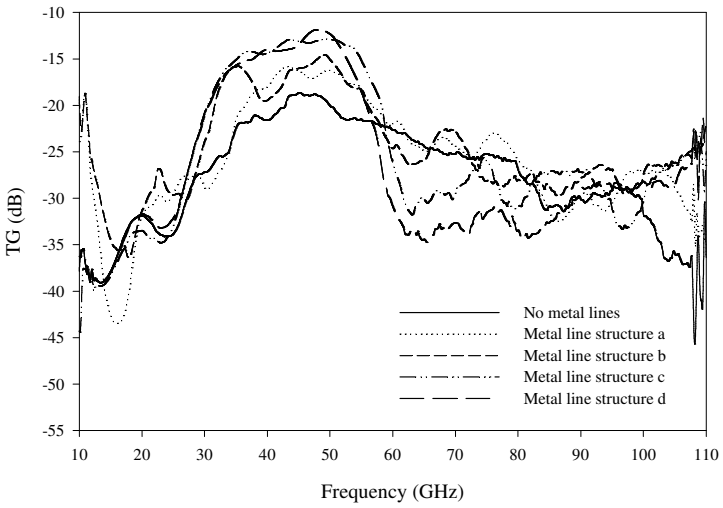
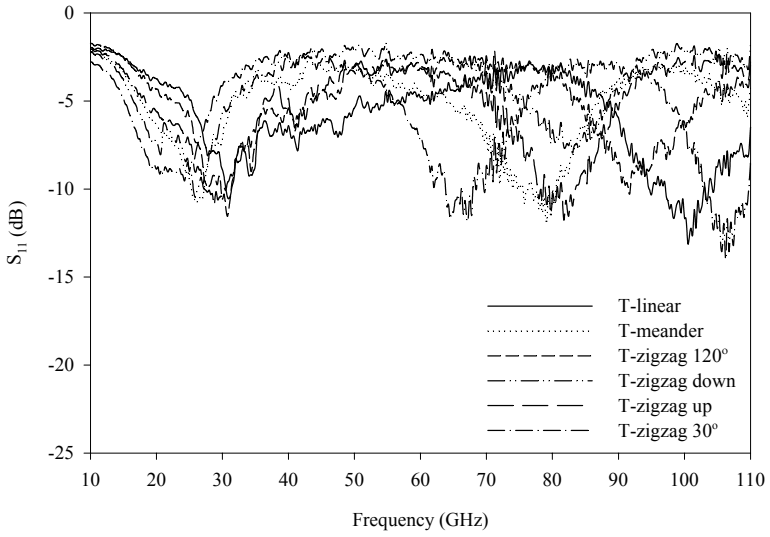
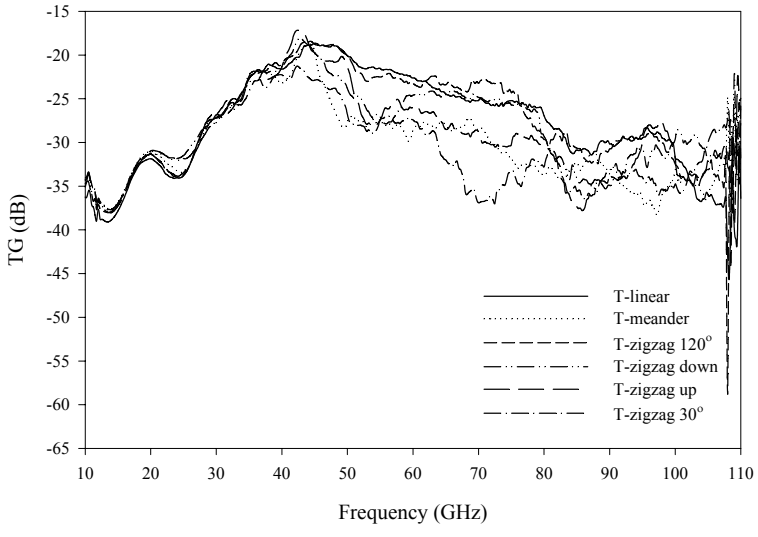


Figure 4.24: The measured effects of metal lines on the transmission gain on 5-KΩ.cm silicon substrate.

Finally, the measurement results of the other monopoles are compared in Fig. 4.25. It is seen that no sharp resonance dips ($<$ -20 dB) can be observed for the monopoles on the 5-KΩ.cm silicon substrate. Nevertheless, we still can find that the longer the unfolded length of the monopole is, the lower the resonant frequencies are.



(a)



(b)

Figure 4.25: The measured results of the other monopole pairs at d = 5 mm on 5-KΩ.cm silicon substrate, (a) S_{11} and (b) transmission gain.

4.4 Intra-Chip Wireless Interconnect Using On-Chip Antennas and UWB Radios

4.4.1 System description

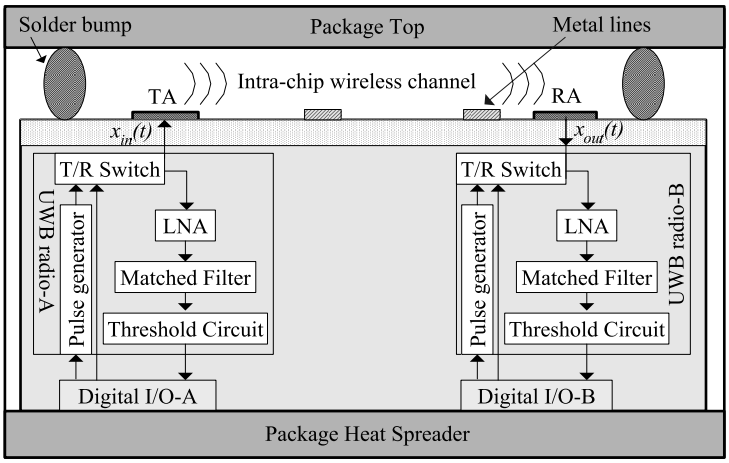


Figure 4.26: Intra-chip wireless interconnect system architecture.

Fig. 4.26 shows the proposed intra-chip wireless interconnect system located inside an IC package to fulfill the interconnect function between digital I/O A and B. The system uses on-chip antennas on the same substrate, including transmit antenna (TA) and receive antenna (RA). It is interesting to note that a unique intra-chip wireless channel is formed between the TA and RA. A transfer function $H(f)$ is defined in the frequency domain for the intra-chip wireless channel as the ratio of $x_{in}(t)$, the signal applied to the TA, to $x_{out}(t)$, the signal received by the RA. In our study $H(f)$ will be characterized by the experimental method. The system uses UWB radios that operate in 22-29 GHz. Its structure and transmitted signal have been described in section 2.1. Here, the PPM signal $x_{in}(t)$ applied to the TA is the same as eq. (2.2). Given $x_{in}(t)$

and the experimentally characterized $H(f)$ the channel output signal $x_{out}(t)$ is easily obtained using the Fourier inverse transform.

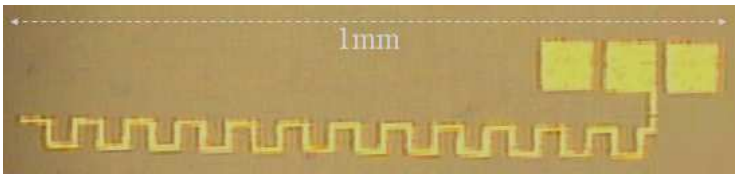


Figure 4.27: On-chip meander antenna top view photograph.

The 1-mm long on-chip meander monopole antenna is used for TA and RA. Its top view photograph is shown in Fig. 4.27 and its cross sectional view is shown in Fig. 4.20 (a). Its fabrication and characterization have already been presented in section 4.3. Fig. 4.28 shows the simulated and measured S_{11} results in 15-50 GHz for the fabricated on-chip meander antenna. It is seen that the measured and simulated locations of the resonance dips agree well for both high and low resistivity cases. They are at 23 GHz and 18 GHz for the 5-KΩ.cm Si and 10-Ω.cm Si substrates, respectively. The feature size of our meander antenna is about 2.5 mm. Based on the exact simulations from the IE3D, it is found that the guided wavelengths at 23 GHz in the 5-KΩ.cm Si substrate and at 18 GHz in the 10-Ω.cm Si substrate of Fig. 4.20 (a) are both about 5 mm. This indicates that the origin of these resonant frequencies comes from the half-wavelength resonance. In addition, it is evident from Fig. 4.28 that the substrate is lossy and the monopole antenna can not operate well in 22-29 GHz if evaluated using 10-dB return loss bandwidth threshold. However, the 6-dB return loss bandwidth threshold is still acceptable in the industrial standard. As shown, for the 5-KΩ.cm and

10-Ω.cm Si substrates the measured S_{11} results are both lower than -6 dB from 22 to 29 GHz, indicating an acceptable matching to a 50-Ω source. In addition, the simulated radiation efficiency is 7 % for the 5-KΩ.cm case and 1.1 % for the 10-Ω.cm case. The low efficiencies are caused by the lossy silicon substrate.

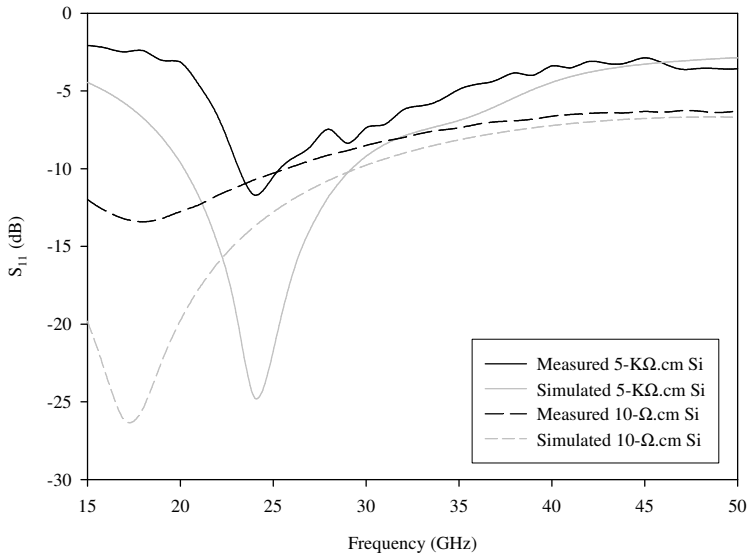


Figure 4.28: S_{11} of the on-chip meander antenna.

4.4.2 System performance evaluation

A. Characterization of intra-chip wireless channel

A test vehicle with the cross section view of Fig. 4.20 (a) was fabricated and measured to characterize the intra-chip wireless channel. The transmit and receive antenna pairs, each the mirror image of the other, were layout in the test vehicle with the separation distance d varied from 2.5 to 40 mm. The measurements were conducted to characterize the intra-chip wireless channel by its transfer function $H(f)$. Fig. 4.29

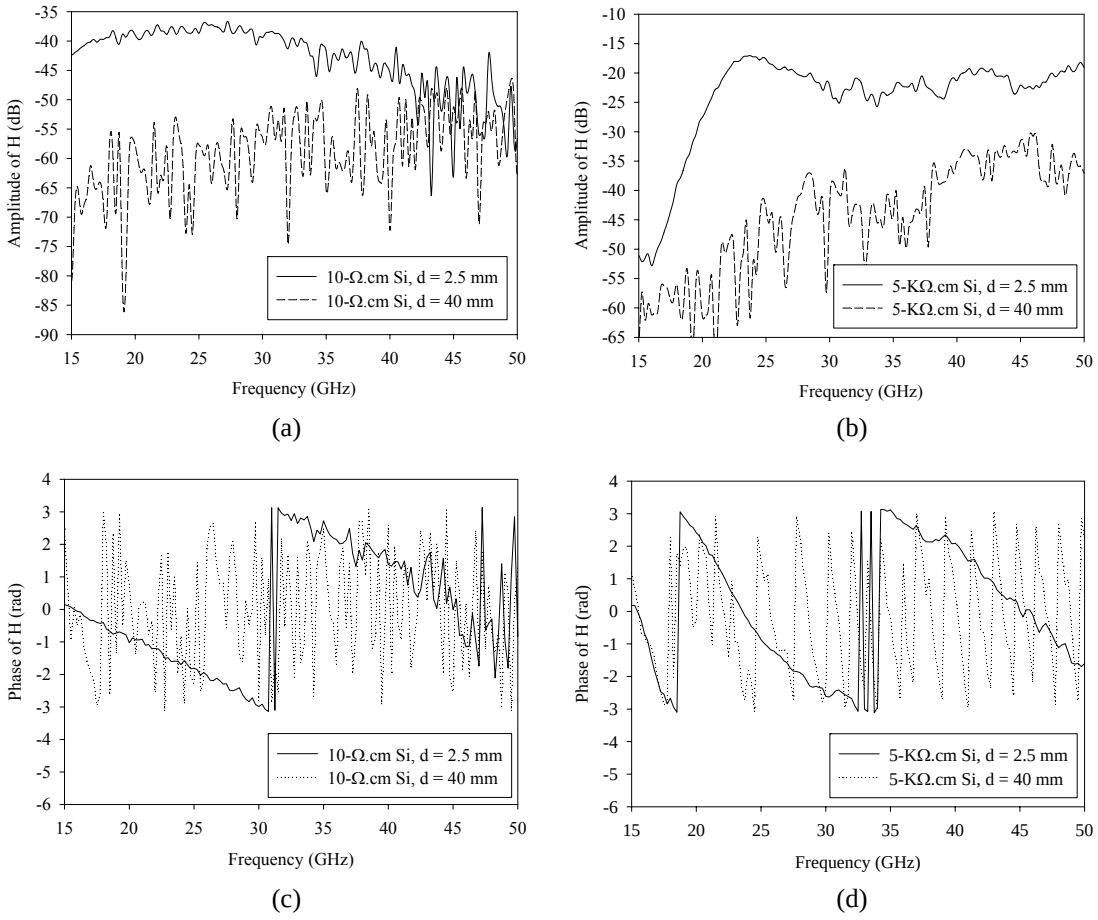


Figure 4.29: Measured $H(f)$: (a) amplitude, 10-Ω.cm Si, (b) amplitude, 5-KΩ.cm Si, (c) phase, 10-Ω.cm Si, and (d) phase, 5-KΩ.cm Si.

shows the measured transfer function $H(f)$ at the interconnect distances of 2.5 and 40 mm on the 5-KΩ.cm and 10-Ω.cm Si substrates. It is seen that both amplitude and phase of the transfer function $H(f)$ fluctuate with frequency indicating that the intra-chip wireless channel is a frequency-selective channel. The frequency-selective characteristics originate from the transmission of multi hybrid electromagnetic modes supported by the intra-chip wireless channel. The intra-chip wireless channel is actually an imperfect dielectric waveguide. The imperfectness of the dielectric waveguide is the result of the intra-chip wireless channel not being designed primarily as a wave guid-

ing structure. Since electric monopole antennas are used, the horizontally-polarized hybrid electromagnetic mode HEM_{11} dominates in the transmission, as a result, the fluctuations should follow a Rician distribution [17]. Fig. 4.29 also shows that the amplitudes of $H(f)$ are higher for the 5-KΩ.cm Si substrate than those for the 10-Ω.cm Si substrate at the same interconnect distance. This reveals that the loss of the intra-chip wireless channel depends on the chip substrate resistivity. The higher the resistivity is, the lower the loss is.

Fig. 4.30 shows the channel loss L_c with the varying interconnect distance on the 5-KΩ.cm and 10-Ω.cm Si substrates. The channel loss that equals to the energy difference between the received signal and the transmitted signal is computed from the measured channel transfer function. It is evident from the figure that the longer interconnect distance is, the larger the channel loss is. It is noted that the existence of metal lines and solder bumps may increase or decrease the channel loss depending on their layout as shown in Fig. 4.24. However, their existence will not change the channel frequency-selective nature and the intra-chip wireless channel in the realistic packaged chip environment still can be treated as a Rician fading channel for system performance analysis.

Having measured the channel transfer function $H(f)$, we can use it to calculate the signal received by the RA $x_{out}(t)$ with respect to the signal applied to the TA $x_{in}(t)$. Fig. 4.31 shows an example of the transmitted data, $x_{in}(t)$ with an normalized amplitude, T_f = 0.3 ns, R_b = 1/T_f = 3.33 Gbps and δ_{opt}= 0.02 ns, and $x_{out}(t)$ received

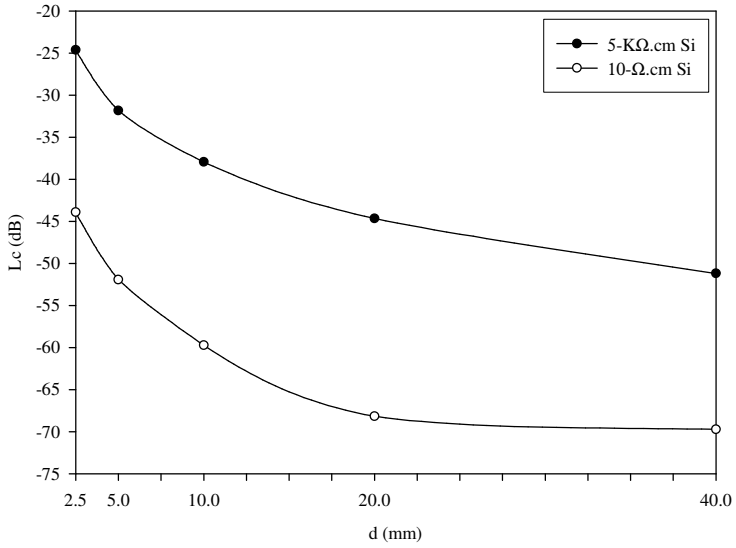


Figure 4.30: Channel loss versus interconnect distance.

by the RA located at d = 2.5 mm on the 5-KΩ.cm Si substrate. It is seen that the received signal suffers loss and delay. From the channel characteristic, we know that the loss of the received signal increases with distance and decreases with substrate resistivity. The delay also increases with distance. We confirm this in our simulation. For brevity, we only show one example here.

B. System BER performance

The performance of the intra-chip wireless interconnect system is evaluated using the method presented in section 3.2.1 in terms of BER under the assumptions of perfect system synchronization and signal corruption from the thermal and switching noises. In the Γ_b calculation, the receiver noise figure F_r is reasonably assumed to be 15 dB. The switching noise is assumed to be T = 10 dB or T = 5 dB lower than the thermal noise according to the measured result [66]. The other parameters used in the evalua-

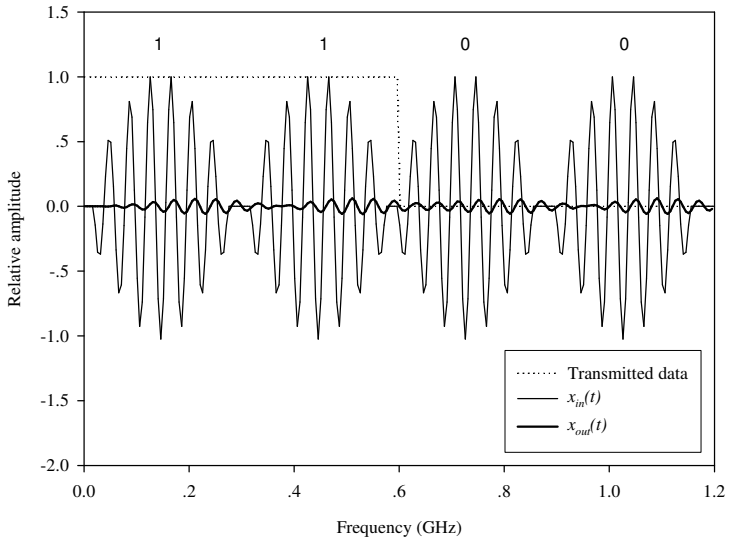
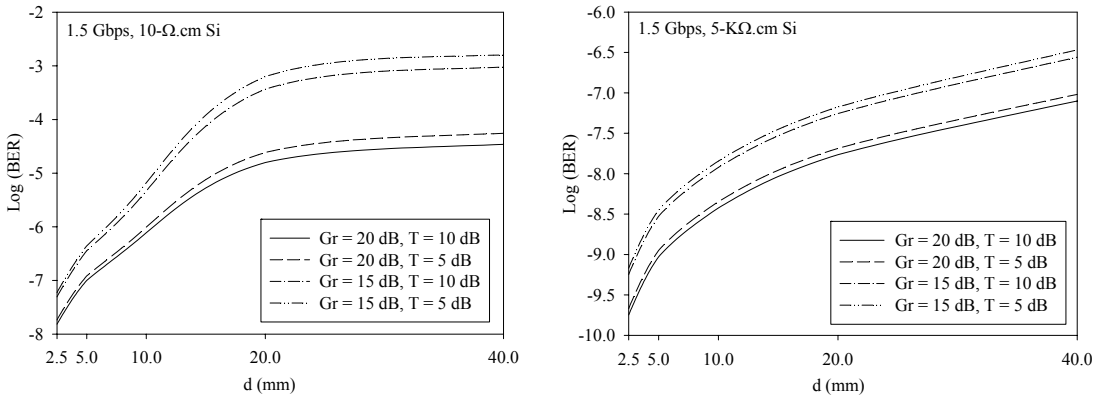


Figure 4.31: Transmitted data, $x_{in}(t)$, and $x_{out}(t)$ with normalized amplitude at d = 2.5 mm and R_b = 3.33 Gbps.

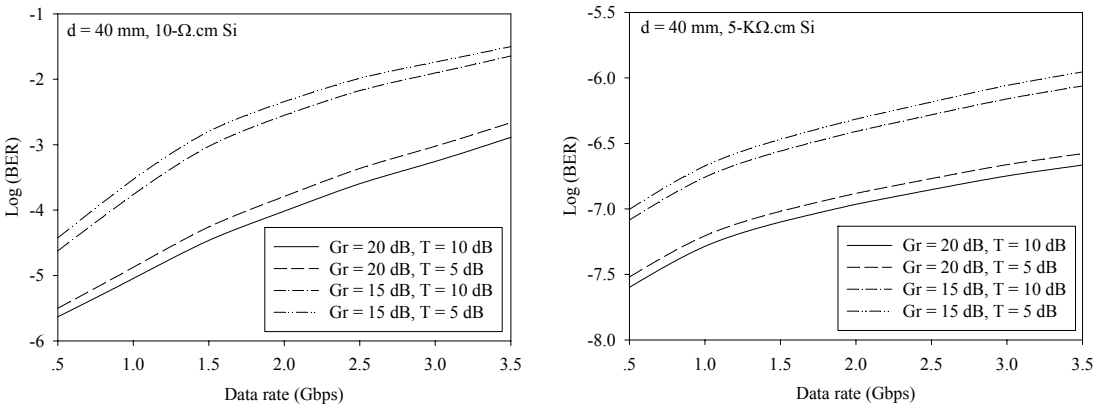
tion are all reasonable values with G_r = 15 or 20 dB, L_m = -4 dB, K = 10 dB and P_t = 0 dBm.

Fig. 4.32 shows the BER versus distance d for the 5-KΩ.cm and 10-Ω.cm Si substrates at R_b = 1.5 Gbps. Fig. 4.33 shows the BER versus data rate R_b for the 5-KΩ.cm and 10-Ω.cm Si substrates at 40 mm distance. As expected, the BER performance degrades with interconnect distance and data rate. In addition, the system on the 5-KΩ.cm Si substrate achieves a better BER than that on the 10-Ω.cm Si substrate. It is also shown that the system on the 10-Ω.cm substrate can support a data rate of 1.5 Gbps with a BER $< 10^{-5}$ up to an interconnect distance of 10 mm with the average transmitted power of 0 dBm; while the system on the 5-KΩ.cm substrate can support a data rate of 3.5 Gbps with a BER $< 10^{-6}$ up to an interconnect distance of 40 mm with the same transmitted power.



(a) (b)

Figure 4.32: BER versus distance d at R_b = 1.5 Gbps on (a) 10-Ω.cm Si and (b) 5-KΩ.cm Si.



(a) (b)

Figure 4.33: BER versus R_b at d = 40 mm on (a) 10-Ω.cm Si and (b) 5-KΩ.cm Si.

Chapter 5

On-Package Antennas for Inter-Chip Wireless Interconnects

LTCC-based on-package antennas for inter-chip wireless interconnects are studied, including a discrete beveled monopole ultrawide-band (UWB) antenna in section 5.1, a UWB integrated circuit package antenna (ICPA) in section 5.2, and 60-GHz ICPAs in section 5.3. A novel inter-chip wireless interconnect system using on-package beveled monopole antennas and UWB radios that operate in 3.1-10.6 GHz is finally studied in section 5.4.

5.1 LTCC-Based Beveled Monopole UWB Antenna

Fig. 5.1 shows the layout and photograph of the beveled monopole antenna in LTCC for UWB applications. Its structure with a slot has good mechanical property, which can successfully combat the warpage or fracture in LTCC fabrication caused by different stress property of the metallization layer and LTCC substrate layer. The finalized footprint of the beveled antenna only has small dimensions of 8×15 mm^2. The final fabricated dimensions are, $L1$ = 3 mm, $L2$ = 15 mm, $L3$ = 8 mm, $L4$ = 2 mm, $L5$ = 2 mm, $X1$ = 6.7 mm, $X2$ = 5 mm, $X3$ = 2 mm, $S1$ = 0.3 mm, $S2$ = 1 mm.

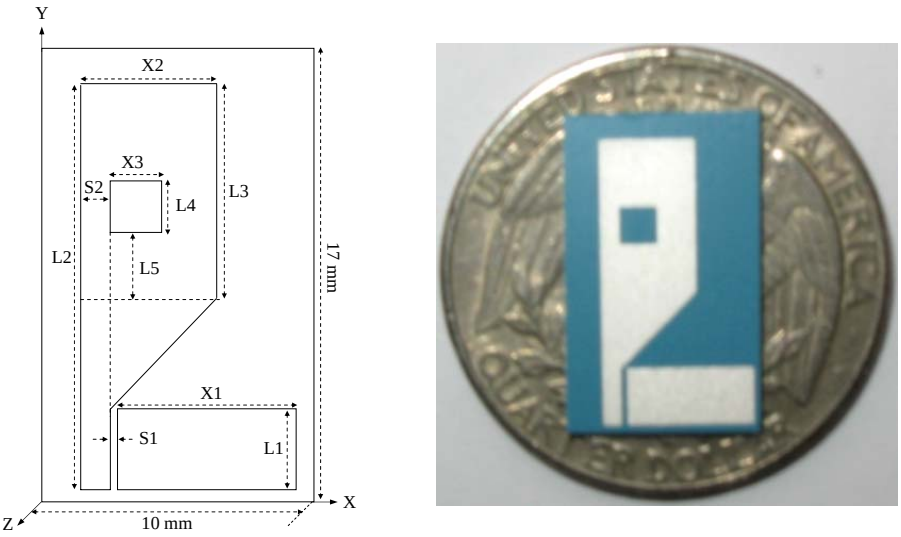


Figure 5.1: Beveled monopole antenna in LTCC for UWB applications.

A. Impedance bandwidth and radiation patterns

The antenna was fed by a PSF-S01 SMA connector in our measurement. The asymmetry of the structure was enhanced by the feeding SMA connector, which would make the cross-polar radiation more significant. The S-parameter was measured with the N5230A network analyzer. Fig. 5.2 shows the measured S_{11} result. As shown the impedance bandwidth is 8.25 GHz from 2.85 to 11.1 GHz. In addition, Fig. 5.3 shows the measured radiation patterns in both H (XZ) and E (YZ) planes at 3.5 GHz, 6.85 GHz and 10 GHz, respectively. As shown, the beveled UWB antenna has high cross-polar radiation. This is confirmed by observing the electrical current distribution across the surface of the antenna. As analyzed in [57], the X-directed current component on the radiating element does not cancel owing to its asymmetry of the structure. This

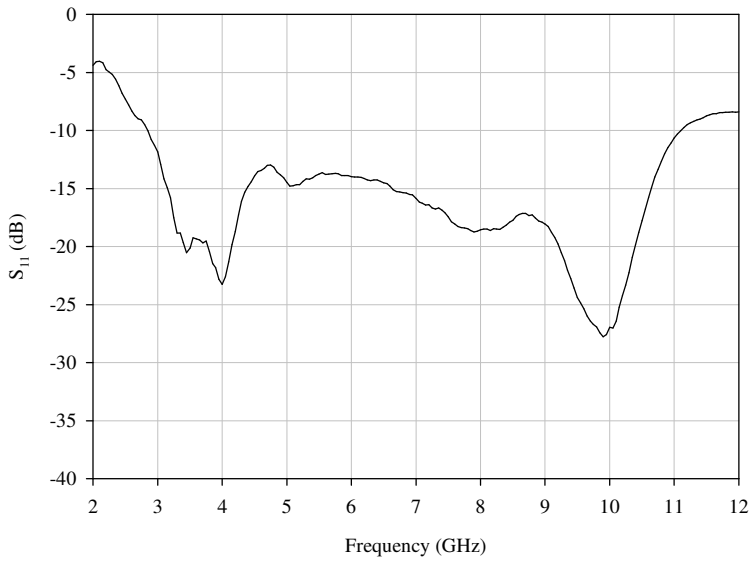


Figure 5.2: Measured S_{11} of the beveled UWB antenna.

leads to the high cross-polar radiation.

B. Transfer functions and gain

The measurement of the transfer functions was conducted in an anechoic chamber. During the measurement the transmitting antenna was fixed while the AUT (the beveled monopole UWB antenna) or the standard antenna was mounted as the receiving antenna. The transmitting and receiving antenna pair was placed in a face-to-face co-plane orientation with a separation distance of 1.6 m. In our measurement the WJ-48430 dual-polarized quad-ridged horn antenna was chosen to be both the transmitting and standard receiving antenna. This antenna has proved to be well matched to the measurement system from 3 to 18 GHz. The transfer functions $S_{21,AUT}(f)$ and $S_{21,STD}(f)$ were then measured by the N5230A network analyzer. It should be mentioned that the system was calibrated to the antenna terminals in advance.

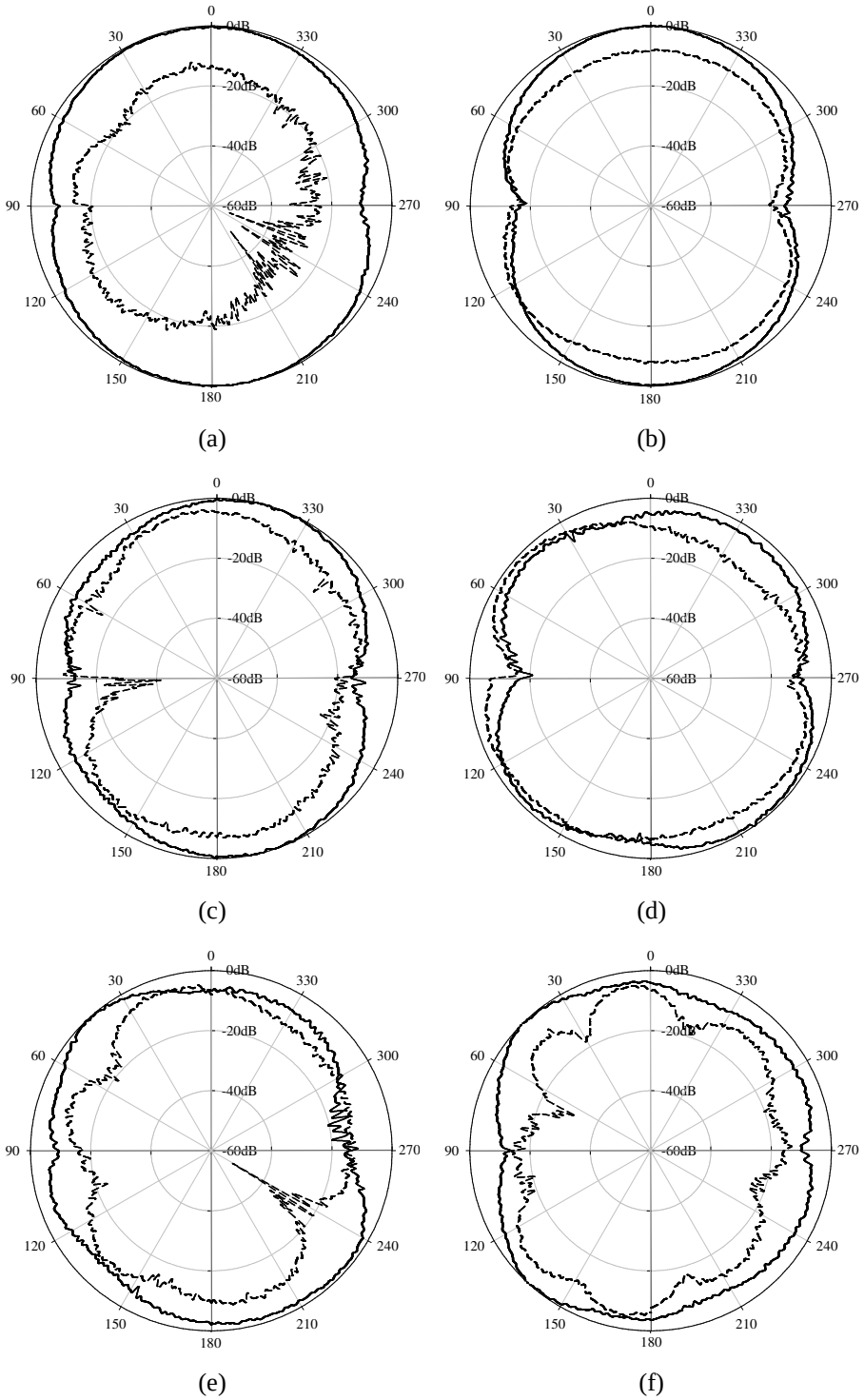


Figure 5.3: Measured radiation patterns of the beveled UWB antenna with solid lines for co-polarization components and short dash lines for cross-polarization components: (a) H plane at 3.5 GHz, (b) E plane at 3.5 GHz, (c) H plane at 6.85 GHz, (d) E plane at 6.85 GHz, (e) H plane at 10 GHz, and (f) E plane at 10 GHz.

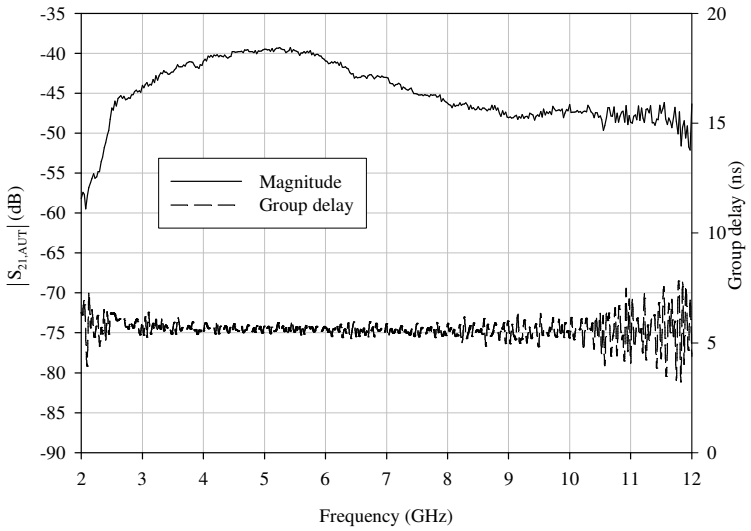


Figure 5.4: Measured transfer function of the beveled UWB antenna.

Fig. 5.4 shows the measured $S_{21,AUT}(f)$ magnitude and group delay. As seen the magnitude of the transfer function is relatively flat and the group delay is relatively constant over the whole UWB frequency range. The normalized antenna transfer function of the AUT is further defined as follows to calibrate the range related effects [48].

$$H_{N,AUT}(f) = \frac{S_{21,AUT}(f)}{S_{21,STD}(f)} H_{N,STD}(f) \tag{5.1}$$

where $H_{N,STD}(f)$ is the normalized antenna transfer function of the standard antenna. It can be readily achieved by referring to the gain data sheet and estimating group delay of the standard horn antenna as illustrated in [48]. Fig. 5.5 shows the $H_{N,AUT}(f)$ magnitude and group delay. It is observed that the magnitude of the normalized transfer functions is rather flat and the group delay is nearly constant over the frequency band of interest. As a consequence, the beveled monopole UWB antenna has proved to be very suitable for UWB radios.

It should be emphasized that the magnitude in decibels of the normalized transfer function is exactly the antenna absolute gain [48]. As seen from Fig. 5.5 that the gain varies from - 5.6 to 2.3 dBi over the whole UWB frequency range of 3.1-10.6 GHz.

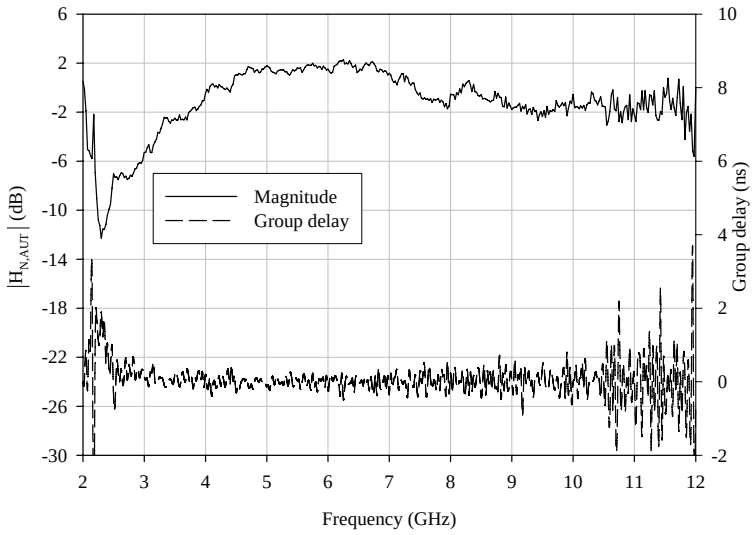


Figure 5.5: Normalized measured transfer function of the beveled UWB antenna.

C. Time-domain characteristics

Two kinds of incident pulse are selected in this study. One is the fourth derivative of a Gaussian function pulse expressed as follows with T_w = 175 ps,

$$s_i(t) = \left(3 - 6\left(\frac{4\pi}{T_w^2}\right)t^2 + \left(\frac{4\pi}{T_w^2}\right)^2 t^4\right) \cdot e^{-2\pi\left(\frac{t}{T_w}\right)^2} \tag{5.2}$$

The other is the modulated pulse expressed as follows with carrier frequency f_c = 5 GHz and a = 300 ps,

$$s_i(t) = sin(2\pi f_c t)e^{-\left(\frac{t}{a}\right)^2} \tag{5.3}$$

The waveforms of these two kinds of incident pulse are illustrated in Fig. 5.6. As seen in Fig. 5.7 their power spectrum density (PSD) comply with the required FCC indoor emission mask.

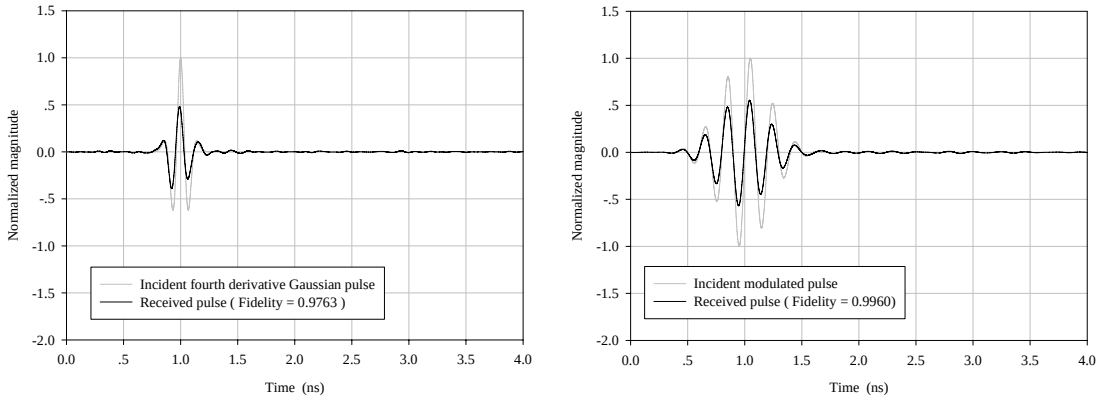
The output waveform at the receiving antenna terminal can be expressed by an inverse Fourier transform as follows,

$$s_r(t) = F^{-1}\left\{S_i(f) \cdot H_{N,AUT}(f) \cdot \prod(f)\right\} \tag{5.4}$$

where $\prod(f)$ represents an ideal bandpass filter from 2 to 12 GHz. Fig. 5.6 also illustrates the received pulses by the beveled UWB antenna. A well-defined parameter named Fidelity is proposed in eq. (5.5) to evaluate the capability of pulse distortion of the antennas [48].

$$Fidelity = \max_{\tau}\left\{\frac{\int_{-\infty}^{\infty} s_i(t)s_r(t+\tau)dt}{\sqrt{\int_{-\infty}^{\infty} s_i^2(t)dt \int_{-\infty}^{\infty} s_r^2(t)dt}}\right\} \tag{5.5}$$

It quantitatively describes how similar the received pulse to the incident pulse. It reaches the maximum unity as the two pulses are exactly the same in shape. As shown in Fig. 5.6 with values of Fidelity better than 0.97 the well-behaved received pulses are demonstrated and the late time ringing is almost negligible. This validates that the beveled monopole UWB antenna does not distort the incident pulse significantly. It also proves its applicability in UWB radios.



(a) (b)

Figure 5.6: Waveforms of the incident pulses and received pulses.

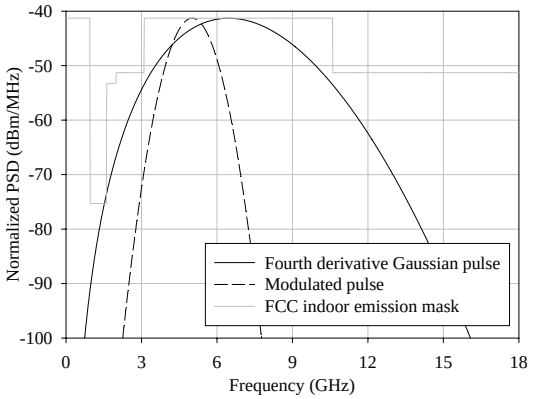


Figure 5.7: The normalized PSD of the incident pulses.

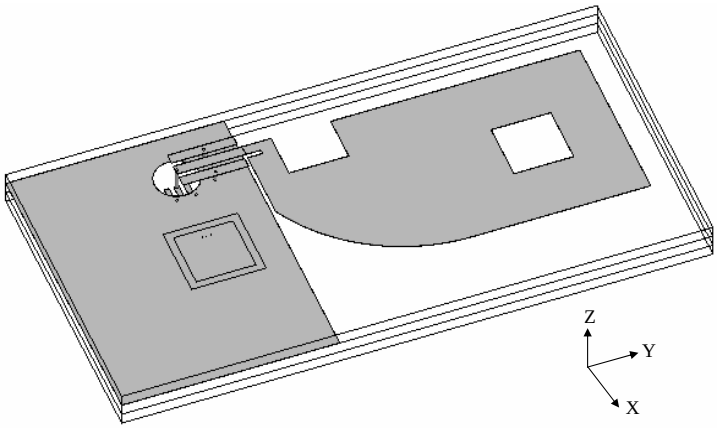
5.2 LTCC-Based UWB ICPA

This section focuses on the UWB antenna integration issue in simulation. No experimentally tests are conducted. In the previous studies UWB antennas are discrete and excited from an external added port but not from the internal transceiver chip [48, 49, 50, 51, 52, 53, 56, 57]. The chip-package co-EM simulation method should be further used to examine the UWB antenna integration performance. Further-

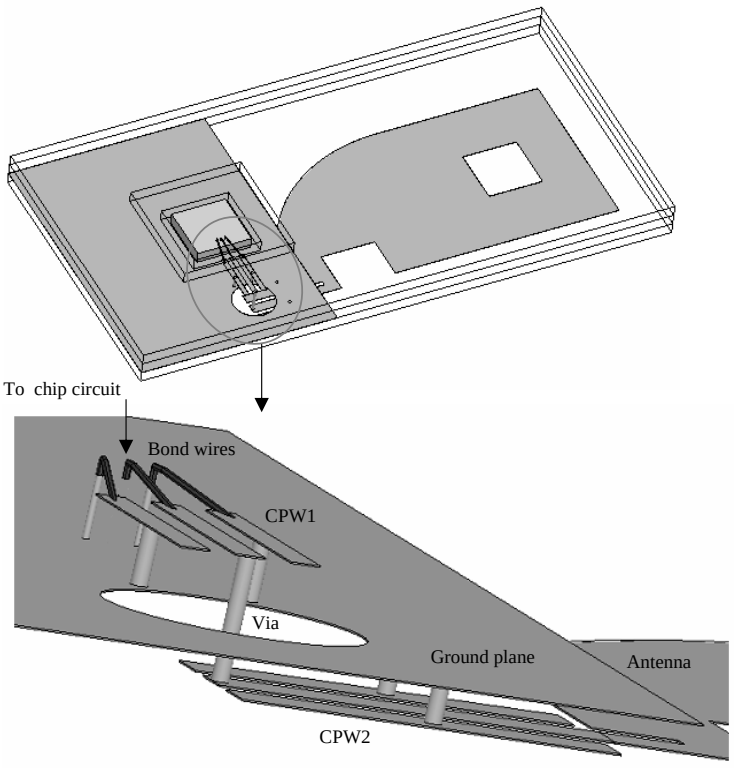
more, the design difficulty of the UWB ICPA still remains in achieving the ultra-wide band impedance matching. Bandwidth enhancement techniques should be adopted in the design of UWB ICPA, such as techniques of using double or trident feeding [78, 79], using multiresonant radiation structures [80], and etc. In what follows a UWB ICPA in LTCC technology is designed to cover the upper multiband UWB frequency range of 5.5-10.6 GHz. The miniaturized antenna is designed to be integrated to an LTCC package format with a dummy UWB transceiver chip and feeding network loaded. The chip-package co-EM simulation method is used in our study to characterize its performance.

5.2.1 Geometry

Fig. 5.8 shows the configurations of the UWB ICPA in a $20\times10\times1.2$ mm^3 LTCC package. The package ceramic material is DuPont 951 with a relative permittivity and loss tangent of 7.8 and 0.0015, respectively. The ICPA is formed by the 10-μm thick silver metallization. As shown in Fig. 5.8 (a) of its 3-D top view three ceramic layers are observed to form the package. The top layer is a 0.4-mm thick radiator layer with an antenna on the surface and a truncated ground plane on the back. The middle layer is 0.4 mm thick with a small cavity of $2.5\times2.5\times0.4$ mm^3. The bottom layer is 0.4 mm thick with a large cavity of $4.1\times4.1\times0.4$ mm^3. Both of them form a package cavity to load a chip. Considering the overwhelming dominance of CMOS integrated circuits and their great potentials to realize the integration of the single-chip UWB CMOS wireless transceiver a silicon chip with the dimensions of $2\times2\times0.4$ mm^3 is



(a)



(b)

Figure 5.8: UWB ICPA: (a) 3-D top view and (b) 3-D bottom view and feeding network structure zoom in view.

loaded into the cavity in our study as clearly shown in Fig. 5.8 (b) of the 3-D bottom view. It should be noted that the UWB CMOS chip is adhered to the cavity base of the common ground plane. This configuration will contribute to the shielding of the CMOS chip from the UWB ICPA.

The zoom in view in Fig. 5.8 (b) shows the detailed antenna feeding network structure. The transmitted signal from the UWB transceiver chip will be firstly fed to the bond wires and CPW1, then feed to the CPW2 by a via through a ground plane aperture, and finally feed to the antenna to radiate the EM energy to the external environment. While for the received signal it is a reverse process. The CPWs and via are made of silver, while the bond wires are assumed to be made of gold to minimize signal transmission loss.

5.2.2 Design and characterization

The design of the UWB ICPA as shown in Fig. 5.8 has many trade off parameters to be considered as the normal antenna design, such as return loss, radiation pattern, gain, radiation efficiency etc. However, the big difficulty lies in the ultra wide band impedance matching. It has to be designed to cover the UWB bandwidth of 5.5-10.6 GHz. In this study, an integrated UWB antenna is first designed and some techniques are used to optimize its shape to achieve good integration impedance matching. Then the feeding network for integration is designed to achieve good matching to 50 Ω in 5.5-10.6 GHz. After that, the feeding network and antenna are combined to characterize the ICPA performance to ensure other parameters meet the requirement.

A. *Antenna design and optimization*

In the UWB integrated antenna design, with reference to the structure of Fig. 5.8 the antenna is feed directly by a lumped port from ground plane with the whole feeding network deleted in simulation. The objective is to characterize the performance of the UWB antenna without feeding network. The initial antenna shape is shown in Fig. 5.9 as type ***a*** with a small footprint of 6.18×11.35 mm^2. As shown in Fig. 5.9 this antenna has UWB performance with 8.5-dB return loss bandwidth in the range of 5.45-11.85 GHz. However, the matching around 7 GHz is not good enough. By observing the antenna current distribution, a slot of $0.15\times0.5\times0.01$ mm^3 has been added in the location with high current distribution as type ***b*** shown in Fig. 5.9 to further achieve the good matching around 7 GHz. As seen from Fig. 5.9 this technique successfully makes the 10-dB return loss bandwidth in the range of 5.25-12.8 GHz. Another consideration in LTCC technology is the good mechanical property. For this purpose a slot of $2\times2\times0.01$ mm^3 has been added based on the design of the type ***b***. This slot is chosen to be located at the place of low current distribution. This technique will make the designed antenna as type ***c*** achieve the expected mechanical property while having no influence on its electrical property. This is confirmed by the S_{11} result in Fig. 5.9. It can be seen that the 10-dB return loss bandwidth still remains in the range of 5.3-12.6 GHz.

B. *Feeding network design*

As shown in the zoom in view of the Fig. 5.8 (b) the whole feeding network

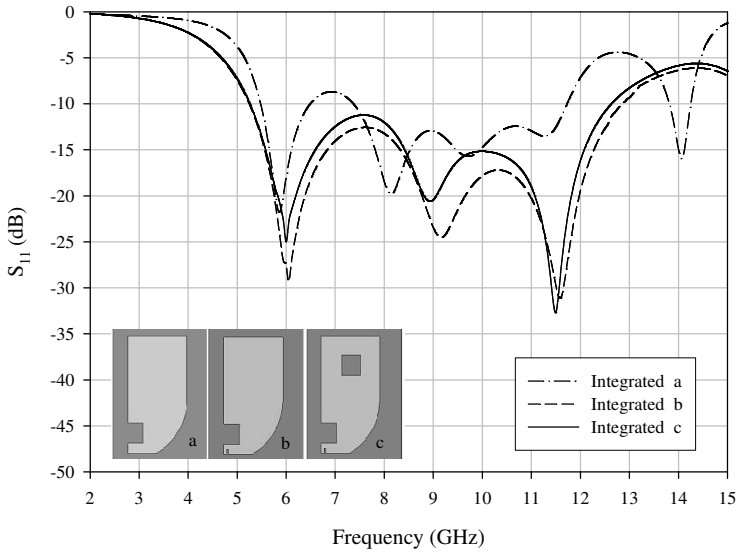


Figure 5.9: Impedance matching optimization of the integrated UWB antennas.

includes bond wires, CPW1, via, and CPW2. It is noted that the ground traces of the CPWs are shorted to the common ground plane. In our design the CPW1, bond wire-CPW1, CPW2, CPW1-via-CPW2 will be designed respectively. With reference to the complete structure of Fig. 5.8 only the antenna and the unrelated feeding network parts are deleted in simulation for the respective part. This partial optimization skill will make it easy to find the design difficulties and save the simulation time. In addition, to ease the design only the return loss is considered, the CPW ground trace has the same width with the signal trace, the gap between the signal trace to the ground trace is fixed at 0.15 mm, and the radius of the shorted via is fixed at 0.05 mm.

Fig. 5.10 shows the simulated S_{11} of every part. Although 50-Ω CPW in normal configurations can be easily designed using some free softwares, such as APPCAD, the HFSS simulation can be used to further characterize its performance inside a custom package. For this purpose, the CPW1 and CPW2 are designed in Fig. 5.10 (a) and

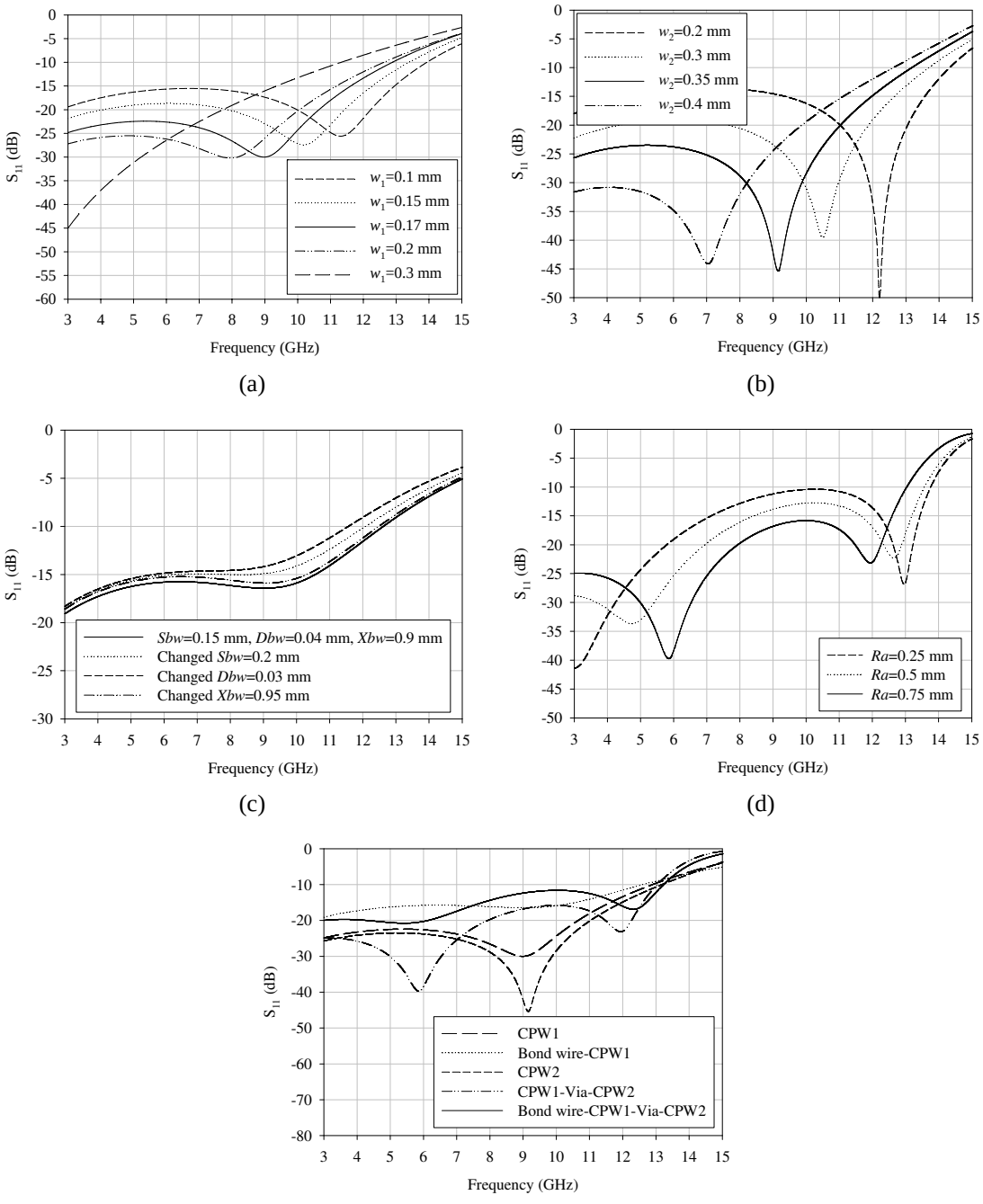


Figure 5.10: S_{11} of the feeding network: (a) CPW1, (b) CPW2, (c) Bond wire-CPW1, (d) CPW1-via-CPW2, and (e) optimized results.

(b) respectively. For the CPW1 design its trace length is fixed at 1.8 mm to remain the structure consistency while its width w_1 is varied to optimize the CPW return loss performance. It is seen from Fig. 5.10 (a) that the best $S_{11} < -20$ dB for the frequency range of 5.5-10.6 GHz is obtained at w_1 = 0.17 mm. For the CPW2 design its trace length is fixed at 2.3 mm while its trace width w_2 is varied to optimize the CPW return loss performance. It is seen from Fig. 5.10 (b) that the best $S_{11} < -20$ dB for the frequency range of 5.5-10.6 GHz is obtained at w_2 = 0.35 mm. The bond wire is designed using the bond wire and optimized CPW1 combined structure. The designed parameters are *Xbw*, *Dbw* and *Sbw*, where *Xbw* is the bond wire length, *Dbw* is the bond wire diameter, and *Sbw* is the gap between the neighboring bond wire feed via centers. It is seen from Fig. 5.10 (c) that the best $S_{11} < -15$ dB for the frequency range of 5.5-10.6 GHz is obtained at *Sbw* = 0.15 mm, *Dbw* = 0.04 mm and *Xbw* = 0.9 mm. The via between CPW1 and CPW2 is designed using optimized CPW1, via and optimized CPW2 combined structure. The aperture radius *Ra* is varied to optimize the return loss performance. It is seen form Fig. 5.10 (d) that the best $S_{11} < -15$ dB is obtained at *Ra* = 0.75 mm. The whole feeding network performance is then obtained by simulating the optimized parts combined structure. It is seen form Fig. 5.10 (e) that $S_{11} < -11$ dB is obtained. This shows that the feeding network can achieve good matching to 50-Ω source.

C. Characterization of UWB ICPA

After the antenna optimization and feeding network design, the characteristics of

the UWB ICPA feeding from the CMOS chip as shown in Fig. 5.8 should be studied. The excitation comes from the transceiver chip. Using the optimized structures for every part the combined structure shows the good impedance matching characteristics as shown in Fig. 5.11. The 10-dB return loss bandwidth is found to be 6.7 GHz from 5.05 to 11.75 GHz, which indicates good matching to a 50-Ω source in an ultra wide frequency band.

Fig. 5.12 shows the simulated impedance characteristics of the UWB ICPA. The impedance characteristics give insight on how the ICPA achieve resonant frequencies. Here the resonant frequency is defined as where the reactance of the input impedance is equal to zero. It is evident from Fig. 5.12 that the impedance characteristics at a specific resonant frequency exhibit a small peak in the resistance and a gentle swing in the reactance from inductive to capacitive. The multi-resonant characteristic can be clearly observed in Fig. 5.12. This multi-resonant characteristic is useful to make the ICPA achieve the ultra wide band performance [80].

Fig. 5.13 shows the UWB ICPA radiation patterns in both E (YZ) and H (XZ) planes at 5.05 GHz, 8 GHz, and 11.75 GHz respectively. According to the figures, the E-plane pattern exhibits dual-polarized properties at all frequencies while the H-plane pattern is relatively uniform at lower frequencies. The cross-polarization component is generally lower than the dominant one for the H-plane pattern at all frequencies. While for the E-plane pattern the cross-polarization component becomes more significant at the higher frequency.

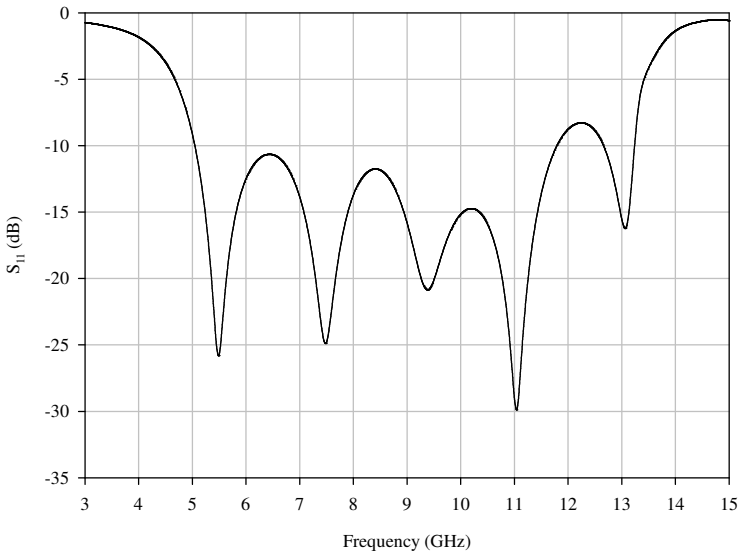


Figure 5.11: UWB ICPA S_{11}.

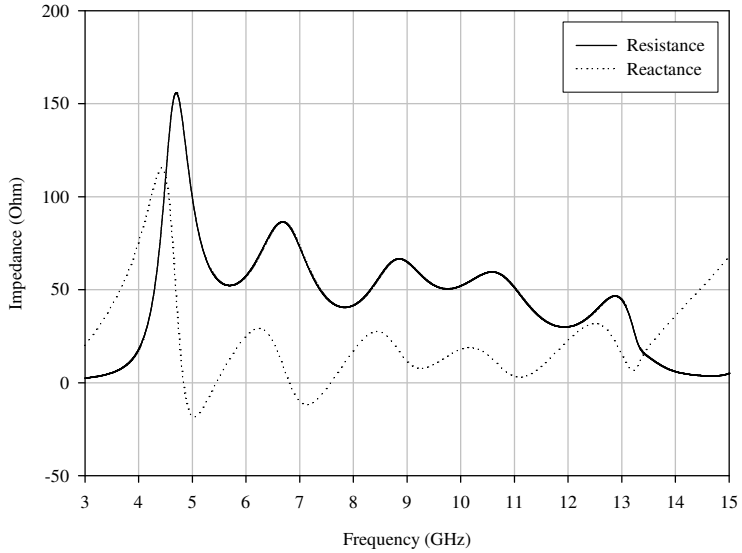


Figure 5.12: UWB ICPA impedance.

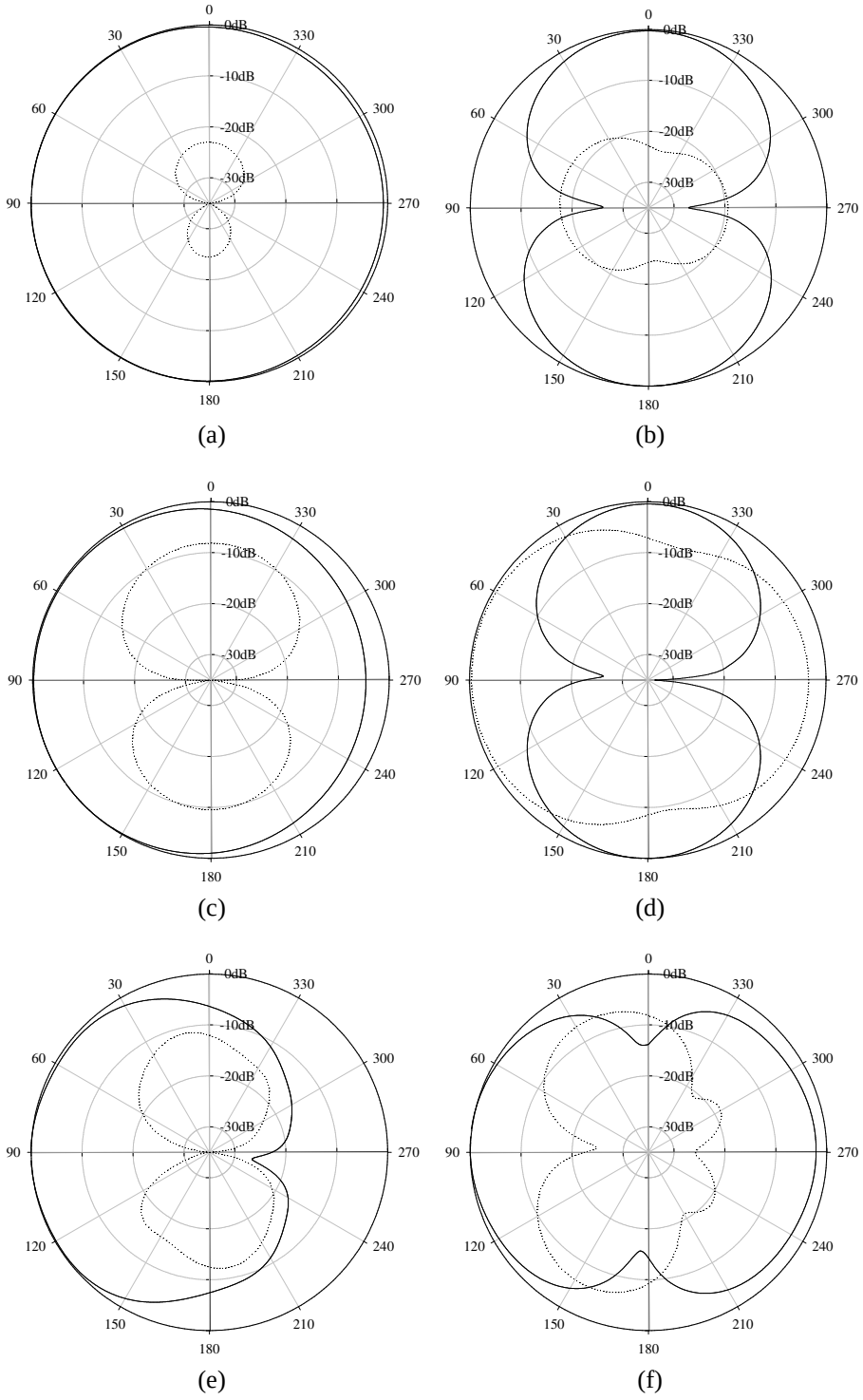


Figure 5.13: UWB ICPA radiation patterns with solid lines for co-polarization components and short dash lines for cross-polarization components: (a) H plane at 5.05 GHz, (b) E plane at 5.05 GHz, (c) H plane at 8 GHz, (d) E plane at 8 GHz, (e) H plane at 11.75 GHz, and (f) E plane at 11.75 GHz.

The simulated UWB ICPA achieves the high radiation efficiency $>$ 96% at 5.05 GHz, 8 GHz, and 11.75 GHz. The gain versus frequency characteristic is also shown in Fig. 5.14. The gain of an antenna is a critical parameter in wireless network design. The high antenna gain is often required to extend the network coverage. It is evident from Fig. 5.14 that the gain varies from 2.5 to 4.3 dBi over the simulated UWB frequency range.

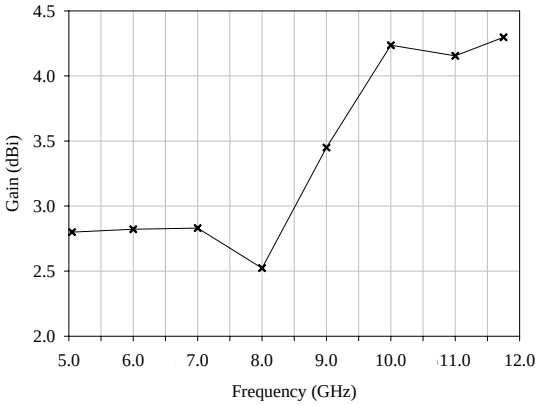


Figure 5.14: UWB ICPA gain.

5.3 LTCC-Based 60-GHz ICPA

The LTCC-based 60-GHz ICPA is designed not only as antenna but also as a package that can carry a single-chip 60-GHz IBM radio transceiver. In this section, three ICPA candidates are presented to cover the 58-65 GHz frequency band with antenna efficiency $\geq$ 77% and available radiation patterns. This work provides the potentials of realizing 60-GHz single-package radios.

5.3.1 Geometry

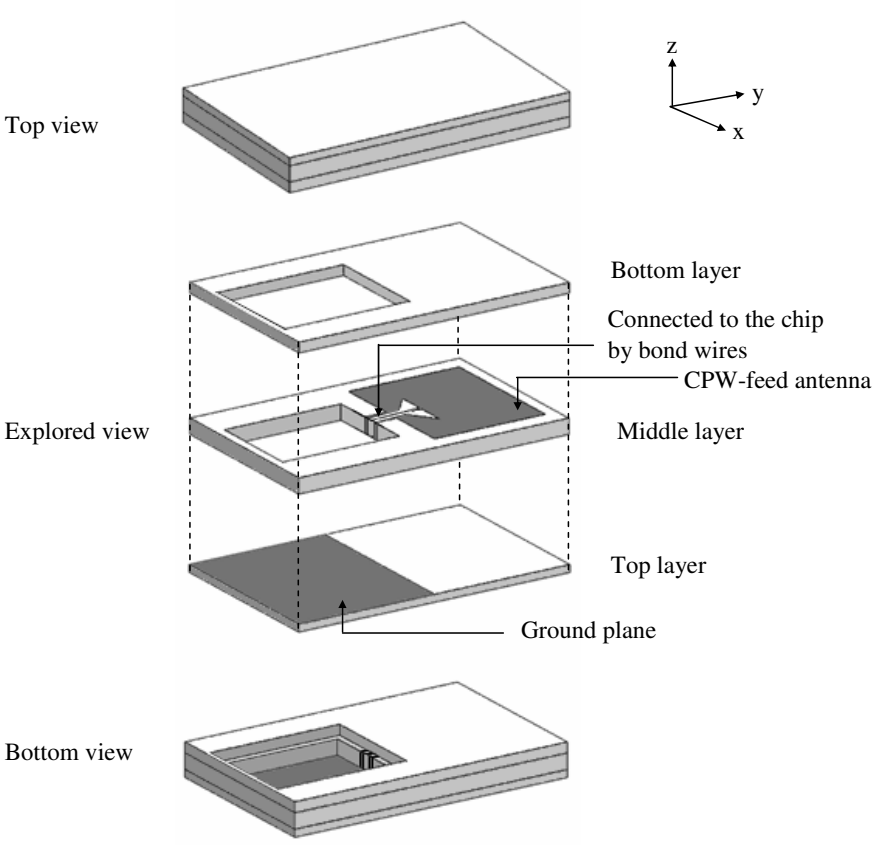
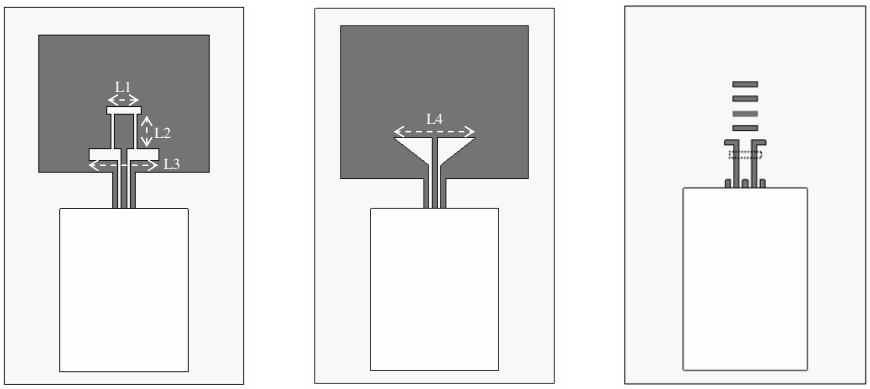


Figure 5.15: 60-GHz ICPA 3D view.

Fig. 5.15 shows the configuration of the designed 60-GHz ICPA in a 11×7×1.3 mm^3 LTCC package. The package ceramic material is LTCC ferro-A6 with a relative permittivity and loss tangent of 5.9 and 0.002, respectively. The ICPA is formed by the 10-μm thick silver metallization. As shown, three ceramic layers are observed to form the package. The top layer is 0.3 mm thick with a truncated ground plane on the back. The middle layer is 0.6 mm thick with a small cavity and with the antenna on the back or inside the layer. The bottom layer is 0.4 mm thick with a large cavity. Both of them form a package cavity to load a chip. It should be noted that the transceiver chip is adhered to the cavity base of the common ground plane. This configuration will contribute to the shielding of the chip from the antenna. In addition, the aperture feeding scheme using via through ground is avoided here to minimize the transmission loss at high frequency band of 60 GHz. Instead the CPW single or differential feeding directly from the signal trace of the chip is adopted. The central distance between ground line and signal line is 250 μm.



(a) (b) (c)

Figure 5.16: 60-GHz ICPA layout: (a) WB-slot ICPA, (b) WB-triangle ICPA, and (c) Yagi ICPA.

Fig. 5.16 (a) and (b) show the layout of a CPW-feed wideband slot (WB-slot) 60-GHz ICPA and a CPW-feed wideband triangle (WB-triangle) 60-GHz ICPA, respectively. They are designed as single-chip packages with a $4.75\times3.75\times0.6$ mm^3 small cavity and a $5.25\times4.25\times0.4$ mm^3 large cavity to carry a single-chip 60-GHz IBM receiver with size of $3.4\times1.7\times0.46$ mm^3 [25]. Fig. 5.16 (c) shows the layout of a differential CPW-fed Yagi 60-GHz ICPA. It consists of one driven element, four director elements on the back of the middle layer, and one reflector element 100 μm deeper inside the middle layer. This antenna is designed as a single-chip package with a $5.3\times3.6\times0.6$ mm^3 small cavity and a $5.8\times4.1\times0.4$ mm^3 large cavity to carry a single-chip 60-GHz IBM transmitter with size of $4.0\times1.6\times0.46$ mm^3 [25].

5.3.2 Design and characterization

The 60-GHz ICPAs were designed in HFSS. The design difficulty still remains in achieving the ultra-wide band impedance matching. The CPW-fed hybrid slot antenna (HAS) achieves impedance bandwidth up to 57% at 4.7 GHz [81]. This structure is the combination of the generalized CPW open-end slot antenna with the standard CPW slot antenna. The center frequencies of the two structures were kept slight apart to increase the bandwidth of the overall structure. The antenna is redesigned at 60 GHz with the layout as shown in Fig. 5.16 (a), where $L3 = 2L1 = 2L2 = \lambda$. The wavelength λ at 60 GHz is 2.2 mm for the simulated structure. It is found from Fig. 5.17 that 10-dB return loss bandwidth is 17.8 GHz from 51.6 to 69.4 GHz, which indicates good matching to a 50-Ω source at 60-GHz frequency band.

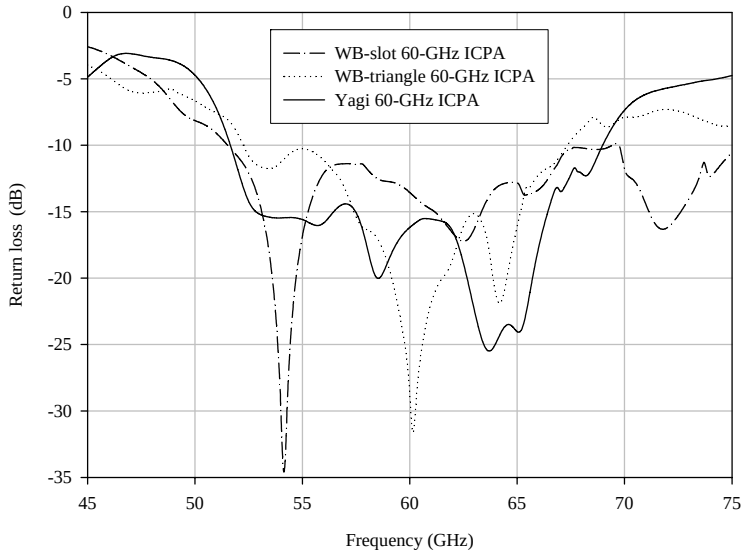


Figure 5.17: 60-GHz ICPA return loss.

The beveled structure is well known for its wideband impedance matching [82]. We creatively use this structure in our design for the WB-triangle antenna with the layout as shown in Fig. 5.16 (b), where $L4 = \lambda$. It is found from Fig. 5.17 that 10-dB return loss bandwidth is 15 GHz from 52.3 to 67.3 GHz, which indicates good matching to a 50-Ω source at 60-GHz frequency band.

For the differential Yagi ICPA with the layout as shown in Fig. 5.16 (c), the return loss is defined as follows,

$$RL = 20 \lg \left(\frac{Z_d - Z_0}{Z_d + Z_0} \right) \tag{5.6}$$

Where Z_d is the input impedance of the differential driven antenna, calculated using two port Z-parameters as $Z_d = 2(Z_{11} - Z_{21}) = 2(Z_{22} - Z_{12})$. Z_0 is of typical value of 100 Ω, 300 Ω or 600 Ω. In this study we choose 100 Ω in our calculation. It is found from Fig. 5.17 that 10-dB return loss bandwidth is 17.2 GHz from 51.7 to 68.9 GHz,

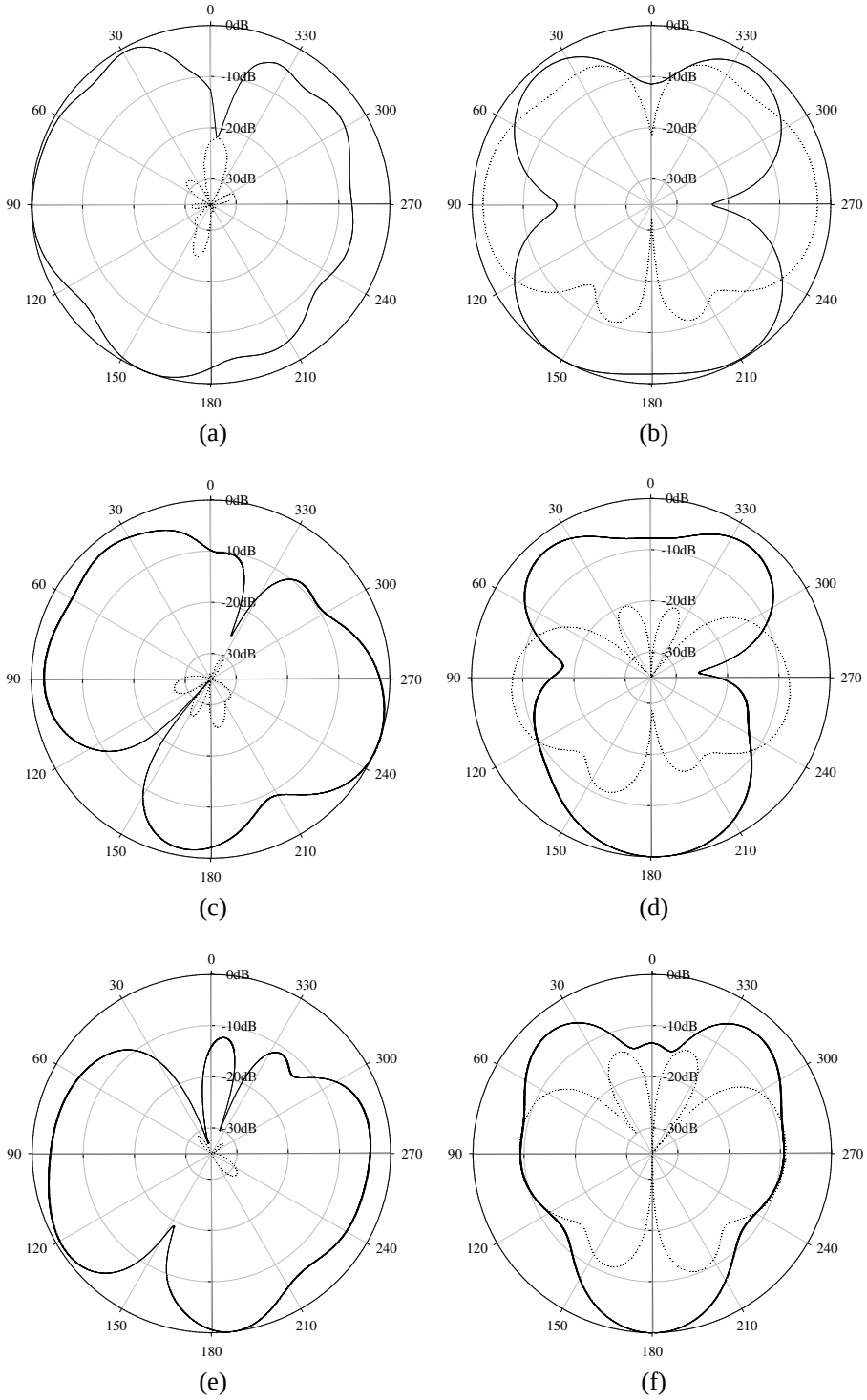


Figure 5.18: 60-GHz ICPA radiation patterns at 60 GHz with solid lines for co-polarization components and short dash lines for cross-polarization components: (a) H plane for WB-slot ICPA, (b) E plane for WB-slot ICPA, (c) H plane for WB-triangle ICPA, (d) E plane for WB-triangle ICPA, (e) H plane for Yagi ICPA, and (f) E plane for Yagi ICPA.

which indicates good matching to a 50-Ω source at 60-GHz frequency band.

Fig. 5.18 shows the designed ICPA radiation patterns in H (XZ) and E (YZ) planes at 60 GHz. As shown the E-plane patterns exhibit dual-polarized properties. It is also found that the H-plane patterns have very small cross-polarization components while for the E-plane patterns they are significant. In addition, the simulated ICPAs all achieve the high radiation efficiency $> 95\%$ at 60 GHz.

5.4 Inter-Chip Wireless Interconnect Using On-Package Antennas and UWB Radios

5.4.1 System description

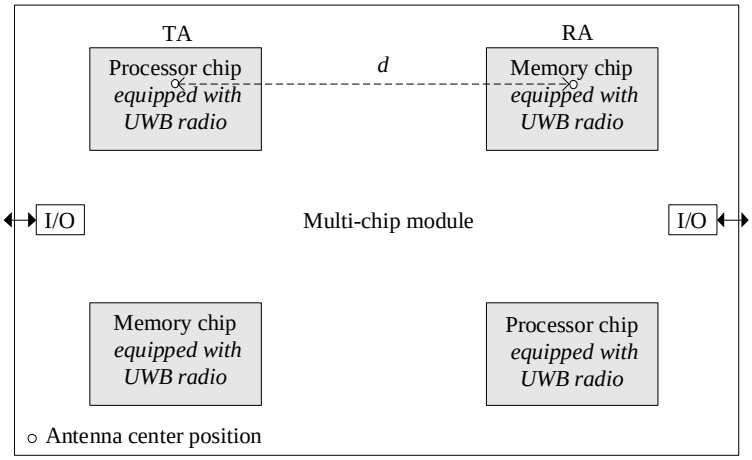


Figure 5.19: Inter-chip wireless interconnect system.

Fig. 5.19 shows the inter-chip wireless interconnect system within a multichip module. It employs a UWB impulse radio to realize a wireless peripheral component interconnect express (PCIe) as detailed in [83], while conventionally the PCIe circuits are used for wire interconnects between chips. This novel interconnect has such ad-

vantages as scalability and reconfigurability. It can also be used at the system level to attain fault tolerance, because one can reconfigure the multichip module by software commands to debug and then to eliminate the fault chips via reconfiguration [84].

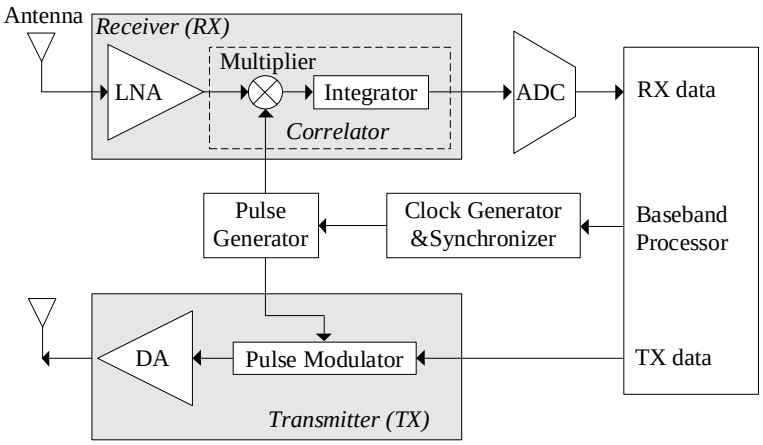


Figure 5.20: Architecture of UWB radio.

Fig. 5.20 shows the block diagram of the UWB radio architecture [83]. As shown, the transmitter comprises a UWB Gaussian pulse generator, modulator, and driver amplifier (DA). The receiver consists of a UWB low-noise amplifier (LNA), a correlator, an analog-to-digital converter (ADC), and clock generation and synchronization circuits. A UWB Gaussian pulse is firstly generated by the pulse generator and then modulated by the pulse modulator. The modulated pulse is then amplified by the UWB DA and finally transmitted by the UWB transmit antenna (TA). The wireless signal is then detected by the UWB receive antenna (RA) and then amplified to a suitable level for signal processing as well as provided enough gain so as to overcome noise in subsequent stages. The data is subsequently recovered by the correlator. The ADC is used to convert the analog demodulated signal into the digital signal. The digital baseband

provides control for the clock generation, synchronization, and data processing.

A UWB radio requires UWB antennas. The beveled monopole UWB antenna fabricated in LTCC substrate as shown in Fig. 5.1 will be adopted in this system. It has S_{11} lower than -10 dB from 3.1 to 10.6 GHz, indicating an acceptable matching to a 50-Ω source. As shown in Fig. 5.19 a unique inter-chip wireless channel is formed between the TA and RA. A transfer function $H(f)$ is defined in the frequency domain for the inter-chip wireless channel as the ratio of $x_{in}(t)$, the signal applied to the TA, to $x_{out}(t)$, the signal received by the RA. In our study $H(f)$ will be characterized by the experimental method. The UWB radio adopts the pulse position modulation (PPM) scheme. The PPM signal $x_{in}(t)$ applied to the TA is the same as eq. (2.2) but with the basic UWB pulse $g(t)$ modified to the fourth derivative of a Gaussian function pulse as expressed in eq. (5.2) and with the waveform shown in Fig. 5.6 (a). It is found from Fig. 5.7 that the PSD of this modified $g(t)$ complies with the required FCC indoor emission mask which occupies the whole 7.5-GHz UWB bandwidth from 3.1 to 10.6 GHz. Given the signal applied to the TA $x_{in}(t)$ and the experimentally characterized $H(f)$ the channel output signal $x_{out}(t)$ is easily obtained using the Fourier inverse transform.

In what follows the theoretical performance of the inter-chip wireless interconnect system of Fig. 5.19 with interconnect length *d* of 20 cm will be evaluated. The UWB radio operates with the radiated power spectral density < -41.3 dBm/MHz (or the average transmitted power P_t less than -2.55 dBm) to meet the emission regulation

over the UWB from 3.1 to 10.6 GHz.

5.4.2 System performance evaluation

A. Characterization of inter-chip wireless channel

The transmit and receive antenna pairs, each the mirror image of the other with the separation distance of 20 cm, were placed in a test multi-chip module PCB board as illustrated in Fig. 5.19 for measurement. The channel transfer function $H(f)$ was then measured to characterize the inter-chip wireless channel. Fig. 5.21 shows the measured transfer function $H(f)$. It is seen that both amplitude and phase of the transfer function $H(f)$ fluctuate with frequency indicating that the inter-chip wireless channel supports the transmission of multi hybrid electromagnetic modes. The inter-chip wireless channel can be regarded as a Rician fading channel. This treatment agrees with the measurements of the radio signal transmission from 2 to 12 GHz. In addition, the time-delay spread of the inter-chip wireless channel is calculated to be negligible as compared with the date rate considered here, and the external interferences are insignificant as the module can be well shielded. Hence, over such a nondispersive Rician fading channel, the system performance depends on the signal-to-noise ratio (SNR) [83].

Fig. 5.22 shows the channel loss L_c with the varying data rate. The channel loss that equals to the energy difference between the received signal and the transmitted signal is computed from the measured channel transfer function. It is evident from the

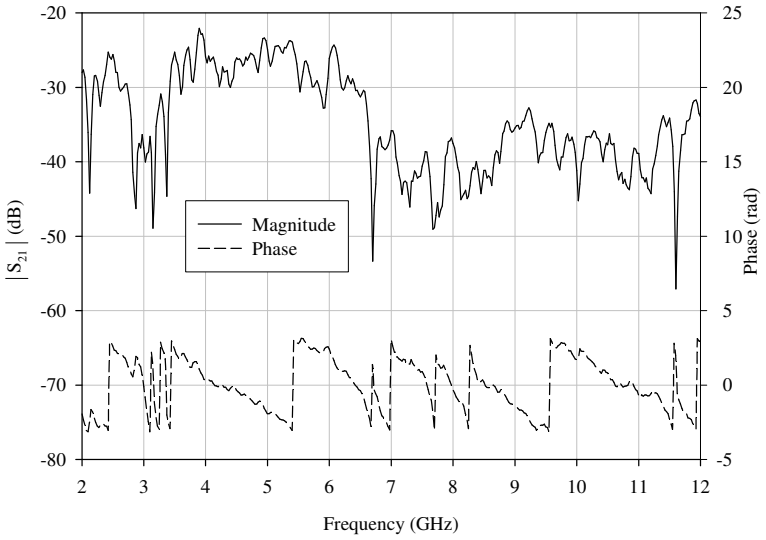


Figure 5.21: Measured $H(f)$.

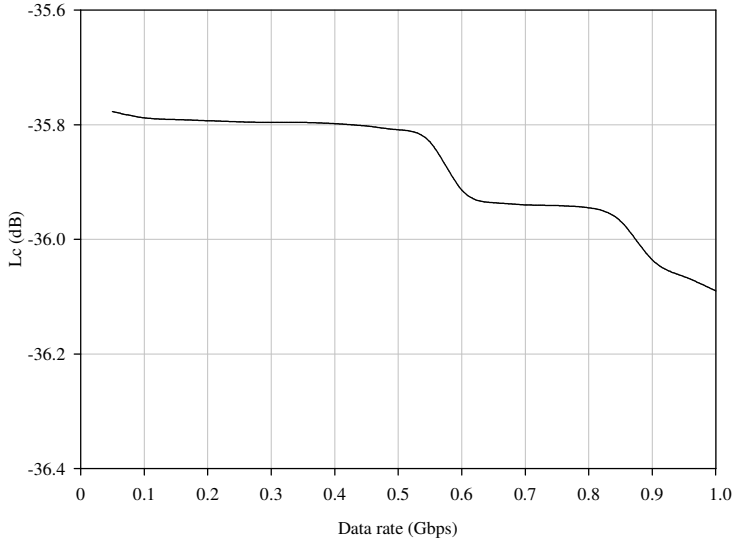


Figure 5.22: Channel loss versus data rate.

figure that the channel loss increases with data rate.

Note that the metal lines and solder bumps exist in a multichip module environment. Their existence may increase or decrease the channel loss depending on their layout, without changing the Rician fading characteristic of the inter-chip wireless channel [65].

B. BER performance

The performance of the inter-hip wireless interconnect system will be evaluated in terms of BER under the assumption of perfect system synchronization. The signal corruption is assumed to be caused by the thermal and switching noise.

In the average bit SNR Γ_b calculation the method presented in section 3.2.1 also can be applied for this inter-chip case, except that the eq. (3.4) should be changed to the equation as follows based on the channel loss L_c

$$E_{rb} = E_{tb} \cdot L_c \cdot G_r \cdot L_m \tag{5.7}$$

The receiver noise figure F_r is reasonably assumed to be 15 or 10 dB [63, 64]. The switching noise is assumed to be T = 10 dB or T = 5 dB lower than the thermal noise according to the measured result [66]. The other parameters used in the evaluation are all reasonable values with G_r = 15 dB, L_m = -4 dB, and K = 10 dB. All above parameters are used to calculate the value of Γ_b.

In BER calculation, we have $P_{b|x}$ acoording to eq. (2.13) for UWB PPM scheme.

$$P_{b|x} = \frac{1}{2} erfc\left(\sqrt{\frac{(1-\rho)\cdot x}{2}}\right), \tag{5.8}$$

where ρ has been presented in eq. (2.14). The above $P_{b|x}$ has the general form of eq. (3.13). Using the BER expression derived as eq. (3.12) we finally get the BER as follows that is precise and easily computed numerically.

$$P_b = \frac{1}{2\pi}\cdot\frac{1+K}{\Gamma_b}\cdot\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \frac{1}{\frac{1-\rho}{2}\sec^2\theta + \frac{1+K}{\Gamma_b}} \exp\left(\frac{-K\frac{1-\rho}{2}\sec^2\theta}{\frac{1-\rho}{2}\sec^2\theta + \frac{1+K}{\Gamma_b}}\right)\cdot d\theta \tag{5.9}$$

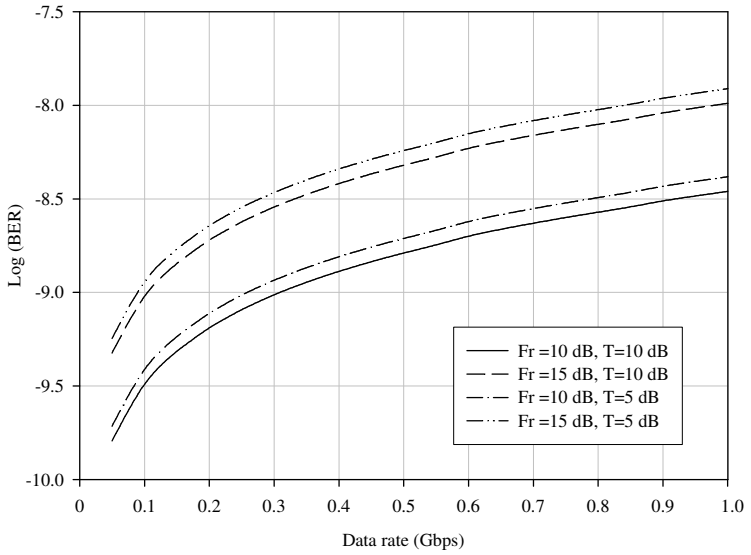


Figure 5.23: BER versus data rate at 20 cm distance.

Fig. 5.23 shows the BER versus data rate at 20 cm distance. As expected, the BER performance degrades with data rate. Taking the worst case as an example, for the fixed 20-cm distance, it degrades from $10^{-8.9}$ at 0.1 Gbps to $10^{-7.9}$ at 1 Gbps. It is shown that the system can support a data rate of 1 Gbps with a BER $< 10^{-7}$ up to an

interconnect distance of 20 cm with radiated power density less than −41.3 dBm/MHz.

Chapter 6

Conclusions & Recommendations

6.1 Conclusions

Chip scale wireless interconnect systems have been analyzed in terms of bit error rate (BER) performance and studied in terms of their antennas, including on-chip antennas for intra-chip wireless interconnects and on-package antennas for inter-chip wireless interconnects.

In chapter 2, a novel inter-chip RF-interconnect (RFI) system has been proposed and analyzed in terms of BER performance. It is concluded that a high interconnect data rate of 3.33 giga bits per second (Gbps) with a low BER $< 10^{-5}$ up to an inter-chip interconnect distance of 3 cm is achievable with the average transmitted power less than -2.85 dBm.

In chapter 3, an intra-chip wireless interconnect system has been studied in terms of BER performance. A method has been presented to evaluate the system BER. The BER

performance of various digital modulation schemes in the system has been evaluated at 25 GHz, including coherent MASK, MPSK, MQAM, GMSK and MSK, as well as noncoherent MFSK and MDPSK. It is concluded that by taking feasible measures a high data rate at 2 Gbps with a low BER $< 10^{-5}$ up to an intra-chip wireless channel of length 2 cm is achievable under the reasonable SNR budget.

In chapter 4, on-chip antennas for intra-chip wireless interconnects have been studied, including on-chip dipole antennas, on-chip 60-GHz inverted-F and quasi-Yagi antennas, as well as on-chip monopoles.

On-chip dipole antenna pair on the grounded silicon substrate has been analyzed to obtain its transmission mechanism for commonly used broadside configuration. The theoretical analysis shows that for a single propagating mode the mutual coupling will be mainly due to direct, high order and leaky waves with minimal TM mode surface wave contribution, while for two propagating modes the TE mode surface wave will be excited and dominated in the coupling. On-chip dipole pair has also been simulated for more complex structures. The effect of the separation distance, the process including micromaching, back-end-of-line (BEOL), and proton implantation, as well as the effect of the interference structures on the dipole pair performance have been studied by characterizing S_{11} and S_{21} parameters. It is concluded that the BEOL, micromaching, and proton implantation methods should be optimized in design to take their advantages. It is also concluded that the existence of metal lines between antenna pairs may improve the antenna transmission performance.

6.1 Conclusions

On-chip 60-GHz inverted-F and quasi-Yagi antennas have been designed, fabricated, and characterized. The design was made using the Zeland IE3D software package. The fabrication was realized with the BEOL process of silicon substrates of low resistivity 10 Ω.cm. The characterization was conducted on wafer with Cascade Microtech coplanar probes and an HP8510XF network analyzer. The results show that the inverted-F antenna achieved a minimum return loss of 32 dB and a gain of -19 dBi at 61 GHz; while the quasi-Yagi antenna a minimum return loss of 6.75 dB and a gain of -12.5 dBi at 65 GHz. Good agreement has been observed between the measured and simulated result. Results also show that a high transmission gain of -46.3 dB at 61 GHz is achieved from the pair of inverted-F antennas at the separation of 10 mm on the standard 10-Ω.cm silicon wafer of thickness 750 μm.

On-chip monopoles of axial length 1 mm have been fabricated on silicon substrates of high resistivity 5 KΩ.cm and low resistivity 10 Ω.cm, respectively. We measured their performance up to 110 GHz for wireless interconnects. Reflection measurements show that a sharp resonance can be seen at 75 GHz for the meander monopole and two at 67 and 104 GHz for the zigzag 30° monopole on the silicon substrate of high resistivity but no such sharp resonance can be seen for them on the silicon substrate of low resistivity. Transmission measurements show that a high gain window exists. It suggests that the operating frequency of wireless interconnects be allocated within the high gain window for good performance. The metal lines running parallel with or vertical to the monopole pairs were also observed to improve the highest gain of this window area.

A novel intra-chip wireless interconnect system using on-chip meander monopole antennas and UWB radios that operate in 22-29 GHz has finally been studied in chapter 4. It is shown that the system on the 10-Ω.cm substrate can support a data rate of 1.5 Gbps with a BER $< 10^{-5}$ up to an intra-chip wireless channel of length 10 mm with the average transmitted power of 0 dBm; while the system on the 5-KΩ.cm substrate can support a data rate of 3.5 Gbps with a BER $< 10^{-6}$ up to an intra-chip wireless channel of length 40 mm with the same transmitted power.

In chapter 5, LTCC-based on-package antennas for inter-chip wireless interconnects have been studied, including a discrete beveled monopole UWB antenna, a UWB integrated circuit package antenna (ICPA), and 60-GHz ICPAs.

The beveled monopole UWB antenna has been fabricated with size of $17\times10\times1$ mm^3. It has achieved impedance bandwidth of 8.25 GHz from 2.85 to 11.1 GHz, gain from -5.6 to 2.3 dBi, and broad patterns. In addition, both frequency domain and time domain characteristics of the beveled antenna are also carefully investigated with a normalized measured transfer function. They all proved applicability of this beveled monopole antenna in UWB radios.

The UWB ICPA with a small footprint of 6.18×11.35 mm^2 has been designed for the fist time in a $20\times10\times1.2$ mm^3 LTCC package format with feeding network and CMOS transceiver chip loaded. The chip-package co-EM simulation method is used. A design guideline based on the return loss parameter is illustrated. Results show that the UWB ICPA achieves a 10-dB return loss bandwidth of 6.7 GHz which covers

the upper UWB band from 5.05 to 11.75 GHz, gain from 2.5 to 4.3 dBi, radiation efficiency $>$ 96%, and broad radiation patterns. This work provides the potentials to realize a single-package UWB radio.

The 60-GHz ICPAs have been designed, including the WB-slot and WB-triangle ICPAs to carry the IBM receiver chip, as well as the differential driven Yagi ICPA to carry the IBM transmitter chip. All designed ICPAs achieve the good impedance matching at 60-GHz frequency band from 58 to 65 GHz with antenna efficiency $\geq$ 95% and available radiation patterns. This work provides the potentials to realize 60-GHz single-package radios.

A novel inter-chip wireless interconnect system using on-package beveled monopole antennas and UWB radios that operate in 3.1-10.6 GHz has finally been studied in chapter 5. It is concluded that a high data rate of 1 Gbps with a low BER $< 10^{-7}$ over an inter-chip wireless channel of length 20 cm can be achieved with the radiated power spectral density less than -41.3 dBm/MHz.

6.2 Recommendations

This thesis only focuses on the study of chip scale wireless interconnect systems and their antennas. The detailed design and implementation should be further carried out. The recommendations are listed as follows:

First, we only evaluated the BER performance of chip scale wireless interconnect

system in theory. The transceiver circuit blocks and integrated antennas should be implemented to realize the complete intra- or inter- chip wireless interconnect system and obtain its measured performance, where the UWB transceiver blocks can be good candidate according to our study.

Second, according to different chip scale wireless interconnect systems there are different suitable antennas. The study should be further carried on to investigate the antenna candidates. The advanced process technologies or fabrication techniques should be investigated to further improve the antenna transmission gain.

Third, we fabricated the on-chip monopoles, inverted-F and quasi-Yagi antennas. Their performance should be further characterized by connected with the designed transceiver circuits. We analyzed on-chip dipole pair. It should be further fabricated and tested for intra-chip wireless interconnects. In addition, we only designed LTCC-based UWB ICPA and 60-GHz ICPAs . It provides the potentials to further realize the single-package radios. The fabrication and measurement should be carried on for these ICPAs, which not only behave as antennas but also as packages that can carry the single-chip UWB or 60-GHz radio transceivers for inter-chip wireless communications.

Fourth, for intra- and inter-chip wireless interconnect systems their channel should be further characterized using experimental and theoretical methods. Although we have obtained some results, the further study will greatly facilitate the system performance analysis.

Author's Publications

International Journal Papers

1. **M. Sun** and Y. P. Zhang, "Performance of Inter-Chip RF-interconnect Using CPW, Capacitive Coupler and UWB Transceiver," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 9, pp. 2650-2655, 2005.

2. Y. P. Zhang, **M. Sun**, and L. H. Guo, "On-Chip Antennas for 60-GHz Radios in Silicon Technology," *IEEE Transactions on Electron Devices*, vol. 52, no. 7, pp. 1664-1668, 2005.

3. Y. P. Zhang and **M. Sun**, "Dual-Band Microstrip Bandpass Filter Using Stepped Impedance Resonators with New Parallel-Coupled Schemes," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 10, pp. 3779-3785, 2006.

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5. Y. P. Zhang, **M. Sun**, and W. Fan, "Performance of Integrated Antennas on Silicon Substrates of High and Low Resistivities up to 110 GHz for Wireless Interconnects," *Microwave and Optical Technology Letters*, vol. 48, no. 2, pp. 302-305, 2006.

6. Y. P. Zhang, L. H. Guo, and **M. Sun**, "High Transmission Gain Inverted-F Antenna on Low Resistivity Si for Wireless Interconnect," *IEEE Electron Device Letters*, vol. 27, no. 5, pp. 374-376, 2006.

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10. **M. Sun** and Y. P. Zhang, "Miniaturization of Planar Monopole Antennas for Ultrawide-Band Applications," submitted to *IEEE Transactions on Antennas and Propagation*, 2006.
11. **M. Sun** and Y. P. Zhang, "A Chip Antenna in LTCC for UWB Radios," submitted to *IEEE Transactions on Antennas and Propagation*, 2006.
12. Y. P. Zhang, Z. M. Chen, and **M. Sun**,"Propagation Mechanisms of Radio Waves over Intra-Chip Channels with Integrated Antennas: Frequency-Domain Measurements and Time-Domain Analysis," submitted to *IEEE Transactions on Antennas and Propagation*, 2006.

Patents

1. An Ultrawide-Band Integrated Circuit Package Antenna, NTU Ref: TD/066/05, Application Date: Oct. 10, 2005.
2. An Integrated Transceiver and Antenna package, IBM patent, Application date: Nov. 2, 2006.
3. Antenna-In-Package Design Techniques for Millimetre-Wave Highly-Integrated Wireless Devices, NTU Ref: TD/061/06, Application date: Nov. 6, 2006.

Conference Papers

1. **M. Sun** and Y. P. Zhang, "A Note on BER Calculation of Digital Modulation Schemes in Wireless Rician Fading Channels," *IEEE Region 10 Infocom Colloquium on Broadband Access Technology*, Singapore, 2004.
2. **M. Sun** and Y. P. Zhang, "Inter-Chip RF-interconnect Using CPW, Capacitive Coupler and UWB Transceiver," in *Proc. of Asia-Pacific Microwave Conference*, India, 2004.
3. **M. Sun** and Y. P. Zhang, "Modeling and Measurement of the On-chip Meander Antenna Pairs," in *Proc. of Asia-Pacific Microwave Conference*, China, 2005.
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7. Y. P. Zhang, **M. Sun**, K. M . Chua, L. L. Wai, D. Liu and B. P. Gaucher, "Antenna-in-Package in LTCC for 60-GHz Radio," submitted to *International Workshop on Antenna Technology 2007*, U.K.

8. **M. Sun** and Y. P. Zhang, "Miniaturization of Planar Monopole Antennas for Ultrawide-Band Applications," submitted to *International Workshop on Antenna Technology 2007*, U.K.

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APPENDIX

Interconnect technologies in future ULSI

Technologies	Pros	Cons	Interconnect performance
Introduction of low-resistivity copper and low-permittivity (k) dielectrics	• It provides performance and reliability enhancement compared with traditional wire interconnect.	• Integration of these new materials into integrated circuit fabrication is a formidable task, requiring material, process, design, and packaging innovations [1]. • The interconnect bandwidth is limited by the wire material.	The wire channel capacity is given by $10^{16}A/l^2$ bps, where A stands for the cross section of a wire and l for the length of the wire. Consider A = 30 um^2 and l = 1 cm, the wire channel capacity is 3 Gbps [2].
Optical interconnect	• It is attractive as off-chip or package/board application. The material bandwidth- limit doesn't exist. The only limit is the propagation delays of optoelectronic components such as transmitters, modulators, and receivers. • Optical interconnects used for off-chip and on-chip clock and signal distribution eliminate the hierarchical constraints imposed by off-chip electrical interconnects, i.e., the lower bandwidth and longer delay time.	• A module is needed to transform optical signals to electrical signals. • The relative size of optical components is a big issue and they exhibit serious challenges to be fabricated in silicon. • It is not cost-effective. The technology depends largely on components made of gallium arsenide and germanium, which are more expensive than silicon. • Alignment is also a more delicate matter in this optical technology. • An on-chip optical interconnect technology may require either impractical high levels of optical signal power or area intensive error correction circuits.	8 Gbps is realized for a high-speed 12-channel link (8 data channels) at the Intel Components Research Lab [3]. The optical I/O is based on an optoelectronic flip-chip pin grid array (FCPGA) package, and the key components of the hybrid package are gallium arsenide VCSELs, p-type intrinsic n-type doped silicon (PIN) photodiode arrays, acrylate polymer waveguide arrays, multiterminal fiber-optic connectors, and the 0.18-μm CMOS transceiver chip. The 3× 3.25 mm^2 transceiver chip occupies only one-third of the total chip area while containing all the circuits needed for use in optical-link transmission.

3-D integration	• 3-D integration has been shown to reduce the number and average length of 2-D global wires by providing shorter 'vertical' paths for connection. It allows minimal interconnection lengths and the elimination of speed-limiting intra- and inter-chip interconnects. • This approach has been effectively used in designing microprocessors and has resulted in a dramatic reduction of size and an unbelievable increase of speed. • The biggest win for 3-D integration may be as an enabler for new systems architectures.	• It needs a new process technology and heat removal remains to be quite challenging.	A self-synchronized RF-interconnect based on capacitive coupling is implemented in 3-D integration technology. It is fabricated and verified in UMC 0.18-μm MOS with a PRBS (Pseudo Random Binaly Sequence) data rate of 3Gbps, a BER of 1.2×10^{-10} and a rms jitter of 1.28ps. The core circuit burns 4mW from a 1.8V supply and occupies 0.02mm^2 chip area [4].
RF interconnect using capacitive coupling	• It follows the mainstream of the ULSI, is compatible with the CMOS technology trend, and has more possibilities with high-frequency silicon technologies and ever-increasing integrated circuit size [6]. • It overcomes the limits of conventional digital interface systems using the direct-coupled interconnect (DCI) and the capacitive coupled interconnect (CCI). It improves the signal-to-noise ratio and lowers the signal swing and output consumption while increases the transmission data rate. • Modern communication algorithms CDMA and/or FDMA have been	• It uses 'active' capacitive coupling to CPW or MTL making it still a 'wire' interconnect method and its performance is limited by interconnect capacitors. • Problems include the area required by a coupling capacitor, which is about 600 μm^2 and its impacts to interconnect delay time.	An RF/baseband FDMA-interconnect transceiver is implemented in 0.18-μm CMOS. It enables reconfigurability and multiple access for multi-I/Os on a shared bus. It achieves an aggregate data rate of 3 Gbps/pin (3.6 Gbps/pin) for bi-directional (uni-directional) signaling while dissipating 92 mW and occupying 0.65 mm^2 [5]. It is expected that the proposed interconnect schemes based on CDMA and FDMA can achieve aggregate data rate beyond 100 Gbps/pin given the 65 nm technology as presented in [6].

	demonstrated to effectively alleviate the undesired cross-channel interference within the shared medium.		In this thesis, a novel inter-chip RF-interconnect (RFI) system is first proposed and analyzed in terms of BER performance. It uses CPW, capacitive couplers, and ultrawide-band (UWB) radios that operate in 22-29 GHz. It is concluded that a high interconnect data rate of 3.33 Gbps with a low BER < 10^{-5} up to an inter-chip interconnect distance of 3 cm is achievable with the average transmitted power less than −2.85 dBm.
RF wireless interconnect	• The interconnect delay is expected to be much smaller than that of the wire interconnect, because the signal can propagate at the speed of light. • It follows the mainstream of the ULSI, is compatible with the CMOS technology trend, and has more possibilities with high-frequency silicon technologies and ever-increasing integrated circuit size. • It has potentials to provide the concurrent multi I/O services. • It can achieve ultra-high data rate. The material limit does not exist. The only limit is the circuit design and implementation. • Since no physical connection is required for different I/Os, the system reconfiguration can be realized by changing modulation/demodulation	• It faces the same fundamental issues related to component (transmitter, antenna, receiver) size and error correction. • Before becoming a viable candidate to replace global wires and/or package interconnects, it must be cost competitive in size, cost and power dissipation. • Its RF power dissipation cannot add a significant amount of heat to an already heavy thermal load. • It will likely require adaptation of new system architectures to fully exploit the capabilities of RF wireless interconnects.	It has been demonstrated for clock distribution at 15 GHz in 0.18-μm CMOS technologies across a 2.2 cm distance. The transmitter occupies an area of 600×400 μm^2., while the receiver occupies an area of 600×600 μm^2 excluding the bond pads. The areas of antennas are included in the estimation. The transmitter and receiver consume ~ 50 and 40 mW, respectively [7]. In this thesis, a novel intra-chip wireless interconnect system using on-chip meander monopole antennas and UWB radios that operate in 22-29 GHz is studied. It is shown that the system on the 10-Ω.cm substrate can support a data rate of 1.5 Gbps with a BER < 10^{-5} up to an intra-chip wireless channel of length 10 mm

	schemes. • As CMOS technologies improve the cost of on-chip antenna and required circuits should decrease. This makes RF wireless interconnect cost effective in future.		with the average transmitted power of 0 dBm; while the system on the 5-KΩ.cm substrate can support a data rate of 3.5 Gbps with a BER < 10^{-6} up to an intra-chip wireless channel of length 40 mm with the same transmitted power. In this thesis, a novel inter-chip wireless interconnect system using on-package beveled monopole antennas and UWB radios that operate in 3.1-10.6 GHz is also studied. It is concluded that a high data rate of 1 Gbps with a low BER < 10^{-7}over an interchip wireless channel of length 20 cm can be achieved with the radiated power spectral density less than −41.3 dBm/MHz.

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