Design of Chopper-Stabilized Amplifiers With Reduced Offset for Sensor Applications

P. K. Chan and J. Cui

***Abstract*—Offset error mechanisms in a single-ended chopper-stabilized amplifier are investigated. The error models and their prediction equations are given. This work also presents a new analytical approach for estimating the switch error in a four-transistor chopping network. A new resistance balancing circuit technique is also introduced, which permits further reduction of dc offsets in conventional chopping operational amplifier (op-amp) or chopping differential difference amplifier (DDA). The HSPICE simulation results have validated the proposed technique and identified dominant error sources using Level-49 BSIM3 model in a standard 0.6-μm CMOS technology. Applying the technique to the fabricated DDA chips at a noninverting gain of ten and a single 3-V supply, the measured results have shown that 40% of the ten samples display no more than 3- and 5-μV offsets at the chopping frequency of 10 and 64 kHz, respectively. The proposed technique offers a potential advantage for improving the yield of low-offset amplifiers in sensory systems.**

***Index Terms*—Analog integrated circuit, chopper-stabilized amplifier, differential difference amplifier (DDA), MOS analog switch, precision amplifier, sensor amplifier.**

I. Introduction

PRECISION amplifiers towards sensory systems have received much attention in analog signal processing. The primary reasons are improvement of performance, reduction of calibration complexity or procedures in lowering the test cost, the support of small-size realizations in area-concern environment, and improvement of yield. Although CMOS operational amplifiers (op-amps) are often preferred to bipolar counterparts in the emerging highly integrated systems, they are greatly limited by dc offsets and low-frequency $1/f$ noise. These nonideal components can be minimized through the well-known offset-canceling circuit techniques which are generally classified into a correlated double-sampling (CDS) method [1] using switched-capacitor technique, chopper-stabilized (CHS) method [2], and a combination of CHS and switched-capacitor methods [3]. Of the techniques, the CHS approach is popular because of its continuous time in nature, making it suitable for interfacing with various types of sensors.

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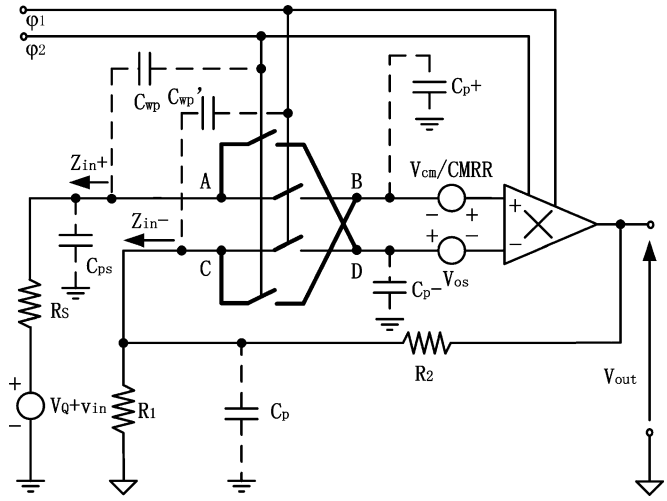

Fig. 1. Error sources and parasitics of a conventional chopping amplifier.

Besides standard single-input precision amplifiers, the differential difference amplifier (DDA) that is widely accepted as improved analog blocks [4]–[7] becomes one of the natural choices in sensor amplifier architecture on the basis of its simplicity for realizing floating input ports. These are successfully demonstrated in sensor circuits like threshold detection-sensing circuits [8], Hall sensor instrumentation amplifiers [9], and control circuits [10] in a gas sensor. Improved performance can be obtained through introduction of a chopper stabilization technique to the design of precision amplifiers. This can be evident from differential chopper-stabilized circuits [11], [12]. Due to symmetry reasons, highly accurate differential circuits are usually guaranteed. For low cost and performance tradeoff solutions, the single-ended chopping amplifier structures are of interest. It is mainly because they are still better than standard sensory amplifiers on performance such as dc offsets, drift, CMRR, and noise simultaneously if properly designed. Typical examples are current sensor [13] in power management IC, signal-conditioning circuits [14] in electrical capacitance tomography, biopotential recording circuits [15]–[17], and so forth.

Despite considerable success in some sensor application-specific cases, the single-ended chopping amplifiers still exhibit limiting issues. To highlight the basic scenario, Fig. 1 shows a conventional noninverting chopping amplifier configuration associated with numerous error sources and parasitics that may cause a potential impact on the circuit accuracy. Using the CHS technique, the circuit CMRR is significantly enhanced because the input-referred common mode error source, like the amplifier dc offset and $1/f$ noise component, is translated to a higher frequency in chopping action. On one hand, this relaxes the critical transistor's matching requirement for achieving high CMRR

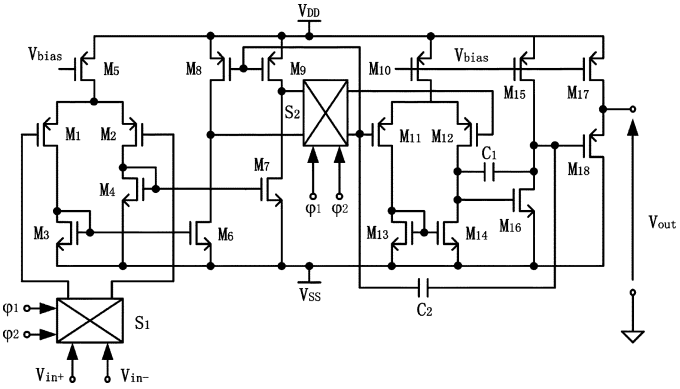

Fig. 2. Simplified schematic of a single-ended chopping op-amp.

in the classical op-amp design. On the other hand, the input chopper contributes to the residual dc and signal-dependent errors (if input signal is large), arising from the combined results of switch charge injection, clock feedthrough, and random mismatch. Besides, the error pertaining to the mismatch of clock wire capacitances $C_{\rm wp}$ and $C'_{\rm wp}$ can be minimized through a careful layout and addressing symmetry. However, a larger dc error will also be encountered because of the unbalance impedances ($\rm Z_{in+}$ and $\rm Z_{in-}$) in the intrinsic physical structure when observed from the viewpoint of effective resistance and effective parasitic capacitance. Such a physical phenomenon causes an uneven split ratio in switch charges. This raises the motivation of this paper on how to strengthen dc offset cancellation to improve precision in the single-ended chopping amplifier. This involves analyzing the second-order effects and devising improved circuit structures.

In Section II, the fundamental error sources in a chopping op-amp are modeled and analyzed. In Section III, the error models are extended to a chopping DDA. In Section IV, we introduce a new resistance balancing technique for compensating the unbalanced resistive gain network in order to achieve better offset reduction. In Section V, the simulation results for compensated chopping op-amp and chopping DDA are compared with their respective analytical results from the dominant error source models. Their implications are discussed in detail. Their reduction of dc offset with respect to the uncompensated chopper stabilized amplifiers is demonstrated with simulation examples. Finally, the experimental results are conducted on a previously published chopping DDA to validate the effectiveness of the proposed resistance balancing methodology. This is then followed by the concluding remarks in Section VI.

II. Error Models and Analysis in Chopping Op-Amp

A. Single-Ended Chopping Op-Amp

A typical single-ended chopping op-amp is shown in Fig. 2. The input chopper $\rm S_1$ transposes the signal to a higher frequency and the internal chopper S_2 demodulates it back to the baseband after amplification by the first gain stage (formed by transistors M_1-M_9). The nonideal effects of the first chopper have been discussed in the prior section. On the other hand, regardless of the gain of second stage (formed by transistors $M_{10}-M_{16}$), the errors of internal chopping switches are reduced by the first stage gain, thus they are negligibly small when compared with

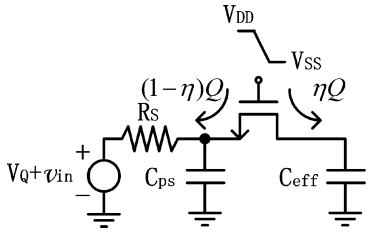

Fig. 3. Switch charge injection analytical model.

that of input counterpart. For driving a lower resistive load, a source–follower buffer $(M_{17}-M_{18})$ can be added as an option but at the expense of reduced output swing. Since a multistage topology is used, the nested-Miller frequency compensation is adopted. Due to very high gain structure, the gain error can be reduced significantly, which improves precision ultimately.

B. Switch Charge Injection in Chopping Network

One of the nonideal effects of the MOS transistor switch is the switch charge injection. Fig. 3 depicts the analytical model for analyzing charge injection error voltage. The source terminal is assumed to have finite source resistance R_S and parasitic capacitance $C_{\rm ps}$, while the other terminal has a load capacitance $C_{\rm eff}$, which is mainly contributed by the input capacitance of the op-amp. When the transistor switch turns from on to off, part of the injected charge is absorbed by the driving source, whereas the other part flows towards the capacitive load. As a result, the charge split ratio is defined as

$$\eta = Q_{\rm ch,eff}/Q_{\rm ch,total} \tag{1}$$

where $Q_{\rm ch,eff}$ is the charge dump at the $C_{\rm eff}$ side, whereas $Q_{\rm ch,total}$ is the total switch charge injection. η is dependent upon terminal impedance. Based on prior work [18], the error charge at the $C_{\rm eff}$ node with finite R_S and $C_{\rm ps}$ is

$$\begin{aligned} Q_{\rm ch,eff} = &-C_{\rm eff}\frac{UC_G}{2C_{\rm eff}}\exp\left(-\frac{V_{HT}}{UC_{\rm eff}R_s}\right) \\ &\times\int_0^{V_{HT}}\left[\mu_n C_{\rm ox}\left(\frac{W}{L}\right)\times R_S(V_{HT}-U\xi)\right. \\ &\left.+1\right]^{\frac{1}{C_{\rm eff}\mu_n C_{\rm ox}\left(\frac{W}{L}\right)R_S^2U}}\times\exp\left(\frac{\xi}{C_{\rm eff}R_S}\right) \\ &\times\left(2-\frac{1}{1+\mu_n C_{\rm ox}\left(\frac{W}{L}\right)R_S(V_{HT}-U\xi)}\right)d\xi \end{aligned} \tag{2}$$

where U denotes the falling rate of the chopping clock, C_G is the total gate capacitance of switch transistor, and ξ is the integral variable. The gate-overdrive voltage of the switch transistor is defined as

$$V_{HT} = V_H - V_S - V_{\rm th} \tag{3}$$

where $V_{\rm H}$ is the ON gate voltage, V_S is the source voltage, and $V_{\rm th}$ is transistor effective threshold voltage including the body effect.

For a normal NMOS switch, the total switch charge injection is

$$Q_{\rm ch,total} = -WLC_{\rm ox}(V_{GS}-V_{\rm th}). \tag{4}$$

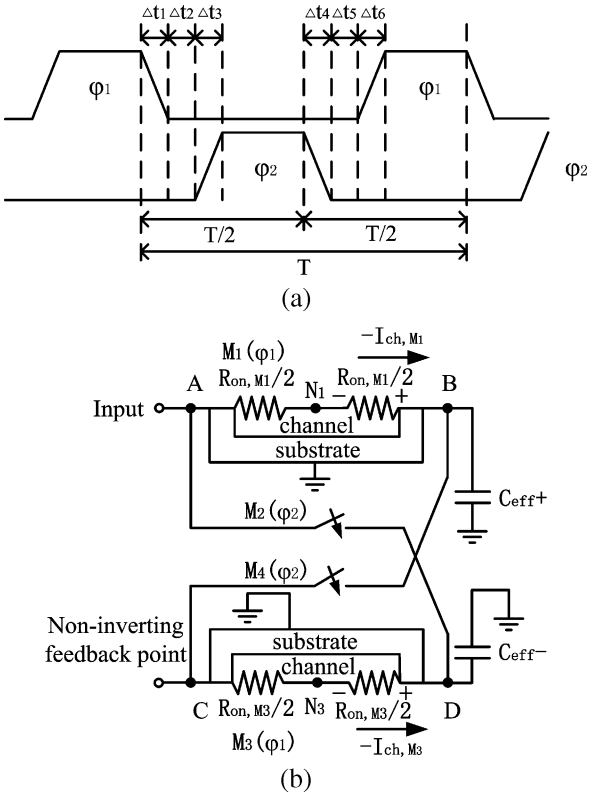

Fig. 4. Switch charge injection voltage errors sampled by capacitive loads. (a) Biphasic nonoverlapping control clock signals φ_1 and φ_2. (b) M_1-M_3 start turning off but M_2-M_4 turn on at $\Delta t_1 + \Delta t_2 + \Delta t_3$ later.

η can be obtained from (1)–(4) for a practically applicable chopping op-amp condition. Fig. 4(a) shows the biphasic clocks with dedicated turn-off times Δt_1 and Δt_4, nonoverlapping times Δt_2 and Δt_5, and turn-on times Δt_3 and Δt_6. In the first half cycle, the clock φ_1 goes from high to low and the complementary clock φ_2 goes from low to high, and vice versa for these biphasic clock signals in the second case. Fig. 4(b) shows the first circuit case that two switch transistors M_1 and M_3 start to turn off, whereas the other two transistor switches turn on at an elapse of time.

For lumped resistance modeling, the switch admittance is $2G_{\rm on}$ (equivalent to $2/R_{\rm on}$) for a half switch. The $G_{\rm on}$ is the on-conductance of a triode switch which is defined as

$$G_{\rm on} \approx \mu C_{\rm ox}(W/L)(V_{GS} - V_{\rm th}). \tag{5}$$

Refer to the middle points $\rm N_1$ and N_3 nodes of lumped resistor model for on switches, they exhibit high impedance with respect to the substrate. When the switches turn from ON to OFF, the channels disappear and N_1 and N_3 become ground since the switch channels merge with the substrate at the instant. This process emulates a sample-and-hold action, with the channel on–off phenomenon being treated as a sampling switch behavior and lumped parasitic capacitors $C_{\rm eff+}$ and $C_{\rm eff-}$ being treated as the sampling capacitors with reference to ground. Note that $C_{\rm eff+} \approx C_{\rm p+}$, $C_{\rm eff-} \approx C_{\rm p-}$, assuming that the effective parasitics are dominated by the input capacitances of amplifier and the routing parasitics are negligible. Finally, potentials induced in each half switch channel of M_1 and M_3 will be sampled by the two lumped parasitic capacitors. Since the channel admittance changes from the on state to the off state of the switch, the average change of half switch admittance in transition time Δt_1 is estimated to be $G_{\rm on(average)} = 1/R_{\rm on}$. This leads to the sampled charge injection error voltage $V_{\rm ch,M_1} = (\Delta Q_{\rm ch,M_1}/\Delta t_1)R_{\rm on,M_1}$ in M_1 and $V_{\rm ch,M_3} = (\Delta Q_{\rm ch,M_3}/\Delta t_1)R_{\rm on,M_3}$ in M_3, respectively. However, they are further averaged by a factor $\Delta t_1/(T/2 - \Delta t_2 - \Delta t_3)$ due to the channel voltage induced in finite turning-off time Δt_1 for given half clock cycle. These charge injection error voltages appear in a form of common-mode dc signals superimposed on either an input signal potential (using noninverting amplifier configuration like the case in Fig. 1) or a virtual analog ground potential (using inverting amplifier configuration) in $C_{\rm eff+}$ and $C_{\rm eff-}$. Based on the relationship that $I = Q/t = V/R$, the mean channel dc charge injection error voltages are written as

$$V_{\rm ch,M_1} = \frac{\Delta Q_{\rm ch,M_1}}{\Delta t_1} R_{\rm on,M_1} \frac{\Delta t_1}{T/2 - \Delta t_2 - \Delta t_3} \tag{6}$$

$$V_{\rm ch,M_3} = \frac{\Delta Q_{\rm ch,M_3}}{\Delta t_1} R_{\rm on,M_3} \frac{\Delta t_1}{T/2 - \Delta t_2 - \Delta t_3}. \tag{7}$$

Since $(T/2) \gg \Delta t_2$ and Δt_3, we have

$$V_{\rm ch,M_1} \approx \Delta Q_{\rm ch,M_1} \frac{R_{\rm on,M_1}}{T/2} \tag{8}$$

$$V_{\rm ch,M_3} \approx \Delta Q_{\rm ch,M_3} \frac{R_{\rm on,M_3}}{T/2}. \tag{9}$$

Using (1)–(5) and (8) and (9), the charge injection error voltage source, arising from M_1 and M_3 in the amplifier differential input, is derived as follows:

$$\begin{aligned} \Delta V_{\rm ch,M_1\&M_3} &= V_{\rm ch,M_1} - V_{\rm ch,M_3} \\ &\approx \eta_1 Q_{\rm ch,M_1} R_{\rm on,M_1}/(T/2) \\ &\quad - \eta_3 Q_{\rm ch,M_3} R_{\rm on,M_3}/(T/2) \\ &\approx -\eta_1 (WL)_1 C_{\rm ox}(V_{GS1} - V_{\rm th1}) R_{\rm on,M_1}/(T/2) \\ &\quad + \eta_3 (WL)_3 C_{\rm ox}(V_{GS3} - V_{\rm th3}) R_{\rm on,M_3}/(T/2). \end{aligned} \tag{10}$$

Note that the differential operation in Fig. 4(b) also subtracts the almost identical analog signals at B and D due to feedback in noninverting configuration or the almost identical analog ground potentials at B and D due to feedback in inverting configuration. This leads to the residual charge injection dc defined in (10).

At the instant that the transistors, M_1 and M_3, switch from on to off, the respective gate-to-source voltage is signal-dependent and given by

$$V_{GS,i} = V_G - V_{S,i} = V_{DD} - V_{S,i} = V_{DD} - (V_Q + v_{\rm in}) \tag{11}$$

with $i = 1, 3$ and V_Q is the quiescent voltage at node A, B, C, and D in Fig. 4(b). Due to the body effect, each threshold voltage of the MOS transistor switch will be modulated by the input signal. Further mismatch in threshold voltages also contributes additional error. For simplicity, the short channel length

and narrow width effects are ignored. The threshold voltage pertaining to the above two effects can be modeled as

$$V_{\mathrm{th},i} \approx V_{\mathrm{th0}} + K1(\sqrt{2\Phi_f + V_{SB,i}} - \sqrt{2\Phi_f}) + K2V_{SB,i} + \Delta V_{\mathrm{th},i} \quad (12)$$

whereas the source-to-bulk voltages in the bulk-modulated transistors are

$$V_{SB,i} = V_{S,i} - V_B = V_{S,i} - 0 = V_Q + v_{\mathrm{in}} \quad (13)$$

with $i = 1, 3$. It is assumed that $\mathrm{V_{th0}}$ is the nominal reference threshold voltage at zero source-bulk voltage. $\Delta \mathrm{V_{th},}_i$ is the lumped deviation of threshold voltage in a single MOS switch transistor with respect to the nominal $\mathrm{V_{th}}$, ranging from -5 to $+5$ mV in a typical process. $K1$ and $K2$ denote the first-order and second-order body effect coefficients, respectively, in the BSIM3 model.

Furthermore, a mismatch in switch area contributes another error. If the ideal dimension is treated as WL, α can be introduced to a MOS switch transistor as the relative mismatch coefficient with respect to the ideal case. They represent the percentage of mismatch from the nominal value of the gate area of the four switch transistors respectively. In practical processes, α ranges from -2% to 2%. Assuming α_1, α_2, α_3, and α_4 represent the percentage of mismatch from the nominal value of the gate area of M_1, M_2, M_3, and M_4, substituting (11)–(13) into (10), we obtain (14). For the clock transition case in second half cycle, there is also a similar result (15) for the signal-dependent charge injection error voltage source $\Delta V_{\mathrm{ch,M_2\&M_4}}$ caused by a $M_2 - M_4$ switch pair in the complementary operation

$$\begin{aligned}
\Delta V_{\mathrm{ch,M_1\&M_3}} &= V_{\mathrm{ch,M_1}} - V_{\mathrm{ch,M_3}} \\
&= \eta_3 (WL)(1+\alpha_3) C_{\mathrm{ox}} \\
&\quad \times [V_{DD} - V_Q - v_{\mathrm{in}} - V_{\mathrm{th0}} \\
&\qquad - K1(\sqrt{2\Phi_f + V_Q + v_{\mathrm{in}}} - \sqrt{2\Phi_f}) \\
&\qquad - K2(V_Q + v_{\mathrm{in}}) - \Delta V_{\mathrm{th},3}] \\
&\quad \times R_{\mathrm{on,M_3}}/(T/2) - \eta_1 (WL)(1+\alpha_1) C_{\mathrm{ox}} \\
&\quad \times [V_{DD} - V_Q - v_{\mathrm{in}} - V_{\mathrm{th0}} \\
&\qquad - K1(\sqrt{2\Phi_f + V_Q + v_{\mathrm{in}}} - \sqrt{2\Phi_f}) \\
&\qquad - K2(V_Q + v_{\mathrm{in}}) - \Delta V_{\mathrm{th},1}] \\
&\quad \times R_{\mathrm{on,M_1}}/(T/2) \qquad (14) \\
\Delta V_{\mathrm{ch,M_2\&M_4}} &= V_{\mathrm{ch,M_2}} - V_{\mathrm{ch,M_4}} \\
&= \eta_4 (WL)(1+\alpha_4) C_{\mathrm{ox}} \\
&\quad \times [V_{DD} - V_Q - v_{\mathrm{in}} - V_{\mathrm{th0}} \\
&\qquad - K1(\sqrt{2\Phi_f + V_Q + v_{\mathrm{in}}} - \sqrt{2\Phi_f}) \\
&\qquad - K2(V_Q + v_{\mathrm{in}}) - \Delta V_{\mathrm{th},4}] \\
&\quad \times R_{\mathrm{on,M_4}}/(T/2) - \eta_2 (WL)(1+\alpha_2) C_{\mathrm{ox}} \\
&\quad \times [V_{DD} - V_Q - v_{\mathrm{in}} - V_{\mathrm{th0}} \\
&\qquad - K1(\sqrt{2\Phi_f + V_Q + v_{\mathrm{in}}} - \sqrt{2\Phi_f}) \\
&\qquad - K2(V_Q + v_{\mathrm{in}}) - \Delta V_{\mathrm{th},2}] \\
&\quad \times R_{\mathrm{on,M_2}}/(T/2). \qquad (15)
\end{aligned}$$

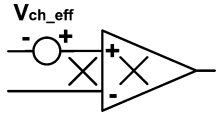

Fig. 5. Input-referred switch charge injection error voltage source.

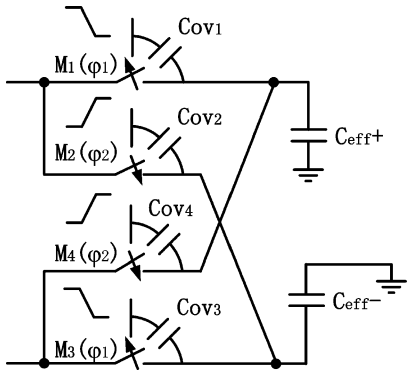

Fig. 6. Clock feedthrough errors induced by chopping switches at first half cycle.

Since the input signal and feedback signal swap with each other at the input terminals of op-amp in every half cycle, the average effective charge injection error voltage in one clock cycle is thus obtained as

$$V_{\mathrm{ch\_eff}} = \frac{\Delta V_{\mathrm{ch,M_1\&M_3}} + \Delta V_{\mathrm{ch,M_2\&M_4}}}{2}. \quad (16)$$

As a result, the charge injection effect in the nonideal chopper model can be separated into an ideal chopper plus an input-referred error voltage source which represents effective switch charge injection as shown in Fig. 5.

C. Clock Feedthrough in Chopping Network

A MOSFET switch in the chopper couples the clock transitions through its gate-source and gate-drain overlap capacitances and introduces the clock feedthrough error to the capacitance associated with the node. Although the ideal differential operation can cancel the clock feedthrough effect, the practical mismatch of switch transistors will lead to a residual dc error.

Assuming the overlap capacitance is constant, for an n-channel transistor switch, the induced error voltage in the effective parasitic capacitor C_{eff} is given by

$$V_{\mathrm{cf}} = -\Delta V_{\mathrm{ck}} \frac{(WL)(1+\alpha_i) C_{\mathrm{ov}}}{(WL)(1+\alpha_i) C_{\mathrm{ov}} + C_{\mathrm{eff}}} \quad (17)$$

where $i = 1, 2, 3, 4$, $\Delta \mathrm{V_{ck}}$ is the change of clock voltage that is positive from V_{DD} to V_{SS} and negative from V_{SS} to V_{DD}, C_{ov} is the overlap capacitance per unit area of gate-drain or gate-source. Refer to Fig. 6, in the first half cycle, the clock feedthrough errors including mismatch with respect to ideal switch area *WL* are

$$V_{\mathrm{cf},M_1} = -(V_{DD} - V_{SS}) \frac{(WL)(1+\alpha_1) C_{\mathrm{ov}}}{(WL)(1+\alpha_1) C_{\mathrm{ov}} + C_{\mathrm{eff}}} \quad (18)$$

$$V_{\mathrm{cf},M_2} = -(V_{SS} - V_{DD}) \frac{(WL)(1+\alpha_2) C_{\mathrm{ov}}}{(WL)(1+\alpha_2) C_{\mathrm{ov}} + C_{\mathrm{eff}}} \quad (19)$$

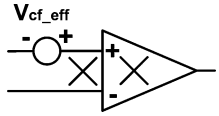

Fig. 7. Input-referred clock feedthrough error voltage source.

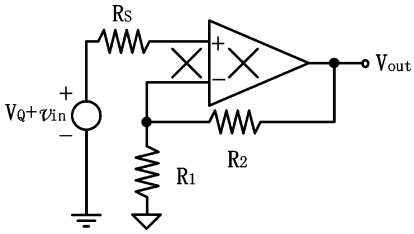

Fig. 8. Noninverting gain circuit with finite open-loop gain chopping op-amp.

$$V_{\mathrm{cf}F,M_3} = -(V_{DD} - V_{SS})\frac{(WL)(1+\alpha_3)C_{\mathrm{ov}}}{(WL)(1+\alpha_3)C_{\mathrm{ov}} + C_{\mathrm{eff}}} \quad (20)$$

$$V_{\mathrm{cf},M_4} = -(V_{SS} - V_{DD})\frac{(WL)(1+\alpha_4)C_{\mathrm{ov}}}{(WL)(1+\alpha_4)C_{\mathrm{ov}} + C_{\mathrm{eff}}}. \quad (21)$$

Hence, the input-referred clock feedthrough error voltage source for the first half cycle becomes

$$\begin{aligned}\Delta V_{\mathrm{cf},1} &= V_{\mathrm{cf},M_1} - V_{\mathrm{cf},M_3} + V_{\mathrm{cf},M_4} - V_{\mathrm{cf},M_2} \\ &= -(V_{DD}-V_{SS})\frac{1}{1+C_{\mathrm{eff}}/[(WL)(1+\alpha_1)C_{\mathrm{ov}}]} \\ &\quad + (V_{DD}-V_{SS})\frac{1}{1+C_{\mathrm{eff}}/[(WL)(1+\alpha_3)C_{\mathrm{ov}}]} \\ &\quad - (V_{SS}-V_{DD})\frac{1}{1+C_{\mathrm{eff}}/[(WL)(1+\alpha_4)C_{\mathrm{ov}}]} \\ &\quad + (V_{SS}-V_{DD})\frac{1}{1+C_{\mathrm{eff}}/[(WL)(1+\alpha_2)C_{\mathrm{ov}}]}. \quad (22)\end{aligned}$$

Since there is a reversal of input terminals and the opposite clock transitions occur in the chopping network during the second half cycle, the induced clock feedthrough error $\Delta V_{\mathrm{cf},2}$ is identical to that of the first half cycle. Consequently, the effective clock feedthrough error in one clock cycle is obtained as

$$V_{\mathrm{cf\_eff}} = (\Delta V_{\mathrm{cf},1} + \Delta V_{\mathrm{cf},2})/2. \quad (23)$$

The input-referred error source model for standalone clock feedthrough effect is illustrated in Fig. 7.

D. Nonideal Effects in Op-Amp

The finite open-loop gain of op-amp affects the precision of the feedback system. Therefore, the finite gain error in Fig. 8 can be derived as

$$\Delta V_{\varepsilon} = v_{\mathrm{in}}\left(-\frac{R_1+R_2}{R_2} \times \frac{1}{A}\right). \quad (24)$$

In addition, other contributions come from dc offset and common-mode error. These models are illustrated in Fig. 9. The common-mode error voltage source equals to the division of the input common mode voltage $\mathrm{V_{CM}}$ over the common-mode rejection ratio (CMRR). Like the dc offset, the common-mode error will be reduced by the CHS technique.

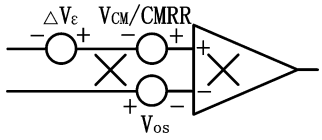

Fig. 9. Finite gain error, dc offset error, and common mode error in a chopping op-amp.

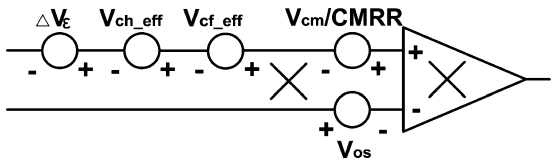

Fig. 10. Input-referred error voltage sources in a chopping op-amp.

This explains why the chopping amplifier has an improved common mode rejection ratio when compared to the conventional counterpart without using the CHS technique.

E. Complete Error Source Models

Taking into account the error source models including switch charge injection, clock feedthrough, finite gain error, common-mode error, and dc offset, these lead to the input-referred voltage sources in Fig. 10. Since the common-mode error as well as the dc offset will be substantially reduced by the chopping op-amp, the effective offset error source can be further simplified as follows:

$$v_{\mathrm{error,OpAmp}} \approx V_{\mathrm{cf\_eff}} + V_{\mathrm{ch\_eff}} + \Delta V_{\varepsilon}. \quad (25)$$

III. Error Models in Chopping DDA

The concept of chopper stabilization can be incorporated into DDA for obtaining further low-noise low-offset characteristics. Like conventional operation, the DDA forces the voltage difference between two floating input ports to the same value in a closed-loop environment such that the chopping DDA becomes a useful instrumentation amplifier for handling floating input signal whilst preserving good accuracy.

Fig. 11 shows the circuit schematic of a single-ended chopping DDA [15]. It is somewhat similar to that of Fig. 2 except with the addition of second input port. Each input port of DDA is identically designed (M_1, M_2, M_5 and input chopping switch network S_1, or M_1', M_2', M_5' and S_1'). The floating input signals are transposed to the chopping frequency through the two input chopping switch networks, S_1 and S_1' whereas the differential pairs $M1' - M2'$ and M1–M2 perform the *V–I* conversion at high frequency simultaneously. First stage gain is achieved by *I–V* conversion in the active load formed by transistors M3–M4 and M6–M9. Through the use of chopper S2, the signal is demodulated back to the baseband frequency but the $1/f$ noise, input common error and dc offset of the first stage are shifted to high frequency simultaneously. The recovered signal is further amplified by the next two-stage amplifier (M10–M16) with source–follower (M17–M18).

Fig. 12 shows the input-referred error voltage source models in a chopping DDA. Since the respective dc offsets and common-mode errors will be suppressed by the CHS action,

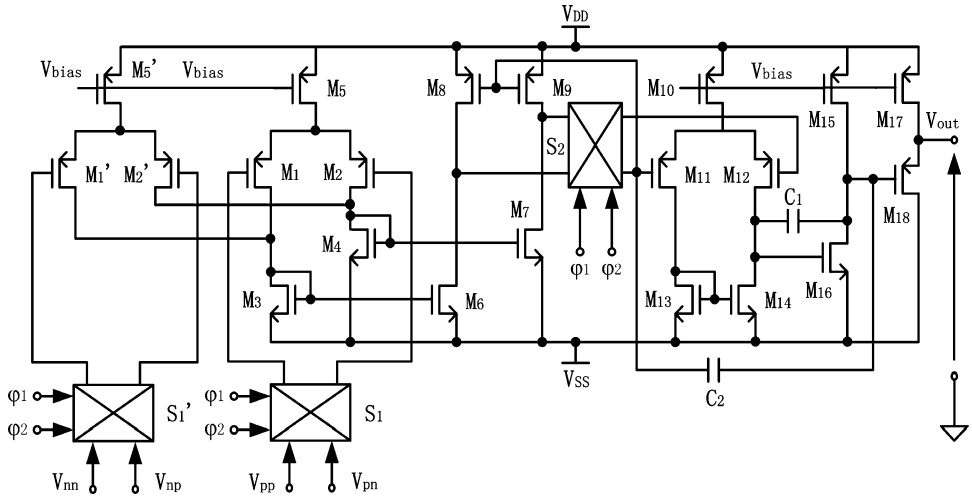

Fig. 11. Simplified schematic of a single-ended chopping DDA.

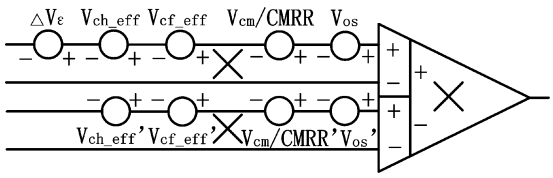

Fig. 12. Input-referred voltage sources in a chopping DDA.

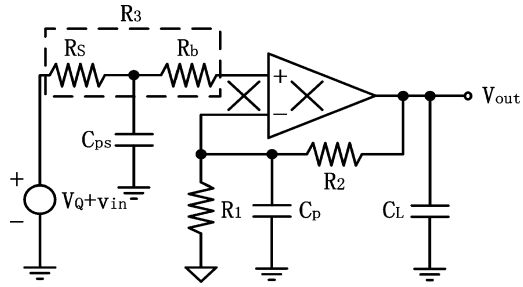

Fig. 13. Adding a resistor for resistance balancing an intrinsic asymmetrical structure in a noninverting amplifier using chopping op-amp.

the effective offset error in a chopping DDA can be further simplified as follows:

$$v_{\text{error,DDA}} \approx V_{\text{cf\_eff}} + V_{\text{ch\_eff}} + \Delta V_{\varepsilon} - V'_{\text{cf\_eff}} - V'_{\text{ch\_eff}}. \quad (26)$$

Based on identically designed input chopping ports, similar error sources and voltage error equations can be established with respect to that of a chopping op-amp as discussed before. Arising from different circuit configurations, the analysis method on switch charge injection is slightly revised. If the chopping switches were connected to either the input source or noninverting feedback point, the signal-dependent charge injection error equations are similar to that of (14) and (15), else dropping the "v_{in}" terms in the relevant equations if the switches are connected to the analog ground in the DDA closed-loop topology for the case without bulk modulation. Except the gain error, it is interesting to observe in (26) that the combined effects of charge injection and clock feedthrough errors in one input port tend to counteract the corresponding errors in the other input port, provided that the random mismatch factors are similar in both ports.

IV. Resistance Balancing Technique for DC Offset Reduction

From the preceding analysis, the first offset contribution comes from the dc input-referred error voltage sources arising from various mismatching effects in MOS device parameters. The second offset contribution, which is one of the key suggestions in this paper, comes from the uneven split ratio of channel charge caused by mismatch of impedance associated with the driving source terminal and effective impedance of the feedback network as illustrated in Fig. 1. However, for a low-frequency sensor signal-processing condition, the impedances contributed by parasitic capacitors are usually high and can be ignored for simplicity in analysis. In addition, due to the nonlinear charge dump in (2), the charge split ratio is nonlinear in nature. Even in $C_{\text{ps}} \neq C_{\text{p}}$, the output error is increased slightly. As a result, the resistive level balancing for impedance matching becomes of prime importance. Hence, it is adequate to compensate an unbalancing DDA structure by adding a simple balancing resistor R_b to fulfill the approximated condition that $(\text{Z}_{\text{in}+} \approx R_{\text{in}+}) \approx (\text{Z}_{\text{in}-} \approx R_{\text{in}-})$. This phenomenon will be validated in Section V-B.

Fig. 13 illustrates the application of the resistance balancing method in an asymmetrical structure of a noninverting amplifier using a chopping op-amp. For an example of $C_{\text{L}} = 25$ pF, $C_{\text{ps}} = 5$ pF, $C_{\text{p}} = 3$ pF, and a typical frequency range from dc to kilohertz in sensor applications, one can exclude the effect of parasitic capacitances because their values are much larger than resistive values at the frequencies of interest. Therefore, we have

$$R_3 = R_S + R_b = \frac{R_1(R_2 + R_{\text{out}})}{R_1 + R_2 + R_{\text{out}}} \approx R_1 \quad (27)$$

with $R_1 < R_2 + R_{\text{out}}$. Note that R_{out} is the effective output resistance of op-amp. From (27), we have

$$R_b = R_1 - R_S \approx R_1 \quad (28)$$

where it is assumed that $R_s \ll R_1$.

TABLE I
SIMULATION PARAMETERS FOR EXAMPLARY MISMATCHED CASES

Parameter Variation	Chopping Op-amp Case 1	Chopping Op-amp Case 2	Chopping DDA Case 1	Chopping DDA Case 2
Vth,S1-M1 Vth,S1-M2 Vth,S1-M3 Vth,S1-M4	-5 mV +5 mV -5 mV +5 mV	+5 mV -5 mV +5 mV -5 mV	-5 mV +5 mV -5 mV +5 mV	+5 mV -5 mV +5 mV -5 mV
Vth,S1'-M1 Vth,S1'-M2 Vth,S1'-M3 Vth,S1'-M4	- - - -	- - - -	+5 mV -5 mV -5 mV +5 mV	-5 mV +5 mV +5 mV -5 mV
(W/L)M1	-2%	+2%	-2%	+2%
(W/L)M2	+2%	-2%	+2%	-2%
(W/L)M1'	-	-	+2%	-2%
(W/L)M2'	-	-	-2%	+2%
(W/L)S1-M1	-2%	+2%	-2%	+2%
(W/L)S1-M2	+2%	-2%	+2%	-2%
(W/L)S1-M3	+2%	-2%	+2%	-2%
(W/L)S1-M4	-2%	+2%	-2%	+2%
(W/L)S1'-M1	-	-	+2%	-2%
(W/L)S1'-M2	-	-	-2%	+2%
(W/L)S1'-M3	-	-	-2%	+2%
(W/L)S1'-M4	-	-	+2%	-2%

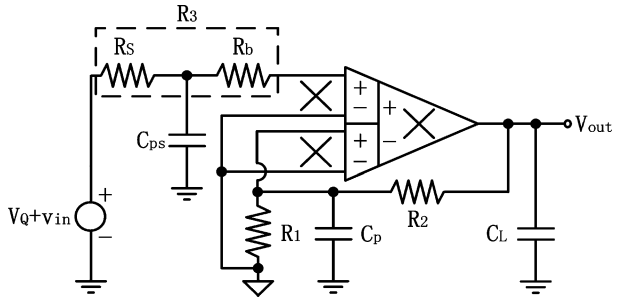

Fig. 14. Resistance balancing in a noninverting amplifier using chopping DDA.

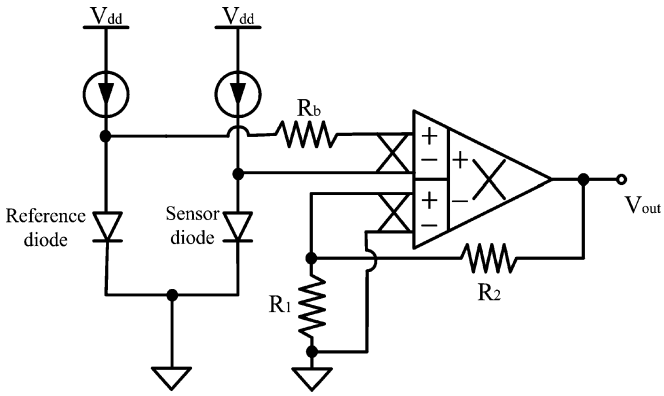

Fig. 15. Micromachined soil moisture sensor application.

Following similar methodology, it can be applied for chopping DDA in Fig. 14 as well. Through adding R_b, the two input chopping networks S_1 and S_1' for floating inputs are now balanced with each other, the result of which shares similar advantages in the chopping op-amp.

Fig. 15 illustrates another example of the proposed precision amplifier for use in sensing a full scale signal of about 1 mV from a micromachined soil moisture sensor [19]. The reference diode sensor is heated up with a resistive heater to produce a reference output voltage. The sensor diode probe is located a distance from the reference diode. Since the volumetric heat capacity is linked to the soil water content, the differential voltage between the reference diode output and sensor diode output indicates the temperature rise with respect to the reference temperature. The range of water content is typically from 0% to 40%. A 1% change of water content, based on a p–n junction sensor of -2.2 mV/°C is 22 μV. Therefore, the application demands a sensing amplifier with good sensitivity. To improve the chopping amplifier sensing performance, a resistance balancing technique is applied. The positive input terminal in upper input port is balanced by the intentional added resistance $R_{\rm b}$, with calculated value according to (28) in a high gain design defined by R_1 and R_2.

V. RESULTS AND DISCUSSION

A. Calculation and Simulation Results of Input-Referred Errors in Chopping Amplifiers

The simulation topologies are based on Figs. 13 and 14, with the assumption that R_S is much smaller than $R_{\rm b}$, whereas the analog ground output resistance is negligibly small in comparison to R_1 and R_2, $C_{\rm ps} = 5$ pF and $C_{\rm p} = 3$ pF. Table I illustrates two exemplary cases of the devices random mismatch in each type of amplifier, with $+/-5$ mV for the threshold voltages in the input choppers S_1, S_1', differential pairs $M_1 - M_2$, $M_1' - M_2'$, and active load transistor pairs $M_3 - M_6$, based on

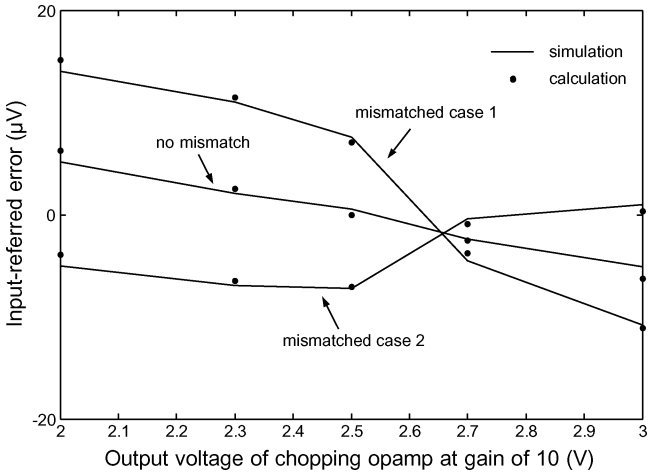

Fig. 16. Simulation and prediction of input-referred error of the chopping op-amp.

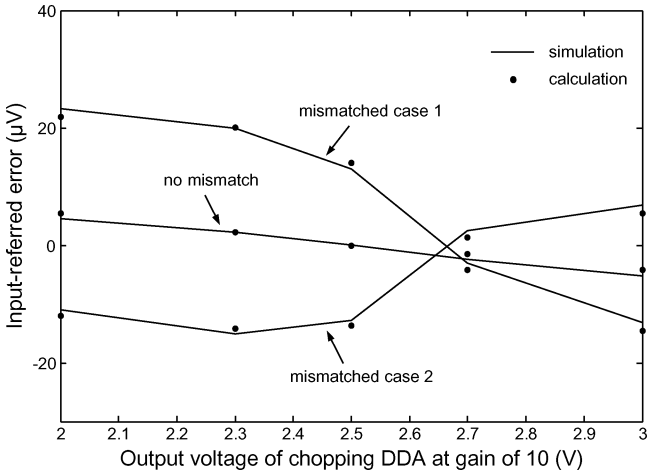

Fig. 17. Simulation and prediction of input-referred error of the chopping DDA.

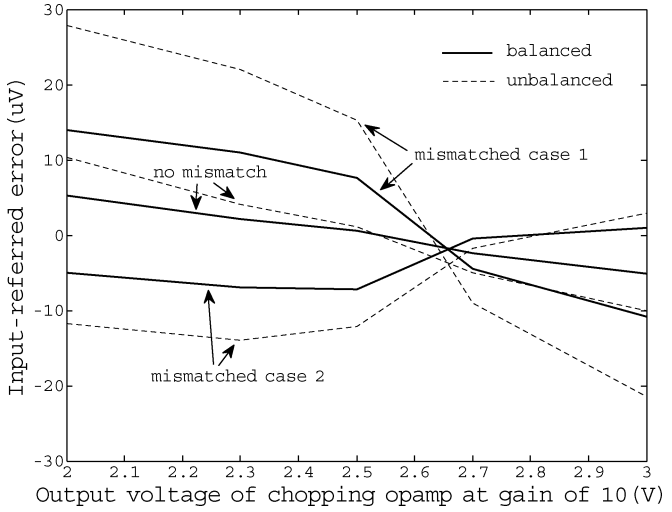

Fig. 18. Simulated input-referred errors of the balanced and unbalanced chopping op-amp.

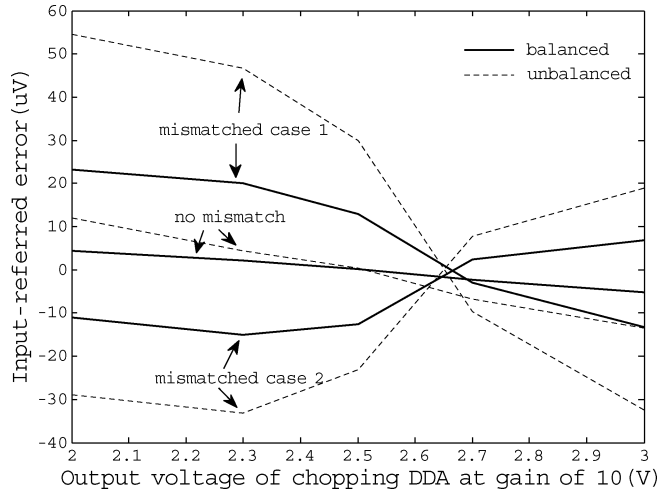

Fig. 19. Simulated input-referred errors of the balanced and unbalanced chopping DDA.

2.5-V V_Q and small input signal. All the mismatches of aspect ratios in the critical matching pairs are assumed with $+/-2\%$ except that of $+/-5\%$ for the input choppers that deal with small transistor size. For a closed-loop gain factor of 10, with a choice of $R_1 = 1\,\mathrm{k}\Omega$, $R_2 = 9\,\mathrm{k}\Omega$, $C_\mathrm{L} = 25\,\mathrm{pF}$, and the assumption of $R_\mathrm{b} \gg R_S$, we can find that $R_3 \approx R_\mathrm{b} \approx 1\,\mathrm{k}\Omega$ from (27) and (28). Therefore, using (1)–(5) and typical values of process and design parameters for computation in MATLAB, the charge split ratio for 1 kΩ is 60.4% in the chopping op-amp, whereas in the chopping DDA, the charge split ratio is 60.4% for 1 kΩ and 35.7% for negligible source resistance value of analog ground reference. Starting from −50 mV with respect to an analog ground reference 2.5 V, an incremental input step of 10 mV dc was applied to each circuit until +50 mV. The dc output of each amplifier was extracted using a 150-Hz RC low-pass filter under a chopping clock frequency of 64 kHz. This ensures harmonics as well as high-frequency noise are rejected substantially. Using realistic Level 49 BSIM3 model from AMS 0.6 μm CMOS process and a single supply of 5 V, the simulated equivalent input-referred errors of each amplifier were obtained against different output voltages in Figs. 16 and 17, respectively. As can be observed, the predicted results are close to the simulation results. Mismatch effect in chopping amplifiers deteriorate the dc precision. Improving matching of critical transistor matching pair will reduce the dc offset. The DDA suffers from relatively higher dc offset than the op-amp counterpart because of the increase in complexity. Referring to the calculated results in Tables II and III, the contributions arising from the charge injection $(V_{\mathrm{ch\_eff}})$, clock feedthrough $(V_{\mathrm{cf\_eff}})$, and finite gain error (ΔV_ε) are summed to obtain the equivalent input-referred error, which gives the insight on how an individual error source makes an impact to the final error. Since the estimated equivalent input-referred error is close to the simulation result, it has confirmed that other error sources such as dc offset and dc common-mode error are suppressed effectively. This also validates the dominant error source models as discussed above. In order to predict the effectiveness of the proposed technique, the same simulations without R_b are done for both chopping op-amp and DDA. Figs. 18 and 19 show the respective comparative simulation result. It can be seen that there are about two to three times improvement on the input-referred dc offsets.

TABLE II
CALCULATION OF INDIVIDUAL INPUT-REFERRED ERROR IN CHOPPING OP-AMP AND COMPARISON OF THE SUMMED ERRORS WITH SIMULATED RESULTS

Input voltage (V)	Ideal Output Voltage (V)	Mismatch Case 2		No mismatch		Mismatch Case 1	
		Calculation of Errors (μV)	Simulation (μV)	Calculation of Errors (μV)	Simulation (μV)	Calculation of Errors (μV)	Simulation (μV)
2.55	3.0	V_{ch_eff} : 29.6 V_{cf_eff} : -23 $\triangle V_{\varepsilon}$: -6.3 **total : 0.3**	**1**	V_{ch_eff} : 0 V_{cf_eff} : 0 $\triangle V_{\varepsilon}$: -6.3 **total : -6.3**	**-5.1**	V_{ch_eff} : -27.8 V_{cf_eff} : 23 $\triangle V_{\varepsilon}$: -6.3 **total : -11.1**	**-10.8**
2.52	2.7	V_{ch_eff} : 24.6 V_{cf_eff} : -23 $\triangle V_{\varepsilon}$: -2.5 **total : -0.9**	**-0.4**	V_{ch_eff} : 0 V_{cf_eff} : 0 $\triangle V_{\varepsilon}$: -2.5 **total : -2.5**	**-2.4**	V_{ch_eff} : -24.3 V_{cf_eff} : 23 $\triangle V_{\varepsilon}$: -2.5 **total : -3.8**	**-4.5**
2.5	2.5	V_{ch_eff} : 15.9 V_{cf_eff} : -23 $\triangle V_{\varepsilon}$: 0 **total : -7.1**	**-7.2**	V_{ch_eff} : 0 V_{cf_eff} : 0 $\triangle V_{\varepsilon}$: 0 **total : 0**	**0.55**	V_{ch_eff} : -15.9 V_{cf_eff} : 23 $\triangle V_{\varepsilon}$: 0 **total : 7.1**	**7.6**
2.48	2.3	V_{ch_eff} : 13.8 V_{cf_eff} : -23 $\triangle V_{\varepsilon}$: 2.5 **total : -6.5**	**-6.9**	V_{ch_eff} : 0 V_{cf_eff} : 0 $\triangle V_{\varepsilon}$: 2.5 **total : 2.5**	**2.1**	V_{ch_eff} : -14 V_{cf_eff} : 23 $\triangle V_{\varepsilon}$: 2.5 **total : 11.5**	**11**
2.45	2.0	V_{ch_eff} : 12.8 V_{cf_eff} : -23 $\triangle V_{\varepsilon}$: 6.3 **total : -3.9**	**-5**	V_{ch_eff} : 0 V_{cf_eff} : 0 $\triangle V_{\varepsilon}$: 6.3 **total : 6.3**	**5.2**	V_{ch_eff} : -14.2 V_{cf_eff} : 23 $\triangle V_{\varepsilon}$: 6.3 **total :15.1**	**14**

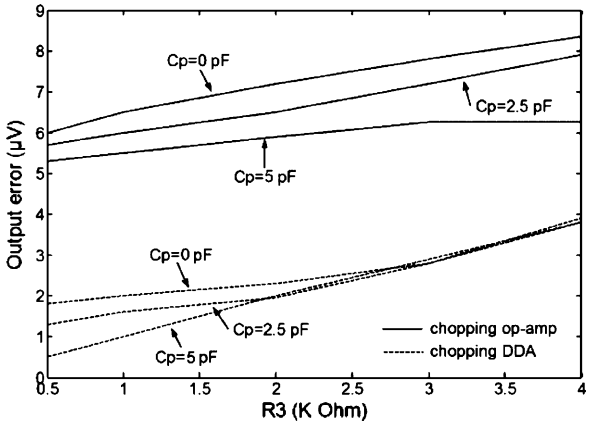

Fig. 20. Output errors of chopping amplifiers with variation of parasitic capacitance and compensation resistance values at no mismatch condition.

B. Effect of Variation of Parasitic Capacitance and Compensation Resistance

It is interesting to examine the effect of unbalanced parasitic capacitance on the output error voltage. Assume all source resistances are negligibly small using buffered output, $C_{\rm ps}$ is 5 pF, $C_{\rm L} = 25$ pF, and $C_{\rm p}$ steps from 0 to 2.5 and to 5 pF. For $V_{\rm Q} = 2.5$ V and $V_{\rm in} = 0$ V, the output error voltage for each type of amplifier is shown in Fig. 20. Even for variation of ± 0.5 kΩ in the nominal compensation resistor R_3 of 1 kΩ, the change of output error voltage gives no more than ± 1 μV, which indicates the insensitivity of both amplifier structures. In overall observation, for higher R_3 values due to overcompensation, the sensitivity of error output voltage with respect to the change of unbalanced parasitic capacitance in dual input ports chopping DDA offers relatively less change when compared to that of the single input port chopping op-amp.

C. Micromachined Soil Moisture Sensor Example

The soil moisture sensor in Fig. 15 is used to compare the chopping amplifier with and without resistance balancing technique. The differential input voltage, caused by the water content change from 1% to 35%, ranges from 22 to 770 μV. The simulation is based on the assumption that an increase of 1% water content corresponds to a decrease of 0.01 °C in temperature [20]. With $R_1 = 1$ kΩ and $R_2 = 99$ kΩ, the closed-loop gain is set to 100 to realize a high gain amplifier for detection of minute sensor signal. Table IV summarizes the respective output voltage for ideal amplifier, unbalanced chopping DDA, balanced chopping DDA together with the respective error at different input signals. The corresponding data are then plotted in Fig. 21 for a view of fluctuation on the output errors across the sensor signal range. It has shown that the balanced DDA can offer 2.3 to 3 times reduction of output errors in water content detection in soil for environmental application, suggesting the improvement on precision sensing function in a sensory system.

D. Measured Results

The core chopping DDA [15] had been fabricated by AMS 0.6 μm CMOS technology, with an active area of 0.24 mm^2

TABLE III
CALCULATION OF INDIVIDUAL INPUT-REFERRED ERROR IN CHOPPING DDA AND COMPARISON OF THE SUMMED ERRORS WITH SIMULATED RESULTS

Input Voltage (V)	Ideal Output voltage (V)	Mismatch Case 2		No mismatch		Mismatch Case 1	
		Calculation of Errors (μV)	Simulation (μV)	Calculation of Errors (μV)	Simulation (μV)	Calculation of Errors (μV)	Simulation (μV)
2.55	3.0	V_{ch_eff} : 56.5 V_{cf_eff} : -46 $\triangle V_{\varepsilon}$: -5 **total : 5.5**	**6.9**	V_{ch_eff} : 0.8 V_{cf_eff} : 0 $\triangle V_{\varepsilon}$: -5 **total : -4.2**	**-5.2**	V_{ch_eff} : -55.5 V_{cf_eff} : 46 $\triangle V_{\varepsilon}$: -5 **total : -14.5**	**-13.2**
2.52	2.7	V_{ch_eff} : 49.3 V_{cf_eff} : -46 $\triangle V_{\varepsilon}$: -2 **total : 1.3**	**2.5**	V_{ch_eff}: 0.5 V_{cf_eff}: 0 $\triangle V_{\varepsilon}$: -2 **total: -1.5**	**-2.4**	V_{ch_eff} : -48.2 V_{cf_eff} : 46 $\triangle V_{\varepsilon}$: -2 **total : -4.2**	**-3**
2.5	2.5	V_{ch_eff} : 32.4 V_{cf_eff} : -46 $\triangle V_{\varepsilon}$: 0 **total : -13.6**	**-12.7**	V_{ch_eff} : 0 V_{cf_eff} : 0 $\triangle V_{\varepsilon}$: 0 **total : 0**	**0.1**	V_{ch_eff} : -31.9 V_{cf_eff} : 46 $\triangle V_{\varepsilon}$: 0 **total : 14.1**	**13**
2.48	2.3	V_{ch_eff} : 29.8 V_{cf_eff} : -46 $\triangle V_{\varepsilon}$: 2 **total : -14.2**	**-15**	V_{ch_eff} : 0.2 V_{cf_eff} : 0 $\triangle V_{\varepsilon}$: 2 **total : 2.2**	**2.2**	V_{ch_eff} : -27.9 V_{cf_eff} : 46 $\triangle V_{\varepsilon}$: 2 **total : 20.1**	**20**
2.45	2.0	V_{ch_eff} : 29 V_{cf_eff} : -46 $\triangle V_{\varepsilon}$: 5 **total : -12**	**-11**	V_{ch_eff} : 0.4 V_{cf_eff} : 0 $\triangle V_{\varepsilon}$: 5 **total : 5.4**	**4.5**	V_{ch_eff} : -27.1 V_{cf_eff} : 46 $\triangle V_{\varepsilon}$: 5 **total : 21.9**	**23.3**

TABLE IV
COMPARISON OF SENSOR INTERFACE OUTPUTS WITH RESPECT TO IDEAL AMPLIFIER, UNBALANCED DDA, AND BALANCED DDA

Differential Input (mV)	Water content change (%)	Ideal amplifier output (mV)	Unbalanced chopping DDA		Balanced chopping DDA	
			V_{out} (mV)	Error (%)	V_{out} (mV)	Error (%)
0.022	1	2.2	2.27	3.25	2.22	1.10
0.11	5	11	11.44	4.04	11.16	1.46
0.33	15	33	34.36	4.13	33.60	1.82
0.55	25	55	56.84	3.35	55.72	1.31
0.77	35	77	79.29	2.97	77.82	1.07

TABLE V
MEASURED RESULTS OF THE CHOPPING DDA

Parameters	Measured Results
DC gain	100 dB
Unit Gain Bandwidth	1.3 MHz
Phase Margin	67.5 degree
PSRR @ 10 Hz	76 dB
Average Slew Rate	1.2 V/ μS
Load	100 kΩ // 30 pF

shown in Fig. 22. The measured DDA performance is shown in Table V. For offset measurement setup, the amplifier output was connected with a 150-Hz RC low-pass filter to reject the chopping noise. A precision HP 3486 multimeter was used to record the dc offset. Precision power supplies having 1-mV tuning resolution were programmed to provide the analog ground of 1.5 V and different dc inputs with reference to the analog ground of 1.5 V. The input-referred dc offset was then calculated for each input case. Care must be taken that the closed-loop gain is chosen not to saturate the amplifier with a given 3-V supply. For validating the resistance balancing technique, ten chopping DDA chips were measured at a noninverting gain of 10 and a single 3-V supply. The results are depicted in Fig. 23. It is evident that the compensation causes reduction

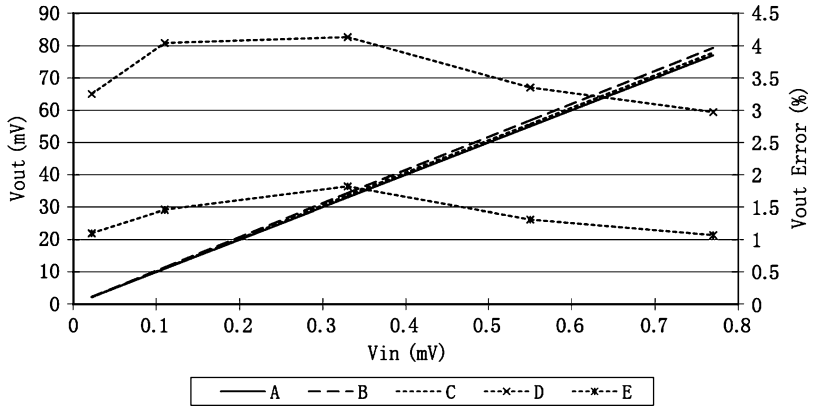

Fig. 21. The simulated results of balanced/unbalanced chopping DDA for micromachined soil entage, and E: balanced error percentage).

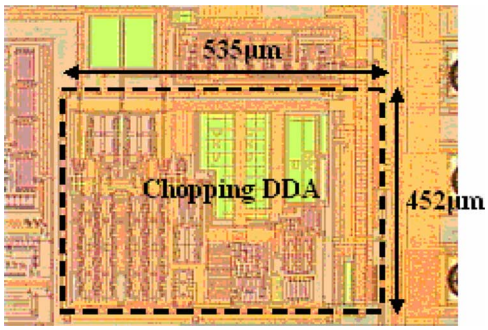

Fig. 22. Microphotography of the chopping DDA.

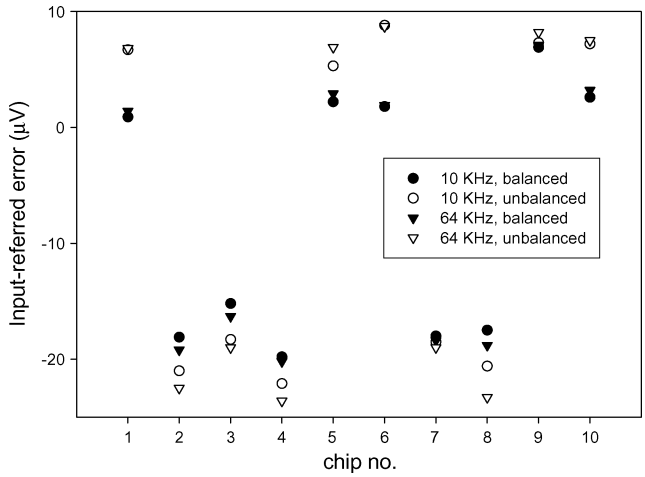

Fig. 23. Measured dc offset results of the balanced/unbalanced chopping DDAs at 10 and 64 kHz chopping frequency and 3-V supply.

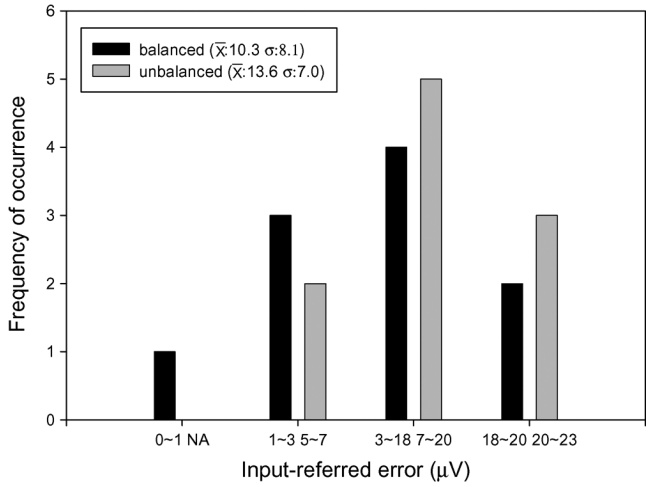

Fig. 24. Histogram of the measured results of balanced/unbalanced chopping DDAs at 3 V and 10 kHz.

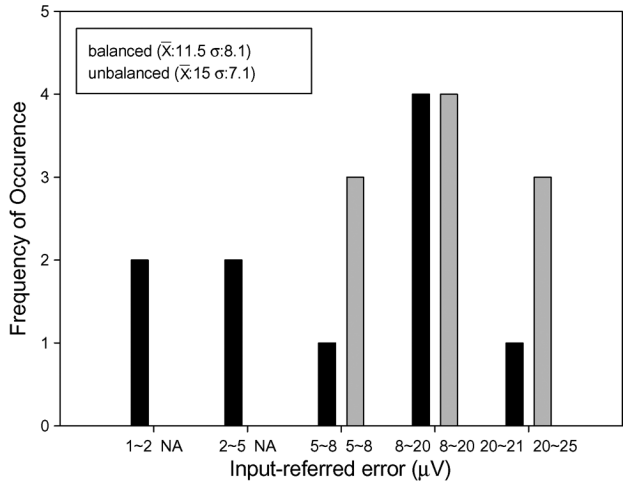

Fig. 25. Histogram of the measured results of balanced/unbalanced chopping DDAs at 3 V and 64 kHz.

of dc offsets, regardless of the chopping frequencies. The dc offset performance is further evaluated through the histograms as plotted in Figs. 24 and 25. With 10 and 64 kHz chopping frequency, the mean value of input-referred offset voltage for compensated chopping DDAs is obtained correspondingly as 10.3 and 11.5μV. More importantly, it is observed a shift in the redistribution of offsets in both histograms. With balancing technique, four out of ten samples move towards lower offset range, with less than 3 and 5 μV offsets at 10 and 64 kHz, respectively, demonstrating the effectiveness of the compensation scheme.

As noise is another critical performance parameter, measurements have been conducted to examine the impact of resistance balancing technique to noise performance. The measured results are depicted in Fig. 26. As can be seen, the input-referred noise root spectral densities based on the closed-loop gain of 10 are 59 $\mathrm{nV}/\sqrt{Hz}$ @10 Hz and 52 $\mathrm{nV}/\sqrt{Hz}$@6 kHz

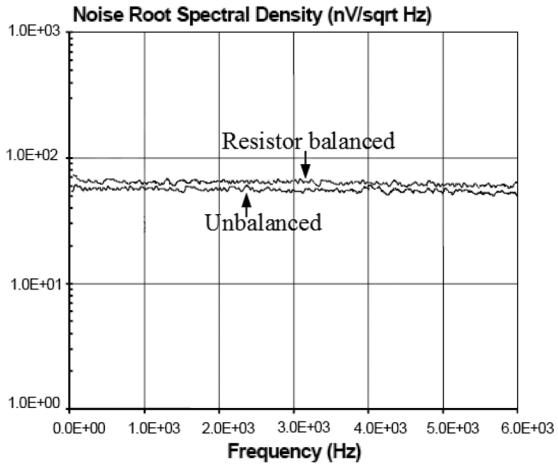

Fig. 26. Input-referred noise with and without balancing resistor from dc to 6 kHz.

without balanced resistor, whereas 62 $\mathrm{nV}/\sqrt{Hz}$@10 Hz and $55\mathrm{nV}/\sqrt{Hz}$ @ 6 kHz with balanced resistor. The result suggests an increase of 3 $\mathrm{nV}/\sqrt{Hz}$, which is sufficiently low to be acceptable. Finally, the almost flat response of noise floor indicates that the $1/f$ noise is suppressed, demonstrating the effectiveness of the proposed scheme.

VI. Conclusion

A new offset reduction approach using a resistance balancing technique for the single-ended chopper-stabilized amplifiers has been presented. A new analytical viewpoint on the switch charge injection in the chopper switch network that is crucial for chopping amplifiers is proposed. Error models together with their respective analytical equations are established for the error analysis to understand the impact of individual error on affecting dc precision. The sum of calculated dominant error sources is compared with the HSPICE simulation results using realistic Level-49 BSIM3 models in a standard 0.6-μm CMOS technology. They agree very well with the theory. An experiment has been conducted on the application of the resistance balancing technique to the fabricated DDA chips. The measured results have confirmed that a respectable number of DDAs has exhibited very low dc offset values, suggesting the proposed work is able to enhance the yield of low-offset amplifiers. This demonstrates the technical merit of simple means to further improve dc precision, which are favorable for sensor applications.

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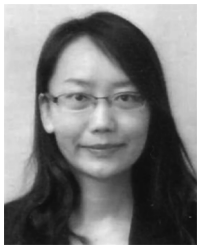

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