CMOS-Fabricated Ring Surface Ion Trap with TSV Integration

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Abstract **–** We present the design, fabrication, and test of ring surface trap on 12-inch wafers with a CMOS process. The design is based on Through Silicon Vias (TSV) interconnects. Up to 200 ions were loaded and cooled; preliminary compensations of electrostatic potential imperfections show that rotational symmetry can be partially restored.

I. Introduction

Micro-fabricated surface electrode ion traps are a leading platform for achieving the blueprint of quantum information processing [1]. These traps are also used for precision spectroscopy [2] and optical frequency metrology [3]. Among recent developments that aim to increase the integration capabilities needed to scale up the platform are the integration of photonic elements for ion addressing [4], [5] and the integration of through-silicon vias (TSV) interconnects [6].

Invented in 2005, surface traps are mostly explored in a linear geometry [7], where wire bondings can access the electrodes from the outer edges. However, for the realization of the surface ion traps with cylindrical symmetry (ring traps), solving the topological problem of contacting isolated electrodes is the prerequisite[8], [9].

Ring traps are interesting for quantum information processing because they may implement a quantum register containing many ions that may be easily shuttled. Their main scientific interest is the possible access to a new quantum degree of freedom: the angular momentum associated to a free tangential motion in the ring [10].

In a previous work, we reported the operation of a linear ion trap with all electrodes connected with TSV [6]. Here we report the trapping and cooling $^{88}Sr^{+}$ ions in a ring surface trap also fabricated with TSV and conventional CMOS technologies. The fabrication process and the TSV compacity also allowed us to integrate in the substrate (under the trap electrodes) several SiN photonic elements (waveguides and gratings) that will be used to steer laser beams to the ions. It is worth mentioning that TSV makes possible integration of different trap geometries, enabling a larger-scale ion trap platform (see Fig. 1).

II. Design and Fabrication

A. Design

Fig. 2 shows the schematic of the ring trap. In our design, ring traps consist of 2 radio-frequency (RF) ring electrodes (R1 and R3), 2 static voltage (DC) ring electrodes (R2 and R4), and 4 DC compensation electrodes. Three sets of electrode sizes are investigated, as shown in Table I. To determine the ion trap height and trap depth, Finite Element Modelling (FEM) is carried out to simulate the pseudopotentials corresponding to different trap sizes. The 2D potentials are shown in Fig. 3(a). The corresponding cross-sections in the radial (R-axis) and vertical (z-axis) directions are shown in Fig. 3(b) and (c). The trapping heights and other parameters corresponding to each trap size are summarized in Table I. We also performed an analytical calculation using the method proposed by R. J. Clark [11]. The difference between FEM and analytical calculation can probably be attributed to the gapless assumption of the analytical calculation. The trapping height of Trap #1 is relatively low (57 µm), requiring tightly focused laser beams. We performed first experiments using Trap #2. In Table II we compiled several trap features from recently-published works about ring-traps [8], [9], [12]. The trap dimensions, trapping heights and integration details are listed.

B. Fabrication

After SiO_2 insulation layer deposition, SiN photonics layer with grating couplers and waveguide is first defined using immersion lithography (Fig. 4(a)). Next, a grounding plane with meshed structure and opening windows is formed using Cu damascene process (Fig. 4(b)). After that, lithography patterning and etching techniques are used to form deep blind vias (20 µm diameter, ~110 µm depth). TSVs are then filled with Cu with electrochemical plating (ECP) after TSV liner, barrier and seed layers deposition (Fig. 4(c)). Subsequently, 3 µm SiO_2 layer is deposited and patterned, followed by ECP of 3 µm Cu and 0.3 µm Au surface as surface electrodes (Fig. 4(d) and (e)). The wafer frontside is temporarily bonded to a handling wafer. The device wafer is then grinded to a thickness of 110 µm. After that, it is etched by ~10 µm to reveal the TSV liner, followed by a knock-off CMP process (Fig. 4(f). Then, the redistribution layer (RDL, 3 µm Cu) is patterned by lithography-defined ECP process (Fig. 4(g)). Subsequently, a polyimide layer (5 µm HD8930) is coated to prevent Cu from oxidizing. Lithography-defined openings are then made on this polyimide layer for the placement of CuSnAg microbumps (Fig. 4(h)). Finally, the device wafer is debonded from the handling wafer.

Glass is selected as the substrate for the interposer due to the superb dielectric property. Its fabrication process is similar to the backside process of TSV integrated trap, where RDL is defined before the polyimide and under bump metallization (UBM). The fabrication details can be found in ref. [13]. The fabricated trap wafer is shown in Fig. 5(a), while the glass interposer wafer is shown in Fig. 5(b).

III. Post Fabrication Characterizations

A. Die-level Characterization

Fig. 6(a) shows the IV tests of Traps #1, #2, and #3. The gaps between R1-R2, R2-R3, and R3-R4 are 6 µm, 6 µm, and 10 µm, respectively. Generally, R2-R3 shows the highest leakage current due to the relatively small gaps and the larger diameter

of R2 compared to R1. However, based on the wafer level Current vs Voltage (IV) test results after frontside processing (Fig. 6(b)), the resistance is typically up to 10^{12} ohm. Process optimization is needed for seed layer etch back on the polyimide. Fig. 6(c) shows the Capacity vs Voltage (CV) tests. The details of the CV test techniques are described in refs. [15] and [16]. Generally, R3-R4 exhibits highest capacitance than other electrode pairs due to the larger diameters. In Trap #2, the R1-R2, R2-R3, and R3-R4 capacitance values are 0.8 pF, 1.4 pF, and 3.5 pF, respectively, which is proportional to the R1, R2, and R3 diameter (Table I). The capacitance is relatively low, as it should be to allow for RF drive of electrodes.

B. Package Level Characterization

Combining the aforementioned factors on pseudopotential simulation and die-level characterization, Trap #2 is selected for ion trap operation. Fig. 7(a) shows the X-ray image of the ring trap with integrated TSV. From the circled region, the TSV interconnects with microbumps are observed. There are 2 TSVs on R1, R2, R4, and 4 TSVs on R3, along with 3 TSVs on each DC compensation electrode. Dummy microbumps are added between ring trap and interposer, facilitating thermal dissipation. A cross-sectional SEM image of the TSVs with microbumps is shown in Fig. 7(b), where the bonded glass interposer is also included (see Fig. 7(c) also). The device-interposer chip is subsequently packaged into a CPGA package for further tests and ion-trapping (Fig. 7 (d)).

The scheme of the setup for a dissipation test based on a resonant circuit is shown in Fig. 8(a), details of the method are reported in ref. [16]. The resonator response of R1 and R3 RF electrodes are measured and benchmarked against an open CPGA package. From the resonance plots (Fig. 8(b)) we deduce an expected power loss quite similar to the TSV-linear trap reported earlier [6]. This indicates that the RF dissipation loss of the TSV-integrated ring trap is within an acceptable range and would not impair the ion trapping operation.

IV. Trap Operation

In order to efficiently trap and cool ions in our ring trap we use basically the same experimental set-up as in ref. [6] except that we chose a different laser geometry that includes two laser cooling directions perpendicular to each other as shown in Fig. 9(a). Along the *y*-axis the cooling laser as well as the photoionization beams (that transforms neutral atoms into ions) are focused using a spherical achromatic lens of 150mm focal length. Along the *x*-axis the cooling laser and the infrared re-pumper beams are focused using a cylindrical lens (150mm focal length). In this way the whole trapping zone is covered by both the cooling and the re-pumper beams. The ions are created and initially trapped in the zone where the photoionization beams are focused and are then free to move along the ring. In Fig. 9(a) one can observe the individual ions in different parts of the ring. Depending on the voltages applied on the compensation DC electrodes one can either localize the ions at chosen positions in the ring or spread them out along the ring (Fig. 9(b)).

However, we found that the trapping potential produced by the electrodes is deformed by parasitic electrostatic fields. This can be seen in Fig. 9(b) where the ions are not uniformly spread along the ring. In the ring regions where the ions are fewer the trapping potential is higher compared to the other parts of the ring. The directions and amplitudes of these parasitic fields does not seem to change in time and are probably due to the presence of charged dusts deposited on the trap surface. Work is in progress to quantitively compensate for the parasitic fields by applying compensating voltages on the 4 sector electrodes surrounding the trapping zone.

The trapping parameters are the following: trap radio-frequency 30MHz, RF voltage amplitude 50V, DC electrode voltages in the range [-10, +10V]. With such parameters we are free to trap from one ion up to a few hundred ions, as shown in Fig. 10.

V. Photonics Integration

Waveguides and gratings have been integrated into the ring-trap substrate, below the electrodes, in order to facilitate the ion-laser addressing as shown in Fig. 10. Gratings have been designed with various radii of curvature (r), as illustrated in Fig. 10(a) and (b). The simulated beam distributions in Fig. 10(c) and (d) show different beam propagations for gratings with $r = 20$ µm and $r = 60$ µm. We measured the beam profiles of gratings with $r = 15$ µm to $r = 60$ µm and obtained the beam waists, as shown in Fig. 11. The measured beam waists provide an understanding of the optical properties of the beam diffracted by the grating, enabling the integration of silicon photonics devices with trapped ions. To complete the integration, a waveguide-grating structure can be inserted that matches to the shape of the ring trap, as shown in Fig. 12. The setup for testing the photonic components in the ion trapping chamber is ongoing. Further details of the photonics integration are discussed in ref. [17].

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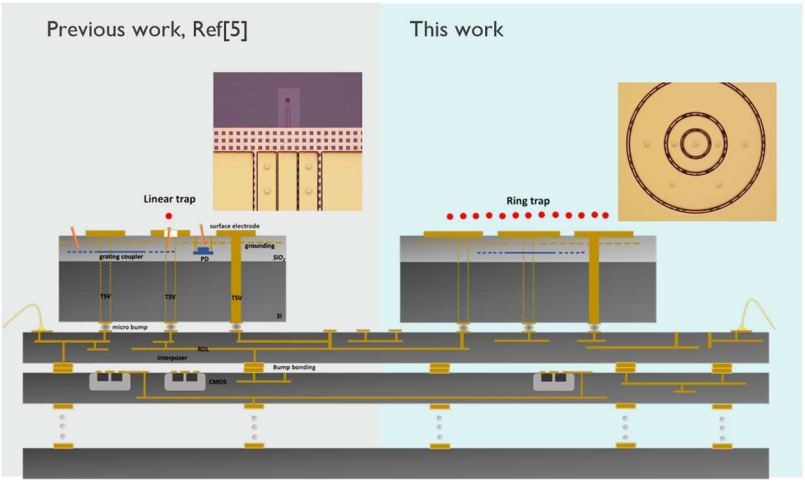

Fig. 1: Architecture of Large-Scale Ion Trap platform: liner trap used for logic operation, while ring trap used for ion storge. Both are located on the same interposer with TSV and microbump connection. The interposer function can be further expanded by wafer-to-wafer bonding

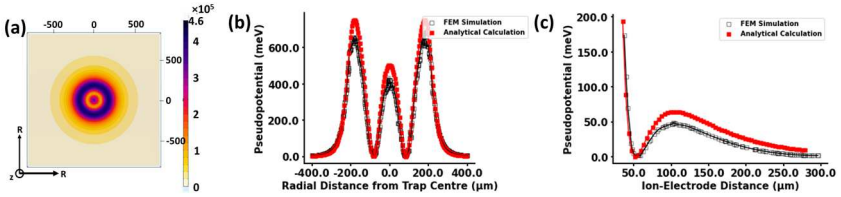

Fig. 3. (a) 2D Pseudopotential distribution in FEM; pseudopotential plots from FEM and analytical calculation along (b) Radial axis, (c) vertical axis (RF amplitude of 100V, RF frequency of 60MHz)

Table I. Summary of trap parameters, ion ring height, ion ring diameter, and trap depths (RF amplitude of 100V, RF frequency of 60MHz)

Trap	R1 (μm)	R2 (μm)	R3 (μm)	R4 (μm)	Ion ring height: FEM Simulation *(Analytical Calculation)*	Ion ring diameter: FEM Simulation *(Analytical Calculation)*
#1	60	130	300	600	90 μm *(78.9 μm)*	140 μm *(156.6 μm)*
#2	60	110	200	600	57 μm *(52.2 μm)*	160 μm *(164.4 μm)*
#3	80	130	300	600	75 μm *(65.3 μm)*	200 μm *(197 μm)*

Table II. Comparison of this work with various ring traps

Ring Traps	RF electrode outer radius (μm)	Ion ring height (μm)	Ion ring diameter (μm)	RF potential amplitude (V)/frequency (MHz)	Numbers of ion trapped	Interconnection	I/O connection
[8]	>650	82	1248	80/52.9	~400	Multi-layer metallization	Perimeter, 30 μm above trap
[9]	1100	390	90	220/5.81	~15	Low AR through SiO_2 vias	N/A
[12]	~3000	100	~6000	100/20	12 trapping sites	Multi-layer metallization	No
This work	300	~75	~200	50/30	~200	High AR through silicon via	Interposer underneath

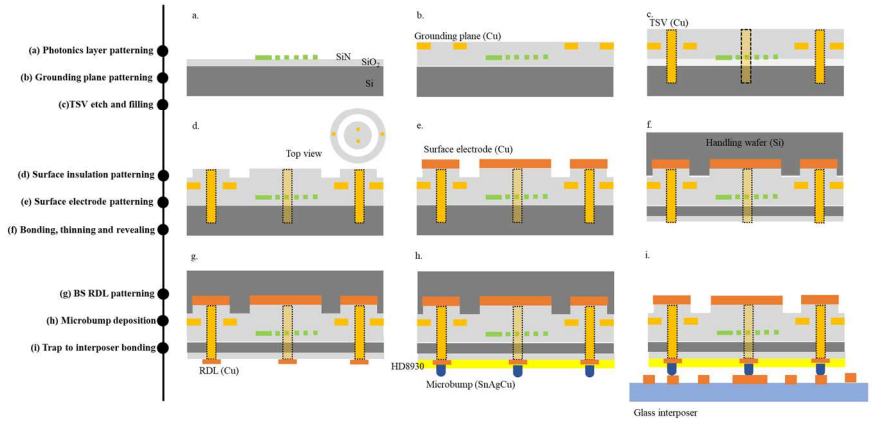

Fig. 4. Fabrication process of photonics and TSV integrated trap; photonics is integrated as the first functional layer but tested separately

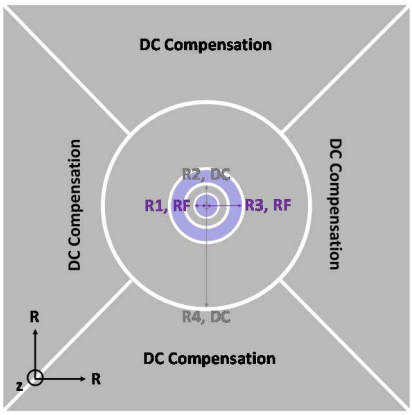

Fig. 2. 2D schematic diagram of ring trap. The first and third inner rings are RF electrodes, while the others are DC electrodes

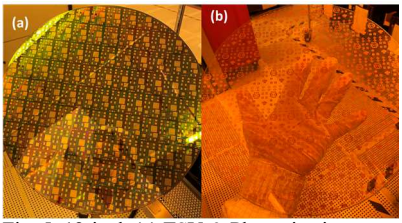

Fig. 5. 12-inch (a) TSV & Photonics-integrated trap device wafer, (b) Interposer glass wafer

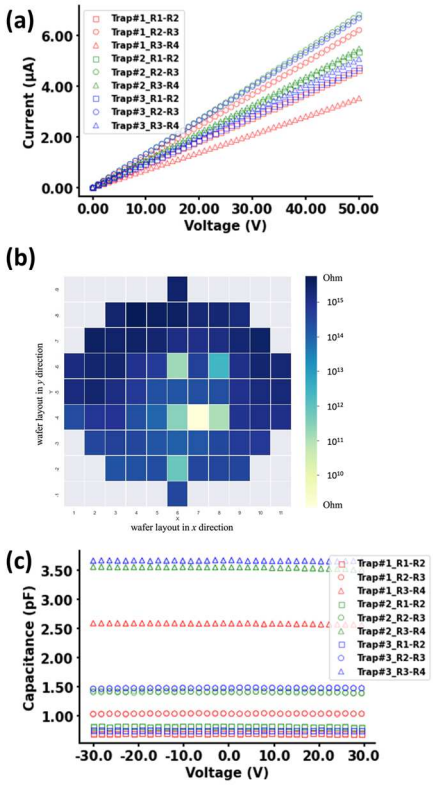

Fig. 6. (a) IV tests of ring trap, (b) wafer-scale leakage current test (tested after frontside process) (c) CV tests of ring trap

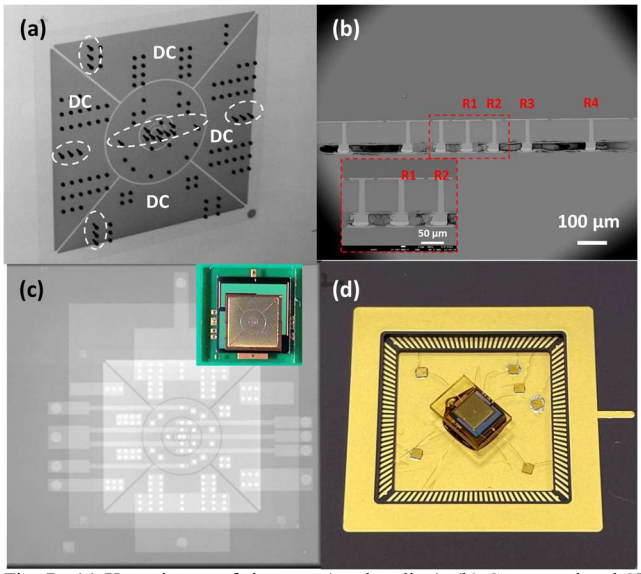

Fig. 7. (a) X-ray image of ring trap (pre bonding), (b) Cross-sectional SEM image of ring trap bonded onto glass interposer, (c) X-ray image of ring trap bonded onto glass interposer, (d) Ring trap-glass interposer on CPGA package

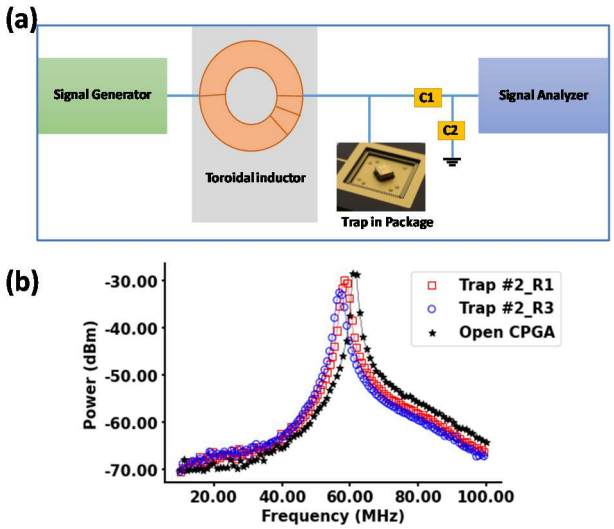

Fig. 8. Resonator test of ring trap with CPGA: (a) test setup, C1:C2=1:20 (b) resonator test results of ring trap and open CPGA

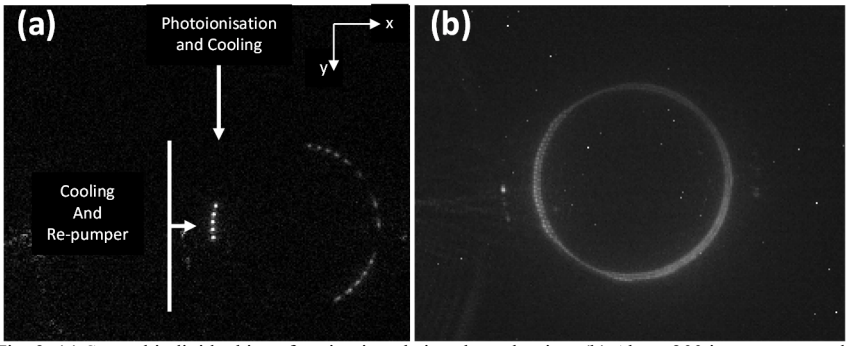

Fig. 9. (a) Several individual ions forming ion chains along the ring. (b) About 200 ions are trapped all along the ring. Individual white spots outside of the ring are either diffused laser light by the trap surface or white camera pixels. (Experiment video in: https://youtu.be/fPuiouDcpz0)

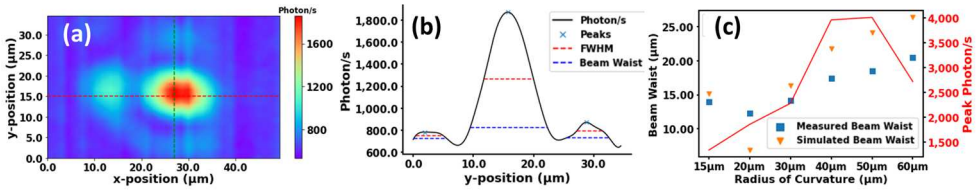

Fig. 11. (a) Typical beam profile, (b) light intensity along y-axis extracted from beam profile, (c) compiled optical properties of light coupled out from gratings with various radius of curvature

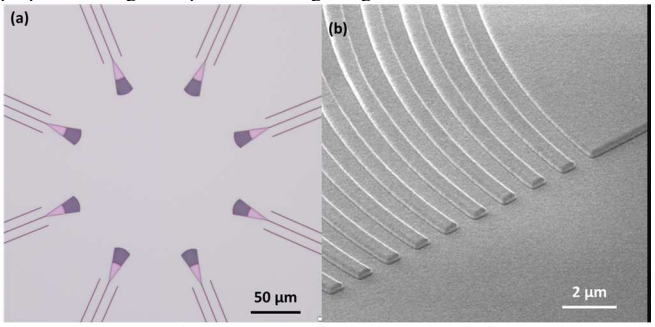

Fig. 12. (a) Integrated output grating design in ring trap, (b) Magnified grating structure under electron microscope

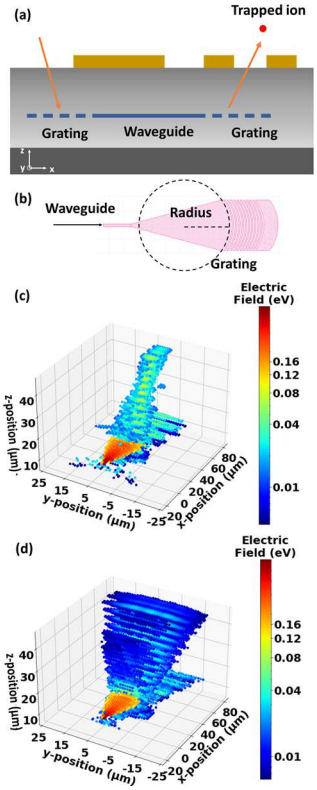

Fig. 10. (a) Schematic diagram of optical addressing by integrated silicon photonics, (b) typical grating design; electric field distribution from, (c) r = 20 µm grating, (d) r = 20 µm grating