STUDY OF PLASMA ETCHING OF SILICON CARBIDE

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Summary

Etching is a very crucial process in the fabrication of SiC microelectronic devices such as Schottky diodes, metal-semiconductor-field-effect-transistors (MESFETs), metal-oxide-semiconductor-field-effect-transistors (MOSFETs). Due to its exceptional chemical inertness, plasma etching is the only practical means of etching SiC. Plasma etching is also advantageous as it is compatible with the conventional complementary metal-oxide-semiconductor (CMOS) process technology. The plasma etching techniques studied so far include the conventional reactive ion etching (RIE) and high density plasma (HDP) etching such as electron cyclotron resonance (ECR) plasma and inductively coupled plasma (ICP). With more stringent requirements placed on the etch rate (depth), etching profiles, surface quality for advanced SiC devices, it is of great importance to understand the mechanisms and behaviors of SiC plasma etching, including the physical damages involved and its consequences on the electrical characteristics of the devices.

In this work, the etching behaviors of *n* type bulk 4H-SiC was studied using RIE and ECR etching processes, using halogen based chemicals, with/without added oxygen. The etch rate, surface roughness and contamination have been measured and analyzed. The etching of SiC based on the ECR plasma technique has been modeled using an artificial neural network based on an improved training algorithm. The modeling results were studied and physical interpretations were given. The plasma etching induced electrical damage was studied using Schottky barrier diodes (SBDs)

as test devices. The objective of this project is to develop an optimum plasma etching process for the fabrication of SiC power devices, with precise etching control and minimum induced damage.

Firstly, we studied the conventional RIE of SiC based on CHF_3+O_2 plasma. The etch rate, surface roughness, and surface composition analysis were studied by varying the O_2 fraction, defined as the ratio of the oxygen flow rate against the total gas flow rate, R.F. power, and process pressure. It was found that the neutral radical F atom concentration plays a dominant role in the etching. The addition of oxygen enhances the etch rate by increasing the F concentration at low O_2 fraction but retards the etch rate at high O_2 fraction by diluting F concentration and forming an oxide-like layer. An increase in R.F. power greatly enhances the etch rate by providing higher neutral radical density, positive ion density, as well as impinging ion energy. As a result, both the reactive rate of chemical reactions attributed to F atoms and the physical ion bombardment are enhanced. In contrast, with increasing process pressure, despite an enhancement in the reaction rate of the chemical reaction, the etch rate decreases due to the weakening of impinging ion energy. The surface roughness is found to be strongly related to the D.C. self-bias, and less affected by the O_2 fraction. At low D.C. self-bias, the etched surface becomes rougher with increasing D.C. self-bias. Auger Electron Spectroscopy (AES) study has related such surface roughness to the micromasking effect induced by Al clusters and carbon residues (C rich layer). It was found that these micromasks can be removed by strong ion bombardment. A threshold D.C. self-bias value was noted, above which no micromasking effect was present. From the results, a process recipe with optimized process parameters has been developed. It gives the highest etch rate of 35.6 nm/min and an r.m.s. surface

roughness of 1.65 nm, achieved with the O_2 fraction, R.F. power and process pressure set at 20%, 200 W (1.13W/cm^2), and 100 mTorr, respectively.

Secondly, we studied the modeling of SiC ECR plasma etching using artificial neural network, based on the BFGS (Broyden, Fletcher, Goldfarb, and Shanno) optimization algorithm. The neural network training was conducted using our ECR etching test results. The results of the new BFGS training algorithm were compared with those obtained using the conventional back propagation (BP) algorithm based on the same feed-forward neural network (FNN) structure with different hidden neuron numbers, different number of iterations and various learning rates. It is shown that the BFGS algorithm requires less hidden neurons and less iteration to obtain the same training results, and it also provides much smaller cross-validation (CV) errors. The r.m.s. and maximum error values of CV test for the BFGS algorithm were less than 5% and ±10%, respectively, while the error for the training samples were even lower. Therefore, the FNN trained by the BFGS algorithm possesses much better approximation and generalization ability. It should be noted this is the first time that the algorithm has been used for the training of FNN in the modeling of plasma etching, and the SiC ECR process modeling results demonstrate that the FNN trained by the BFGS algorithm are fast, reliable and accurate.

Thirdly, we studied the ECR plasma etching of SiC in SF_6+O_2 plasma. It was demonstrated that using the high density ECR plasma, an etch rate as high as 78.1 nm/min can be achieved at 60% O_2 fraction, 550 W microwave power, -200V D.C. bias and 4 mTorr process pressure. The etched surface is smooth, with an r.m.s. surface roughness of 1.48 nm and with no sign of micromasking effect. With the help of FNN numerical modeling trained by the BFGS algorithm, the etching behavior of

ECR was studied with varying process parameters which include microwave power, D.C. bias, process pressure and O_2 fraction. The modeling results of the etch rate were analyzed using 3-D surface plots and 2-D contour plots, which clearly reveal the interaction of the various process parameters and their resultant effects on the etch rate. It is found that by varying O_2 fraction and process pressure, optimized etch rate peaks can be achieved. Increasing D.C. bias and microwave power are found to result in the optimized etch rate peaks occurring at higher O_2 fraction and process pressure, respectively. In addition, increasing D.C. bias or microwave power will increase the etch rate. However, there is saturation in the etch rate at higher D.C. bias, which however, does not occur at higher microwave power. Based on these modeling results, detailed physical interpretations of the etching process are given in terms of the chemical reaction of 4H-SiC with F, O, and positive ion bombardment.

Lastly, we designed and fabricated thermal oxide field plate terminated SBDs to study plasma etching induced damage (PEID). In a set of carefully designed experiments, we deliberately separated the contribution of damages from different sources, i.e. chemical etching and physical sputtering. The D.C. electrical properties of the SBDs etched with RIE plasmas with characteristics that were mainly dominated by chemical etching (CE), physical sputtering (PS), and reactive ion etching (CE+PS), have been investigated and compared with an unetched control sample (CR). It is found that chemical etching results in a lower Schottky barrier height (SBH) for the CE sample as compared to the CR sample, which is attributed to the formation of a carbon-rich layer at the surface. Their ideality factor and series on-resistance, however, do not deviate significantly. On the other hand, the PS sample is found to have a high on-resistance, high ideality factor and low SBH. The deep level transient spectroscopy (CDLTS) characteristics of the PS sample reveal the presence of four deep-level

defects, which are attributed to impinging positive Ar ions bombardment induced damage. The observed inhomogeneity of the electrical characteristics for the CE+PS sample, can be modeled by two SBDs with different SBHs connected in parallel. The SBDs with a lower SBH and high leakage current is related to chemical etching induced damage, while that with a higher SBH suffers from a slight physical sputtering damage but has no chemical etching induced damage. Through this study, the effects of chemical and physical etching induced damage on the electrical characteristics of the SBDs have been examined, and the understanding achieved is important in the formulation of plasma recipes that will minimize PEID.

Table of Contents

List of Abbreviations

A.C.	Alternating current
AES	Auger Electron Spectroscopy
AFM	Atomic Force Microscope
AI	Artificial Intelligence
ANN	Artificial Neural Network
BFGS	Broyden, Fletcher, Goldfarb, And Shanno
BP	Back Propagation
BPNN	Back Propagation Neural Network
CCD	Central Composite Design
CCP	Capacitively Coupled Plasma
CDLTS	Capacitance Deep Level Transient Spectroscopy
CMOS	Complementary Metal-Oxide-Semiconductor
CTE	Coefficients of Thermal Expansion
CV	Cross-Validation
D.C.	Direct current
DI water	Deionized Water
DOE	Design of Experiments
ECR	Electron Cyclotron Resonance
GA	Genetic Algorithm
HDP	High Density Plasma
HNN	Hidden Neuron Number
ICP	Inductively Coupled Plasma
IMPATT	Impact Ionization Avalanche Transit Time
IPA	Isopropyl Alcohol
ITO	Indium-Tin-Oxide
LR	Learn Rate
L-TLM	Linear Transfer Length Method

MEMS	Microelectromechanical System
MESFET	Metal Semiconductor Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MS	Metal-Semiconductor
M.W.	Microwave
PAE	Power Added Efficiency
PECVD	Plasma Enhanced Chemical Vapor Deposition
PFC	Power Factor Correction
PEID	Plasma Etching Induced Damage
RCA	Radio Corporation Of America
R.F.	Radio Frequency
RIE	Reactive Ion Etching
r.m.s.	Root-Mean-Square
RSF	Relative Sensitivity Factor
RSM	Response Surface Methodology
RTA	Rapid Thermal Anneal
SBC	Schottky Barrier Contact
SBD	Schottky Barrier Diode
SBH	Schottky Barrier Height
SC-1	Standard Clean Step 1
SC-2	Standard Clean Step 2
sccm	Standard Cubic Centimeters Per Minute
SEM	Scanning Electron Microscope
TE	Thermionic Emission
UCS	Unetched Control Sample

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Background

Silicon carbide (SiC) is a wide bandgap semiconductor with many excellent properties. For example, 4H-SiC has a much higher bandgap of 3.28 eV, high breakdown electric field of 3MV/cm at a doping level of 2×10^{15} cm^{-3}, and higher thermal conductivity of 4.9 $Wcm^{-1}K^{-1}$ than the conventional semiconductor Si. In addition, it has a high electron saturation drift velocity of 2×10^{7} cm/s and can also operate at much higher temperatures of above 400°C and with a high breakdown electric field of 2.0 ~ 2.5 MV/cm [1-3]. Despite its advantages, and the fact that SiC was discovered earlier than Si [4], there was no significant breakthrough in its growth technology until 1980's when bulk SiC crystal was successfully grown by a seeded sublimation technique, which is now commonly known as the modified Lely process [5]. The use of this new technology enables commercial production of SiC wafers of consistently high quality and reasonable wafer size: from the year 2007, high quality 4-inch SiC wafers have been commercially available [6].

Due to its many desirable properties, SiC has found applications in many areas, which include power electronics [7, 8], radio frequency and microwave transistors [9], radiation hard electronics [10], various sensors working in harsh and/or strong

irradiation environments, such as sensors for jet engines or space stations [11, 12] , microelectromechanical system (MEMS) [13], photoconductive switches [14]. So far, its application has been most successful in the area of power electronics. SiC based Schottky rectifiers that can offer blocking voltages and conduction currents rating up to [600 V, 20 A] and [1200 V, 10 A/20 A] have been successfully developed and are commercially available [8, 15]. With near ideal performance in high voltage switching operations, these rectifiers can be used in various applications, including Power Factor Correction (PFC) circuits in A.C.-D.C. power supplies, AC motor drives, solar inverters [16, 17]. Besides rectifiers, SiC has also been widely employed as the semiconductor for R.F./M.W. power devices, for example, metal-semiconductor-field-effect-transistor (MESFET) that can be used in a variety of hybrid and monolithic high power microwave amplifiers. The R.F. power available from an impact ionization avalanche transit time (IMPATT) diode in SiC is about a hundred times higher than in Si or GaAs [9, 18]. MESFETs marketed by Cree Inc. boast a best power performance of 5.2 W/mm at 3.5 GHz and 63% power added efficiency (PAE) for a 0.7 μm·48mm device in a monolithic microwave IC (MMIC) [9, 19].

It should be noted that SiC is the only compound semiconductor that can be thermally oxidized to form thermal oxide for use as masks in processing and device passivation layers, as well as high quality thermal oxide to serve as gate dielectrics. Thus, it is possible to fabricate all devices found in Si integrated technology using SiC, including high quality, stable metal-oxide-semiconductor-field-effect-transistor (MOSFET) transistors, such as trench U-shape MOSFETs and double-implanted MOSFETs [8, 15], and integrated circuits. This is an area of work that is ongoing, and once it is successfully developed and commercialized, will certainly propel and accelerate the SiC technology further for more practical applications.

1.2 Motivation

During the last decade, much progress has been made in advancing SiC based devices and related processing technology. This progress has been driven by the need to develop SiC electronic devices that can operate at high power, high frequency, high temperature and high field regimes, beyond the operating range of conventional Si based devices. In the development of process technology for the fabrication of SiC devices, it is important to be able to pattern and etch SiC with good process control, reproducibility, high etch rate and high quality etched surface with minimum defects. However, SiC has long been well known for its hardness and chemical inertness. It has a Mohs hardness of 9.0, and is the second hardest material next to diamond [20] Indeed, due to its extreme hardness, SiC has been the material widely used in sand paper and as lapping and polishing abrasives [21] In microelectronic application, the hardness and chemical inertness of SiC allow it to operate in hostile environments. However, the same strengths also render the etching of SiC challenging. As SiC can withstand the attack of most conventional wet etching agents at room temperature [21], plasma etching is the only practical etching technique available [22]. To date the reactive ion etching (RIE) technique has been widely applied for the etching of SiC. [21] New plasma etching techniques that utilize high density plasma such as electron cyclotron resonance (ECR) plasma, inductively coupled plasma (ICP) etc, have also been developed to enhance the etch rate of SiC [21].

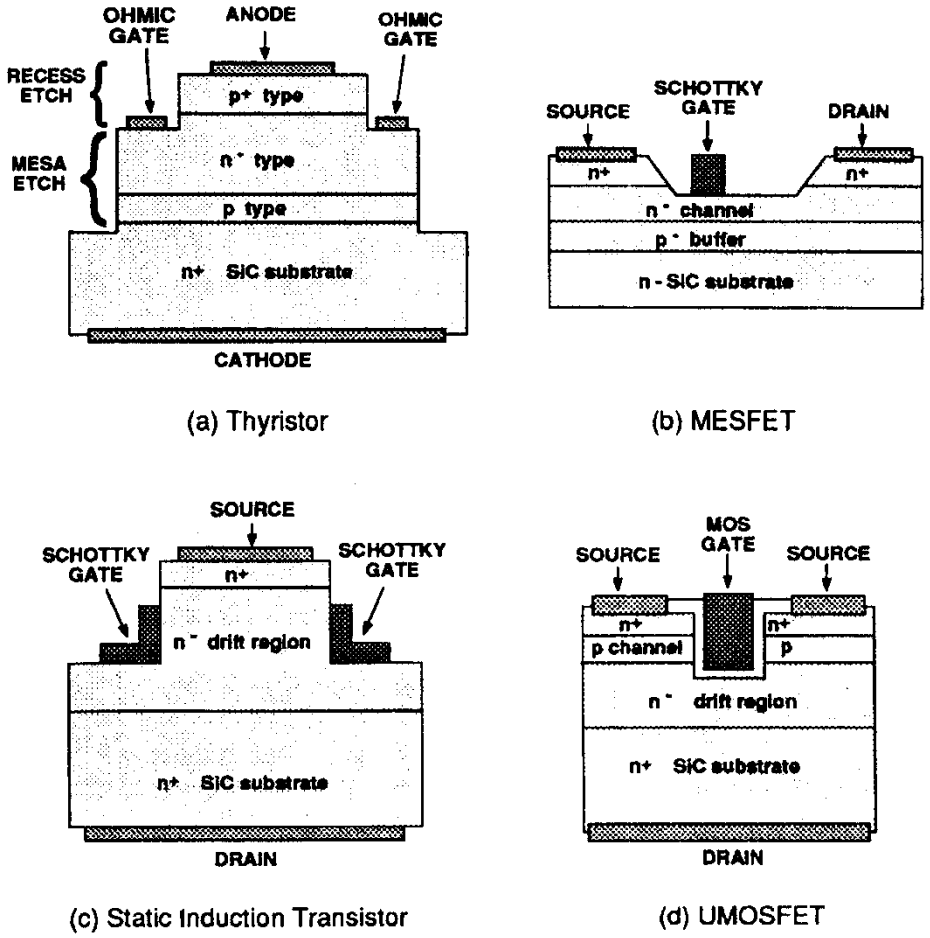


Fig. 1.1: Schematics of SiC power switching devices (a) thyristor, (b) MESFET, (c) static induction transistor, and (d) UMOSFET [24].

Despite the rapid development in SiC plasma etching technology, there is a need to achieve an in depth understanding of the plasma etching process and mechanism for SiC, and advance the technology to meet emerging process requirements. For example, with the development of modern and advanced SiC power devices as illustrated in Fig. 1.1, the requirements placed on the plasma etching process have become more stringent and diversified. Mesa etching will require higher etch rate to achieve reasonable etch time but has less demand on the etch depth control. On the other hand, gate recess etching requires more precise etch rate control and high quality etched surfaces with minimum etching-induced damage, which otherwise may degrade the

electrical characteristics of the devices. This is especially crucial for channel or contact recess etching, which has a very high demand on surface quality. Towards this end, a detailed understanding of the etching mechanism and its effect on the quality of the etched surface is essential. The advance of SiC MEMS technology and the development of various sensors that can operate in harsh and irradiative environment [10-12] have also introduced new demands on the etching process of SiC, which include high etch rate and high aspect-ratio.

Coupled with the need to tailor SiC etching process to meet specific requirements, there is also a need to improve the etching process design and control. It should be noted that in many SiC devices, the various SiC layers with different dopant types and/or doping levels do not have sufficient etching selectivity to serve as etch stop layer to each other [23]. Therefore, the etching process control is achieved mainly through having a good knowledge of the plasma etching behavior and a precise control of the etching time. To understand in detail the plasma etching process, it is important to develop a reliable, practical and robust plasma etching model that can accurately predict the etching characteristics, for example, the etch rate as a function of all the process parameters. Such a model is not only useful for process control and design, but it can also help in the understanding of the etching mechanisms involved and the interaction of different process parameters on the etching characteristics.

1.3 Objectives

The objective of this work is to study plasma etching of 4H-SiC for device fabrication using the RIE and ECR-RIE techniques. The main aims of the project include understanding in detail the etching characteristics and the mechanisms

involved, and the effects of the various process parameters such as the etchant gas mixture, microwave power, R.F. power, D.C. self-bias and process pressure on the etch rate, surface roughness and etched surface morphology. The surface damage due to etching will also be investigated through studying the electrical characteristics of 4H-SiC Schottky barrier diodes fabricated that are subjected to different etching processes. We will also develop a model for the etching process using artificial neural networks to simulate and predict the etching characteristics, and understand the interaction of the various process parameters in the complex plasma process. This is important towards achieving a better process control necessary to meet different etching requirements in the fabrication of 4H-SiC devices. We also target to develop and optimize etching recipes for 4H-SiC that will give rise to higher etch rate with precise etch rate control and minimum etching induced damage.

In the following, the objective of the research work is elaborated in three parts.

1 We aim to study the reactive ion etching (RIE) of n^+ type bulk 4H-SiC based on CHF_3+O_2 plasma as a function of the etchant gas composition, R.F. power and process pressure, and to develop an optimized working recipe. The etching behavior will be characterized in terms of the etch rate, etched surface roughness and surface atomic elements analyzed using Auger electron spectroscopy (AES).

2 We target to develop a numerical model for studying the electron cyclotron resonance (ECR) plasma etching of 4H-SiC. A feed-forward neural network (FNN) trained by the BFGS (Broyden, Fletcher, Goldfarb, and Shanno) algorithm will be developed. Based on the FNN developed, the etching

behavior of 4H-SiC based on an ECR plasma will be modeled and analyzed with physical interpretations provided.

3 We seek to compare and understand plasma etching induced damage (PEID) on 4H-SiC samples that are subjected separately either to mainly chemical etching, or mainly to physical etching, or to a combination of both chemical and physical etching processes. A batch of 4H-SiC Schottky barrier diodes (SBDs) will be fabricated and subjected to the above different etching processes. Their electrical characteristics, such as series on-resistance, Schottky barrier height (SBH), ideality factor, will be determined and correlated to the PEID involved in the different etching processes. The results are useful towards optimizing the RIE process to alleviate or even eliminate PEID.

1.4 Major Contributions of the Thesis

The major contributions of this thesis are summarized as follows:

a) The reactive ion etching (RIE) of n^+ type 4H-SiC based on CHF_3+O_2 plasma has been studied by varying the O_2 fraction, R.F. power and process pressure. Oxygen is found to directly affect the F concentration and hence the etch rate. In addition, the formation of an oxide-like layer at high O_2 fraction can result in a decreased etch rate. Increasing the R.F. power has been found to enhance the etch rate, while increasing process pressure has been shown to lead to an opposite effect. Very rough etched surface observed under certain RIE conditions and has been attributed to Al contamination arising from the etching chamber electrodes and C residue induced micromasking effect. This effect is

observed to be highly correlated to the physical ion bombardment controlled by the D.C. self bias. A threshold D.C. self-bias of between -320 V and -330 V is observed, below which the micromasking effect exists, and above which it is absent. In this study, an optimum etching process recipe has been developed, with a 20% O_2 fraction, 200 W (1.13 W/cm^2) R.F. power, 100 mTorr process pressure, and 10 sccm total feed in gas flow rate. The optimized etch rate achieved is 35.6 nm/min, and the etched surface is very smooth with an r.m.s. surface roughness of 1.65 nm. The optimized recipe has been successfully applied by other research students for the fabrication of high quality 4H-SiC based MESFETs and MOSFETs.

b) A numerical model using a feed-forward neural network (FNN) has been developed to simulate ECR SF_6+O_2 plasma etching of 4H-SiC. The FNN was trained by the BFGS (Broyden, Fletcher, Goldfarb, and Shanno) optimization algorithm, which has been used for the first time in the area of plasma etching process modeling [25]. The BFGS algorithm is superior to the conventional back propagation (BP) algorithm, as it has resulted in much smaller errors, with 5 % r.m.s. error and ±10 % maximum error of cross-validation (CV) test, while the errors for the training samples are even lower. The simulated etch rates of 4H-SiC are found to be consistent with the experimental results. The FNN trained by the BFGS algorithm is powerful and can be used to develop optimized etching recipes for 4H-SiC for different applications.

c) Using the FNN trained by the BFGS optimization algorithm, the ECR plasma etching of 4H-SiC with a SF_6 + O_2 plasma was numerically simulated. The results clearly revealed the relationship between the etch rate and the various

process parameters such as the microwave power, D.C. bias, process pressure and O_2 fraction. In the analysis of the results, physical interpretations have been given to explain the plasma and etching characteristics as a function of the process parameters, and the roles of pure chemical reaction and physical ion bombardment (sputtering) on the overall etching behavior. The simulation results suggest that by controlling these process parameters, it is possible to develop optimized etching recipes for SiC that can cater for different applications.

d) The ECR SF_6+O_2 plasma etching of n^+ doped bulk 4H-SiC was studied in terms of the role of oxygen in the etching process. The Auger electron spectroscopy (AES) results suggest that chemical etching of carbon by oxygen is not significant even at high O_2 fraction. With an increase in O_2 fraction, the surface roughness is found to increase, due to surface oxidation and oxygen ion related physical ion bombardment. However, even at the highest O_2 fraction, relatively smooth etched 4H-SiC surfaces free of Al clusters and C rich-layers were observed, which is attributed to the high D.C. bias applied. The highest etch rate that has been achieved for 4H-SiC using the ECR plasma etching is 79.1 nm/min, under the process conditions of 550 W microwave power, -200 V D.C.bias, 4 mTorr process pressure, and 60% O_2 fraction.

e) Plasma etching induced damage (PEID) was studied on *n* type 4H-SiC using thermal oxide field terminated SBDs fabricated in this work as the test vehicle. Three plasma etching processes with characteristics dominated by chemical etching, physical sputtering, and their combination, were performed to understand the contribution of damages from the different sources. 4H-SiC

SBDs not subjected to etching were also fabricated for comparison. Capacitance-voltage (*C-V*), current-voltage (*I-V*) and deep level transient spectroscopy were used to assess the quality of the SBDs, and extract their key parameters, which include ideality factor, series on-resistance and Schottky barrier height (SBH). Surface damage arising from chemical etching has been found to lower the SBH, which in turn leads to a high leakage current. On the other hand, damage due to physical sputtering has resulted in a very high series on-resistance, a high ideality factor, and *I-V* characteristics that deviate from the thermionic emission model. As for the damage that is due to a combination of chemical etching and physical sputtering, inhomogeneity in electrical characteristics has been observed at the Schottky interface, with electrical characteristics that can be modeled as a pair of SBDs with different SBHs connected in parallel. The SBD model with a lower SBH and high leakage current can be attributed to the Schottky contact area that is dominant by chemical etching induced damage, while that with a higher SBH can be assigned to the Schottky contact area with the chemical etching induced damage being etched away by physical sputtering.

1.5 Organization

There are seven chapters in this dissertation, which are organized as follows:

CHAPTER ONE The background and the motivation of the research are presented. The main contributions of the dissertation are summarized, and the organization of this dissertation is given.

CHAPTER TWO An introduction to monocrystalline SiC is given, including its crystalline structure, physical and electrical properties. Also included is an introduction and literature survey of plasma etching process, mechanism of plasma etching of SiC, neural network and its modeling of plasma etching of FNN trained by the BFGS optimization algorithm, and plasma etching induced damage.

CHAPTER THREE The reactive ion etching (RIE) of n^+ type bulk 4H-SiC based on CHF_3 and O_2 plasma is systematically studied by varying the various process parameters, which include etchant gas chemical composition, R.F. power, and process pressure. The etch rate and surface roughness are characterized and discussed in relation to the micromasking effect. Based on the study, an optimized recipe working for $CHF_3 + O_2$ reactive ion etching of 4H-SiC is developed.

CHAPTER FOUR A numerical modeling of electron cyclotron resonance (ECR) plasma etching of 4H-SiC using artificial neural network is developed. The modeling results obtained are also compared and verified using experimental etching results.

CHAPTER FIVE The ECR plasma etching of n^+ type bulk 4H-SiC based on SF_6+O_2 plasma is presented. By varying the etchant gas chemical composition, the etching behaviors are studied in terms of the etch rate and surface roughness. An artificial neural network has been trained and used to model the effects of etchant gases chemical composition, microwave power, D.C. bias, and process pressure on the ECR plasma etching of 4H-SiC. Physical interpretation of the modeling results is also presented.

CHAPTER SIX Plasma etching induced damage (PEID) attributed to chemical plasma etching, physical sputtering, and a combination of both mechanisms is studied using *n* type 4H-SiC thermal oxide field plate terminated Schottky barrier diodes

(SBDs). The capacitance-voltage and current-voltage characteristics of the SBDs fabricated and subjected to the different etching mechanisms are compared and discussed in relation to the damage induced.

CHAPTER SEVEN Conclusions of the research work and recommendations for future work are presented.

Chapter 2

Plasma Etching of SiC – A Literature Review

2.1 Introduction

Silicon carbide (SiC) is a wide bandgap semiconductor with attractive material properties for microelectronic applications [26-35]. Due to its high electron saturation velocity, high breakdown electric field strength and high thermal conductivity, silicon carbide is highly suitable for high-power and high frequency power devices [36, 37]. The material strength and stability also render SiC a useful candidate for microelectromechanical systems (MEMS) technologies [38]. One of the crucial steps in the fabrication of SiC devices is the etching process for creation of mesa isolation structures, recessed gate, recessed channel. However, due to the exceptional chemical inertness of SiC and the strong bonding between Si and C (Si-C bond energy is 1.34 times stronger than the Si-Si bond energy) [23], etching of SiC with good etched surface quality and high etch rate is a major technological challenge. Currently, plasma-based etching is the only practical way of etching SiC. In this chapter, beginning with an introduction of SiC material properties, a literature survey will be presented to specifically address the current plasma etching technology for SiC.

2.2 Mono-Crystalline Silicon Carbide

2.2.1 Crystallographic Structure

SiC is the only known binary compound of silicon and carbon that possesses one-dimensional polymorphism called polytypism. In a polytypic compound, similar sheets of atoms or symmetrical variants are stacked atop each other and related according to a symmetry operator. The differences between the polytypes only arise in the direction perpendicular to the sheets (along the c-axis) [39]. In SiC, each sheet represents a bilayer composed of one layer of Si atoms and one layer of C atoms. The basic unit in the SiC polytypes consists of a primarily covalently bonded (88% covalent and 12% ionic) tetrahedron of four C atoms with one Si atom at the centre as shown in Fig. 2.1. The SiC crystal is composed of these basic tetrahedron structure joined to each other at the corners [39].

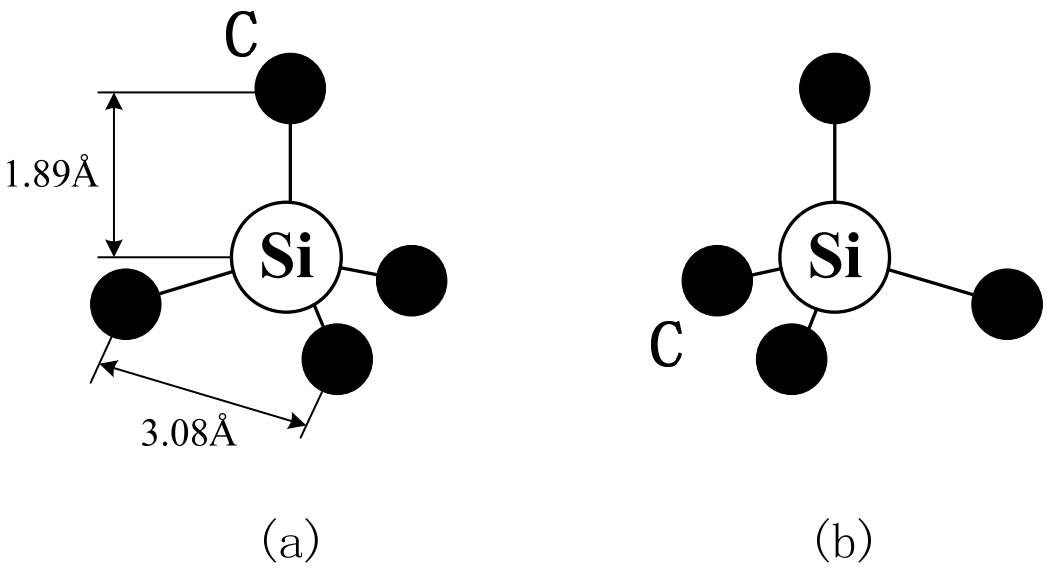


Fig. 2.1: (a) The basic structure unit in SiC. (b) The structure of (a) after being rotated 180º around the stacking direction [39].

The different stacking sequences of the SiC bilayers give rise to numerous polytypes of SiC, which are named according to their stacking sequence. Although as many as 250 or more polytypes of SiC have been reported [40], only a few of them (such as 4H-SiC and 6H-SiC) are commercially available and used for semiconductor devices. Their crystallographic structures and stacking sequences are shown in Fig. 2.2. The 3C-SiC, also referred to as β-SiC, is the only form of SiC with a cubic crystal lattice structure. The non-cubic polytypes of SiC are referred to as α-SiC. The 4H-SiC and 6H-SiC are two of the many possible SiC polytypes with a hexagonal crystal structure. Similarly, 15R-SiC is the most common of the many possible SiC polytypes with a rhombohedral crystal structure [39, 41].

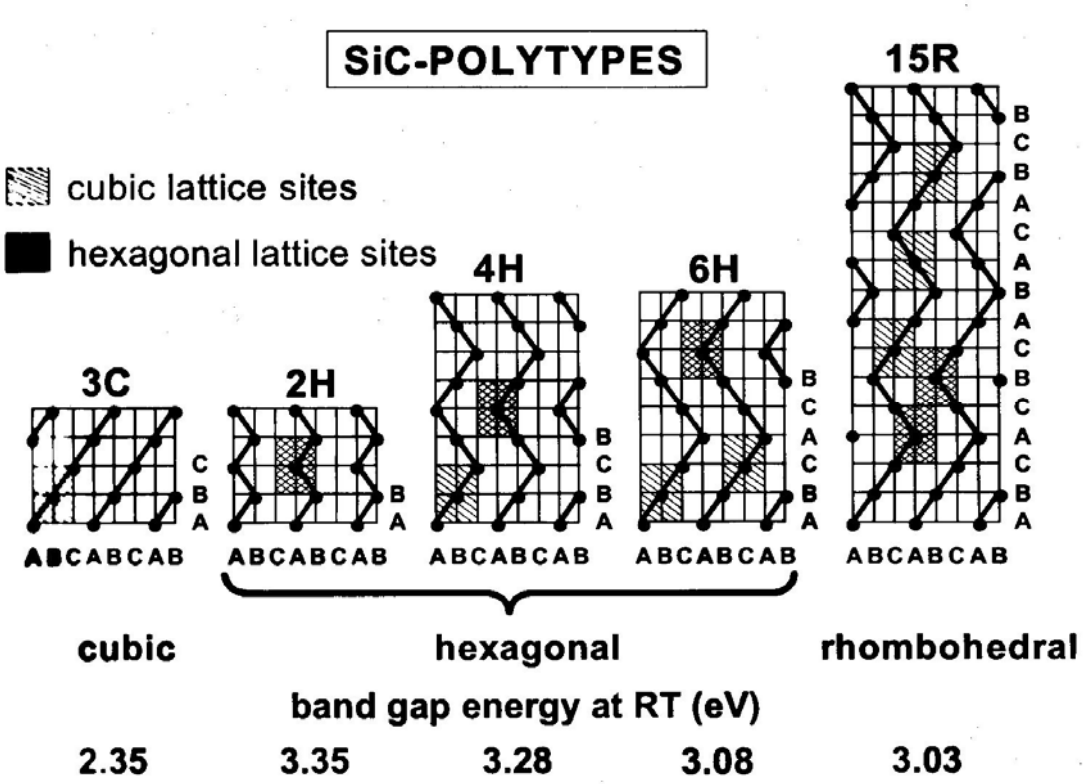


Fig. 2.2: The crystallographic structure of some common SiC polytypes, 2H, 3C, 4H, and 6H. [42]

	Si	GaAs	3C-SiC	6H-SiC	4H-SiC	2H-GaN	Diamond
Lattice Constant *a* [Å]	5.43	5.65	4.36	3.08	3.08	3.189	3.567
Lattice Constant *c* [Å]	n.a.	n.a.	n.a.	15.12	10.08	5.185	n.a.
Bond length [Å]	2.35	2.45	1.89	1.89	1.89	1.95	1.54
CTE [10^{-6}/K]	2.6	5.73	3.0	4.5		5.6	0.8
Density [g/cm^3]	2.3	5.3	3.2	3.2	3.2	6.1	3.5
Thermal Conductivity λ [W/cm K]	1.5	0.5	5.0	5.0	5.0	1.3	20.0
Melting point	1420	1240	2830	2830	2830	2500	4000
Mohs hardness			9.0	9.0	9.0		10.0

Table 2.1: The physical properties of three most commonly used polytypes of SiC and other semiconductor materials [20].

2.2.2 Physical and Electrical Properties of SiC

Shown in Table 2.1 are the physical properties of three most commonly studied polytypes of SiC and other semiconductor materials such as Si, GaAs and GaN [20]. The apparent anisotropic properties in different SiC polytypes are due to the stacked double layers of hexagonal polytypes. Owing to the different arrangements of Si and C atoms within the SiC crystal lattice, each SiC polytype exhibits unique properties. From Table 2.1, it is clear that SiC has excellent mechanical properties, which are second only to 2H-GaN and Diamond. For example, SiC has a shorter bond length, which renders it an excellent chemical stability and makes it capable to withstand harsh, corrosive and irradiative environments. SiC also has a very high thermal conductivity, which is only next to diamond, making it highly suitable for high power devices. SiC has a lattice constant "*a*" that closely matches that of 2H-GaN and their coefficients of thermal expansion (CTE) are close enough so that SiC can be used as a reliable substrate for epitaxial growth of GaN. However, due to its very high hardness

	Si	GaAs	3C-SiC	6H-SiC	4H-SiC	2H-GaN	Diamond
E_g [eV]	1.12	1.43	2.4	3.0	3.2	3.4	5.5
E_c [MV/cm]	0.25	0.3	2.0	2.5	2.2	3.0	5.0
V_{sat} [10^7cm/s]	1.0	1.0	2.5	2.0	2.0	2.5	2.7
$\mu_{n.\perp c}$ [cm^2/V s]	1350	8500	1000	500	950	400	2200
$\mu_{n.\parallel c}$ [cm^2/V s]	n.a.	n.a.	n.a.	100	1150	n.a.	n.a.
μ_P [cm^2/V s]	480	400	40	80	120	30	1600
ε_r	11.9	13.0	9.7	10.0	10.0	9.5	5.0

Table 2.2: The electrical properties of three most commonly used polytypes of SiC and other semiconductor materials [23].

and melt point (which are only second to diamond), together with its extraordinary chemical inertness, SiC has proved to be a technical challenge in its processing, including fabricating high quality SiC wafers, wafer polishing, ion implantation, etching.

The electrical properties of these semiconductor materials are shown in Table 2.2 [20]. The different arrangements of Si and C atoms within the SiC crystal lattice give each SiC polytype its unique electrical and optical properties. Even for a given polytype, some important electrical properties, such as carrier mobility, are anisotropic, i.e. they are strong functions of the crystallographic direction. In comparison with other materials, it is clear that SiC has several merits enable it to operate at extremely high temperatures, at high frequencies and to sustain high breakdown voltages with very low specific on-resistance. These merits include band gap, critical electric field and saturation velocity, whose values are only second to those of 2H-GaN and diamond. Compared to 2H-GaN, SiC has its own merit of being capable to form its own native oxide which can provide SiC devices with high quality gate dielectrics and passivation. Compared with 6H-SiC, 4H-SiC exhibits a higher bandgap, higher

mobility with minimum anisotropy, higher saturation electron velocity, comparable breakdown field strength, and comparable thermal conductivity. This makes 4H-SiC currently the best candidate for the fabrication of SiC high power microwave devices.

2.3 Plasma Etching

2.3.1 Fundamentals of Plasma

Plasma is considered as the fourth state of matter, apart from solid, liquid, and gaseous states. In general, plasma is defined as a collection of quasi-neutral discharged gas that exhibits certain collective behaviors [43]. Such discharged gases usually contain electrons, positive and negative charged ions, neutral atoms, molecules, and molecular fragments. From the general definition of plasma, it is clear that plasma has two important properties: the quasi-neutrality and collective motion. The generation and sustainment of plasma need external excitation power sources, such as thermal sources, electric sources, and irradiation sources.

In general, based on the degree of ionization (β), defined as the ratio of the electron density against the gas molecular density before discharge, plasma can be grouped as fully ionized plasma ($\beta = 1$), strongly ionized plasma ($\beta \geq 10^{-2}$), and weakly ionized plasma ($\beta \leq 10^{-3}$) [44]. On the other hand, from the status of thermodynamic equilibrium between different particles within plasma, plasma can also be categorized as thermal plasma when local thermodynamic equilibrium is achieved between particles of electrons, ions, and neutral particles, usually at high pressure, e.g., atmospheric pressure; and cold plasma when plasma system is under thermally nonequilibrium status, usually taking place in at low pressure. Due to the existence of the very chemically active neural radicals, cold plasmas, also been frequently referred

to as glow discharge, are widely applied in the semiconductor processes, especially plasma etching. Hence, we will focus on discussing on glow discharge, i.e., the cold plasma.

2.3.1.1 Properties and Characterization of Glow Discharge

Glow discharge is a low-pressure, low degree of ionization (low plasma density) plasma state of non-local-thermodynamic-equilibrium [45]. This thermal nonequilibrium manipulates itself as the particles, i.e. the electrons, ions, and neutral particles, are significantly different in their kinetic energies, or their temperatures. Usually, the electron temperature in the glow discharge is much higher than the temperatures of ions and neutral particles.

As a state of matter consisting of neutral particles, electrons and ions of nearly equal numbers of opposite charges, glow discharge has several unique properties, compared with the other states of matter [45].

Firstly, one of the most important properties of plasmas is quasineutrality. The generation and elimination of negative charges (electrons and negative ions) are companied with the generation and elimination of positive charges (positive ions) of almost equal amount. Due to the strong Coulomb force between electrons and positive ions, they are distributed in such a way that the quasineutrality is maintained within a very small local volume. This does result in an almost space charge free inside plasmas. Similar to conductive metals, plasma tends to shield the external/internal electric field to maintain the neutrality through redistributing of electrons and ions. This phenomenon is known as Debye shielding. The shielding occurs in a distance called the Debye length.

Secondly, due to being subjected to the constantly impacts from the intimate and remote electric and magnetic fields of other particles, all the charged particles moving within the plasma are affected by the electric and magnetic fields from other charged particles such that their kinematics are termed as collective motion. Such kind of effects have far more important impacts on the charged particles compared to the individual hard collisions normally happen within normal idea neutral gases, plasmas are vocationally being referred as collisionless. One of the examples of the collective motion is plasma oscillation.

Thirdly, plasmas can form a positively charged space charge layer at the interface of plasma and any solid surface, e.g., the wall of metal containment vessel and various solid dielectric materials. This space charge layer is referred as plasma sheath. Usually, plasma sheath is about a few Debye lengths thick. The forming of plasma sheath is due to the fact that electrons have a faster diffusion rate compared with ions. This results in an accumulated negatively charged solid surface and an internal electric field that repulses electrons inside the plasma from closing to the surface while attracts positively charged ions to impinge into the solid's surface. To shield this electric field, a layer of positively charged space charge layer is formed, referred as positive ion sheath. Through controlling the energy of impinging positive ions, this positive ion sheath plays a critical role in introducing positive ion bombardment in ion enhanced plasma etching.

Due to that the behaviors of plasmas are the collective behaviors of a large amount of electrons, ions, and neutral particles, these collective behaviors are usually being quantitatively measured with a few plasma parameters. Typical parameters

include plasma temperature, plasma density, degree of ionization, Debye length, and plasma frequency [45].

Firstly, the plasma temperature measured in Kelvins is an informal measure of the thermal kinetic energies of electrons, ions, and neutral particles of plasma. In the conventional glow discharge used for semiconductor plasma etching processes, electrons have a much higher temperature compared with ions and neutral particles, typically several thousand degrees Celsius. While the temperatures of ions and neutral particles are normally very close to ambient temperature. Plasma temperature, especially the electron temperature determines the degree ionization β.

Secondly, the plasma density is another parameter to characterize the properties of plasmas. Plasma density is conventionally referred as the electron density, defined as the number of free electrons per unit volume. A highly related parameter is the degree of ionization β, with its definition was introduced earlier in the subsection 2.3.1. Normally, a high plasma density is much desirable in enhancing the efficiency and rate of plasma etching processes. To achieve high density plasma (HDP), with the help of microwave excitation power, magnetic field, various plasma techniques have been developed, including inductively coupled plasma (ICP), electron cyclotron resonance (ECR) plasma, and helicon plasma.

Thirdly, it is already pointed out that the depths of plasma shielding and positive ion sheath are representing the depth of plasma that an external/internal electric field can penetrate into plasmas. This depth is usually being measured by Debye length λ_D [45]:

$$\lambda_D = \sqrt{\frac{k_B T_e}{4\pi n_e q^2}} \tag{2.1}$$

where k_B, T_e, n_e, and q are Boltzmann constant, electron temperature, electron density, and elementary charge, respectively. From above equation, it is clear that the Debye length is determined by the temperature and density of electron.

Fourthly, the parameter plasma frequency is related to plasma oscillation. When some electrons displace a tiny distance with respect to positive ions, a strong electric produced from this displacement will force these electrons to restore to their balanced positions. The resulting restoring Coulomb force causes the plasma electrons to oscillate internally at a frequency which is referred as plasma frequency.

2.3.1.2 Glow Discharge Reactor

The conventional glow discharge reactor applied in plasma etching process uses an alternating current (A.C.) external excitation power source to generate glow discharge. The benefits coming with using an A.C. external excitation power source are twofold. Firstly, electrodes of glow discharge reactor do not need to be conductive; and secondly, electrons can absorb sufficient energy during field oscillation to introduce more ionization by electron-neutral particle collisions such that plasma can be generated at low pressure, e.g., 1 mTorr. The glow discharge reactors used in plasma etching process include capacitively coupled plasma (CCP), ICP, ECR plasma, helicon plasma. In the following subsection, we will discuss the conventional CCP and ECR plasma that have been used in this work.

1. Capacitively Coupled Plasma Reactor

A standard capacitively coupled plasma reactor for reactive ion etching (RIE) is composed of a parallel plate capacitor with the lower electrode plate (the sample stage) driven by a 13.56 MHz radio frequency (R.F.) power supply through an impedance

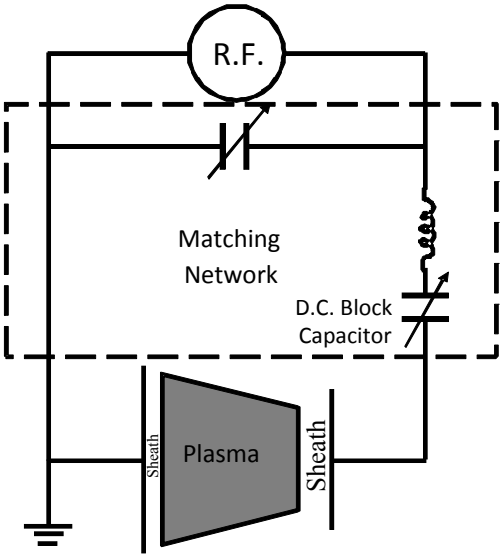


Fig. 2.3: The schematic diagram of capacitively coupled plasma reactor [46].

matching network and coupled with a blocking capacitor. A schematic diagram is shown in Fig. 2.3 [46].

The generation of glow discharge starts from the ionization of low pressure gases under high external electric field. The precursors of igniting of glow discharge are the electrons generated from random sources such as photoionization or field emission. Under external electric field, these precursor electrons are accelerated to gain enough energy to ionize the neutral molecular in the following collisions. These collisions produce ions, excited neutral particles, neutral molecular fragments, more electrons [46]:

$$\begin{aligned} \text{Dissociative attachment:} \quad & e + AB \rightarrow A^- + B^+ + e \\ \text{Dissociation:} \quad & e + AB \rightarrow e + A + B \\ \text{Ionization:} \quad & e + A \rightarrow A^+ + 2e \end{aligned} \tag{2.2}$$

Besides, electrons are generated through secondary electron emission, i.e., electrons being generated at the cathode electrode by impact ionization of energetic positive ions. This mechanism of generation of electrons becomes dominant when the process pressure is less than 300 mTorr [44]. On the other hand, these produced charged particles from collisions are neutralized through recombination of particles to release photons through photoemission, or to be neutralized by the electrodes and walls of the containment vessel [45]:

$$\begin{aligned} \text{Ion-ion recombination:} \quad & A^- + B^+ \rightarrow A + B \\ \text{Electron-ion recombination:} \quad & e^- + A^+ \rightarrow A \end{aligned} \tag{2.3}$$

The plasma is self-sustaining once a balance is established between the generation and neutralization of charged particles.

In a CCP reactor, once a sustaining plasma is built-up, under R.F. excitation, plasma sheaths are developed at the surfaces of both grounded and R.F. power driven electrodes, refer to as the anode and cathode, respectively. The negative potentials of the two electrodes corresponding to the plasma potential are asymmetrical and related to the area of the electrodes. By treating these sheaths as capacitors and assuming the current density of the positive ions across sheaths is uniform and is equal at both electrodes, a relationship between the negative potential and the electrode area can be approximately established [45]:

$$\frac{V_C}{V_A} = \left(\frac{A_A}{A_C} \right)^4 \tag{2.4}$$

where V_A, A_A, are the negative potentials corresponding to the plasma potential and areas of the anode, respectively, and V_C, and A_C are corresponding parameters to the

cathode. It is clearly seen that the negative potential of sheath has a reverse relationship with the area of the corresponding electrode. Usually, the anode is grounded and its area (A_A) includes the anode area and the area of the grounded wall of the containment vessel and is much larger than the area of cathode. This translates into a much higher negative potential being developed at the cathode, i.e., the R.F. power driven electrode.

For the cathode, due to the blocking effect of the connected blocking capacitor, the negative charges accumulated on the electrode at each electric cycle are preserved. This results in a constant negative potential, which is normally referred to as the D.C. self-bias. In a CCP reactor, the value of the D.C. self-bias is dependent on the plasma density which in turn is determined by the R.F. power and process pressure. Hence the D.C. self-bias is proportional to the R.F. power and inverse of the process pressure as follows [43]:

$$V_{D.C.\,Self\text{-}Bias} \propto \sqrt{\frac{W_{R.F.}}{P}} \tag{2.5}$$

where $V_{D.C.\ Self\text{-}Bias}$, $W_{R.F.}$, and P are the D.C. self-bias, R.F. power, and process pressure, respectively.

2. Electron Cyclotron Resonance Plasma Reactor

Electron cyclotron resonance (ECR) plasma reactor is an electrodeless HDP reactor. In a conventional configuration, an ECR is composed of a microwave power supply, an excitation chamber which is surrounded by one or more static magnets, and a process chamber. For etching process and thin film deposition, ECR plasma reactor usually works under low process pressure.

The basic mechanism of an ECR plasma reactor is the ECR effect. In a static and uniform magnetic field, a moving electron will be subjected to the Lorentz force and to circulate around the magnetic field lines in circular or helix obits with a characteristic cyclotron angular frequency ω_{ce} and the gyro-radius R, i.e. the radius of the circular orbit [47]:

$$\omega_{ce} = \frac{qB}{m_e}$$
$$R = \frac{2\pi v_e}{\omega_{ce}} \tag{2.6}$$

where q, B, and m_e are the electron charge, magnetic field, and electron mass, respectively, and v_e is the velocity of the electron. In the presence of an electric field, the electron is accelerated with an increased velocity perpendicular to the static magnetic field resulting in an outward, spiraling motion along a magnetic field line. When the electric field is applied from an external microwave excitation power source with its angular frequency ω equals to the characteristic cyclotron angular frequency ω_{ce}, the electron's spiral motion is in phase with the alternating electric field and results in it to be resonantly accelerated with each change in polarity. This is called electron cyclotron resonance effect where the microwave energy is coupled to the natural resonant frequency of the electron gas in the presence of a static magnetic field [47]. This translates into a very high energy of the cyclotron electrons which results in a high degree of dissociation and ionization of plasmas (10^{-2} for ECR compared to 10^{-6} for RIE) [48] through a series collisions of resonance electrons and neutral particles. The conditions of the excitation microwave power and the static magnetic field that meet the characteristic cyclotron angular frequency of Eqn. (2.6) and plasmas being

generated under these conditions are referred to as ECR conditions and ECR plasmas, respectively.

In reality, the external excitation microwave power source usually uses the industrial microwave frequency of 2.45 GHz and is transmitted to the feed-in gases in the excitation using a waveguide, or a resonance cavity, or a coaxial applicator, and is coupled to the feed-in gases through a microwave transparent quartz or alumina window [47]. With the 2.45 GHz external source, the ECR condition is met when applying a static magnetic field of 875 gauss [48]. During the ECR heating of electrons, it is desirable to be "collisionless". Such collisions between cyclotron electrons and neutral particles can cause energy lost and randomization of electron motion directions. In practice, this requirement is to be satisfied by keeping the process pressure under 20 mTorr [47].

Due to the fact that the magnetic field supplied from magnetic coils decreases with the distance from the coils, ECR accelerated electrons are pushed out of the high magnetic field region to the process chamber under a longitudinal force due to the diverging magnetic field. This results in a negative potential in the direction of the wafer under which positive ions diffuse out of the excitation chamber to the process chamber through ambipolar diffusion.

Due to the configuration of ECR plasma reactor being essentially electrodeless [47], the sample stage can be biased independently by connecting to an external R.F. or D.C power source [47]. This allows the independent control over the sheath potential and hence the desired etch anisotropy. It should be noted that both conventional CCP and ECR reactors use an R.F. power to generate self developed bias, i.e., the D.C. self-bias. However, for the conventional CCP reactor, the control of D.C.

self-bias is coupled to other parameters such as plasma density and process pressure. In contrast, in an ECR reactor, the control of D.C. self-bias is by the R.F. power alone and decoupled from other parameters. To distinguish them in this thesis, the bias developed in an ECR plasma process is referred to as D.C. bias while that developed in a RIE process is referred to as D.C. self-bias.

2.3.2 Plasma Etching Mechanisms

The basic plasma etching mechanism involves both physical and chemical processes [23]. It is well known that a variety of species can be produced in a plasma discharge [49], e.g., charged particles (ions and electrons), photons, and neutral species (radicals). Based on these species, plasma etching can proceed via a combination of physical and chemical mechanisms. The dominant mechanism is determined by the volatility of the reaction by-products and the energy of the ionized species. In practice, this translates into choices regarding the feed gas (inert or reactive), the plasma pressure and the choice of connecting the sample biasing electrode either to the R.F. power source or to ground [23]. These conditions result in different plasma etching processes which can be grouped into four categories as illustrated in Fig. 2.4 [50]. The first process is sputtering, which is a purely physical removal of the material by energetic ions of the gas molecules. The second process is chemical reaction etching in which electrically neutral but chemically reactive atoms/molecules called radicals formed in the plasma react with the substrate material to produce volatile species. The third process is ion enhanced energetic etching where energetic ions chemically activate the surface by breaking strong chemical bonds and removing volatile etching products and thus enhances etching reactivity. The last process is ion-enhanced protective etching where ion bombardment removes inhibitor

layers from the surface of the substrate orthogonal to the ion flux, allowing chemical etching to proceed [50].

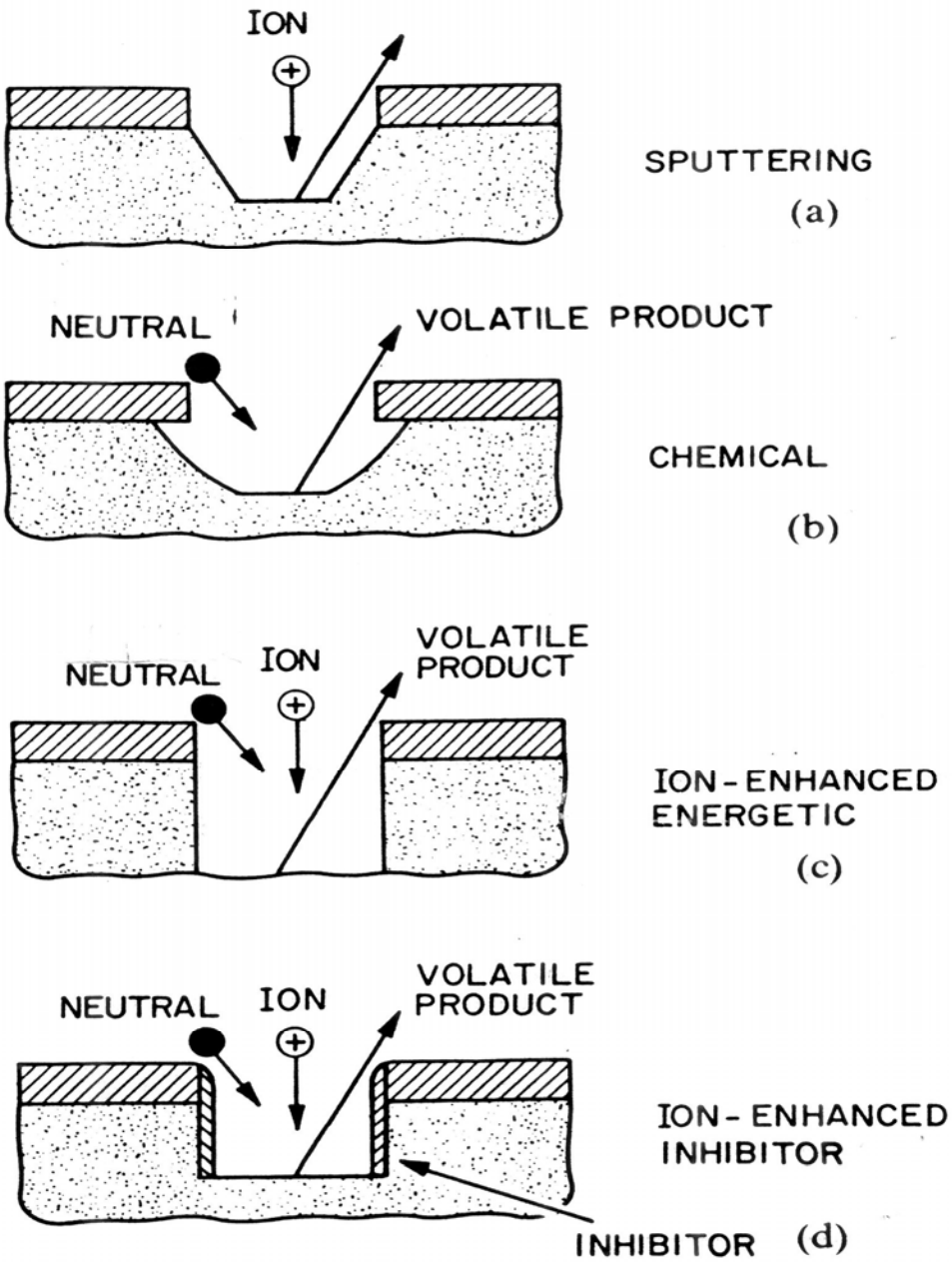


Fig. 2.4: The four basic plasma etching processes: (a) sputtering, (b) chemical reaction etching, (c) ion-enhanced energetic etching and (d) ion-enhanced protective etching [50].

Reactive ion etching (RIE), whose actions is predominantly based on the last two categories, operates at relatively low pressures (from few mTorr to hundreds of mTorr) with the sample placed on the R.F. powered cathode, thus resulting in the production of fairly energetic ions along with the formation of reactive radicals. Plasma-based etching in the RIE mode generally allows for the most useful trade-offs between etch rates and anisotropy [23].

2.4 Plasma Etching Technology for Silicon Carbide

There are several techniques available for etching SiC, including wet etching [2, 21], hot gases etching [51], amorphization etching [52, 53], photoelectrochemical etching [54-56], and plasma etching. Among them, plasma etching is the most extensively studied, and widely and successfully applied etching technique for SiC.

In the study of plasma etching of SiC, there are several issues that need to be addressed, i.e. etch rate, selectivity, uniformity, and surface quality. Due to its high chemical inertness, the task of achieving a controllable and predictable high etch rate in SiC is one of the most important. With the development of plasma etching technology, more new techniques have been developed to improve the etch rate, as summarized in Table 2.3. However, in order to achieve controllable and predictable etch rate, one needs to understand the etching mechanism. With the improved etch rate, other issues must also be considered, i.e. the selectivity, uniformity and surface quality, and addressing these issues remains a significant technical challenge. The progress of plasma etching techniques is summarized below.

Reactor	SiC	Gas	Condition at highest ER	ER(Å min^{-1})
RIE	6H	CHF_3/O_2	20sccm, 200W, 0%O_2	32
		SF_6/O_2		410
		CH_4/O_2		278
		NF_3/O_2		293
	3C	SF_6	150W, 80mtorr	700
	6H, 4H	NF_3	225mtorr, 95-110sccm, 275W	1500
ECR	6H	CF_4/O_2	5W, -100V, 17.5%O_2, 50sccm	800
	3C, 6H	CF_4/O_2	650W, -100V, 17%O_2, 50sccm	700
	6H	20 SF_6/10 Ar	750W, 250 R.F., 2mtorr, 30sccm	4500
	3C, 5H	SF_6/O_2	1200W, 1mtorr, 4sccm	2500
	6H	10 Cl_2/5 Ar	1000W, 150 R.F., 1.5mtorr, 15sccm	2500
		10 Cl_2/5 H_2	1000W, 150 R.F., 1.5mtorr, 15sccm	1000
		4 IBr/4 Ar	1000W, 250 R.F., 1.5mtorr, 15sccm	1100
		NF_3	800W, 100 R.F., 1mtorr, 10sccm	1600
		SF_6	800W, 100 R.F., 1mtorr, 10sccm	450
ICP	6H	Cl_2Ar or/He	100 Cl_2, 750W, 250 R.F., 5mtorr	100
		Cl_2/Xe	13% Cl_2, 750W, 250 R.F., 5mtorr	260
		IBr/Ar	10% Ar, 750W, 250 R.F., 5mtorr	800
		ICl/Ar	66% Ar, 750W, 250 R.F., 5mtorr	250
	6H	NF_3/O_2 or Ar	100% NF_3, 750W, 250 R.F., 5mtorr	4000
	4H	NH_3	100% NF_3, 500W, 50 R.F., 2mtorr	8000
	6H	SF_6	100% SF_6, 900W, -450V, 5mtorr	9700
Helicon Plasma	4H	30 SF_6/7/5O_2	25% O_2, 200W, -500V,.6 mtorr	13,500

Table 2.3: Published plasma etching data of SiC [21].

Generally, the plasma etching techniques being used in etching SiC can be divided into two categories, the conventional RIE and the high density plasma etching techniques, e.g., inductively coupled plasma (ICP), electron cyclotron resonance (ECR) plasma, helicon plasma, as shown in Table 2.3. High density plasma has several advantages over the conventional RIE, such as higher plasma density, decoupling of ion energy and ion flux, and low working pressure [21]. In addition, they usually offer higher etch rates and result in good surface quality. For example, by using SF_6 based magnetically enhanced ICP, D. W. Kim et al [57] demonstrated a very high etch rate of 1500 nm/min for 6H-SiC. Though the conventional RIE technique may not be as good as the high density plasma techniques in a number of aspects, it is still quite a

Etching Product	Boiling Points (°C)
$SiCl_4$	57.6
SiF_4	-86
CCl_4	76.8
CF_4	-128
CO_2	-78.5 (Sublimation)
CO	-181.5

Table 2.4: Boiling points of potential etch products in plasma etching of SiC using halogen gas plus oxygen plasma

widely used etching technique due to its simpler and reliable equipment setup and requirements.

The etchant gases used in etching SiC generally belong to two categories, the fluorine based etchant gases (e.g., CF_4, CHF_3, SF_6, NF_3.), and other halogen based etchant gases (e.g., Cl_2,IBr, ICl, ClF_4.) [58, 59]. The fluorine based etchant gases are normally preferred due to the fact that their plasma etching products have lower boiling points and are therefore more volatile, as shown in Table 2.4 [21]. Reactive ion etching of silicon carbide (SiC) using fluorinated gas and oxygen has been extensively studied [21, 23, 60, 61]. Although the detailed etching mechanism involved is still not yet fully understood, it is believed that both physical ion bombardment and chemical reactions are involved [23, 61, 62]. During plasma etching of SiC, the ions strike the substrate surface with sufficient energy to break the Si-C bond, and the chemical reactions most likely to be responsible for the removal of the Si and C atoms of SiC are listed below [23]:

$$Si + mF \rightarrow SiF_m \qquad m = 1 \sim 4, \tag{2.7}$$

$$C + mF \rightarrow CF_m \tag{2.8}$$

$$C + nO \rightarrow CO_n \qquad n = 1 \sim 2 \tag{2.9}$$

$$SiC + mF + nO \rightarrow SiF_m + CF_m + CO_n \tag{2.10}$$

It is generally agreed that F is the main etchant species reacting with Si and C atoms, either through pure chemical reactions, or ion assisted/enhanced chemical reactions or both, as shown in Eqs. (2.7) and (2.8) [23, 62]. After the incident ions have weakened or broken the Si-C bond, F atoms react preferentially with Si atoms. This results in the formation of a carbon-rich layer, and its removal is thought to be an etch rate limiting step [63]. The removal of this carbon-rich layer can occur through chemical reactions with F and/or O atoms, as indicated in Eqs. (2.8) and (2.9), assisted by ion bombardments, i.e., ion-enhanced energetic etching, and/or ion-enhanced protective etching [23], or through pure physical sputtering [21, 61, 62, 64]. The effect of oxygen on the RIE process of SiC is very complex and will be further discussed in detail in the next chapter when our 4H-SiC RIE results are presented.

The choice of mask material is crucial for any plasma etching process. Many materials have been chosen to act as masks in the etching of SiC, including Su8, Ti, Al, Ni, ITO [62, 63]. Studies have demonstrated that the crucial index of etch selectivity of SiC over mask changes with the etching conditions [62, 63]. For example, when the gas pressure was varied from 60 to 240 mTorr in a CHF_3/O_2 mixture RIE system, the etch selectivity of 4H-SiC over Ni mask was found to increase drastically from 5 to 34. [65] Other factors such as total gas flow rate, R.F. power, gas composition, can also influence the etch selectivity [65, 66]. Among all the above mentioned mask materials, Ni remains one of the most successful mask materials due to its very high selectivity [63]. However, a high stress exists at the Ni-SiC interface because of the large lattice mismatch between Ni and SiC and, additionally, the adhesion of Ni on SiC is in

general poor, especially for thick layers. This hinders the application of thick Ni masks. To solve this issue, in this work, we developed a dual-layer metal mask. By adding in a thin Ti layer between Ni and SiC, the adhesion ability of the Ni based mask has been greatly improved. This dual-layer mask has been widely used in this thesis.

2.5 Neural Network and Plasma Etching Process Modeling

Numerical modeling is very important for the plasma etching of SiC, as it can be used to study and understand the complex etching behavior under the interaction of several process parameters. Besides, it allows a precise control of the etching process because the etching control of SiC is very often based on the etch rate and etch time, instead of an etching resistive stop layer [23]. Furthermore, it can provide guidelines in the design of new etching recipes and help in verifying the experimental results. One of the most widely used numerical modeling techniques for plasma etching in the microelectronic industry is artificial neural network (ANN) modeling [67, 68].

ANN is propelled by the advance of computer science, especially the advance of larger scale parallel computing systems and artificial intelligence (AI). By connecting a vast amount of parallel and fully interconnected working units known as neurons, ANN can model any complex and unknown functions through “training”, by mimicking the behavior of human brain [69]. In the application of ANN for modeling of plasma etching process, the feed-forward neural network (FNN) under supervised training is the most suitable and has been widely used [67, 68]. In the training stage, the ANN gains knowledge by “learning”, which involves feeding known data, termed as “training sample”, to the ANN and adjusting the connection weights between neurons according to the training algorithms, to minimize the errors between the given

answers and the network outputs. A FNN with properly selected structure and suitable training algorithm can model the behaviors of the objectives by predicting the unknown behavior that does not exist in its training data with high accuracy, feasibility and robustness [70].

Most of the work reported on the modeling of plasma etching and related processes used FNNs trained by the conventional back-propagation (BP) algorithm [67, 68], referred to as BPNN. The details of the BP algorithm can be found in Chapter four. Despite some inherent weaknesses, e.g. the need for longer training time and more neurons and the issue of overfitting, the BPNN algorithm has achieved great success in the past. It has been widely used to model the plasma etching behavior of different materials, including silicon dioxide [71], polysilicon [72], SiC [73], and others [74]. For example, Y. L. Huang et al [75] has successfully used a three-layer BPNN to model the plasma etching polysilicon and demonstrated that by carefully adjusting the hidden neuron number, a reliable plasma etching model based on a limited training sample size can be achieved. Also, it was demonstrated by C. D. Himmel et al [72] that BPNN is superior to conventional statistical techniques, i.e. the response surface methodology (RSM), in the modeling of polysilicon plasma etching process. Besides being used for the modeling of plasma etching behaviors of different materials, the BPNN has been successfully used in other aspects of plasma etching. For example, D. Stokes et al applied BPNN to construct a predictive model, to control in real time the etch rate and D.C. bias in the RIE etching of a GaAs/AlGaAs metal-semiconductor-metal structure through an indirect adaptive control strategy [76]. B. Kim et al used it to study plasma induced charge damage on MOS devices [77], and model actinometry-based optical emission spectroscopy data for plasma etch process prediction [78].

It has been clearly established that BPNN plays a very important role in modeling plasma etching processes. However, despite its remarkable success, it still has a few important drawbacks, such as long training time, more neurons, overfitting. In this thesis, we have proposed and developed a more advanced training algorithm, the Broyden, Fletcher, Goldfarb, and Shanno (BFGS) algorithm, for the modeling of plasma etching of 4H-SiC [25]. A detailed comparison of the BPNN and BFGS algorithms, and the modeling results for the plasma etching of 4H-SiC using the BFGS algorithm will be presented in Chapter four and five respectively. Compared with the BP algorithm used in a BPNN, the BFGS algorithm is a more advanced quadratic quasi-Newton algorithm. By utilizing a special designed rank-two correction method and an inexact line search scheme, BFGS algorithm has been demonstrated to have a much better convergence property which translates to a fast training time, less neuron number required, and a better immunity to overfitting.

2.6 Plasma Etching Induced Damage

The physical and chemical reactions involved in the plasma etching of SiC will inevitably induce damage on the surface of the etched samples. Several kinds of surface damage have been reported [23, 79], which include surface roughening, surface contamination by RIE residues, and lattice defects either at the surface or underneath it caused by physical ion bombardments. These defects can degrade the electrical characteristics of SiC devices and are undesirable. For example, the Schottky barrier height and breakdown voltage of 4H-SiC Schottky barrier diodes were noted to decrease arising from defects originated from enhance physical sputtering in an ICP-RIE process when a large D.C. self bias was applied [21]. Similarly, Koo et al [80] reported that the effective interface state density and fixed oxide charges of ICP etched

MOS capacitor samples increased by 34% and 49% respectively for 4H-SiC NMOS capacitors and 4% and 125% respectively for 6H-SiC PMOS capacitors when compared with those of the control samples that were not etched. These origins of the physical defects which account for the degraded electrical characteristics have yet to be determined. It was reported that oxidation of ICP plasma etched 4H-SiC at 900 to 1250ºC can alleviate the damage done to the etched surface and improve its electrical characteristics, while annealing in N_2 at 1050ºC has no effect [81].

Many researchers have reported that fluorine based plasma etching processes can lead to etched surfaces that are rough. By using Auger electron spectroscopy (AES), it has been shown that aluminum is present on the etched surface [82]. It is generally believed that the Al residue is due to redeposition of sputtered Al from the Al mask used, the Al electrodes of the plasma chamber, and/or even from the wall of chamber onto the etched surface. These Al clusters can render the etched surface rough during the etching process by the micromasking effect [21, 82]. The introduction of hydrogen into the plasma can inhibit the deposition of Al residues by forming volatile alane (AlH_3) [21]. It was reported [82] that an addition of 10 percent of H_2 into the plasma can completely remove the Al residues and prevent the micromasking effect. It was also found [65] that increasing the oxygen concentration (40%) in a CHF_3/O_2 RIE process can improve the surface quality by smoothing the surface and removing residues. As the role of oxygen in the plasma etching of SiC is still unclear [21, 23, 62], the mechanism by which an oxygen-rich plasma smooth etched SiC surfaces remains to be confirmed. The etching induced surface roughness of SiC was also studied for high density plasma, such as ICP [83] where it was found that the surface roughness has an inverse relation with the D.C. bias and is strongly dependent on the etchant gas

used. AES studies of etched SiC surfaces have also revealed the presence of other residues such as F and O [84].

2.7 Summary

In summary, in this chapter, we first presented some basic information of SiC, including its crystallographic structures for different polytypes, its physical and electronic properties. Then we presented the basic information on the plasma etching. After introducing the basic information, we presented a literature review. In this literature review, we firstly discussed and summarized the plasma etching techniques used for etching SiC, its chemical reactions, the selection of etchant gases and mask materials. Secondly, we introduced the numerical modeling of plasma etching based on artificial neural network, especially the application of feed-forward neural network trained by the conventional back propagation algorithm and its application in modeling plasma etching process. Lastly, we discussed the plasma etching induced damage on SiC, including the study on the plasma etching induced micromasking effect, its damage on the electrical properties of Schottky barrier diodes and MOS capacitors.

Chapter 3

Reactive Ion Etching of Silicon Carbide

3.1 Introduction

Reactive ion etching (RIE) is one of the most widely used processes in SiC based microelectronic device fabrication. It offers several advantages, which include the ability to etch small features with precise control and high aspect ratio, to provide smooth and clean etched surfaces, reasonable etch rate, environmental friendliness, compatibility with standard CMOS manufacturing process. On the other hand, the RIE process also suffers from several disadvantages. For example, in gate or channel recess etching or mesa etching, plasma etching process need to be stopped at the interface of two SiC layers of different dopant type and/or different doping level. Due to poor selectivity between SiC layers of different doping types and/or levels, [23, 55], there is no native etch-stop layer, resulting in little etch depth control. This is quite different compared to for Si device fabrication processes where the devices are mainly built through implantation instead of epitaxially grown Si layers. In addition, RIE may lead to surface damage, which includes surface roughening, surface contamination, and crystalline structure damage. [23, 79]. Under certain condition, the surface damage may result in the so-called micromasking effect [82], while crystalline structure

damage may induce enhanced leakage current and noise for SiC devices fabricated, such as Schottky diodes and transistors. [85]

To precisely control the RIE process of SiC in terms of the etch rate and quality of the etched surface, it is crucial to understand its detailed mechanism and characteristics, and the damage it brings about. In this chapter, the RIE of 4H-SiC based on CHF_3+O_2 plasma is studied in terms of etch rate and etched surface roughness as functions of O_2 fraction, R.F. power and process pressure. Since a severe micromasking effect was observed in our RIE process, special attention has been dedicated to the study of this effect. The etching induced damage has also been studied on Schottky contact/diode and the results will be presented in Chapter six.

3.2 Experimental Setup

The samples used in this work are 5×5 mm^2 bulk 4H-SiC, *n*-doped (N_d = 6.9×10^{18} cm^{-3}), 8º off-axis toward the $\langle 11\bar{2}0\rangle$ orientation, and with Si-terminated face, purchased from CREE Research Inc. The samples were first cleaned in acetone, followed by rinsing in isopropyl alcohol (IPA) and in a deionized water ultrasonic bath for a duration of 5 minutes each. After cleaning, the samples were blown dry with N_2 gas and dried in oven at 110°C for 30 minutes. To withstand the harsh RIE environment, a dual-layer metal mask consisting of 30 nm Ti followed by 300 nm Ni has been selected. The metal layers were deposited by electron beam evaporation. The patterning of the metal mask was carried out using a standard lift-off process.

The RIE tests were performed using a CHF_3+O_2 plasma, with CHF_3 as the reactive fluorinated gas and O_2 as the additive. A standard R.F. powered and capacitively coupled parallel plate plasma reactor was used for the RIE. The schematic

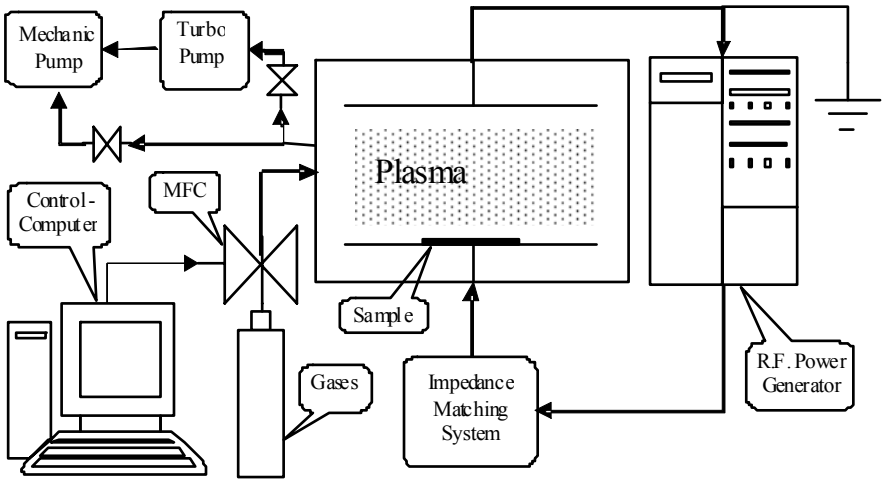


Fig. 3.1: The schematic diagram of the RIE system used in this work.

diagram of the plasma reactor is shown in Fig. 3.1. The electrodes of the reactor are made of Al with a diameter of 15 cm. The spacing between the upper and lower electrodes is 4.5 cm. The lower electrode is driven by a 13.56 MHz R.F. power source while the upper electrode is grounded.

The characterization of the morphology of the etched pattern was carried out using a LEO 982 scanning electron microscope (SEM). The etch depth was measured with a Dektak3 ST stylus surface profilometer. The etched surface roughness was characterized using a Shimadzu SPM-9500J2 atomic force microscope (AFM), and the surface element analysis was performed by a JEOL JAMP 7800F Auger electron spectrometer (AES).

3.3 Selection of Mask

The selection of mask is essential for high-quality pattern transfer in SiC microelectronic devices and MEMS fabrication, as such masks are required to withstand the harsh corrosive RIE environment and survive a long etching duration. Hence, the mask material must be hard enough and at the same time it should have a reasonably high etch rate selectivity over SiC as well as a good adhesion to SiC, without introducing or contributing with any contamination. Conventional mask material candidates for plasma etching include photoresist (PR), SiO_x, SiN_x, Al, Ni, Cr, Indium-Tin-Oxide (ITO) [62, 63]. Among them, Ni has gained great success as a hard mask material due to its hardness, reasonably high selectivity and minimum contamination [86]. However, it also has some drawbacks such as leading to high strain at the SiC-Ni interface attributed to lattice mismatch and variable selectivity under different etching conditions [65, 66].

In this work, Ni was used as the main mask material. Based on Ni, two mask structures, namely, a single Ni (100 nm) metal mask, and a dual-layer metal mask composed of 30 nm Ti + 300 nm Ni, were developed. A general purpose positive photoresist AZ1518™ (~ 1.5 μm) mask was also used to serve as comparison. The metal masks (Ni and Ti + Ni) were fabricated by electron beam evaporation, followed a standard lift-off process. The AZ1518™ positive photoresist mask was fabricated by using a standard photolithography process.

Mask	Thickness	Result
Photoresist (Az 1518)	~ 1.5 μm	Failed
Ni	100 nm	Failed
Ti + Ni	Ti: 30 nm Ni: 300 nm	Good

Table 3.1: The RIE test for selection of masks.

A special RIE test that gives rise to the highest Ni etch rate was designed to study the suitability and durability of the various masks proposed. The conditions are as follows: the flow rates of CHF_3 and O_2 were set at 10 sccm and 2 sccm, respectively, the process pressure was fixed at 90 mTorr and the R.F. power at 200 W. Under these conditions, a large D.C. self-bias of about –340 V was developed at the substrate. The test duration was set to be long, of about 100 min. The RIE test results are summarized in Table 3.1. In Table 3.1, "Failed" refers to the situation that the mask has been etched away during the etching process and "Good" means that the mask has survived the etching process. The remaining Ni in the dual-layer metal mask at the end of the etching process is about 100 nm thick compared to its initial thickness of 300 nm.

The results reveal that the conventional 1.5 μm thick AZ1518™ photoresist mask cannot survive the 100 min RIE test. The etch rate of AZ1518™ was found to be much higher than that of SiC, by about a factor of 10, consistent with previously reported results [86]. On the other hand, for the 100 nm thick single layer Ni mask, it still failed our demanding RIE test despite its hardness and high resistance to corrosive RIE environment. Although the dry etching selectivity of Ni over SiC may be as high as about 30 [86], the dry etching selectivity changes considerably under different etching conditions. For example, under certain circumstances such as high D.C. self-bias, the dry etching selectivity of Ni with respect to SiC may decrease to about 5 [65]. Therefore, for those applications that need deep etching, a thicker Ni mask layer is

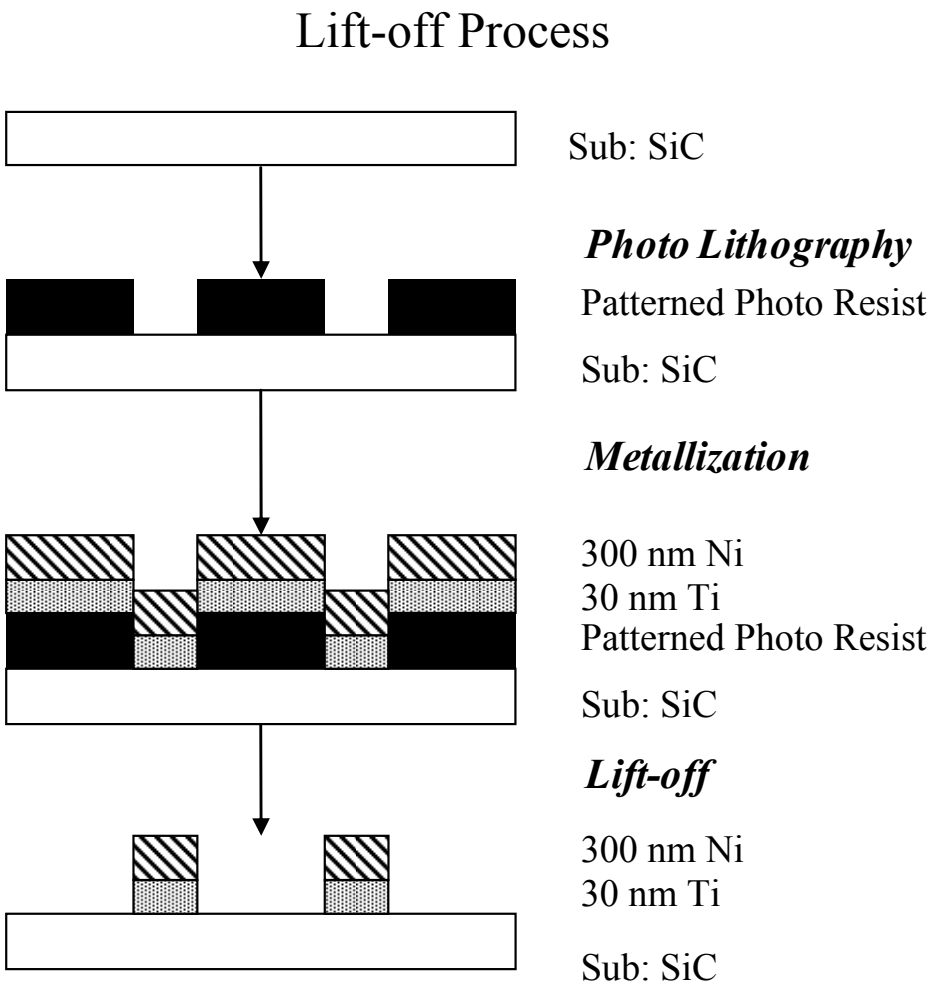


Fig. 3.2: The structure and the lift-off procedure for fabricating a Ti-Ni dual-layer structure metal mask.

required. However, due to a number of factors such as lattice mismatch between SiC and Ni, intrinsic internal stress and mismatch in the thermal expansion coefficients, a thicker Ni layer will lead to a high strain being developed at the SiC-Ni interface, rendering Ni layers thicker than 150 nm prone to peel off [86]. In this regard, adding an interfacial layer, such as a thin Ti layer, which has a much better adhesion to SiC, will relieve the interfacial strain and considerably improve the adhesion between the thick Ni mask and the SiC substrate. In our study, the use of a Ti (30 nm) + Ni (300

nm) dual-layer metal mask has successfully passed the RIE test. Another advantage of using such a mask structure is that the mask can be easily and completely removed after the RIE process by immersing it into a diluted HF solution. The structure and the fabrication procedure are shown in Fig. 3.2. Unless otherwise mentioned, this mask structure has been employed for the rest of the etching experiments in this project.

3.4 Results and Discussion

In the following, the RIE etching of 4H-SiC is studied in terms of the etch rate and r.m.s. surface roughness, as a function of the oxygen fraction, R.F. power and process pressure. The etched surface was analyzed with Auger electron spectroscopy (AES) and scanning electron microscopy (SEM). The formation of a carbon rich layer at the top surface and the micromasking effect will also be investigated.

3.4.1 The Effect of the Oxygen Fraction

In this test, RIE of 4H-SiC was studied with varying oxygen fraction, defined as the ratio of the O_2 flow rate to the total gas flow rate (CHF_3+O_2), from 0 to 80%. The other process parameters, i.e. R.F. power, process pressure, total gas flow rate, and process duration, were fixed at 200 W (1.13 W/cm^2), 100 mTorr, 10 sccm, and 60 minutes, respectively.

Fig. 3.3 shows the etch rate versus the O_2 fraction. The etch rates obtained are repeatable within the experimental error limits that are indicated in the figure. As can be seen, the etch rate increases initially with increasing O_2 fraction, and peaks at an O_2 fraction of 20%. Beyond that, it decreases sharply and is nearly zero at around 80% O_2 fraction. The optimum O_2 fraction of 20% gives rise to a maximum etch rate of 35.6 nm/min. This initial increase in the etch rate is attributed to the enhanced dissociation

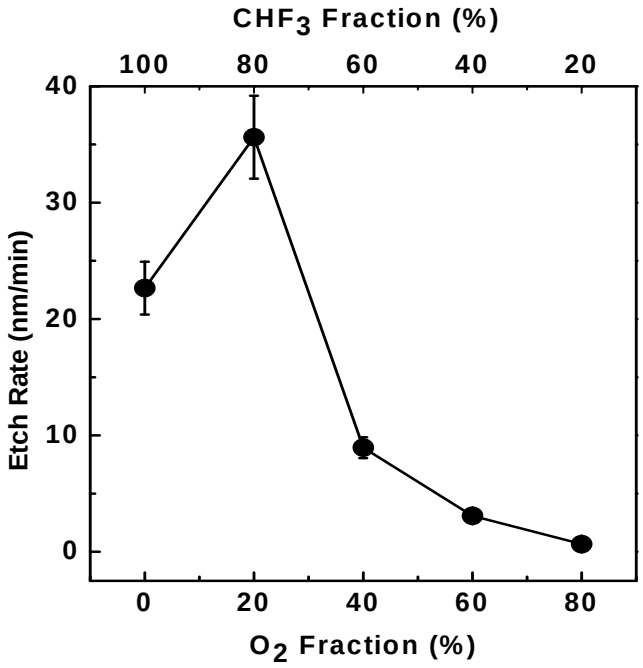


Fig. 3.3: The etch rate of SiC versus O_2 fraction.

of C-F bonds through reacting with oxygen atoms, resulting in an increase in the concentration of fluorine atoms that are responsible for the etching [87, 88]:

$$\left.\begin{matrix} O \\ O_2 \end{matrix}\right\} + CF_X \rightarrow \begin{cases} COF_2 \\ CO \\ CO_2 \end{cases} + F, F_2. \qquad (3.1)$$

As suggested by Eqn. (3.1), this enhancement is believed to be derived from two sources. Firstly, O atom reacts with unsaturated fluoride species (e.g. CF_x) to release more active F atoms. Secondly, O atoms inhibit F atoms and/or fluorocarbon species (e.g. CF_x) recombination and thus prevent the loss of F atoms.

The increase in the O_2 fraction from 20 to 40% results in a sharp decrease in the etch rate by about 75% from its maximum value of 35.6 nm/min to 8.9 nm/min. The

etch rate eventually drops to less than 1 nm/min with a further increase in O_2 fraction to 80%. Two plausible factors are believed to account for the sharp decrease in the etch rate observed at higher O_2 fraction. Firstly, the dilution of F concentration under high O_2 fractions will reduce the availability of F atoms, and result in slower etch rates, given that the total feed gas flow rate was kept constant. Secondly, under high O_2 fraction, there may be more O atoms adsorbing on the etched surface, making it more "oxide-like" (SiO_x). This oxide-like layer reduces the availability of Si and hence lowers the etch rate.

The fluorinated etchant gases and oxygen are also frequently used for the plasma etching of Si, such as SF_6/O_2, CF_4/O_2, CHF_3/O_2. Comparing the mechanisms of plasma etching of Si and SiC, there are similarities and differences between them. In terms of similarities, F atoms are the main etchant species in the etching of Si and SiC. In the case of plasma etching of Si, F atoms react with Si to form volatile SiF_m ($Si + mF \rightarrow SiF_m$, m = 1 – 4). In the case of plasma etching of SiC, likewise, F atoms play the main role in etching Si to form volatile SiF_m. In addition, F atoms are responsible for etching C ($C + mF \rightarrow CF_m$, m = 1 - 4). Similar to the plasma etching of SiC, the role of additive gas O_2 in the etching of Si is to regulate the F atom concentration. By reacting with fluorinated gas, it will help to release more F atoms to enhance the etch rate at low O_2 fraction. Whereas at high O_2 fraction, it will reduce the etch rate by diluting F atom concentration. In addition, at high O_2 fraction, O atoms can also be chemisorbed onto the Si surface to form an oxide-like layer to block the F atoms from reacting with Si underneath and result in a lower etch rate. Hence, for both plasma etching of Si and SiC, with increasing O_2 fraction, the etch rate will increase at low O_2 fraction and decrease at high O_2 fraction.

There are differences in the plasma etching of Si and SiC. For example, the role of O_2 in the plasma etching of Si is always indirect, i.e. O atoms do not react directly with Si to remove it. In contrast, in the plasma etching of SiC, O atoms are believed to react directly with C to form volatile CO_n ($C + nO \rightarrow CO_n$, $n = 1 - 2$), especially at high O_2 fraction. Another difference is the role of positive ion bombardment. In the plasma etching of Si, F atoms can quickly form a fluorinated skin (F atom adsorption) with a small portion of F atoms penetrating into the fluorinated layer to break subsurface Si-Si bonds and to free SiF_m molecules. In this case, positive ion bombardment serves only to remove the etching products and renders it anisotropic. Compared with Si, SiC has a stronger Si-C bonds and is more chemically inert. Hence, positive ion bombardments are usually required to break the strong Si-C bonds before F can react with Si and C atoms. In addition, the positive ion bombardment is believed to play a role in remove the C rich layer being form during the etching process when the C etch rate is lower than that of Si. In general, due to its chemical inertness, under the same plasma condition, the etch rate of SiC is about two orders of magnitude lower than that of Si.

It is worthy to note that the etch rate peak does not necessarily correspond to the point that F reaches it maximum concentration [88]. This is due to the existence of the oxide-like layer and the C rich layer that further complicate the process. The removal of the oxide-like layer is believed to be achieved through physical sputtering, while the removal of the C rich layer is more complicated, could be due to physical sputtering or plasma chemical etching with the assistance of ion bombardment, and is still under debate [62, 63, 89]. Hence, the etch rate is also determined by the D.C. self-bias and process pressure, apart from the F concentration. In this work, we have also

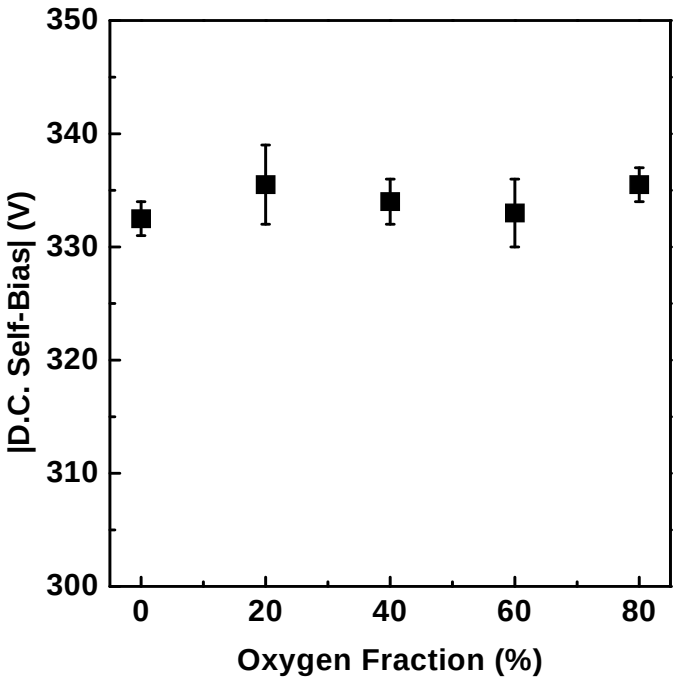
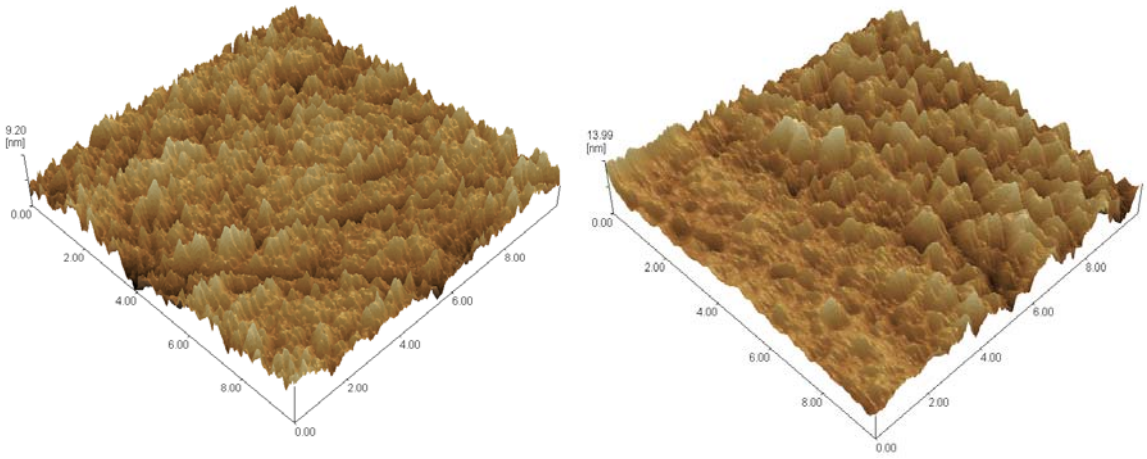


Fig. 3.4: The D.C. self-bias investigated as a function of the oxygen fraction.

investigated the effects of the D.C. self-bias and chamber pressure on the etch rate, and the results will be presented shortly in this chapter.

For the set of experiments with results reported in Fig. 3.3, we have also studied the influences of O_2 fraction on the D.C.self-bias, which is a very important parameter that controls the etch process. As can be seen in Fig. 3.4, the D.C. self-bias, which directly controls the energy of the impinging ions, remains nearly constant at –334 V ± 1.4 V with changing O_2 fraction. This is not surprising since the D.C. self-bias is mainly determined by the applied R.F. power and the process pressure, both of which were maintained constant in these experiments. The high D.C. self-bias developed provides stable and efficient high energetic ions in the plasma for physical ion bombardment. It is likely that the strong physical ion bombardment breaks the Si-C



(a) (b)

Fig. 3.5: The AFM images of the SiC surfaces of (a) unetched control sample (r.m.s. surface roughness is 1.23 nm) and (b) sample etched at 20% O_2 fraction (r.m.s. surface roughness is 1.65 nm).

bonds efficiently and leaves chemically activated Si atoms and/or C atoms to be etched by neutral species such as F and/or O atoms. In this set of experiments, since the D.C. self-bias does not vary much, the change in the etch rate at different O_2 fractions is mainly attributed to the different chemical reaction rates. As will be seen in other sets of experiments for the RIE of 4H-SiC using the same source gases under different R.F. powers and process pressures, a direct correlation between the etch rate and the D.C. self-bias has been observed [22].

Besides affecting the etch rate of 4H-SiC, changing the O_2 fraction has also been found to have an effect on the surface roughness. Fig. 3.5 shows the AFM images scanned over an area of 10×10 μm^2 of the unetched control SiC sample and the sample etched at 20% O_2 fraction. The root mean square (r.m.s.) surface roughness of all the samples is plotted as a function of the O_2 fraction in Fig. 3.6. The r.m.s. surface roughness of an unetched control sample of the same area is 1.23 nm. As can be seen from Fig. 3.6, with increasing O_2 fraction from 0 to 80%, there is an increase in the

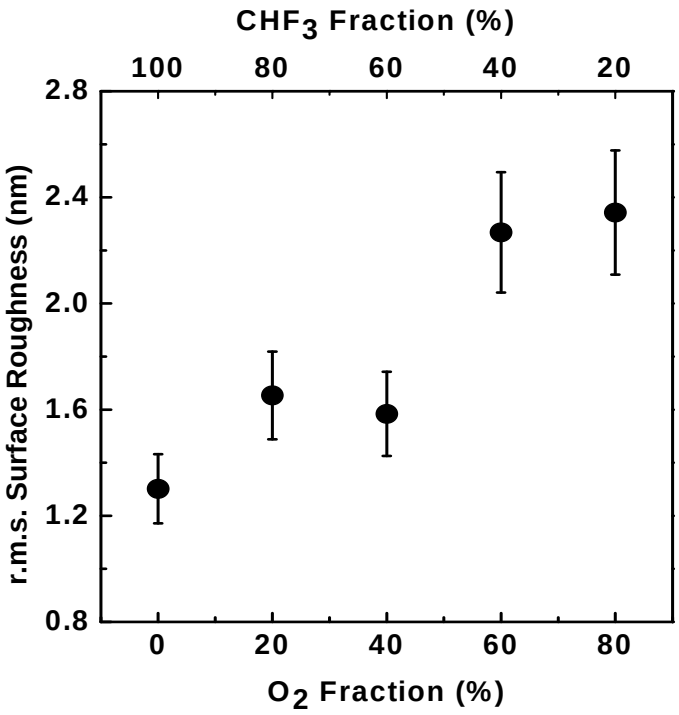


Fig. 3.6: The r.m.s. surface roughness of the etched surfaces versus O_2 fraction over a scanning area of 10 × 10 μm^2.

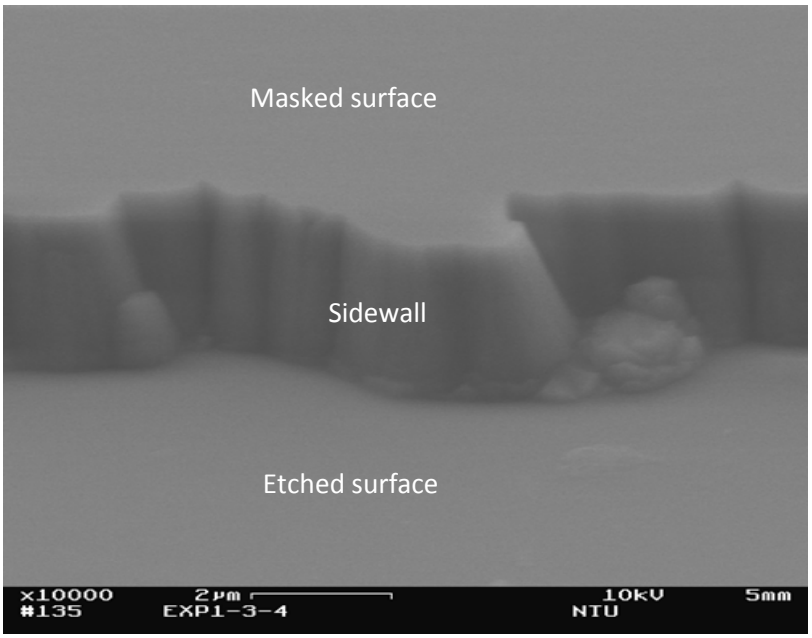


Fig. 3.7: SEM picture of the pattern etched using a 20% O_2 fraction.

r.m.s. surface roughness from 1.31 to 2.34 nm. There are several possible reasons that can account for the obtained roughness results. Firstly, the increase in the O_2 fraction results in a dilution of the concentration of F atoms, which are mainly responsible for the chemical reactions occurring in the RIE process. This therefore weakens the chemical etching and contributes to a rougher surface as it has been demonstrated that chemical reactions during the RIE process tend to smoothen the surface [90, 91]. Secondly, the formation of an oxide-like layer at the surface due to the surface oxidation at higher O_2 fraction and/or surface chemisorption, may also account for the rougher etched surface observed [91]. Indeed, the presence of an oxide-like layer in our samples has been confirmed by our AES results, and will be shown shortly.

From Fig. 3.3 and Fig. 3.6 it can be seen that, for O_2 fractions beyond 20%, the sharp decrease in the etch rate is accompanied by an increase in the surface roughness. Therefore, the optimum O_2 fraction that provides a large etch rate and yet minimum surface roughness still remains at 20%. Fig. 3.7 shows the SEM micrograph of the profile of the surface etched at the optimal etching condition. As can be seen, smooth and anisotropic etched surface profile has been obtained, with no obvious trenching effect that has been frequently observed in the plasma etching of SiC [92-94]. Similar SEM images have also been observed for samples etched at other O_2 fractions.

To further understand the properties of the etched surface, we have performed AES experiments on an unetched control sample and the sample etched at the optimum condition of 20% O_2 fraction, denoted as sample A and sample B respectively. The AES results are shown in Fig. 3.8. To make these results comparable, the relative sensitivity factors (RSFs) supplied by the equipment manufacturer were

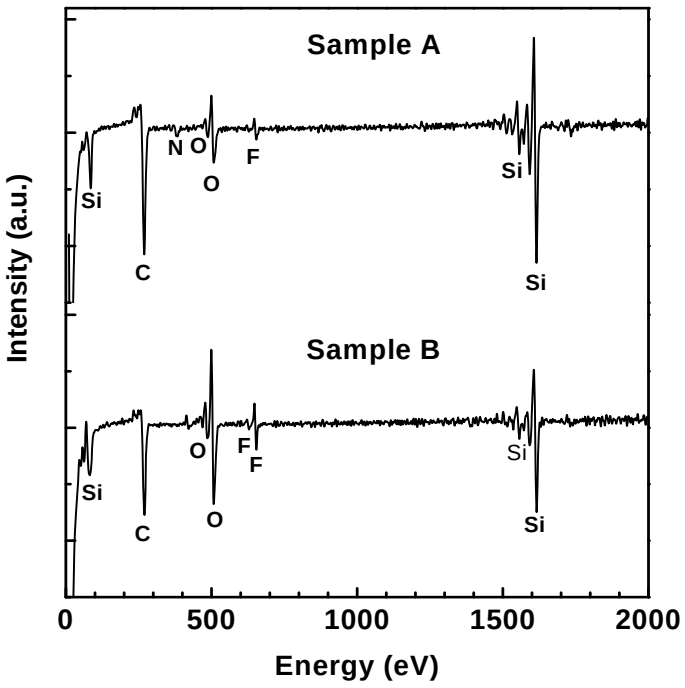


Fig. 3.8: The AES spectra of the unetched control sample A and the sample B etched at 20% O_2 fraction.

used to quantify the data. The relative concentrations of the different elements are shown in Table 3.2. In this thesis, all Auger spectra are quantified using relative sensitivity factors (RSFs) as supplied by JEOL Asia, the equipment manufacturer. This approach is semi-quantitative but is generally adequate for comparison purposes and all values are rounded to the nearest 1% so they may not add up to exactly 100%. The AES results reveal an increase in the residual oxygen upon etching. This shows that an oxide-like layer can be formed even at 20% O_2 fraction, possibly by surface oxidation or chemisorption. As stated before, this oxide-like layer can slow down the etch rate and may result in rougher surface for samples etched at even higher O_2 fraction. It is noted that a small amount of oxygen is also found in the unetched control sample, which could arise from a thin native surface oxide layer.

Element	C	N	O	F	Al	Si	Ni	Ti	C/Si Ratio
Relative sensitivity factor (RSF)	0.128	0.158	0.371	0.954	0.309	0.137	0.485	0.351	
Sample A	38	2	6	1	-	53	-	-	0.72
Sample B	35	-	17	2	-		-	2	0.80

Table 3.2: The relative concentration of elements (atom%) extracted from Fig. 3.8 of unetched control sample, denoted as sample A, and etched sample under 20% O_2 fraction plasma, denoted as sample B.

A C rich-layer, or C residue layer, formation is frequently observed and reported in the reactive ion etching of SiC [23, 63, 95]. Its formation is believed to arise from the different etch rates of Si and C, with C having a slower etch rate compared to silicon [23]. This C rich-layer can act as an inhibitor layer during the RIE process and hence the removal of C can be the rate-limiting step in the etching of SiC [63, 95]. However, the mechanism by which the C rich-layer is being removed in the etching process is still unclear at present. It could be due to direct physical sputtering [21, 96], or ion assisted/enhanced plasma etching (chemical in nature) [63, 95]. Irrespective of the mechanism, a larger D.C. self-bias is usually favorable for the removal of C. From the AES results, the C/Si ratios for samples A and B are found to be 0.72 and 0.80, respectively. Since these ratios are quite close, we conclude that no C rich-layer, or C residue layer is formed for the sample etched with a 20% oxygen fraction. Similar results have been observed for samples etched at other oxygen fractions. The absence of an obvious C rich-layer in our samples may be attributed to the large D.C. self-bias voltage developed, which helps in the removal of C atoms. Hence no C rich-layer

exists to limit the etch rate, and the etch rates of our samples are determined mainly by chemical reactions rather than physical removal mechanisms.

The absence of Al contamination in our samples is consistent with the smooth etched surface observed. Aluminum contamination has been established to lead to micromasking effect in the etching of SiC and is largely responsible for coarse etched surfaces observed [61]. From our AES results shown in Table 3.2, the etched sample (Sample B) is observed to be free of Al contamination. This is despite that our plasma reactor has a large naked Al lower electrode, which can serve as a source of Al contamination under physical ion bombardment. The reason for this Al-free surfaces in our etched samples may be that hydrogen atoms, which are derived from the dissociation of CHF_3, react with aluminum to produce the volatile by-product alane (AlH_3) [21, 23]. Besides, the energetic ion bombardment could also sputter Al contamination efficiently from the sample surface.

3.4.2 The Effect of the R.F. Power

In this set of experiments, RIE of 4H-SiC was studied with varying R.F. power from 40 to 200 W. The other process parameters, i.e. process pressure, gas composition, total gas flow rate, and duration, were kept constant at 100 mTorr, 20% O_2 plus 80% CHF_3, 10 sccm, and 1 hour, respectively. Fig. 3.9 shows the change in D.C. self-bias with varying R.F. power. With increasing R.F. power from 40 to 200 W, the D.C. self-bias monotonically increases from -131 to -335 V and the sheath region developed at the R.F. power driven electrode was observed to be expanded. With increasing D.C. self-bias, positive ions gain higher kinetic energy while being accelerated in the plasma sheath, and hence lead to a stronger ion bombardment at the substrate.

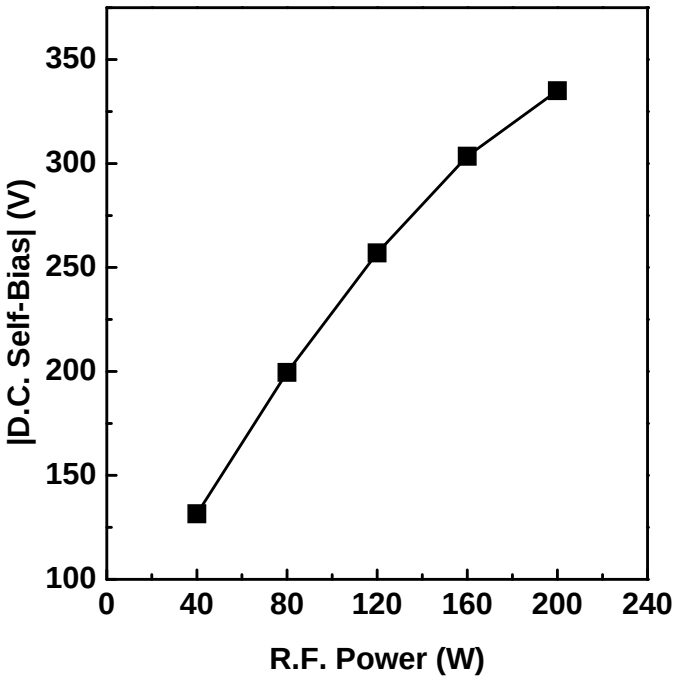


Fig. 3.9: The D.C. self-bias varies as a function of R.F. power.

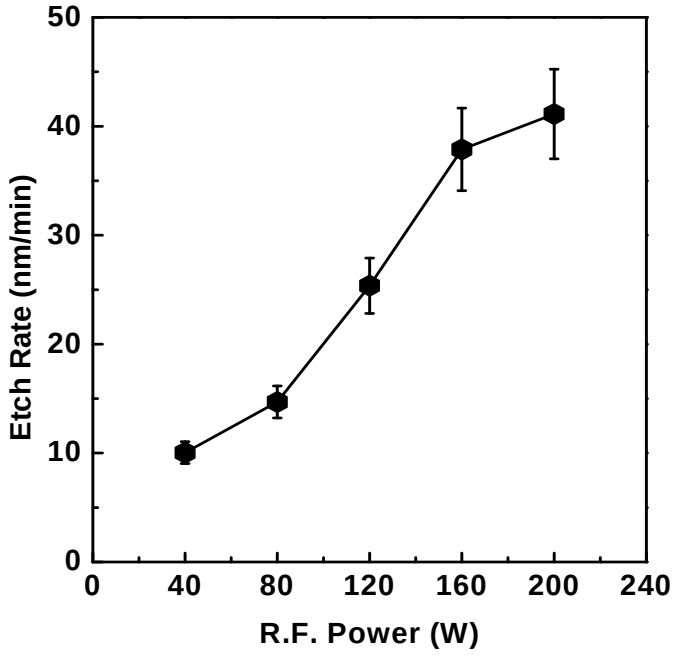


Fig. 3.10: The etch rate variation as a function of applied R.F. power.

Fig. 3.10 shows the etch rate as a function of the applied R.F. power. With increasing the R.F. power from 40 to 200 W, the etch rate monotonically increases by about four times from 10 to 41 nm/min. This is due to the fact that the plasma density increases accordingly and consequently translates into a higher electron density, higher neutral radical concentration, and higher positive ion concentration. A higher F concentration, which is the main etching species, will lead to enhanced chemical reaction with Si and C atoms. Concurrently, the ion bombardment is also intensified due to a higher positive ion concentration and higher D.C. self-bias. This also contributes to a higher etch rates as there are two major roles that the ion bombardment plays in an ion assisted plasma etching, i.e. pre-activate the surface by bombarding and breaking surface chemical bonds, e.g., the Si-C bonds (4.52 eV) [23]; and remove the volatile chemical reaction byproducts. There appears to be a saturation in the etch rate as the R.F. power increases from 160 to 200 W, which may be due to limitation of diffusion rates of neutral radicals and positive ions [63, 94].

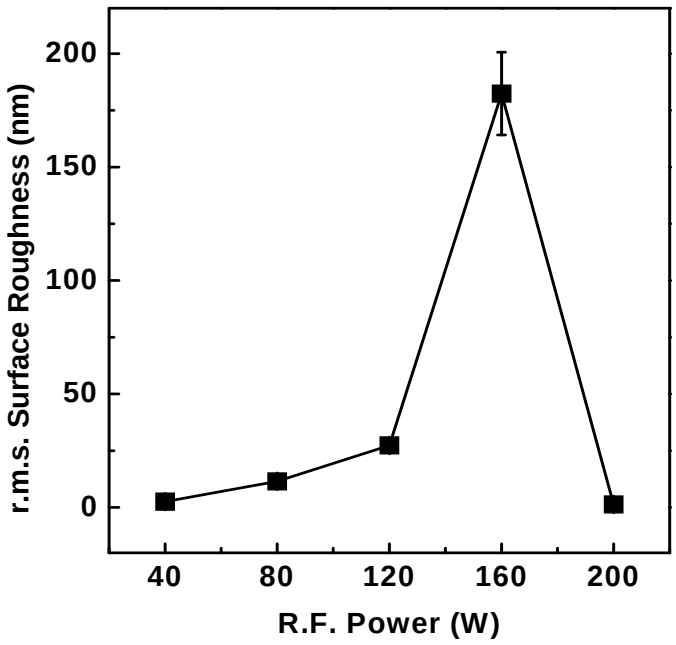


Fig. 3.11: The surface roughness in r.m.s. changes as a function of R.F. power.

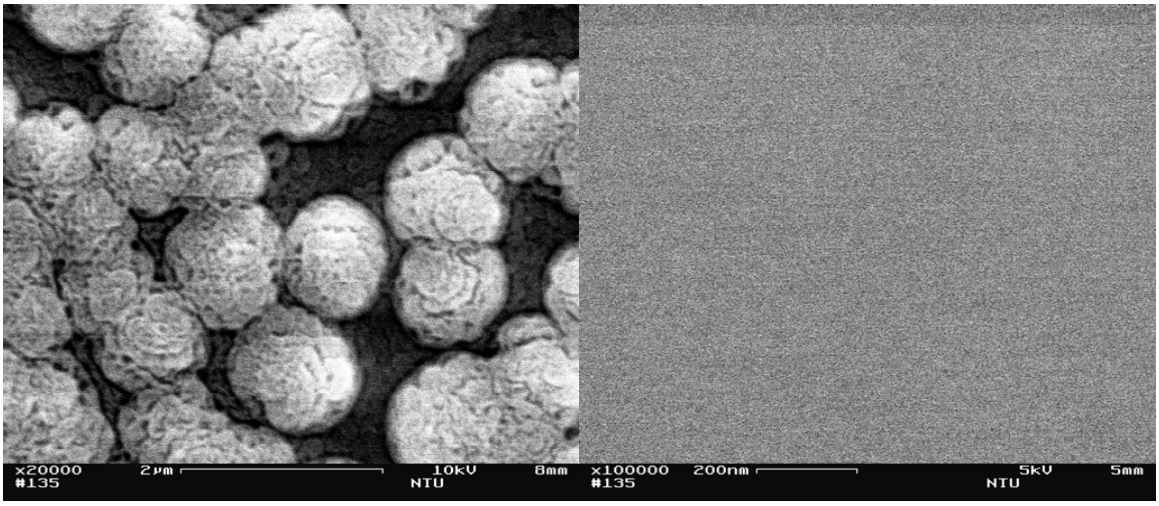


Fig. 3.12: The SEM pictures of the surface being etched at 160 W R.F. power (left) and at 200 W R.F. power (right).

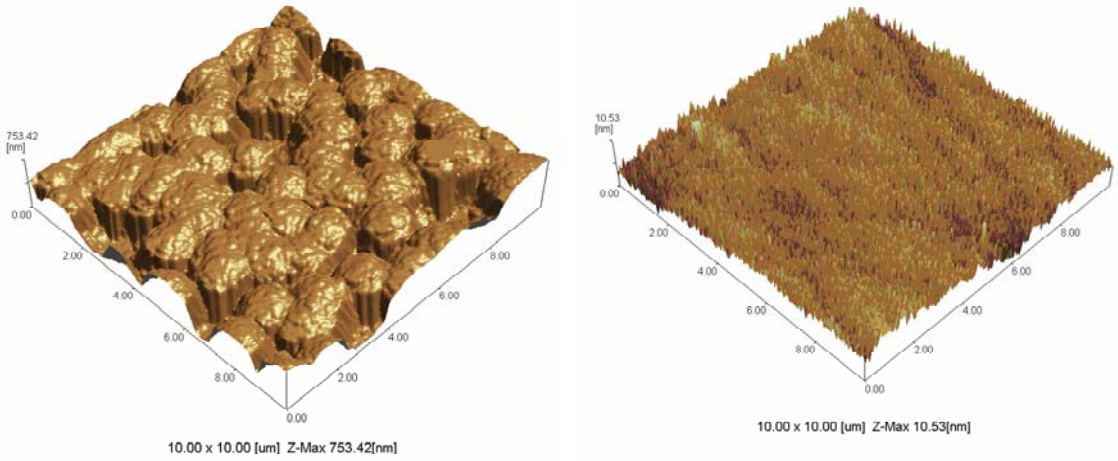


Fig. 3.13: The AFM surface morphology of the surface dry etched at 160 W R.F. power (r.m.s. surface roughness is 182.4 nm) (left) and at 200 W R.F. power (r.m.s. surface roughness is 1.3 nm) (right).

Fig. 3.11 shows the root-mean-square (r.m.s.) surface roughness (measured over an area of 10×10 μm^2 of the etched samples) as a function of the R.F. power. As can be seen, the r.m.s. surface roughness increases drastically from 2.6 to 182.4 nm with increasing R.F. power from 40 to 160 W. However, a further increase in the R.F. power to 200 W leads to a sharp decrease in the r.m.s. surface roughness to 1.3 nm. Fig. 3.12 and Fig. 3.13 show the SEM and AFM micrographs, respectively, of the

R.F. Power [W]	Element	C	N	O	F	Al	Si	Ni	C/Si Ratio
	Relative sensitivity factor (RSF)	0.128	0.158	0.371	0.954	0.309	0.137	0.485	
Unetched control sample (UCS)		38	2	6	1	-	53	-	0.72
200		35	-	18	2	-	45	-	0.8
160		46	-	14	3	8	28	1	1.64
120		39	-	17	9	12	21	2	1.86
80		32	-	17	12	14	24	1	1.33
40		39	-	15	9	11	25	1	1.56

Table 3.3: The relative surface concentration of various chemical elements in arbitrary unit versus R.F. power.

samples etched at 160 W and 200 W R.F. power. It is observed that the samples etched at 160 W R.F. power and below in general have noticeable spiked and blackened etched surfaces, a typical signature of micromasking effect. In contrast, the surface of the sample etched at 200 W R.F. power is totally clean and smooth, comparable to the unetched control sample.

We have performed AES measurements for the etched samples and unetched control sample (UCS), and the elements deduced on the surfaces etched at different R.F. powers are shown in Table 3.3. The results clearly reveal that both Al and a C rich layer (SiC_x) (the latter being manifested by the ratio of Si and C that is larger than unity) exist on the surface of the samples etched at lower R.F. power ($\leq$ 160 W). This will lead to micromasking effect and hence roughened etched surface, as corroborated by the surface roughness, SEM and AFM micrographs shown earlier on. In contrast, the control sample and the sample etched at 200 W R.F. power do not suffer from the micromasking effect and their surfaces are relatively smooth. Therefore, we conclude

that the surface roughening at lower R.F. power (≤ 160 W) is attributed to micromasking effect arising from Al and the presence of a C rich layer. In addition, beside Al, in the samples with micromasking effect, we also found a small amount of Ni, which could come from the dual-layer metal mask.

3.4.3 The Effect of the Process Pressure

In this set of experiments, RIE of 4H-SiC test chip was studied when varying the process pressure from 77 to 320 mTorr. The other process parameters, i.e. R.F. power, gas composition, total gas flow rate, and duration, were kept constant at 200 W, 20% O_2 plus 80% CHF_3, 10 sccm, and 1 hour, respectively.

Fig. 3.14 shows the D.C. self-bias as a function of the process pressure. It can be seen that with increasing process pressure from 77 to 320 mTorr, the D.C. self-bias drops almost linearly from -344 to -270 V. Higher process pressure will lower the free electron temperature due to a shortened mean-free-path, resulting in a decrease in the plasma density and D.C. self-bias. This in turn will weaken the ion bombardment onto the substrate, in terms of ion density as well as ion translation kinetic energy. As shown in Fig. 3.15, an increase in the process pressure will lead to a decrease in the etch rate of 4H-SiC. With increasing process pressure from 77 to 320 mTorr, the etch rate drops by about 43.8% from 44.1 to 24.8 nm/min.

The effect of process pressure on RIE process is well established [87]. With increasing process pressure, the ion density and ion energy will be reduced, while the neutral radical density will be increased, resulting in the etching being more chemical in nature [87]. However, instead of enhancing the etch rate, the etch rate drops which clearly demonstrates that physical ion bombardment is the rate limit factor that controls the overall RIE process.

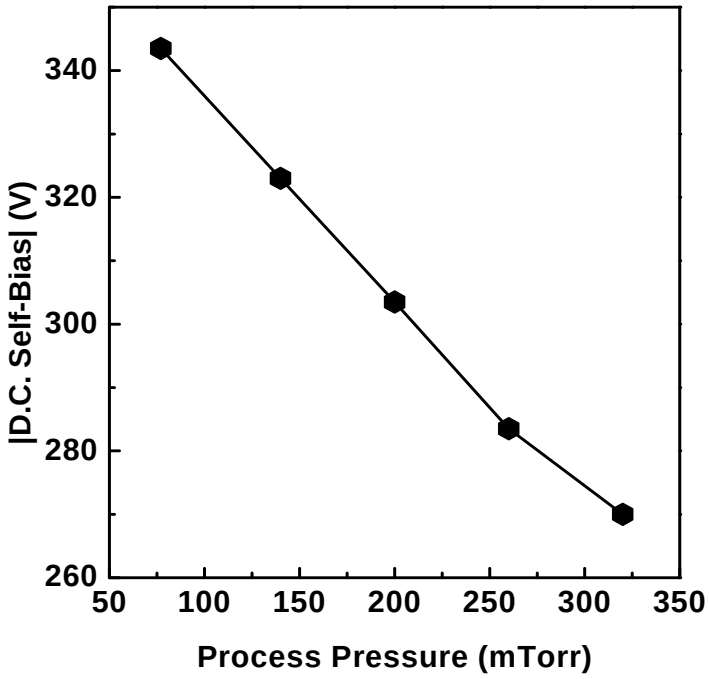


Fig. 3.14: The dependence of the D.C. self-bias as a function of the process pressure.

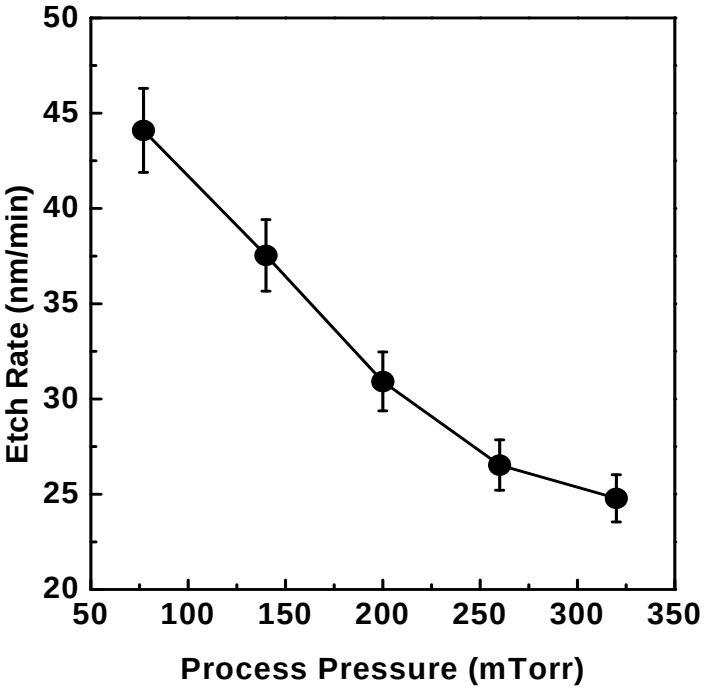


Fig. 3.15: Etch rate dependence on the process pressure.

Fig. 3.16 shows the r.m.s. surface roughness as a function of process pressure. It can be seen that with increasing process pressure from 77 to 320 mTorr, the r.m.s. surface roughness increases from 0.9 to 14.2 nm. A visual inspection reveals that the surface etched at 77 mTorr is mirror clean, similar to the unetched control sample. In contrast, the other samples show sign of micromasking effect on the etched surface, i.e. roughened blacken surface full of coarse texture. Fig. 3.17 shows the AFM surface morphology of the samples etched at 320 mTorr (left) and 77 mTorr (right), which clearly reveals the roughened surface for the sample etched at the higher process pressure.

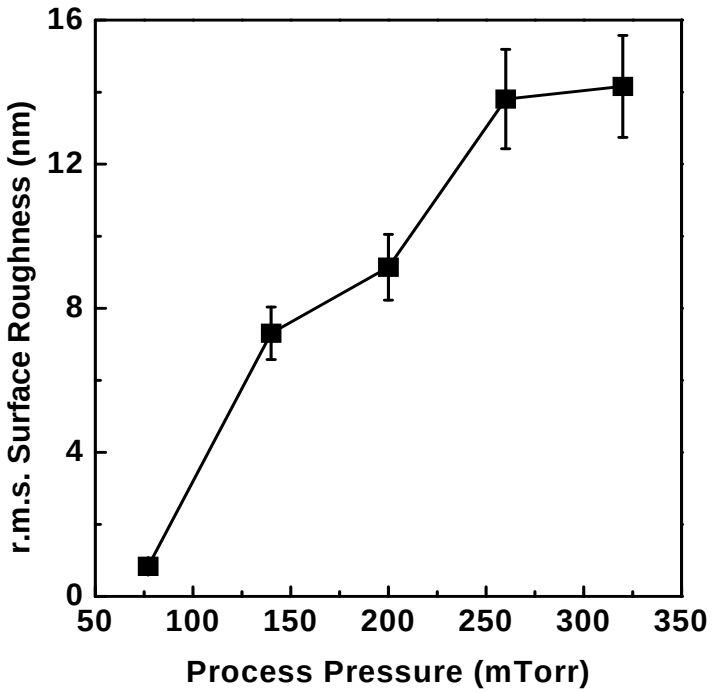


Fig. 3.16: Surface roughness in r.m.s. various as a function of process pressure.

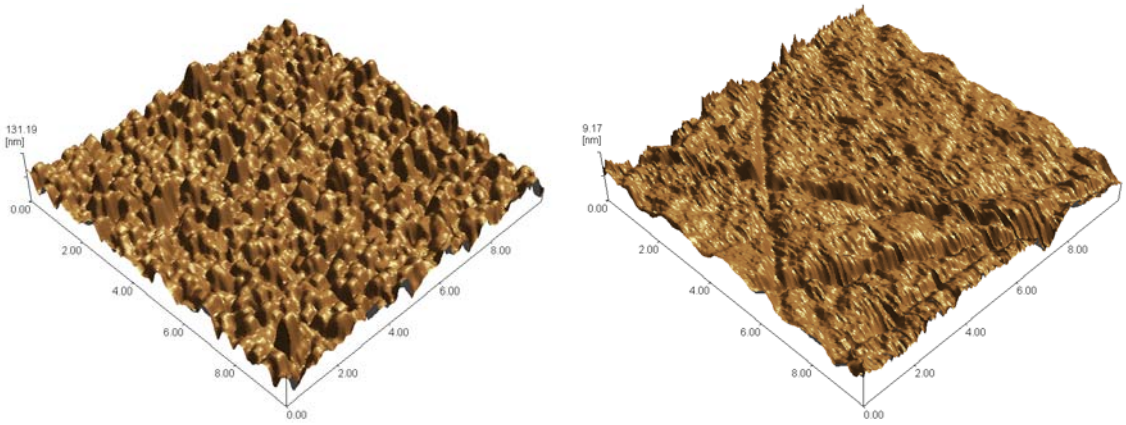


Fig. 3.17: The AFM surface morphology of the surface being etched at 320 mTorr (r.m.s. surface roughness is 14.2 nm) (left) and at 77 mTorr (r.m.s. surface roughness is 0.84 nm) (right).

Similarly, to verify the micromasking effect and its origin, we have performed AES surface analysis test. The results are shown in Table 3.4. Indeed the AES results clearly reveal the existence of both Al contaminant and C rich layer for samples etched at higher process pressures. However, these are not observed for the unetched control sample and the sample etched at 77 mTorr process pressure. This demonstrates the existence of micromasking effect, with its origin attributed to the Al contaminant and C rich layer.

As demonstrated in Fig. 3.16, the surface roughness increases with increasing process pressure and hence decreasing the D.C. self-bias. In contrast, as shown in Fig. 3.11, the surface roughness increases with the R.F. power and hence increasing the D.C. self-bias. It is noted that in both cases, the micromasking effect is present when the D.C. self-bias is less than about -320 ~ -330 V. Besides, the r.m.s. surface roughness is observed to increase moderately from 7.3 to 14.2 nm when the D.C. self-bias changes from -323 to -270 V. Considering that with increasing process pressure, the chemical reaction is enhanced while the physical ion bombardment is actually

Process Pressure [mTorr]	Element	C	N	O	F	Al	Si	Ni	C/Si Ratio
	Relative sensitivity factor (RSF)	0.128	0.158	0.371	0.954	0.309	0.137	0.485	
Unetched control sample (UCS)		38	2	6	1	-	53	-	0.72
77		41	-	5	-	-	54	-	0.76
140		32	-	16	11	14	26	1	1.23
200		26	-	23	12	17	19	3	1.37
260		26	3	16	15	16	21	3	1.24
320		24	2	20	13	17	20	4	1.20

Table 3.4: The relative concentration of surface elements in arbitrary unit versus process pressure.

weakened, the increase in surface roughness may more likely be due to the enhanced chemical etching. A detailed discussion of the relation between the micromasking effect and the D.C. self-bias is presented in the following section.

3.4.4 The Micromasking Effect and the D.C. Self-Bias

The micromasking effect is one of the surface morphology defects brought about during plasma etching process. It severely degrades the quality of the etched surface with observable roughened, blackened and textured surface, and thus should be avoided. While the root cause of micromasking effect is still under debate [23], in the case of SiC etch, it has been widely reported that metal contamination was found to exist concurrently with micromasking effect [23]. It is believed that the origin of the metal contaminants is due to physical sputtering of metal mask and/or uncovered electrode, such as Al from Al mask and/or electrode [82]. The metal particles redeposited onto the etching surface act as micro-size mask and thus prohibit the localized dry etching of the underlying layer on the surface, which reduces the local etch rate and makes it extremely uneven, eventually causing darkened, grass-like

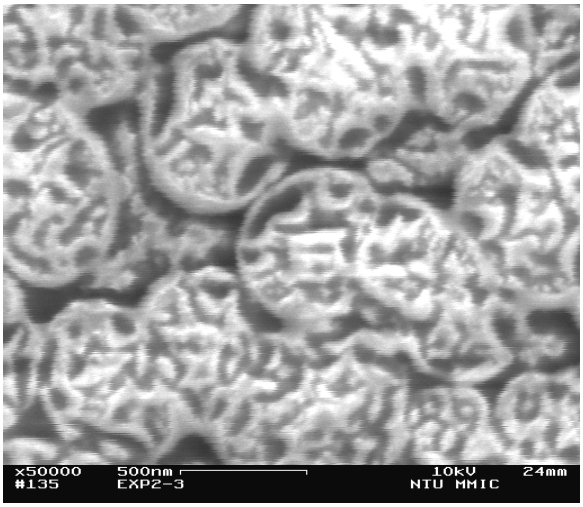


Fig. 3.18: SEM picture of a surface that has undergone serious micromasking. RIE process parameters are set as 120 W R.F. power, 100 mTorr process pressure, 2 sccm O_2, 8 sccm CHF_3, and 1 hour etching duration.

textured etched surface. A typical SEM picture of a surface that suffered from the micromasking effect is shown in Fig. 3.18. A further surface analysis test using AES can identify the existence of metal contamination, such as Al, as shown in Fig. 3.19.

Similarly, Al contamination originated from Al made lower electrode can also cause micromasking effect in chlorinated or fluorinated plasma etching of Si [46]. In most cases, an addition of hydrogen gas to chlorinated or fluorinated plasma can remove the Al contamination and eliminate the micromasking effect by forming volatile product alane (AlH_3) [21].

In our RIE tests, besides the Al contamination, a C rich layer (manifested as C/Si ratio larger than unity) can also be observed especially under certain circumstances such as low R.F. power or high process pressure when the D.C. self-bias is low. This has been earlier demonstrated in our AES results. It is believed that the etching of C is mainly controlled by physical sputtering or positive ion bombardment assisted plasma

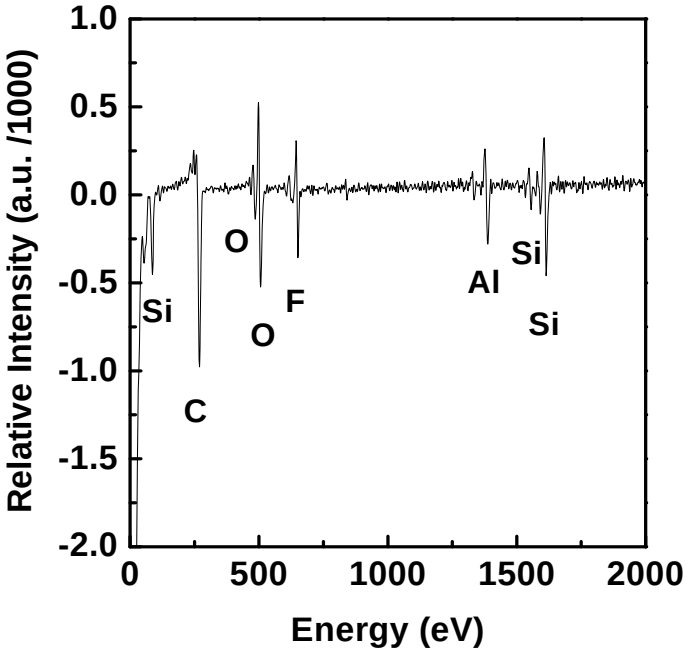


Fig. 3.19: AES spectrum of RIE etched sample with micromasking effect. The etching condition is: R.F. power 160W, process pressure 100 mTorr, CHF_3 flow rate 8 sccm, and O_2 flow rate is 2 sccm.

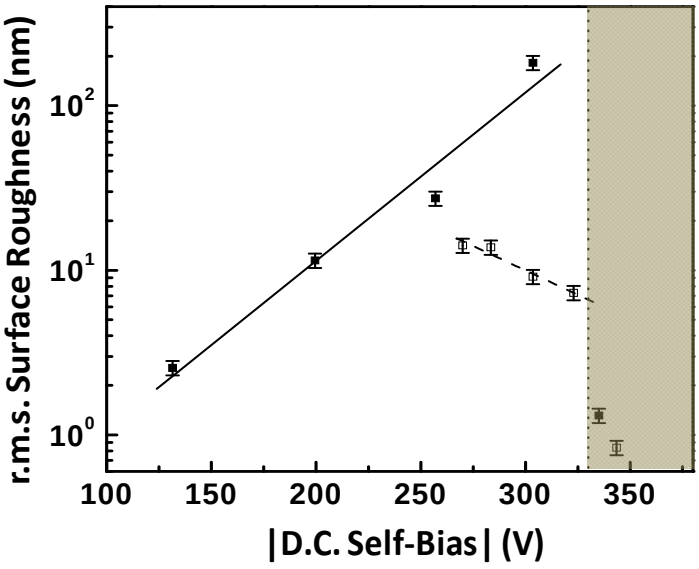


Fig. 3.20: The r.m.s. surface roughness in r.m.s. with error bar as a function of the D.C. self-bias, when either the R.F. power (■) or the process pressure (□) is varied. The grey shaded area demarcates experimental conditions for which no micromasking effect was observed.

etching. Under low D.C. self-bias, the C etch rate is weakened compared with that of Si, leading to the formation of a C rich layer. This C rich layer, which is amorphous in nature, may consist of a mixture of sp^3 and sp^2 bonded C across different areas [23]. Under weak positive ion bombardment, the strongly bonded sp^3 areas have a much lower etch rate and hence act as micromask during the etching process.

As the presence of Al contamination and C rich layer, which are the sources of roughened etched surfaces, are highly correlated to the D.C. self-bias, we have plotted the r.m.s. surface roughness as a function of the D.C. self-bias, for two sets of etching experiments with varying R.F. power and process pressure, respectively, as shown in Fig. 3.20. It can be seen from the figure that a clear threshold D.C. self-bias exists around -320 to -330 V, beyond which the surface is relatively smooth. Therefore, it can be concluded that the micromasking effect induced by Al contamination and C rich-layer exist only at D.C. self-bias values lower than the threshold value, whereas samples that were etched in conditions that provided resulted in a D.C. self-bias above the threshold value are free of micromasking effect.

For Al contamination induced micromasking effect, an increase in the D.C. self-bias at constant process pressure will enhance Al sputtering from the chuck electrode and introduce heavier Al contamination, which in turn causes more severe micromasking effect and surface roughening. However, when the D.C. self-bias is sufficiently high and the sputtering effect is too strong to result in the formation of Al clusters on the surface, then there is no Al contamination induced micromasking effect. Similarly, for C rich layer induced micromasking effect, increasing the D.C. self-bias will enhance the etch rate of C. Unless the D.C. self-bias is sufficiently high to overcome the strong C-C (6.2 eV) bonds, increasing the D.C. self-bias will enhance

the etch rate of the weakly bonded sp^2 C rich area rather than the strongly bonded sp^3 C rich area. This will result in more severe micromasking effect and hence enhanced roughened etched surface. However, when the D.C. self-bias is higher than some threshold value, all C residues can be removed efficiently such that no C rich layer and its associated micromasking effect induced surface roughening are observed.

Enhanced chemical reactions due to either a higher R.F. power or higher process pressure will only enhance the etch rate of the areas with no micromasks, whereas the areas with micromasks are less affected. This will result in more severe micromasking effect induced surface roughening provided that the D.C. self bias is not high enough to overcome the micromasked areas. Based on the above discussion, our surface roughness results can be understood as follows. For the sets of experiments with varying R.F. power, the initial increase in R.F. power enhances both the physical ion bombardment and chemical etching. Before reaching the threshold D.C. self-bias, the micromasking effects due to the Al contamination and C rich layer result in rougher etched surfaces with increasing R.F. power. However, once the threshold D.C. self-bias is reached, all micromasks have been removed and the etched surfaces are smooth and free of micromasking effect. For the sets of experiments with varying process pressure, , the surface roughness increases with decreasing the D.C. self-bias under increasing process pressure in the region below the threshold D.C. self-bias, which can be attributed to enhanced chemical etching reaction.

Finally, we can now indicate the most possible mechanisms responsible for the removal of Al and C at D.C. self-bias above the threshold value. In our case, the Al contaminants are most likely been etched by physical sputtering, in contrast with literature data which previously reported that the Al was etched away chemically by

deliberately introducing hydrogen gas into the plasma [21, 82] As for the removal of C, , it is more likely that it is etched away by physical sputtering or positive ion assist plasma etching instead of through a purely chemical etching.

3.5 Summary

In this chapter, we have studied reactive ion etching (RIE) of n^+ type 4H-SiC based on CHF_3+O_2 plasma. The etch rate, surface morphology, surface roughness and surface elements, were studied by varying the O_2 fraction, R.F. power and process pressure. While the F is found to play a dominant role in the plasma etching process, the role of O is multiple. At low O_2 fractions, it enhances F concentration which in turn increases the etch rate, while at high O_2 fractions, it dramatically lowers the etch rate by diluting F concentration and forming protective oxide-like surface layers by chemisorption. An increase in the R.F. power greatly enhances the etch rate by providing higher densities of the neutral radicals and the positive ions, as well as an increased impinging ion energy. In contrast, the etch rate decreases with increasing process pressure due to the weakening of impinging ion energy, despite a general enhancement of the chemical reactions.

The surface roughness is strongly affected by the D.C. self-bias but less affected by the O_2 fraction. At low D.C. self-bias values, the etched surface becomes rougher with increasing the D.C. bias. Auger Electron Spectroscopy (AES) analyses have related such surface roughness to the micromasking effect induced by Al clusters and carbon residues (C rich layer). The appearance and the extent of the micromasking effect was affected by the positive ion bombardment, which in turn, was controlled by the D.C. self-bias and can be removed at high D.C. self-bias values above a threshold

value of between -320 and -330 V when no micromasking effect has been observed regardless of the value of O_2 fraction and the etched surface is mirror clean, similar to the unetched control sample.

In this study, apart from the understanding gained about the RIE process of 4H-SiC, an optimum etching condition has also been deduced. It is found to occur at 20% O_2 fraction, 200 W (1.13 W/cm^2) R.F. power, 100 mTorr process pressure, and 10 sccm total feed in gas flow rate. The optimized etch rate achieved is 35.6nm/min, and the etched surface is very smooth， with an r.m.s. surface roughness of 1.65 nm.

Chapter 4

Numerical Modeling of 4H-SiC Plasma Etching Based on Artificial Neural Network

4.1 Introduction

Plasma etching of SiC is a key process in the fabrication of SiC based devices. Unfortunately, it does not have a reasonably high selectivity over different dopant types/doping levels [55]. As a result, it suffers from a lack of a reliable etching stop layer for the various important etching processes such as mesa etch, recess etch, or trench etch. In practice the etching depth control and optimization are largely dependent on etch rate estimation. Hence, a detailed knowledge of the plasma etching behavior and its modeling are essential to achieve a better process control for the fabrication of SiC devices. Due to the extremely complicated non-linear plasma behavior [22], models that are based on plasma physics and statistics are difficult to derive and are not robust. In contrast, based on the advance of computer science and artificial intelligence, neural networks of different paradigms have been widely used in the semiconductor plasma etching process modeling [67, 75, 97] and real-time control [98, 99], as they are capable of learning complex relationships between groups of related parameters [100].

As one of the most widely used neural network paradigms, the feed-forward neural network (FNN) is composed of a vast number of parallel simple processing units (neuron) in a layered architecture [101]. In a properly trained FNN, the complex relationships between groups of related parameters are stored in these connected weights and threshold values of each processing neuron. The FNN belongs to a large category of supervised neural network that can be further broken down based on the different training algorithms, e.g. the conventional back propagation (BP) algorithm, generalized regression algorithm, genetic algorithm (GA). Among these algorithms, BP algorithm is the most extensively studied with huge success in various process modeling and real-time control regimes, including plasma etching process [67, 75]. Despite the success, as a crude gradient descent optimization algorithm, it has some inherent disadvantages, including non-convergence, slow convergent rate, over-fitting [102].

In this chapter, a novel numerical model of FNN trained by the Broyden, Fletcher, Goldfarb, and Shanno (BFGS) algorithm is developed to simulate with high accuracy the ECR plasma etching of 4H-SiC based on SF_6+O_2 plasma [25]. Although the BFGS training algorithm has been in other fields for decreasing the training time, it has not been used for the modeling of plasma etching process. We have also compared the BFGS with the BP algorithm in terms of their approximation and generalization ability, which are important in the application of FNN for the simulation and control of SiC etching process. The first part of the chapter presents the background of the FNN structure and its working principles, the BFGS algorithm and the conventional BP algorithm. The advantages of the BFGS algorithm over the conventional BP algorithm, including their approximation and generalization ability, are also discussed. In the second part, the performances of both the BFGS and BP algorithms are extensively

tested with our experimental etching data and the results are compared in terms of convergence property and r.m.s. error of cross-validation test to obtain the best FNN structure. In the last part, we compared the modeled etch rates with our test results, and obtained a very good fit between the two.

4.2 Artificial Neural Network and Training Algorithm

4.2.1 Network Architecture [101]

Fig. 4.1 schematically shows a typical three-layer FNN structure used in this work, which has one input layer with n input nodes, one hidden layer with h neurons, and one output layer with m neurons. By denoting the synaptic weights between the input layer and hidden layer as $w_{ji}\left(j=1,2,\cdots,h;i=1,2,\cdots,n\right)$ and the threshold of hidden neurons as $\theta_j\left(j=1,2,\cdots,h\right)$, the input signal I_j (not shown in the figure) and output signal O_j of the j^{th} hidden neuron can be expressed as functions of network input signals $x_i(i=1,2,\cdots,n)$ as:

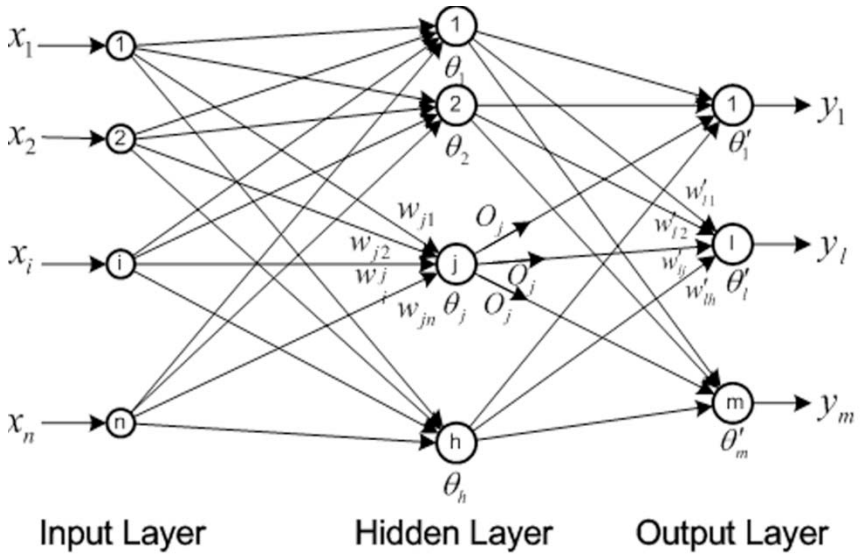


Fig. 4.1: Network architecture of a three-layered feed-forward neural network.

$$I_j = \sum_{i=1}^{n} w_{ji} x_i \qquad j = 1, 2, \cdots, h, \tag{4.1}$$

$$O_j = f_j\left(I_j + \theta_j\right) = \frac{1}{1 + \exp\left[-\left(I_j + \theta_j\right)\right]} \qquad j = 1, 2, \cdots, h \tag{4.2}$$

where $f_j\left(I_j + \theta_j\right)$ is the transfer function of the j^{th} hidden neuron. Each output in the network is determined by the synaptic weights between the output neuron and all hidden neurons, $w'_{lj}\left(l = 1, 2, \cdots, m; j = 1, 2, \cdots, h\right)$ and the bias $\theta'_l\left(l = 1, 2, \cdots, m\right)$ of the output neuron in the same manner, i.e.

$$y_l = \frac{1}{1 + \exp\left[-\left(\sum_{j=1}^{h} w'_{lj} O_j + \theta'_j\right)\right]} \qquad l = 1, 2, \cdots, m \tag{4.3}$$

4.2.2 Back-Propagation (BP) Algorithm [101]

The principle of using FNN to model plasma etching is to utilize its function approximation ability to describe the relation between the parameters in the etching process. This is done by training the neural network using some samples (shown as input-output pairs) taken from the etching process testing, such that the input-output relation of the network can properly fit the given samples. The conventional training method uses BP algorithm to minimize the mean-squared error between the given outputs in the samples and the neural network outputs. The error function is usually taken as:

$$\min_{w} E = \frac{1}{2} \sum_{p=1}^{N} \sum_{l=1}^{m} \left(\hat{y}_{lp} - y_{lp}\right)^2 \tag{4.4}$$

where $\hat{y}_{lp}\left(l = 1, 2, \cdots, m; p = 1, 2, \cdots, N\right)$ is the desired output in each sample, y_{jp} is the corresponding ANN output, and N is the sample size. From Eqs. (4.2) and (4.3), it can

be seen that the input-output relation in ANN is fully determined by all the weights and thresholds: $w_{ji}\left(j=1,2,\cdots,h;i=1,2,\cdots,n\right)$, $w'_{lj}\left(l=1,2,\cdots,m;j=1,2,\cdots,h\right)$, $\theta_j\left(j=1,2,\cdots,h\right)$ and $\theta'_l\left(l=1,2,\cdots,m\right)$, which together form a weighting vector $\boldsymbol{W}$.

The BP algorithm uses a simple iteration formula to sequentially update $\boldsymbol{W}$, starting from a random vector $\boldsymbol{W}_0$, until a stable solution is obtained. The iteration formula is

$$\left.\begin{aligned}\Delta\boldsymbol{W}_k &= -\eta\frac{\mathrm{d}E}{\mathrm{d}\boldsymbol{W}_k}\\ \boldsymbol{W}_{k+1} &= \boldsymbol{W}_k+\Delta\boldsymbol{W}_k\end{aligned}\right\}\quad k=0,1,2,\cdots\cdots, \tag{4.5}$$

where η is referred to as the learning rate (LR), $\frac{\mathrm{d}E}{\mathrm{d}\boldsymbol{W}_k}$ is the gradient vector of the error function with respect to the weighting vector $\boldsymbol{W}$. By substituting Eqn. (4.2) into Eqn (4.3)., and then substituting the result output y_l into Eqn. (4.4), the error function as well as the gradient vector can be explicitly expressed in terms of the weighting vector $\boldsymbol{W}$. All components in the gradient vector can be analytically expressed as follows:

$$\frac{\partial E}{\partial W'_{lj}}=\sum_{p=1}^{N}y_{lp}\left(\hat{y}_{lp}-y_{lp}\right)\left(y_{lp}-1\right)O_j\qquad l=1,2,\cdots,m;j=1,2,\cdots,h,$$

$$\frac{\partial E}{\partial \theta'_j}=\sum_{p=1}^{N}y_{lp}\left(\hat{y}_{lp}-y_{lp}\right)\left(y_{lp}-1\right)\qquad j=1,2,\cdots,h,$$

$$\frac{\partial E}{\partial W_{ji}}=\sum_{p=1}^{N}\sum_{l=1}^{m}y_{lp}\left(\hat{y}_{lp}-y_{lp}\right)\left(y_{lp}-1\right)W'_{lj}O_j\left(1-O_j\right)x_i$$

$$j=1,2,\cdots,h;i=1,2,\cdots,n,$$

$$\frac{\partial E}{\partial \theta_i}=\sum_{p=1}^{N}\sum_{l=1}^{m}y_{lp}\left(\hat{y}_{lp}-y_{lp}\right)\left(y_{lp}-1\right)W'_{lj}O_j\left(1-O_j\right)$$

$$i=1,2,\cdots,n.$$

Sometimes, a momentum term α is introduced in the iteration formula Eqn. (4.5) to improve the convergence property, i.e.

$$\boldsymbol{W}_k = \boldsymbol{W}_k - \eta \frac{\mathrm{d}E}{\mathrm{d}\boldsymbol{W}_k} + \alpha \Delta \boldsymbol{W}_k . \tag{4.6}$$

4.2.3 Approximation Ability and Generalization Ability of FNN

The FNN possesses excellent approximation ability, as shown by Kolmogorov [101] that for any continuous mapping *f*, there must exist a three-layer neural network that can implement *f* exactly. However, owning to some limitations or difficulties in getting samples in practical application, only finite (or even fewer) samples can be used in training the network. Despite this, it is necessary that the network should still be precise for the input-output pairs not presented in the training samples. This requirement is referred to as the generalization ability of FNN, and is as important as the approximation ability.

In fact, the learning of the FNN can be regarded as performing a simple fitting operation in a multiple input/output space, while to get the input-output pairs not included in the training samples can be viewed as interpolating or extrapolating on the fitting hyperspace. In most cases, the approximation ability and the generalization ability can be unified provided the structure of FNN (number of hidden neurons), the training sample selection and the learning algorithm are properly selected. However, in many cases, these two abilities are in contradiction, especially when more hidden neurons are adopted; and in the worst case, it may even result in the so-called “over fitting” phenomenon such that the FNN possesses very poor generalization ability. This phenomenon is mostly caused by an improper BP algorithm, as the algorithm shown in Eqn. (4.5) is nothing but using the steepest decent method with a constant step-length to solve the unconstrained optimal problem shown in Eqn. (4.4), and the

algorithm shown in Eqn. (4.6) can be viewed as a simplified conjugate gradient method also with a constant step-length. As the convergence cannot be guaranteed by these two simplified methods, excessive hidden neurons may have to be used to reduce the training error in Eqn. (4.4) to an acceptable level.

4.2.4 BFSG Training Algorithm

To overcome the above-mentioned drawback in using the BP learning algorithm, the BFGS algorithm is used in this work, which is one of the most promising methods for solving the unconstrained optimal problem shown in Eqn. (4.4). For an unconstrained optimal problem, the conventional Newton algorithm is based on a quadratic model from a truncated Taylor series expansion of the objective function (i.e. error function in the FNN training) around $\boldsymbol{W}_k$:

$$E\left(\boldsymbol{W}_k+\boldsymbol{\delta}\right)=E_k\left(\boldsymbol{\delta}_k\right)=E_k+\boldsymbol{g}_k^T\boldsymbol{\delta}+\tfrac{1}{2}\boldsymbol{\delta}^T\boldsymbol{G}_k\boldsymbol{\delta}\,, \tag{4.7}$$

where $E_k(\delta)$ is the resulting quadratic approximation at iteration k, $\boldsymbol{\delta}=\boldsymbol{W}-\boldsymbol{W}_k$, $\boldsymbol{g}_k=\nabla E_k=\dfrac{\mathrm{d}E}{\mathrm{d}\boldsymbol{W}_k}$ is the gradient of the objective function, and $\boldsymbol{G}_k=\nabla^2 E_k$ is the Hessian matrix. However, one problem associated with the conventional Newton algorithm is that the Hessian matrix may not be positively definite and consequently the line search direction may not point in the direction of descending error function. Even if the Hessian matrix is positively definite, the calculation of the matrix is time consuming and hence inefficient. To cope with a more general scenario, a class of quasi-Newton algorithm including the BFGS algorithm has been proposed in the literature, in which a symmetric, positive definite matrix $\boldsymbol{B}_k$ is used to approximate the Hessian matrix [102]. The BFGS optimization algorithm was proposed independently by Broyden, Fletcher, Goldfarb, and Shanno in 1970 [102], in which a rank-two

correction method was used to calculate and update $\boldsymbol{B}_k$, and to preserve $\boldsymbol{B}_k$ to be symmetric and positively definite. The use of an inexact line search scheme in the algorithm improves the computation speed and allows the algorithm to have a global convergence property [102]. To date, it remains the best quasi-Newton optimization algorithm. The BFGS algorithm generally comprises four sequential steps. In the k^{th} iteration, the BFGS algorithm is as follows:

Step 1: Set line search direction

$$\boldsymbol{s}_k = -\boldsymbol{B}_k^{-1}\boldsymbol{g}_k \tag{4.8}$$

Step 2: Linear search along the search direction s_k, i.e. find the step-length such that

$$f\left(\boldsymbol{W}_k + \alpha_k \boldsymbol{s}_k\right) = \min_{\alpha \geq 0}\left(f\left(\boldsymbol{W}_k + \alpha \boldsymbol{s}_k\right)\right) \tag{4.9}$$

In the inexact line search scheme, it is selected to satisfy the following relations

$$\begin{aligned} E\left(\boldsymbol{W}_k + \alpha_k \boldsymbol{s}_k\right) &\leq E\left(\boldsymbol{W}_k\right) + \rho\alpha_k \boldsymbol{g}_k^T \boldsymbol{s}_k \\ \left|\boldsymbol{g}\left(\boldsymbol{W}_k + \alpha_k \boldsymbol{s}_k\right)^T\right| &\leq -\sigma \boldsymbol{g}_k^T \boldsymbol{s}_k \end{aligned} \tag{4.10}$$

where $\rho \in \left(0, \frac{1}{2}\right)$, $\sigma \in \left(\rho, 1\right)$.

Using the line search result, the new weighting vector is updated as

$$\boldsymbol{W}_{k+1} = \boldsymbol{W}_k + \alpha_k \boldsymbol{s}_k \tag{4.11}$$

Step 3: Update $\mathbf{B}_k$ to $\mathbf{B}_{k+1}$ by using the following rank-two correction

$$\boldsymbol{B}_{k+1} = \boldsymbol{B}_k + \frac{\boldsymbol{\gamma}_k \boldsymbol{\gamma}_k^T}{\boldsymbol{\gamma}_k^T \boldsymbol{\delta}_k} - \frac{\boldsymbol{B}_k \boldsymbol{\delta}_k \boldsymbol{\delta}_k^T \boldsymbol{B}_k}{\boldsymbol{\delta} T_k^T \boldsymbol{B}_k \boldsymbol{\delta}_k}, \tag{4.12}$$

where

$$\begin{aligned} \boldsymbol{\delta}_k &= \boldsymbol{W}_{k+1} - \boldsymbol{W}_k \\ \boldsymbol{\gamma}_k &= \boldsymbol{g}_{k+1} - \boldsymbol{g}_k \end{aligned} . \tag{4.13}$$

Step 4: Check convergence by some specified criterion. Conventionally, this criterion is set as the gradient of the objective function to be smaller than a given value to stop the iteration, i.e.

$$\sqrt{\boldsymbol{g}_k^T \boldsymbol{g}_k} \le \varepsilon \tag{4.14}$$

The iteration starts from letting k=0, while the initial value of components in the weighting vector is set randomly in the interval [0, 1], and the initial matrix $\boldsymbol{B}_0$ is a symmetric, positively definite matrix, where normally it is set as $\boldsymbol{B}_0=\boldsymbol{I}$. The iteration process sequentially follows: first to calculate the search direction by Eqn. (4.8) and then perform the inexact line search based on Eqn. (4.10); update the weighting vector $\boldsymbol{W}_k$ to $\boldsymbol{W}_{k+1}$ by Eqn. (4.11) and $\boldsymbol{B}_k$ to $\boldsymbol{B}_{k+1}$ by Eqs. (4.13) and (4.12); after that the gradient $\boldsymbol{g}_k$ is compared with the convergent criterion as shown in Eqn. (4.14). When the convergent criterion is satisfied, the training iteration ends; otherwise, set k=k+1 and repeat the whole iteration calculation.

Due to the better convergence property of the BFGS algorithm, the FNN will require less hidden neurons to reach the same training error and result in a better generalization ability. The detailed comparison between the BP and BFGS training algorithms in the modeling of plasma etching of SiC will be given in the next section.

4.3 Experimental Setup

In this work, the SiC samples used for the etching tests were 5 × 5 mm^2 *n* type bulk 4H-SiC wafers, silicon faced, 8° off-axis toward the $\langle 11\bar{2}0 \rangle$ orientation, with a doping level of 6.9×10^{18} cm^{-3}. The SiC samples were cleaned using a standard RCA clean process. The mask used for the plasma etching test was a dual metal layer that consisted of 30 nm thick titanium and 300 nm thick nickel, deposited using electron beam evaporation and patterned using a standard lift-off process.

The plasma-etching test was performed with a standard electron cyclotron resonance (ECR) plasma reactor [103]. The system is shown schematically in Fig. 4.2. The ECR plasma system consists of a cylindrical excitation chamber Attached immediately below the excitation chamber is the deposition chamber. The system is essentially a downstream design whereby ions produced in the excitation chamber are extracted into the process chamber through the diverging magnetic field. The excitation source is a 1.5 kW, 2.45 GHz microwave generator (AX2115) from the Applied Science Technology Inc. The substrate bias power supply is a 600 W, 13.56 MHz R.F. generator (RFX-600) from Advanced Energy Inc. The microwave power is guided through a rectangular waveguide and introduced into the ECR magnetron excitation chamber through a quartz window. With currents of 120 A and 100 A for the upper and lower magnetic coils, respectively, a magnetic field of 875 G required for the ECR condition is generated in the middle of the excitation chamber. The divergent magnetic field configuration accelerates the plasma towards the deposition chamber where the substrates are located. The substrate stage is isolated from the grounded chamber wall and is driven by the 13.56 MHz R.F. generator.

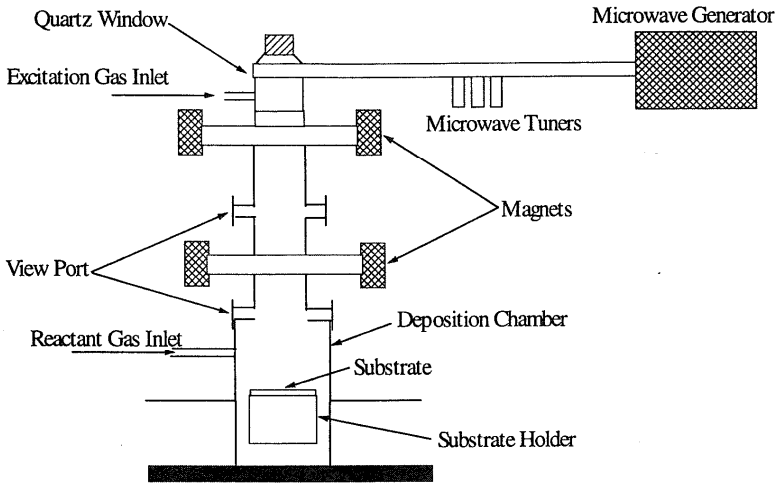


Fig. 4.2: The schematic diagram of ECR plasma system.

In the plasma-etching test, SF_6 and O_2 were used as the etchant gases. The etch rate was characterized with a surface stylus profilometer. The process parameters for a high density plasma reactor include gas flow rates, microwave power, R.F. power, D.C. bias, process pressure, temperature, process duration. As a standard two-level with center point full factorial test has shown that plasma etching behavior is highly nonlinear, high order experiment design models are required to simulate it more accurately. In this work, a four-factor and five-level standard Box-Wilson CCD was used for our design of experiments (DOE) [104]. To save the test budget, we focus on four most important process parameters (i.e. the input variables of FNN), namely, the microwave power, D.C. bias, process pressure, and O_2 fraction defined as the ratio of O_2 flow rate to the total gas flow rate of 10 sccm. The ranges of the parameters used are listed in Table 4.1. To meet the requirement of the Box-Wilson CCD, a total of 25 tests were performed to obtain 25 samples to be used in the FNN training. The details of the 25 samples were listed in Table 5.2. In addition, another 25 randomly selected

Process Parameter	Adjust Range
Microwave Power [W]	200 ~ 1000
D.C. **Bias [V]**	-100 ~ -500
Process Pressure [mTorr]	1 ~ 15
Oxygen Fraction [%]	0 ~ 100

Table 4.1: Process Parameters and adjustable ranges in the DOE etching process test.

tests were also performed for the purpose of cross-validation. The output of the FNN is the the etch rate of 4H-SiC.

4.4 Modeling Results and Discussion

4.4.1 Number of Hidden Neurons

It has been conceptually shown in the previous section that the BFGS algorithm based FNN has great advantages over the conventional BP algorithm based FNN. In this section, we will verify it using our etching test results as samples in the FNN training, and then compare the performance of these two algorithms. The inputs of the FNN are process pressure, microwave power, D.C. bias, and O_2 fraction as listed in Table 4.1, and the output is the SiC etch rate. The comparison is performed with different numbers of hidden neurons and various learning rates in the BP algorithm, while the performance is measured by the training error (E) of the error function shown in Eqn. (4.4), the cross-validation (CV) test results and the existence of over-fitting phenomenon.

Fig. 4.3 compares the final training error with respect to the hidden neuron number (HNN) of FNN for both BFGS and BP algorithms, and various learning rates (LR) for the BP algorithm. All trainings were terminated at 1000 iterations. For the BP

algorithm, the momentum is set at 0.1. It is obvious that for the BFGS algorithm, the training error rapidly decreases from near 0.04 to less than 2×10^{-3} with increasing HNN from 1 to 5, and then almost remains constant at 1.5×10^{-3} with a further increase in the HNN up to 10. In contrast, for the conventional BP algorithm, it results in a training error that is almost independent of the HNN in the range of 1 to 10. In addition, the LR also has less impact on the training error for the BP algorithm. As LR changes from 0.1 to 0.3, the training error only decreases from 0.07 to 0.04 approximately, and further increasing LR has no effect on the training error. The results demonstrate that the BFGS algorithm is more powerful and efficient than the BP algorithm in the FNN training and with less HNN needed. It can be seen from this result that the number of 5 hidden neurons seems a proper choice for the FNN trained by BFGS algorithm, whereas the HNN should be larger than 10 for using BP algorithm to get as smaller training error as the BFGS algorithm.

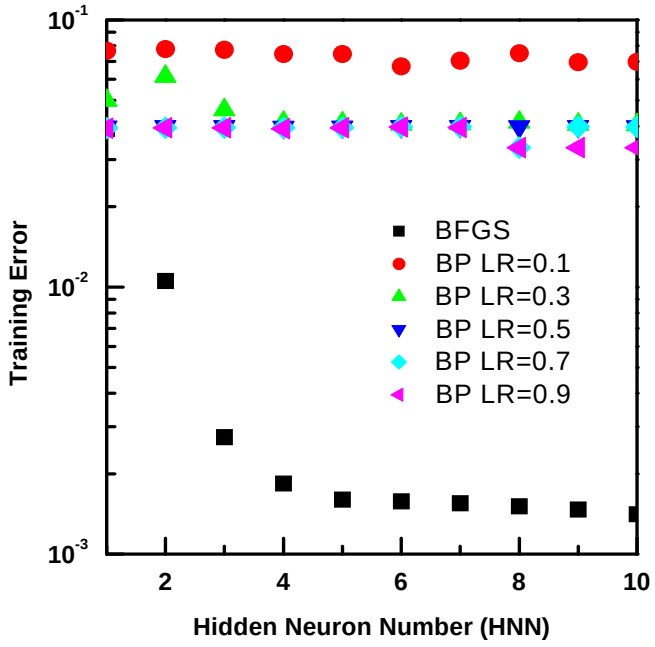


Fig. 4.3: Training error versus HNN and LR.

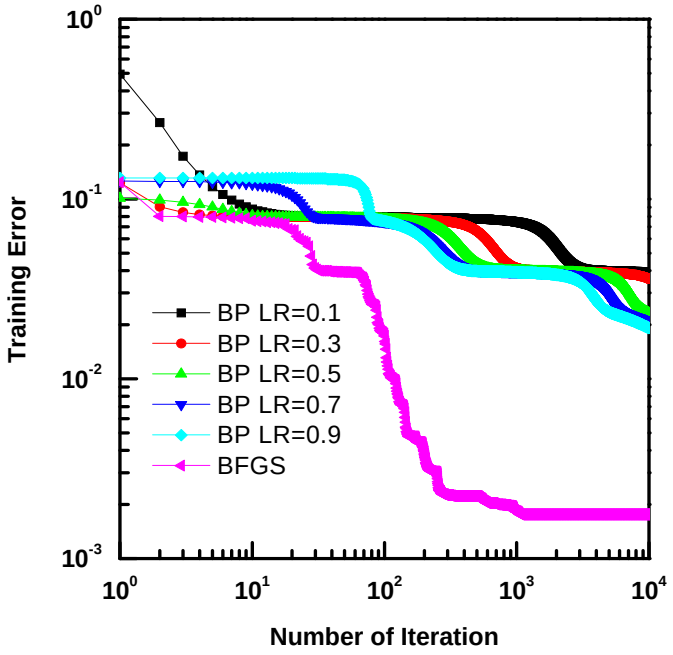


Fig. 4.4: Training error versus number of iterations.

Fig. 4.4 shows the training error with respect to the number of iterations for the BFGS and BP algorithms, both with 5 neurons in the hidden layer. In the BP algorithm, the LR is taken from 0.1 to 0.9 with the same momentum 0.1. It can be seen that the training error for the BFGS algorithm drops to less than 2×10^{-3} after 1000 iterations and has the fastest descent rate compared to all BP algorithms. In contrast, the BP algorithm with the best LR will only reach near 2×10^{-2} after 10000 iterations. The results clearly demonstrate the advantage of a super-linear convergent rate enjoyed by the BFGS algorithm.

4.4.2 Cross-Validation Test

To further compare the performance of these two training algorithms, the r.m.s. error obtained from the cross validation (CV) test with respect to the number of hidden neuron are given in Fig. 4.5 with different LRs from 0.1 to 0.9 for the BP algorithm.

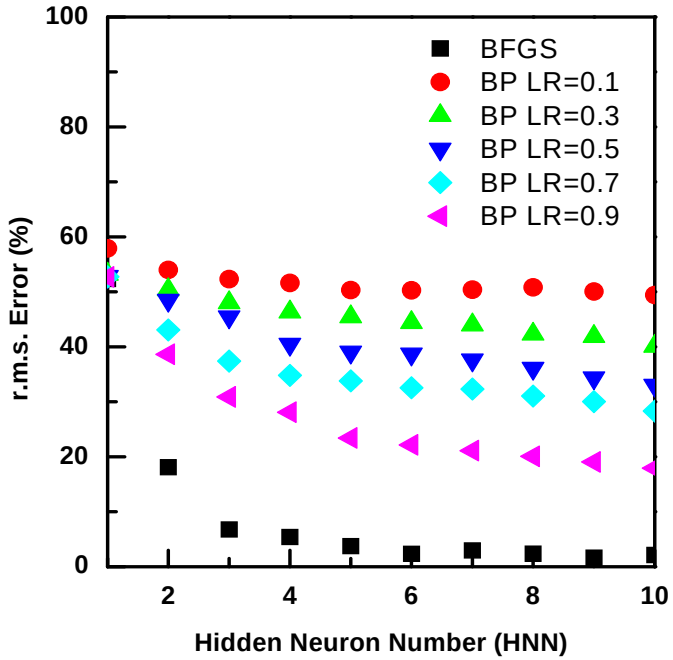


Fig. 4.5: r.m.s. error of the CV test versus HNN.

The number of iterations was set at 1000 for both training algorithms. For the BFGS algorithm, the r.m.s. error drops to less than 5% as the HNN is increased to 5, and a further increase in the HNN does not have much effect in terms of reducing the average error. In contrast, the best CV test result for the conventional BP algorithm (10 HNN and LR = 0.9) shows an r.m.s. error of 18%, which is much higher than the result obtained from the BFGS algorithm. The results unambiguously demonstrate that the BFGS algorithm has a much less CV r.m.s. error compared to the conventional BP algorithm. This is very important as the CV test error represents the generalization ability of the FNN.

4.4.3 Over Fitting Phenomenon

As a larger training error implies that the FNN will be inaccurate even for some training samples (i.e. the FNN possesses poor approximation ability), the training error

thus must be maintained at lower values. To reduce the training error in using the BP algorithm, the conventional method is to increase the number of hidden neurons and/or the training iterations. However, while this will enhance the approximation ability, the generalization ability will generally be weakened. The worst scenario is the so-called over-fitting phenomenon. One of the over-fitting examples is shown in Fig. 4.6, which is observed from the training of the BP based FNN with the network parameters HNN, LR, momentum, and training error restriction set at 20, 0.5, 0.1, and 1×10^{-5}, respectively. It is obvious that over-fitting is a result of the manipulation of the degradation of generalization ability, despite the fact that the training error can reach a very low level of below 10^{-5} after a very large number of training iterations. Over fitting appears mainly because a large HNN brings out too many network parameters of synaptic weights and thresholds (a total of 121 in this case) which is much larger than the number of samples. In contrast, because the BFGS algorithm can very effectively achieve a reasonably low training error with far less hidden neurons, the neural network is more accurate and less prone to over-fitting.

It can be concluded from the simulation results that the BFGS algorithm based FNN possesses great advantages in terms of super-linear convergence, strong approximation and generalization abilities, high accuracy and faster training speed with less prone to over-fitting. This is demonstrated Fig. 5.5 in Chapter Five in which the dependence of etch rate on the O_2 fraction and the D.C. bias has been studied using the BFGS algorithm. This is a typical modeling result out of a three-layer BFGS algorithm based FNN with five hidden neurons, trained with 25 training samples based on five-level Box-Wilson CCD. With this FNN configuration, the overall r.m.s. error and the maximum error were well within 5% and ±10%, respectively.

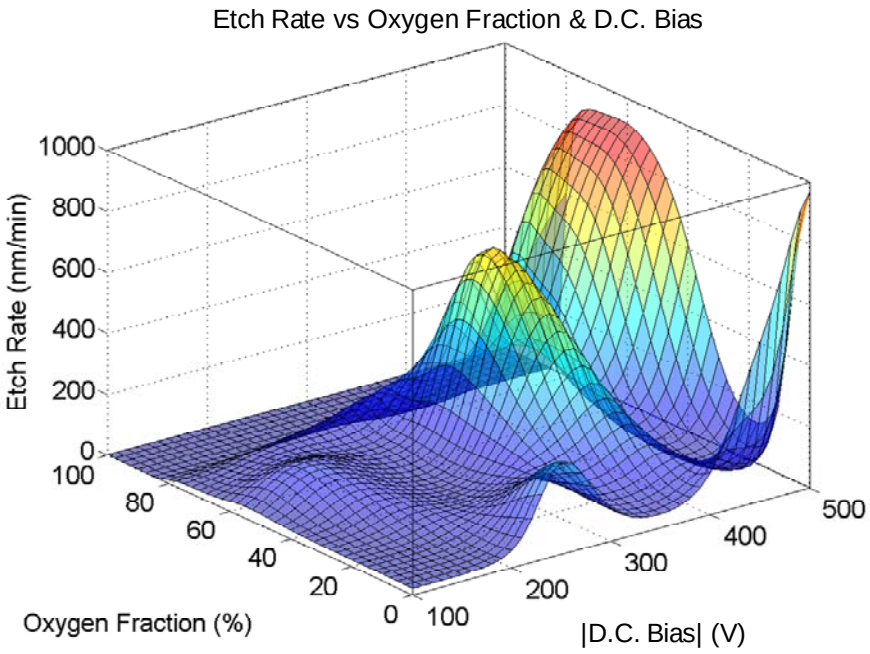


Fig. 4.6: An example of over-fitting phenomenon. The other ECR process parameters are set as 10 sccm total gas flow rate, 5 mTorr process pressure, and 500 W microwave power.

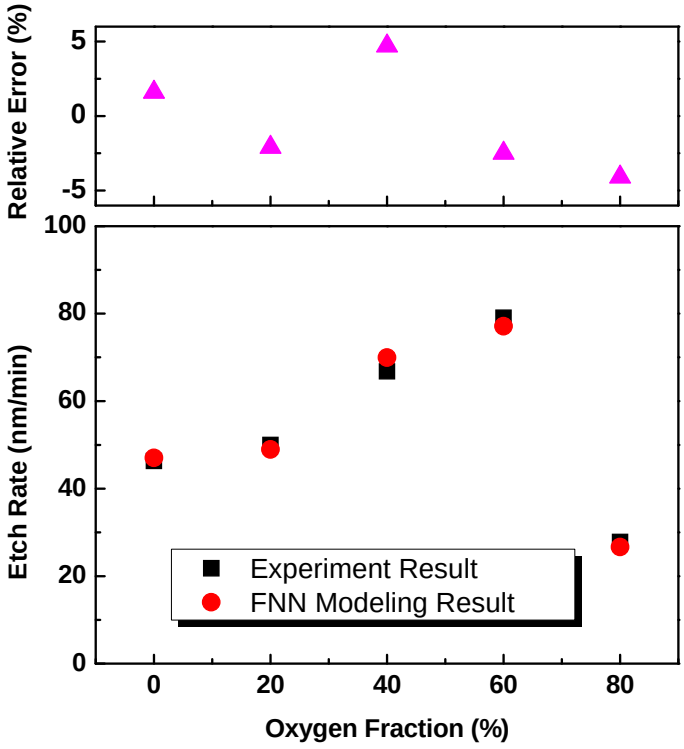


Fig. 4.7: Comparison of etch rate of 4H-SiC as a function of O_2 fraction with the FNN modeling result.

Fig. 4.7 shows the ECR test results of etch rate versus O_2 fraction [105] together with the modeling results obtained using the BFGS algorithm based FNN. The ECR test parameters, i.e. microwave power, D.C. bias, process pressure, total feed-in gas flow rate, were set at 550 W, -200 V, 4 mTorr, and 10 sccm, respectively. The results clearly demonstrate that the modeled etch rates closely match our ECR test results with less than ±5% relative error.

4.5 Summary

In this chapter, a numerical modeling of ECR plasma etching of 4H-SiC using the FNN trained by BFGS optimization algorithm has been developed based on our experimental etch rate results. The modeling results are compared with the results coming from the same FNN and the same experimental data, but trained by conventional BP algorithm with different hidden neuron numbers, different number of iterations and various learning rates. It has been shown that the numerical modeling using the FNN trained by BFGS algorithm can produce better results with less error compared to the conventional BP algorithm. The r.m.s. and the maximum errors of CV testing for the BFGS algorithm are less than 5% and ±10%, respectively, while the errors for training samples are even lower. Therefore, it is sufficiently accurate to provide reliable simulation results to understand the plasma etching mechanism and for practical etching application. The simulated etch rates for 4H-SiC have also been found to be consistent with the experimental results. Therefore, the FNN trained by the BFGS algorithm can be used to develop optimized etching recipes for 4H-SiC for different applications. Using the FNN developed, we have numerically modeled ECR plasma etching of SiC as functions of the O_2 fraction, microwave power, D.C. bias and process pressure. These results will be presented in Chapter Five.

Chapter 5

Electron Cyclotron Resonance Plasma Etching of SiC and Modeling

5.1 Introduction

With increasing demand placed on more advanced applications of SiC in power devices and MEMS, the requirements on etching process control, such as etch depth/etch rate, etch profile, and etching induced damage, are becoming more stringent. Hence, a precise and practical numerical modeling of the etching process is desirable. In addition, modeling helps in understanding the etching mechanism and optimizing the process parameters, while saving the testing sample budget during the research and development stage. Due to the extremely complicated non-linear plasma behavior [22], models that are based on plasma physics and statistics are difficult to derive and less robust. With the advance of computer based artificial intelligence such as artificial neural network techniques, it is possible to simulate the highly nonlinear and complex plasma etching behavior when precise physical equations are not known or too complicated to calculate. To date, neural networks of different paradigms have been widely used in the semiconductor plasma etching processing modeling [67, 75, 97] and real-time control [98, 99]. As one of the most widely used neural network paradigms, the feed-forward neural network (FNN) is composed of a vast number of

parallel simple processing units (neuron) in a layered architecture. We have used the BFGS (Broyden, Fletcher, Goldfarb, and Shanno) optimization algorithm to train the FNN for the modeling of plasma etching of SiC [25], as presented in Chapter four. It was demonstrated that the FNN trained by the BFGS algorithm has better function approximation and generalization ability compared to the conventional BP algorithm, and thus provides more accurate modeling results.

For the plasma etching of SiC, fluorinated gases such as SF_6, CF_4, NF_3, plus various additive gases, normally O_2, Ar, H_2, or other fluorinated gases [23, 106] are widely used as etchant gases. Due to the highly reactive F atoms and the highly volatile etching byproducts, e.g. SiF_4, CF_4 [106], relatively high etch rates with minimum surface contamination can be readily achieved. Furthermore, by varying the O_2 fraction (defined as the ratio of O_2 flow rate to the total gas flow rate), microwave power, D.C. bias, and process pressure, the etching process can be tuned from pure isotropic chemical etching to totally anisotropic physical sputtering. Therefore, the etch rate, etching profile and surface morphology, can be controlled according to different process requirements. Despite the well developed etching process for SiC, to date, the mechanism of plasma etching of SiC is still under debate, especially the roles played by C and O_2 in the etching process [21, 23, 62].

In this chapter, we first present our ECR plasma etching results on n^+ doped 4H-SiC based on SF_6+O_2 plasma, with special emphasis on the role of oxygen in the etching mechanism. The etch rate, surface roughness, and surface contamination are measured and studied. In the second part of this chapter, we present the results of numerical modeling of ECR plasma etching of 4H-SiC with SF_6+O_2 plasma based on the FNN with five hidden neuron trained by the BFGS algorithm developed in Chapter

four [25]. The modeling results are presented in terms of etch rate versus O_2 fraction, microwave power, D.C. bias and process pressure and discussed in terms of their physical and chemical mechanisms. The ultimate goal is to achieve an in-depth understanding of the complex ECR plasma etching behaviors of 4H-SiC through virtual means of simulation, and this knowledge will be useful in controlling real etching process of SiC.

5.2 Experimental Setup

The detailed configuration of the ECR plasma reactor used for the study and the sample preparation can be found in Chapter Four.

A series of etching experiments was carried out by varying the O_2 fraction from 0 to 80%, while keeping the microwave power, D.C. bias, total gas flow rate, process pressure, and etching duration constant at 550 W, -200 V, 10 sccm, 4 mTorr, and 30 minutes, respectively. The morphology of the etched pattern was characterized using a LEO 982 scanning electron microscope (SEM). The etch depth was measured with a Dektak^3 ST stylus surface profilometer. The etched surface roughness was characterized by a Shimadzu SPM-9500J2 atomic force microscopy (AFM), and the surface element analysis was performed using a JEOL JAMP 7800F Auger electron spectrometry (AES).

5.3 ECR Plasma Etching Test Results and Discussion

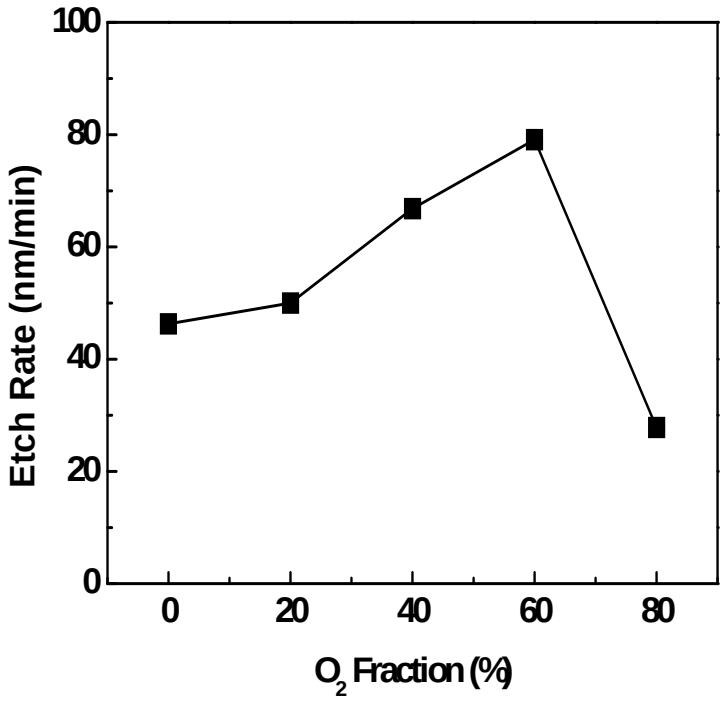


Fig. 5.1: The etch rate versus O_2 fraction.

Fig. 5.1 shows the etch rate as a function of the O_2 fraction. It increases from 46.3 to 79.1 nm/min with O_2 fraction up to 60%, after which it decreases sharply to 27.8 nm/min at an O_2 fraction of 80%. The change in the etch rate is not directly related to physical ion bombardment as the D.C. bias was kept constant in the experiments. The initial increase in the etch rate is attributed to the larger O_2 fraction that results in the releasing of more F neutral radical atoms [23]. In addition, the presence of a higher oxygen atomic concentration at increasing O_2 fraction has been reported to enhance the carbon etch rate by chemical reactions to form volatile by-products like CO and CO_2 and hence increase the etch rate [23]. However, as will be seen in our work, the role that oxygen plays in the etching of carbon is insignificant. The subsequent decrease in the etch rate at larger O_2 fraction is attributed to the

Element	C	N	O	F	Si	Al	C/Si Ratio
Relative Sensitivity Factor (RSF)	0.128	0.158	0.371	0.954	0.137	0.309	
Unetched Control Sample (UCS)		-	2	-	54	-	0.815
0% O_2	47	-	2	3	48	-	0.979
20% O_2	43	1	3	3	50	-	0.860
40% O_2		-	3	2	51	-	0.863
60% O_2	40	-	4	2	54	-	0.741
80% O_2	40	-	8	2	50	-	0.800

Table 5.1: The relative concentration of surface elements in arbitrary unit.

dilution of fluorine atom concentration, and the formation of an oxide-like layer as evidenced from the AES results as shown in Table 5.1.

The relative concentrations of the different elements on the etched surface, as determined using AES, are listed in Table 5.1. Contrast to the unetched control sample, all the etched samples are found to have F residue, arising from the fluoride gas plasma used for the etching. Besides, with increasing the O_2 fraction from 0 to 80%, the O concentration increases from about 2%, which is likely attributed to oxygen in the ambient, to 8%. This increase is due to the chemisorption of oxygen onto the SiC surface during the plasma etching process.

Regarding the role of O_2 in the etching reaction with carbon, if oxygen does react with carbon chemically and efficiently, especially at higher O_2 fractions, then that should engender some silicon-rich layer due to the silicon etch rate being weakened by the dilution of fluorine concentration and the presence of an oxide-like layer. However, the results in Table 5.1 do not suggest the presence of a silicon-rich

layer, even at high O_2 fractions. Therefore, it is suggested that O_2 does not play a significant role in the chemical etching of carbon. It is interesting to note that in a similar study, F. Lanois et al [62] found the existence of a carbon-rich layer irrespective of the O_2 flow rate (SF_6 flow rate was kept constant), which is not observed in our case. The only notable difference between their experiments and ours is their much lower D.C. bias of -37V, compared to -200V used in our work. Therefore, it can be concluded that physical ion bombardment plays a significant role in the etching of carbon [21].

Fig. 5.2 shows the root mean square (r.m.s.) surface roughness extracted from the AFM scanning of etched surfaces over an area of 10×10 μm^2. The results of oxygen surface relative concentration deduced from AES are also shown. It is seen that the surface roughness increases moderately from 1.07 to 1.72 nm with increasing the O_2 fraction. A similar trend has been observed and studied [107, 108], and is attributed to surface oxidation [91]. The surfaces etched at lower O_2 fractions ($\leq$60%) are smoother than the unetched control sample with an r.m.s. roughness of 1.48 ± 0.09 nm. This is because at high SF_6 fractions, the SiC surface chemical reactions with F atoms dominate, which tends to smoothen the surface [96]. The increase in the oxygen surface relative concentration with the O_2 fraction as shown Fig. 5.2 is attributed to chemisorption or to the residues from ion bombardment. This suggests the presence of an oxide-like layer when etching at high oxygen fractions.

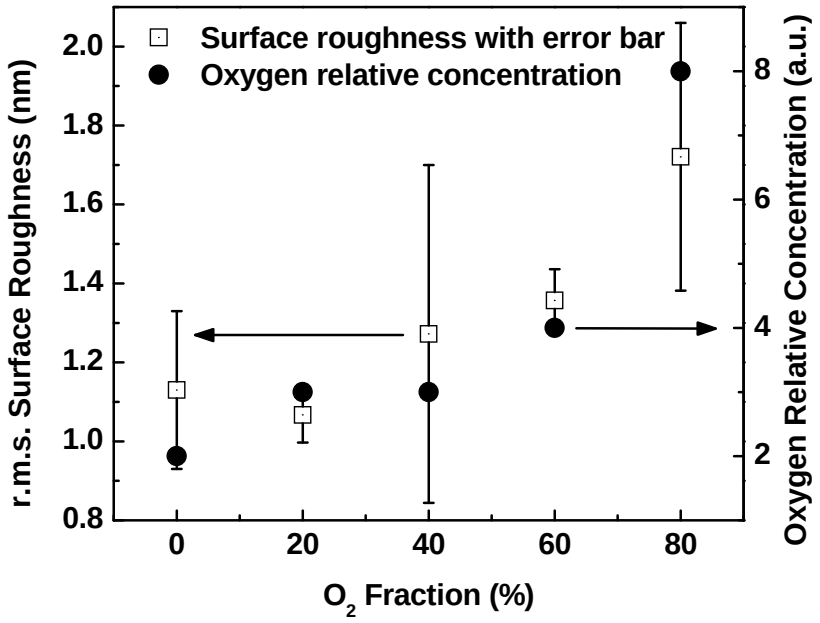


Fig. 5.2: r.m.s. surface roughness and oxygen surface relative concentration versus O_2 fraction.

Fig. 5.3 and Fig. 5.4 show the AFM and SEM micrographs of the etched surface profile at 0% O_2 fraction. Beside some defects observed at the sidewall which are due to the mask defects, the etched surface profile appears smooth and free of micro-trench effects. No spikes and blackened etched surfaces, usually induced by Al clusters [82, 109] and/or carbon rich-layer [109], are observed. As confirmed from the AES results, the etched surfaces are free of metal contamination and of any carbon rich-layer, as indicated by the C/Si ratio. This may be attributed to the high D.C. bias used that prevents the formation of Al clusters at the surface. It also enhances the carbon etch rate and prevents the formation of a carbon rich-layer [109].

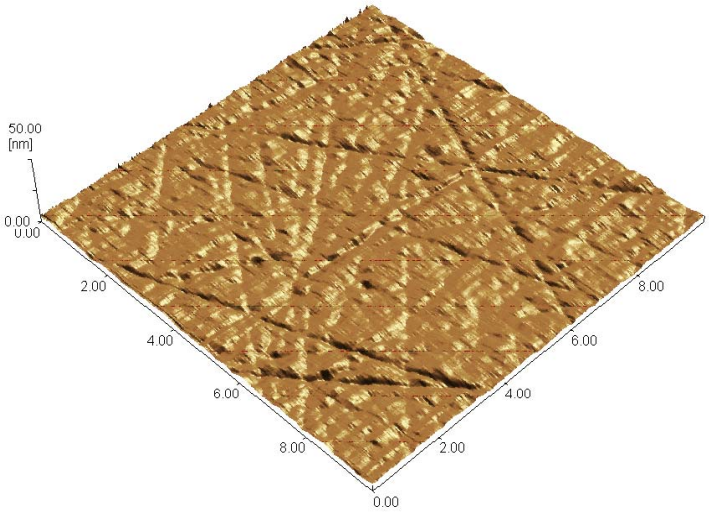


Fig. 5.3: A typical AFM micrograph of surface etched at 0% O_2 fraction (r.m.s. surface roughness is 1.13 nm).

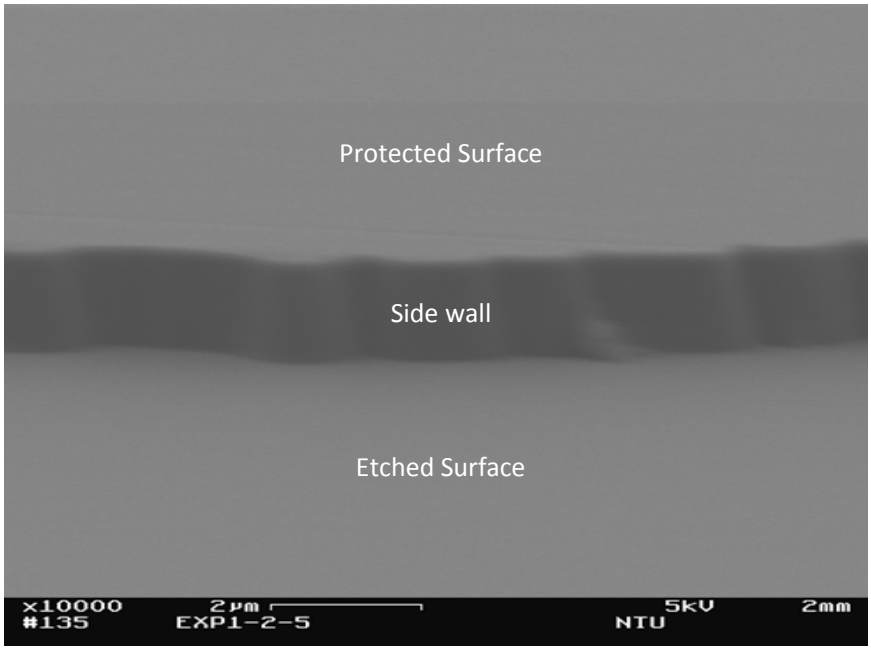


Fig. 5.4: A typical surface profile SEM micrograph etched at 0% O_2 fraction for 30 minutes.

5.4 Modeling Results and Discussion

5.4.1 Training Sample Set

The modeling of ECR plasma etching of 4H-SiC is based on our physical etching test results. The detailed ECR plasma etching test and the sample preparation can be found in Chapter Four. The training samples were selected strictly based on a five-level Box-Wilson central composite design (CCD) (see Appendix A) [104]. Four ECR plasma process parameters, namely O_2 fraction, microwave power, D.C. bias, and process pressure, were varied to study their effects on the etch rate. According to the five-level Box-Wilson CCD, the sample size required for a four-factor DOE is 25. The detailed DOE together with the FNN numerical simulation results and their relative errors in percentile compared with the experimental results are listed in Table 5.2.

By comparing the error calculated using Eqn. (4.4) for the 25 training samples and 25 cross-validation samples with different hidden neuron numbers (from 1 to 10), it has shown in Chapter four that the best strategy is to use 5 hidden neurons in the FNN trained by BFGS algorithm with 1000 iterations. An r.m.s. error less than 5% and a maximum error less than ±10% have been achieved, which are sufficiently accurate for providing reliable simulation results to understand the plasma etching mechanism and for practical etching application.

By using the properly trained FNN, we can give different input values to the network to get the corresponding outputs through the input-output relation shown in Eqs. (4.1)-(4.3), and the simulation results are thus obtained. As the relationship between the etch rate and the four parameters cannot be easily presented, we will use

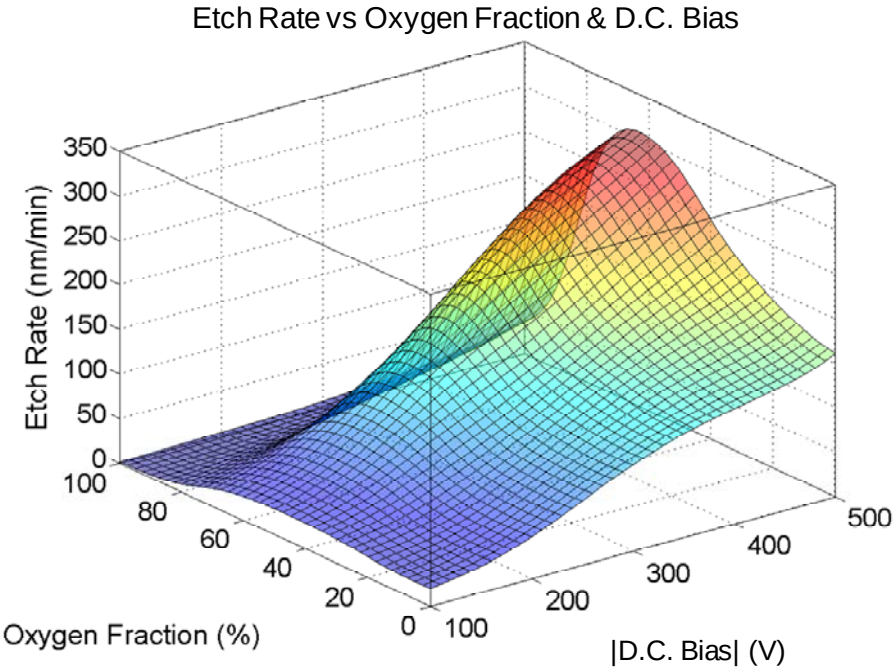
No	O_2 Fraction [%]	Microwave Power [W]	|D.C. Bias| [V]	Pressure [mTorr]	Etch Rate [nm/min]	Simulated Etch Rate [nm/min]	Relative Error [%]
1	20	400	200	5	47.6	47.92	0.67
2	60	400	200	5	58.0	57.82	-0.31
3	20	800	200	5	66.4	66.94	0.81
4	60	800	200	5	108.0	108.32	0.3
5	20	400	400	5	138.4	137.61	-0.57
6	60	400	400	5	210.2	209.72	-0.23
7	20	800	400	5	271.6	269.48	-0.78
8	60	800	400	5	367.2	364.92	-0.62
9	20	400	200	11	49.7	50.2	1.01
10	60	400	200	11	35.9	35.94	0.11
11	20	800	200	11	81.6	81.39	-0.26
12	60	800	200	11	113.5	113.97	0.41
13	20	400	400	11	196.4	194.83	-0.8
14	60	400	400	11	177.9	177.93	0.02
15	20	800	400	11	379.8	377.6	-0.58
16	60	800	400	11	397.4	394.82	-0.65
17	40	600	300	8	148.2	147.71	-0.33
18	0	600	300	8	137.6	137.42	-0.13
19	80	600	300	8	47.2	48.13	1.97
20	40	200	300	8	103.2	102.97	-0.22
21	40	1000	300	8	285.0	282.75	-0.79
22	40	600	100	8	32.4	32.88	1.48
23	40	600	500	8	422.3	419.47	-0.67
24	40	600	300	2	82.5	82.07	-0.52
25	40	600	300	14	93.6	94.26	0.71

Table 5.2: Training sample set designed by five-level Box-Wilson CCD and the FNN numerical simulation results with their relative errors in percentile compared with the experimental results.

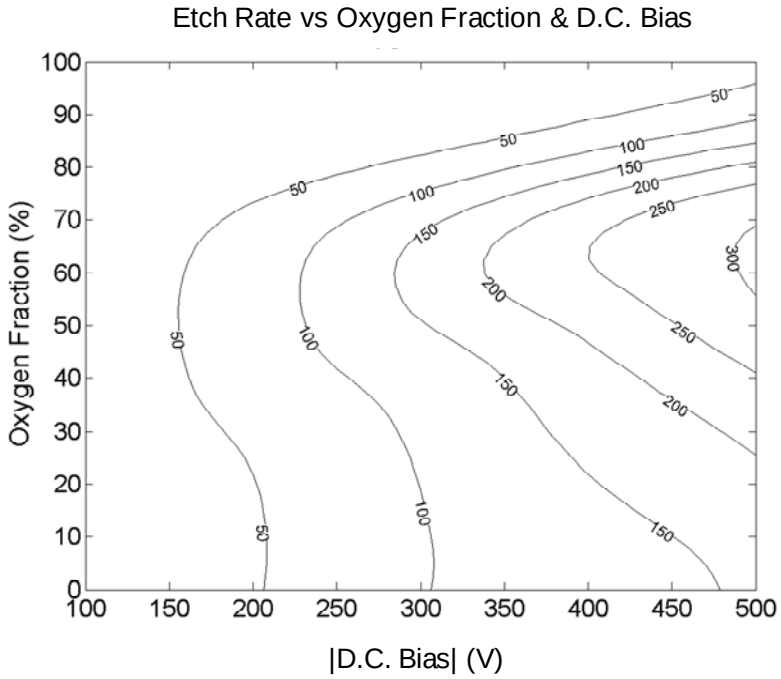
3D surface plots and 2D contour plots to depict the relations between the etch rate and two specific parameters while keeping the other two parameters constant. The simulation results will be given in the following sections.

5.4.2 Etch Rate Versus O_2 Fraction and D.C. Bias

The simulation results of the etch rates dependence on the O_2 fraction and D.C. bias are shown in Fig. 5.5 (a) and (b) in a 3D surface plot and 2D contour plots,



(a)



(b)

Fig. 5.5: Etching rate versus oxygen fraction and D.C. bias with microwave power and process pressure setting at 550 W and 4 mTorr, respectively. (a) 3-D plot; (b) 2-D contour plot of Fig. 5.5 (a).

respectively. The other two process parameters, the microwave power and the process pressure are fixed at 550 W and 4 mTorr, respectively. As can be seen from the figure, at every D.C. bias, there exists an optimum O_2 fraction at which the etch rate reaches a maximum. This maximum etch rate is also noted to be more prominent at higher D.C. bias values. The O_2 fraction at which the maximum etch rate occurs is affected by the D.C. bias, and it changes from about 47.5% at -100 V to 62.5% at -500 V, as clearly shown in Fig. 5.6. This simulation results are consistent with our experimental results in this chapter [105].

The role of oxygen in the plasma etching of SiC is still under investigation [21, 23, 62, 107]. Conventional explanations attribute the change in the etch rate with varying the O_2 fraction to the effects of neutral radicals F and O. F is the main etchant that reacts with silicon and carbon from SiC to form volatile products SF_m, and CF_m (m=1 ~ 4).

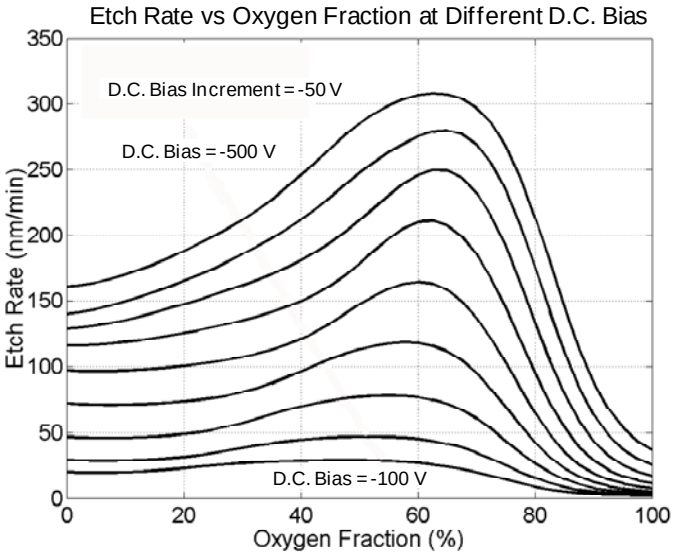


Fig. 5.6: Etching rate versus oxygen fraction at different D.C. bias values with microwave power and process pressure setting at 550 W and 4 mTorr, respectively.

The introduction of O_2 as an additive is believed to have multiple effects on the etching behavior [107]. Firstly, at low O_2 fraction, the addition/presence of O atoms helps to increase the concentration of F atoms by reacting with unsaturated fluoride species to release F neutral radicals, while depleting those polymer-forming species that will reduce F concentration [23]. Therefore, initially the etch rate increases with the O_2 fraction. However, when the O_2 fraction becomes substantially large, it will dilute the F concentration and decrease the etch rate, assuming that the total gas flow rate is kept constant. In addition, the formation of an oxide-like layer at higher O_2 fractions will reduce the availability of silicon and further lower the etch rate. Therefore, there exists a peak in the etch rate as seen in Fig. 5.5 and Fig. 5.6, at some intermediate oxygen fraction levels.

The direct role of oxygen atoms in the chemical etching of carbon, as proposed by some research groups, is still under debate [21, 23, 62, 107]. With the support of in-line plasma diagnosis tests, e.g. using optical emission spectroscopy (OES), it was shown that there exist C-based gaseous species (e.g., CO, CO_2, and COF_2.) in the reaction chamber [110], which suggests that C in SiC can react directly with O to form volatile byproducts, e.g. CO and CO_2 [23]. On the other hand, it was also proposed that C is being etched through physical sputtering [62]. Nevertheless, in either way, the existence of a carbon rich layer even at higher O_2 fractions [23] suggests that such a role of oxygen, if it exists, is inefficient and insignificant.

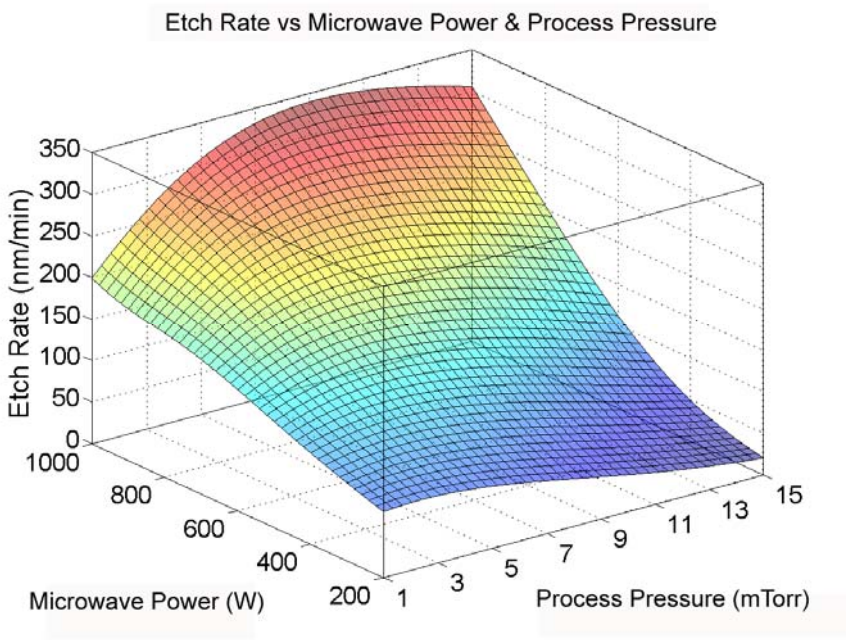
Our previous results [105] indicated that an oxide-like layer was formed by chemisorption of oxygen at the SiC surface. The oxide-like layer acts as an inhibiter layer and blocks F atoms from reaching the SiC surface. Hence it lowers the effective F available and reduces the etch rate of SiC. As this oxide-like layer is believed to be

etched away mainly through physical sputtering, therefore, its effectiveness in inhibiting the etching of SiC is affected by the applied D.C. bias. With increasing the D.C. bias, it is observed there is an increase in the O_2 fraction at which the maximum etch rate is achieved, from 47.5% at -100 V to 62.5% at -500 V. As the oxide-like layer is sputtered under strong ion bombardment, more F atoms are able to reach the SiC surface. Assuming that the maximum concentration of F atoms occurs at an oxygen fraction beyond 62.5%, therefore we expect more F atoms to be available for etching at higher D.C. bias and higher oxygen fraction, as seen in the results obtained. The etch rate is also noted to saturate at high D.C. bias, which could be due to limited chemical etching species of F neutral radical, whose generation becomes the bottleneck of the overall etching process. The highest etch rate achieved at -500V D.C. bias and about 62.5% O_2 fraction is about 308.2 nm/min. It should be noted that the high D.C. bias might bring about some undesirable effects, e.g., damaged etched surface, deteriorating yield, reduced selectivity of mask.

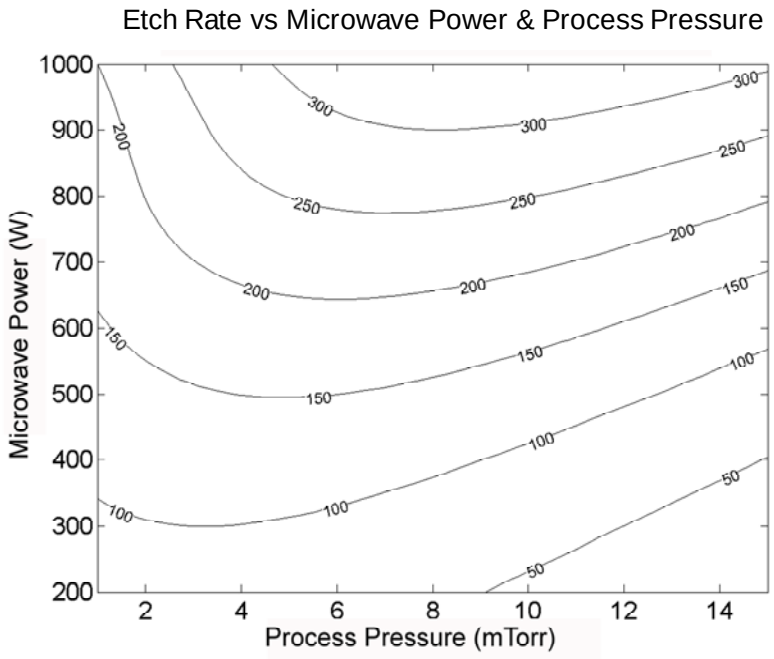
5.4.3 Etch Rate Versus Process Pressure and Microwave Power

Fig. 5.7 (a) and (b) show the simulation results of etch rate with respect to the process pressure and microwave power in 3D surface plot and 2D contour plots, respectively. The D.C. bias and the O_2 fraction are fixed at -300 V and 60%, respectively. A maximum etch rate is observed as a function of process pressure at different levels of microwave power investigated. With an increase in the microwave power, the maximum etch rate increases and occurs at higher process pressure. As shown in

Fig. 5.8, as the microwave power increases from 200 to 1000 W, the process pressure corresponding to the maximum etch rate shifts significantly from around 2.4



(a)



(b)

Fig. 5.7: Etch rate versus process pressure and microwave power with oxygen fraction and D.C. bias setting at 60% and -300 V, respectively. (a) 3-D plot; (b) 2-D contourplot.

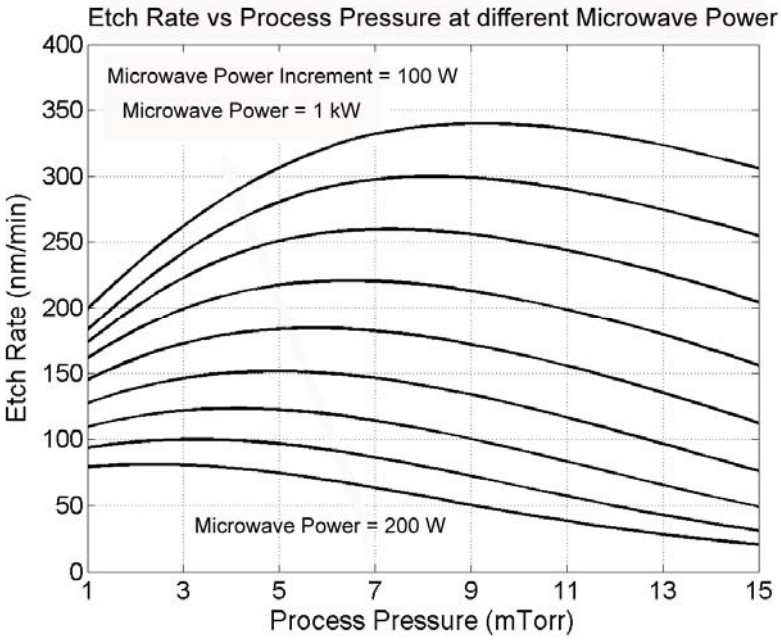


Fig. 5.8: 2D plot of etch rate versus process pressure at different microwave power with oxygen fraction and D.C. bias setting at 60% and -300 V.

to 9 mTorr. Correspondingly, the maximum etch rate peak increases from 81.3 nm/min at 200 W microwave power to more than 340 nm/min at 1000 W microwave power.

The initial increase in the etch rate with process pressure is due to an increase in the etchant gas concentration, which is the rate limiting factor in determining the overall etch rate. A maximum etch rate is reached when the limiting factor is changed from the etchant concentration to impinging positive ion flux and impact energy. The decrease in the etch rate at higher process pressure is attributed to the combined effects of electron temperature, neutral radical densities, positive ion energy, density and flux [111]. At high process pressure, the average electron temperature will drop due to the shorter electron mean-free-path. As a result, the electron-molecule impact ionization rate will decrease. Together with the increasing recombination rate of ions and the shortening of ion mean-free-path, both the energy and concentration of the positive ions will decrease. This eventually will become the rate limiting factor that reduces the

etch rate, despite an increase in F concentration with the process pressure because of the increasing overlap between elementary reaction cross sections and electron energy distribution functions [111].

With increasing microwave power, the plasma density is increased and the higher impinging positive ion flux will result in a higher etch rate. However, as can be seen from the simulation results, at low process pressure, e.g. 1 mTorr, the increase in the etch rate with microwave power is less compared to that at higher process pressure. Besides, at lower process pressure the etch rate appears to be slightly saturated at higher microwave power. This can be explained as at low process pressure, the etchant availability is the limiting factor that constrains the etch rate from increasing with the microwave power. Under higher microwave power when a larger positive ion flux is generated, the etching mechanism will be more limited by the etchant concentration rather than the ion flux. This explains the observation that the maximum etch rate occurs at higher process pressures at higher microwave powers, as the pressure range over which the etching is limited by the etchant concentration is enlarged.

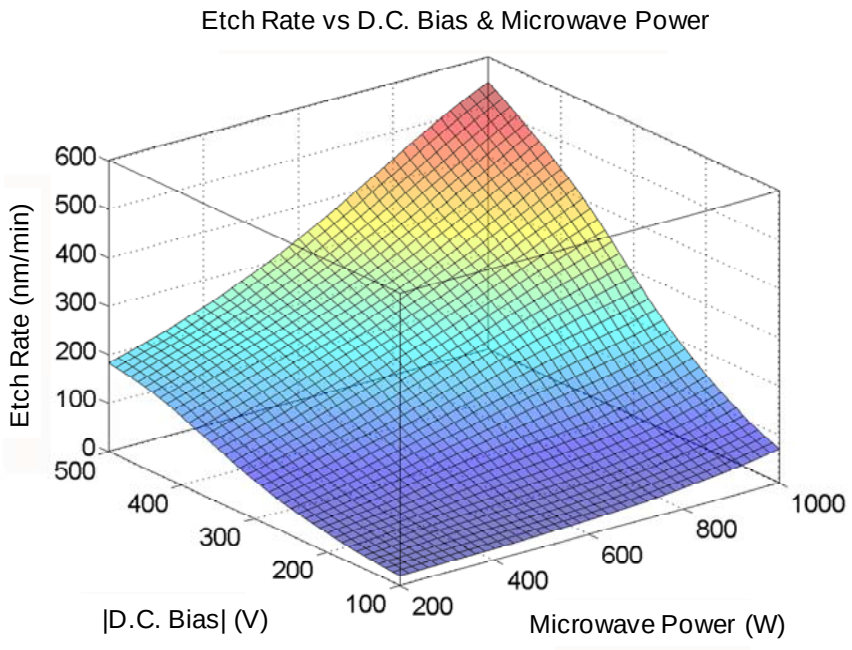
The highest etch rate obtained here is very much suitable for applications such as mesa etching, etc, which require high etch rate but less etching induced damage. This is because the increase in the etch rate is the result of increasing neutral radicals and higher positive ion density and hence higher impinging ion flux. When the impinging positive ion energy is controlled under certain level by adjusting the bias, high etch rate can be achieved with controlled etching induced damage.

5.4.4 Etch Rate Versus Microwave Power and D.C. Bias

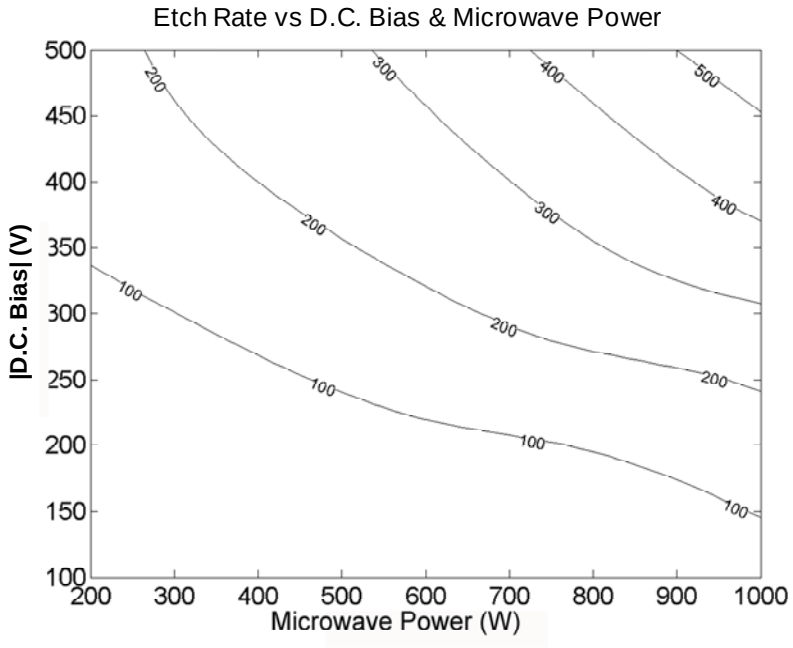
Shown in Fig. 5.9 (a) is the 3-D surface plot of etch rate with respect to the microwave power and D.C. bias, and in Fig. 5.9 (b) its contour plot. The other

parameters, the process pressure and the O_2 fraction are set at 4 mTorr and 60%, respectively. This simulation results are used to examine the combined effects of microwave power and D.C. bias on the etch rate. It is clearly shown that both the microwave power and D.C. bias significantly affect the etch rate of SiC. The etch rate increases with the microwave power, with the rate of increase being steeper under higher D.C. bias values. Similarly, the etch rate also increases with the D.C. bias, with a steeper rate of increase being observed at higher microwave power level.

The simulation results can be understood based on the mechanism of damage-induced ion assisted plasma etching [23]. Positive ion bombardment plays multiple roles in assisting and enhancing the etching process. Firstly, it will bombard the surface, break the strong chemical bonds, such as Si-C and C-C bonds, amorphize the unprotected surface and make it more chemically active. Secondly, it will knock out the etching by-products and oxide-like layer formed due to the chemisorption. The chemical etching by the neutral species, i.e. F, is still dominant in the overall etching process with the assistance of positive ion bombardment. At lower D.C. bias, the increase in the etch rate with microwave power is quite limited. This is because even at larger microwave power, which results in an increase in the concentration of both the F atoms and positive ions, the impinging ion energy (which is mainly controlled by the D.C. bias) remains low. This makes the positive ion bombardment process a limiting factor that prevents the etch rate from increasing with the microwave power. Similarly, at lower microwave power, a higher D.C. bias only brings about a moderate increase in the etch rate. This is due to the limited availability of the neutral etchant F



(a)



(b)

Fig. 5.9: Etch rate versus D.C. bias and microwave power with oxygen fraction and process pressure setting at 60% and 4 mTorr, respectively: (a) 3-D plot; (b) 2-D contour plot.

atoms and positive ions that limits the increase in the etch rate. However, when both the microwave power and D.C. bias are increased, a much stronger increase in the etch rate is observed.

There is a slight saturation in the etch rate observed at larger microwave power with increasing D.C. bias. Similar to the results shown in Fig. 5.5, it is due to the limited F supply, which is now the rate limiting factor. In contrast, no saturation trend has been observed in the relationship between the etch rate and microwave power at any given D.C. bias. It is believed that with increasing microwave power, both the concentrations of positive ions and neutral etchant F atoms will increase and result in a higher etch rate.

The highest etch rate achieved at 1000 W microwave power and -500 V D.C. bias is about 548.9 nm/min. This is especially useful for the etching of microelectromechanical systems (MEMS) or via hole formation for power electronic devices. It provides a highly anisotropic etching with high etch rate, which are needed to ensure a reasonable etching time for deep etching with a high aspect ratio, with less consideration for etching induced damage.

5.5 Summary

In this chapter, we first studied the role of oxygen in the SF_6-O_2 ECR plasma etching of n^+ doped bulk 4H-SiC. The AES results suggest that the chemical etching of carbon by oxygen is not significant even at high O_2 fraction. The surface roughness was found to increase with the O_2 fraction, due to surface oxidation and oxygen ion related physical ion bombardment. However, even at the highest O_2 fraction, relatively smooth etched 4H-SiC surfaces free of Al cluster and C rich-layer were observed,

which is attributed to the high D.C. bias applied. The etch rate as high as 78.1 nm/min with an r.m.s. surface roughness of 1.48±0.09 nm can be achieved at 60% O_2 fraction, 550 W microwave power, -200V D.C. bias and 4 mTorr process pressure.

Secondly, ECR plasma etching of 4H-SiC with SF_6+O_2 plasma has been numerically modeled using the FNN trained by the BFGS optimization algorithm. An overall r.m.s. error and a maximum error of less than 5% and ±10%, respectively, have been achieved, which are sufficiently accurate for providing reliable simulation results to understand the 4H-SiC plasma etching mechanism and for practical etching application. The etching behavior of ECR was studied with varying process parameters which include microwave power, D.C. bias, process pressure and O_2 fraction. The modeling results of the etch rate were analyzed using 3-D surface plots and 2-D contour plots. It is found that by varying O_2 fraction and process pressure, optimized etch rate peaks can be achieved. Increasing the D.C. bias and microwave power results in optimized etch rate peaks occurring at higher O_2 fraction and process pressure, respectively, while at the same time augmenting the etch rate. However, there is a saturation in the etch rate at higher D.C. bias values, which however, does not occur at higher microwave power. The simulation results clearly demonstrated the relationship between the etch rate and the process parameters such as the microwave power, D.C. bias, process pressure and O_2 fraction, and their combined effects in terms of the contributions of pure chemical reactions and physical ion bombardment (sputtering) to the overall etching behavior. The modeling results suggest that by controlling these process parameters, it is possible to develop optimized etching recipes for SiC that can cater for different applications.

Appendix A Box-Wilson Central Composite Design [104]

Box-Wilson Central Composite Design (CCD) is a design of experiments (DOE) for fitting quadratic models of response surface methodology (RSM). A standard Box-Wilson CCD consists of a 2^k factorial design (k is the factor number) with a few center points and a group of $2k$ star points. Fig. 5.10 shows the Box-Wilson CCD with three factors (k=3). From Fig. 5.10, it is clear that each factor of Box-Wilson CCD has five levels. Hence, the total sample size for a k factors Box-Wilson CCD is 2^k+2k+N_C, where N_C is the number of center points.

In our Box-Wilson CCD for our FNN modeling of ECR plasma etching of SiC, there are four factors, namely, O_2 fraction, microwave power, D.C. bias, and process pressure. Therefore, the sample size is $2^4+2\times4+1=25$. Here only one center point number was chosen. For a four factors (x1, x2, x3, and x4) Box-Wilson CCD, all the 25 samples can be determined as listed in Table 5.3.

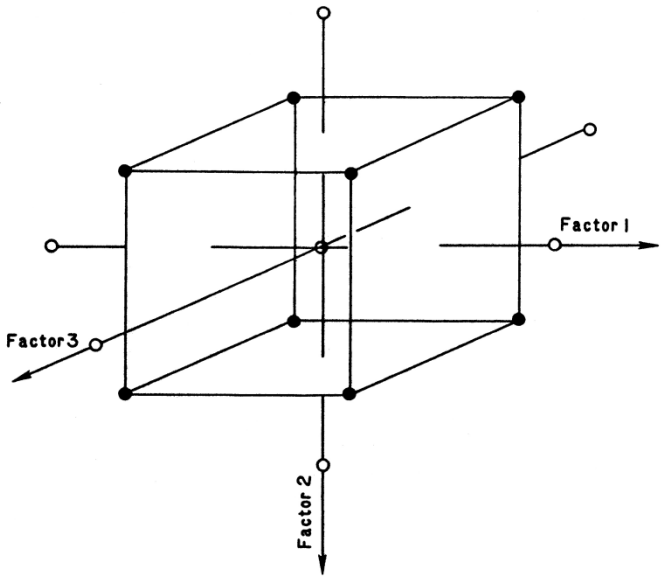


Fig. 5.10: The Box-Wilson central composite design (CCD) with 3 variables.

No.	x1	x2	x3	x4	No.	x1	x2	x3	x4
1	-1	-1	-1	-1	14	1	1	-1	1
2	-1	-1	-1	1	15	1	1	1	-1
3	-1	-1	1	-1	16	1	1	1	1
4	-1	-1	1	1	17	$-\alpha$	0	0	0
5	-1	1	-1	-1	18	α	0	0	0
6	-1	1	-1	1	19	0	$-\alpha$	0	0
7	-1	1	1	-1	20	0	α	0	0
8	-1	1	1	1	21	0	0	$-\alpha$	0
9	1	-1	-1	-1	22	0	0	α	0
10	1	-1	-1	1	23	0	0	0	$-\alpha$
11	1	-1	1	-1	24	0	0	0	α
12	1	-1	1	1	25	0	0	0	0
13	1	1	-1	-1					

Table 5.3: The list of 25 samples of a four-factor, five-level Box-Wilson CCD.

In Table 5.3, "±1" represents the distance from center of the design space to a factorial point for a factor and "±α" represents the distance from the center of the design space to a star point for a factor. In order to make the design to have circular, spherical, or hyper-spherical symmetry, α can be determined as:

$$\alpha = \left(2^k\right)^{1/4} \tag{5.1}$$

Hence, in our Box-Wilson CCD, $\alpha = (2^4)^{1/4} = 2$. The center point of our Box-Wilson CCD was set to the medium values of the practical adjusting range of the process parameters. ±α presents the lowest and highest values of the process parameters within the practical adjusting ranges. The process parameters corresponding to "±1", "±α", and the center point are listed in Table 5.4.

	O_2 Fraction [%]	**Microwave Power [W]**	**|D.C. Bias| [V]**	**Process Pressure [mTorr]**
Center Point	40	600	300	8
-1	20	400	200	5
1	60	800	400	11
$-\alpha$	0	200	100	2
α	80	1000	500	14

Table 5.4: The list of process parameters corresponding to "±1", "±α", and the center point.

Chapter 6

Study of Plasma Etching Induced Damage Using SiC Schottky Barrier Diode

6.1 Introduction

It is well known that reactive ion etching of SiC will in general bring about several kinds of damage to its etched surface. These include surface contamination, changing surface stoichiometry, surface dopant passivation, point defects in the lattice leading to amorphous surface [112]. In general, it is believed that in order to reduce plasma etching induced damage (PEID), the D.C. self-bias has to be lowered to reduce physical ion bombardment. However, the outcomes are never straightforward as there is no simple relationship that exists between PEID and the D.C. self-bias [113, 114]. To effectively reduce or even eliminate PEID, it is necessary to understand how the two resultant effects of the RIE process, i.e. physical sputtering and chemical etching, will lead to SiC damages.

In this chapter, *n* type 4H-SiC Schottky barrier diodes (SBDs) are used as test vehicle for studying PEID. The reason for using SBDs is that their electrical characteristics are very sensitive to the quality of the metal-semiconductor (MS) interface, which in turn is determined by the damage that may result from the etching process. Three sets of experiments, with the samples subjected to mainly chemical

etching (CE), physical sputtering (PS) and their combination (CE+PS), are designed to understand the damages that are resulted from these processes. The electrical characteristics of the SBDs studied include capacitance-voltage (*C-V*), current-voltage (*I-V*), and deep level transient spectroscopy (DLTS). Through this study, we aim to understand PEID in relation to the etching plasma characteristics, and propose how it can be minimized through controlling the plasma process parameters.

6.2 Fabrication of Schottky Barrier Diode

The fabrication process for 4H-SiC SBDs to study PEID involves two parts, sample preparation and plasma etching tests.

6.2.1 Sample Preparation

Fig. 6.1 illustrates schematically the fabrication process for 4H-SiC SBDs. The SBD samples were fabricated on 5×5 mm^2 chips of N doped 4H-SiC n^+ substrate with a 10 μm thick n^- epitaxial-layer. These samples were cut from 2" Si faced SiC wafers purchased from CREE Research. The orientation of the 4H-SiC is 8° off-axis of $\langle 0001 \rangle$ pointing towards $\langle 11\bar{2}0 \rangle$. The doping levels of the n^- epitaxial-layer and n^+ substrate are 2×10^{15} cm^{-3} and $>1\times10^{19}$ cm^{-3} respectively. The steps involved in the fabrication process are as follows:

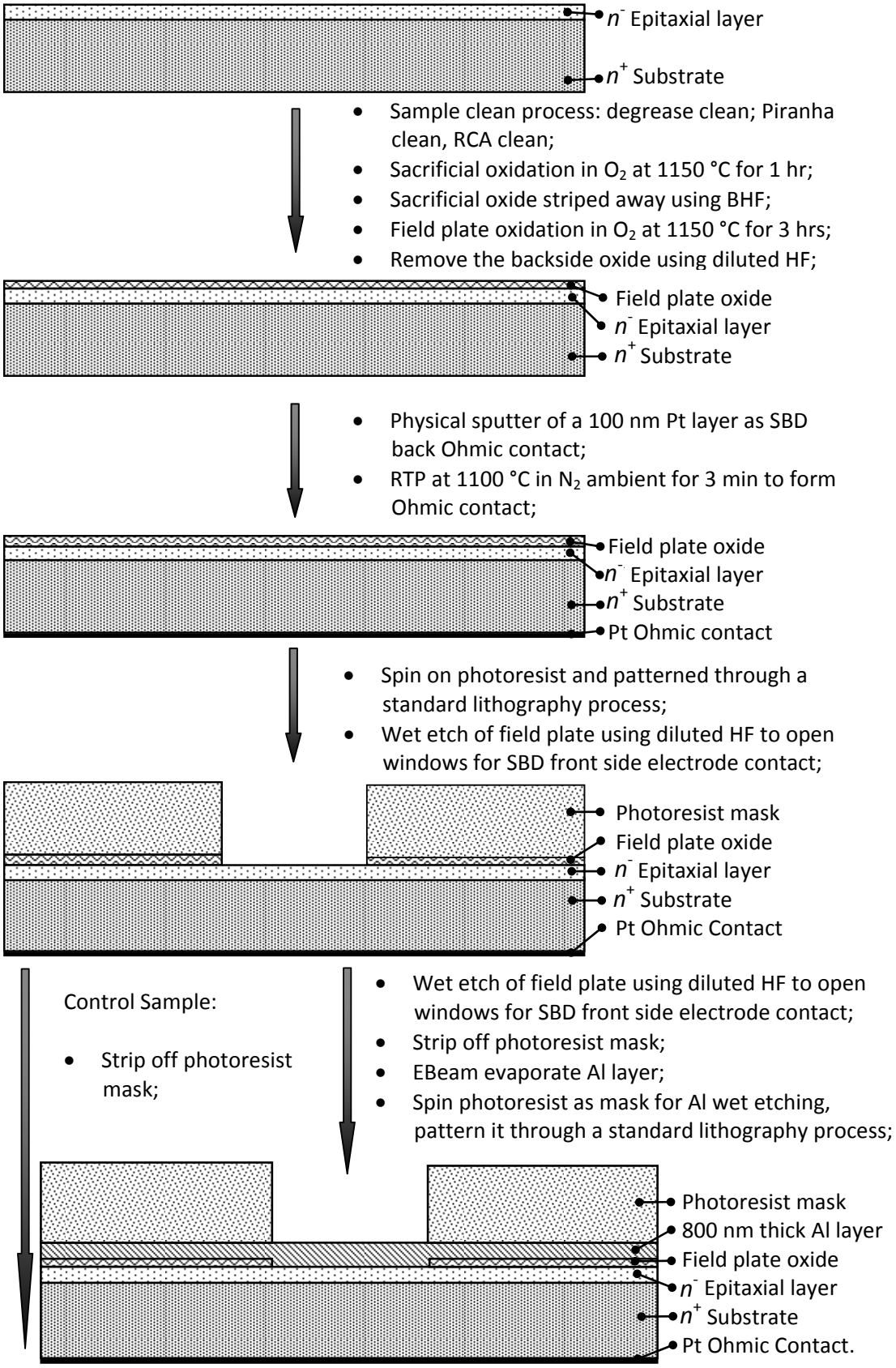


Fig. 6.1: Schematic Process Flow for the Fabrication of 4H-SiC SBDs.

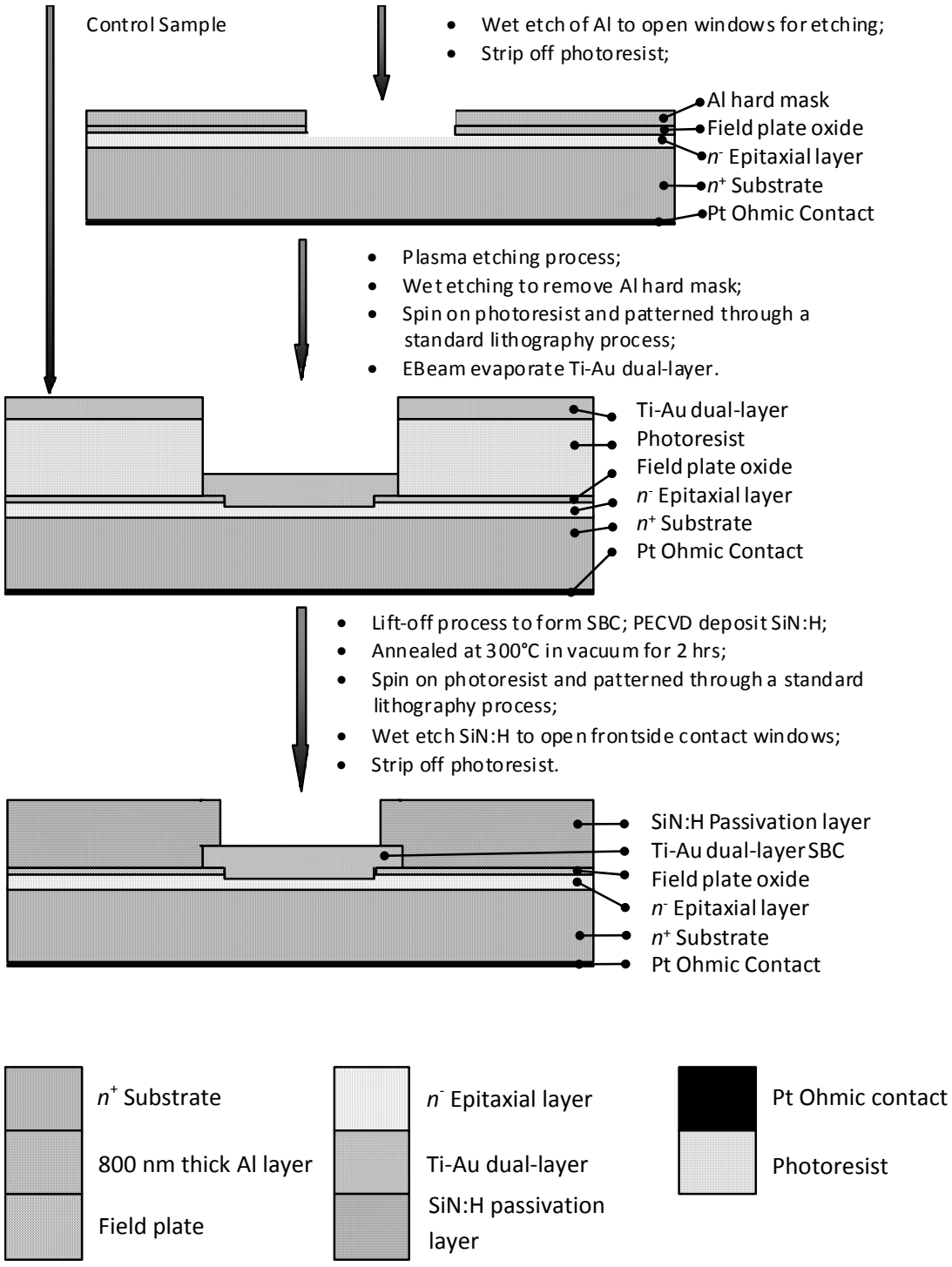


Fig. 6.1: Schematic process flow for the fabrication of 4H-SiC SBDs (continued).

Step	Process Name	Chemical	Temperature	Duration
1	Degrease	Acetone	>50 °C	5 min
		IPA	>50 °C	5 min
2	Rinse	DI Water	Room Temp	5 min
3	Piranha Clean	H_2SO_4:H_2O_2=1:1	No Control	15 min
4	Rinse	DI Water	Room Temp	5 min
5	Strip Oxide	HF:H_2O =1:10	Room Temp	5 min
6	Rinse	DI Water	Room Temp	5 min
7	RCA SC-1	NH_4OH:H_2O_2:H_2O=1.5:1.5:5	>80 °C	15 min
8	Rinse	DI Water	Room Temp	5 min
9	Strip Oxide	HF:H_2O =1:10	Room Temp	5 min
10	Rinse	DI Water	Room Temp	5 min
11	RCA SC-2	HCl:H_2O_2:H_2O=1.5:1.5:5	>80 °C	15 min
12	Rinse	DI Water	Room Temp	5 min
13	Strip Oxide	HF:H_2O =1:10	Room Temp	5 min
14	Rinse	DI Water	Room Temp	5 min

Table 6.1: Cleaning process for the 4H-SiC wafers.

A. *4H-SiC chip cleaning process.* The details of the cleaning process are listed in Table 6.1. The cleaning process consists of three steps, which are degrease, removal of organic contaminants and metallic contaminants. Except for the first degrease step, the other steps are followed by a rinse in deionized water (DI water) to remove the chemical residue of the previous cleaning step, a stripping of oxide layer by dipping into a diluted HF solution, and another rinsing in DI water to remove the HF residue.

The first degrease step served to remove grease and other organic contaminants by dipping the 4H-SiC chips sequentially into hot acetone and isopropyl alcohol (IPA), for 5 minutes each. Following the degrease, the samples were rinsed in DI water to

remove organic solvent residues. To further remove organic contaminants and organic solvent residues, the 4H-SiC chips were cleaned by the Piranha clean process and submerged into a H_2SO_4 and H_2O_2 solution. After stripping the oxide grown during the Piranha process and rinsing in DI water, the 4H-SiC chips were subjected to a slightly modified RCA (Radio Corporation of America) standard clean process. In SC-1 (Standard Clean Step 1), the 4H-SiC chips were grown with a thin SiO_2 layer of about 1 nm thick which would be removed in the subsequent oxide stripping process. After stripping the oxide and rinsed in DI water, the 4H-SiC chips were subjected to SC-2 (Standard Clean Step 2) process in which the metallic (ionic) contaminants, which might be partly contributed by the SC-1 process, were effectively removed. The 4H-SiC chips were then stripped off of oxide residue, rinsed in DI water, dried with dry N_2 gas blow and baked in oven at 110°C for 40 minutes. Upon the completion of the above cleaning process, the 4H-SiC chips were thoroughly cleaned and ready for the next process step.

B. *Sacrificial oxidation and dry thermal oxidation for fabrication of field plate.* After the cleaning process, the 4H-SiC chips were subjected to a sacrificial oxidation process to remove surface defects and possible contaminant residues. The SiC chips were thermally oxidized in pure O_2 ambient at a temperature of 1150°C for 3 hours to obtain a thermal oxide layer of about 40 to 50 nm thick. The sacrificial oxide layer was subsequently removed in a diluted HF solution. To reduce the surface leakage current, a 50 nm high quality dry thermal oxide was grown on top to serve a field plate. It was grown in pure O_2 ambient at a temperature of 1150°C for 3 hours and then annealed in pure N_2 ambient at the same temperature for 1 hour.

C. *Formation of back ohmic contact.* The back metal contact of SBD consists of 100 nm thick Pt layer, sputtered onto the backside of the 4H-SiC chips by Ar sputtering. Prior to the formation of back contact, the backside oxide layer, which was grown concurrently with the thermal field plate oxide, was carefully etched away using diluted HF solution while keeping the field plate oxide intact. To form good backside ohmic contacts, the samples were subjected to rapid thermal anneal (RTA) in an N_2 ambient at 1100°C for 3 minutes. The formed ohmic contacts were characterized using a standard linear transfer length method (L-TLM). The contact resistivity of the samples is between 1.1×10^{-4} and 7.0×10^{-4} $\Omega\cdot cm^2$, which is comparable to published data [115].

D. *Formation of front Schottky barrier contact (SBC)*. To open front contact windows, a thin layer of photoresist acting as a wet etch mask was spun onto the surface of field plate and patterned through a standard photolithography process. The front contact window was opened through wet etching of oxide using diluted HF solution. Following that, the photoresist mask was removed by acetone. After opening the front contact window, all the samples, except the one used as the control sample, were plasma etched under different conditions prior to forming Schottky contacts. The details of the plasma etching process are presented in section 6.2.2. After the plasma etching process, another thin photoresist layer was spun onto the front side of all samples including the control sample, and was patterned through standard photolithograph process to open windows for front contact electrode, which has a width of 25 μm overlapping the field plate. A dual metal layer of 30 nm Ti layer plus 300 nm Au was deposited onto the front side of the samples using Ar sputtering, and pattered to form the front Schottky contact electrode through a standard lift-off process. The SBC electrode has a circular shape with a radius of 100 μm.

GAS	**Flow Rate** [sccm]	R.F. **Power** [W]	**Pressure** [mTorr]	**Temperature** [°C]	**Deposition Rate** [nm/min]
SiH_4	100	60	800	300	64
N_2O	30				
N_2	600				

Table 6.2: The PECVD process parameters for the deposition of a-SiN:H.

E. *Formation of silicon nitride passivation layer*. To protect the SBDs from environment moisture and to reduce surface leakage current, a hydrogenated amorphous silicon nitride layer (a-SiN:H) of 100 nm thick was deposited on the front surface using the PECVD process. The PECVD system used for the deposition of silicon nitride passivation layer is the Plasma Therm 790^{TM} system and the process recipe is listed in Table 6.2. To improve the quality of the deposited a-SiN:H, the samples were *in-situ* annealed in vacuum at 350°C for 3 hours. The window to the front contact electrode was patterned through a standard lithography process and opened by wet etching of a-SiN:H using diluted HF solution.

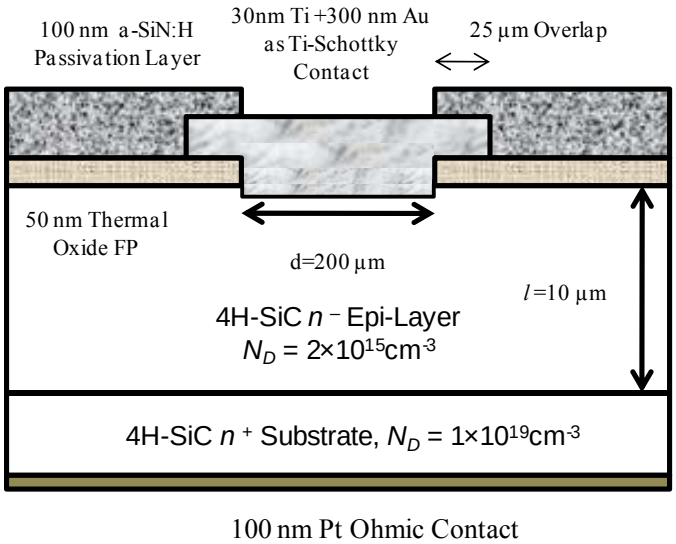


Fig. 6.2: Schematic diagram of SBDs fabricated in this work.

The schematic diagram of the final SBD device fabricated is shown in Fig. 6.2.

6.2.2 Plasma Etching Process

To study the effects of PEID on the electrical characteristics of *n* type 4H-SiC Schottky barrier diodes (SBDs), three plasma etching tests were designed to specifically address the damage due to positive ion bombardment (physical sputtering), chemical plasma etching and their combined effect (ion enhanced plasma etching, that is, CE+PS). A good understanding of the contribution of each type of etching to PEID will be useful towards developing 4H-SiC plasma etching processes that can maximize etch rate and minimize PEID.

As shown in Fig. 6.1, the samples for the plasma etching tests were first stripped off the photoresist mask left from the previous process. A hard mask meant for subsequent plasma etching tests, consisting of an 800 nm thick Al layer, was then evaporated onto the front surface using Ar sputtering. The Al layer was patterned to open windows for plasma etching through a standard lithography process, using a patterned photoresist as the mask and a wet chemical etching process. The latter involved using an etchant solution $18H_3PO_4$+Acetic Acid+HNO_3+$2H_2O$ to attack Al while keeping the thermal oxide field plate intact. After removing the photoresist mask, the samples were ready for the plasma etching tests.

The plasma etching tests were performed using a Plasma Theme ^{TM} PECVD 790 series plasma reactor. The reactor has two chambers, each with one pair of identical 8 inch upper and bottom Al electrodes which are powered by a 13.56 MHz R.F. power source capable of providing up to 600 W. For one chamber (the PECVD chamber), the R.F. power is driven to the upper electrode and the lower electrode is grounded to result in a low D.C. bias. For the other chamber (the RIE chamber), the R.F. power is

driven to the lower electrode to result in a very higher D.C. bias while the upper electrode is grounded.

Three types of plasmas, based on CF_4 alone, Ar alone, and CF_4+Ar, were used to result in different etching conditions that are characterized by mainly chemical etching (CE), physical sputtering (PS), and their combination, (CE+PS), respectively. Ar was chosen as a feed gas in the etching process so that when no CF_4 is used, strong physical sputtering can be achieved. The duration of the plasma etching for all the three tests was set at 30 minutes. The detailed process settings are listed in Table 6.3. To achieve CE, a very low D.C. self-bias is necessary to minimize the impact of physical ion bombardment onto the etched surface. To this end, the CE test was conducted in the PECVD chamber where only less than -40 V D.C. self-bias was developed compared to several hundred volts that is typically developed in the RIE chamber. The other plasma tests were conducted in the RIE chamber. To prevent potential contamination arising from the Al electrodes that may lead to micromasking effect, the electrode surfaces were covered with 8 inch Si wafers during the etching process. With this precaution, and due to our very small sample size (5×5 mm^2), the

	Ar Flow Rate [sccm]	**CF_4 Flow Rate [sccm]**	**R.F. Power [W]**	**|D.C.Bias| [V]**	**Pressure [mTorr]**
Sample CE	-	20	200	≤ 40	50
Sample PS	20	-	200	413	50
Sample CE+PS	20	20	200	431	50
Sample CR	-	-	-	-	-

Table 6.3: Plasma etching parameters setting for different test samples, namely, chemical etching sample (sample CE), physical sputter sample (sample PS), ion enhanced plasma etching sample (sample CE+PS), and unetched control sample (sample CR).

	Etch Rate [nm/min]	r.m.s. Surface Roughness [nm]	Etched Surface Assessment
Sample CE	0.11±0.04	9.43	Rough surface with few particles
Sample PS	0.08±0.01	1.48	Smooth surface
Sample CE+PS	13.7±0.93	1.72	Smooth surface
Sample CR	-	0.96	Smooth surface

Table 6.4: The etch rate, r.m.s. surface roughness, and etched surface assessment of CE, PS, CE+PS and unetched control samples.

samples were free of Al induced micromasking effect. At the end of the plasma etching tests, the Al masks on these samples were removed by using the same wet etching process that was used to define the Al mask. Together with the control sample, these etched samples were then ready for the next process step to form the front SBC.

6.3 Plasma Etching Results

The etched surfaces of the 4H-SiC subjected to different plasma etching tests were characterized in terms of the etch rate and r.m.s. surface roughness. The latter was measured by an atomic force microscope within a scan area of 10×10 μm^2. In addition, these etched surfaces were inspected and assessed under naked eye. The results are listed in Table 6.4 and the AFM pictures are shown in Fig. 6.3.

From Table 6.4, it is seen that the etch rates for CE and PS samples are 0.11 nm/min and 0.08 nm/min respectively, which are significantly lower than that of CE+PS sample of 13.7 nm/min. This demonstrates that mono-crystalline 4H-SiC is too chemically inert to be efficiently etched through pure CE process without the assistance of ion bombardment. On the other hand, the very low etching efficiency, or the so-called sputter yield, of pure PS process has led to an even lower etch rate

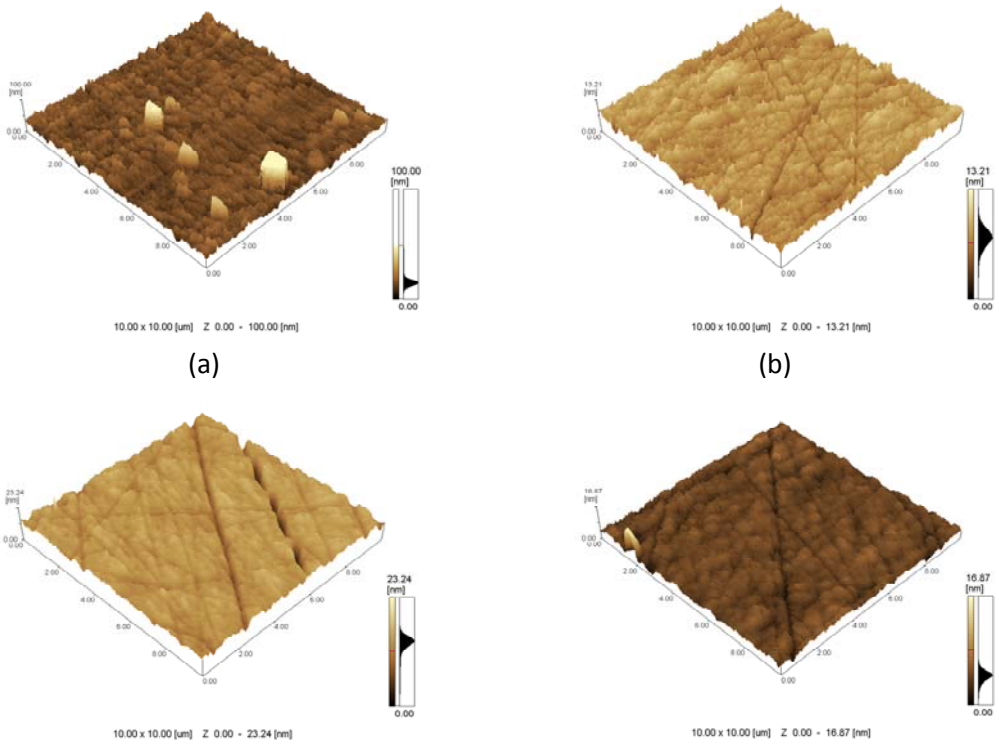


Fig. 6.3: AFM pictures of (a) chemical plasma etched surface, (b) physical sputtered surface, (c) reactive ion etched surface, and (d) unetched control surface.

compared to the CE process. In contrast, the CE+PS process which combines both CE and PS, greatly enhances the etch rate. Considering that the process has not been optimized in this study, the etch rate of 13.7 nm/min obtained for the CE+PS process is quite respectable.

From the r.m.s. roughness listed in Table 6.4 and the AFM pictures shown in Fig. 6.3, it is clear that the PS sample and CE+PS sample show a smooth etched surface with a slightly higher r.m.s. surface roughness compared to the unetched CR sample.

In contrast, the CE sample shows a much higher r.m.s. surface roughness. This result is consistent with our study of RIE process on SiC presented in Chapter three. At low D.C. bias, as in the case of CR sample, the etched surface is prone to various micromasking effects induced by C residues, e.g. the C rich-layer, that appear due to the slower etch rate of C [22]. The Al induced micromasking effect is excluded due to the precaution taken by covering up the metal electrodes with Si wafer. When at high D.C. bias, as in the case of PS and CE+PS samples, the strong ion bombardment will increase the etch rate of C and remove the micromask by sputtering away the C residues. Therefore, the PS sample and CE+PS sample are smooth and free of micromasking effect induced surface roughening. However, the ion bombardment itself can cause some damage to the chip surface, resulting in a slight increase in the r.m.s. surface roughness compared to the unetched CR sample.

6.4 Electrical Modeling of 4H-SiC SBD

In this section, we present the theoretical modeling of the electrical properties of 4H-SiC SBD, including its current-voltage (*I-V*), capacitance-voltage (*C-V*), and capacitance transient (capacitance deep-level transient spectroscopy) characteristics.

6.4.1 High Frequency Capacitance Voltage Characteristics

For an ideal SBD, the Schottky barrier junction capacitance C_D can be expressed as [116]:

$$C_D \equiv A\frac{\varepsilon_S}{W_D} = A\sqrt{\frac{q\varepsilon_S N_D}{2\left[\phi_B - V_R - \Delta\phi_b - \left(kT/q\right)\right]}} \tag{6.1}$$

where A, ε_S, W_D, ϕ_B, N_D, k, T, q, and V_R are the area of the SBD, permittivity of 4H-SiC, the width of depletion region, junction build-in potential, doping concentration underneath the Schottky contact, Boltzmann's constant, absolute temperature in Kelvin, electronic charge and reverse bias voltage respectively. $\Delta\phi_b$ is the image-force barrier lowering (or Schottky effect). In a high frequency capacitance measurement, C_D is measured by reverse biasing the SBD with a D.C. voltage and superimposing on it a small high frequency sinusoidal signal. By plotting $1/C_D^2$ versus V_R, the doping concentration N_D and SBH (ϕ_B) can be extracted. From the intercept of the $1/C_D^2$ versus V_R curve with the x-axis, V_I, the SBH (ϕ_B) can be obtained as follows,

$$\phi_B = V_I + \frac{kT}{q}\ln\left(\frac{N_D}{N_C}\right) + \frac{kT}{q} - \Delta\phi_b \tag{6.2}$$

where N_C is the conduction band density of states, which is $N_C = 1.7\times10^{19}\text{cm}^{-3}$ for 4H-SiC [117]. From the slope of $1/C_D^2$ versus V_R curve, the doping concentration N_D can be extracted,

$$N_D = \frac{2}{q\varepsilon_S\left[-\dfrac{d\left(1/C^2\right)}{dV_R}\right]A^2} \tag{6.3}$$

The image-force barrier lowering $\Delta\phi_b$ can also be calculated as follows [116]:

$$\Delta\phi_b = \sqrt{\frac{q\mathscr{E}_m}{4\pi\varepsilon_S}} \tag{6.4}$$

where $\mathscr{E}_m$ is the electric field intensity at the surface of the semiconductor.

6.4.2 Current-Voltage Characteristics

For an *n* type 4H-SiC SBD with light to moderate doping level and not at very low temperature, the dominant current transport mechanism is thermionic emission (TE). The TE current density *J* can be expressed as [116, 118]:

$$J = J_s\left[\exp\left(\frac{qV_F}{\eta kT}\right)-1\right] \tag{6.5}$$

$$J_s = A^{**}T^2\exp\left(-\frac{q\phi_B}{kT}\right) \tag{6.6}$$

$$A^{**} = \frac{4\pi q m^* k^2}{h^3} \tag{6.7}$$

where A^{**} is the Richardson constant, which is A^{**} = 146 $Acm^{-2}K^{-2}$ [119] for 4H-SiC. m^*, h, η and V_F are the effective electron mass, Planck's constant, ideality factor, and forward bias voltage, respectively. When V_F is larger than $3\eta kT/q$, Eqn. (6.5) is reduced to

$$J = J_s\exp\left(\frac{qV_F}{\eta kT}\right) \tag{6.8}$$

By plotting ln(J) versus V_F, the ideality factor η can be extracted from the slope $dV_F/d\ln(J)$ as given by

$$\eta = \frac{q}{kT}\left(\frac{dV_F}{d\ln J}\right) \tag{6.9}$$

The saturation current density J_S can be deduced from the *y*-intercept, from which the SBH ϕ_B can be determined,

$$\phi_B = \frac{kT}{q}\ln\left(\frac{A^{**}T^2}{J_S}\right) \tag{6.10}$$

When J is high enough to result in a significant potential drop across the series resistance R_{ON}, the forward bias V_F in Eqn. (6.8) has to be replaced by $V_F - J\,R_{ON}$. By differentiating V_F in Eqn. (6.8) with respect to ln(J), we obtain:

$$\frac{\mathrm{d}\left(V_F\right)}{\mathrm{d}\left(\ln J\right)} = R_{ON}J + \frac{\eta kT}{q} \tag{6.11}$$

Therefore, R_{ON} can be extracted from the slope of the linear part of the d(V_F)/d(ln$J$) versus J curve.

In this study, a more accurate method was used to extract the SBH ϕ_B. By substituting Eqn. (6.6) into Eqn. (6.8) and rewriting Eqn. (6.8) as [120]

$$\ln\left(\frac{J}{T^2}\right) = \ln A^{**} - \frac{q}{k}\left(\phi_B - \frac{V_F}{\eta}\right)\frac{1}{T} \tag{6.12}$$

The SBH q, ϕ_B can be extracted from the slope of the ln(J/T^2) versus $1/T$ curve. Usually, this curve exhibits very high linearity such that q, ϕ_B can be determined more accurately [120].

6.4.3 Capacitance Deep-Level Transient Spectroscopy

Capacitance deep-level transient spectroscopy (CDLTS) is a characterization tool that utilizes the junction capacitance transient characteristics to detect deep-level traps inside the semiconductor. The conventional CDLTS uses a double boxcar approach to measure the capacitance transient signal, as was first proposed by Lang [121] and illustrated in Fig. 6.4 [122]. The SBD is repetitively pulsed between forward

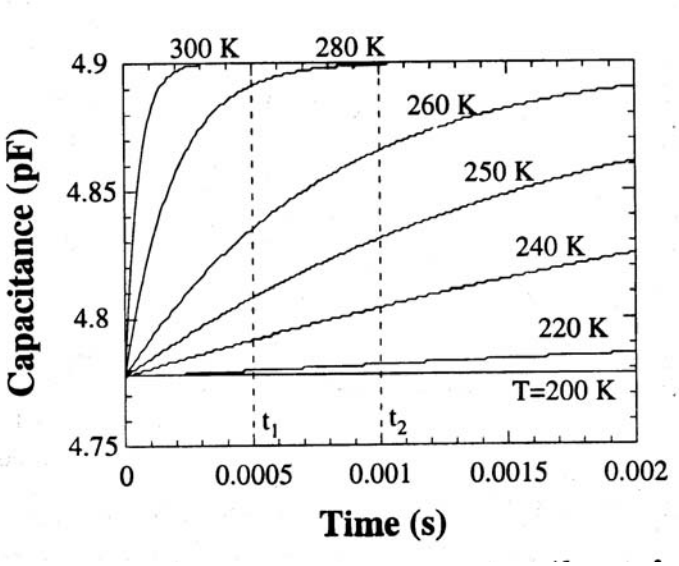


Fig. 6.4: An example of transient capacitance curves with capacitance transient signal gated at t_1, and t_2. [122].

and reverse bias, while the measurement temperature scans slowly from low to high. Each time that the SBD is pulsed to reverse mode, the electrons that were trapped during the forward bias mode, are detrapped from the deep-level traps. During the detrapping process, the electric field in the depletion region increases and the depletion region width decreases, resulting in an increase in the junction capacitance with time. At each temperature, a transient curve can be obtained. In a standard boxcar CDLTS test, the transient characteristic is extracted by measuring the capacitance transient signal at two different times t_1 and t_2, as shown in Fig. 6.4.

$$C(t) = C_0\left[1 - \frac{n_T(0)}{2N_D}\exp\left(\frac{-t}{\tau_e}\right)\right] \tag{6.13}$$

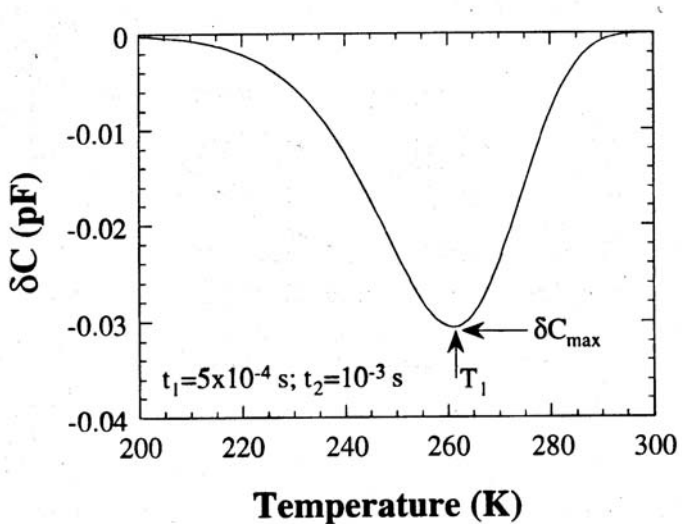


Fig. 6.5: A typical plot of δ*C*-*T*. [122]

The transient capacitance can be expressed as [122] where C_0 is the capacitance in the steady state, that is C ($t = \infty$), n_T is the deep-level trap density occupied by electrons and N_D is the substrate doping level. τ_e is the electron emission time constant, which depends on temperature as follows

$$\tau_e = \frac{\exp\left[(E_C - E_T)/kT\right]}{\gamma_n \sigma_n T^2} \tag{6.14}$$

In the equation above E_C-E_T is the trap energy measured from the conduction band edge, and σ_n and γ_n are the electron capture cross section and electron emission coefficient, respectively. For 4H-SiC, $\gamma_n = 3.25\times10^{21}(m_n/m_0)cm^{-2}s^{-1}K^{-2}$, where m_n is the electron density-of-states effective mass. As shown in Fig. 6.4, when the *C*-*t* waveforms are sampled at two different times, $t=t_1$ and $t=t_2$, one can determine $\delta C = C(t_1) - C(t_2)$, which can be expressed as

$$\delta C = C(t_1) - C(t_2) = \frac{C_0 n_T(0)}{2N_d}\left[\exp\left(\frac{-t_2}{\tau_e}\right) - \exp\left(\frac{-t_1}{\tau_e}\right)\right] \tag{6.15}$$

By slowly scanning the measurement temperature and repetitively pulse the SBD between forward and reverse bias at each temperature, one can draw a plot of δC-T, as shown in Fig. 6.5 [122].

The τ_e corresponding to the maximum δC shown in Fig. 6.5 can be calculated as:

$$\tau_{e\max} = \frac{t_2 - t_1}{\ln(t_2 / t_1)} \tag{6.16}$$

By varying t_1 and t_2, one can calculate a series of τ_{emax} and plot the emission Arrhenius plot of $\ln(\tau_{e\max} T)$ versus $1/T$, where T is the temperature corresponding to the CDLTS peak, i.e. $\delta C_{\max}$. From its slope we can determine $(E_C - E_T)/k$ .From its intercept on the axis of $\ln(\tau_{e\max} T^2)$, we have $\ln[1/\gamma_n \sigma_n]$. If the γ_n is known, we can calculate σ_n. The trap density N_T can be calculated as follows,

$$N_T = \frac{\delta C_{\max}}{C_0} \frac{2 N_D r^{r/(r-1)}}{1 - r} \tag{6.17}$$

where $r = t_2/t_1$.

6.5 Electrical Measurements of 4H-SiC SBDs

The current-voltage (I-V) and capacitance-voltage (C-V) characteristics of the SBDs were measured in a sealed and shielded chamber vacuumed to 5 to 10 mTorr. The samples were mounted onto a temperature controllable sample stage (MMR Technologies, Inc.), which was connected to a programmable temperature controller K-20 (MMR Technologies, Inc.). The temperature could be varied continuously from room temperature to 700 K with about 0.5% accuracy. For I-V measurements, an HP

4156A precision semiconductor parameter analyzer with sensitivity down to fA was used. An HP 4284A precision LCR meter was used for high frequency *C-V* and capacitance deep-level transient spectroscopy (CDLTS) measurements. The capacitance was measured by superimposing a small high frequency sinusoidal signal to a D.C. bias voltage. The frequency and the amplitude of the high frequency sinusoidal signal were set at 1 MHz and 25 mV respectively. All the measurement equipment and temperature controllers were controlled by a computer through a standard IEEE 488 bus. In our study, the temperature range was set between 300 K and 550 K.

6.6 Results and Discussions

In this section, the doping level, forward and reverse bias current-voltage characteristics, series resistance, ideality factor of CR, PS, CE, and CE+PS samples are extracted from the *C-V* and *I-V* characteristics. The results are discussed in relation to the etching conditions that these samples were subjected to. In additional, the CDLTS results of these samples are presented and discussed.

6.6.1 Doping Concentration

Fig. 6.6 plots $1/C^2$ versus bias voltage measured at room temperature (300 K) for the SBDs subjected to different etching tests. As discussed in section 6.4, the doping level of the epitaxial layer underneath the Schottky contact metal can be deduced from the slope of the plot. From Fig. 6.6, it is clearly seen that the curves for CR, PS, CE, and CE+PS samples are all linear in the range of the bias voltage measured, and are virtually parallel to each other, which means that they have a similar doping level. This is not unexpected as the different etching conditions are not expected to result in

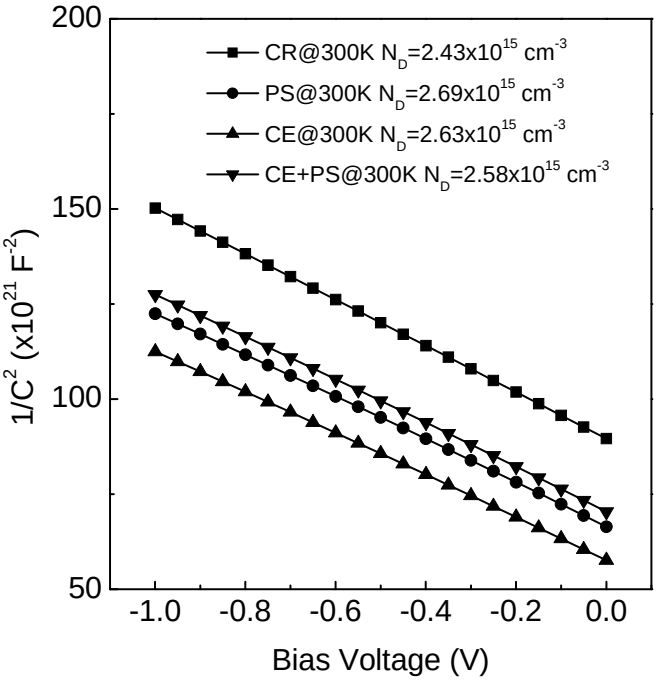


Fig. 6.6: The $1/C^2$ versus bias voltage measurement results carried out at room temperature (300 K).

a change in the doping concentration. More than 20 SBDs per etching process were studied with the doping concentration of the samples deduced using Eqn. (6.3). The results are presented in Table 6.5 and in the box plot in Fig. 6.7. As can be seen from the results, the doping concentrations deduced among all the samples are comparable, and close to the nominal doping level of 2×10^{15} cm^{-3} quoted by Cree Research. The largest difference between the mean values of the different samples is about ±10%, which may be attributed to errors involved in determining the slopes of the curves, as well as doping concentration variation across the 4H-SiC wafer, from which the samples were cut. Hence, based on our results, we conclude that the different plasma etching processes have not caused any significant change to the doping level, and the

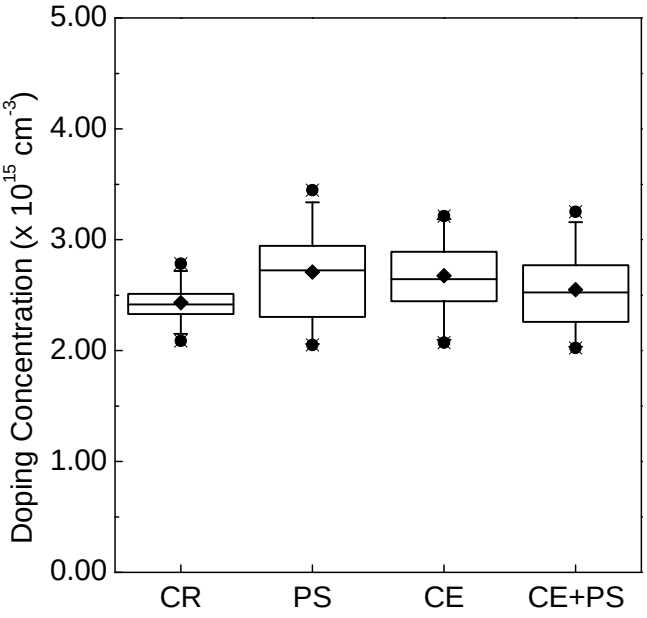


Fig. 6.7: The box plot of doping concentration (N_D) measured at room temperature (300 K). The solid diamond represents the mean value of the data. The upper and lower edges of the boxes represent the 75% and 25% of the data respectively, the upper and lower solid circles represent the 95% and 5% of the data respectively, and the upper and lower crosses represent the maximum and minimum values respectively.

Doping Level	CR	PS	CE	CE+PS
Average [$\times 10^{15}$ cm^{-3}]	2.45	2.70	2.67	2.54
Standard Deviation [$\times 10^{15}$ cm^{-3}]	0.146	0.388	0.317	0.352

Table 6.5: The average doing level and its standard deviations deduced for samples subjected to of CR, PS, CE and CE+PS samples. The results are based on the measurements of about 20 SBDs.

C-V measurement technique is still an effective way of determining the doping concentrations despite the presence of any surface damage.

6.6.2 Forward Bias Current-Voltage Characteristics

The forward bias *I-V* characteristics of the SBDs were measured in the range of 0 to 2 V at different temperatures from 300 to 550 K. A qualitative discussion of the *I-*

V results will be given in this section, whereas the quantitative analysis of the series resistances, ideality factors and Schottky barrier heights of these samples will be presented in the subsequent sections.

Fig. 6.8 shows the I-V curves for the four samples measured at room temperature (300 K). The CR sample reveals a low forward bias current density of ~1 nA/cm^2 at 0.4 V and a high turn on current density of ~100 A/cm^2 at 2.0 V. The linear region in the (log*J*)-V_F plot of the CR sample spans almost 11 orders of magnitude, which attests to the uniformity of the Schottky junction contact and suggests the dominance of the TE conduction.

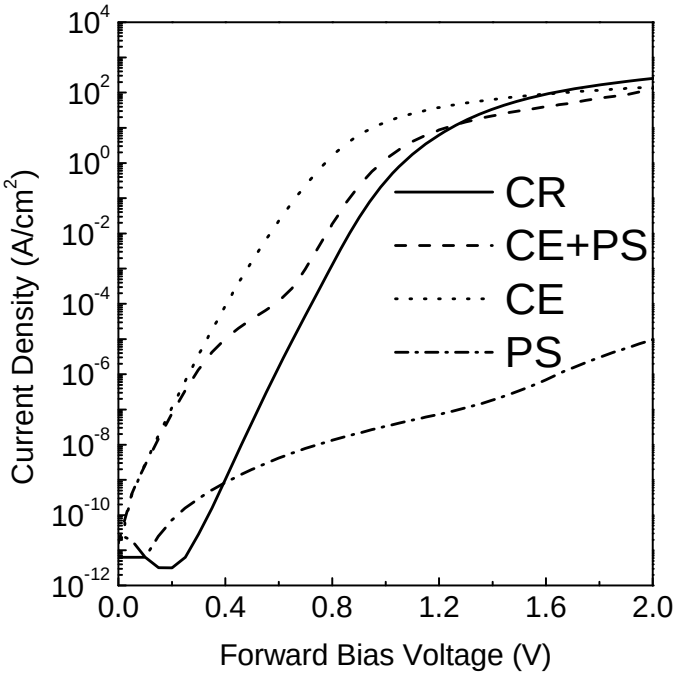


Fig. 6.8: Forward bias current-voltage characteristics of the CE, PS, CE+PS and CR samples.

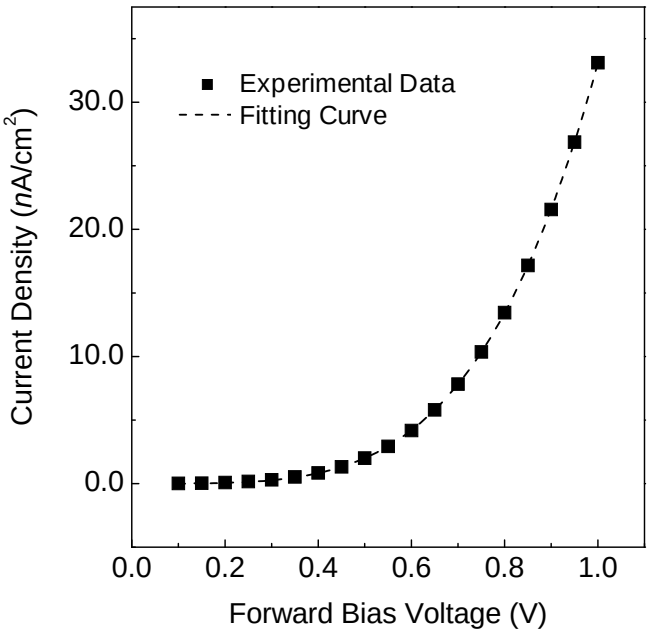


Fig. 6.9: The power relationship fitting of J-V_F characteristic of the PS sample between 0.1 to 1 V.

In contrast, the PS sample exhibits a very different forward bias current characteristic. As seen in Fig. 6.8, its forward bias current is much lower compared to the other samples. For example, it only has a current density of about 10 μA/cm^2 at 2.0 V which is nearly seven orders of magnitude lower than the other samples. Its (log$J$)-V_F plot also reveals poor linearity. These results indicate that the PS sample has a very high series resistance and the dominant conduction mechanism is no longer TE. The PS sample has been mainly subjected to Ar ion bombardment, which can introduce lattice defects that act as deep-level generation-recombination centers inside the semiconductor [112]. Therefore, trap-assisted tunneling, hopping or space charge limited current is more likely the dominant conduction mechanism [123]. Indeed, its J-V_F curve over a lower voltage range of between 0.1 to 1.0 V, where it is expected that

the series resistance effect has not set in, can be perfectly fitted by a power law of $J = 3.31\times10^{-8}V_F^{4.04}$, as shown in Fig. 6.9. Similar power laws have been observed for GaAs SBDs of different dopant types heavily damaged by Ar ion sputtering. It should be noted that such power law conduction mechanism cannot be described using any existing well-developed and simplified conduction models [123]. Severe damage from Ar physical sputtering also can cause amorphization at the surface, which leads to the formation of a resistive layer and accounts for the high series resistance of the PS sample.

Similar to the CR sample, the CE sample also clearly exhibits a linear region in the forward bias ($\log J$)-V_F plot, which suggests that the TE conduction is the dominant mechanism. It also has a much higher forward bias current density in the linear region. For example, its current density is 100 μA/cm^2 at 0.4 V, compared to only 1 nA/cm^2 at the same voltage for the CR sample. This suggests that the chemical etching has significantly lowered its SBH, which may be due to possible damage that include Fermi level pinning by the introduction of a large density of interface states [112], or surface polymerization [114].

For the CE+PS sample, comparing its I-V characteristic with that of the PS sample, and noting that both were subjected to comparable D.C. self bias during the etching process, the results suggest that most of the damage in the CE+PS sample caused by physical sputtering during the etching process has been etched away by the CE process. It is noted that two linear regions exist in its ($\log J$)-V_F plot and in between a clear kink can be clearly seen around 0.4 to 0.7 V. The existence of these two linear regions can be attributed to the presence of a pair of SBDs with different SBHs that are connected in parallel [124]. The first linear region at lower voltages represents the

turn on of one of the SBDs with a lower SBH. The kink signifies the series resistance limited current region that is associated with this SBD. The second linear region at higher voltages manifests the turn on of the other SBD with a higher SBH. This deviation from the ideal Schottky barrier interface can be explained in terms of defects such as difference in the crystal symmetry of the metal with respect to the semiconductor or variation in orientation at the metal–semiconductor interface, due to localized faceting of the interface which has been observed to create inhomogeneity in the SBH [125]. Other reasons attributed for this anomaly includes contamination of the Schottky metal, formation of mixture of different metallic phases of the Schottky metal with different Schottky barrier heights, dopant clustering [125]. In our case, as the two linear regions are only observed for the CE+PS sample, but not individually for the CE and PS samples, we propose that the origin is due to inhomogeneity at the MS interface arising from a combination of CE and PS etching. In a plasma process, one of the well known issues is its instability, due to internally generated electric and magnetic fields [45]. Random perturbations caused by the plasma instability can result in the plasma switching to a spatially inhomogeneous mode [126], and lead to inhomogeneous etching. In our RIE process, the same spatial plasma inhomogeneity due to the plasma instability may account for the inhomogeneity in the etching process for the CE+PS sample. This inhomogeneity is likely to be enhanced in the CE+PS sample compared to the CE and PS samples, due to a combination of the two different etching mechanisms involved in the plasma etching process for the CE+PS sample.

A closer look at Fig. 6.8 reveals that the first linear region of the (log$J$)-V_F curve of the CE+PS sample almost overlaps with that of the CE sample, whereas the second liner region approaches that of the unetched CR sample. It is proposed that the former is associated with the SBD contact area where the damage due to CE is still present in

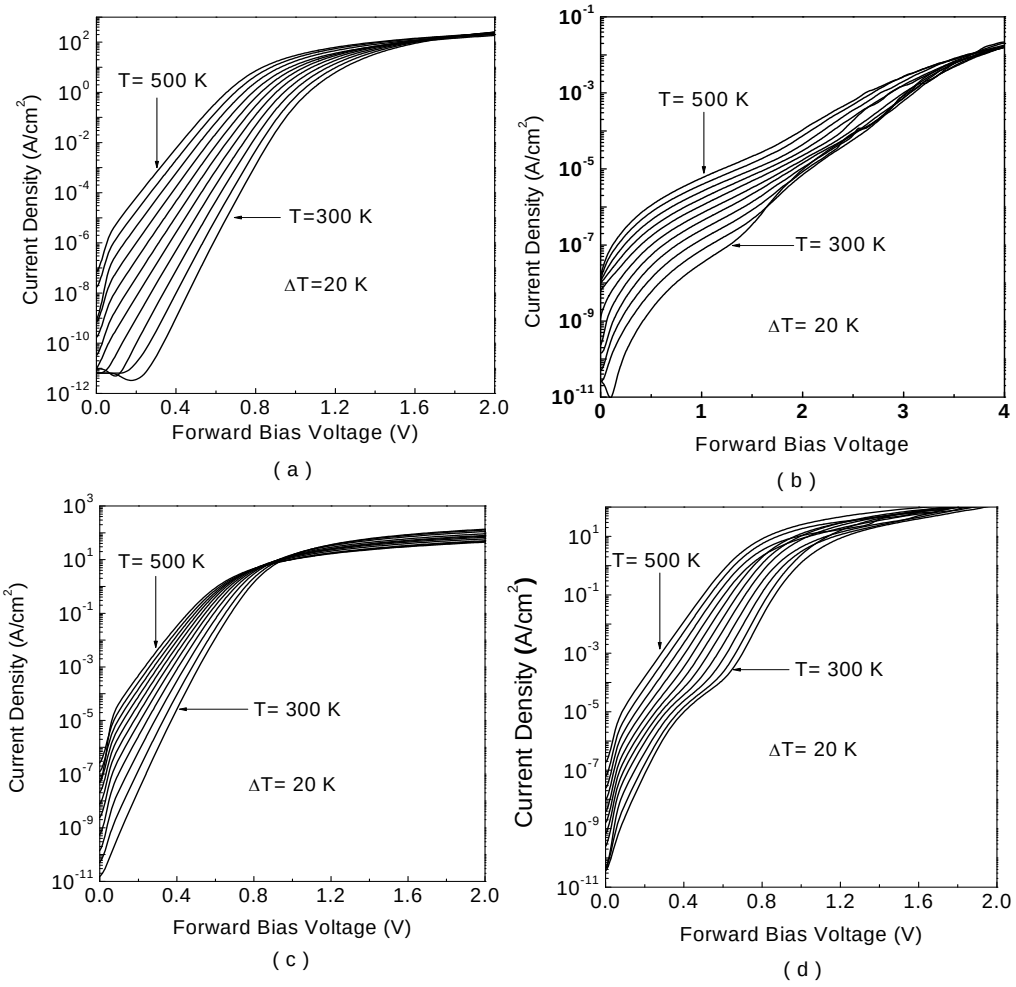


Fig. 6.10: The forward bias at different temperature for (a) CR sample, (b) PS sample, (c) CE sample, and (d) CE+PS sample.

the CE+PS sample, whereas the latter is associated with the remaining SBD area where the damage due to CE has been sputtered away. This is consistent with the earlier point that the MS interface is non-homogeneous.

Fig. 6.10 shows the forward bias *I-V* characteristics measured from 300 to 500 K with a step of 20 K. For the CR and CE samples, it can be seen that the high linearity in the (log*J*)-V_F plot is maintained throughout the studied temperature range, indicating that the same TE conduction mechanism at higher temperature. As for the

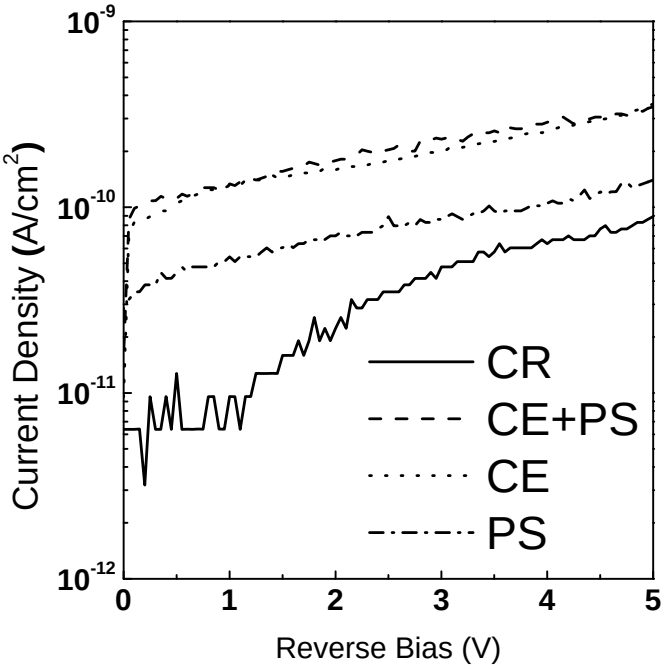


Fig. 6.11: The leakage currents versus reverse bias measured at room temperature (300 K).

CE+PS sample, the kink in the current observed at room temperature is observed to soften and ultimately disappear at higher temperature. This can be explained as at higher temperature, the SBD with a higher SBH will dominate the current conduction according to an Arrhenius's law, and hence the conduction has been reduced from that of two SBDs in parallel to just one SBD. In contrast, for the PS sample, the non-linear behavior persists throughout the range of temperature investigated.

6.6.3 Reverse Bias Current-Voltage Characteristics

Fig. 6.11 shows the leakage current under reverse bias from 0 to 5 V for the four samples measured at room temperature (300K). It is clearly seen that all the plasma etched samples, i.e. CE, PS, and CE+PS samples, have higher reverse bias leakage current compared to the unetched CR sample. In addition, the reverse bias current for

the CE sample almost overlaps with that of the CE+PS sample. As for the PS sample, it has a reverse bias current density that is in-between the unetched CR sample and the CE and CE+PS samples.

The high reverse bias leakage current density of the CE sample compared to the CR sample may be due to its lower SBH as a result of the chemical etching, the details of which shall be presented in the subsection 6.6.6. The overlap of leakage current curves of the CE and CE+PS samples suggests that chemical etching induced damage dominates the reverse bias current characteristic of these samples. As for the PS sample, it has an excess reverse bias leakage current density compared with the CR sample. Considering the high defect density in the depletion region of the PS sample beneath the MS interface, it is postulated that the excess reverse bias leakage current is derived from generation current from these traps in the depletion region [123]. The CE and CE+PS samples' high reverse bias leakage current is largely due to the SBH lowering due to chemical etching induced surface damage, including introducing donor-like interface states. [127]

6.6.4 Series Resistance

The series resistance R_{ON} can be extracted from the linear region of the J-V curve measured at room temperature (300 K) under strong forward bias. In the case of the CR, CE and CE+PS samples which exhibit clearly linear regions in the log$J$-V_F plot and series resistance limited current at high forward bias voltages, R_{ON} can be readily determined. In contrast, the PS sample does not exhibit similar I-V characteristics and hence its series resistance is not clearly defined. For comparison, we have applied the same procedure to determine its R_{ON} as for the other samples, over a voltage range of 1.2 V to 2.0 V.

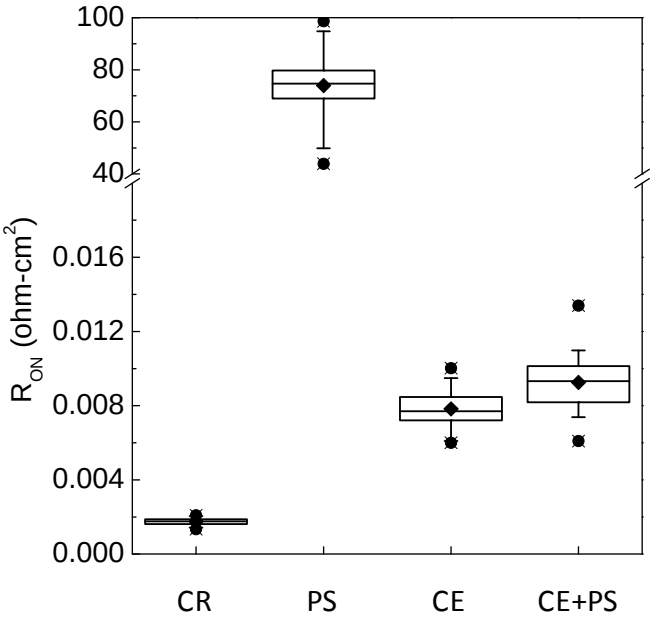


Fig. 6.12: The box plot of R_{ON} measured at room temperature (300 K).

R_{ON}	CR	PS	CE	CE+PS
Average [Ω-cm^2]	0.0018	73.96	0.0078	0.0092
Standard Deviation [Ω-cm^2]	0.0002	11.48	0.001	0.0014

Table 6.6: The mean R_{ON} and its standard deviation measured at room temperature (300 K).

As can be seen from Fig. 6.8, all the CR, CE and CE+PS samples have similar series resistance limited current characteristics, which suggest that they have comparable R_{ON}. It is worth noting that, except for the different plasma etching conditions that these samples were subjected to, they were fabricated using an identical process. Therefore, it is reasonable to assume that the difference in their R_{ON} is mainly due any changes in the metal-SiC interface property brought out by the plasma etching.

Fig. 6.12 shows the box plot of R_{ON} measured at room temperature (300 K) for the CR, PS, CE, and CE+PS samples. Their mean values and standard deviations are listed in Table 6.6. It can be seen from the results that the CR sample has a reasonably low R_{ON} of only 1.8 mΩ-cm^2. In contrast, the PS sample has the highest R_{ON} of 74 Ω-cm^2, which is at least four orders of magnitude higher than the CR sample. The drastic increase in R_{ON} for the PS sample may be attributed to the existence of a highly resistive and disordered SiC surface layer caused by the Ar ion physical sputtering [112]. On the other hand, both the CE and CE+PS samples exhibit R_{ON} of 7.8 and 9.2 mΩ-cm^2 respectively, which are increased compared to that of the CR sample, but not as much as that seen for the PS sample. The increase is likely due to a change in the metal-SiC interface property brought about by the chemical plasma etching, including a change in the stoichiometry, presence of residue of etching products and even surface polymerization [112, 114]. It is worth noting that, from our previous study, a carbon rich layer was also formed under a low D.C. self-bias RIE process that was characterized by mainly chemical etching [22].

6.6.5 Ideality Factor

The ideality factor of the SBDs was extracted from the linear region of the (ln$J$)-V_F curves. Fig. 6.13 shows the box plot of ideality factor measured at room temperature (300 K) for the CR, PS, CE, and CE+PS samples. Their mean values and standard deviations are listed in Table 6.7. For the CE+PS samples, because of the existence of two linear regions in the (ln$J$)-V_F plot, two ideality factors are correspondingly evaluated over the lower and higher bias voltage ranges, and are

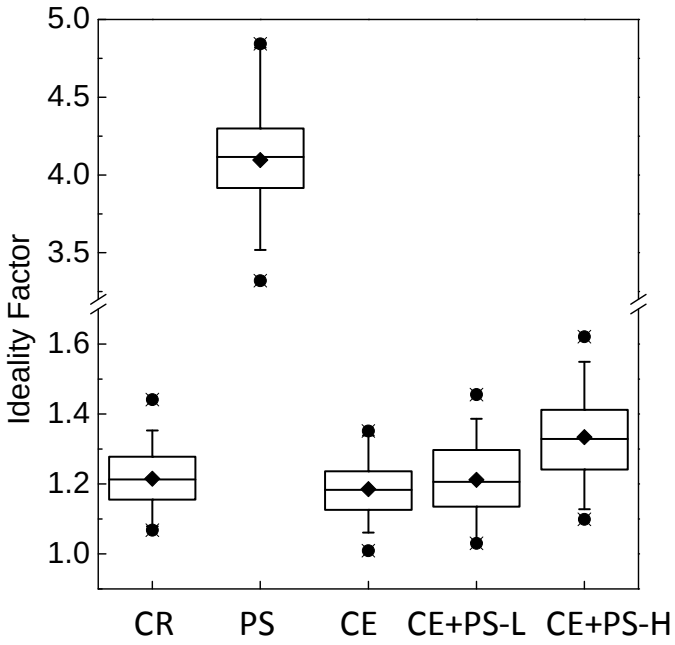


Fig. 6.13: The box plot of ideality factor of the CR, PS, CE, and CE+PS samples measured at room temperature (300 K). For the CE+PS sample, two ideality factors are deduced, CE+PS-L and CE+PS-H, which denote the ideality factors measured at lower and higher bias linear regions.

Ideality Factor	CR	PS	CE	CE+PS-L	CE+PS-H
Average	1.22	4.09	1.19	1.21	1.33
Standard Deviation	0.088	0.347	0.090	0.103	0.122

Table 6.7: Mean and standard deviation of ideality factor of the CR, PS, CE, and CE+PS samples measured at room temperature (300 K).

denoted as $\eta_{CE+PS-L}$ and $\eta_{CE+PS-H}$, respectively. At room temperature, the mean ideality factors of the CR, CE and CE+PS samples are 1.22, 1.19, and 1.21 ($\eta_{CE+PS-L}$), respectively. They are close to the ideal value of 1.0, which suggests that the SBDs have reasonably good Schottky contact [128] and demonstrates that the dominant conduction mechanism of the CR, CE and CE+PS ($\eta_{CE+PS-L}$) samples is TE. The deviation from the theoretical ideality factor of 1 [118] could due to bias dependence of barrier height, electron tunneling through the barrier, and the carrier recombination

within the depletion region [118]. The ideality factor $\eta_{CE+PS-L}$ is associated with the SBD where the surface damage is mainly attributed to chemical etching, similar to the CE sample. As the ideality factors of the CR, CE and CE+PS ($\eta_{CE+PS-L}$) samples are very close to each other, it means that the damage associated with chemical etching has not affected the forward bias conduction mechanism of the SBDs. The ideality factor $\eta_{CE+PS-H}$ of the CE+PS sample that corresponds to the SBD with a higher SBH has a mean value of 1.33, which is slightly higher than $\eta_{CE+PS-L}$. This may be caused by damage induced by Ar ion physical sputtering.

As the (ln$J$)-V_F curve of the PS sample is not linear and does not correspond to TE conduction, its ideality factor is not defined. Nevertheless, for comparison purpose, we have also applied the same procedure to deduce its ideality factor as for the other samples, over the same voltage range of 0.2 V to 0.4 V where the ideality factors of the other samples were determined. It is found the PS sample exhibits a very high apparent ideality factor of 4.09. This large deviation from the ideal value is consistent with our previous discussion that the dominant conduction mechanism may be due to trap-assisted tunneling, hopping or space charge limited current.

6.6.6 Schottky Barrier Height

The SBHs of the control sample and the samples subject to different plasma etching processes have been deduced from the C-V curves according to Eqn. (6.2). For inhomogeneous Schottky contact, as in the case of CE+PS sample, the SBH obtained from the C-V measurements represents its average over the whole contact area. The box plot of the SBHs is shown in Fig. 6.14 and their mean values and standard

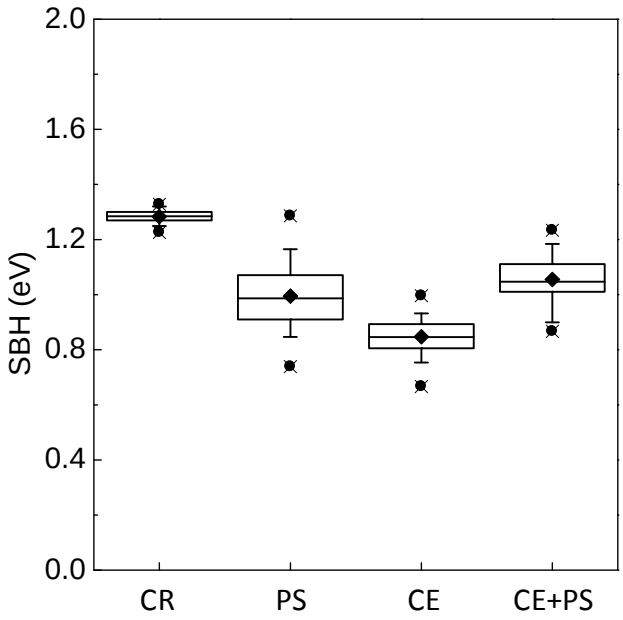


Fig. 6.14: The SBH of the CR, PS, CE, and CE+PS samples measured at room temperature (300 K). The solid diamond represents the mean value of the data. The upper and lower edges of the boxes represent 75% and 25% of the data respectively, whereas the upper and lower solid circles represent the 95% and 5% of the data respectively.

SBH	CR	PS	CE	CE+PS
Average[eV]	1.28	1.00	0.85	1.03
Standard Deviation [eV]	0.023	0.110	0.063	0.082

Table 6.8: The means and the standard deviations of the CR, PS, CE and CE+PS samples.

deviations are summarized in Table 6.8. The SBH has also been extracted from the slope of the $\ln(J/T^2)$-$1/T$ curve, over the temperature range from 300 to 550 K based on Eqn. (6.12). For the CE+PS sample, because of the existence of two linear regions, the SBH has been individually evaluated at lower and higher bias voltages, and are denoted as SBH(CE+PS-L) and SBH(CE+PS-H), respectively. For comparison, we have also deduced the apparent SBH of the PS sample using the *I-V* result despite that the conduction is not strictly by thermionic emission (TE). The results are shown in

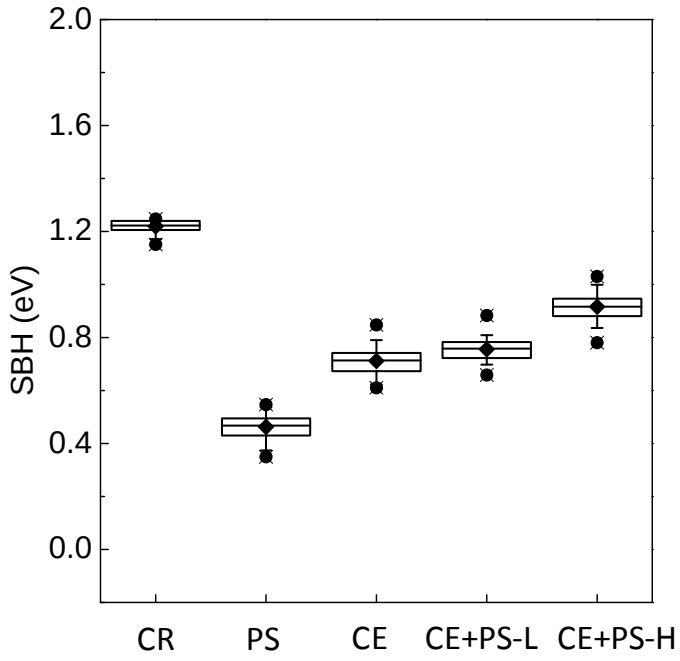


Fig. 6.15: The box plot of SBH of the CR, PS, CE, and CE+PS samples. The solid diamond represents the mean value of the data. The upper and lower edges of the boxes represent 75% and 25% of the data respectively, whereas the upper and lower solid circles represent the 95% and 5% of the data respectively.

SBH	CR	PS	CE	CE+PS-L	CE+PS-H
Average [eV]	1.22	0.46	0.71	0.76	0.92
Standard Deviation [eV]	0.024	0.047	0.051	0.042	0.050

Table 6.9: The means and standard deviations of SBH of the CR, PS, CE, and CE+PS samples.

box plot in Fig. 6.15 and listed in Table 6.9. All these results obtained are based on the measurement of about 20 SBDs per each etching process.

Comparing the SBHs extracted using the two methods, it is noticed that the values extracted from *C-V* measurements are generally slightly higher than those extracted from *I-V* measurements, except for the PS sample. It has been reported that

the difference in SBH deduced using the two different methods is related to the ideality factor, whereby a higher ideality factor will lead to a larger deviation [112]. This is indeed seen in our case as the PS sample has the largest apparent ideality factor of 4.09.

The SBHs of the unetched CR sample are slightly higher than the reported range of 0.8-1.17 eV [120], which may be attributed to the presence of a high quality field plate thermal oxide that provides surface passivation. It has been previously reported that with a suitable passivation layer, the SBH can be improved by up to 30% through reducing surface state density [129]. The lower SBH of the CE sample compared to the CR sample has resulted in a higher forward and reverse bias current density. As pointed out earlier on, chemical etching induced SBH lowering can be attributed to several possible factors, e.g. Fermi level pinning by the introduction of a large density of interface states [112] or surface polymerization [114]. Similar results of low SBH and high forward bias and/or reverse bias current density have been reported for SiC SBDs fabricated based on mainly chemical etching using ICP at 0 V D.C. bias [81, 113, 114]. For example, B. Li et al reported that the CF_4/O_2 ICP etching of 6H-SiC Au-SBD at 0V D.C. bias has resulted in a high leakage current of 0.1 μA at -20 V, a low SBH of about 0.9 eV and a high ideality factor of about 1.7 [114]. They attributed this to surface contamination caused by the formation of a carbon rich polymeric layer at the surface, arising due to the different etch rates of Si and C. Similarly, we have also reported in Chapter three the formation of a carbon rich-layer at low D.C. self bias in our RIE etching of 4H-SiC, which can lead to a rough and textured etched surface [22]. This carbon rich-layer may be responsible for the rough etched surface with an r.m.s. surface roughness of 9.43 nm, a high forward and reverse bias current density, and a low SBH of our CE sample. However, it should be noted that the ideality factor

of our CE sample of 1.19 is comparable with the ideality factor of 1.22 of the unetched CR sample, and much better than the 1.7 reported by B. Li et al for their device. The SBH of the PS sample deduced using *I-V* measurements 0.46 eV is the lowest among all the samples. This is manifested in the lower forward bias current and reflects the severe damage at the surface as a result of the physical sputtering. For the CE+PS sample, we shall refer to the SBD with a lower SBH as SBDL and the one with a higher SBH as SBDH. For SBDL, its SBH (0.76 eV) and ideality factor (1.21) are very close to those of the CE sample of 0.71 eV and 1.19 respectively. This suggests that the SBDL is attributed to the contact area, which has been effected by damage related to chemical etching. In contrast, the SBDH exhibits improved characteristics with a higher SBH. This is consistent with the earlier discussion that the SBDH corresponds to the contact area where the chemical etching induced surface damage/contamination has been removed by physical sputtering.

6.6.7 Capacitance Deep-Level Transient Spectroscopy

To detect and investigate deep-level defects in 4H-SiC which may arise from the etching, we have performed capacitance deep-level transient spectroscopy (CDLTS) measurements for the four samples over the temperature range from 300 to 550 K. Due to the limited integration time capability of the LCR meter (around 50 ms), we focused only on the study of deep-level traps with slower response time of 100 msec. In the experiments, the samples were first pulsed to 2 V for 50 sec for deep-level traps to capture electrons. They were then pulsed to -5 V to emit electrons, during which the transient capacitance was monitored with elapsing time. A standard double boxcar method was used with t_1/t_2 = 100 msec/3000 msec.

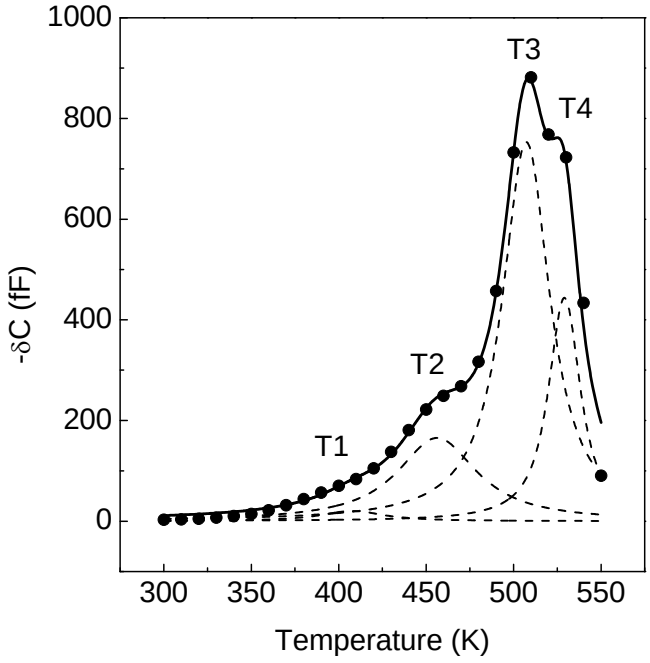


Fig. 6.16: The CDLTS plot of PS sample in which four trap peaks, namely T1, T2, T3, and T4 are identified and deconvoluted.

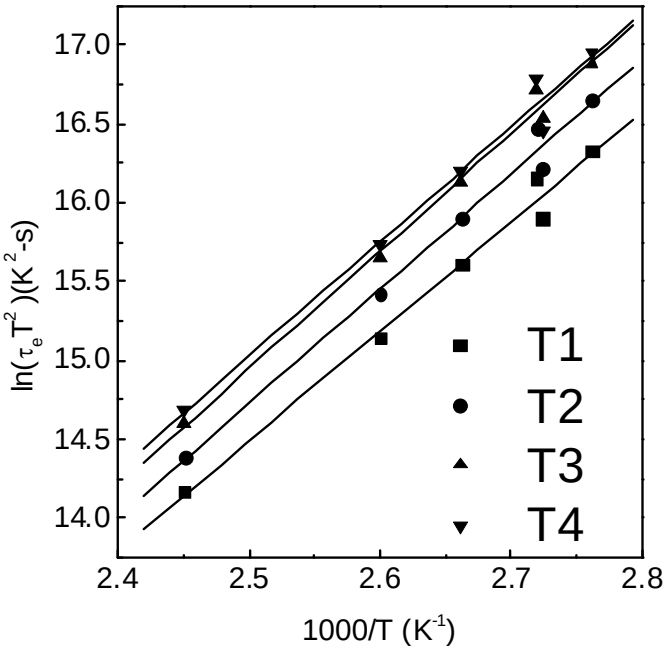


Fig. 6.17: Arrhenius plot for traps T1, T2, T3, and T4 found in PS sample.

Trap Level	E_C-E_T [eV]	Capture Cross Section (σ_n) [cm^2]	Density [cm^{-3}]	Defect Label
T1	0.60	6.98×10^{-20}	3.97×10^{13}	Z1/Z2 [130]
T2	1.24	1.24×10^{-13}	3.22×10^{14}	E7 [131]
T3	1.05	2.29×10^{-17}	1.48×10^{15}	
T4	1.02	5.59×10^{-18}	9.00×10^{14}	

Table 6.10: Trap level measured with respect to the conduction band edge E_C-E_T, capture cross section σ_n, and trap density of the traps T1, T2, T3, and T4. These traps are likely attributed to the known defect levels in 4H-SiC as shown in the last column.

Out of the four samples investigated, only the PS has measurable CDLTS signal. As for the other CR, CE, and CE+PS samples, no CDLTS peak signal was detected. This can be due to the absence of deep level defects with high density in these samples, or due to the limitation of the system's sensitivity.

Fig. 6.16 shows the CDLTS results obtained for the PS sample. It can be seen that a very strong CDLTS peak exists, which can be deconvoluted into four transient peaks, denoted as T1, T2, T3 and T4, which occur at the temperatures 408.0 K, 456.2 K, 507.2 K and 529.0 K respectively. Based on the result shown in Fig. 6.16, a series of Arrhenius plots can be obtained and are shown in Fig. 6.17. From these plots, the trap parameters, i.e. trap level measured with respect to the conduction band edge E_C-E_T, capture cross section σ_n, and trap density, can be estimated for the four traps and the results are listed in Table 6.10. It worth noting that the parameters used in the calculation are: doping level $N_D = 2\times10^{15}$ cm^{-3}, electron density-of-states effective mass $m_n = 0.77m_0$ [3], and the coefficient $\gamma_n = 2.5025\times10^{21}$ cm^{-2}s^{-1}K^{-2} [3]. It is noticed that all the four traps have very high trap density ranging from about 4×10^{13} cm^{-3} for T1 to 1.5×10^{15} cm^{-3} for T3. The result suggests a severely damaged surface layer introduced by Ar ion physical sputtering for the PS sample.

6.7 Summary

In this chapter, plasma etching induced damage (PEID) on *n* type 4H-SiC wafers was studied using SBDs fabricated that were subjected to different etching conditions. Three samples subjected to plasma etching conditions with distinctly different characteristics, namely chemical plasma etching (CE), physical sputtering (PS), and reactive ion etching (CE+PS), were investigated. A control sample (CR) with an unetched surface was also studied to serve as a reference for comparison. The capacitance-voltage, current-voltage and deep level transient spectroscopy characteristics of these SBD samples were measured and analyzed to extract useful parameters such as SBH, series on-resistance and ideality factor. It is found that chemical etching results in a lower SBH and leads to a higher leakage current for the SBD. However, the ideality factor and series on-resistance are not much affected compared to the CR sample. The lowering of the SBH due to chemical etching is attributed to the formation of a carbon-rich layer at the surface. In contrast, physical sputtering is found to lead to severe damages, resulting in a very high series on-resistance, a very large ideality factor. The CDLTS results reveal that four deep-level defects with very high density exist inside the depletion layer of the SBDs. For the CE+PS sample, inhomogeneity has been observed at the Schottky interface, and can be modeled by two SBDs with different SBHs connected in parallel. The SBD with a lower SBH and high leakage current is associated with the chemical etching induced damage, while the one with a higher SBH is associated with the surface that is free of chemical etching induced damage. However, it still suffers from slight damage due to physical sputtering.

Chapter 7

Conclusions and Recommendations

7.1 Conclusions

In this thesis, the etching process for *n* type bulk 4H-SiC have been studied using reactive ion etching (RIE) and electron cyclotron resonance (ECR) plasma etching techniques based on halogen plus oxygen plasma.

The plasma etching of n^+ type bulk 4H-SiC using the RIE process and CHF_3+O_2 plasma was first studied. The etch rate, surface morphology, surface roughness and surface elements were studied by varying the O_2 fraction, R.F. power and process pressure. While F is found to play a dominant role in the plasma etching process, the role of O is found to be multiple. At low O_2 fractions, the additive oxygen enhances the etch rate by increasing the F concentration, while at high fractions, it dramatically lowers the etch rate by diluting F concentration and inducing the formation of an oxide-like layer by chemisorption. An increase in R.F. power greatly enhances the etch rate by providing higher neutral radical density, higher positive ion density, as well as larger impinging ion energy. In contrast, with increasing process pressure, the etch rate decreases due to the weakening of impinging ion energy. The surface roughness is affected mainly by physical ion bombardment controlled by the D.C. self-bias, and to a lesser extent by the O_2 fraction. At low D.C. self-bias, r.m.s. surface roughness of the

etched surface is basically proportional with the D.C. bias. Auger electron spectroscopy (AES) study has related such surface roughness to the micromasking effect induced by Al clusters and a C rich layer on the surface. The micromasking effect can be removed at high D.C. self-bias. When the D.C. self-bias is higher than a threshold value of between -320 and -330 V, no micromasking effect has been observed regardless of the value of O_2 fraction and the etched surface is mirror clean. An optimized recipe was developed in this study. It gives the highest etch rate of 35.6 nm/min and an r.m.s. surface roughness of 1.65 nm, with the O_2 fraction, R.F. power and process pressure set at 20%, 200 W (1.13W/cm^2), and 100 mTorr respectively. In this study, we have gained an insight into 4H-SiC plasma etching mechanism and the nature of the micromasking effect and its relation with the D.C. self-bias.

Next, we have developed a numerical model for the simulation of ECR plasma etching of 4H-SiC, based on a feed-forward neural network (FNN) trained by the BFGS (Broyden, Fletcher, Goldfarb, and Shanno) optimization algorithm using our experimental etch rate results. This is the first time that the algorithm has been used for the training of FNN in the modeling of plasma etching. To establish its effectiveness and superiority, the modeling results were compared with those obtained from the same FNN, but trained by the conventional back propagation (BP) algorithm. The BFGS algorithm has been found to fit the experimental etch rate results with very good accuracy. The r.m.s. error and maximum error of cross-validation (CV) test for the BFGS algorithm are less than 5% and ±10%, respectively, while the errors for the training samples are even lower. These values are much better compared to those obtained using the conventional BP algorithm, which so far has been commonly used for the modeling of plasma etching. The FNN trained by the BFGS algorithm developed in this work is able to provide reliable and accurate simulation results,

which are important towards the understanding of the ECR plasma etching mechanism and the designing of etching process recipes for practical application. It can also be applied to other aspects of plasma etching, such as providing real-time control, plasma diagnosis data analysis.

The FNN developed in this work has been used to systematically model the ECR plasma etching of n^+ type bulk 4H-SiC with SF_6+O_2 plasma. Experimental etch rate data that followed a five-level Box-Wilson central composite design (CCD) were used for the training of the FNN. The ECR plasma etch rate was studied by varying over a wide range the key process parameters: microwave power, D.C. bias, process pressure and O_2 fraction. The interaction of these process parameters and their resultant effects on the etch rate were also analyzed and interpreted physically in terms of the ECR plasma etching mechanism that involves both chemical and physical etching. It is found that by varying the O_2 fraction and process pressure, optimized etch rate peaks can be achieved. Increasing the D.C. bias and microwave power are found to result in optimized etch rate peaks occurring at higher O_2 fractions and process pressures, respectively. In addition, increasing the D.C. bias or microwave power will also increase the etch rate. However, this increase is saturated at higher D.C. bias, which however, does not occur at higher microwave power. Hence, by controlling these process parameters, it is possible to develop optimized etching recipes for 4H-SiC to cater for various applications, such as power electronic devices, microelectromechanical systems (MEMS) or via hole formation, which have different requirements on etching anisotropy, etched structure aspect ratio, etch rate and etching induced damage.

Following the simulation of the ECR plasma etch rate, experimental ECR SF_6+O_2 plasma etching of n^+ doped bulk 4H-SiC was studied in terms of the role of oxygen in the etching process. The chemical etching of carbon by oxygen is found to be insignificant even at high O_2 fraction. The surface roughness is noted to increase with increasing O_2 fraction, which is attributed to surface oxidation and oxygen ion related physical ion bombardment. Nevertheless, overall the surface roughness is still small, of about 1.7 nm, and the etched 4H-SiC surfaces are relatively smooth. This has been attributed to the high D.C. bias applied that avoided the formation of Al clusters and C rich-layer on the etched surface. The highest etch rate achieved for 4H-SiC using the ECR plasma etching is 79.1 nm/min, which occurs at the process conditions of 550 W microwave power, -200 V D.C. bias, 4 mTorr process pressure, and 60% O_2 fraction.

The plasma etching induced damage (PEID) on *n* type 4H-SiC wafers was studied using Schottky barrier diodes (SBDs) fabricated in this work that were subjected to different etching conditions. Three samples etched with RIE plasmas with characteristics that were mainly dominated by chemical etching (CE), physical sputtering (PS), and reactive ion etching (CE+PS), were investigated. A control sample (CR) with an unetched surface was also studied to serve as a reference for comparison. The capacitance-voltage, current-voltage and deep level transient spectroscopy (CDLTS) characteristics of these SBD samples were measured and analyzed to extract important device parameters such as the Schottky barrier height (SBH), series on-resistance and ideality factor. It is found that chemical etching results in a lower SBH and leads to a higher leakage current for the CE sample. However, the ideality factor and series on-resistance are not much affected compared to the CR sample. The lowering of the SBH due to chemical etching is attributed to the

formation of a carbon-rich layer at the surface. In contrast, physical sputtering is found to lead to severe damages to the PS sample, resulting in a very high series on-resistance and a very large ideality factor. The CDLTS results reveal that four deep-level defects with very high density exist inside the depletion layer of the PS sample. For the CE+PS sample, inhomogeneity has been observed at the Schottky interface, and can be modeled by two SBDs with different SBHs connected in parallel. The SBD with a lower SBH and high leakage current is associated with the chemical etching induced damage, while the other one with a higher SBH is associated with the surface that is free of chemical etching induced damage. However, it still suffers from slight damage due to physical sputtering. This study reveals how the plasma etching characteristics, which comprise chemical and physical etching, have contributed to the PEID and its consequent effects on the electrical characteristics of the SBDs

7.2 Recommendations

There are several recommendations for future research work that can be further pursued.

1. To further understand the plasma etching process, it will be important to be able to directly monitor the plasma characteristics through techniques such as optical emission spectroscopy, laser induced fluorescence and Langmuir probe. These techniques allow the ion density, ion energy, electron temperature, electron energy distribution function, plasma potential of the plasma to be measured directly and hence provide a useful link to understand and correlate the plasma etching process conditions to the PEID.

2. Using the artificial neural network that we have developed in this work, and coupled with the plasma diagnostic and monitoring tools as mentioned above, we can develop real time control of the plasma process. This is important given the open-loop nature of the RIE process which is not very robust and requires frequent tuning. Such an approach will lead to improvement in the etching process, such as better control of selectivity, uniformity, anisotropy and etch depth.

3. In our study, we have used SBD as a test vehicle to study the PEID due to its sensitivity to the Schottky interface quality. With the development of techniques to deposit high quality dielectric film, another very useful test vehicle, metal-insulator-semiconductor capacitor (MISC) can be used to study the PEID. Such studies are also important in view of the current development of power metal-oxide-semiconductor-field-effect-transistor (MOSFET), and allow the understanding of the effects of PEID on the electrical characteristics of such devices.

Author's Publications

Journal Papers

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