

# Design and Analysis of Ultra Low Power True Single Phase Clock CMOS 2/3 Prescaler

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**Abstract**—In this paper the power consumption and operating frequency of true single phase clock (TSPC) and extended true single phase clock (E-TSPC) frequency prescalers are investigated. Based on this study a new low power and improved speed TSPC 2/3 prescaler is proposed which is silicon verified. Compared with the existing TSPC architectures the proposed 2/3 prescaler is capable of operating up to 5 GHz and ideally, a 67% reduction of power consumption is achieved when compared under the same technology at supply voltage of 1.8 V. This extremely low power consumption is achieved by radically decreasing the sizes of transistors, reducing the number of switching stages and blocking the power supply to one of the D flip-flops (DFF) during Divide-by-2 operation. A divide-by-32/33 dual modulus prescaler implemented with this 2/3 prescaler using a Chartered 0.18  $\mu\text{m}$  CMOS technology is capable of operating up to 4.5 GHz with a power consumption of 1.4 mW.

**Index Terms**—D-flip-flop (DFF), dual modulus prescalers, frequency dividers, frequency synthesizer, high speed digital circuits, true single-phase clock (TSPC).

## I. INTRODUCTION

THE HIGH SPEED dual modulus prescaler is a critical functional block in frequency synthesizers which uses wide-band pulse swallow frequency dividers. The prescaler operates at the highest frequencies and consumes more power than other circuit blocks of the frequency synthesizer. In a pulse swallow frequency divider, the prescaler has two selectable division ratios,  $N$  and  $N + 1$ . It is combined with programmable counters  $P$  and  $S$  as in Fig. 1, to perform a programmable division ratio of  $(N \times P + S)$ .

The prescaler is a synchronous circuit which is formed by D flip-flops and additional logic gates. Due to the incorporation of additional logic gates between the flip-flops to achieve the two different division ratios, the speed of the prescaler is affected and the switching power increases. Various flip-flops have been proposed to improve the operating speed of dual-modulus prescalers. The optimization of the D flip-flop in the synchronous stage is essential to increase the operating frequency and reduce the power consumption. The high speed operation of MOS transistors is limited by their low transconductance. Therefore, dynamic and sequential circuit techniques or clocked logic gates such as, true single phase clocks [1]–[4], must be

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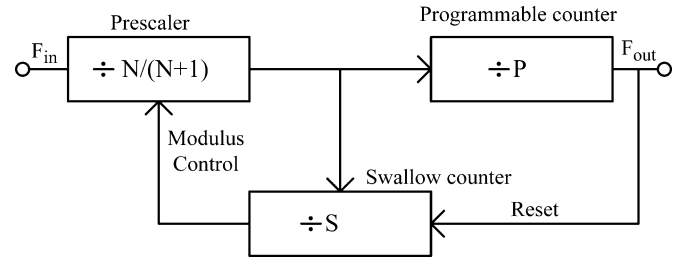


Fig. 1. Topology of the Pulse Swallow frequency divider.

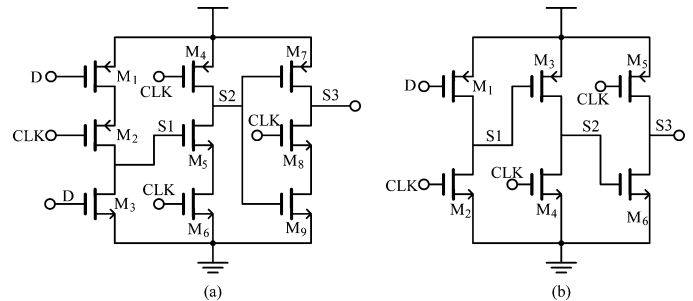


Fig. 2. (a) TSPC flip-flop. (b) E-TSPC flip-flop.

used in designing synchronous circuits to reduce circuit complexity, increase operating speed, and reduce power dissipation.

The state of the art CMOS  $N/(N + 1)$  prescalers have achieved maximum operating frequencies up to 24 GHz [5] using current mode logic (CML) [6], [7], architectures at the expense of power consumption. The fastest frequency dividers were designed at fixed division ratios [8]. In this paper, the power consumption and frequency of operation of TSPC and E-TSPC 2/3 prescalers are analyzed and an ultra low power TSPC 2/3 prescaler is proposed. Based on this design a 32/33 prescaler is then implemented, which is highly suitable for high resolution fully programmable frequency synthesizers [9].

## II. ANALYSIS OF E-TSPC AND TSPC PRESCALERS

In this section, the power consumption and the maximum operating frequency of the E-TSPC [10] and TSPC [1], [11] based flip-flops are analyzed. In each stage, an E-TSPC flip-flop uses only two transistors while a TSPC flip-flop uses three transistors as shown in Fig. 2.

Of various dynamic logic CMOS circuit techniques, TSPC dynamic CMOS circuit is operated with one clock signal only to avoid clock skew problems. The load capacitances of both TSPC and E-TSPC flip-flops in divide-by-2 mode (node S3 connected

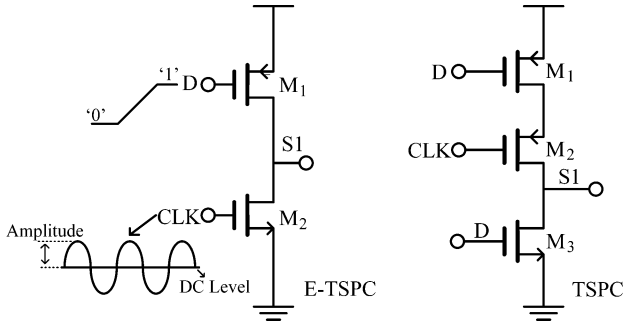


Fig. 3. Schematic of the first stage of E-TSPC and TSPC flip-flops.

to input D), are manually calculated using the method described in [12] and [13] given by

$$C_{L\_TSPC} = C_{dbM8} + 2C_{gdM8} + C_{dbM7} + 2C_{gdM7} + C_{gM3} + C_{gM1} \quad (1)$$

$$C_{L\_ETSPC} = C_{dbM6} + 2C_{gdM6} + C_{dbPM5} + 2C_{gdM5} + C_{gM1}. \quad (2)$$

From (1) and (2) the load capacitance of the TSPC flip-flop is higher than that of the E-TSPC flip-flop resulting in higher switching power for the TSPC flip-flop since it is directly depends on the output load capacitance as shown in (3)

$$P_{switching} = f_{clk} C_L V_{dd}^2. \quad (3)$$

Here,  $C_L$  is the load capacitance and  $f_{clk}$  is the operating frequency. However, there is a period during which a direct path exists between the supply voltage and ground resulting in the short circuit power. The short-circuit power depends on the transistor sizes and rise and fall times of the input signal. The analysis in [14] shows that having lesser load capacitance results in lower short circuit power. However, it is well known that in a 2/3 prescaler, the E-TSPC flip-flop uses lesser switching power, but significantly more short-circuit power. This short-circuit power exists every 4th clock cycle when the E-TSPC flip-flop is operated as a divide-by-2 circuit [15]. It is also stated that the short circuit power in E-TSPC circuits is higher and dependent on the transistor sizes assuming that the output of the voltage controlled oscillator (VCO) is the full swing signal. In reality at the GHz range in many applications, the VCO output is not a full swing signal and the output signal has a certain DC level which affects the short circuit power of both logic types.

To verify the dependence of power consumption against the DC level and amplitude of the sinusoidal clock waveform, single stages of both circuits shown in Fig. 3 are simulated. Two sets of simulations are carried out, one with same size transistors for both TSPC and E-TSPC stages and the other being with same driving capability (TSPC PMOS transistor are twice the widths of the E-TSPC PMOS transistors) to have a fair comparison for the two circuits. Due to the constraints of the length of the paper, only simulation results for the same driving capability are shown in Fig. 4. For each fixed DC level (0.7–1.2 V) the amplitude of the clock signal is varied from 400–600 mV and input D is switched from logic “0” to logic “1” with a rise time of 70 ps. In both cases TSPC stage consumes lesser power compared to that of the E-TSPC stage. The main aim here is to show how the

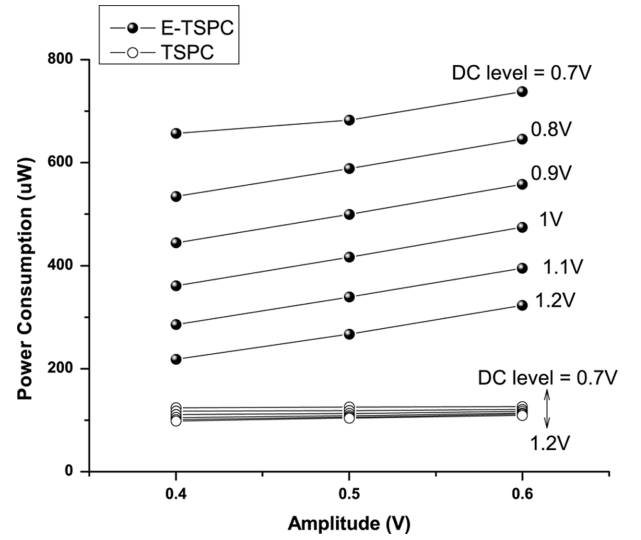


Fig. 4. Power consumption against different DC levels and amplitude of clock signal for single stages of E-TSPC and TSPC.

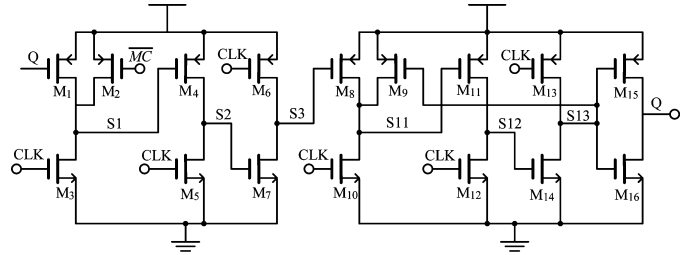


Fig. 5. E-TSPC 2/3 prescaler in [15].

power consumption is affected by the variation in the DC level and the amplitude of the clock signal obtained from the VCO which is sinusoidal and its DC level and amplitude can be included in the design of the VCO in a phase locked loop (PLL). The simulation results in Fig. 4 indicate that for the E-TSPC circuit, the DC level should be high for negative edged clock circuits to obtain low power consumption and power consumption is significantly varied from 200–700 uW with respect to the DC level and amplitude of the clock signal. For TSPC, the power consumption remains almost constant for the same variation of the DC level and amplitude of the clock signal. The TSPC circuits can be directly driven from the VCO output with high DC level and amplitude from 400–600 mV. E-TSPC circuits also need larger amplitude for the clock signal compared to that of TSPC circuits. This analysis suggests TSPC is a better choice for ultra low power applications. From the results a DC level between 0.7–1.2 V and an amplitude between 400–600 mV are chosen for the clock signal that drives the TSPC prescaler.

### III. E-TSPC BASED 2/3 PRESCALER

The E-TSPC architecture has the merit of a higher operating frequency compared to that of the TSPC architecture. A simplified E-TSPC divide-by-4/5 prescaler is proposed in [16] to achieve the operating frequency of 1.2 GHz. An improved speed and optimized E-TSPC 2/3 prescaler unit is proposed in [15] where the digital gates are embedded into the flip-flops to effectively reduce the propagation delay and power consumption.

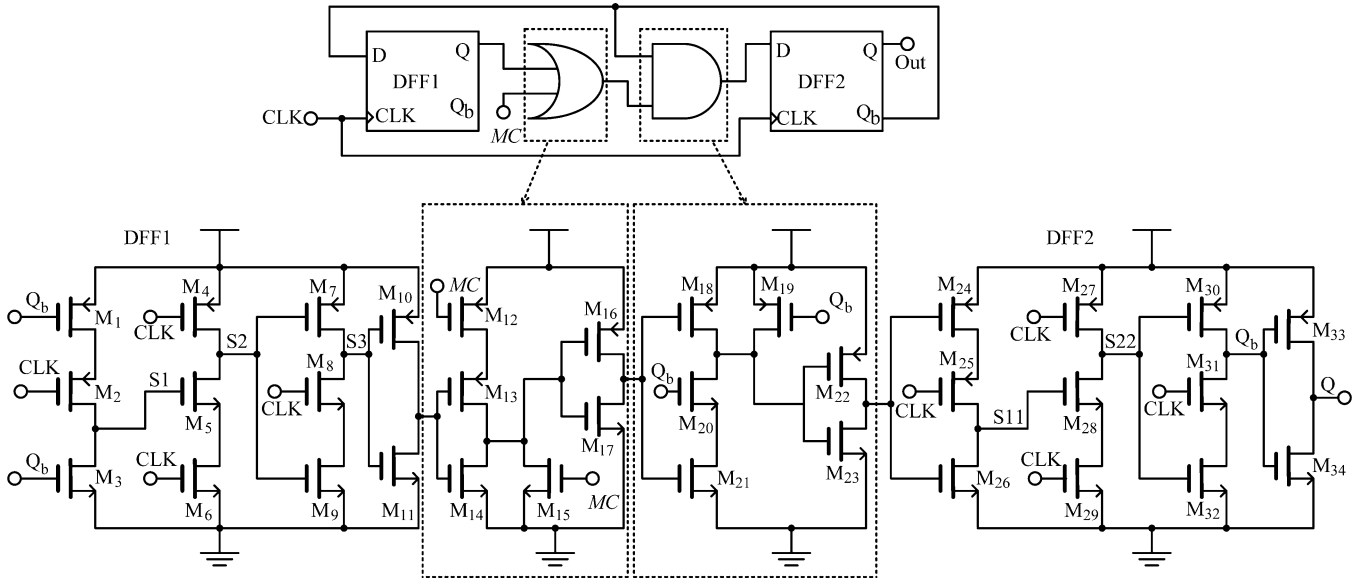


Fig. 6. Conventional TSPC 2/3 prescaler circuit and equivalent gate level schematic.

The problem associated with the 2/3 prescaler unit in [17] is that the both D flip-flops switch at half of the input frequency even if one of the D flip-flop does not participate in the divide-by-2 function resulting in unnecessary power consumption. A simplified and optimized E-TSPC 2/3 prescaler unit is proposed in [15] which reduces the power consumption by 25% is shown in Fig. 5.

The 2/3 prescaler unit in [15] uses two D flip-flops (DFF) and two AND gates rather than an AND gate and OR gate as in [17] to effectively block the switching activities and reduce the short circuit power in DFF1. The first AND gate is embedded in the first stage of DFF1 with one of the input is controlled by  $\overline{MC}$  and the other AND gate is embedded in the first stage of DFF2. During the divide-by-2 mode when control signal  $\overline{MC}$  is high, DFF1 is blocked at the input and the nodes S1, S2, S3 of the DFF1 have logical values of “1,” “0,” and “1” respectively blocking the switching activities. This architecture still has short circuit power in the first stage of DFF1 and all stages of DFF2. Since the first stage of DFF1 is driven by a voltage controlled oscillator (VCO) whose output signal is sinusoidal with a certain DC level in most of frequency synthesis applications, the power consumption in the first stage of DFF1 is very high as discussed in Section II.

The prescaler in [15] eliminates only the switching power in DFF1 during the divide-by-2 mode but does little to the short circuit power making the circuit not suitable for ultra low power applications. The re-simulated results shows that the 2/3 prescaler unit in [15] has the maximum operating frequency of 6.7 GHz with a full swing sinusoidal signal while the 2/3 prescaler unit in [17] has the maximum frequency of operation around 5.5 GHz at supply of 1.5 V. This analysis shows that TSPC architectures are more suitable for ultra low power applications since they have lower short circuit power, while their switching power and propagation delay can be reduced with different techniques described in [2]–[4], [18]. In Section IV an improved speed and low power TSPC 2/3 prescaler is proposed which reduces the switching power consumption, improves frequency of operation and in the Section V an ultra low power TSPC 2/3 prescaler is

proposed which reduces the total power consumption in the divide-by-2 mode by 67% theoretically, compared to that of existing TSPC 2/3 prescaler units.

#### IV. DESIGN I: IMPROVED TSPC 2/3 PRESCALER

In this section, a new TSPC 2/3 prescaler with improved speed and low power is proposed. The conventional 2/3 prescaler consists of two D flip-flops, an OR gate and a AND gate as shown in Fig. 6. In a conventional divide-by-2/3 TPSC prescaler, DFF1 is loaded only by an OR gate, while DFF2 is loaded by an AND gate, DFF1 and an output stage making up a much larger load. Due to the large load on DFF2, it limits the speed of operation and this topology causes substantial power dissipation. The difficulty to embed the OR, AND gates into the DFF introduces additional propagation delay by the digital gates which limits the speed of conventional 2/3 prescaler.

The conventional TSPC 2/3 prescaler unit has lower short circuit power compared to the 2/3 prescalers proposed in [15] and [17], but has higher switching power due to large switching capacitances at output node of the each stage. The total load capacitance  $C_L$  at output node Qb of the conventional 2/3 prescaler unit is

$$C_L = C_{dbM30} + C_{dbM31} + 2(C_{gdM31} + C_{gdM30}) + C_{gM1} + C_{gM3} + C_{gM19} + C_{gM20} + C_{gM33} + C_{gM34}. \quad (4)$$

The switching power  $P_{\text{switching}}$  contributed by the conventional TSPC 2/3 prescaler with 12 switching nodes is given by

$$P_{\text{switching}} = \sum_{i=1}^{12} f_{\text{clk}} C_{Li} V_{dd}^2 \quad (5)$$

where the  $C_{Li}$  is the load capacitances of node S1, S2, S3 of DFF1, DFF2, logic gates and  $f_{\text{clk}}$  is the frequency of the input clock signal. The total power consumption in the conventional prescaler is mainly due to switching power contributed by the node capacitances of 12 stages. TSPC-based 4/5, 8/9 prescaler

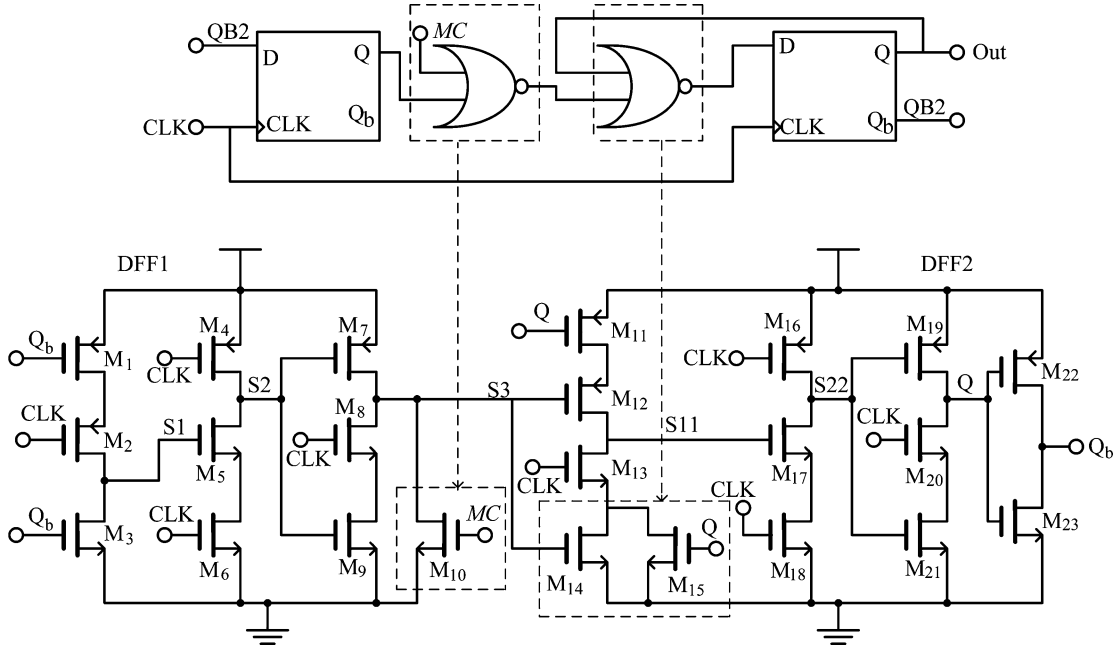


Fig. 7. Proposed Design-I TSPC 2/3 prescaler circuit and equivalent gate level schematic.

units are proposed in [19] which improves speed by 13% compared to that of the conventional prescaler, which can work up to 1.9 GHz. The prescaler proposed in [20] improves the speed by using two NOR gates in the place of an OR, AND gates. Here one of the NOR gates drive the DFF1 and other NOR gate drives the DFF2. This prescaler is implemented with CML [6] logic flip-flops which consume large power and the digital gates embedded in to the CML logic flip-flops needs buffers at the output stage to create sufficient output voltage swing [21]. An improved speed and low power 2/3 prescaler implemented in the TSPC logic style is proposed as in Fig. 7 similar to the prescaler in [20], the proposed prescaler uses two embedded NOR gates instead of an AND gate and an OR gate as the conventional TSPC 2/3 prescaler.

In the proposed 2/3 prescaler, the first NOR gate is embedded in to the third stage of DFF1 using a single NMOS transistor M10, whose drain is connected to node S3 of DFF1 and the other NOR gate is embedded in to the first stage of DFF2. By doing so, an extra inverter driven by node S3 of DFF1 and additional stages introduced by the digital gates in between DFF1 and DFF2 of the conventional TSPC 2/3 prescaler are eliminated reducing the number of switching nodes to 7 in the proposed prescaler. The substantial reduction of the nodes in the proposed 2/3 prescaler reduces the switching power  $P_{\text{switching\_Design-I}}$  as given by

$$P_{\text{switching\_Design-I}} = \sum_{j=1}^7 f_{\text{clk}} C_{Lj} V_{dd}^2. \quad (6)$$

The total capacitance at the output node Q of the proposed 2/3 prescaler is given by (7)

$$C_{L\_Design-I} = C_{dbM19} + C_{dbM20} + 2(C_{gdM20} + C_{gdM19}) + C_{gM11} + C_{gM15} + C_{gM22} + C_{gM23}. \quad (7)$$

The total load capacitance ( $C_{L\_Design-I}$ ) of the proposed 2/3 prescaler at the output node "Q" is significantly reduced compared to the load capacitance of the conventional 2/3 prescaler

resulting in a reduction of propagation delay and power consumption. The reduction of switching power in the proposed Design-I 2/3 prescaler compared to the conventional TSPC 2/3 prescaler when both the circuits are designed with same transistor sizes is given by (8)

$$P_{\text{switching-saved}} = \sum_{i=1}^{12} f_{\text{clk}} C_{Li} V_{dd}^2 - \sum_{j=1}^7 f_{\text{clk}} C_{Lj} V_{dd}^2. \quad (8)$$

In this analysis, both the circuits conventional TSPC 2/3 prescaler and the Design-I 2/3 prescaler are designed using same width of 3  $\mu\text{m}$  for the PMOS and 2  $\mu\text{m}$  for the NMOS transistors. The node capacitances at each output node for both circuits are assumed as the same since all the devices have same aspect ratio. Based on this assumption, the switching power saved by the Design-I prescaler is almost 42% and its speed is improved by 1.3 times compared to that of the conventional TSPC 2/3 prescaler, which are also verified by simulation and measurement results. Since there is reduction of total number stages in the Design-I prescaler, the short circuit power also reduced significantly.

The proposed 2/3 prescaler has higher input sensitivity which enables the divider to be coupled directly to a wide range VCO's, without any need of external buffers as in the prescalers in [17] and [15]. By fixing the DC level of VCO output signal, the power consumption can be substantially reduced at the expense of the reverse isolation [22] due to the absence of buffers. Apart from the reduction of propagation delay and power consumption, the proposed prescaler reduces the area since it uses only 23 transistors to perform divide-by-2 or divide-by-3 compared to the conventional prescaler which uses as many as 32 transistors. The output "Q" drives transistors M11 and M14 of DFF2 and "Qb" drives transistors M1 and M3 such that loading on the output "Qb" is reduced compared to conventional 2/3 prescaler. This technique allows the proposed

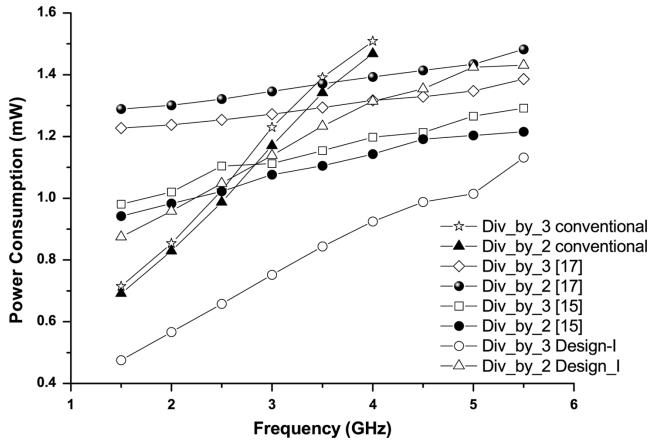


Fig. 8. Frequency versus power consumption of different prescalers.

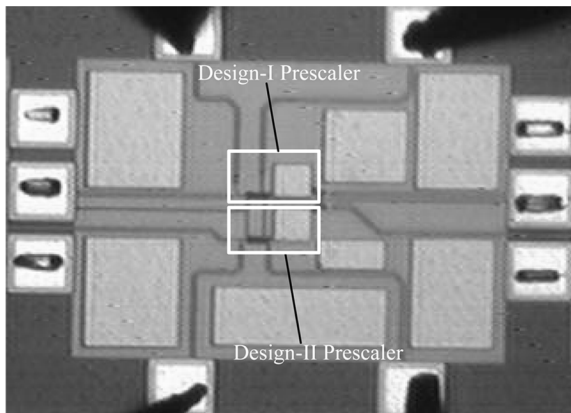


Fig. 9. Die photograph of the proposed TSPC 2/3 prescaler.

2/3 prescaler to reduce the propagation delay and switching power.

## V. SIMULATION AND MEASUREMENT RESULTS

The simulations are performed for all the above mentioned state-of-art prescalers and the proposed prescaler using the Cadence Spectre and the Chartered 0.18  $\mu\text{m}$  CMOS technology. Fig. 8 shows the power consumption against the frequency for the E-TSPC based prescalers in [17], [15] at 1.5 V power supply and the conventional and proposed TSPC 2/3 prescaler at 1.8 V power supply to have fair comparison since the maximum operating frequency of the E-TSPC based prescaler is higher than that of the TSPC based prescaler. Even though, the prescaler unit in [15] uses a different architecture to reduce the power, at higher frequencies, its power consumption is almost same as that of the prescaler in [17]. It is also found that from the simulation results, the total power consumed by the conventional TSPC 2/3 prescaler unit is lesser than that of E-TSPC based prescalers due to lower short circuit power consumption. The simulation results shows that the conventional 2/3 prescaler can only operate up to a maximum frequency of 4.2 GHz.

Fig. 8 clearly indicates that the power consumption of the proposed unit is higher in the divide-by-2 mode, which is almost double the power consumed during the divide-by-3 mode. From the simulation results at 2.4 GHz, it is observed that the proposed prescaler draws a current of 549  $\mu\text{A}$ , 251  $\mu\text{A}$

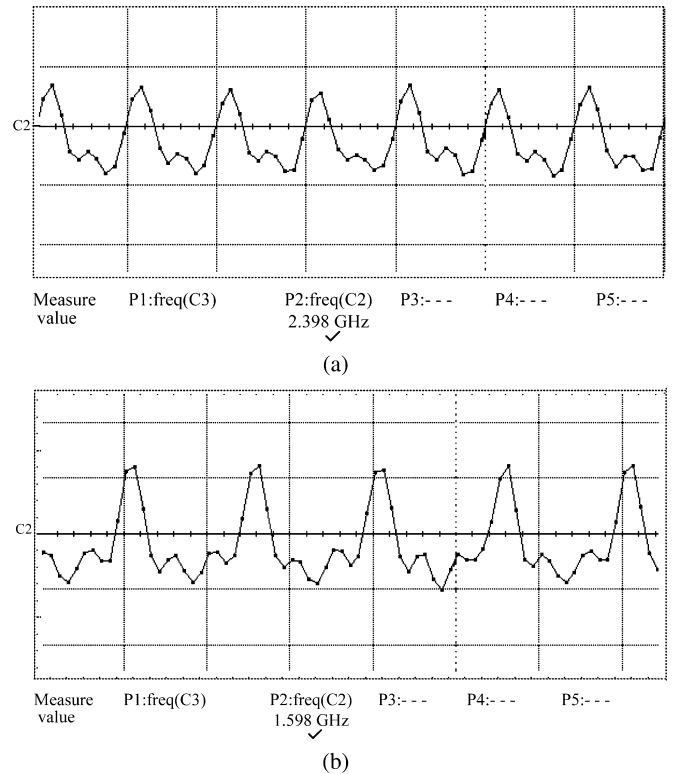


Fig. 10. Measured waveforms of Design-I prescaler at 4.8 GHz. (a) divide-by-2 mode, (b) divide-by-3 mode.

in the divide-by-2 and divide-by-3 modes respectively. The die photograph of the proposed Design-I 2/3 prescaler is shown in Fig. 9 together with the Design-II ultra low power 2/3 prescaler which is described in the next section. From the measurement results, the maximum frequency of operation of the Design-I prescaler is 4.9 GHz with a power consumption of 1.35 mW. Fig. 10(a), (b) shows the measured output waveform of the proposed Design-I prescaler at 4.8 GHz in divide-by-2 and divide-by-3 modes respectively.

The power consumption of the proposed TSPC 2/3 prescaler is 2.7, 2.2 times less than the power consumption of the E-TSPC prescalers in [17], [15] and 1.6 times less than that of the conventional 2/3 TSPC prescaler when simulations for all the circuits are carried at 1.8 V power supply. During the divide-by-2 mode when control signal MC is logically high, the transistor M10 is turned on, allowing a direct path from the supply to ground if transistor M7 is turned on. This direct path results in the high short circuit power in the third stage of DFF1.

In the Fig. 11 it is shown that node S2 will go low for half of the input clock period during which transistor M7 is turned on creating a direct path from supply to the ground since transistor M10 is always on during divide-by-2 mode. The shadow lines indicate the period during which short circuit power is exhibited in the 3rd stage of DFF1. However, the total power  $P_{2/3\_Design-I}$  consumed by the proposed Design-I prescaler in divide-by-2 mode is the sum of the switching in DFF2, DFF1, the short circuit power in DFF2 and the short circuit power in 3rd stage of the DFF1 as in (9)

$$P_{2/3\_Design-I} = P_{\text{switching-DFF1}} + P_{\text{short-S3-DFF1}} + P_{\text{short-DFF2}} + P_{\text{switching-DFF2}} \quad (9)$$

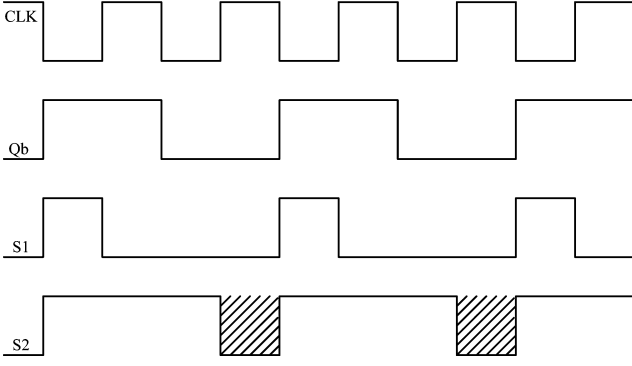


Fig. 11. Divide-by-2 operation of the proposed 2/3 prescaler unit.

In the divide-by-2 mode both DFF1, DFF2 toggle at half of the input frequency. Since DFF1 has 3 stages and DFF2 has 4 stages, the total switching power of DFF1 and DFF2 during divide-by-2 mode is given by (10), (11)

$$P_{\text{switching\_DFF2\_Design-I}} = \sum_{i=1}^4 f_{\text{clk}} C_{Li} V_{dd}^2 \quad (10)$$

$$P_{\text{switching\_DFF1\_Design-I}} = \sum_{i=1}^3 f_{\text{clk}} C_{Li} V_{dd}^2. \quad (11)$$

Here,  $C_{Li}$  is the load capacitance at the output node of each single stage in the Design-I prescaler. The flip-flop DFF1 of the Design-I prescaler consumes double the power consumed by DFF2 during divide-by-2 operation. When simulations are carried from 2 to 5 GHz, the 3rd stage of DFF1 consumes around 1.6 times the power consumed by DFF2. The simulation and measurement results indicate that the Design-I prescaler saves more than 50% of power consumption by other prescalers only in divide-by-3 mode. The power saved is around 25% in the divide-by-2 mode when compared with the power consumption of the conventional TSPC 2/3 prescaler above 2 GHz. An ultra low power TSPC 2/3 prescaler is proposed in the Section VI which ideally reduces the power consumption of DFF1 in the proposed 2/3 prescaler in Design I to zero during the divide-by-2 mode.

## VI. DESIGN-II: ULTRA LOW POWER TSPC 2/3 PRESCALER

In this section an ultra low power 2/3 prescaler (Design-II) is proposed as shown in Fig. 12, a further improved version of the Design-I prescaler. As shown in Fig. 12, an extra PMOS transistor M1a is connected between the power supply and flip-flop DFF1 whose input is the control logic signal MC. Ideally, DFF1 should not be active during the divide-by-2 mode as only DFF2 participates in the divide-by-2 operation. In this new design, when the control logic MC is logically high during the divide-by-2 mode, the PMOS transistor M1a is turned-off and DFF1 is disconnected from the power supply. Thus by switching off DFF1 completely during the divide-by-2 mode, the short circuit power and switching power of DFF1 is removed completely.

The divide-by-3 operation is performed when the control signal MC goes logically low during which the PMOS transistor M1a turns on and supplies power to DFF1. The divide-by-3 operation is performed as it is done by the proposed prescaler

of Design-I. However in the Design-II, DFF1 operates at a reduced supply voltage due to the V<sub>ds</sub> drop across transistor M1a. Since the frequency of operation is directly related to the power supply, the maximum operating frequency of Design-II becomes lower than that of the proposed 2/3 prescaler of Design-I. The PMOS transistor M1 in Design-I is removed in Design-II thus making the first stage of DFF1 similar to that of first stage in prescalers designed using E-TSPC flip-flops [17]. With this modification, the maximum frequency of operation of the Design-II is improved and is almost same as that of the Design-I. The die photograph of the proposed ultra low power 2/3 prescaler of Design-II is shown in Fig. 8.

The power consumed by the circuit of Design-II in the divide-by-2 mode is given by the switching and short circuit power of DFF2 alone as in (12)

$$P_{2/3\_Design-II} = P_{\text{switching\_DFF2}} + P_{\text{short\_DFF2}}. \quad (12)$$

### A. Power Saving Analysis for the Divide-by-2 Mode

The percentage of power saved by the Design-II prescaler in the divide-by-2 mode is ratio of the difference in power consumed by Design-I and Design-II prescalers to the power consumed by Design-I prescaler as in (13)

$$P_{2/3\% \text{ saved}} = \frac{P_{2/3\_Design-I} - P_{2/3\_Design-II}}{P_{2/3\_Design-I}} * 100. \quad (13)$$

Since both circuits use same flip-flop DFF2, which consumes the same power in both the circuits during divide-by-2 and divide-by-3 modes, the power saved by the Design-II prescaler is given by subtracting (12) from (9)

$$\begin{aligned} P_{2/3\_Design-I} - P_{2/3\_Design-II} \\ = P_{\text{switching\_DFF1\_Design-I}} + P_{\text{short\_S3\_DFF1\_Design-I}}. \end{aligned} \quad (14)$$

The flip-flops DFF1, DFF2 of Design-I prescaler are simulated with separate power supply to find out the approximate relation between the power consumption of both D flip-flops during the divide-by-2 operation. Fig. 13 shows the simulated power consumption of the both the D flip-flops and the results indicate that the power consumed by DFF1 is approximately twice the power consumed by the DFF2. Moreover, from the theoretical analysis it is found that the power consumed by the DFF1 during divide-by-2 operation is almost twice of the power consumed by DFF2. This assumption makes (14) simplified

$$\begin{aligned} P_{\text{switching\_DFF1\_Design-I}} + P_{\text{short\_S3\_DFF1\_Design-I}} \\ = 2(P_{\text{switching\_DFF2\_Design-I}} + P_{\text{short\_DFF2\_Design-I}}). \end{aligned} \quad (15)$$

Thus the power consumed in the divide-by-2 mode by the Design-I prescaler in (9) is rewritten as (16)

$$P_{2/3\_Design-I} = 3 * (P_{\text{switching\_DFF2\_Design-I}} + P_{\text{short\_DFF2\_Design-I}}). \quad (16)$$

Thus substituting (15) and (16) in (12), the amount of power saved by the Design-II 2/3 prescaler is equal to 67%.

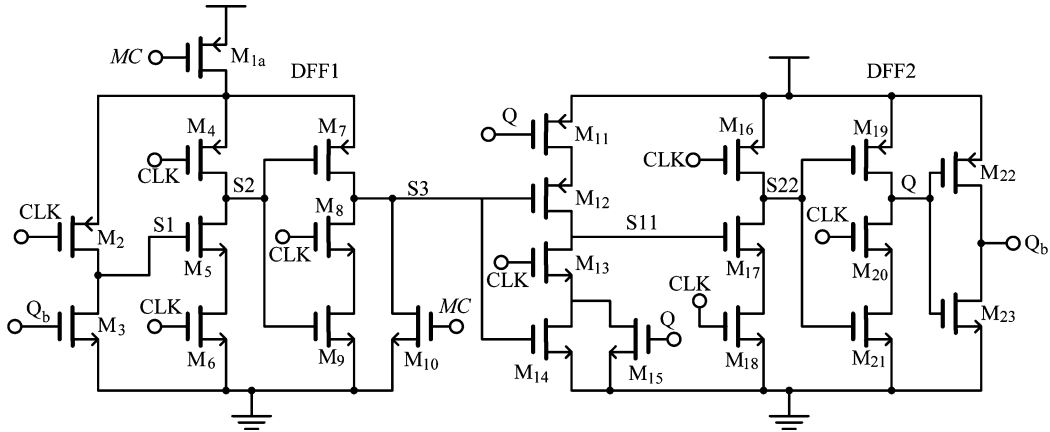


Fig. 12. Proposed Design-II TSPC 2/3 prescaler.

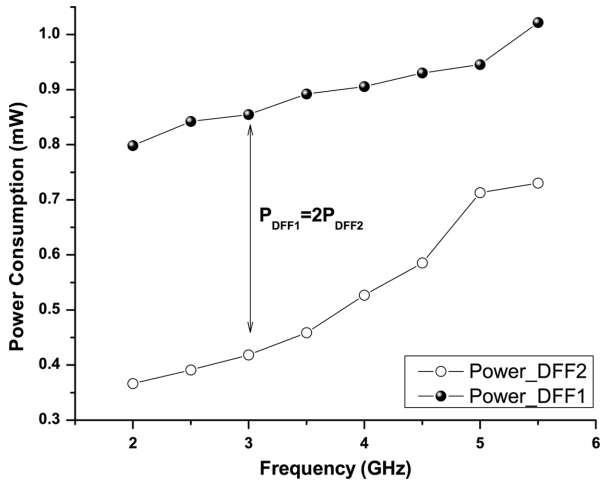


Fig. 13. Power consumption of Design-I Prescaler during divide-by-2 mode.

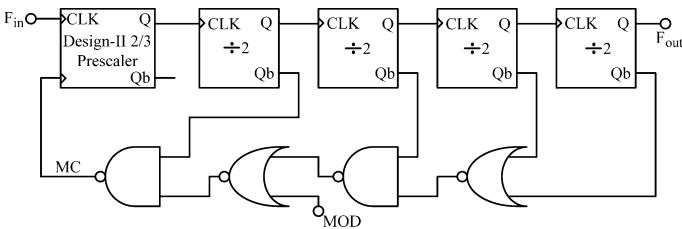


Fig. 14. Topology of 32/33 prescaler.

### B. A 32/33 Prescaler Using Design-II Prescaler

The amount of power saved by the Design-II prescaler in divide-by-2 mode is ideally 67% compared to that of Design-I and also reduces power consumption by 50% compared to conventional prescaler during divide-by-3 operation as discussed in Section V. The assumption here is, during the divide-by-2 operation no power is consumed by DFF1 neglecting the leakage current. To further verify the advantages of the proposed ultra low power prescaler of Design-II, a divide 32/33 dual modulus unit [9], [23] is implemented with the 2/3 prescaler of Design-II as shown in Fig. 14. In this 32/33 prescaler, the proposed 2/3

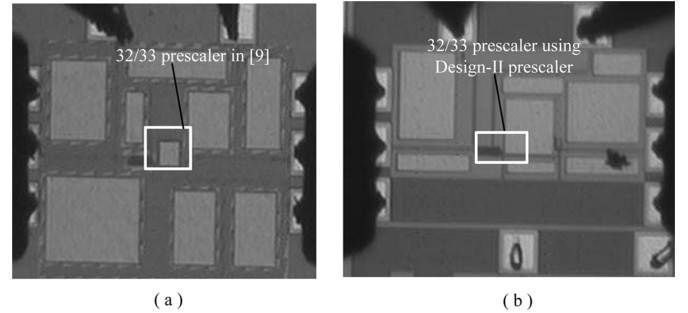


Fig. 15. Die photograph of (a) 32/33 prescaler in [9], (b) 32/33 prescaler using Design-II 2/3 prescaler.

prescaler unit is followed by four stages of the toggled TSPC divide-by-2 units. Fig. 15 shows the die photograph of the 32/33 prescaler in [9] and the 32/33 prescaler implemented with the prescaler of Design-II using Chartered 0.18um CMOS process.

When the control signal MOD is logically high, the 32/33 prescaler function as divide-by-32 unit and the control logic signal MC to the 2/3 prescaler goes logically high allowing it to operate in divide-by-2 mode for the whole 32 clock cycles. Since control logic signal MC is logically high, DFF1 in the Design-II 2/3 prescaler is completely turned-off for the entire 32 input clock cycles. When control logic signal MOD is logically low, the 32/33 prescaler unit function as divide-by-33 unit during which 2/3 prescaler operates in divide-by-3 mode for 3 input clock cycles and in divide-by-2 mode for 30 input clock cycles during which DFF1 in the Design-II 2/3 prescaler turns off completely thus reducing the power consumption of 32/33 prescaler using Design-II 2/3 prescaler.

### C. Power Saving Analysis During Divide-by-32 Mode

The total power consumed by the 32/33 prescaler using Design-I 2/3 prescaler during divide-by-32 is equal to the sum of switching and short circuit power of the DFF1, DFF2 over 32 clock cycles, power consumed by four asynchronous divide-by-2 circuits, and the power consumed by the logic gates

$$\begin{aligned}
 P_{32\text{-Design-I}} &= P_{\text{switching-DFF1}} + P_{\text{switching-DFF2}} \\
 &+ P_{\text{Div-by-16}} + P_{\text{short-DFF2}} \\
 &+ P_{\text{short-S3-DFF1}} + P_{\text{logic-gates}} \quad (17)
 \end{aligned}$$

The power consumed by the four asynchronous divide-by-2 circuits is given by (18)

$$P_{\text{Div-by-16}} = \frac{\sum_{i=1}^4 f_p C_{Li} V_{dd}^2}{2^{i-1}} + \sum_{i=1}^4 I_{SCi} V_{dd}. \quad (18)$$

Here,  $f_p$  is the frequency of the output signal from the 2/3 prescaler which can be half or one-third of the input clock signal and  $I_{SCi}$  is the total short-circuit current of the each asynchronous divide-by-2 circuit. Each of the asynchronous divider toggles at half the operating frequency of the preceding divide-by-2 circuit. Similarly, the power consumed by the 32/33 prescaler during the divide-by-32 operation using the Design-II prescaler is equal to the sum of switching and short circuit power of DFF2 over 32 clock cycles (DFF1 off) and the power consumed by the 4 asynchronous dividers and logic gates as given by (19). Here, the power consumed by the 4 asynchronous dividers is the same as in (18)

$$P_{32\_DesignII} = P_{\text{switching-DFF2}} + P_{\text{short-DFF2}} + P_{\text{Div-by-16}} + P_{\text{logic-gates}}. \quad (19)$$

Here, the power consumed by DFF2 is the same in Design-I and Design-II. The power saved by the 32/33 prescaler during the divide-by-32 mode using Design-II prescaler is obtained from (17) and (19), which is equal to the power consumed by DFF1 of the Design-I prescaler. Here, the power consumed by DFF1 always refers to the Design-I 2/3 prescaler since power consumed by DFF1 of Design-II prescaler is zero

$$P_{32\_saved} = P_{\text{short-S3-DFF1}} + P_{\text{switching-DFF1}}. \quad (20)$$

#### D. Power Saving Analysis During Divide-by-33 Operation

The total power consumed by the 32/33 prescaler using Design-I prescaler during the divide-by-33 operation is equal to the sum of switching power of the flip-flops DFF1, DFF2, short circuit power of DFF2, short circuit in the 3rd stage of DFF1 over 30 clock cycles, short circuit and switching power of DFF1, DFF2 over 3 clock cycles, power consumed by four asynchronous divide-by-2 circuits and the power consumed by the digital gates

$$P_{33\_Design-I} = \frac{30}{33}(P_{\text{switching-DFF1}} + P_{\text{short-S3-DFF1}} + P_{\text{short-DFF2}} + P_{\text{switching-DFF2}}) + P_{\text{Div-by-16}} + \frac{3}{33}(P_{\text{switching-DFF1}} + P_{\text{switching-DFF2}} + P_{\text{short-DFF2}} + P_{\text{short-DFF1}}) + P_{\text{logic-gates}}. \quad (21)$$

Similarly, the power consumed by the 32/33 prescaler using Design-II prescaler during the divide-by-33 operation is equal to the sum of the switching, short circuit power of DFF2 over 30 clock cycles, switching and short circuit power of DFF1, DFF2

over 3 clock cycles, power consumed by the 4 asynchronous dividers and digital logic gates given by (22)

$$P_{33\_Design-II} = \frac{30}{33}(P_{\text{switching-DFF2}} + P_{\text{short-DFF2}}) + P_{\text{Div-by-16}} + \frac{3}{33}(P_{\text{switching-DFF1}} + P_{\text{switching-DFF2}} + P_{\text{short-DFF2}} + P_{\text{short-DFF1}}) + P_{\text{logic-gates}}. \quad (22)$$

Since power consumed by DFF2, 4 asynchronous dividers and the logic gates are same in both cases, the total amount of power saved by the 32/33 prescaler during the divide-by-33 using Design-II prescaler is equal to 0.9 times the power consumed during divide-by-32. From the analysis discussed in Section V and VI, it is verified that Design-I prescaler reduces power by almost 50% during the divide-by-3 operation but consumes the same power as conventional TSPC 2/3 prescaler does during the divide-by-2 operation. The proposed ultra low power prescaler of Design-II consumes same power as the Design-I prescaler does during the divide-by-3 operation but saves 67% of power during the divide-by-2 operation which is also theoretically verified in the design of 32/33 prescaler. Here the design is not optimized and devices of the same size (3  $\mu\text{m}$  for PMOS and 2  $\mu\text{m}$  for NMOS) is employed for all the flip-flops in the asynchronous divide-by-2 stages. The simulation results shows that 32/33 prescaler consumes a power of 788  $\mu\text{W}$ , 807  $\mu\text{W}$  during divide-by-32, divide-by-33 modes respectively at 2.5 GHz. The asynchronous dividers and logic gates account for 60% of total power consumption of the 32/33 prescaler. By progressively reducing the device width ratio of PMOS/NMOS of stage 1 to stage 4 in the asynchronous divide-by-2 circuits as follows: 3  $\mu\text{m}/2 \mu\text{m}$ , 2.25  $\mu\text{m}/1.5 \mu\text{m}$ , 1.5  $\mu\text{m}/1 \mu\text{m}$ , 0.75  $\mu\text{m}/0.5 \mu\text{m}$ , according to the decreasing operating frequency of the flip-flops, the power consumption can be further reduced. The simulations shows that the asynchronous stage and logic gates account for about 56% of total power consumption and the total power consumption of the 32/33 prescaler is reduced to 713  $\mu\text{W}$ , 730  $\mu\text{W}$  during divide-by-32 and divide-by-33 operating modes respectively. Further attempts to reduce the transistor widths below 0.75  $\mu\text{m}$  for PMOS and 0.5  $\mu\text{m}$  NMOS affect the functioning of the prescaler. The experimental results for the 32/33 prescaler are not optimized but the functioning of the proposed 2/3 prescaler is verified in the design of 32/33 prescaler.

#### VII. MEASUREMENT AND SILICON VERIFICATIONS

A complete analysis and comparison of the performance of the proposed TSPC 2/3 prescalers, the conventional TSPC 2/3 and E-TSPC based prescalers in [17], [15] is carried out on the ground that the prescaler in [15] has the best performance in the literature that is constructed using single-phase clock. The simulations are performed using Cadence SPECTRE RF for a 0.18um CMOS process. For silicon verification, the proposed 2/3 prescalers and the 32/33 prescaler implemented with the proposed Design-II prescaler and 32/33 prescaler in [9] are fabricated using the chartered 1P6M 0.18 um CMOS process and the PMOS and NMOS transistor sizes are fixed to 3 um/0.18 um and 2 um/0.18 um, respectively. On-wafer measurements are

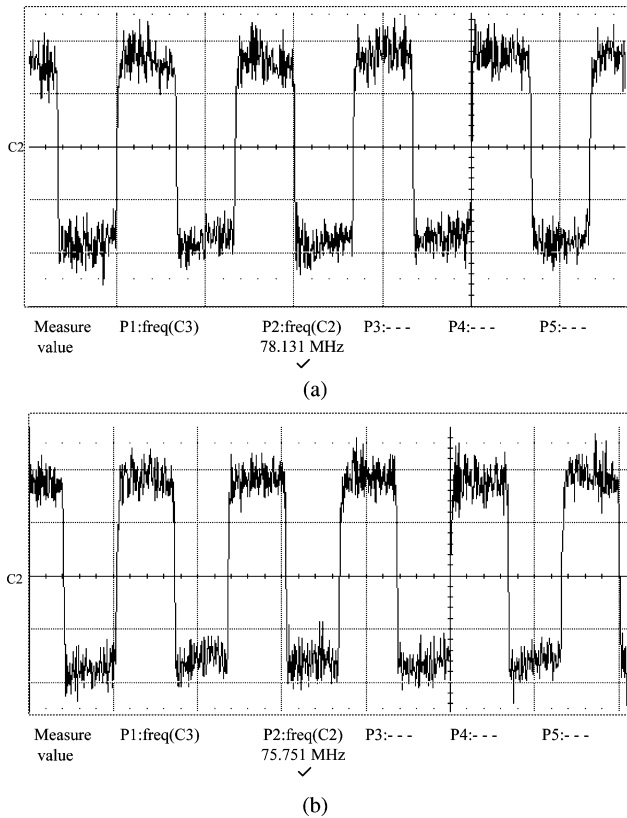


Fig. 16. Measured results of 32/33 prescaler (a) Divide-by-32, (b) divide-by-33.

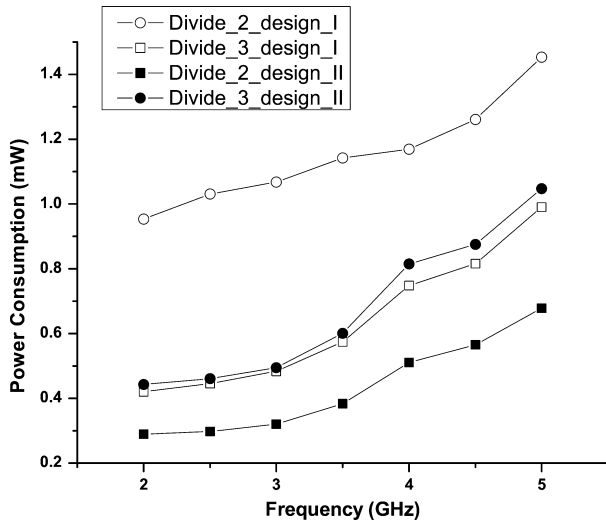


Fig. 17. Measured power consumption of the proposed prescaler units.

carried out using an 8 inch RF probe station. The input signal for the measurement is provided by the 83650B 10 MHz-50 GHz HP signal generator and the output signals are captured by the Lecroy Wavemaster 8600A 6G oscilloscope. The phase noise of the prescaler unit is measured using the Agilent E4407B 9 kHz-26.5 GHz spectrum analyzer.

Fig. 16 shows the measured output waveform of the 32/33 prescaler at 2.5 GHz input frequency in divide-by-32 and divide-by-33 mode respectively. Fig. 17 shows the measured power consumption against frequency of operation of the

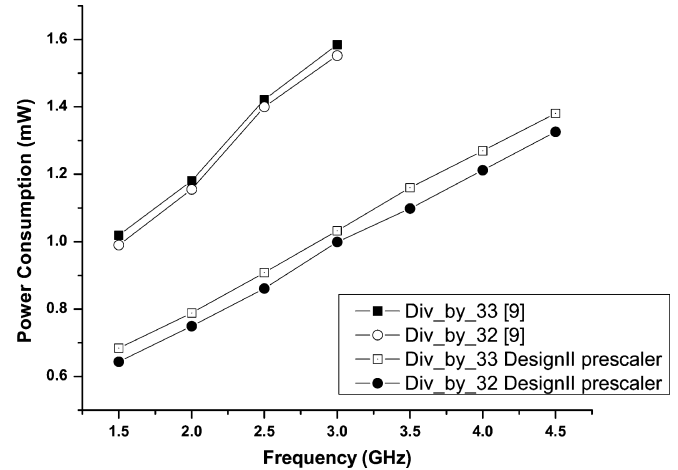


Fig. 18. Measured power consumption of the 32/33 prescaler units.

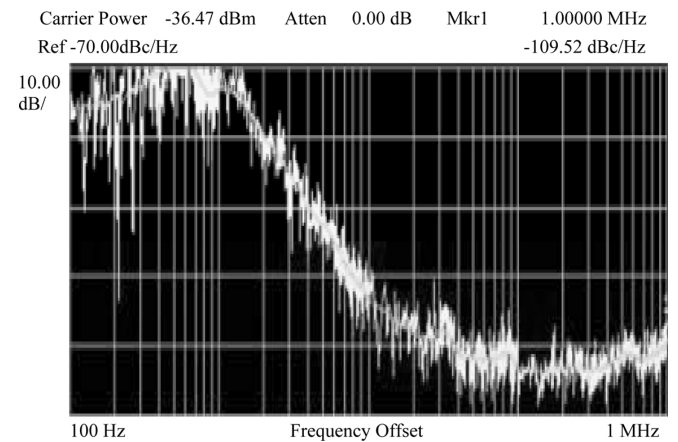


Fig. 19. Measured phase noise of the 32/33 prescaler using Design-II prescaler.

two proposed prescalers of Design-I and Design-II during the divide-by-2 and divide-by-3 mode respectively. The Design-I prescaler achieves lower power consumption compared to that of existing architectures of single-phase-clock family, but dissipates large short-circuit power in divide-by-2 operation. The results indicate that the proposed ultra low power 2/3 prescaler of Design-II consumes 67% less power compared to the Design-I prescaler during in divide-by-2 operation.

The measured maximum operating frequency of both proposed 2/3 prescalers is 4.9 GHz. The power consumption of the Design-II prescaler during the divide-by-2 and divide-by-3 modes is 0.6 mW, 0.922 mW respectively, while the power consumed by the Design-I prescaler is 1.33 mW, 0.86 mW respectively when the input frequency is 4.8 GHz. Fig. 18 shows the measured power consumptions of the 32/33 prescaler in [9] and 32/33 prescaler using Design-II prescaler. The maximum operating frequency of 32/33 is 3.2 GHz with a power consumption of 1.7 mW, while the maximum operating frequency of 32/33 prescaler implemented using the Design-II prescaler is 4.5 GHz with a power consumption of 1.4 mW. The results clearly indicate that the proposed low power prescaler of Design-II saves more than 50% of power compared to that of all the existing architectures reported in the literature thus far. The proposed prescalers of Design-I and Design-II also improve the

TABLE I  
PERFORMANCE OF DIFFERENT PRESCALERS AT 2.5 GHz

Design Parameters	Prescaler in [17]	Prescaler in [15]	Design-I Prescaler	Design-II Prescaler
Process ( $\mu\text{m}$ )	0.18	0.18	0.18	0.18
supply voltage (v)	1.5	1.5	1.8	1.8
Max.Frequency (GHz) (Sim/Measured)	5.5 / –	6.7 / –	5.5 / 4.9	5.5 / 4.9
Power(mW) (sim/measured) Divide-by-2 mode	1.78 / –	1.433 / –	0.923 / 1.03	0.252 / 0.306
Power(mW) (sim/measured) Divide-by-3 mode	1.643 / –	1.554 / –	0.369 / 0.445	0.387 / 0.461

maximum frequency of operation by 1.3 times compared to the conventional TSPC 2/3 prescaler. Fig. 19 shows the phase noise measured for the 32/33 prescaler using the Design-II prescaler which is  $-109.52$  dBc/Hz at 1 MHz offset. Table I compares the performance of the proposed prescalers and the prescalers reported in [17] and [15].

### VIII. CONCLUSION

In this paper, the effect of the DC level and amplitude of the sinusoidal clock signal on power consumption of TSPC and E-TSPC circuits are analyzed and an investigation on the performance of the E-TSPC and conventional TSPC 2/3 prescalers is carried out. Two low power TSPC 2/3 prescalers (Design-I and Design-II) are proposed whose maximum operating frequency can be extended up to 4.9 GHz. The low power is achieved by a switching off DFF1 during the divide-by-2 operation using the control logic signal MC. The proposed ultra low power 2/3 prescaler of Design-II saves more than 50% of power compared to that of the existing architectures and is also silicon verified in the design of a dual modulus TSPC 32/33 prescaler whose maximum operating frequency is 4.5 GHz with a power consumption of 1.4 mW. This low power prescaler unit can be used in the design of ultra low power fully programmable frequency synthesizers below 5 GHz applications.

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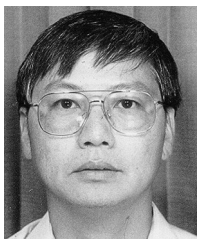
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