

A CMOS Analog Front-End IC for Portable EEG/ECG Monitoring Applications

K. A. Ng and P. K. Chan

Abstract—A new digital programmable CMOS analog front-end (AFE) IC for measuring electroencephalograph or electrocardiogram signals in a portable instrumentation design approach is presented. This includes a new high-performance rail-to-rail instrumentation amplifier (IA) dedicated to the low-power AFE IC. The measurement results have shown that the proposed biomedical AFE IC, with a die size of 4.81 mm², achieves a maximum stable ac gain of 10 000 V/V, input-referred noise of 0.86 μ V_{rms} (0.3 Hz–150 Hz), common-mode rejection ratio of at least 115 dB (0–1 kHz), input-referred dc offset of less than 60 μ V, input common mode range from –1.5 V to 1.3 V, and current drain of 485 μ A (excluding the power dissipation of external clock oscillator) at a \pm 1.5-V supply using a standard 0.5- μ m CMOS process technology.

Index Terms—Analog IC, biomedical circuits and systems, electrocardiogram (ECG), electroencephalograph (EEG), instrumentation amplifier (IA), rail-to-rail amplifier.

I. INTRODUCTION

THE realization of a portable device for electroencephalograph/electrocardiogram (EEG/ECG) recording is important for monitoring human or nonhuman subjects without restricting their mobility [1]–[7]. With such devices, successful monitoring of a patient's EEG/ECG had been performed on out-field physiological studies [1], [2]. In portable applications, there is a constant demand for reduced device size and weight without impacting recording quality. The ultimate goal is to make the subject of study unconscious of the existence of the recording device while the EEG/ECG monitoring process is taking place. A feasible solution [2] is to integrate most of the analog front-end (AFE) circuitry onto an IC and perform telemetry on the bio-potential signal to a remote computer. Recently, there has been a few reported AFE implementations using the IC approach [4]–[7] for single bio-potential measurement.

ECG and EEG signals are considered to be weak signals with signal amplitudes ranging from 100 μ V in the case of the EEG signal and up to 5 mV for the ECG signal [8]. With reference to [8], the ECG signal bandwidth ranges from 0.1 to 150 Hz for

normal operation. In addition, due to the skin–electrode interface, the dc half-cell voltage can be as high as \pm 300 mV and the maximum input-referred noise voltage must be less than 30 μ V_{pp} for a bandwidth from 0.1 to 150 Hz. For the EEG signal, the typical bandwidth can range from 0.3 to 100 Hz, and the input-referred noise should be less than few μ V_{pp}. Similar to the ECG signal, the dc half-cell voltage during EEG measurements can be as high as \pm 300 mV. Both ECG and EEG are vulnerable to common-mode interference from the 50/60-Hz mains supply. For a typical condition where the patient is isolated from the earth ground, the common-mode signal coupled to a human body can be calculated approximately to be as high as 1 mV_{pp} [9].

An AFE IC implemented in CMOS VLSI technology is attractive due to its low current consumption capability, dense integration, and wide availability. However, the dominant $1/f$ noise of MOS devices will greatly limit the minimum detectable signal in CMOS instrumentation amplifiers (IAs) at low frequency. In addition, due to finite transconductance of MOS transistors and threshold voltage variation from device to device, they often exhibit poor input offset and inferior common-mode rejection ratio (CMRR) performance when compared to the bipolar transistor counterparts. These nonideal effects give a significant challenge to the circuit design that demands an AFE IC to offer low offset, low noise, high gain, as well as high CMRR simultaneously. If these design issues are tackled, it avoids the dc saturation problem and the minute EEG/ECG signals being swamped by electronic circuit noise or radiated common-mode interference. In addition, the variation of dc common-mode voltage, arising from the EEG/ECG inputs, becomes another critical problem for the AFE circuitry to operate in a lower supply voltage, for example, at a 3-V supply. Although this may not be an issue in most of the reported AFE implementations [3]–[7] using a 6-V supply or above, the operating headroom becomes inadequate in a reduced supply voltage. Therefore, the primary goal of the AFE IC design is to accomplish a low-power task with a reduced supply voltage without jeopardizing the signal quality or dynamic range. This permits the usage of button-cell-sized batteries, which leads to substantial reduction of power consumption, size, weight, and electrical hazard.

A new CMOS AFE IC for portable biomedical applications is presented, with advantages of system operation in a reduced supply voltage (\pm 1.5 V) whilst offering a high CMRR, low input-referred noise, and rail-to-rail input common-mode range. Being powered with two 1.5-V button cell batteries and using some external components, it provides eight multiplexed inputs for EEG/ECG signal acquisition and conditioning functions on

Manuscript received October 1, 2004; revised March 27, 2005. This paper was recommended by Associate Editor G. Cauwenberghs.

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Digital Object Identifier 10.1109/TCSI.2005.854141

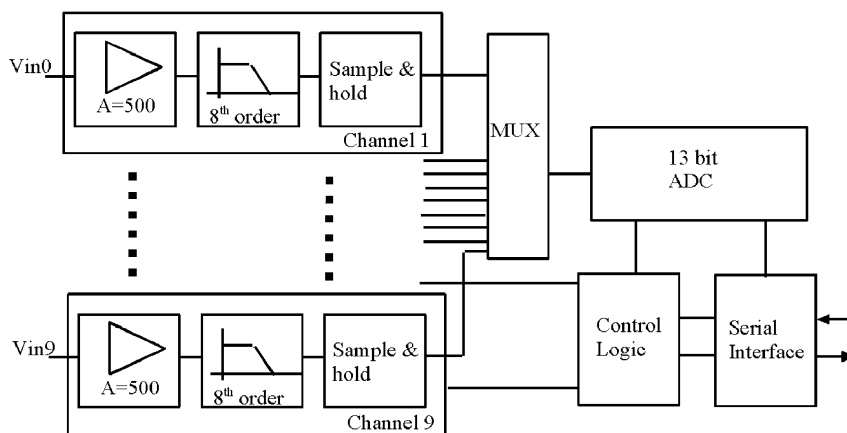


Fig. 1. AFE IC for nine-channel ECG acquisition [5].

a single IC. In addition, a built-in serial interface provides the capability to control the functions and to test the chip.

Section II reviews different state-of-the-art AFEs. Section III describes the architecture of the proposed AFE chip and the design of its individual block. The experimental results are presented in Section IV, which is then followed by the concluding remarks in Section V.

II. AFE IMPLEMENTATIONS FOR PORTABLE MONITORING APPLICATIONS

The early portable EEG/ECG monitoring devices are based on extensive usage of discrete components [1], [2] or thick-film technology [3] in the AFE design. Although these methodologies benefit short design time in conjunction with a wide choice of discrete analog components, they are bulky for system realization and consume high power dissipation.

With the availability of VLSI technology, various types of AFE ICs were reported in [4]–[7]. They provide an attractive means for portable monitoring tasks because there is a reduction in the number of external components required together with the possibility of obtaining lower power consumption. One of the primary objectives is to achieve full integration. Illustrated in Fig. 1, the incorporation of an analog-to-digital converter (ADC) allows data communication with digital devices, which can be regarded as the representative examples [4], [5] targeted for ultimate system-on-chip approach, with the incorporation of a digital signal processor for full function. However, for dedicated EEG recording process, the switching activity of the on-chip digital system has the possibility to cause significant interference to the sensitive analog circuit. The digital noise, arising from the injection to the common silicon substrate, couples to the critical front-end stage which processes only a few tens of μV_{pp} in the input signal. The partition design [6], [7] presents another design context because the ADC is isolated from the AFE IC, as shown in Fig. 2.

Nevertheless, it is common to observe that they operate at high supply voltages, consume reasonably high power consumption, and support single bio-signal-type measurement. In this paper, a new AFE IC for portable EEG and ECG acquisition applications is proposed to alleviate the problems and to provide an optimum tradeoff for meeting the stringent

biomedical performance requirements. The proposed AFE IC is based on a partition design approach.

III. DESIGN AND IMPLEMENTATION OF PROPOSED AFE

A. System Specifications

With typical signal amplitudes of less than $100 \mu\text{V}$ (for the EEG) or 5 mV (for the ECG) [8], the AFE has to provide a stable programmable ac gain from 200 to 10 000 V/V to amplify the very small voltage signal amplitudes for post-processing tasks. The targeted maximum output swing is $\pm 1 V_p$ in a $\pm 1.5\text{-V}$ supply. Having a common-mode interference level of as high as 1 mV_{pp} [9] on the output of the electrodes, the input CMRR of the AFE has to be greater than 80 dB to meet the standard specifications for ECG and EEG [8]. With the key objectives for high CMRR performance and mechanical simplicity, the AFE IC is designed to accept inputs coming from normal disposal electrodes. Although the alternative approach using active electrodes are effective in further reducing common-mode noise pick-up, they increase the cost due to extra packaging. Most often, they suffer from increased power consumption due to the use of conventional low-noise analog amplifiers with typical high supply and high current drain. In view of the potential reduction of battery-powered operating time, the active electrodes are preferred for laboratory or clinical measurements. Regarding the high sensitivity of the AFE, the internal amplifiers are needed to contribute low input offset voltages so as to prevent the dc saturation from the output of any internal amplifying device. The AFE inputs should also provide balanced and high input impedance ($> 1 \text{ G}\Omega$) to reduce the measurement loading effect of the electrodes, and to reject the potential common mode signal arising from the impedance mismatch [8].

B. AFE IC Architecture

The proposed AFE system chip in Fig. 3 consists of an 8:1 input analog multiplexer, a new rail-to-rail input IA, a programmable gain amplifier (PGA), a low-pass filter, and an output scaling amplifier. A digital interface is also integrated to support flexible configuration for ECG or EEG acquisition and to facilitate on-chip circuit characterization. Compared with previous architectures [4]–[7], the proposed architecture only utilized one IA with the multiplexed inputs. It is important to

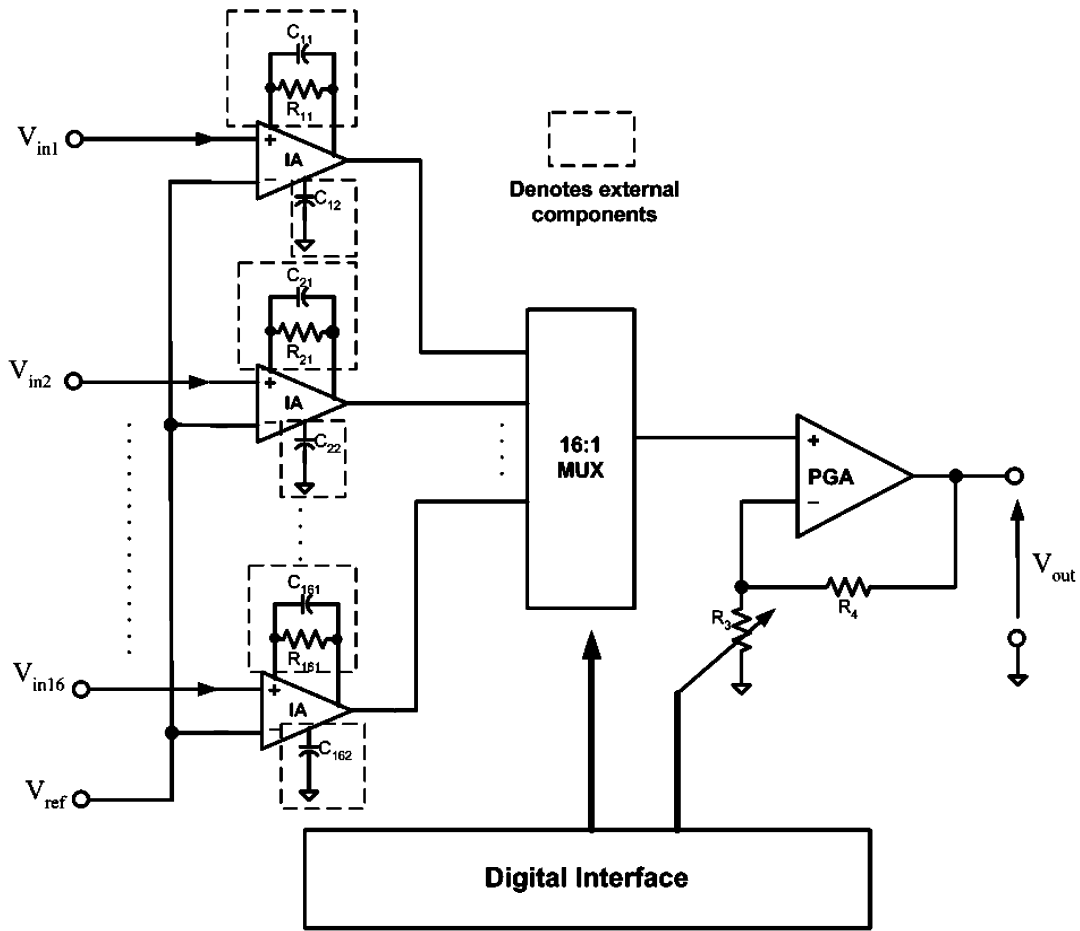


Fig. 2. AFE IC for 16-channel EEG acquisition [6], [7].

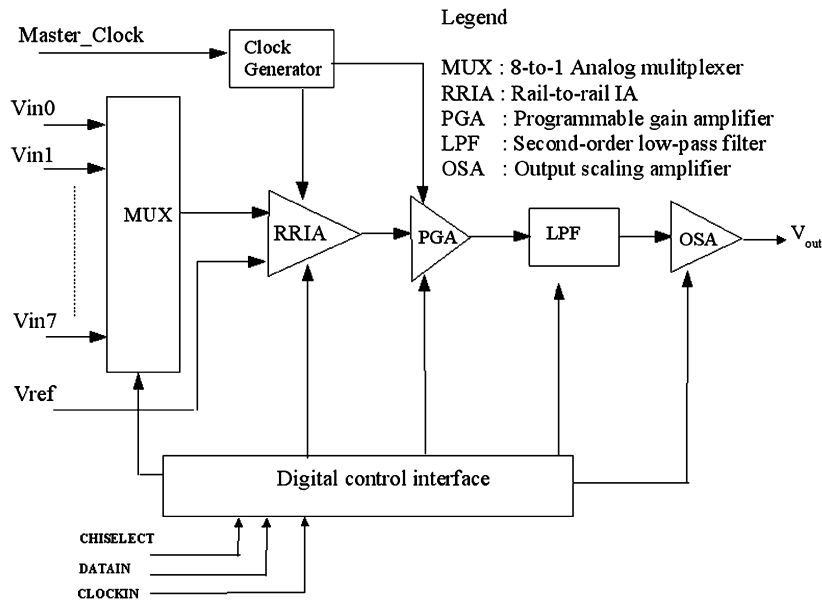


Fig. 3. System block diagram of the proposed AFE IC.

note that the AFE IC can only monitor one channel at a time; to make it a truly multichannel system, it would need eight copies of the IA at the expense of greater power dissipation and area. To attain full output swing of $\pm 1 V_p$ in a $\pm 1.5\text{-V}$ supply, the AFE gain can be programmed from 200 V/V (for ECG) to

10 000 V/V (for EEG). Derived from an external clock input, an on-chip clock generator provides the necessary clock signals for the chopping amplifiers in both the rail-to-rail IA and the PGA. The functions of each building block are described in the subsequent sections.

C. 8-to-1 Analog Multiplexer

The 8-to-1 analog multiplexer allows the selection of one out of eight inputs to be acquired and signal conditioned. Each switch path within the multiplexer is made up of a CMOS transmission gate. As the EEG and ECG input signals are low-frequency signals, the switch sizes can be made small to minimize the chip area. Different input information can be time multiplexed to a common IA and, hence, there will be uniform gain.

D. Rail-to-Rail Instrumentation Amplifier

The most critical component in the AFE is that of the input IA. It directly dictates the input-referred noise and input CMRR. Not only does it provide high and balanced input impedance, it supports a rail-to-rail input common-mode range in a reduced supply environment.

The classic three op-amp IA [10] and the current-mode IA [11]–[14] are popular approaches. Though simple to implement using discrete components, they require at least three op-amps and several resistors. Integrating the low-noise, rail-to-rail op-amps on an AFE chip would result in area and power penalties compared to a single IA. For meeting high CMRR performance, these amplifiers require the resistors and op-amp gain to be precisely matched, thus the trimming technique such as on-chip laser trimming will be needed to achieve more than 80 dB of CMRR [8], [13]. In [6] and [7], the current-feedback amplifier, which is designed using MOS transconductance input stages, serves as the input IA of the AFE. Since the MOS transconductance is significantly lower than that of the BJT transistor, the noise performance of such stages will be higher than their bipolar equivalents. In particular, the CMOS amplifier design [6], [7] is constrained by the $1/f$ noise, and so the large input transistor sizes are adopted to achieve lower $1/f$ noise and better matching characteristic in the differential input pair. Recently, [15] has reported an IA suitable for EEG signal acquisition. To provide stable signal amplification, it uses negative feedback around a simple operational transconductance amplifier with the closed-loop gain determined by the ratio of two capacitors. However, this amplifier is constrained by high $1/f$ noise (which needed large transistor sizes) and has an CMRR that just meets the minimum specification of 80 dB. Another promising approach is the differential difference amplifier (DDA)-based noninverting IA [16], [17], which has favorable properties such as simplicity and acceptable low power dissipation. Fig. 4 shows the basic DDA noninverting amplifier. Its input/output relation is defined as

$$V_{\text{out}} = V_{\text{in}} \times \left(\frac{R_2}{R_1} + 1 \right). \quad (1)$$

The major advantage of the DDA noninverting amplifier over the three op-amp IA or current-mode IA is that it requires only one active amplifier plus two resistors to set the instrumentation gain. In this DDA-based design, the CMRR performance is related only to the mismatch of the input ports. Mismatch between resistors R_1 and R_2 only affects the gain factor, but it does not degrade the CMRR of the amplifier. Incorporating the chopper stabilization technique [18]–[21] into the DDA, it allows a higher tolerance to input ports mismatch, thus attaining

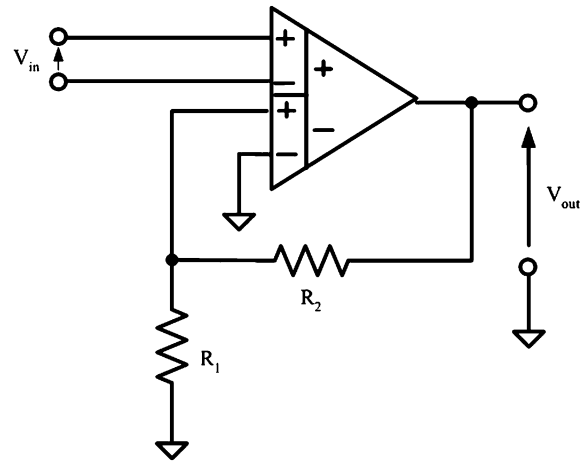


Fig. 4. Noninverting DDA for use an IA [16].

high CMRR and low input offset and $1/f$ noise simultaneously. More importantly, the component matching issues are relaxed. The DDA in this work is based on the chopper-stabilized DDA described in [20], and the circuit is depicted in Fig. 5. Each DDA input port consists of one transconductance stage (M_1 – M_2 or M_3 – M_4) and a MOS chopping switch network (S_1/S_2). S_1 and S_2 modulate the respective input differential signal to the chopper frequency. The differential currents flowing through transistors M_7 and M_8 are converted back to differential voltages via the active load (M_{11} – M_{12}). On the other hand, the transistors M_{11} and M_{12} in conjunction with the switch network S_3 constitute the demodulator. The common gate connection of the active load is commutatively connected to the drains of M_{11} and M_{12} via the periodic chopping action of S_3 . The output voltage at the drains of M_{11} and M_{12} are thus demodulated. Finally, the differential output of the first stage is coupled to the inputs of the two-stage amplifier (M_{13} – M_{19}), which serves multiple functions as a differential-to-single-ended converter, final gain stage, and buffer. Nested-Miller frequency compensation is implemented from the topological placement of C_1 and C_2 . The transistor dimensions for the pMOS differential-input-based chopper-stabilized DDA of Fig. 5 are depicted in Table I.

To operate at a ± 1.5 -V supply, the input common-mode voltage range is significantly limited because the variation of the dc voltage between each signal electrode with reference to the reference electrode can be as high as ± 300 mV, depending on the conditions of the skin–electrode interface. For some applications, the supply voltage will be just ± 1.2 V when NiMH/NiCad rechargeable batteries power them. This further restricts the input common-mode range. Hence, the IA has to exhibit rail-to-rail characteristic in this design. Although the well-known rail-to-rail amplifier topologies [22], [23] contribute good performance, they may not be suitable for this application on the basis of meeting the biomedical specifications of high CMRR, low noise, and low offset in a wide-input common-mode range simultaneously.

A new rail-to-rail input IA is proposed in Fig. 6. In this realization, two chopper-stabilized DDAs are arranged in parallel configuration. Depending on the input common-mode range, only one chopper-stabilized DDA is active at any time. The

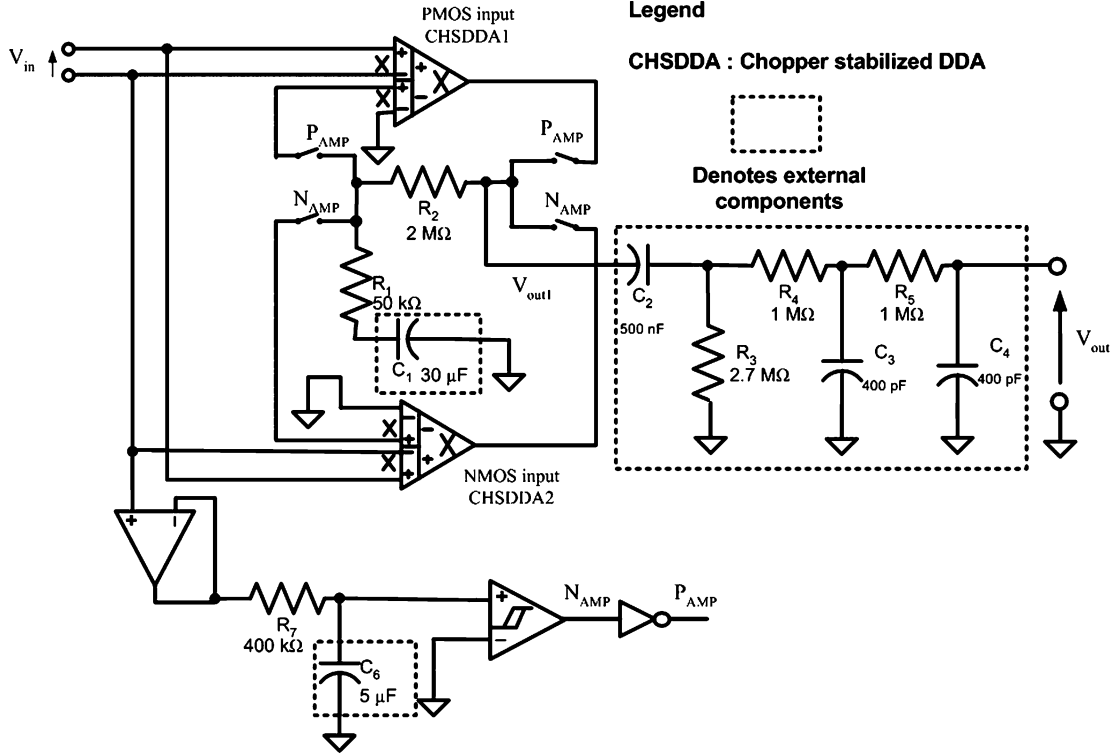


Fig. 6. Proposed rail-to-rail IA with dc blocking and bandpass filtering functions.

input differential voltage signals are modulated concurrently and translated to the current signals via the transconductance cells having identical transconductance gain of G_m . The modulated signals at the inputs of the transconductors can be written as

$$V_{m1}(t) = V_1(t) \cdot m(t) + V_{n1}(t) \quad (3)$$

$$V_{m2}(t) = V_2(t) \cdot m(t) + V_{n2}(t) \quad (4)$$

where $V_{n1}(t)$ and $V_{n2}(t)$ model the respective input-port component of the DDA which combines dc offset and $1/f$ noise, and $m(t)$ describes the chopping function at a frequency f_{chop} . Its time-domain definition and Fourier series are given as

$$m(t) = \begin{cases} 1, & 0 < t < \frac{T_{\text{chop}}}{2} \\ -1, & \frac{T_{\text{chop}}}{2} < t < T_{\text{chop}} \end{cases}, \quad T_{\text{chop}} = \frac{1}{f_{\text{chop}}} \quad (5a)$$

$$m(t) = 2 \sum_{k=1}^{\infty} \frac{\sin\left(\frac{k\pi}{2}\right)}{\left(\frac{k\pi}{2}\right)} \cos(2\pi f_{\text{chop}}kt). \quad (5b)$$

From (3) and (4), the input choppers translate the input signals of the chopper-stabilized DDA to the sidebands of the fundamental and every odd harmonics of f_{chop} . The undesired components $V_{n1}(t)$ and $V_{n2}(t)$ still reside at the baseband spectrum. The current signals are then summed and converted to a voltage signal $V_{mt}(t)$ with a transimpedance gain of K . After the second demodulator, $V_{mt}(t)$ is translated back to the baseband spectrum. Assuming that stage A of Fig. 7(a) exhibits infinite bandwidth and no signal delay, the signal at the output of the demodulator is

$$V_{dm}(t) = G_m \cdot K [(V_1(t) \cdot m(t) \cdot m(t) + V_{n1}(t)) \cdot m(t) - (V_2(t) \cdot m(t) \cdot m(t) + V_{n2}(t) \cdot m(t))]. \quad (6)$$

Legend

CHSDDA : Chopper stabilized DDA

Denotes external components

From (5a), it is worked out that $(m(t) * m(t) = 1)$ [21], and hence (6) can be simplified as

$$V_{dm}(t) = G_m \cdot K \cdot [V_1(t) - V_2(t)] + G_m \cdot K \cdot [(V_{n1}(t) - V_{n2}(t)) \cdot m(t)]. \quad (7)$$

As can be seen in (7), the output of the demodulator $V_{dm}(t)$ consists of a baseband component, which is the output of the ideal chopper-stabilized DDA transfer function plus the frequency-translated dc offset and $1/f$ noise residing at the odd harmonics of the chopping frequency. The last singled-ended output amplifier further amplifies $V_{dm}(t)$ with a gain of A . If a low-pass filter with maximum cut-off frequency at $f_{\text{chop}}/2$ is added in this stage, the frequency-translated dc offset and $1/f$ noise, defined as the second term in (7), will be subsequently removed. In practice, when stage A exhibits finite signal bandwidth and nonzero signal delay, the output of the demodulator would contain the spectral components around the even harmonics of the chopper frequency [18], [19]. The baseband chopper-stabilized DDA transfer function would also suffer the same gain degradation as described in [18] and [19]. However, the low-pass filter in the last amplifier stage would remove the spectral components due to the dc offset, $1/f$ noise, and even-order harmonics, leaving only the baseband signal at the final output $V_{\text{out}}(t)$. The final signal at the output of the low-pass filter is therefore obtained as

$$V_{\text{out}}(t) = G_m \cdot K \cdot [V_1(t) - V_2(t)] \quad (8)$$

$$V_{\text{out}}(t) = G_m \cdot K \cdot [(V_{pp} - V_{pn}) - (V_{np} - V_{nn})]. \quad (9)$$

From (8) and (9), the analysis has shown that the chopper-stabilized DDA implements the original DDA function with the additional advantage of removing the dc offset and $1/f$ noise.

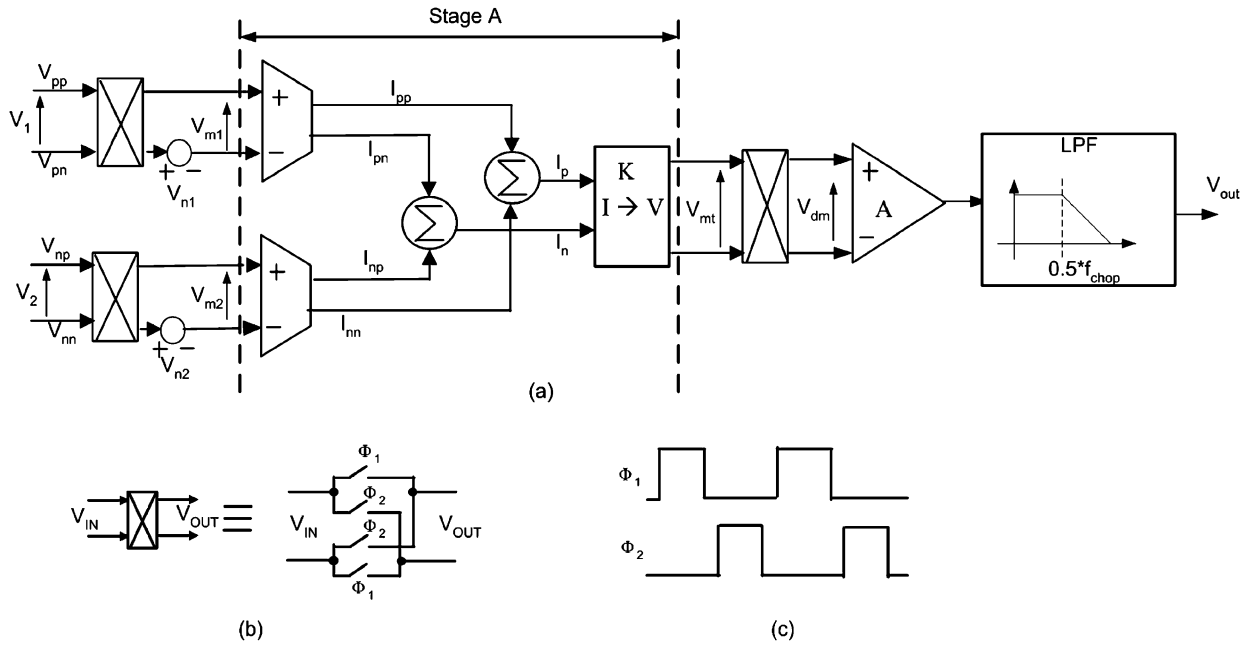


Fig. 7. Block diagram of the chopper-stabilized DDA and its associated clock signals for the chopping switches.

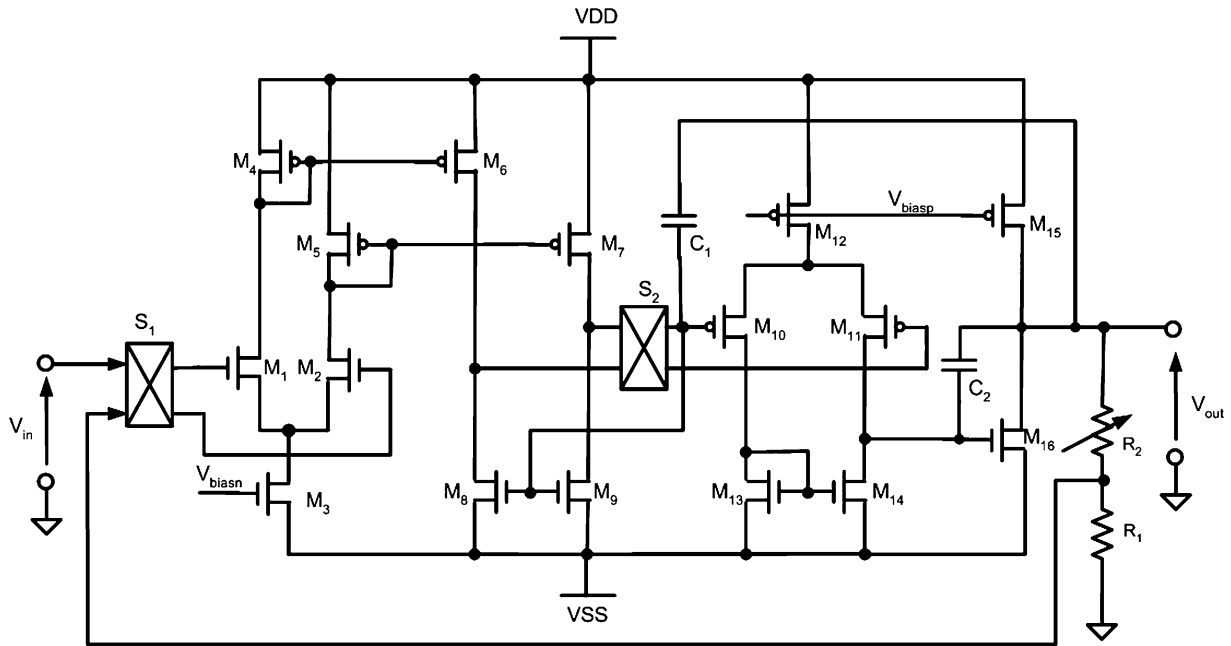


Fig. 8. PGA with chopper stabilization.

F. Programmable Gain Amplifier

The PGA shown in Fig. 8 provides further amplification with respect to the output of the rail-to-rail IA. To prevent the input impedance of the amplifier from loading the bandpass filter output of the rail-to-rail IA, a noninverting configuration is used. Note that the first chopper-stabilized stage inside the PGA is derived from the chopper-stabilized DDA by just removing one input differential port. By digitally connecting the resistors via CMOS switches, the amplifier provides programmable voltage gain of 5, 10, 25, and 50 V/V. For EEG acquisition, the AFE is programmed such that the PGA has a gain of 50 V/V and the output scaling amplifier has a gain of 5 V/V. Assuming

typical input-referred offset of CMOS amplifiers of tens of millivolts, the total gain of this amplifier and the output scaling amplifier will force the final output to saturate at either a supply level of ± 1.5 V. In order to alleviate the offset problem, the chopper-stabilization technique is realized in the design.

G. Low-Pass Filter

The second-order low-pass filter [10] in Fig. 9 is used to attenuate the frequency harmonics generated by the chopping action of the PGA. It also permits further attenuation of the frequency harmonics generated by the chopping action of the DDAs inside the rail-to-rail IA. In addition, the Q factor of this low-pass filter

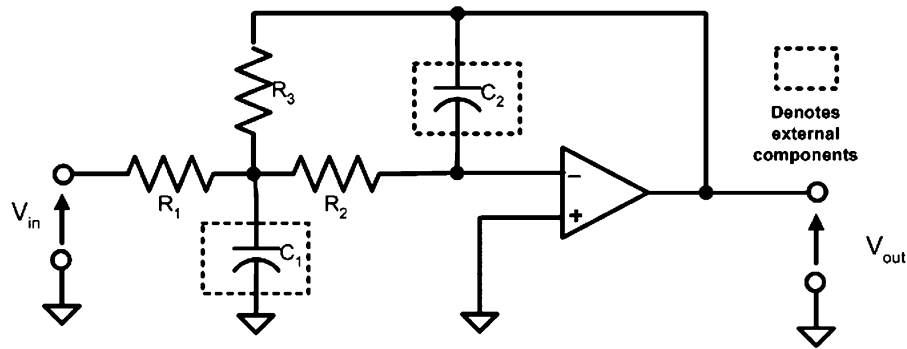


Fig. 9. Second-order low-pass filter.

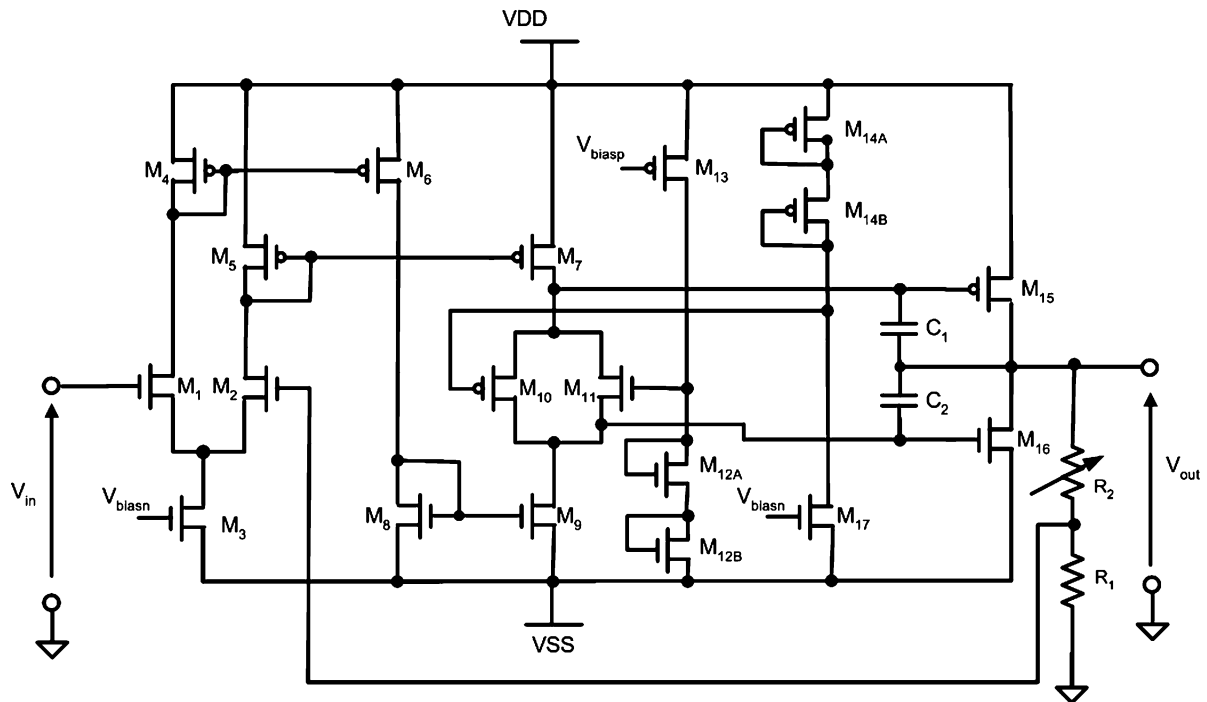


Fig. 10. Circuit schematic of the output scaling amplifier [26].

is set to 1 to compensate for the gradual low-pass roll-off characteristic arising from the low-pass section of the rail-to-rail IA after 100 Hz. This ensures that the frequency roll off at 150 Hz is sharp. To maximize design reuse, the op-amp used for this filter is the same circuit as that of the output scaling amplifier, which will be discussed in the subsequent section. From HSPICE simulation, the combined effect of the bandpass filter in the rail-to-rail IA and the low-pass filter attenuates the chopping clock related signal, with a residual value of $56 \mu\text{V}_{pp}$ at the AFE output. This simulation was done with the total AFE gain set at 10 000 V/V and adding intentional 5-mV offset at the inputs of the rail-to-rail IA.

H. Output Scaling Amplifier

The output scaling amplifier, as depicted in Fig. 10, provides the output drive needed for the inputs of an external ADC. To reduce power consumption, the output scaling amplifier has utilized a standard low-voltage, class-AB output stage [26], which

is capable of driving a 10-k Ω resistive load in parallel with a 30-pF capacitive load. In addition, it provides a 5-V/V or unity gain to achieve the total gain of 10 000 V/V for the EEG signal or 200 V/V gain for the ECG signal. By spreading the high gain between all of the amplifier stages when acquiring the EEG signal, the risk of instability via parasitic feedback is minimized.

The operation of the output scaling amplifier is briefly explained as follows. The input differential stage is formed by transistors M_1 and M_2 , which converts the input differential voltages to differential currents flowing through M_5 and M_4 . The differential currents are mirrored via M_6 – M_9 to flow through transistors M_{10} and M_{11} . Transistors M_{10} , M_{11} , M_{15} , and M_{16} form a loop to set up the class-AB biasing condition. The feedback path formed by R_1 and R_2 sets the closed-loop amplifier gain. When the output stage needs to sink a large load current, V_{in} goes low and causes the voltages at the source and drain of M_{11}/M_{10} to increase. M_{16} will be forced to turn on harder and M_{15} will be forced closer to turn off. Hence, M_{16} will sink the large load current. When the output stage needs to source a large load current, V_{in} goes high and causes the voltages at the source

and drain of M_{11}/M_{10} to decrease. M_{15} will be forced to turn on harder and M_{16} will be forced closer to turn off. Hence, M_{15} will source the large load current.

I. Digital Interface

The digital interface adopts three wire inputs: CHIPSELECT, DATAIN, and CLOCKIN inputs. The input CLOCKIN allows a clock to shift serial data from the input DATAIN to the on-chip control registers that directly control the configurations and test functions of the AFE chip. The CHIPSELECT input serves to turn on/off the AFE chip and keep the final output pin in a state of high output impedance when the AFE is tuned off. With this feature, the CHIPSELECT input provides an expansion capability for the AFE since multiple chip-select inputs can be used to enable multiple AFE chips individually.

J. Clock Generator

The clock generator generates the nonoverlapping phase clocks for the chopper stabilization operation in the rail-to-rail IA and PGA. An off-chip oscillator is needed to drive a clock signal on the MASTER_CLOCK input. The outputs of the nonoverlapping clock generator will not directly drive all of the chopper switches in the rail-to-rail IA and PGA. Otherwise, it would cause potential clock skews at the inputs of the choppers. Instead, separate clock buffers are established to drive the chopping switches of the pMOS differential-input-based DDA, nMOS differential-input-based DDA, and PGA. Each clock buffer would provide dedicated nonoverlapping clocks to the chopper switches within the individual amplifier.

IV. RESULTS AND DISCUSSIONS

The AFE system chip is fabricated using the AMIS 0.5- μm CMOS process. Occupying an area of 2.28 mm \times 2.11 mm, as shown in the chip microphotograph in Fig. 11, the floor plan of the chip employs mixed-signal layout techniques [27] to minimize the digital signals from disturbing the sensitive analog signals. For example, the noisy clock generator is placed far away from the input multiplexer and rail-to-rail IA. This helps to minimize the weak input signals from being disturbed by the switching noise of the clock generator. A large decoupling capacitor is also placed close to the rail-to-rail IA and 8-to-1 analog multiplexer so as to provide better on-chip supply decoupling for both circuits. The chip has three sets of VDD and VSS pads to minimize common impedance coupling between the sensitive analog circuits, output drivers, and the digital circuits.

Two 1.5-V battery cells are utilized to power the AFE IC and the minimum supply voltage is ± 1.0 V. At a low current consumption of 485 μA , a 500-mAhr battery can supply power for this AFE chip continuously for a minimum of 1000 h (approximately six weeks). For all measurements, the AFE IC is clocked at 10 kHz with an external oscillator circuit [28] consuming 40.5 μA at a ± 1.5 -V supply. The input common range is almost rail-to-rail with the positive input range limited to below 200 mV from the positive supply. For verifying the programmable gain capability of the AFE chip, Fig. 12 shows the possible gain of the AFE chip, with a bandwidth of 0.3–150 Hz. The AFE gain can be programmed from 0 dB to a maximum of

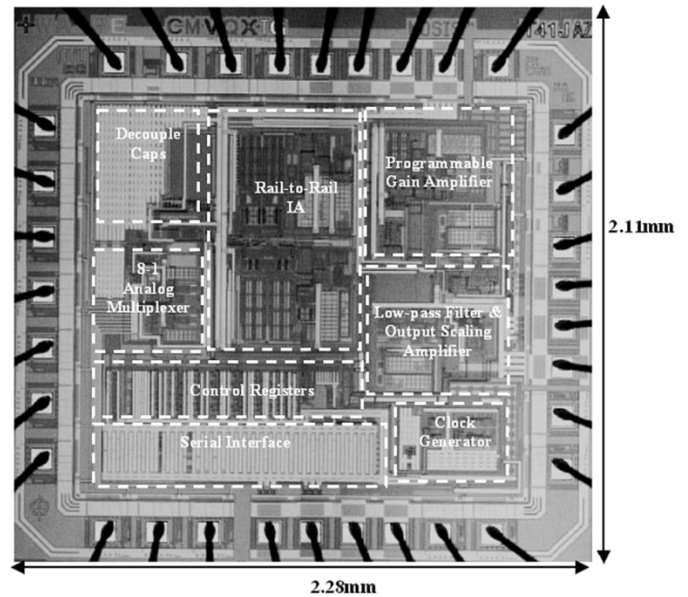


Fig. 11. Microphotograph of the complete AFE chip.

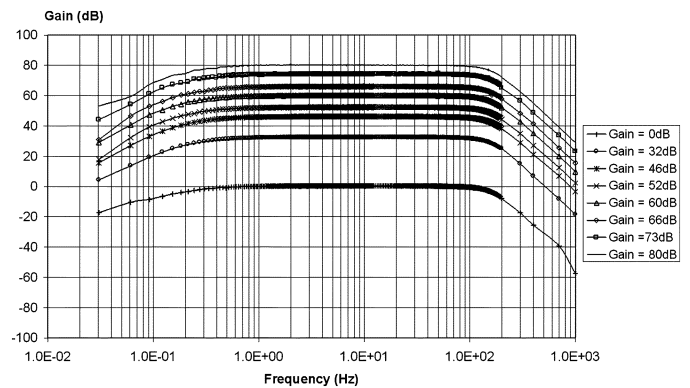


Fig. 12. Frequency response of the AFE for a bandwidth of 0.3–150 Hz.

80 dB. With the wide range of programmable gain, the AFE is capable of amplifying ECG as well as EEG signals. As shown in Table II, the measured gain results are close to the theoretical prediction.

For evaluating the noise performance of the AFE, Table III summarizes the input-referred noise of the AFE for 0.3–150-Hz bandwidth. The worst case input-referred noise is 0.86 μV_{rms} when the pMOS differential-input-based chopper-stabilized DDA is the active IA. Nevertheless, at this noise level, it is still suitable for EEG/ECG acquisition. For accessing the CMRR aspect, the respective frequency-dependent CMRR performance for either the active pMOS differential-input-based chopper-stabilized DDA or the active nMOS differential-input-based chopper-stabilized DDA is depicted in Fig. 13. Note that the pMOS differential-input-based chopper-stabilized DDA is the active IA when the input common-mode voltage ranges from VSS to 0 V whereas the nMOS differential-input-based chopper-stabilized DDA is the active IA when the input common-mode voltage ranges from 0 V to VDD. Regardless of the input common-mode range, the CMRR is at least 115 dB from 0 to 150 Hz, and this is more than sufficient for ECG or EEG measurement requirements. In addition, despite the

TABLE II
COMPARISON OF THE MEASURED GAIN WITH THE SPECIFIED
GAIN OF THE AFE IC

Specified gain (dB)	Measured Gain (dB)	Error (dB)	Condition
0	0.35	+0.35	Measured at 10 Hz
32	32.4	+0.40	
46	46.2	+0.20	
52	52.4	+0.40	
60	60.2	+0.20	
66	66.1	+0.10	
74	74.1	+0.10	
80	80.2	+0.20	

TABLE III
INPUT-REFERRED NOISE VOLTAGE OF THE AFE FOR 0.3–150-Hz BANDWIDTH

AFE Gain (V/V)	Condition	PMOS chopper stabilized DDA active	NMOS chopper stabilized DDA active
200	Chop @ 10 kHz	0.86 μV_{rms}	0.68 μV_{rms}
10,000	Chop @ 10 kHz	0.86 μV_{rms}	0.59 μV_{rms}

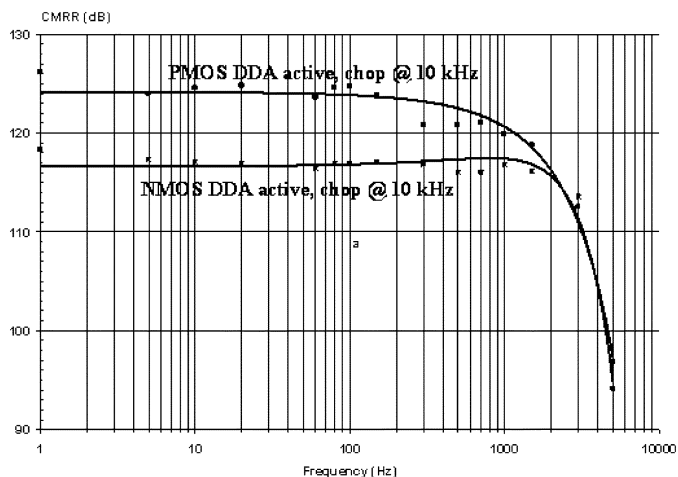


Fig. 13. CMRR performance of the AFE chip.

decrease of CMRR to 90 dB at 5 kHz, this is not detrimental to the AFE performance, as the maximum EEG/ECG signal bandwidth is much lower than 5 kHz. For evaluating the offset aspect, the input-referred offset results for ten samples are illustrated in Fig. 14. It is noted that the maximum offset value is less than 60 μV . Further investigation has revealed that the input-referred offsets are contributed mainly by the low-pass filter and the output scaling amplifier. Nevertheless, for all of the samples, the input-referred offsets did not cause any output saturation. For accessing the linearity of the AFE, the spectral of the AFE output signal in response to a 5.8-mV_p sinewave test signal is depicted in Fig. 15. It shows that the distortion components are 71 dB below a test signal with fundamental frequency of 30 Hz. For this measurement, the AFE gain was set to 200 V/V such that the output swing was approximated as 1.16 V_p. This demonstrates that there is no cross-over distortion since the input stimulus is made close to the biopotential signal, which will not false trigger the comparator in the hysteresis window of ± 80 mV in the design. The typical chopping clock signal was measured to be 47 μV_{pp} at the AFE output under

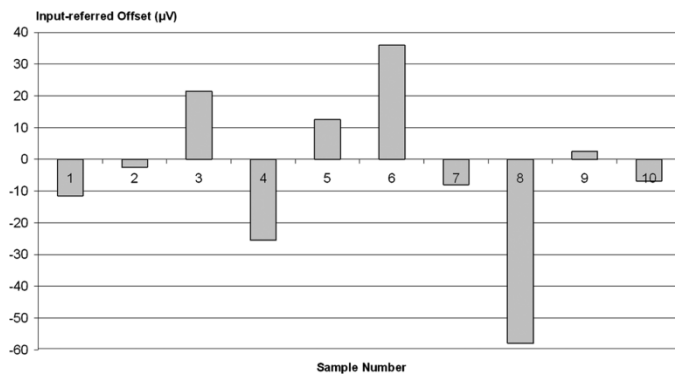


Fig. 14. Input-referred offset of the AFE chip samples (chopping at 10 kHz).

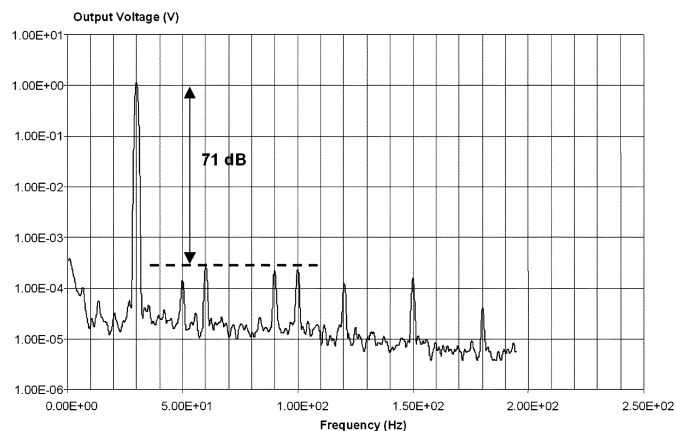


Fig. 15. Signal spectrum of AFE response to a 30-Hz input sinewave with 5.8-mV_p amplitude.

the maximum gain of 10 000 V/V. This shows that the filter of the system is sufficient to attenuate the chopping clock signal to insignificant amplitudes.

To demonstrate this AFE chip capable of acquiring an ECG signal, the AFE chip was set up to acquire the ECG of a human subject at his chest position V5 as defined in [8]. During the recording session, the AFE gain was set to 400 V/V. The output of the AFE is depicted in Fig. 16, and it clearly shows the QRST complex of the acquired ECG signal. The input-referred ECG signal is 6.25 mV_{pp}.

To test the EEG signal acquisition capability of the AFE IC, the AFE IC was set up to acquire an EEG signal from a human subject. The reference electrode was placed on the subject's right mastoid and the ground electrode was placed on the subject's forehead. The acquired EEG signal at site P3 on the subject's scalp is shown in Fig. 17. For this measurement session, the subject was sitting on a chair with both eyes closed. Since the AFE gain was set to 10 000 V/V, the average input-referred EEG signal strength was calculated as 40 μV_{pp} . Fig. 18 shows the signal spectral of Fig. 17. As can be seen in Fig. 18, there is a strong signal activity at a frequency of 11.7 Hz. This coincides with the alpha-wave activity characterized by signal frequencies from 8 to 13 Hz [8]. Another experiment was performed where the same subject under study was asked to close both eyes, followed by opening both eyes for 3 s and then closing both eyes thereafter [8]. The result of this experiment is depicted in Fig. 19. It indicates that the alpha-wave activity ceases

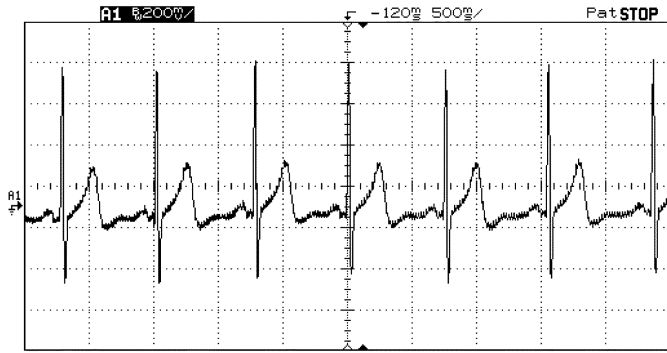


Fig. 16. Captured ECG signal at V5 position [8] with the AFE gain of 400 V/V.

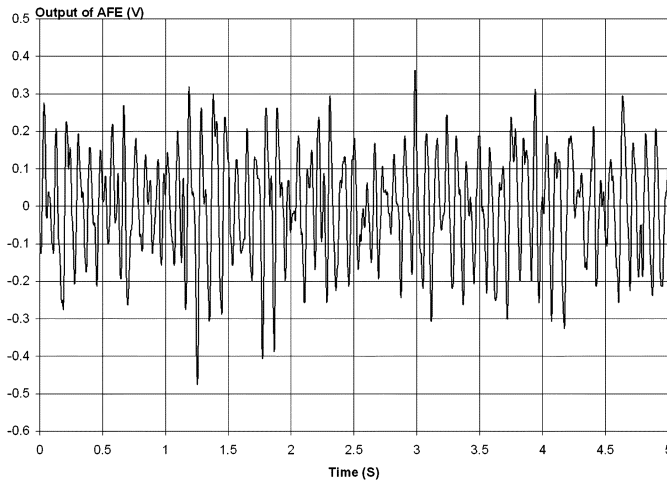


Fig. 17. Captured EEG signal at P3 position [8] with an AFE gain of 10000 V/V.

when both eyes are open but the activity resumes when both eyes are closed.

To demonstrate the measurement of both ECG and EEG in the multiplexed mode, an experiment was set up such that the reference electrode was placed on the subject’s right mastoid and the ground electrode was placed on the subject’s forehead. The V_{in0} input of the AFE was connected to the electrode placed on FP1 position of the subject’s head and the V_{in1} of the AFE was connected to the electrode placed on the left shoulder position of the subject. The acquired signals at both sites are shown time-multiplexed in Fig. 20. In this experiment, the AFE settling time was governed by the time constant of filter circuits and measured to be 5.28 s.

Comparing the new rail-to-rail IA with the published EEG amplifier in [15], the MOS transistors in the EEG amplifier operated in the subthreshold region, which allows it to have a much lower power consumption ($0.9 \mu\text{W}$) and better power efficiency than the proposed rail-to-rail IA. On the contrary, the proposed rail-to-rail IA was designed to operate in the strong inversion region in exchange for a more predictable circuit characteristic, which leads to better manufacturing yield. In addition, the rail-to-rail IA benefits for obtaining high CMRR are in spite of the mismatch effects arising from fabrication in manufacturing process. The EEG amplifier in [15] also has a smaller active area (0.22mm^2) than the proposed rail-to-rail IA (0.56mm^2). This is

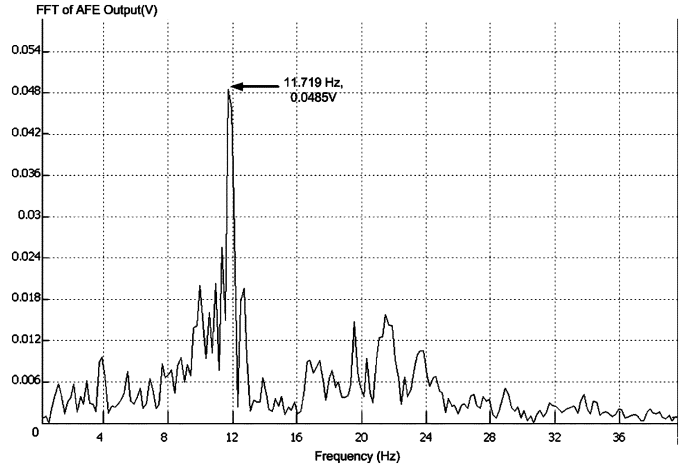


Fig. 18. Signal spectrum of the EEG signal depicted in Fig. 17.

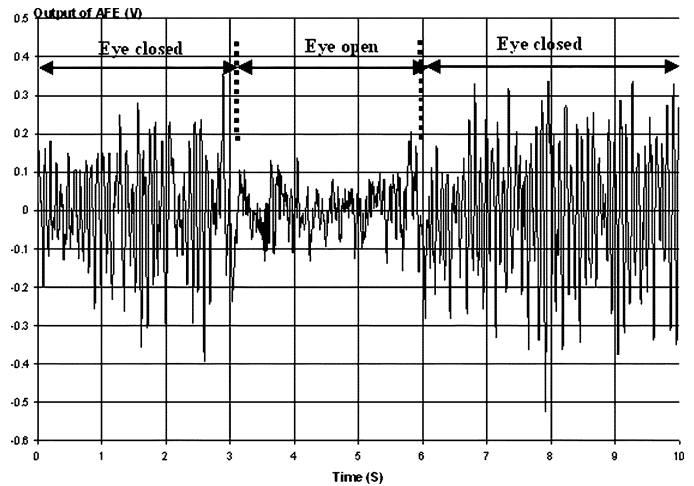


Fig. 19. EEG signal acquired at site P3 with eyes open and closed.

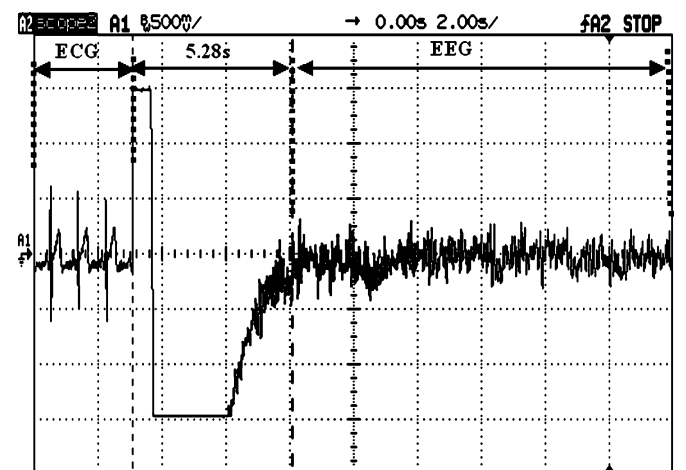


Fig. 20. Acquisition of both ECG and EEG signals. The ECG signal is captured at shoulder position [8] with an AFE gain of 2000 V/V. EEG signal is captured at the FP1 position [8] with an AFE gain of 10000 V/V.

due to the use of a more complex chopper-stabilized DDA circuit topology within the rail-to-rail IA. However, it is possible to further reduce the active area of the rail-to-rail IA by adopting

TABLE IV
PERFORMANCE COMPARISON WITH OTHER PUBLISHED AFE ICs

Parameter	Ref [5]	Ref [6]-[7]	This Work
Technology	2 μm CMOS	2.4 μm CMOS	0.5 μm CMOS
Supply (V)	10	9	+/- 1.5
No. of Channels	9	16	1 ^{Note 1}
Application	ECG	EEG	ECG & EEG
Area (mm ²)	65 ^{Note 2}	24	4.81
Supply current in each supply (μA)	27000 ^{Note 3}	520	485 ^{Note 4}
Normalized supply current per channel (μA)	3000	32.5	485
EEG Bandwidth (Hz)	-	0.3 – 150	0.3 – 150
ECG Bandwidth (Hz)	0.1 – 250	-	0.3 – 150
Mid-band gain (dB)	-	Up to 74	0 – 80
Input common mode range (V)	-	-3.8 to 1.5	-1.5 to 1.3
Inter-channel gain mismatch (%)	-	0.9	0.01
PSRR + @ 10Hz (dB)	-4	40	65
PSRR - @ 10Hz (dB)	-	-	52
Input-referred noise (μV_{rms})	0.61	1.39	0.86
Input-referred dc offset (μV)	-	< 1000	< 60
CMRR @ 50 Hz (dB)	-	99	117
Channel cross talk @ 100Hz (dB)	85	-	123

Note 1: Single channel with 8 multiplexed inputs.

Note 2: This includes the area of the integrated ADC. From the micrograph in [5], the ADC occupied 43 % of the total chip area.

Note 3: This includes the power consumption of the integrated ADC.

Note 4: The measurement does not include the power consumption of external oscillator circuit [28], which consumes 40.5 μA .

a simpler chopper-stabilized DDA topology in the next prototype AFE IC. The EEG amplifier in [15] also does not need any external passive components to define the frequency response of the amplifier. However, it is possible to replace the external passive filters of the rail-to-rail IA by the log-domain filters in the next prototype AFE IC.

Table IV summarizes the comparison of the measured parameters of this AFE chip with those of reported AFE IC works. It can be seen that the proposed AFE IC offers technical merits of reduced supply voltage, reasonable low power, very high gain and sensitivity, low gain mismatch for different time-multiplex inputs, very low crosstalk, and input rail-to-rail operation, yet offers comparable measured results of the critical performance parameters such as CMRR, noise, and offset. Although the present AFE implementation is not fully integrated, this is justifiable in terms of performance aspect and multiple bio-potential measuring or processing functions in the context of the IC realization of the previous state-of-the-art devices.

V. CONCLUSION

The design of a CMOS AFE IC for portable biomedical signal acquisition applications is presented. The AFE IC is capable of acquiring either ECG or EEG signal without any change of external hardware. The system IC offers benefits in terms of acceptable silicon area and power consumption. Since the proposed system architecture has utilized only one instrumentation amplifier for the eight multiplexed inputs, the system gain is highly matched for each multiplex input signal. Besides, the new circuit topology of the rail-to-rail instrumentation amplifier overcomes the operation headroom constraint in a reduced supply. Through utilizing the parallel chopper

stabilized DDA configuration in conjunction with the input common-mode sensing circuitry in the proposed rail-to-rail instrumentation amplifier design, we have shown that the $1/f$ noise and offset are significantly reduced while offering very high CMRR, very high gain, and very high sensitivity without compromising on the power tradeoff and the input common-mode range. The measurement results have validated that the AFE IC meets the design objectives and is suitable for portable biomedical signal acquisition applications.

ACKNOWLEDGMENT

The authors want to thank P. Y. Wang and X. P. Fan for allowing their EEG signals to be recorded. They also want to express their gratitude to Prof. L. M. Goh for advice during the EEG recording sessions.

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