Z-source Inverters with Enhanced Voltage Boost for Renewable Energy Systems

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Summary

Worldwide economic growth has initiated a strong demand for energy, which unfortunately cannot be met indefinitely by fossil fuels. That motivates the development of renewable energy systems like wind, solar and tidal farms, which by nature are non-polluting and abundant. Outputs from these renewable sources are also mostly electrical, which by far is the most efficient form of energy for transmission and distribution over long distance. Renewable energy is therefore a promising green alternative even though it is unlikely to replace fossil fuels any sooner.

Although renewable energy is mostly electrical, connecting renewable sources to the utility mains or localized smart grids is not a trivial task, frequently complicated by climatic variations. Energy conditioning is therefore almost always needed, and is usually achieved by placing a power electronic conditioner between each renewable source and the grid. A typical power conditioner would consist of a power flow controller and a power converter interfaced by sensors and semiconductor driving circuits. The power controller would add features like maximum power point tracking, grid synchronization and fast dynamics to the system, which are presently well established. Upon receiving the command from the controller, the power converter realizes the physical conversion of magnitude, frequency and phase of the electrical quantities before smooth grid connection can be effected.

A frequent feature demanded by the conversion is voltage boosting, which presently is met by introducing an elementary dc-dc boost converter to the system. This certainly is a straightforward and reliable extension, which presently might not have further scope for improvement. A more recent recommendation is to use the Z-source dc-ac inverters either alone or accompanied by a front-end rectifier if ac inputs are encountered like in wind and tidal generation. Adding a rectifier will strictly not modify the basic Z-source

energy inversion concept, and is therefore not specifically addressed in this thesis.

Unlike traditional inverters whose output voltages can only be stepped down, Z-source inverters form a new class of impedance-source inverters whose outputs can both be stepped up and down. This flexibility is accompanied by further improvement in robustness since accidental turning on of two switches from the same phase will no longer cause damages. Dead-time protecting against such shoot-through condition is therefore not needed. Instead, shoot-through condition is intentionally used by the Z-source inverters for safe voltage boosting without compromising their usual voltage buck ability. Z-source inverters are therefore promising alternatives for renewable generation, and have earlier been tested for solar and wind generation.

Despite these improvements, Z-source inverters are presently known to be burdened by low modulation ratios at high gains, whose consequential effects are high component stresses and poor spectral performances. To avoid these shortcomings, the intention here is to formulate a few new Z-source inverters whose overall modulation ratios can be raised without limiting gains. Their component stresses will be reduced greatly, while voltage boost, reliability and waveform quality will be enhanced strongly. These advantages have already been proven in theory, simulation and experiment, and would definitely raise the attractiveness of Z-source inverters as the power stages of renewable systems.

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List of Abbreviations

CCM	Continuos Conduction Mode
CSE	Capacitive-Shunt Embedded
CSI	Current Source Inverter
DCLC	DC-Link-Cascaded
DCM	Discontinuous Conduction Mode
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
EPLD	Erasable Programmable Logic Device
IGBT	Insulated Gate Bipolar Transistor
ISE	Inductive-Series Embedded
MC	Multi-Cell
MPP	Molypermalloy Powder
MPPT	Maximum Power Point Tracking
NPC	Neutral-Point-Clamped
PD	Phase Disposition
PV	Photovoltaic
PWM	Pulse-Width Modulation
SC	Switched-Capacitor
SL	Switched-Inductor
SPWM	Sinusoidal Pulse-Width Modulation
SVPWM	Space Vector Pulse-Width Modulation
TL	Tapped-Inductor
VSI	Voltage Source Inverter

List of Symbols

B	Boost factor of Z-source inverter
C	Capacitor
$\cos\phi$	Power factor
D	Diode
i_C	Capacitor current
i_{dc}	DC input current
i_L	Inductor current
i_{in}	DC-link current
I_o	Peak ac output current
L	Inductor
M	Modulation index
N	Neutral point
SW	DC side switch
SX (X = A, B or C)	Switch in the inverter circuitry
SX' (X = A, B or C)	Counterpart of SW
S_x (x = a, b or c)	Switching function of inverter
T	Switching period
T_0	Shoot-through interval
T_1	Non-shoot-through interval
V_C	Capacitor voltage
V_{dc}	DC input voltage
$\hat{v}_i$	Peak dc-link voltage in the Z-source inverters
v_L	Inductor voltage
V_S	Line rms voltage
V_x (x = a, b or c)	Modulation reference
$\hat{v}_x$	Peak ac output voltage in the Z-source inverters

Chapter 1 Introduction

1.1. Background and Motivation

Growing concerns with air pollution and global warming has pushed the international community to adopt and keep raising the percentage of energy produced through renewable means [1]-[5]. Renewable energy is basically energy produced from natural resources like sunlight, wind, rain, tides and geothermal heat that are "endlessly" replenished by nature. It is therefore an important source of clean energy worldwide that can greatly supplement traditional power generation. It has since drawn enormous interests from the industries, environmentalists, governments and end users with many of them encouraged by incentives offered by the local and federal governments.

Among the renewable sources, wind energy systems [5][8] are considered the most efficient and widely installed either onshore or offshore. They however might not be as conveniently installed as solar systems, which now are popularly embedded within the building architectural design. Their lack of moving mechanical parts, and hence lower maintenance costs, are also advantages that have motivated continuous research in

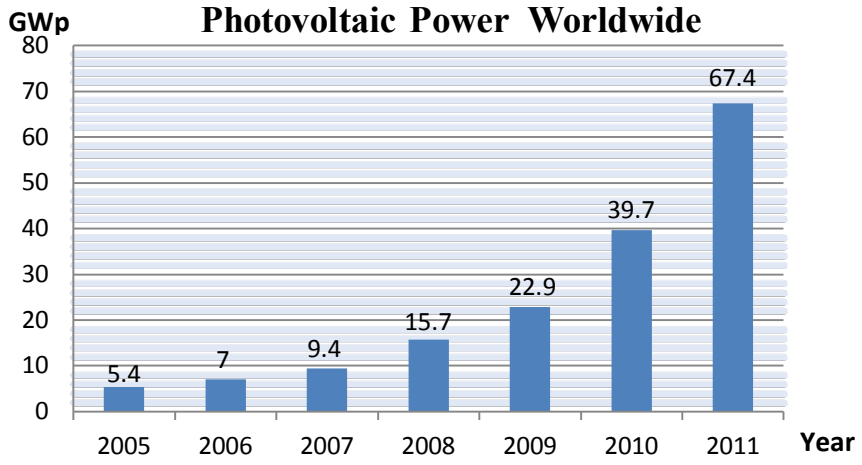


Fig. 1.1 Photovoltaic power worldwide.

raising photovoltaic (PV) efficiency and their subsequent usages in urban cities and remote solar farms [8]-[13].

To provide some background statistics showing their respective popularities, a market report documented by the European photovoltaic industry association is referred to. In that report, it is stated that from the end of 2005 to the end of 2011, the photovoltaic market has expanded by more than ten times, reaching 67.4 GW, as shown in Fig. 1.1[2]. The photovoltaic energy generated can either be off-grid or grid-tied, which from another statistic source [3], it is understood that off-grid applications has dominated the market before 1999. The equilibrium arrives at 2000, after which grid-tied applications grow at a faster rate as demonstrated in Fig. 1.2. At 2010, grid-tied applications dominate the market with a share of 97%. The wind power market, on the other hand, increases by 250% to 121 GW. Together, the total power generated from renewable sources increases by 75% to 280 GW at the end of 2008, as compared to the end of 2004 [5].

Regardless of the types of renewable energy considered though, some forms of energy conversion systems are almost always necessary to extract the maximum power and

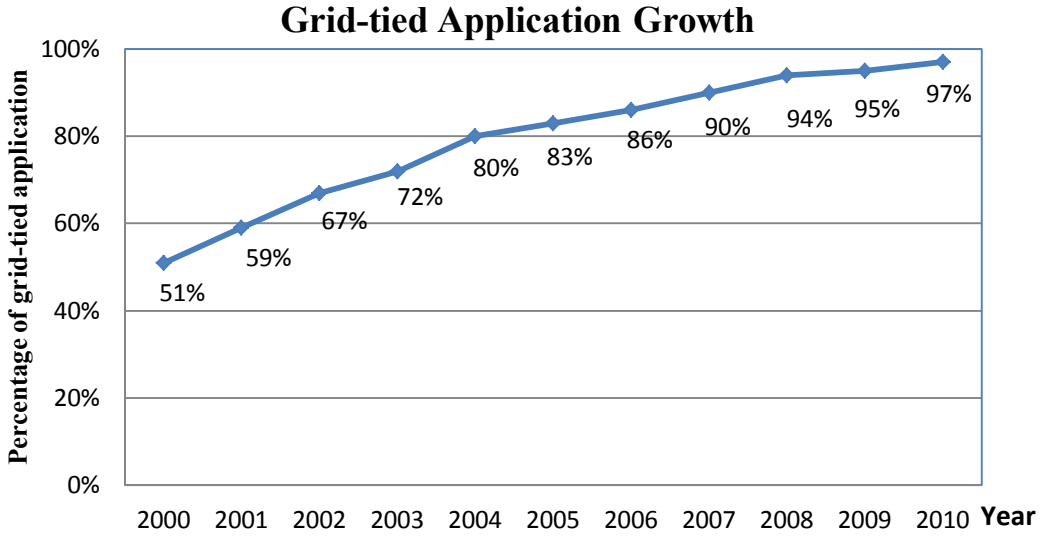


Fig. 1.2 Application contribution of photovoltaic energy

nullify variations caused by climatic changes [1]. Doing so helps to recover the investment costs sooner, and better streamline the process of grid connection, which presently is the most convenient way of distributing energy to distant consumers. The general rule of thumb enforced throughout the conversion process is to maintain high efficiency, quality and reliability, while not disturbing the grid significantly. These are challenges that must be addressed in the control schemes and realized by the power converters before sizable renewable sources can be tied to the grid for long term energy harnessing.

The aspect of control development usually covers maximum power point tracking, improved dynamics and fault ride-through, which presently have many recommended solutions [14][15]. The second aspect of proper converter design has also been actively investigated with one criterion commonly stated being to add voltage boost functionality to the converter. Recently, a new class of dc-ac Z-source inverters was proposed in [45], and has already been recommended for renewable applications [58]-[65]. For cases where ac inputs are available like with wind generators, ac-dc rectifiers can be placed before the Z-source inverters without modifying their operational principles. It is therefore appropriate to consider only dc-ac inversion without sacrificing generality.

Unlike the two-stage approach of connecting a dc-dc boost converter to a dc-ac voltage-source inverter (VSI), Z-source inverters are commonly referred to as single-stage topologies with both buck and boost capabilities. They are therefore more flexible than the traditional VSI and current-source inverter (CSI), whose outputs can only be stepped down or up, but not both. This, together with other advantages of the Z-source inverters like their lower sensitivity to noises, has aroused great interests among researchers with many insightful findings discussed. Contributing to the effort, a number of new findings has been proposed in the thesis, whose brief outlines are written in the next section before details are presented in later chapters.

1.2. Major Contributions of Thesis

Throughout the course of development, a number of new theoretical contributions has been made, and subsequently proven in simulations and experiments. They are briefly summarized here as:

- *Proposed alternate-cascading and dc-link-cascading techniques for merging multiple impedance networks to produce a higher voltage boost.*

- *Generalized the voltage-type switched-inductor Z-source inverters with multiple generic cells, and proposed the current-type switched-capacitor Z-source inverters with multiple generic cells. The former gives a higher voltage boost, while the latter gives a higher current boost.*

- *Proposed the tapped-inductor Z-source inverters, whose higher voltage boost is introduced by the turns ratio of the coupled inductors.*

- *Compared all existing boosting techniques, and subsequently proposed the alternate-cascaded switched-inductor and tapped-inductor topologies. Their gains are slightly reduced, but they have better distribution of component stresses.*

- *Proposed alternate-cascaded trans-Z-source inverters with high gains and lower stresses, while yet using lesser components.*

1.3. Organization of Thesis

This thesis is organized as nine chapters with most chapters focusing on the design of new Z-source inverters with enhanced voltage boost. A brief description of each chapter is now provided to give an overview of the thesis before proceeding to read the details in each individual chapter.

Chapter 1 begins by introducing the background and motivation behind the project, before listing down the new contributions discovered. Organization of the thesis is also shared to give insights on what to expect in each individual chapter.

Chapter 2 proceeds to review a few existing buck-boost topological options, before discussing their modulation concerns. This chapter is not meant to be exhaustive, but rather to provide basic knowledge on buck-boost energy conversion, which might be helpful for later chapters. A short review of typical photovoltaic systems is also provided here to show how converters can be incorporated to an example renewable source application.

Chapter 3 begins with the first contribution on embedded Z-source inverters with either asymmetrical or symmetrical structures. It covers a few impedance networks, which are subsequently generalized in Chapter 4, where cascading techniques are also discussed.

Chapter 5 continues to discuss a few non-cascaded Z-source inverters with enhanced voltage boost. Comparison between them and other existing techniques is also discussed to clearly identify advantages and shortcomings of each individual technique.

Chapter 6 extends the knowledge gained from Chapter 5 with two integrated techniques proposed for merging advantages in a few newly created Z-source inverters.

Chapter 7 adds a third integrated technique for creating Z-source inverters with enhanced voltage boost, while yet using lesser components than those discussed in Chapter 6.

Chapter 8 simulates a grid-tied photovoltaic system with one of the enhanced boost

Z-source inverters included. The intention is not really to create new thought, but to show the feasibility of realizing a system with the enhanced boost Z-source inverters.

Last but not least, Chapter 9 concludes the thesis, and recommends a few topics for future research.

Chapter 2 Voltage Buck-Boost Concepts

Power inverters of both two-level and multilevel configurations have so far been broadly applied to a vast number of dc-ac energy conversion systems, including ac motor drives [1], renewable energy interfaces [39] and uninterruptable power supplies [40]. Among the identified applications, inverters with both voltage-buck and boost operating capabilities might at times be needed, especially in renewable energy harnessing, where wide voltage tuning is needed for compensating unpredictable source voltage fluctuations caused by environmental, climatic and geographical changes.

In this chapter, a number of voltage-buck-boost inverters are reviewed to illustrate the concepts from which they are developed. A step-by-step understanding of the concepts reviewed here is deemed as helpful to the subsequent understanding of more advanced Z-source energy conversion concepts to be presented from Chapter 3 onwards. A short review of photovoltaic systems, chosen here as an example renewable source application, is also provided to show clearly where converters are included in them.

2.1. Elementary Two-Stage Buck-Boost Inverter

Fig. 2.1 shows a normal six-switch inverter for converting dc power from (e.g.) PV modules to ac power either for local consumption or channeling to the grid [16][17]. Its efficiency is high, and is now a standard topology found in many applications and products. It however lacks voltage tuning flexibility in the sense that its output voltage

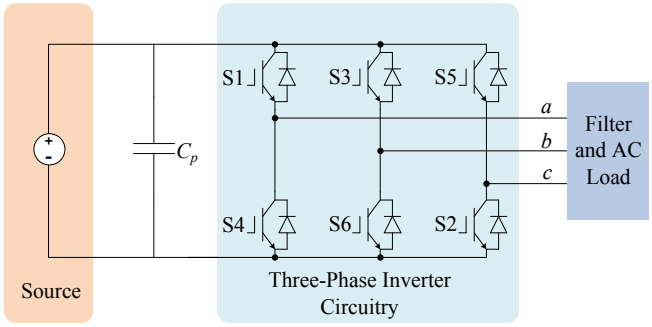


Fig. 2.1. Topological illustration of single-stage buck converter.

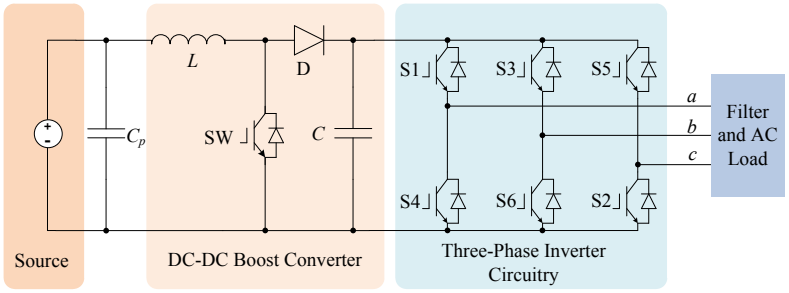
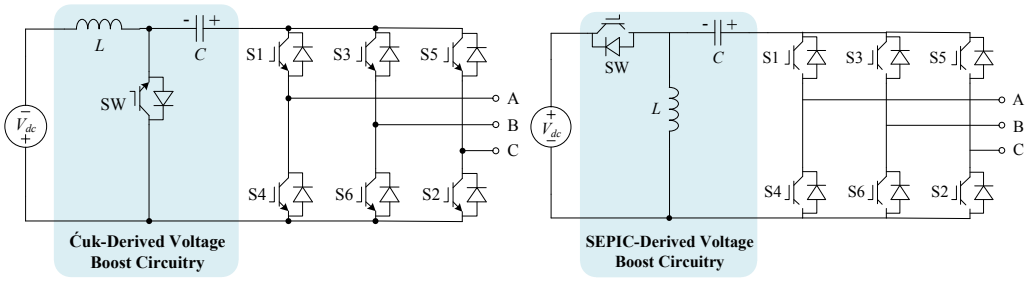


Fig. 2.2. Topological illustration of two-stage buck-boost inversion using a front-end dc-dc boost converter.

can only be stepped down but not up. For higher gain, either a line-frequency transformer can be added to its ac terminals or a dc-dc boost converter can be introduced to its dc terminals [41]. The latter shown in Fig. 2.2 is commonly referred to as the two-stage topology since the two elementary converter modules are merely placed together without any attempt to merge their functionalities. Its advantages would then be simplicity, independent control and the presence of a dc-link capacitor for buffering the two converter modules. It however includes an extra switch, its accompanied driving circuits and other passive components, which can be removed, if appropriate integration is practiced. This in fact is the motivation that has led to the development of various single-stage buck-boost inverters that use lesser components. A few of them is discussed next to illustrate the concepts behind them, which supposedly are applicable to other existing buck-boost converters too.

2.2. Ćuk and SEPIC-Derived Buck-Boost Inverters

Instead of the elementary dc-dc boost converter shown in Fig. 2.2, a Ćuk or SEPIC dc-dc converter can be placed in front of the six-switch inverter to create two more alternative two-stage solutions. They certainly will function well, but if some merging of converter functionalities is preferred, those single-stage Ćuk and SEPIC-derived inverters shown in Fig. 2.3 are recommended [44]. The demonstrated inverters use the same amount of components, comprising a VSI bridge, an inductor, a capacitor and one additional switch. Comparing with their unmerged two-stage correspondences, they use lesser passive components, and can therefore be more compact without compromising their introduced boosting ability [41].



(a) (b)

Fig. 2.3. Topologies of (a) Ćuk- and (b) SEPIC-derived buck-boost inverters.

Other variants like the diode-assisted Ćuk and SEPIC inverters can also be derived, but will not change the basic operating principles of the inverters [42]. It is therefore deemed as sufficient to demonstrate their operating characteristics using only the Ćuk and SEPIC-derived inverters shown in Fig. 2.3. Discussion on these two inverters is presented next to show how their switches should be controlled to introduce boost functionality to the basic VSI bridge.

2.2.1. Operational Principles of Ćuk-Derived Buck-Boost Inverter

The Ćuk-derived buck-boost inverter shown in Fig. 2.3(a) has two distinct operating modes, depending on whether a short circuit is formed across the dc-link of the VSI bridge. Expressions relevant to both operating modes are presented, as follows.

Non-Shoot-Through State: The non-shoot-through state is initiated by turning on switch *SW* to give the equivalent circuit shown in Fig. 2.4(a) for representing the Ćuk-derived inverter. Current I_L flows through the switch *SW* and dc source V_{dc} to charge inductor *L* with a rate of V_{dc}/L. Simultaneously, capacitor *C* clamps the dc-link voltage of the VSI bridge, which can either be in its active or null state (six active and two null states in total). For active state, energy from *C* will further be discharged to the external ac load.

Shoot-Through State: When switch *SW* turns off, the second shoot-through state surfaces, whose equivalent circuit is shown in Fig. 2.4(b). Inductive current I_L now

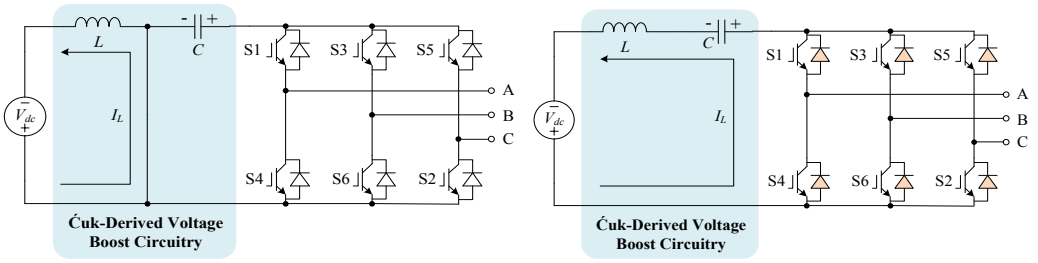


Fig. 2.4. Equivalent circuits of Ćuk-derived two-level inverter when (a) *SW* is ON and (b) *SW* is OFF.

discharges at a rate of $(V_{dc} - V_C)/L$, where V_C represents voltage across the capacitor C. The discharge current flows through the dc source, capacitor C (charging it in turn) and all anti-parallel diodes of the VSI bridge. DC-link of the VSI bridge is therefore shorted with no energy transfer to the ac load and zero line voltages appearing across it. This indeed is the same condition experienced by the load when *SW* is on and the VSI bridge is in its null state. The two states can therefore be interchanged to vary the amount of boosting introduced without modifying the normalized volt-sec average appearing across the load.

Understanding next that I_L must return back to its original value at the end of a period T, its incremental amounts in the two states must be equal in magnitude, as represented by the first expression in (2.1), where d_{ST} represents the duty ratio of the shoot-through state. Simplifying it leads to the second expression in (2.1) for computing V_C, which undoubtedly is a boosted value since $d_{ST} \leq 1$.

$$\frac{V_{dc}}{L} \cdot d_{ST} \cdot T = \frac{(V_C - V_{dc})}{L} \cdot (1 - d_{ST}) \cdot T \;; \qquad V_C = \frac{1}{1 - d_{ST}} \cdot V_{dc} \tag{2.1}$$

From (2.1), the ac output voltage $\hat{v}_{ac}$ can eventually be derived as [41]:

$$\hat{v}_{ac} = M \cdot \frac{V_C}{2} = M \cdot \frac{1}{1 - d_{ST}} \cdot \frac{V_{dc}}{2} \;; \qquad B = \frac{1}{1 - d_{ST}} \tag{2.2}$$

where M is the inverter modulation ratio, and $B = 1/(1 - d_{ST})$ is usually referred to as the boost factor. Overall voltage gain from the dc source to ac output is then given by $M \cdot B$.

2.2.2. Operational Principles of SEPIC-Derived Buck-Boost Inverter

Like its Ćuk-derived companion, the SEPIC-derived buck-boost inverter shown in Fig. 2.3(b) also has two distinct operating states, whose details are presented as follows.

Non-Shoot-Through State: Non-shoot-through state prevails when switch *SW* is on, leading to the equivalent circuit drawn in Fig. 2.5(a). Current I_L now flows through *SW* and the dc source to charge inductor L at a rate of V_{dc}/L. Together, capacitor C and the dc source also help to clamp the dc-link voltage of the VSI bridge at $V_{dc} + V_C$, which would appear across the ac load if the VSI is in its active state.

Shoot-Through State: Shoot-through state is introduced by turning *SW* off, leading to the equivalent circuit shown in Fig. 2.5(b). In this state, current I_L flows through all anti-parallel diodes of the VSI bridge to charge capacitor C and discharge inductor L at a rate of $-V_C/L$. With all anti-parallel diodes conducting, dc-link voltage of the shorted VSI bridge, and hence all three-phase line voltages, are zero. To the ac load, the shoot-through state is therefore no different from the non-shoot-through null state, whose relative time durations can be adjusted to vary the voltage gain without changing the normalized volt-sec average applied to the load.

Again setting the incremental changes in I_L in the two states to be equal, the capacitor

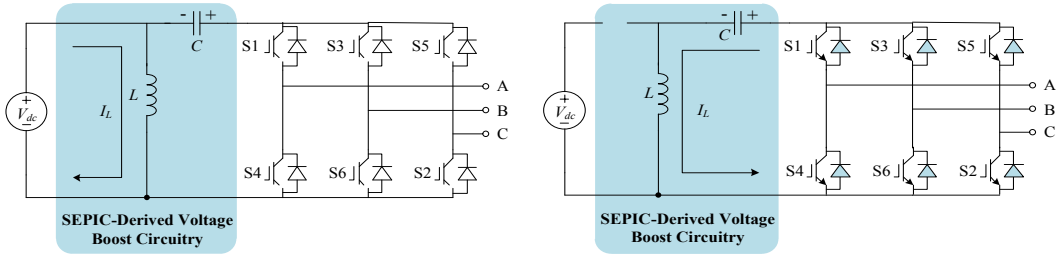


Fig. 2.5. Equivalent circuits of SEPIC-derived two-level inverter when (a) *SW* is ON and (b) *SW* is OFF.

voltage V_C can promptly be derived as:

$$\frac{V_{dc}}{L} \cdot d_{ST} \cdot T = \frac{V_C}{L} \cdot (1 - d_{ST}) \cdot T \;; \qquad V_C = \frac{d_{ST}}{1-d_{ST}} \cdot V_{dc} \tag{2.3}$$

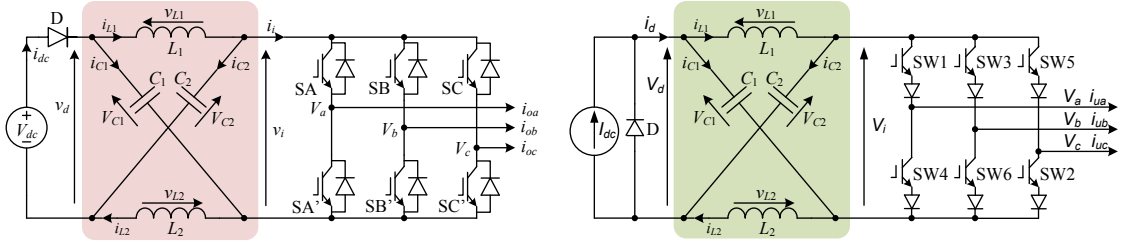
The ac output voltage is then given by [42]:

$$\hat{v}_{ac} = M \cdot \frac{V_C + V_{dc}}{2} = M \cdot \frac{1}{1-d_{ST}} \cdot \frac{V_{dc}}{2} \;; \qquad B = \frac{1}{1-d_{ST}} \tag{2.4}$$

where overall gain from the dc source to ac output is the same as that of the Ćuk-derived buck-boost inverter. The only difference observed between the two inverters is their different capacitor voltages with the SEPIC-derived circuit having a smaller value and hence a slight advantage in terms of lower voltage stresses (compare (2.1) and (2.3)).

2.3. Z-Source Buck-Boost Inverters

Z-source inverters were first proposed in [45] in both voltage-type and current-type configurations. The former is shown in Fig. 2.6(a), where a unique X-shaped impedance network is clearly seen between the input source and traditional VSI bridge. This impedance network gives the inverter its voltage-boost ability in addition to the usual voltage-buck operation that the VSI bridge can produce. Details of these operating modes are now discussed, which certainly will be helpful for comparison with later chapters where more advanced Z-source inverters are proposed.



(a) (b)

Fig. 2.6. Topologies of (a) voltage-type and (b) current-type Z-source buck-boost inverter.

2.3.1. Voltage-Type Z-Source Inverter

Voltage and current-type Z-source inverters have been developed at about the same time [45], but to date, interest in the former is slightly more intensive with its modulation [46][31]-[33], dynamics [34][35][47] and sizing [48] now investigated. Related applications like in motor drives [49]-[53], solar generation [55]-[64], fuel cell [36][37][54][65] and electric vehicles [56] have also been tried.

Regardless of the themes investigated, operating principles of the Z-source inverter remain unchanged, and would always involve charging of its two inductors for voltage boosting. Normal two-stage inverters would usually demand an additional active switch, which fortunately is avoided by the Z-source inverter. Instead, it substitutes the additional switching action demanded by the turning on of two switches from the same phase-leg of the VSI bridge (e.g. SA and SA' in Fig. 2.6(a)). Merging of functionalities among the existing switches is therefore visible, and the Z-source inverter is undeniably a single-stage inverter, which presently has been popular [18]-[30].

Unlike the earlier discussed Ćuk and SEPIC-derived inverters though, dc-link current of the Z-source inverter now flows through its shorted switches and not their anti-parallel diodes. Current flowing through the shorted switches will not cause damages, if not prolonged, because of the limiting action introduced by the dc inductors. Z-source inverter is therefore less prone to electromagnetic noises, and is generally a safer topology that does not require dead-time protection. Its two operating states are now described as follows.

Shoot-Through State: Shooting through of the VSI bridge is effected by turning on two switches from at least one of its phase-legs. The resulting equivalent circuit is shown in Fig. 2.7(a) with the VSI bridge and far-left diode *D* replaced by a short and open-circuit, respectively. Voltages across the inductors are then given by $v_L = V_C$, assuming that the impedance network is symmetrical ($v_{L1} = v_{L2} = v_L$ and $V_{C1} = V_{C2} = V_C$).

Non-Shoot-Through State: Non-shoot-through state of a Z-source inverter represents any of the six traditional active states or two null states of the VSI bridge. Its equivalent circuit is shown in Fig. 2.7(b) with diode *D* conducting. Voltages across the inductors are then rewritten as $v_L = V_{dc} - V_C$.

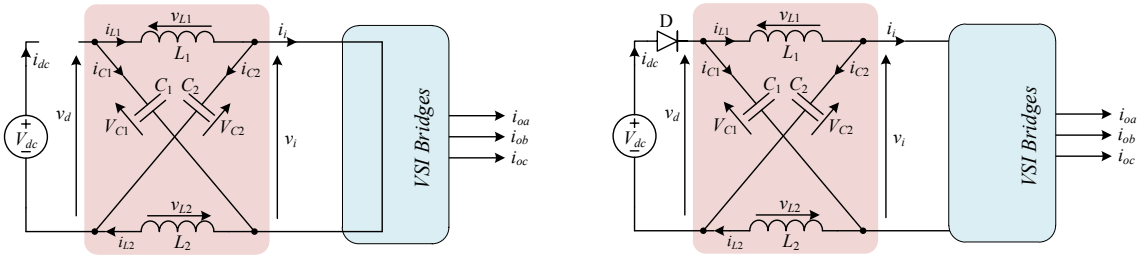
Averaging v_L over a switching period to zero then gives rise to the following expressions for relating the capacitor voltage V_C, peak dc-link voltage $\hat{v}_i$ and peak ac output voltage $\hat{v}_{ac}$ to the source voltage V_{dc}:

$$V_C = \frac{1-d_{ST}}{1-2d_{ST}} V_{dc} \tag{2.5}$$

$$\hat{v}_i = \frac{1}{1-2d_{ST}} \cdot V_{dc} \tag{2.6}$$

$$\hat{v}_{ac} = \frac{1}{1-2d_{ST}} \cdot \left(\frac{MV_{dc}}{2}\right) \tag{2.7}$$

where d_{ST} represents the fractional shoot-through time, $B = 1/(1-2d_{ST}) \geq 1$ is the boost factor, and $\frac{MV_{dc}}{2}$ is the peak phase output voltage from a traditional VSI [44]. Equation (2.7) clearly informs that for voltage-buck operation, d_{ST} should be set to zero, causing *B* to be 1. Voltage $\hat{v}_{ac}$ is then reduced by lowering *M* accordingly. On the other hand, for voltage-boost operation, d_{ST} should be non-zero, leading to $B > 1$. As seen later while reviewing the modulation theories, *M* should correspondingly be reduced according to $M \leq 1.15 \times (1 - d_{ST})$.



(a) (b)

Fig. 2.7. Equivalent circuits of voltage-type Z-source buck-boost inverter during (a) shoot-through and (b) non-shoot-through states.

2.3.2. Current-Type Z-Source Inverter

The current-type Z-source inverter, representing the dual of the voltage-type Z-source inverter, was studied in [45], and drawn in Fig. 2.6(b). In addition to the traditional nine active and null states, the added X-shaped impedance network allows current following into the dc-link of the CSI bridge to be interrupted (by turning off all switches for example) without causing any overvoltage. The resulting open-circuit state helps to introduce voltage-buck (or current-boost) functionality to the otherwise voltage-boost (or current-buck) only CSI, hence introducing greater flexibility to its control.

So far, the current-type Z-source inverter has not been as popular as its voltage-type variant, but some knowledge on it is definitely helpful given that it has recently been tried for solar energy harnessing [66]-[69]. The following therefore reviews its operating principles, which also would be helpful for comparison with more advanced current-type inverters presented in later chapters.

Open-Circuit State: A unique feature of the current-type Z-source inverter is its ability to assume open-circuit state by turning off all switches without causing overvoltage. This uniqueness is in fact the reason for its ability to boost current in addition to the usual current-buck operation supported by its CSI bridge. Its equivalent circuit can in turn be drawn as in Fig. 2.8(a) with its CSI bridge shown opened and diode *D* shown shorted. Relevant current expressions can then be derived as $I_{L1} = I_{L2} = I_L = i_{C1} = i_{C2} = i_C$, $i_d = I_L + i_C = 2I_L$ and $i_i = 0$.

Non-Open-Circuit State: When the current-type Z-source inverter enters one of the traditional six active or three null CSI states, diode *D* naturally blocks to give the non-open-circuit equivalent circuit drawn in Fig. 2.8(b). Its current relationships can follow up be summarized as $i_d = I_{dc}$, $i_C = I_{dc} - I_L$ and $i_i = I_L - i_C = 2I_L - I_{dc}$.

Averaging the Z-source capacitor current to zero in a switching period then leads to the

following expressions for computing the inductor current I_L, peak dc-link current $\hat{\imath}_i$ and peak ac current $\hat{\imath}_{ac}$ in terms of the source current I_{dc}.

$$I_L = \frac{1-d_{OC}}{1-2d_{OC}} \cdot I_{dc} \tag{2.8}$$

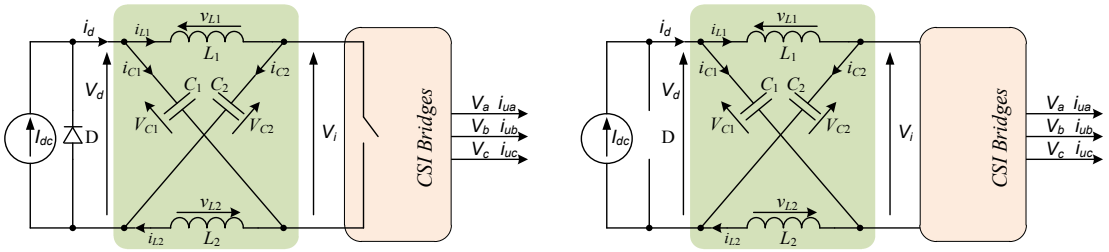
$$\hat{\imath}_i = \frac{1}{1-2d_{OC}} \cdot I_{dc} \tag{2.9}$$

$$\hat{\imath}_{ac} = \frac{1}{1-2d_{OC}} \cdot (MI_{dc}) \tag{2.10}$$

where d_{OC} represents the fractional time duration of the open-circuit state in a period, and MI_{dc} is the peak phase output current from a traditional CSI [69]. The boost factor here is $B = 1/(1-2d_{OC}) \geq 1$, which is the same as its voltage-type companion discussed in Section 2.3.1. Voltage-boost or current-buck operation is commanded now by setting d_{OC} to zero and lowering M accordingly. On the other hand, voltage-buck or current-boost operation is introduced by setting a non-zero d_{OC} to get $B > 1$. While doing so, M must be reduced according to $M \leq 1.15 \times (1 - d_{OC})$, as explained in the next section.

2.4. Pulse-Width Modulation Schemes for Buck-Boost Inverters

Modulation of buck-boost inverters shares the same basic operating principles. They demand the insertion of shoot-through or open-circuit states to the traditional VSI or CSI state sequences without modifying their normalized volt-sec or current-sec averages. The requirement then is to insert shoot-through or open-circuit states within null



(a) (b)

Fig. 2.8. Equivalent circuits of current-type Z-source buck-boost inverter during (a) open-circuit and (b) non-open-circuit states.

intervals only since they produce the same set of zero three-phase line voltages or currents to the externally connected ac load. This also means if the gain demanded increases, duration of the null states must be increased to accommodate for the longer shoot-through or open-circuit states. Corresponding active states of the inverter must therefore be reduced accordingly.

Based on these operating principles, a few modulation schemes have been proposed, but mainly associated with the Z-source inverters. They nonetheless can also be applied to other buck-boost inverters including the Ćuk and SEPIC-derived inverters studied earlier, as long as the appropriate gating signals are directed to the switches. They are therefore reviewed here without any emphasis on a specific type of inverter.

2.4.1. Simple Boost Method

The simple boost method is the simplest scheme proposed for Z-source inverter in [45] and illustrated in Fig. 2.9. Even though Fig. 2.9 and all other modulation figures presented hereon are for the voltage-type configuration, they are equally applicable to the current-type configuration after performing a simple logic state mapping to be discussed shortly.

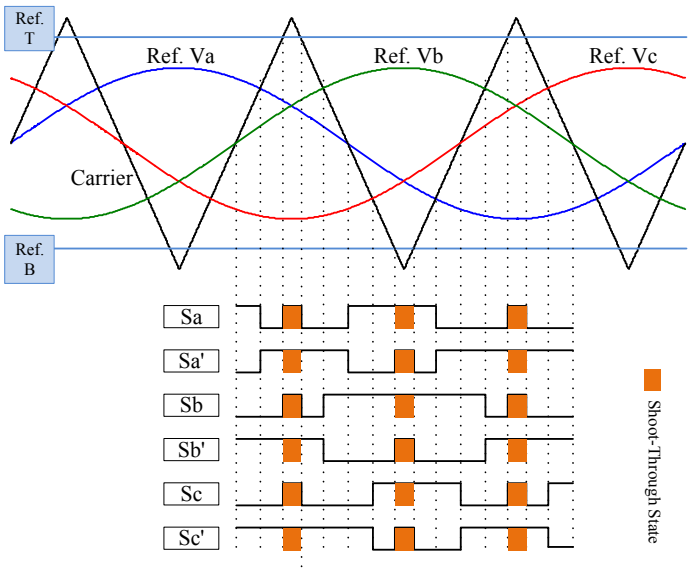


Fig. 2.9. Switching sequence generated by simple boost modulation scheme.

As per the modulation of a traditional VSI, three sinusoidal references are used in Fig. 2.9 to divide the switching period into non-shoot-through active and null states. Two additional linear references are then included to insert shoot-through states within the null intervals. To be more specific, when the carrier rises above the upper line or below the lower line, the inverter closes all its switches or at least two of them from the same phase-leg. Doing so always inserts the shoot-through states at the edges of each switching period, which in theory will not result in minimum switching. The inserted shoot-through time is however favorably kept constant to reduce low-order ripples detected in the inductor currents and capacitor voltages [45].

2.4.2. Maximum Boost and Maximum Constant Boost Methods

The maximum boost method is shown in Fig. 2.10, where instead of two additional lines, the maximum and minimum envelopes of the three-phase sinusoidal references are used for shoot-through insertion. Using the same comparison rules, the full null intervals will now be replaced by shoot-through states. The amount of boosting obtained will certainly be higher, but given that the shoot-through time is no longer constant, low-order ripples will surface in the impedance network. To reduce the ripples without increasing inductances and capacitances, the maximum constant boost method is proposed in [70]. The method uses the modified shoot-through reference lines shown in Fig. 2.11, which will keep a constant separation between them to give a constant boost ratio. Ripple

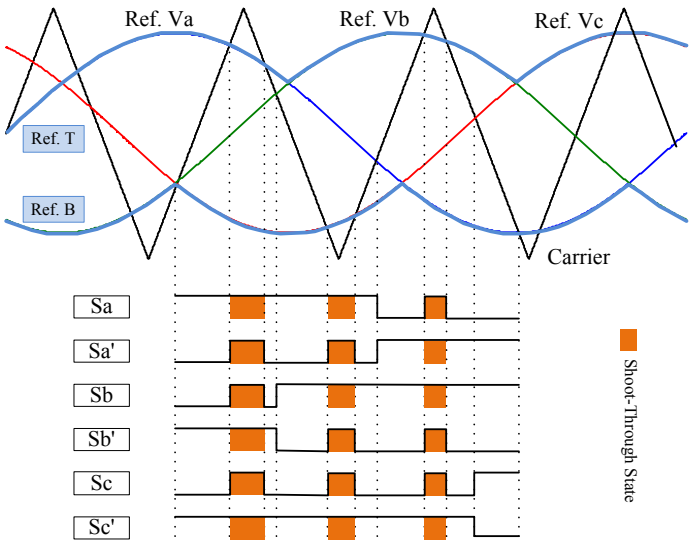


Fig. 2.10. Switching sequence generated by maximum boost modulation scheme.

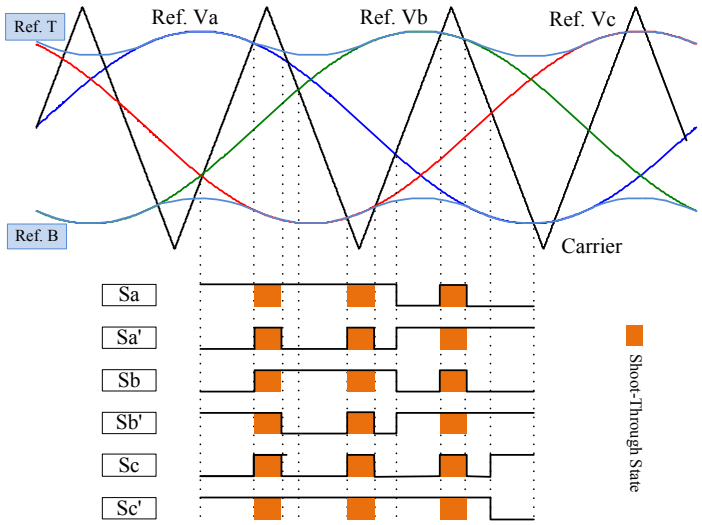


Fig. 2.11. Switching sequence generated by maximum constant boost modulation scheme.

components in the voltages and currents are therefore lower, together with the obtainable gain.

2.4.3. Modified Reference Method

Like the simple boost method, maximum boost and maximum constant boost methods insert the shoot-through states at the edges of each switching period. In theory, this does

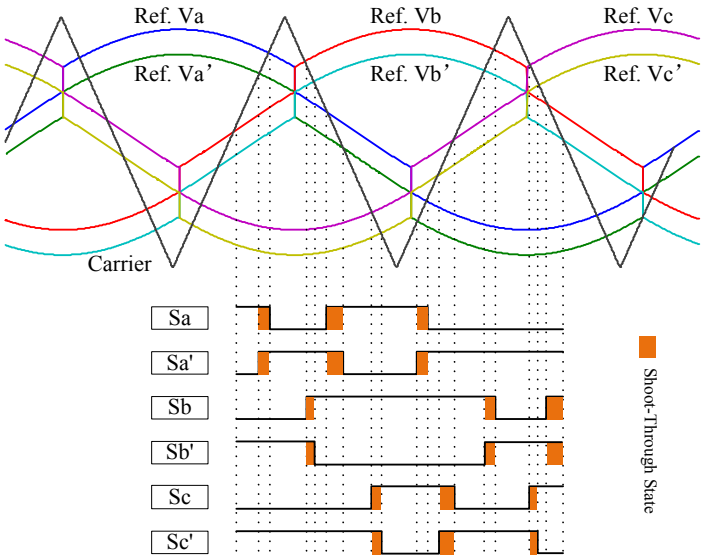


Fig. 2.12. Switching sequence generated by modified reference modulation scheme.

not give minimum commutations. To optimize on that aspect, the method shown in Fig. 2.12 is recommended. It uses two modified sinusoidal references per phase-leg for independent control of its two switches [46].

$$\begin{cases} V_{\max(SX)} = V_{\max} + V_1 \\ V_{\max(SX')} = V_{\max} + V_2 \end{cases}$$
$$\begin{cases} V_{\mathrm{mid}(SX)} = V_{\mathrm{mid}} + V_2 \\ V_{\mathrm{mid}(SX')} = V_{\mathrm{mid}} - V_2 \end{cases}$$
$$\begin{cases} V_{\min(SX)} = V_{\min} - V_2 \\ V_{\min(SX')} = V_{\min} - V_1 \end{cases}$$
$$V_1 = d_{ST} \ , \ V_2 = d_{ST}/3 \ , \ X = A, B \text{ or } C , \tag{2.11}$$

By vertically shifting these references according to (2.11), shoot-through states are inserted by advancing or delaying the switching instants of the two switches per phase-leg without additional commutation. Shoot-through states are therefore found between two non-shoot-through active states or between one active and one null states, and not at the edges of each switching period.

2.4.4. State Mapping for Modulation of Current-Type Inverters

A simple way of modulating the current-type inverters is to map their switching states from those of the voltage-type inverter. This is feasible since both inverters share the same hexagonal shape for their vector diagrams, as illustrated in Fig. 2.13. It is therefore a direct one-to-one map for the active states, which can conveniently be done by discrete

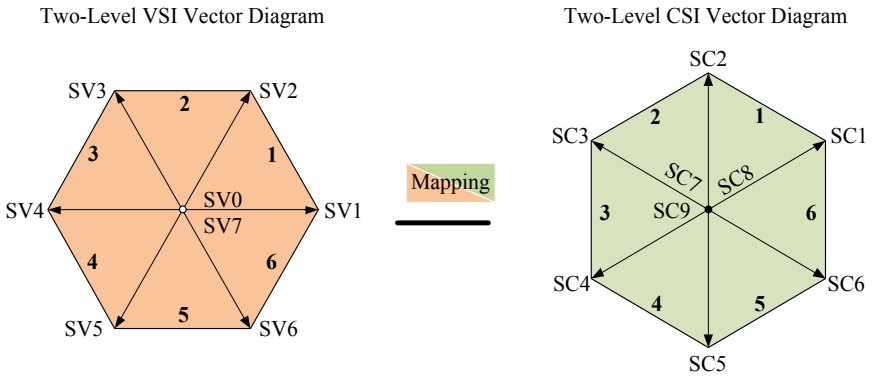


Fig. 2.13. Illustration of vector diagram mapping from VSI to CSI.

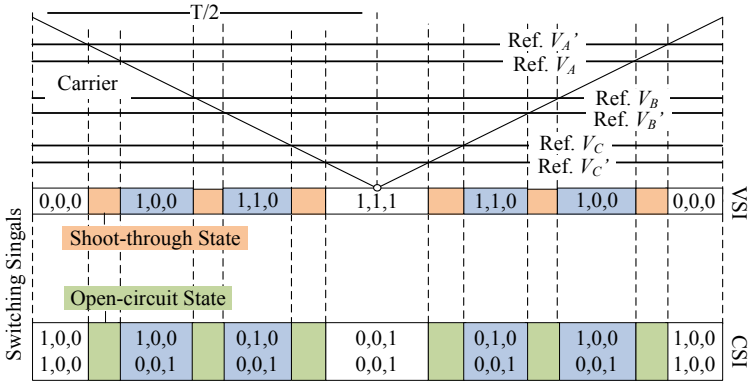


Fig. 2.14. Illustration of switching state mapping from voltage-type to current-type Z-source inverter.

chips or a programmable logic device. Mapping of the two voltage-type null states to three current-type null states, although slightly more involved, can still be implemented according to [71]. Lastly, all obtained shoot-through states can be mapped to a single open-circuit state with all switches of the CSI bridge opened. An example illustrating the mapping is shown in Fig. 2.14, where the upper state sequence is for the voltage-type inverter and the lower mapped sequence is for the current-type inverter.

2.5. Structures of Grid-Tied Photovoltaic Systems

From the statistical data read in Chapter 1, it cannot be denied that PV generation is presently a well-developed technology with many ways of realization. A few common PV structures are now reviewed to give an indication of where power converters can be incorporated. The review is not meant to be exhaustive, and is presented as two levels of realization. The first level categorizes PV inverters in terms of the ways PV modules are connected. The second level comprises only two categories, depending on the number of power conversion stages used. To some extent, decision made at level 2 is dependent on that made at level 1.

2.5.1. Level 1 – PV Module Connection

Referring to [12], PV structures can be categorized as centralized, string, multi-string

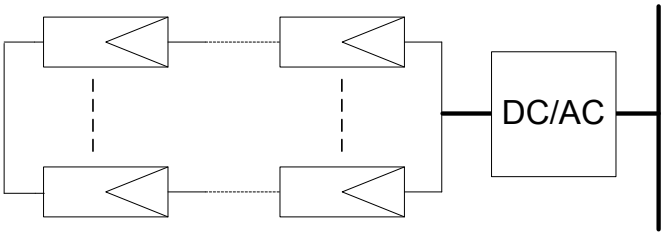


Fig. 2.15 Centralized connection of PV modules.

and modular connections. For centralized connection shown in Fig. 2.15, all PV modules are grouped together before being connected to the grid by a centralized inverter with high ratings. The PV modules are mostly in series to produce the high voltage needed by the centralized dc-ac inverter, which now needs no transformer or dc-dc converter for voltage boosting. Reliability of the centralized inverter can however be poor, and the PV modules would be more prompt to partial shading effect. To address these concerns, the string configuration shown in Fig. 2.16 is proposed. Some decentralization has now been introduced since the PV modules are no longer clustered together, but organized as strings. Each string has its own inverter, which certainly can be controlled independently even if some strings malfunction.

A modification to the string configuration, referred to as the multi-string configuration, is shown in Fig. 2.17. Here, each string has its own dc–dc converter, which is eventually connected to a common dc–ac inverter. Therefore, each dc-dc converter can perform its own maximum-power-point-tracking (MPPT) for its associated string, and at the same time, boost its input voltage to a high enough value suitable for tying to the dc-ac inverter. However, like the centralized arrangement, the common dc-ac inverter would

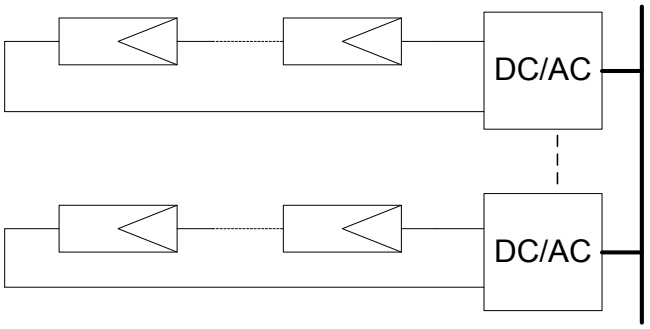


Fig. 2.16 String connection of PV modules.

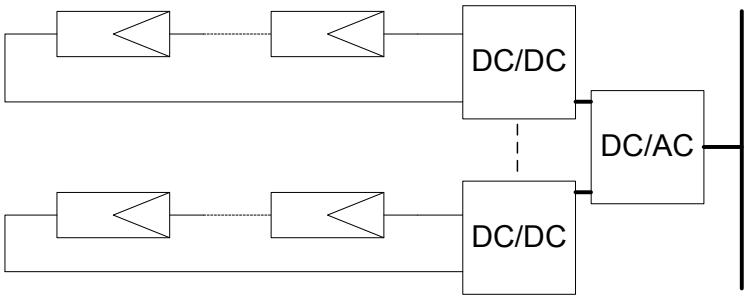


Fig. 2.17 Multi-string connection of PV modules.

form a single point of failure, which surely is undesirable.

The last possible configuration is the modularized system shown in Fig. 2.18, where each PV panel is drawn to have its own dc-ac inverter, forming an ac module in turn. The main challenge here is to develop a modularized inverter that can have all needed features for grid connection, while at the same time, maintain high efficiency. These goals have continually motivated researchers to find new converter topologies, like those reported in [12].

2.5.2. Level 2 – Number of Power Conversion Stages

Depending on the type of PV configuration chosen, the inverter realized can either be single or double conversion stages. For single-stage, the PV power is converted and injected to the grid by using only a single inverter with high efficiency, as shown in Fig. 2.19. The PV modules therefore need to be series-connected to give the required high dc voltage for direct connection to the dc side of the inverter. Alternatively, a line-frequency transformer can be added to the inverter ac output for voltage boosting if the terminal voltage from the PV modules is not high enough. Adding a transformer also

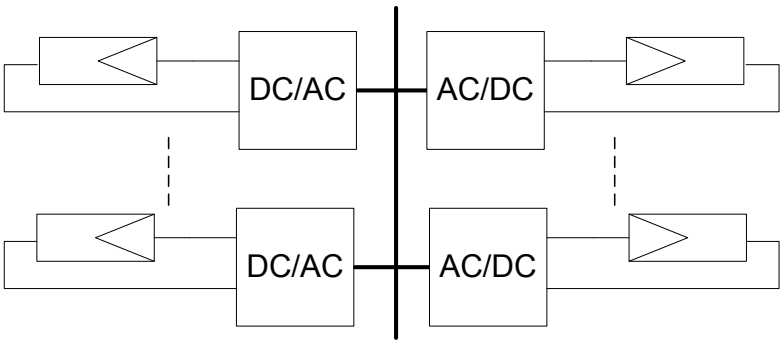


Fig. 2.18 AC modular connection of PV modules.

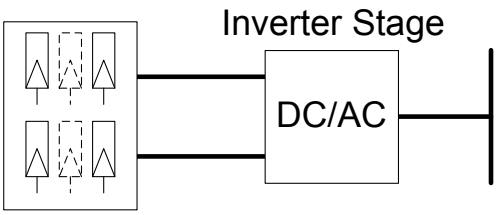


Fig. 2.19 Illustration of single-stage conversion system.

provides isolation, which might be requested by some national grid codes. Control of the single-stage inverter can be quite involved though because it has to track the maximum power point of the PV modules, and feed the power to the grid with satisfactory quality.

In contrary, the two-stage power conversion system shown in Fig. 2.20 provides a voltage boost capability in the front-end dc-dc converter. Therefore, the bulky line-frequency transformer can be removed if electrical isolation is not required. In detail, the target of the first stage is to boost the voltage and track the maximum power point (MPP) usually using a simple boost-type dc-dc converter with or without an intermediate high-frequency transformer. With these functions, the front-end dc-dc converter would ensure proper energy conversion from the PV over a very wide input range. The only likely disadvantage with the two-stage solution is its efficiency and reliability might generally be lower since more passive and active components are involved in the energy conversion process, as compared to the single-stage solution.

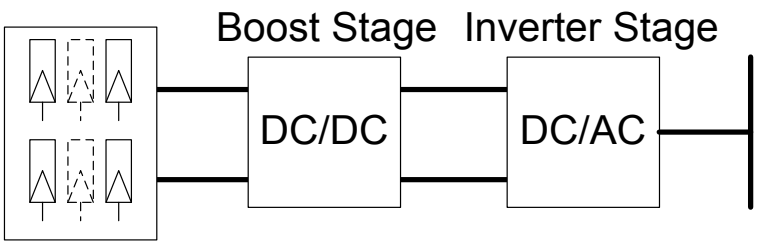


Fig. 2.20 Illustration of two-stage conversion system.

2.6. Summary

As a background, Chapter 2 shares basic knowledge on buck-boost inverters with both single-stage and two-stage structures, including their topologies and modulation schemes. That knowledge can help with understanding of more advanced developments presented from Chapter 3 onwards. As a start, the standard two-stage converter with a dc-dc boost converter added to a dc-ac inverter is reviewed. It is certainly a straightforward and robust approach for gaining buck-boost flexibility, but might presently lack rooms for research excellence. Single-stage topologies including the Ćuk-derived, SEPIC-derived and Z-source inverters are next reviewed, together with their common modulation principles. The intention here is not really to view at all existing circuits, but to acquire enough knowledge related to buck-boost inversion. This knowledge can subsequently be applied to other more advanced Z-source inverters proposed here as contributions of the thesis.

Chapter 3 Embedded Z-Source Inverters

Over the years, developments linked to Z-source inverters have advanced along many different directions, but still using the same impedance network, as shown in Fig. 2.6. That certainly proves the effectiveness of the network, but does not solve any of its existing shortcomings. One of them is linked to the chopping current or voltage imposed on the dc source if no external filter is added after the source. The chopping terminal quantities are caused by the existence of a diode either in series or parallel with the source, as shown in Fig. 2.6. They can have high instantaneous values that will not only raise the semiconductor ratings, but will also complicate the MPPT process found in most renewable energy systems [73]. At times, the chopping current quantities might also hinder the system response since averaging of measured signals is usually needed, and can even degrade the lifetime of the input source.

To smooth the quantities, one simple method is to add a low-pass LC filter after the source. Although effective, the added filter usually raises the system cost, and can at times complicate the system design since more LC resonant modes need to be considered. Therefore, instead of relying on an external filter, the embedded impedance concept is proposed in [72], where dc sources are embedded within the impedance network to gain filtering advantages without adding external filters. Building on this new embedded concept, a number of alternative inverter topologies named as the embedded Z-source inverters is studied and verified here in simulation and experiment.

Note that overall gains of the embedded inverters remain unchanged, which strictly is not in line with the theme of enhanced boost defined for this thesis. They nonetheless are important since concepts understood from them can later be applied to those enhanced boost topologies presented from Chapter 3 onwards to create variants that have added advantages. Specific details can be found in the relevant chapters.

3.1. Capacitive-Shunt Embedded Z-Source Inverters

Capacitive-shunt embedded (CSE) Z-source inverters are the first group of alternative

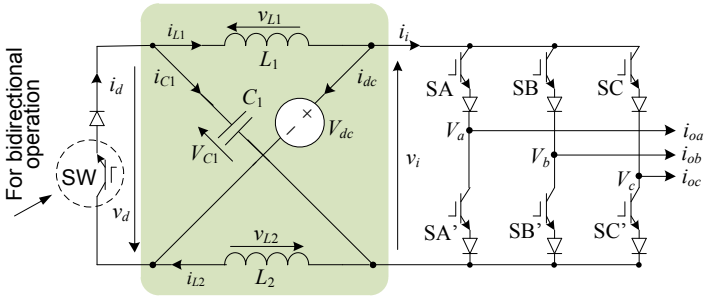


Fig. 3.1. Schematic of asymmetrical CSE Z-source inverter.

inverters studied with internal filtering ability. They can either be of the asymmetrical or symmetrical types, whose similarities and differences are outlined below.

3.1.1. Asymmetrical Topology

An illustration of the asymmetrical CSE inverter is shown in Fig. 3.1, where a feature noted is its rear-end CSI bridge rather than the more common VSI bridge. It is therefore comparable to the current-type Z-source inverter shown in Fig. 2.6(b), and can enter either the open or non-open-circuit state, as reviewed in Chapter 2. Despite this noted similarity, it is still important to verify that no other erroneous states will surface during each switching cycle. To ensure that, each of the three permitted switching states are examined in turn, beginning with the non-open-circuit null state. Equivalent circuit of the state drawn in Fig. 3.2(a) reveals that its inductive voltage expressions can be determined as (3.1), whose values are positive, implying that the inductive currents are ramping up linearly.

$$v_{L1} = V_{C1}; \qquad v_{L2} = V_{dc} \tag{3.1}$$

Upon transiting from the null state to an active state, the equivalent circuit changes to that drawn in Fig. 3.2(b), where an output voltage source v_i is drawn for representing the CSI bridge and external ac load. This representation is justified since the immediate ac output of a CSI bridge is usually connected to a filter capacitor, which when viewed at the inverter dc-link, will appear like a voltage source. The new set of inductive voltage expressions are then written as (3.2), which strictly are negative since v_i is always higher than V_{dc} and V_{C1} for voltage-boost operation.

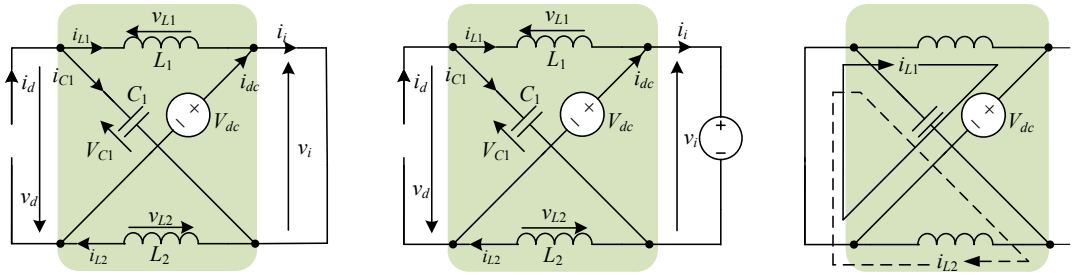


Fig. 3.2. Equivalent circuits of asymmetrical CSE Z-source inverter when in (a) null state, (b) active state and (c) open-circuit state.

$$v_{L1} = V_{C1} - v_{i1} \;\; ; \;\; v_{L2} = V_{dc} - v_i \tag{3.2}$$

Moving on to consider the third open-circuit equivalent circuit shown in Fig. 3.2(c), the inductive voltages can be rewritten as (3.3), which again are negative.

$$V_{dc} = -v_{L1} \; ; \; V_{C1} = -v_{L2} \; ; \; i_{L1} = -i_{dc} \; ; \; i_{L2} = i_{C1} \tag{3.3}$$

With all three states present in a switching cycle, the above derived equations can conclude that the null state causes the inductive currents to rise, while the open-circuit state causes them to fall. The net change Δi_L depends on their respective time durations since their voltage magnitudes are noted to be the same, as seen from (3.1) and (3.3). If Δi_L is positive, the inverter responds by producing v_i to be larger than $V_{dc} \approx V_{C1}$, so that the inductive voltages detected in the active state are negative. This corresponds to the voltage-boost mode, whose resulting negative inductive voltages force the positive Δi_L back to zero at the end of the switching cycle. Although this scenario is conceptually feasible, it is practically less likely to surface since voltage-buck operation with $v_i \le V_{dc} \approx V_{C1}$ is more likely to prevail whenever open-circuit state is used.

Therefore, instead of considering $\Delta i_L > 0$, the alternative cases of $\Delta i_L < 0$ and $\Delta i_L = 0$ are considered with nearly the same conclusion drawn. To be more precise, v_i will be stepped down naturally by the inverter to a value smaller or equal to $V_{dc} \approx V_{C1}$. That in turn gives rise to either a set of positive or zero inductive voltages that would smoothly bring Δi_L back to zero at the end of the active interval. For these cases, diode D in the equivalent circuits of Fig. 3.2(a) and (b), will not erroneously "jump" from off to on

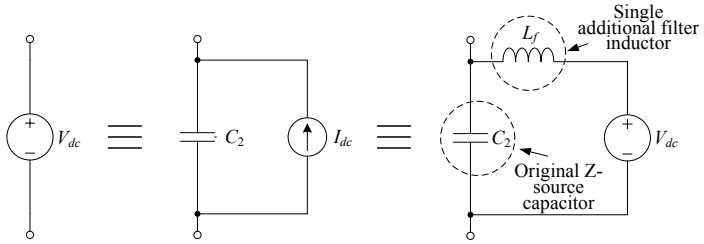


Fig. 3.3. Equivalent source representations for analyzing CSE inverters.

since forward voltage across it, expressed as $v_d = v_i - V_{dc} - V_{C1}$, is always negative for voltage-buck mode with $v_i \leq V_{dc} \approx V_{C1}$. This confirms that overall accuracy of the proposed CSE Z-source inverter is preserved in both voltage-buck and boost operating modes.

Another point to note with the CSE inverter is that its gain is the same as that of the conventional current-type Z-source inverter shown in Fig. 2.6(b) since their switching states give rise to the same mathematical equations. In fact, the CSE inverter can be viewed as a current-type inverter since its rear-end terminals are tied to a three-phase CSI bridge and its input dc source can be represented by the parallel connection of a capacitor and a current source. The latter is demonstrated by the second circuit drawn in Fig. 3.3. Instead of including an explicit current source, the third arrangement of connecting a voltage source in series with a filter inductor L_f can be used as an alternative, and is drawn at the far-right of Fig. 3.3. Comparing with the conventional Z-source inverter conditioned by a second-order input filter, the CSE inverter powered by the third source arrangement still uses one lesser filter capacitor since the capacitance needed is provided by one of the existing network capacitors, as indicated in Fig. 3.3.

3.1.2. Symmetrical Topology

The topology shown in Fig. 3.1 is asymmetrical since only one of its shunt branches has a dc source embedded, while the other is a storage capacitor. Although it has already been proven to function well, its asymmetry causes unbalanced electrical stresses to be experienced within the impedance network. For illustration, the voltage-boost operating mode is considered during which input diode D is always reverse-biased. Since D is not conducting, current flowing through inductor L_1, connected in series with C_1, is always zero on average. On the other hand, current flowing through L_2 is supplied by the dc

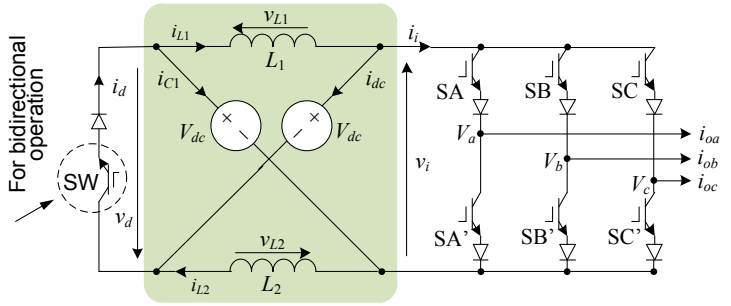


Fig. 3.4. Schematic of symmetrical CSE Z-source inverter.

source, which surely is non-zero on average in order for it to transfer energy to the external ac load. Therefore, even though $V_{dc} \approx V_{C1}$, the current stresses and hence thermal dissipations experienced by the two Z-source inductors are different.

To better balance out the operating conditions, the symmetrical structure shown in Fig. 3.4 is recommended as an alternative, where C_1 is replaced by a second dc source having the same terminal voltage. Doing so will not affect the voltage gain expressions, but will balance out the required current ratings of L_1 and L_2. At first sight, the requirement for two dc sources might appear as a severe disadvantage, but on second thought, configuring two dc sources might not be tough if multiple source units like photovoltaic (PV) panels, fuel cells and batteries are available. The configured sources should ideally be equal in order to balance out the electrical stresses within the impedance network.

This is however not a strict requirement since any slight unbalance intentionally or unintentionally introduced will simply be absorbed within the impedance network with some components experiencing slightly higher stresses than the others. The underlying principle is the same as that governing the smooth operation of the asymmetrical CSE inverter, where only one source is used. Therefore, for unbalance, the only necessary design provision is to cater for an alternative current flow path by paralleling capacitors with the input sources. This allows reverse power to occasionally flow from the source with higher voltage to the other with lower voltage through its paralleled capacitor. Such scenario is likely to happen frequently within renewable energy systems, where voltages of unidirectional sources change with climatic conditions.

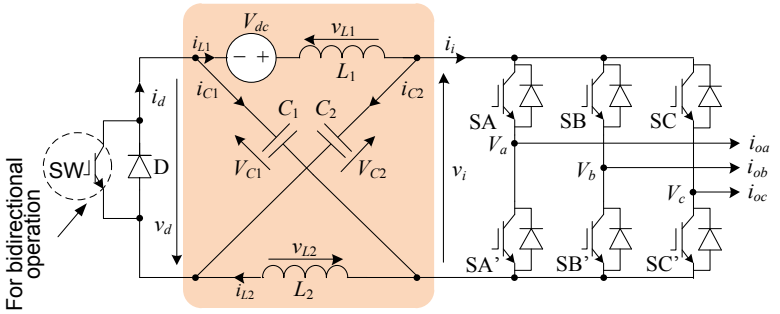


Fig. 3.5. Schematic of asymmetrical ISE Z-source inverter.

3.2. Inductive-Series Embedded Z-Source Inverters

In addition to embedding sources to the shunt branches, a second possibility is to insert them in series with the Z-source inductors to derive the inductive-series embedded (ISE) Z-source inverters. Types, operating principles and advantages of the ISE inverters over the conventional and CSE Z-source inverters are described in details, as follows.

3.2.1. Asymmetrical Topology

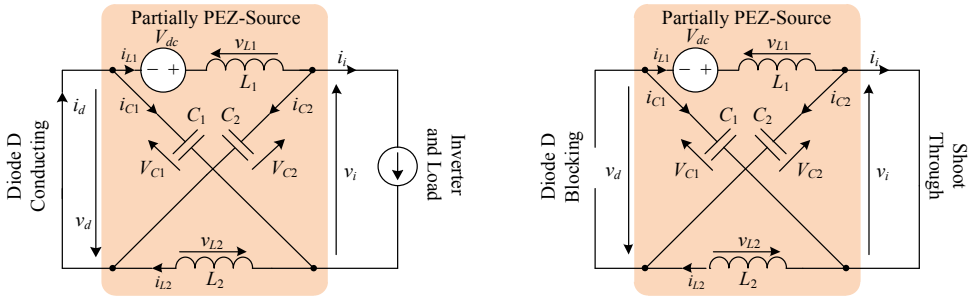
The asymmetrical ISE inverter implemented using only a single dc source is shown in Fig. 3.5. Its asymmetry causes voltage stresses experienced by its Z-source capacitors C_1 and C_2 to be unbalanced. Mathematically, this unbalance in capacitive voltages, together with other gain expressions, can be derived by analyzing those equivalent circuits drawn in Fig. 3.6(a) and (b) for representing the non-shoot-through and shoot-through states, respectively. Performing such analyses appropriately gives rise to the following sets of preliminary voltage expressions [7].

Non-Shoot-Through with Diode D Conducting

$$\begin{cases} v_{L1} = V_{dc} - V_{C2} \\ v_{L2} = -V_{C1} \\ v_i = V_{C1} + V_{C2} \end{cases} \tag{3.4}$$

Shoot-Through with Diode D Blocking

$$\begin{cases} v_{L1} = V_{dc} + V_{C1} \\ v_{L2} = V_{C2} \\ v_i = 0 \end{cases} \tag{3.5}$$



(a) (b)

Fig. 3.6. Equivalent circuits of asymmetrical ISE Z-source inverter when in (a) non-shoot-through and (b) shoot-through states.

Setting average voltages across the inductors to zero then gives rise to the following two capacitive voltages, expressed as:

$$\begin{cases} V_{C1} = V_{dc}\dfrac{d_{ST}}{1-2d_{ST}} \\ V_{C2} = V_{dc}\dfrac{1-d_{ST}}{1-2d_{ST}} \end{cases} \tag{3.6}$$

Equation (3.6) clarifies that voltage stress experienced by C_2 is higher than that across C_1 over the full shoot-through variation range expressed as $0 \le d_{ST} < 0.5$. Despite that, the input-to-output voltage gain of the asymmetrical ISE inverter remains the same as that of the conventional Z-source inverter. The ISE inverter therefore does not suffer any gain degradation even though it has the added advantage of implicit source filtering contributed by one of its Z-source inductors. No external filter is thus needed.

3.2.2. Symmetrical Topology

The unbalanced capacitive voltages experienced by the asymmetrical ISE inverter can

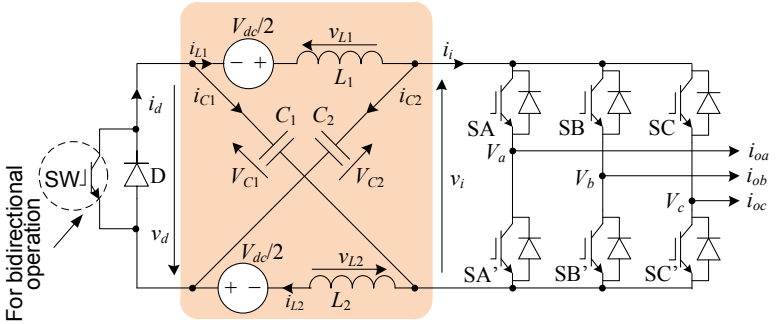


Fig. 3.7. Schematic of symmetrical ISE Z-source inverter.

be equalized by adding a second dc source in series with L_2 in addition to the one placed in series with L_1. The resulting symmetrical topology is shown in Fig. 3.7, where one noted feature is that the voltage of each source is $0.5V_{dc}$ and not V_{dc} like in Fig. 3.5. Since both sources are connected in series when in the non-shoot-through state like in Fig. 3.8(a), total source voltage appearing across the external ac load would still be V_{dc}. Mathematical expressions for representing it and the shoot-through equivalent circuit in Fig. 3.8(b) can thus be derived as [7]:

Non-Shoot-Through with Diode D Conducting

$$\begin{cases} v_L = V_{dc}/2 - V_C \\ v_i = V_{dc}/2 + V_C - v_L = V_{dc} - 2v_L = 2V_C \end{cases} \tag{3.7}$$

Shoot-Through with Diode D Blocking

$$\begin{cases} v_L = V_{dc}/2 + V_C \\ v_i = 0 \end{cases} \tag{3.8}$$

Averaging the inductive voltage to zero in a switching period then leads to the following Z-source capacitive voltage expression.

$$V_C = \frac{V_{dc}/2}{1 - 2d_{ST}} \tag{3.9}$$

Comparing (3.9) with the first expression in (2.5) immediately reveals that ISE and conventional Z-source inverters share the same denominator, but have different numerators. Numerator of (3.9) is fixed at $0.5V_{dc}$, which certainly is smaller than that of (2.5) expressed as $(1 - d_{ST})V_{dc}$. The latter changes from V_{dc} to $0.5V_{dc}$ as d_{ST} increases

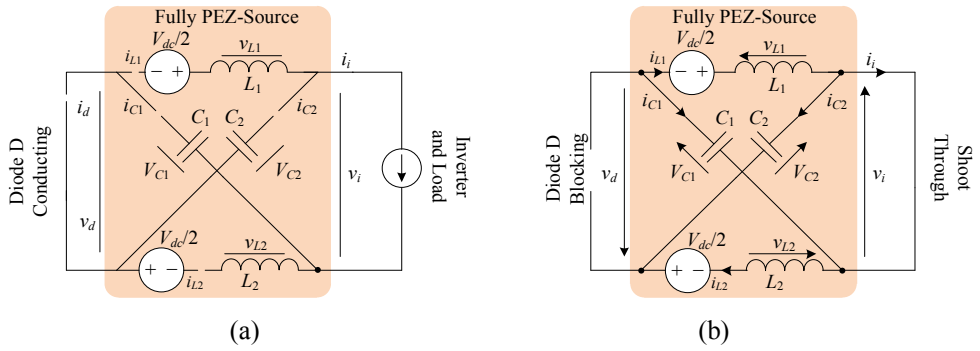


Fig. 3.8. Equivalent circuits of symmetrical ISE Z-source inverter when in (a) non-shoot-through and (b) shoot-through states.

from 0 to 0.5. Therefore, voltage stresses experienced by the two capacitors of the ISE inverter are always smaller than those within the conventional Z-source inverter. This certainly is logical since the dc sources embedded within the impedance network are there to share the voltage stresses experienced by the capacitors, hence allowing their voltages to be lowered. The same explanation can be applied to the asymmetrical ISE inverter shown in Fig. 3.5, where only one dc source is embedded to share one of the capacitive voltages. Therefore, one capacitive voltage V_{C1} appears smaller, while the other unshared capacitive voltage V_{C2} appears similar to that of the conventional Z-source inverter, as depicted by (2.5).

Proceeding next to substitute (3.9) into the non-shoot-through equations listed in (3.7), the peak dc-link and ac output voltages are found to be similar to those listed in (2.6). Therefore, the ISE inverters proposed here are summarized to produce the same voltage gain, while at the same time offer advantages like lower capacitive voltage stresses and smoother source currents filtered solely by the existing Z-source network.

3.3. Other Features for Comparison

Earlier mathematical proofs and discussions have already confirmed that the embedded Z-source inverters experience lower component stresses and have internal source filtering ability, while producing the same gain as their conventional counterparts. In addition to these characteristic features, other issues like LC parameter selection, semiconductor stresses, spectral performances and dynamic responses can be of interest, and are therefore raised here for further comparison. Instead of comparing both CSE and ISE inverters with their conventional counterparts, only the ISE inverter is considered if the mathematical derivation or theoretical explanation is too lengthy. This partial comparison is deemed as sufficient since CSE inverters are after all the duals of the ISE inverters, and therefore need not be explicitly duplicated.

3.3.1. LC Parameter Selection

At present, the most prominent factor hindering the application of Z-source inverters is their passive X-shaped *LC* impedance network. Attempts to size them appropriately are therefore important, and have previously been pursued by a few researchers in [74]-[76].

These findings are equally applicable to the embedded Z-source inverters, which use the same X-shaped impedance network except with one or two sources embedded within it. Considered the ISE inverter as an example, the first governing rule of thumb to apply is to select the Z-source capacitors C_1 and C_2 to be large enough to provide the required amount of energy storage. Having large enough capacitors also help to bias the impedance network more towards the voltage-source nature so that it better adapts with the rear-end VSI bridge tied to an overall inductive load.

Upon confirming the required capacitances, inductors L_1 and L_2 are sized so that the input diode will not unintentionally block when in a non-shoot-through state, which when happened, will give rise to those additional unwanted switching states reported in [75]. That means diode current with its ripple considered must always be above zero when in the non-shoot-through state ($i_d > 0$ in Fig. 3.5 and Fig. 3.7). Since $i_d = i_{L1} + i_{C1} = i_{L1} + (i_{L2} - i_i)$, the limiting condition can further be re-written as:

$$\begin{aligned} &\textbf{\textit{Asymmetrical ISE}}: \quad i_{L1} + i_{L2} > i_i \quad \Rightarrow (I_L + \Delta i_{L1}) + (I_L + \Delta i_{L2}) > I_o \\ &\textbf{\textit{Symmetrical ISE}}: \quad i_L > 0.5 i_i \quad \Rightarrow (I_L + \Delta i_L) > 0.5 I_o \end{aligned} \tag{3.10}$$

where $\{I_{L1} = I_{L2} = I_L\}$ are the equal average inductor currents since average capacitor currents are zero, $\{\Delta i_{L1}, \Delta i_{L2}, \Delta i_L\}$ are the peak current ripples, and I_o is the peak ac current, which is also the "worst case" dc-link current i_i when in the non-shoot-through state.

Since the inductor current is also the source current, its value can be determined by considering power balance on the dc and ac sides:

$$I_L = 3\, V_o\, I_o \cos\varphi \,/\, (2\, V_{dc}) \tag{3.11}$$

where V_o and $\cos\varphi$ are the peak ac output voltage and power factor imposed by the external ac load. Upon substituting the load requirements to (3.11) and then to (3.10), a ripple current requirement can be derived for sizing the Z-source inductors. Taking the symmetrical ISE inverter as an example, the calculated current ripple requirement of $\Delta i_L > 0.5 I_o - I_L$ can be combined with the following ripple equation (3.12) for the

non-shoot-through state to derive the final expression (3.13) for sizing L.

$$\Delta i_L = \frac{(T - T_0)}{L}\left\{\frac{V_{dc}}{2} - \frac{V_{dc}/2}{1 - 2T_0/T}\right\} \tag{3.12}$$

$$L > \frac{V_{dc}(T - T_0)T_0/T}{(1 - 2T_0/T)(I_L - 0.5I_0)} \tag{3.13}$$

A comment raised here is that when the same analytical procedures are applied to the conventional Z-source inverter, the same governing equation listed in (3.13) is derived, although some intermediate mathematical expressions might be different. This is expected since the embedded concept does not alter the original characteristic features of a Z-source inverter, even though it favorably introduces source filtering and lower component stresses to the inverter.

3.3.2. Semiconductor Ratings

While describing the operational principles of the embedded inverters in the earlier two sections, an important feature emphasized is their unchanged dc-link electrical quantities, as compared with their conventional counterparts. That means if the conventional voltage-type and ISE Z-source inverters are considered, their dc-link voltage stresses experienced by switches remain the same, and given by the first expression in (2.6). Maximum current stresses experienced by the switches in both inverters are also the same, whose value is determined by considering the shoot-through state introduced by turning on two switches from a phase-leg.

Referring to their respective circuit diagrams drawn in Fig. 2.6(a), Fig. 3.5 and Fig. 3.7, the relevant current stress expression is derived as $i_i = 2i_L$, which means twice the current computed using (3.11). Proceeding next to consider the input diodes found in both inverters, it is again clear that they experience the same maximum voltage and current stresses given by $v_D = -V_{dc} / (1 - 2d_{ST})$ when in the shoot-through state and $i_D = 2i_L$ when in the non-shoot-through null state.

3.3.3. Waveform Qualities

Output waveform qualities of the proposed embedded Z-source inverters are not

expected to deviate greatly from their conventional counterparts. The same modulation schemes reviewed in Section 2.4 can be used for controlling both inverters with their current-type duals requiring only an additional set of digital logic for mapping out the appropriate CSI gating signals [71]. Since they use the same modulation method and assume the same switching state types, their waveform qualities should virtually be the same, as confirmed later in simulation.

3.3.4. Dynamic Responses

Dynamic response of the conventional Z-source inverter was earlier studied in [47], where it is explicitly proved that the conventional Z-source inverter is a non-minimum-phase (NMP) entity with a right-half-plane (RHP) zero. Being a NMP entity, the inverter output will initially move in the opposite direction towards that of reference change even though it would eventually catch up with the reference as time progresses. That means if a step increase in output reference is assumed, the inverter actual output will fall before rising some time later to catch up with the reference. This behavior is closely linked to two phenomena inherited by the conventional Z-source inverter, named as the dc and ac phenomena. The dc phenomenon is associated with the front-end Z-source impedance network, and is proved by performing small-signal analysis. Effects from this phenomenon are however small, and can generally be ignored, leaving only the ac phenomenon to consider.

For demonstrating the ac phenomenon, the example state variation drawn in Fig. 3.9 is considered, where a short null duration T_N is shown in order to maximize the inverter output, while keeping the semiconductor stresses near to the lowest [70],[77]. A step increase in output is next introduced by lengthening the shoot-through duration T_0, and shortening the active duration T_A accordingly. Lengthening of T_0 would raise the output voltage, but the boosting effect can only be felt after the elapse of a delay, during which the Z-source capacitors C_1 and C_2 are charging up to their new higher steady-state values. Shortening of T_A, on the other hand, would cause the inverter output voltage to fall instantaneously since it immediately causes a reduction in volt-sec average. The overall dynamic response would then be an initial drop in output voltage before it reverses and rises towards its new higher steady-state value.

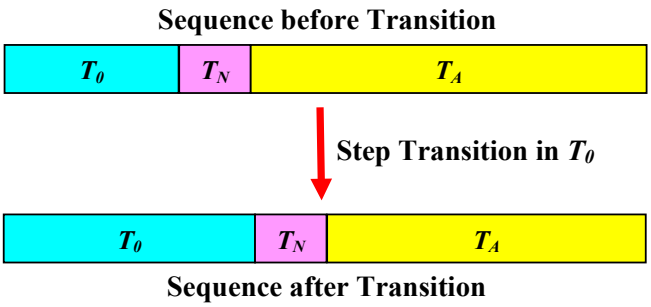


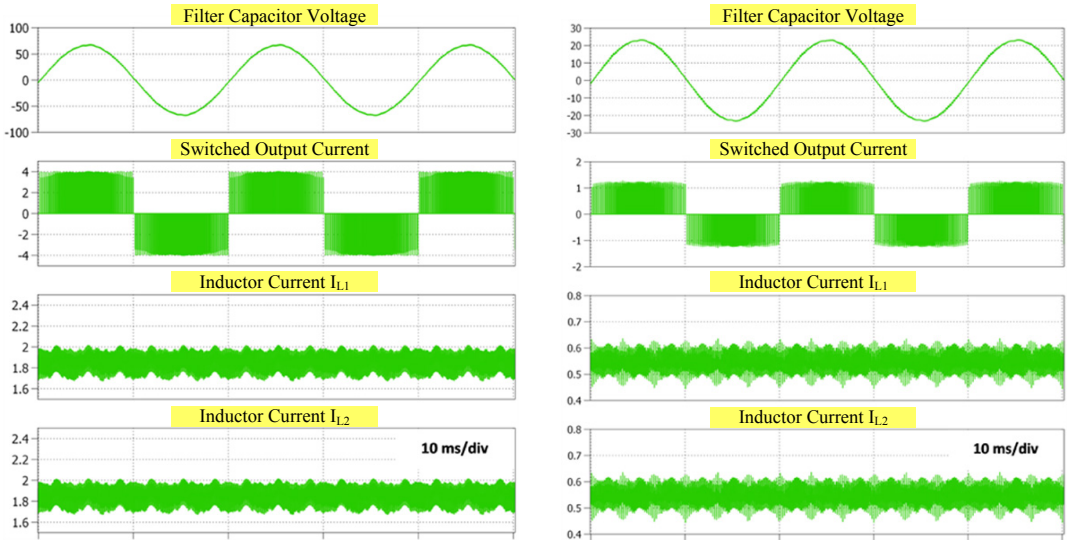
Fig. 3.9. Illustration of step increase in shoot-through time T_0 to raise the inverter output voltage.

The same dynamic phenomena are also experienced by the ISE Z-source inverters with their dc phenomenon again not expected to be prominent since they give rises to almost the same small-signal equations as their conventional counterparts. At their ac rear end, the same non-shoot-through and shoot-through state types are again used, which mean the earlier description related to Fig. 3.9 is equally applicable here for the ISE inverters. The ISE inverters are therefore NMP entities too with the same dynamic responses as the conventional Z-source inverter. This conclusion further strengthens the attractiveness of the ISE inverters since they are again proved to suffer no performance degradation even with new advantages introduced.

3.4. Simulation and Experimental Results

The proposed topologies were initially verified using the PLECS libraries coupled to the Matlab/Simulink platform, before experimental testing was performed on the asymmetrical and symmetrical ISE inverters. For the first set of simulations performed with the CSE inverters, its input voltage was set to V_{dc} = 60 V, and its impedance network was assembled using $L_1 = L_2 = 10$ mH and $C_1 = C_2 = 15$ μF. As understood from Section 3.3.1, the larger inductance was chosen mainly to bias the network more towards the current-source nature before it was eventually cascaded with a rear-end CSI bridge operating at 5 kHz. The capacitance, on the other hand, was chosen based on sizing details discussed in Section 3.3.1, whose main objective is to keep the inverters away from those unwanted operating modes described in [75].

Beginning by setting the control parameters to M = 0.6×1.15 and d_{ST} = 0, the symmetrical CSE inverter was initially programmed to operate in the voltage-boost



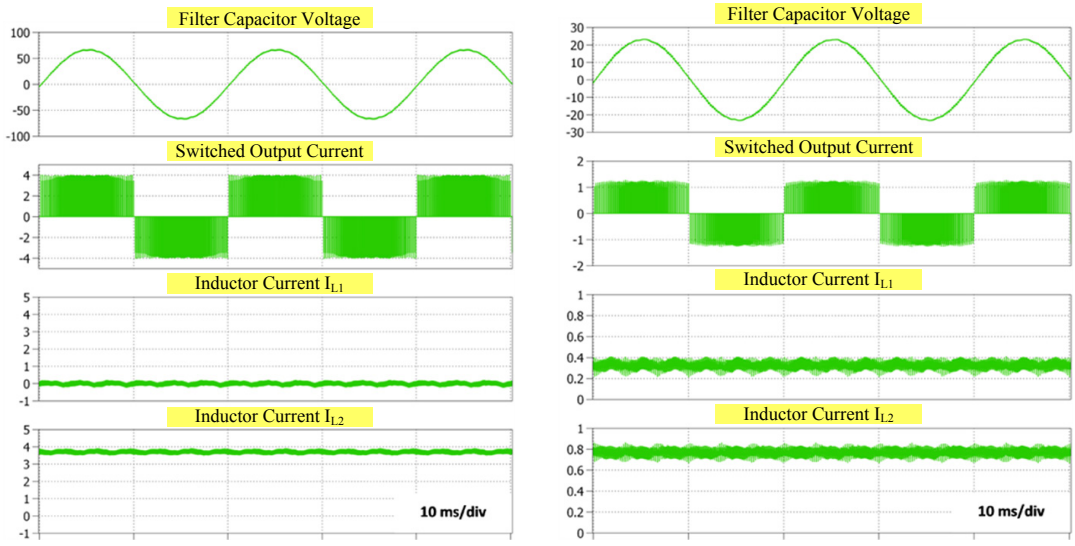
(a) (b)

Fig. 3.10. Simulated filter capacitor voltage, switched current, L_1 current, and L_2 current of the symmetrical CSE inverter with (a) $M = 0.6\times1.15$ and $d_{ST} = 0$, and (b) $M = 0.7\times1.15$ and $d_{ST} = 0.3$.

mode, whose captured results are shown in Fig. 3.10(a). As expected, the peak ac voltage is boosted to 75 V, which is higher than the maximum of $1.15\times V_{dc}/2 = 34.5$ V that can be produced by a conventional VSI. Re-setting the control parameters to $M = 0.7\times1.15$ and $d_{ST} = 0.3$ for voltage-buck operation, Fig. 3.10(b) shows the simulated waveforms, where the peak ac voltage of 23.5 V is noted to be lower than the benchmark of 34.5 V set by the conventional VSI.

The same sets of results were re-simulated and presented in Fig. 3.11 after one of the dc sources was removed to realize the asymmetrical CSE inverter. As observed, the peak ac voltage of the asymmetrical inverter is boosted to 75 V during current-buck mode and lowered to 23.5V during current-boost mode, which are both the same as the symmetrical circuit. The only difference noted are the unequal inductive currents flowing through the two Z-source inductors of the asymmetrical inverter, as compared with the equalized inductive currents flowing in the symmetrical inverter.

Similar to the CSE inverters, the validity of the ISE inverters was verified in simulation before a hardware platform was constructed for testing them in the laboratory. Parameters used for the simulations and experiments were the same and summarized as $V_{dc} = 60$ V, $L_1 = L_2 = 2$ mH, $C_1 = C_2 = 2200$ μF, $R_{Load} = 30$ Ω and $L_{Load} = 5$ mH. The last



(a) (b)

Fig. 3.11. Simulated filter capacitor voltage, switched current, L_1 current, and L_2 current of the asymmetrical CSE inverter with (a) $M = 0.6 \times 1.15$ and $d_{ST} = 0$, and (b) $M = 0.7 \times 1.15$ and $d_{ST} = 0.3$.

two parameters were for the external ac load. Here, the capacitance was sized larger mainly to bias the impedance network more towards the voltage-source nature before connecting it to the rear-end VSI bridge, as suggested in Section 3.3.1. The inductance, on the other hand, was chosen to meet the current ripple constraint needed to keep the inverters away from those unwanted operating modes discussed in [75].

A further comment shared here is that although the sizing calculations were performed to find the optimal or minimum *LC* values, the real values tested were not the minimum because of financial and other operating constraints imposed on the laboratory. They were therefore chosen among existing components that could best meet the computed optimum. The power stage was next interfaced to a modulator board built using simple *LF444* op-amp and *LM311* comparator chips. The modulator received its references and carrier from a combination of digital signal processor and digital-to-analog signal converters. The modulator outputs directly fed a driver board with six *IR2183* chips needed to produce six independent gating commands for driving the VSI bridge with shoot-through states inserted.

The assembled setup was eventually tested and found to produce results that match closely with those obtained from simulation. Because of their close similarities and nearly the same information conveyed, only the experimental results are discussed here

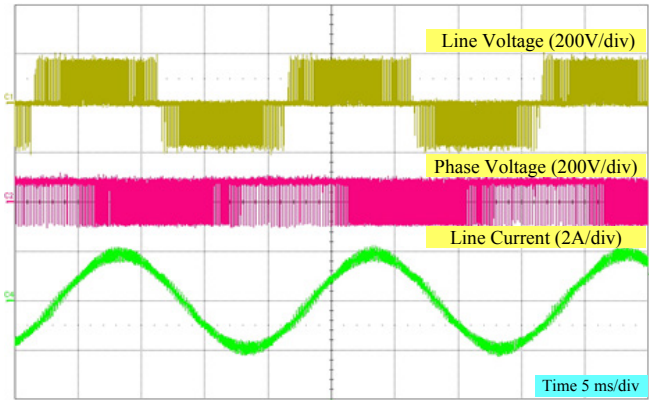


Fig. 3.12. Experimental line voltage, phase voltage, and line current of symmetrical ISE inverter with $M = 0.7 \times 1.15$ and $d_{ST} = 0.3$

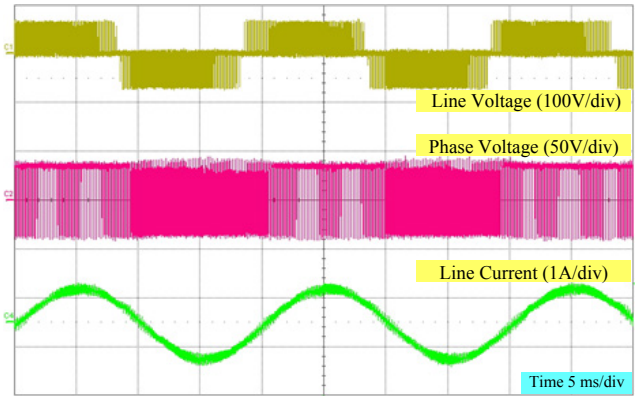


Fig. 3.13. Experimental line voltage, phase voltage, and line current of symmetrical ISE inverter with $M = 0.7 \times 1.15$ and $d_{ST} = 0$

to avoid duplication. Starting with the symmetrical configuration, Fig. 3.12 and Fig. 3.13 show the recorded experimental results for $M = 0.7 \times 1.15$ and $d_{ST} = 0.3$, and $M = 0.7 \times 1.15$ and $d_{ST} = 0$, respectively. The former represents voltage-boost operation with its dc-link voltage, reflected by the line voltage pulse height, raised to ≈170 V. The latter, on the other hand, represents voltage-buck operation with its dc-link voltage kept at the input value of 60 V. With shoot-through inserted, relevant ac quantities should also be boosted by 2.5 times (= 1 / (1 – 2 × 0.3)) for the same M, which indeed is the case reflected by dividing the peak ac current in Fig. 3.12 with that in Fig. 3.13 (1.8 / 0.7 = 2.6).

Repeating the experiment with one dc source removed, Fig. 3.14 and Fig. 3.15 show the recorded results for the asymmetrical ISE inverter with the same voltage buck and boost conclusions drawn. The only atypical feature noted in these figures is the positively offset phase voltage, measured between the output terminal of a phase-leg and cathode

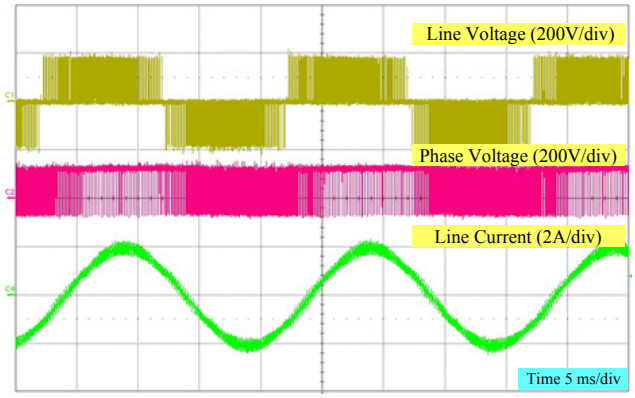


Fig. 3.14. Experimental line voltage, phase voltage, and line current of asymmetrical ISE inverter with $M = 0.7 \times 1.15$ and $d_{ST} = 0.3$

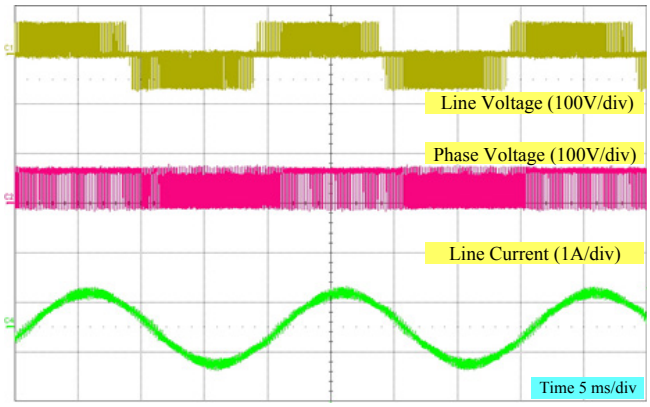


Fig. 3.15. Experimental line voltage, phase voltage, and line current of asymmetrical ISE inverter with $M = 0.7 \times 1.15$ and $d_{ST} = 0$

of input diode D in Fig. 3.5. This positive offset is caused by the unequal voltages appearing across the two Z-source capacitors, which in fact correspond to the positive and negative amplitudes of the observed phase-leg voltage.

To better illustrate this unbalance, Fig. 3.16 and Fig. 3.17 show the dc voltages measured across the two Z-source capacitors and currents flowing through the corresponding inductors of the symmetrical and asymmetrical ISE inverters, respectively. Electrical quantities of the former are clearly balanced within the X-shaped impedance network, but not for the latter. Despite this difference, ac loads connected to the inverter outputs still receive the same supply quality. That means the best topology to adopt is solely decided by the availability of the second dc source.

Moving on to verify those additional features discussed in Section 3.3, Fig. 3.18 shows the normalized spectral plots of a conventional Z-source inverter, an ISE inverter and a

CSE inverter, which unquestionably are similar. This is expected since the inverters were controlled by the same modulation scheme, and the added mapping logic for the CSE inverter is not expected to alter its spectral characteristics. Dynamic responses of the inverters were also tested by initiating a step transition of the output command at the indicated time instant shown in Fig. 3.19. In that figure, the three-phase currents of both the conventional and ISE Z-source inverters are chosen for illustrating the NMP responses simply because they are smoothed, and therefore will show the initial drops in values more distinctly. The currents will eventually rise to their new steady-state values as time progresses. The plotting of smoothed ac voltages for the conventional current-type and CSE Z-source inverters can also be attempted, but their results are not expected to convey any new information. Because of that, the time-varying voltage plots are not included here for conciseness without compromising quality.

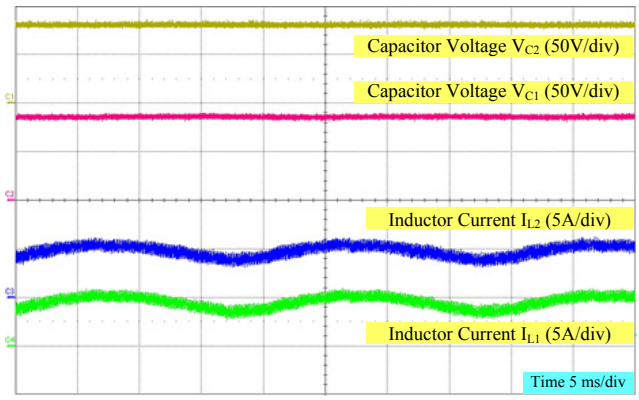


Fig. 3.16: Experimental voltages across C_2 and C_1, and current through L_2 and L_1 of symmetrical ISE inverter with $M = 0.7 \times 1.15$ and $d_{ST} = 0.3$

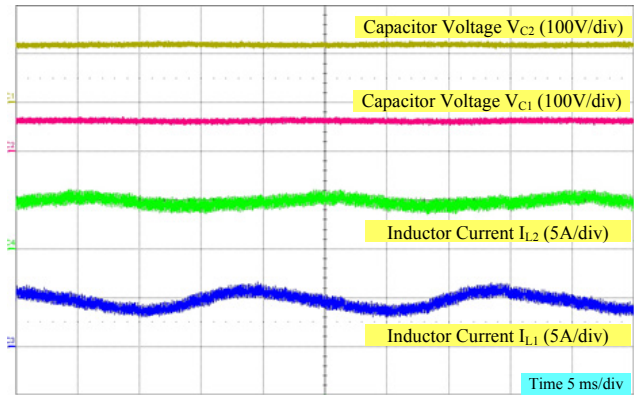
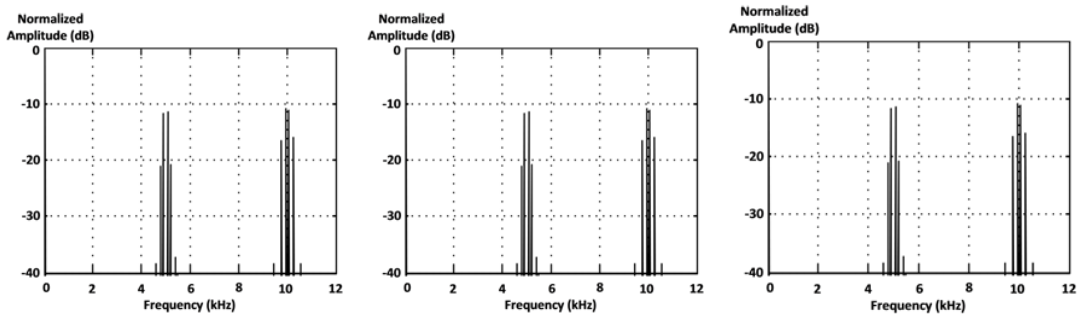


Fig. 3.17: Experimental voltages across C_2 and C_1, and current through L_2 and L_1 of asymmetrical ISE inverter with $M = 0.7 \times 1.15$ and $d_{ST} = 0.3$



(a) (b) (c)

Fig. 3.18. Normalized spectra of (a) traditional voltage-type, (b) ISE and (c) CSE Z-source inverters with $M = 0.7 \times 1.15$ and $d_{ST} = 0.3$.

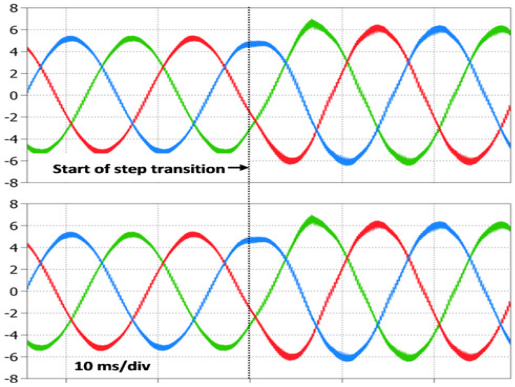


Fig. 3.19. Simulated three-phase output currents of traditional voltage-type (upper) and ISE (lower) Z-source inverters when d_{ST} changes from 0.1 to 0.2 with the normalized null interval kept constant at 0.2.

3.5. Summary

Four embedded Z-source inverters with either asymmetrical or symmetrical impedance networks are studied. Unlike their traditional counterparts, these inverters have their dc sources embedded within their impedance networks to gain advantages like implicit source filtering without additional hardware and lower component stresses. These features are no doubt attractive given also that voltage gains and spectral performances of the inverters remain unchanged. The proposed inverters are therefore competitive alternatives, whose performance characteristics have already been tabulated in TABLE 3.1 for comparison with their traditional precedence.

Before ending this section, it is also important to mention here that the same embedded

inverters have been studied in [19] at about the same time, but named differently as the quasi-Z-source inverters. Although drawn differently too, embedded and quasi-Z-source inverters are fundamentally similar, and should therefore not be distinguished in this thesis.

TABLE 3.1 TOPOLOGICAL AND PERFORMANCE FEATURES OF TRADITIONAL, CSE AND ISE Z-SOURCE INVERTERS

	Z-source Inverter Types		
	Traditional	**CSE**	**ISE**
Inverter bridge types	Voltage or current-type	Current-type	Voltage-type
Implicit source filtering	**No** Chopping source current during voltage-boosting unless filtered by external filter	**Yes** Additional L_f needed for realizing current source	**Yes** Filtering provided by existing Z-source inductors
Source voltage and current expressions	***Voltage-type*** 1 unit of V_{dc} $2i_L$ - i_i in active state $2i_L$ in null state 0 in shoot-through state ***Current-type*** 1 unit of I_{dc} $2V_C$ - v_i in active state $2V_C$ in null state 0 in open-circuit state	1 unit of I_{dc} for asymmetrical OR 2 units of $I_{dc}/2$ for symmetrical AND V_C for both asymmetrical and symmetrical	1 unit of V_{dc} for asymmetrical OR 2 units of $V_{dc}/2$ for symmetrical AND i_L for both asymmetrical and symmetrical
DC-link voltage or current gain	$\hat{v}_i = \frac{1}{1-2T_0/T} \cdot V_{dc}$	$\hat{i}_i = \frac{1}{1-2T_0/T} \cdot I_{dc}$	$\hat{v}_i = \frac{1}{1-2T_0/T} \cdot V_{dc}$
AC voltage or current gain	$\hat{v}_{ac} = \frac{0.5M}{1-2T_0/T} \cdot V_{dc}$	$\hat{i}_{ac} = \frac{M}{1-2T_0/T} \cdot I_{dc}$	$\hat{v}_{ac} = \frac{0.5M}{1-2T_0/T} \cdot V_{dc}$

Chapter 4 Enhanced Z-source Inverters – Cascading Techniques

Modern power electronic applications usually demand some amount of voltage-boosting, especially those directly connected to the grid like in most renewable energy systems. For the case of PV systems, higher voltage boost avoids series connecting of large number of PV panels, which then minimizes partial shading. It is also mentioned in [24] that inverters with boost functionality has a better ability to track the maximum power point, especially during low irradiation and partially shaded conditions Traditional VSIs are therefore not suitable since they can only step down voltages.. To introduce the required voltage boost, single-stage buck-boost inverters are recommended [75][79], where Z-source inverters are presently among the popular few [45]. Existing Z-source inverters are however burdened by some disadvantages like poorer spectral performance and higher component stresses mainly linked to their low modulation ratios at high voltage or current gains.

To resolve the limitation, two cascading techniques are proposed and named as the alternate cascading and dc-link cascading methods. Before cascading can be done, two generalized impedance networks must be developed and duplicated. Upon cascaded accordingly, the inverters thus formed would have higher voltage gains and other unique advantages linked to high modulation ratios. Simulation and experimental testing have already been performed with captured results confirming the claimed advantages.

4.1. Hybrid-Source Impedance Networks

The purpose of this section is to group existing impedance networks used by various Z-source inverters together before proposing generalized network entities that can be used to represent them. Focus would first be given to the voltage-type inverters before diverting to their current-type duals.

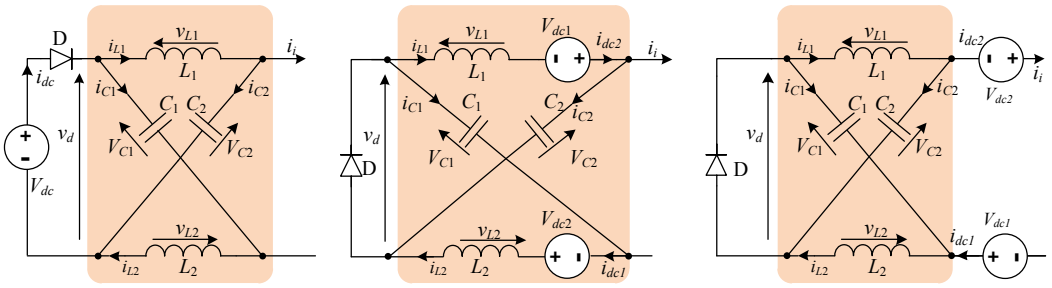


Fig. 4.1. Impedance networks used in (a) traditional, (b) embedded and (c) dc-link embedded Z-source inverters.

4.1.1. Voltage-Type Impedance Networks

Fig. 4.1 shows three impedance networks that have earlier been used for the conventional, embedded and dc-link embedded voltage-type Z-source inverters with the same voltage gains produced [86]. The first two networks have already been studied in Section 2.3.1 and Chapter 3, while the third network was explicitly mentioned in three references [86][88][89] at about the same time. The third network does not solve the issue of chopping source current like in the conventional Z-source inverter, but it produces the lowest capacitor voltages among the three possibilities. It can therefore be an attractive option for certain applications, and should rightfully be considered hereon.

Note also that two sources are explicitly shown with the last two networks, which certainly have the advantage of creating a symmetrical network for reducing common and differential mode noises. Their simultaneous presence is however not necessary, meaning that only one of them needs to be there with no drop in voltage gain expected [87]. The only difference comes from the second network, where omission of one source gives rise to asymmetrical voltage and current sharing among the capacitive and inductive elements, even if their values are selected to be the same ($L_1 = L_2 = L$ and $C_1 = C_2 = C$). This concern has already been discussed in Chapter 3. Regarding sources, a closer view at the networks also reveals that they differ only in their source placements with the locations indicated in Fig. 4.1(b) having the best internal filtering and those in

Fig. 4.1(c) having the lowest capacitive voltages.

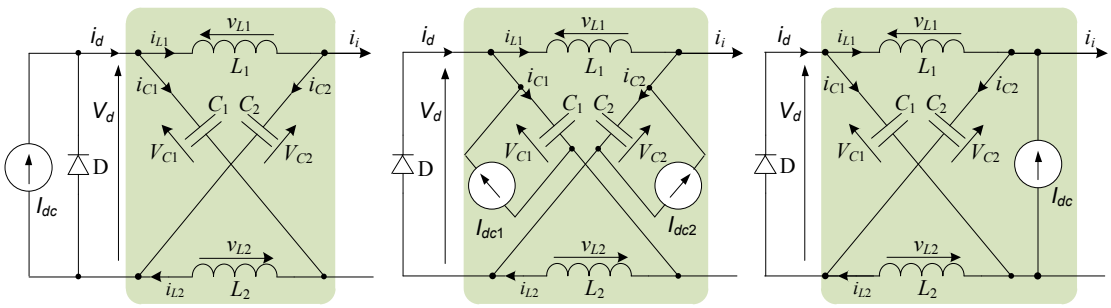
4.1.2. Current-Type Impedance Networks

Quite expectedly, current-type duals of those networks shown in Fig. 4.1 exist, and are drawn in Fig. 4.2 for realizing conventional, embedded and dc-link embedded current-type Z-source inverters. Note again that although two sources are explicitly drawn in Fig. 4.2(b) and (c), only one of them needs to be there to gain filtering and stress reduction benefits with no drop in current gain expected. Omission of one source for the network in Fig. 4.2(b) would however lead to asymmetrical voltage and current sharing among the components, even if their values are symmetrical ($L_1 = L_2 = L$ and $C_1 = C_2 = C$).

4.1.3. Hybrid-Source Impedance Networks

Upon understanding their characteristic differences, an attempt to merge the three voltage-type impedance networks leads to the generic network entity shown in Fig. 4.3(a). Being a merged entity, the network in Fig. 4.3(a) can obviously be used for constructing any hybrid combinations of traditional, embedded and dc-link embedded Z-source inverters with the same usual operating states, discussed as follows:

Shoot-Through: Introduced by turning on two switches from at least a phase-leg of the VSI bridge. While doing so, the far-left diode *D* blocks, giving rise to the inductive voltage expression of $v_L = V_C + 0.5V_{dc2} + V_{dc3}$.



(a) (b) (c)

Fig. 4.2. Impedance networks used in (a) traditional, (b) embedded and (c) dc-link embedded current-type Z-source inverters.

Non-Shoot-Through: Referred to any of the eight traditional active and null states of a VSI. In this state, diode *D* conducts, leading to $v_L = V_{dc1} + 0.5V_{dc2} - V_C$.

Averaging v_L over a switching period and equating it to zero then give rise to the following expressions for computing the network capacitive voltage V_C, peak dc-link voltage $\hat{v}_i$ and peak ac output voltage $\hat{v}_{ac}$ in terms of the source voltages V_{dc1}, V_{dc2} and V_{dc3} [95]:

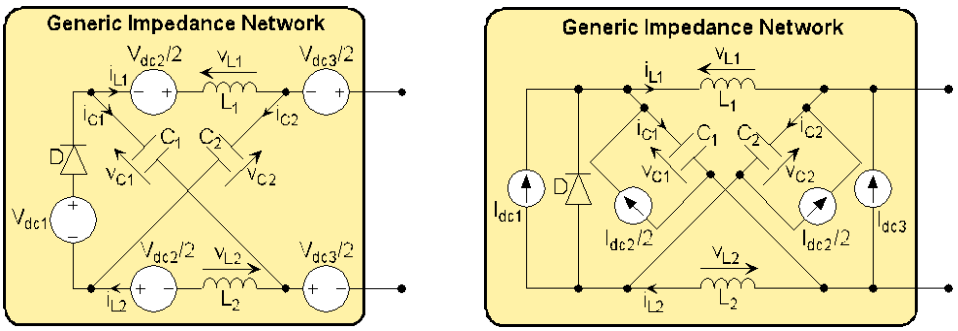
$$V_C = \frac{1-d_{ST}}{1-2d_{ST}}V_{dc1} + \frac{0.5}{1-2d_{ST}}V_{dc2} + \frac{d_{ST}}{1-2d_{ST}}V_{dc3}$$

$$\hat{v}_i = \frac{1}{1-2d_{ST}}(V_{dc1} + V_{dc2} + V_{dc3})$$

$$\hat{v}_{ac} = \frac{0.5M}{1-2d_{ST}}(V_{dc1} + V_{dc2} + V_{dc3}) \qquad (4.1)$$

Being generic, (4.1) can be simplified to those gain expressions governing conventional, embedded and dc-link embedded Z-source inverters, after setting (V_{dc2}, V_{dc3}), (V_{dc1}, V_{dc3}) and (V_{dc1}, V_{dc2}) to zero, respectively. These cases represent only three sub-cases with source placement at only one location each. Other cases with two or more sources placed at different locations are possible, but will not be explicitly discussed here because of their straightforwardness.

Other than the voltage-type generalized network shown in Fig. 4.3(a), the dual



(a) (b)

Fig. 4.3. Generic network entities for implementing (a) voltage-type and (b) current-type hybrid-source inverters.

current-type network can similarly be derived by merging the conventional, embedded and dc-link embedded Z-source networks discussed in [86][88]. The resulting generalized current-type network is shown in Fig. 4.3(b), where again three distinct locations for source placement are possible. Inverters thus formed can then assume the following two operating states, defined as:

Open-Circuit: Introduced by turning off all switches of the CSI bridge. Diode *D* then conducts naturally, giving rise to $i_C = 0.5I_{dc2} + I_{dc3} + I_L$.

Non-Open-Circuit: Referred to any of the nine traditional active and null states of a CSI. In this state, diode *D* reverse biases naturally, giving rise to $i_C = I_{dc1} + 0.5I_{dc2} - I_L$.

Averaging the capacitive current to zero per switching cycle then results in the following generic set of equations for expressing the network inductive current I_L, peak dc-link current $\hat{\imath}_i$ and peak ac output current $\hat{\imath}_{ac}$ in terms of the three input currents of I_{dc1}, I_{dc2} and I_{dc3} [95]:

$$I_L = \frac{1-d_{OC}}{1-2d_{OC}} I_{dc1} + \frac{0.5}{1-2d_{OC}} I_{dc2} + \frac{d_{OC}}{1-2d_{OC}} I_{dc3}$$
$$\hat{\imath}_i = \frac{1}{1-2d_{OC}} (I_{dc1} + I_{dc2} + I_{dc3})$$
$$\hat{\imath}_{ac} = \frac{M}{1-2d_{OC}} (I_{dc1} + I_{dc2} + I_{dc3}) \quad (4.2)$$

4.2. Generalized Cascading Techniques

Two methods of cascading multiple hybrid-source networks are now discussed with their relevant ac voltage gain expressions derived, and advantages and disadvantages stated.

4.2.1. Alternate-Cascading Method (Voltage-Type Networks)

The simplest and most direct way of cascading *N* voltage-type networks is shown in Fig.

4.4 for the example case of $N = 2$. The resulting output voltage is expected to double, but that is more because the input voltages have doubled through cascading two similar copies of the network drawn in Fig. 4.3(a). The voltage gains are still the same with the governing expressions written in (4.3), after setting $N = 2$ for the example considered in Fig. 4.4. Equation (4.3) clearly resembles (4.1), which is expected based on the explanation described earlier. The direct series-cascading technique is therefore not a favorably recommended approach since it does not introduce any new advantages to the circuit.

$$V_C = \frac{1-d_{ST}}{1-2d_{ST}} V_{dc1} + \frac{0.5}{1-2d_{ST}} V_{dc2} + \frac{d_{ST}}{1-2d_{ST}} V_{dc3}$$

$$\hat{v}_i = \frac{1}{1-2d_{ST}} V_{dc\_Tot}; \qquad \hat{v}_{ac} = \frac{0.5M}{1-2d_{ST}} V_{dc\_Tot}$$

$$V_{dc\_Tot} = N(V_{dc1} + V_{dc2} + V_{dc3}) \tag{4.3}$$

Recommending an alternative approach, the conceptually less obvious alternate-cascading method is introduced here using the example illustration drawn in Fig. 4.5 for the case of $N = 2$. To arrive at the configuration drawn in Fig. 4.5, network 2 is first flipped horizontally with respect to network 1. That results in voltages and

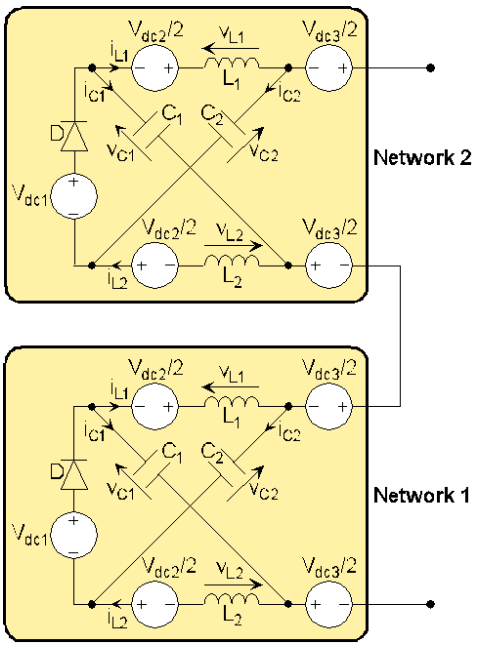


Fig. 4.4. Direct-cascading of two hybrid-source network entities.

currents of its lower inductive branch $H_{2(2)}$ to now point in the same directions as those of the upper inductive branch $H_{1(1)}$ of network 1. Wiring them in shunt by adding the two indicated (dotted) lines will then not affect the circuit, but would allow one of the branches to be removed, which for the example shown in Fig. 4.5, it is assumed to be $H_{2(2)}$. Removing $H_{2(2)}$ will not affect the remaining $H_{1(1)}$ branch, as can be proved by re-performing simple averaging and state analyses with the remaining three inductive branches still chosen to have the same inductance.

The alternate-cascaded network formed would still produce the same shoot-through and non-shoot-through states with their inductive voltages summarized as:

Shoot-Through: Diodes D reverse-bias, and hence giving rise to $v_L = 2V_C + 2V_{dc2}/3 + 2V_{dc3}$.

Non-Shoot-Through: Diodes D forward-bias, and hence giving rise to $v_L = V_{dc1} + 2V_{dc2}/3 - V_C$.

The voltage expressions of interest are then derived as:

$$V_C = \frac{1-d_{ST}}{1-3d_{ST}} V_{dc1} + \frac{2}{3(1-3d_{ST})} V_{dc2} + \frac{2d_{ST}}{1-3d_{ST}} V_{dc3}$$
$$\hat{v}_i = \frac{2}{1-3d_{ST}} (V_{dc1} + V_{dc2} + V_{dc3})$$
$$\hat{v}_{ac} = \frac{M}{1-3d_{ST}} (V_{dc1} + V_{dc2} + V_{dc3}) \quad (4.4)$$

where it is clearly seen that the input-to-output voltage gain of the alternate-cascading method is much higher than that of the direct-cascading method ($M/(1-3d_{ST})$ for the former versus $M/(1-2d_{ST})$ for the latter), while yet using one lesser inductive branch.

Note also that while the network in Fig. 4.5 is still drawn with multiple sources, they can in principle be set to zero as per discussed earlier, but surely, at least one of them must

remain to power the cascaded network. The upper and lower dc-link terminals of the network can then be connected to a two-level VSI bridge, whose functionality is again to commutate the inverter between shoot-through and non-shoot-through states. As per its single-network precedence discussed in Section 4.1.1, the added VSI bridge alone does not provide independent control flexibility to each of the sources, unless additional control mechanisms are implemented within them.

Applying the same concept to the generalized case of cascading N basic networks further results in the topology shown in Fig. 4.6, where all even numbered entities are horizontally flipped with reference to their odd-numbered counterparts. One inductive branch is then removed from each pair of adjacently numbered networks to arrive at the final expanded LC network drawn in Fig. 4.6. That alternate-cascaded network uses N – 1 lesser inductors, as compared to the structure obtained by direct-cascading. Generalized expressions for relating V_C, $\hat{v}_i$ and $\hat{v}_{ac}$ to the three input voltages of V_{dc1}, V_{dc2} and V_{dc3} for the alternate-cascaded network can also be derived as (4.5), which certainly is much higher in gain than the direct-cascading method represented by (4.3).

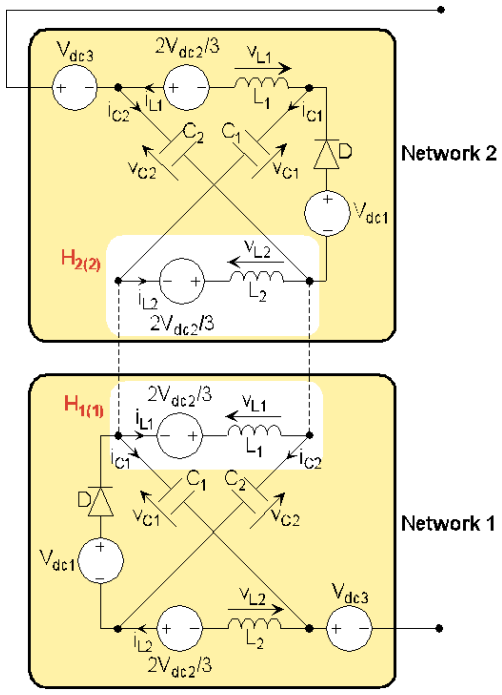


Fig. 4.5. Alternate-cascading of two hybrid-source network entities.

$$V_C = \frac{1-d_{ST}}{1-(N+1)d_{ST}} V_{dc1} + \frac{N/(N+1)}{1-(N+1)d_{ST}} V_{dc2} + \frac{N d_{ST}}{1-(N+1)d_{ST}} V_{dc3}$$

$$\hat{v}_i = \frac{1}{1-(N+1)d_{ST}} V_{dc\_Tot}$$

$$\hat{v}_{ac} = \frac{0.5M}{1-(N+1)d_{ST}} V_{dc\_Tot} \qquad (4.5)$$

Moreover, the denominator of (4.5) indicates that the maximum gain of the alternate-cascaded network arrives earlier at $d_{ST} = 1 / (N + 1)$, rather than at 0.5 for the direct-cascading method. A smaller d_{ST} allows a larger M to be set for overall improvement in output waveform quality, as also experienced by the traditional VSI. There however is a limit for M defined as $1.15 \times (1 - d_{ST})$. These accompanied

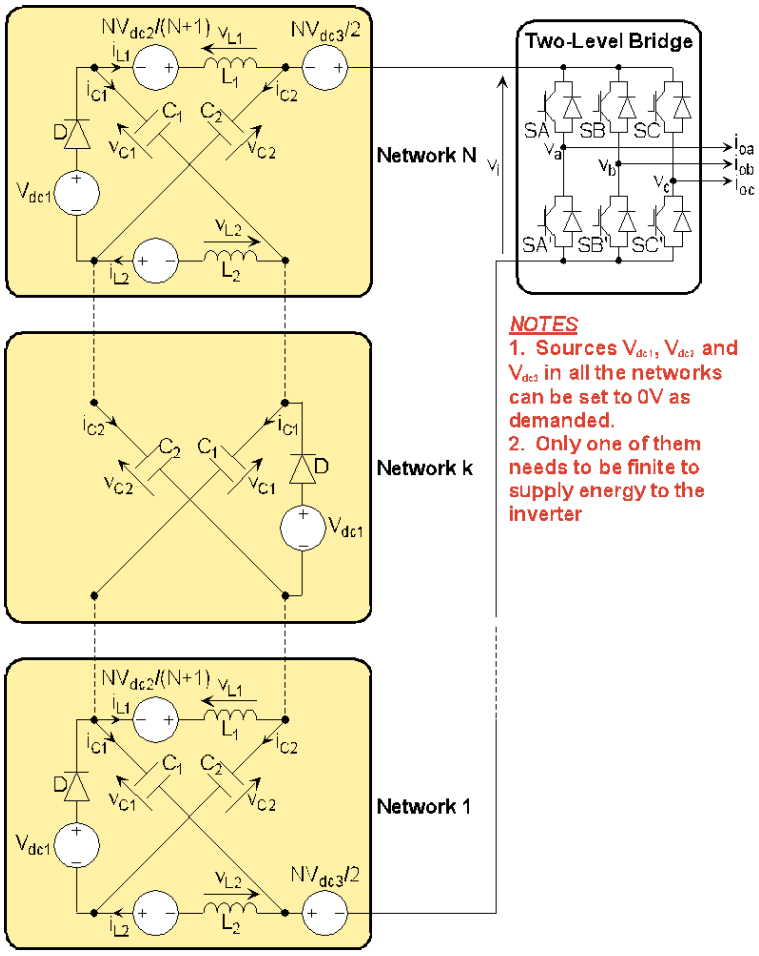


Fig. 4.6. Two-level hybrid-source inverter formed by alternate-cascading of impedance networks.

advantages, together with the lower number of inductive elements needed, definitely will strengthen the attractiveness of the alternate-cascading method.

While producing the desired voltage boosting, it is equally of concern to investigate on the dc side current, since it is expected to be much larger than the ac load current. An expression relating them can easily be derived by balancing power flows on the dc and ac sides, and noting that average currents flowing through all sources and inductors in the Z-source networks are equal. Doing so then results in:

$$I_L = \frac{3}{2}\left(\frac{\hat{v}_{ac}}{V_{dc\_Tot}}\right)\hat{\imath}_{ac}cos\varphi = \frac{3}{4}\left(\frac{M}{1-(N+1)T_0/T}\right)\hat{\imath}_{ac}cos\varphi \qquad (4.6)$$

where I_L is the common inductor current, $\hat{\imath}_{ac}$ is the peak ac load current, and cosφ is the load power factor. Using (4.6) and noting that all diodes D reverse-biased when in a shoot-through state, the corresponding shoot-through current flowing through the inverter phase-legs is deduced as $I_{ST} = (N + 1)\, I_L$, which must surely be considered when selecting the appropriate semiconductor ratings.

4.2.2. DC-Link-Cascading Method (Voltage-Type Networks)

Another cascading method is illustrated in Fig. 4.7, where $N - 1$ additional capacitors and $2(N - 1)$ additional diodes are used for connecting N impedance networks together at their respective dc-links. Of the N networks considered, only network 1 can take the generalized form drawn in Fig. 4.3(a), inferring that it can freely be configured to any of the three existing networks (traditional, embedded and dc-link embedded) or any hybrid combination of them. For the remaining $N - 1$ networks, they must strictly be of the dc-link embedded type with V_{dc1} and V_{dc2} set to zero, because of reasons that would be obvious shortly. The third sources V_{dc3} in those networks are not zero, but rather replaced by capacitors C_k (k = 2 to N), whose voltage values are shown later to depend on the shoot-through duration and network index ranging from 2 to N.

The N networks are then cascaded together at their dc-links by using $2(N-1)$ diodes, divided into two groups, and labeled as $D1$ and $D2$ respectively. These added diodes allow the inverter to still enter the shoot-through and non-shoot-through states, whose operating features are summarized as follows:

Shoot-Through: Triggered by shorting at least one phase-leg, which in turn causes diodes D and $D2$ to turn off naturally, and hence isolating the N impedance networks. At the same time, diodes $D1$ conduct to short the positive terminals of all networks to the

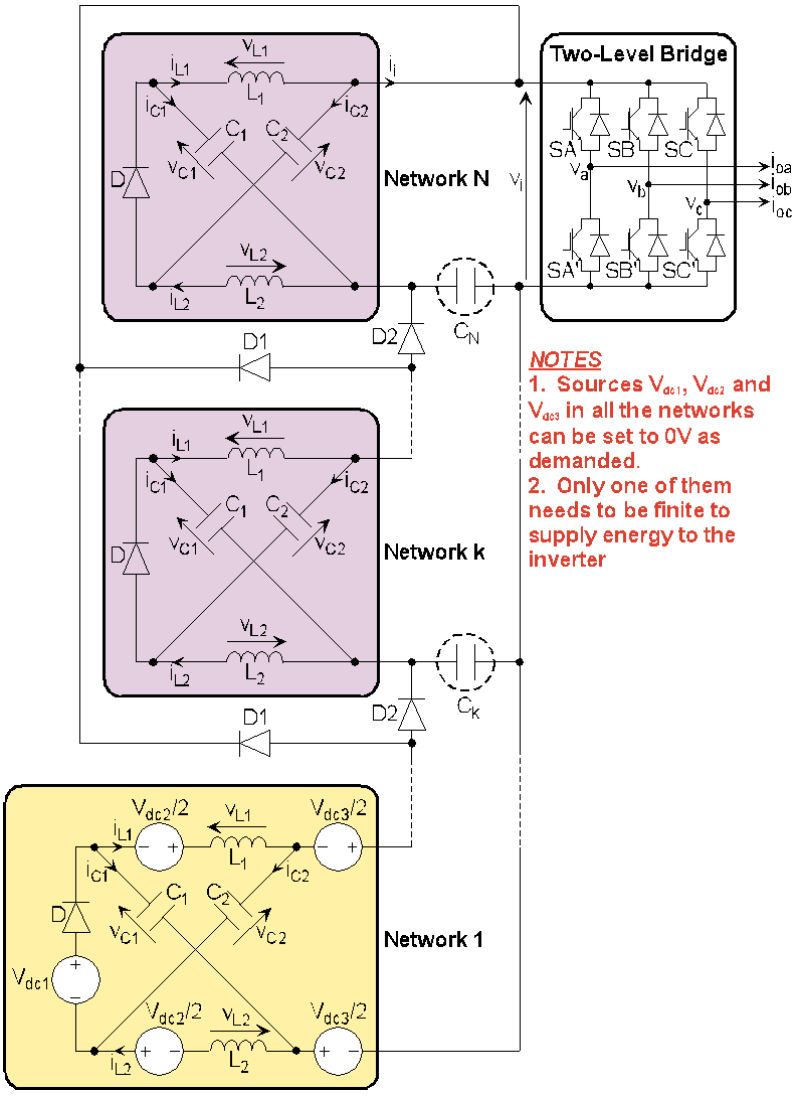


Fig. 4.7. Two-level hybrid-source inverter formed by dc-link-cascading of impedance networks.

negative dc rail of the rear-end VSI bridge.

Non-Shoot-Through: Diodes *D1* block naturally, while diodes *D2* and *D* conduct to tie all C_k together with one series impedance network inserted in between any two adjacent capacitors.

Averaging the two states then gives rise to the following mathematical expressions for computing voltage V_{C_k} across C_k, V_C within the k^{th} network powered by C_k, peak dc-link $\hat{v}_i$ and ac output $\hat{v}_{ac}$ voltages. Note that these equations are obtained with the total input source voltage scaled upwards to V_{dc_Tot} for easier comparison purposes.

$$V_{C_k} = \frac{1}{(1-2d_{ST})^{k-1}} V_{dc\_Tot}$$

$$V_C = \frac{d_{ST}}{(1-2d_{ST})^{k}} V_{dc\_Tot}$$

$$\hat{v}_i = \frac{1}{(1-2d_{ST})^{N}} V_{dc\_Tot}$$

$$\hat{v}_{ac} = \frac{0.5M}{(1-2d_{ST})^{N}} V_{dc\_Tot} \qquad (4.7)$$

The denominator of $\hat{v}_{ac}$ in (4.7) is clearly raised to the power of *N*, which upon inverted, will give rise to a much higher voltage gain than that obtained by the direct-cascading method. But unlike the alternate-cascading method whose maximum gain is reached earlier when d_{ST} increases to 1 / (*N* + 1), the dc-link cascading method reaches its maximum voltage gain only when d_{ST} further increases to 0.5. The operating ranges of *M* and d_{ST} of the dc-link-cascading method are therefore no different from those of the direct-cascading method, even though its voltage gain is much higher. The higher gain would however lead to much larger current flow on the dc side since power is conserved throughout the circuit if parasitic losses are neglected. Based on this understanding, an expression for determining the inductor current flowing through each network (e.g. I_{Lk} in Network *k* of Fig. 4.7) can be determined, as follows.

$$I_{Lk} = \frac{3}{2}\left(\frac{\hat{v}_{ac}}{V_{dc\_Tot}}\right)(1-2d_{ST})^{k-1}\hat{\imath}_{ac}cos\varphi = \frac{3}{4}\left(\frac{M(1-2d_{ST})^{k-1}}{(1-2d_{ST})^{N}}\right)\hat{\imath}_{ac}cos\varphi \quad (4.8)$$

Using (4.8), shoot-through current I_{ST} flowing through the VSI phase-legs is follow-up determined as (4.9), whose value is helpful for semiconductor selection.

$$I_{ST} = 2\sum_{k=1}^{N} I_{LK} = 3\left(\frac{\hat{v}_{ac}}{V_{dc\_Tot}}\right)\left(\frac{1-(1-2d_{ST})^{N}}{2d_{ST}}\right)\hat{\imath}_{ac}cos\varphi = \frac{3M}{2}\left(\frac{1-(1-2d_{ST})^{N}}{(2d_{ST})(1-2d_{ST})^{N}}\right)\hat{\imath}_{ac}cos\varphi \quad (4.9)$$

4.2.3. Cascading Methods (Current-Type Networks)

A common feature noted with the above two proposed cascading methods is the introduction of some forms of shunt interfacing for connecting the *N* networks together. More specifically, shunt inductive interfacing has been introduced by the alternate-cascading method, while shunt shoot-through insertion has been introduced by the dc-link-cascading method. This understanding, when transferred to the dual current-type network shown in Fig. 4.3(b), means either series capacitive interfacing or series open-circuit insertion. Unfortunately, series capacitive interfacing and hence alternate-cascading do not appear to be feasible for the current-type network, and will therefore not be discussed further.

The second option of inserting series open-circuit states to the *N* current-type networks is conceptually realizable, but has to include additional active switches rather than diodes. For a quick visualization of how that can be done, the circuit in Fig. 4.7 can be modified with its rear end replaced by a CSI bridge, network 1 replaced by the generalized current-type network shown in Fig. 4.3(b), and C_k replaced by L_k. Diodes *D1* should then be removed, while diodes *D2* should be replaced by active switches. These switches are programmed to turn off when the rear-end CSI bridge enters its open-circuit state. Individual networks then enter their respective open-circuit states, causing the final ac output current to be boosted by $M/(1-2d_{OC})^{N}$, as intended.

Although realizable, this method of cascading networks is not economically favorable because of the additional switches and accompanied gate driving circuits needed. Cascading of current-type networks is therefore generally not recommended, even though still realizable by adopting the dc-link-cascading technique.

4.3. Extension to Three-Level Neutral-Point-Clamped Inverters

As noted from past literature, conventional, embedded and dc-link embedded Z-source inverters can be extended to their three-level variants with better output waveform quality and lower semiconductor stresses [86][90]. Similar extension is now tested with the cascading concepts to evaluate their feasibility. To do that, the main feature checked is the likelihood of forming three distinct, equally spaced dc voltage levels to which a three-level neutral-point-clamped (NPC) bridge [91]-[93] can be connected.

Beginning with the alternate-cascaded structure, a possible way of introducing the third neutral terminal between the already present positive and negative dc rails is to divide V_{dc1} of the middle network into two, and duplicate a copy of diode *D*. The neutral terminal can then be tapped from the midpoint of the divided V_{dc1}, as demonstrated in Fig. 4.8. Adopting this method also means that the number of networks *N* cascaded together must always be odd with the middle network notated as $k = (N + 1)/2$. The equally spaced dc potentials formed can then be tied to the rear-end NPC bridge, as demonstrated in Fig. 4.8. Modulation of this extended NPC inverter is no different from those discussed in [86][90] for the conventional, embedded and dc-link embedded Z-source inverters, even though its gain is higher for a specified shoot-through duration.

Considering now the dc-link-cascaded structure drawn in Fig. 4.7, the general judgment deduced is that it cannot be extended to include three-level switching because there is no easy way of introducing the centrally placed neutral potential. It is therefore not further considered, and the general conclusion drawn is that only the alternate-cascading

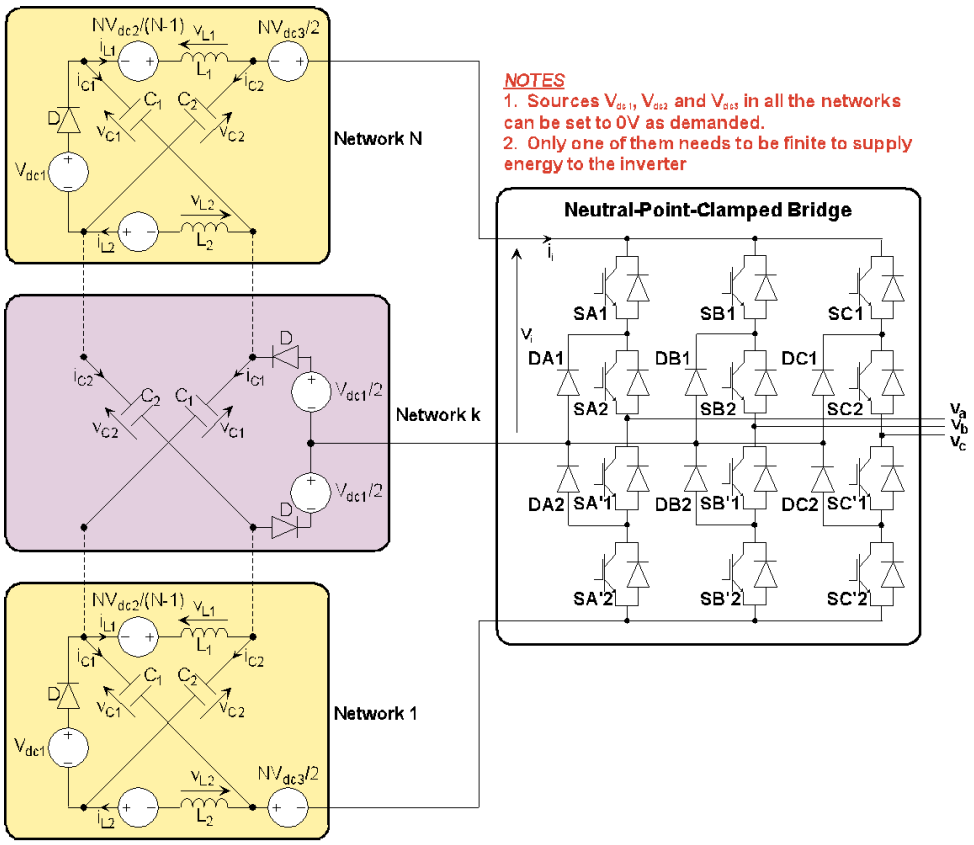


Fig. 4.8. Three-level hybrid-source inverter formed by alternate-cascading of impedance networks.

technique can be used for realizing three-level hybrid-source inverter with enhanced voltage boost.

4.4. Topological Comparison

At first sight, the proposed generalized cascaded inverters might not appear attractive because of their higher component counts on the dc side. Even with lesser inductors needed by the alternate-cascading method, the overall component count is still higher than that of the conventional Z-source inverter. This might not be avoidable if higher voltage boost without using a transformer is demanded. Despite that, the number of components added should still be kept minimal to keep the total cost and introduced parasitic low. The latter, if not reduced, will cause the obtainable gain to be much lower than its theoretical value, and hence defeating the purposes of cascading. The number of

networks to cascade is therefore a decision closely related to the materials available for realization, overall gain required and financial support awarded for the design.

To better help in making a sound decision, this section documents an elaborated comparison between the proposed cascading techniques and their single-network precedence. Comparison with the two-stage configuration formed by connecting an enhanced dc-dc boost converter to a rear-end inverter is also discussed since it is an approach that most professionals would prefer because of its simplicity and straightforwardness.

4.4.1. Single Network versus Multiple Networks

Besides providing high gain, the proposed generalized inverters might still have some convincing advantages over those existing Z-source inverters, when they are commanded to produce the same output voltage from the same given input voltage. Taking the example case of total input voltage set to NV_{dc3} with V_{dc1} and V_{dc2} set to zero, the relationship governing shoot-through duty ratios of the conventional and proposed inverters is derived as (4.10), after their input-to-output voltage gains are set equal with M set to $1.15 \times (1 - d_{ST})$. This condition of M would ensure that the gain is maximized, while the semiconductor stresses are minimized [86]-[88].

$$\frac{1-\delta_t}{1-2\delta_t} = \frac{1-\delta_{alt}}{1-(N+1)\delta_{altt}} = \frac{1-\delta_{dcl}}{(1-2\delta_{dcl})^N} \tag{4.10}$$

where δ is a more compact form for representing shoot-through duration d_{ST}, and subscripts "*t*", "*alt*" and "*dcl*" are included for denoting traditional, alternate-cascaded and dc-link-cascaded Z-source inverters, respectively.

Using (4.10), the relative capacitive voltage stresses V_{C_alt}/V_{C_t} and V_{C_dcl}/V_{C_t} experienced by the different hybrid-source networks can be deduced from (4.1), (4.5) and (4.7), and plotted in Fig. 4.9. Note that while deriving the capacitive voltage ratios

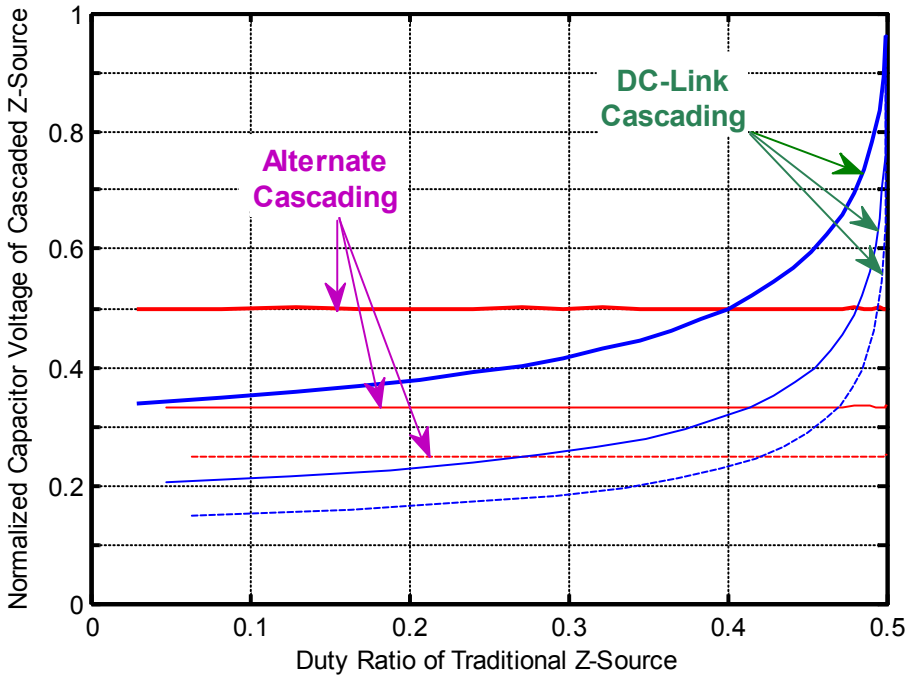


Fig. 4.9. Capacitive voltage ratios V_{C_alt}/V_{C_t} and V_{C_dcl}/V_{C_t} versus traditional Z-source duty ratio δ_t when producing the same voltage gain. Bold solid, solid and dashed lines represent $N = 2$, 3 and 4, respectively.

and other ratios hereafter, the right hand expressions of (4.1) have been scaled up by N to account for the common total input voltage of NV_{dc3} set for the example test case. While computing V_C for the dc-link-cascading method, the worst case voltage in network N has also been considered.

From Fig. 4.9, it is clear that the alternate-cascading method results in a fixed reduction of the capacitive voltage stress, whose amount is inversely proportional to the number of networks connected together. Also shown is the much greater reduction introduced by the dc-link-cascading method, whose extent lessens and ends up rising above that of the alternate-cascading method as δ_t increases towards 0.5. Doing the same to compute their dc-link voltage ratios $\hat{v}_{i\_alt}/\hat{v}_{i\_t}$ and $\hat{v}_{i\_dcl}/\hat{v}_{i\_t}$ results in Fig. 4.10, which again shows both methods giving rise to lower dc-link voltages, and hence lower semiconductor stresses experienced by their rear-end VSI bridges. The extent of reduction is observed to be greater for the dc-link-cascading method, but lessens as δ_t approaches 0.5.

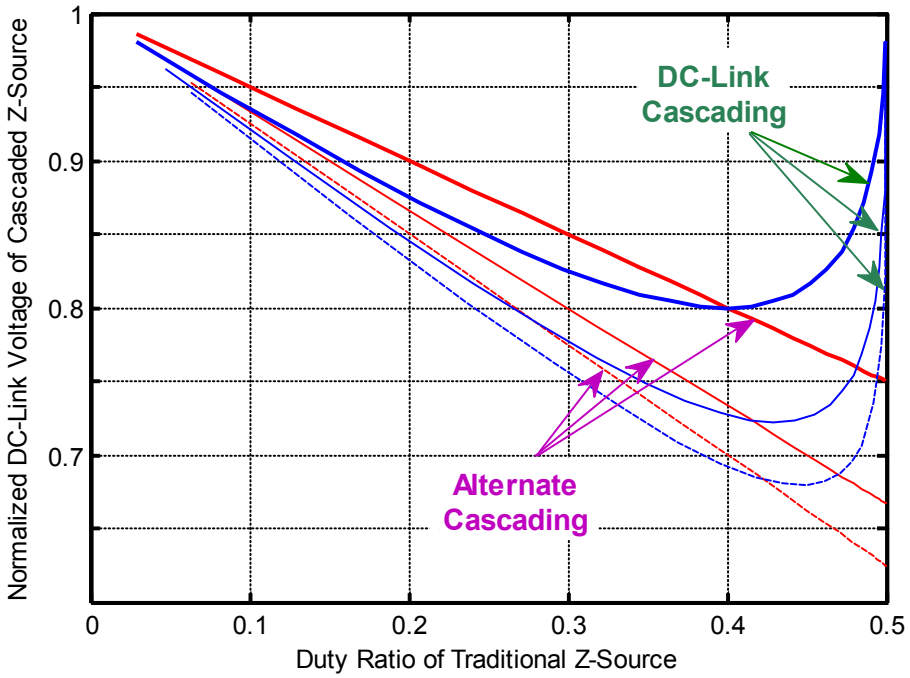


Fig. 4.10. DC-link voltage ratios $\hat{v}_{i\_alt}/\hat{v}_{i\_t}$ and $\hat{v}_{i\_dcl}/\hat{v}_{i\_t}$ versus traditional Z-source duty ratio δ_t when producing the same voltage gain. Bold solid, solid and dashed lines represent $N = 2$, 3 and 4, respectively.

The next factor of interest for comparison is the sizing of each inductor, which rightfully should be chosen to avoid those additional unwanted states identified in [75]. Those additional states surface when any of the diodes D unintentionally block when in the non-shoot-through state. Obviously, that happens when the diode current falls to zero, which is more likely at network N, where the voltage level is the highest. That then means the condition to avoid the unwanted states is:

$$i_L + i_C = 2i_L - i_i \geq 0 \quad \Rightarrow I_L - \Delta i_L/2 \geq I_{ac}/2$$
$$\Delta i_L \leq 2I_L - I_{ac} \tag{4.11}$$

where I_{ac} is the peak ac output current fixed by the load and represents the worst case value for i_i, I_L is the average inductive current, and Δi_L is the peak-to-peak inductive current ripple. For the dc-link-cascading technique, I_L and Δi_L should more rightfully be

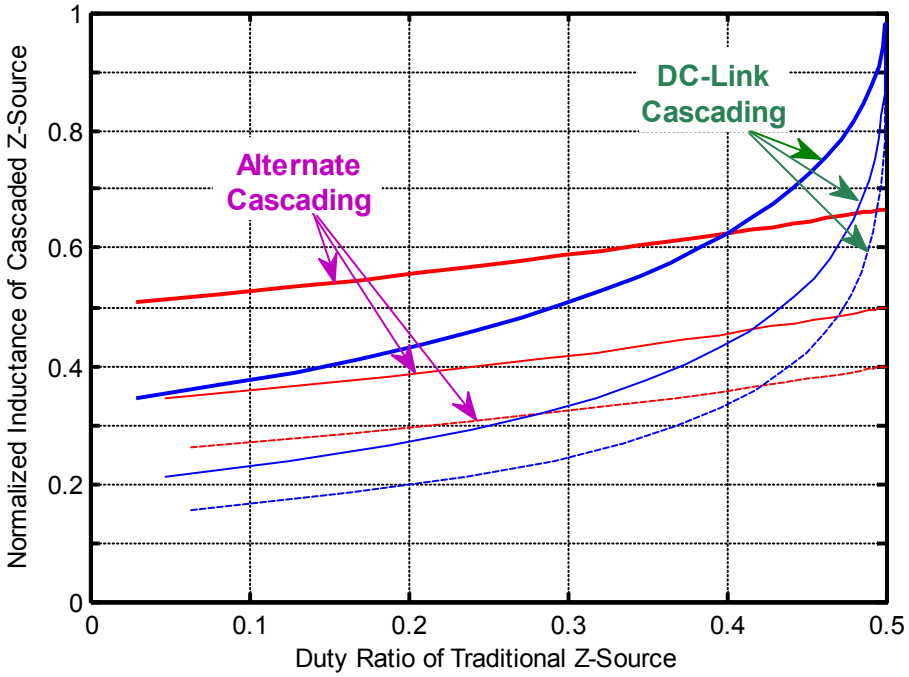


Fig. 4.11. Minimum inductance ratios L_{alt}/L_t and L_{alt}/L_t versus traditional Z-source duty ratio δ_t when producing the same voltage gain. Bold solid, solid and dashed lines represent $N = 2$, 3 and 4, respectively.

replaced by I_{LN} and Δi_{LN} for network N, whose inductor current expression is given in (4.8).

Upon selecting an appropriate upper limit for Δi_L based on (4.11) and noting that the non-shoot-through current ripple can be written as $\Delta i_L = V_C(1-\delta)T/L$, the smallest inductances needed by the two multi-network inverters can be determined for a fixed switching frequency (= 1 / T) and realistic operating range for δ. Value of V_C needed for the calculation can also be determined from (4.5) for the alternate-cascading method or (4.7) for the dc-link-cascading method. The computed inductances can then be normalized with reference to that of the conventional single-network inverter having the same upper ripple current limit for Δi_L. The resulting ratios are plotted in Fig. 4.11, which unarguably shows the smaller inductance requirement of the two multi-network inverters with the dc-link-cascading method having a greater advantage over a wider range of δ_t. The dc-link-cascading method would however require $2N$ inductors, which

is more than the $N + 1$ needed by the alternate-cascading method.

As for capacitance, circuit analysis reveals that currents flowing through the Z-source capacitors are different for the alternate-cascading method ranging from $-I_L$ to $-NI_L$ when in the shoot-through state. The maximum of $-NI_L$ flows through C_2 of the uppermost network N and C_1 of the lowermost network 1, based on the labeling convention adopted in Fig. 4.6. Charge released per capacitor is then $\Delta Q = \delta_{alt} N I_L T$, which will in turn lead to a voltage drop of $\Delta v_C = \Delta Q / C_{alt}$. The required capacitance is then determined as $C_{alt} = \delta_{alt} N I_L T / \Delta v_C = (\delta_t I_L T / \Delta v_C)\,(1/(1 - \delta_t (N-1)/N))$, after applying (4.10) to maintain a constant input-to-output voltage ratio. For $0 \le \delta_t < 0.5$ and $(N-1)/N \to 1$ if N is large, the worst-case alternate-cascading capacitance is written as $C_{alt} < 2C_t$, where $C_t = \delta_t I_L T / \Delta v_C$ is the capacitance needed by the conventional Z-source inverter for the same Δv_C. Note however that for a more realistic example like $N = 3$ used in the experiment and maximum $\delta_t = 0.3$ limited by parasitic, the smallest value for C_{alt} is $1.25C_t$, rather than doubling.

In contrast, current flowing through each capacitor in the dc-link-cascaded inverter is $-I_{Lk}$ when in the shoot-through state. The corresponding voltage drop is then $\Delta v_C = \delta_{dcl} I_{Lk} T / C_{dcl}$, whose value is maximum at the $k = 1$ network. At that network, current I_{L1} is the same as I_L for the alternate-cascading method and conventional Z-source inverter, if they have the same input-to-output voltage gain. The required capacitance to produce the same ripple variation is then written as $C_{dcl} = \delta_{dcl} I_L T / \Delta v_C < C_t$, since $\delta_{alt} < \delta_t$ for the same input-to-output voltage gain. Individual capacitance sizing for the dc-link-cascading method is therefore analyzed to be better than its conventional precedence, while the alternate-cascading method is poorer, whose extent depends on the number of networks being cascaded.

Summarizing the above discussion, the cascading techniques do have some interesting advantages, even though their high LC component count does not appear attractive at first sight. Their adoption should therefore not be ruled out completely, but rather judged

based on the overall system requirements on a case-by-case basis.

4.4.2. Multiple Networks versus Direct Two-Stage Connection

It certainly is possible to realize an inverter with enhanced boosting by connecting an enhanced dc-dc boost converter to a dc-ac inverter without reducing any component through functionality merging. Such arrangement is simple, and allows independent control of the two conversion stages without subjecting the modulation ratio M of the inverter to constraints imposed by the boost duration of the dc-dc converter. That certainly is favorable since M can always be kept close to 1.15 to keep the semiconductor voltage stress low for any commanded gain. This advantage is however diluted by the alternate-cascading technique, whose extent of dilution lessens as the number of networks N rises. The reason is obvious after referring to (4.5), where it is seen that the maximum gain is attained at a much higher δ_{alt} $(= 1/(N+1))$, which in turn allows a much higher $M \leq 1.15 \times (1 - \delta_{alt})$ to be set. The value of this higher M increases as the number of networks N increases.

Other than being independence and an associated lower voltage stress, the two-stage configuration might not have other prominent advantages over the multi-network cascaded Z-source inverters. Instead, its usual requirement for at least one active switch and some accompanied gating circuitries for the front-end dc-dc converter, even for only unidirectional power flow, makes it more complex and susceptible to failures. Its rear-end VSI bridge, being not protected by inductances, must also be protected by dead-time delays, which are prone to false tripping caused by electromagnetic interference (EMI). These disadvantages are not met by the proposed cascaded Z-source inverters, and in fact all Z-source inverters reported to date.

4.5. Experimental Results

For testing the alternate-cascading concept, three hybrid-source networks using a reduced number of four ($N + 1$, where $N = 3$) inductors were assembled. The inductance

and capacitance values used for each network were L = 5 mH and C = 2200 μF, respectively. The overall alternate-cascaded network assembled was then powered by a single 100-V dc source placed at the dc-link, implying NV_{dc3} = 100 V with the other source values set to zero in Fig. 4.6. Note that with this source arrangement, no unbalance was introduced to the three networks, unlike the second NPC test case described shortly, where an unbalance was distinctly observed. The three-network structure, terminated by a two-level VSI bridge, was then tested under voltage-buck operation with $M = 0.8 \times 1.15$ and $\delta_{alt} = 0$, respectively. The corresponding experimental waveforms obtained using the same modulation technique reviewed in Section 2.4.3 are printed in Fig. 4.12.

As anticipated, the dc-link voltage, reflected by the phase voltage (measured with respect to the negative dc rail) and line voltage pulse heights, is measured at 100 V, which is the same as the input voltage since no voltage boosting is commanded yet. The ac current amplitude measured in the figure is about 2 A, which can be boosted by tuning δ_{alt} to a non-zero value. To illustrate that, Fig. 4.13 shows the recaptured waveforms with the control parameters retuned to $M = 0.8 \times 1.15$ and $\delta_{alt} = 0.2$ to initiate voltage-boost operation. With a boosted dc-link voltage of about 275 to 300 V available for powering the rear-end inverter bridge, its ac current amplitude is boosted to around 5 A, which represents an ac gain of around 2.5. This measured gain is however lower than that calculated theoretically, because of system parasitic found in the not yet optimized experimental setup.

The 100-V source was next split into two 50-V units, and connected to V_{dc1} of networks 1 and 3 in Fig. 4.8 with the other indicated sources set to zero ($V_{dc2} = V_{dc3} = 0$ V in networks 1 to 3, and $V_{dc1} = 0$ V in network 2). The two-level bridge was also intentionally replaced by a three-level NPC bridge before performing the experiments again under the same voltage-buck and boost operating conditions described earlier. Corresponding waveforms obtained using the NPC modulation technique described in [95] are shown in Fig. 4.14 and Fig. 4.15. The same voltage and current gain information

is conveyed, but with better conditioned three-level phase and five-level line voltage waveforms displayed.

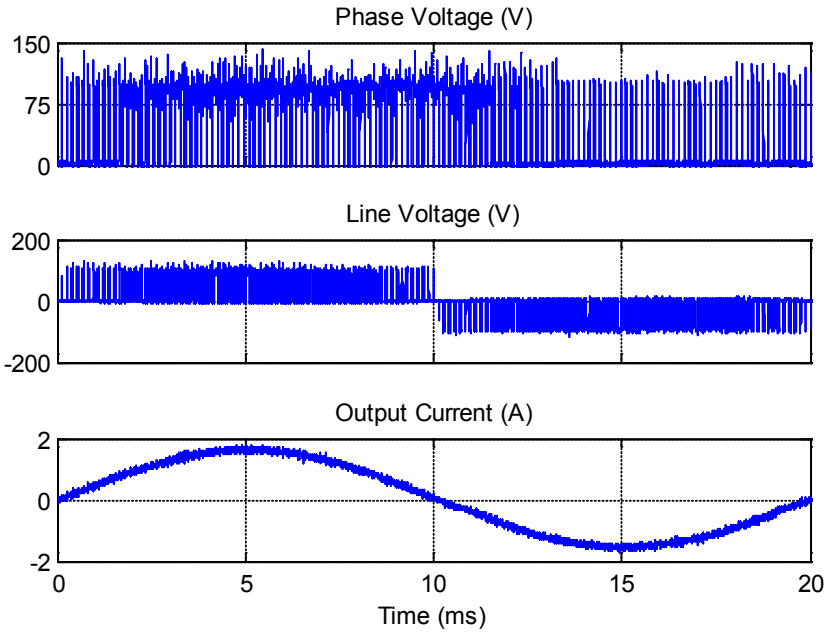


Fig. 4.12. Experimental ac waveforms of a two-level, three-network inverter realized by alternate-cascading with $M = 0.8 \times 1.15$ and $\delta_{alt} = 0$.

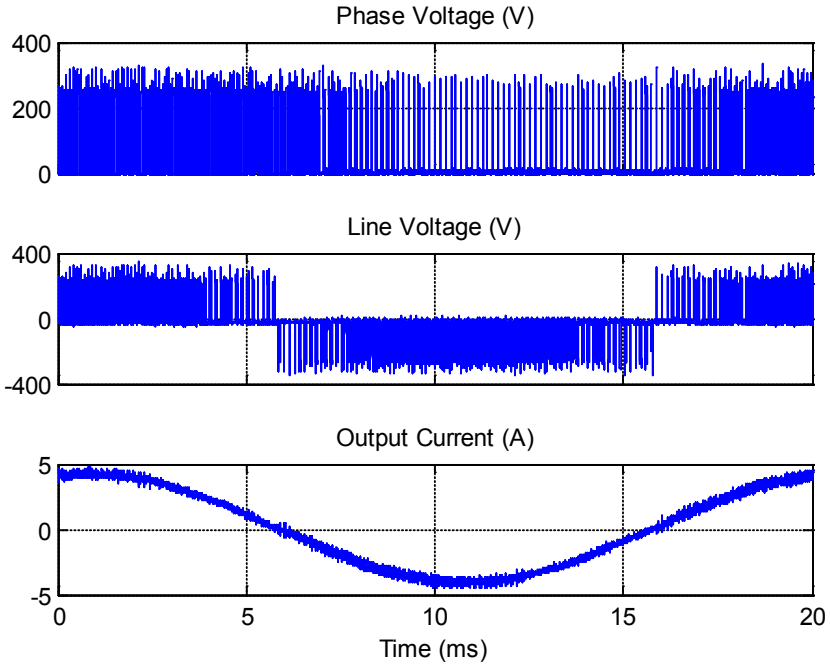


Fig. 4.13. Experimental ac waveforms of a two-level, three-network inverter realized by alternate-cascading with $M = 0.8 \times 1.15$ and $\delta_{alt} = 0.2$.

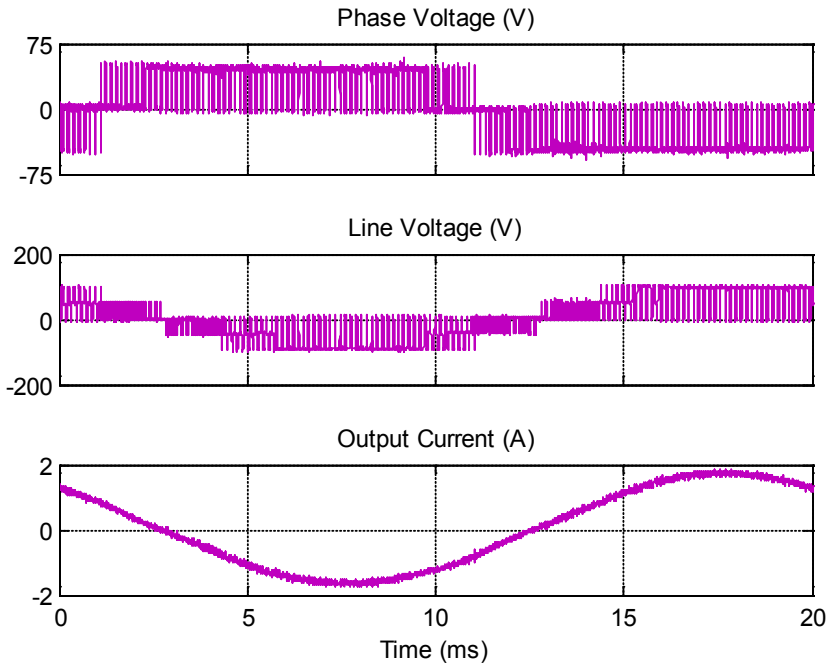


Fig. 4.14. Experimental ac waveforms of a three-level NPC, three-network inverter realized by alternate-cascading with $M = 0.8 \times 1.15$ and $\delta_{alt} = 0$.

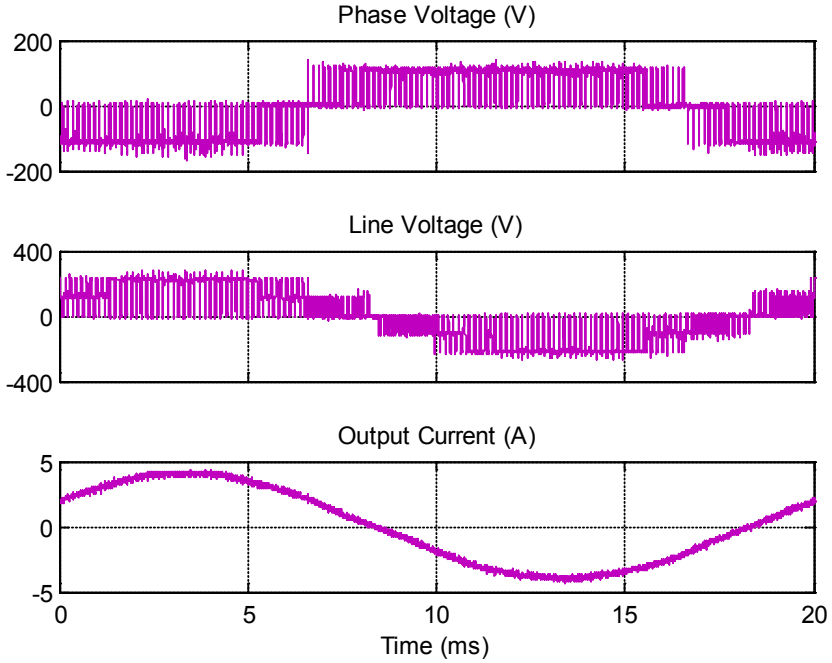


Fig. 4.15. Experimental ac waveforms of a three-level NPC, three-network inverter realized by alternate-cascading with $M = 0.8 \times 1.15$ and $\delta_{alt} = 0.2$.

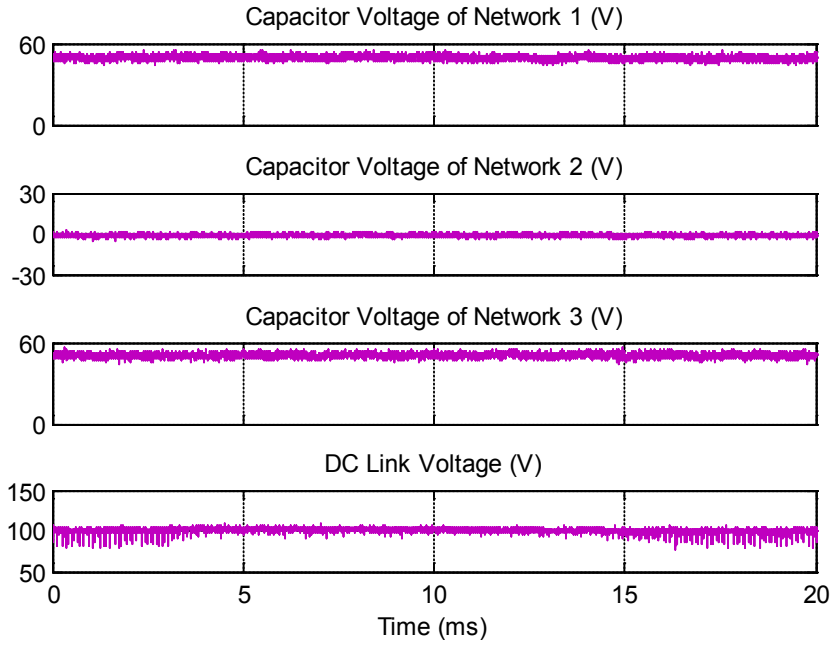


Fig. 4.16. Experimental dc waveforms of a three-level NPC, three-network inverter realized by alternate-cascading with $M = 0.8 \times 1.15$ and $\delta_{alt} = 0$.

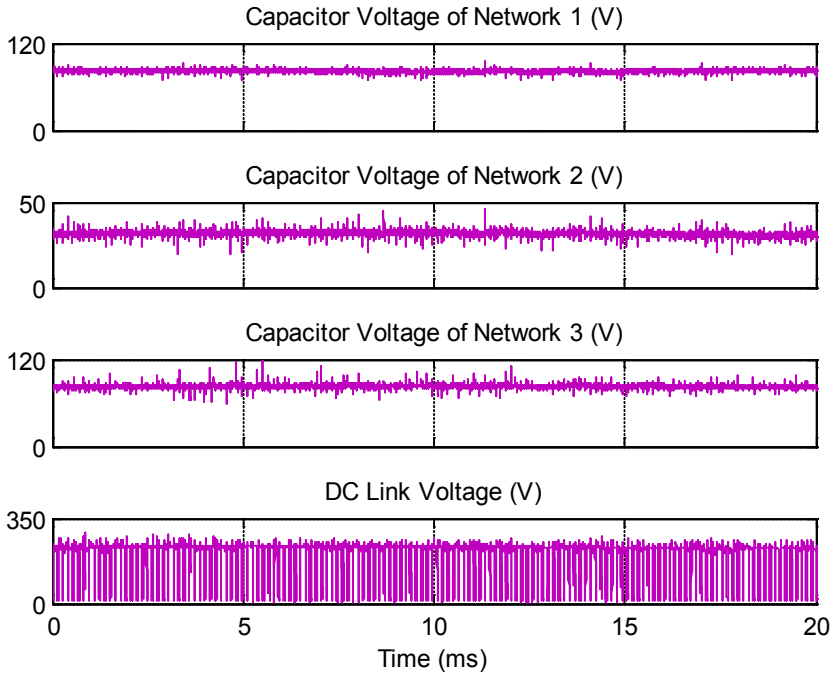


Fig. 4.17. Experimental dc waveforms of a three-level NPC, three-network inverter realized by alternate-cascading with $M = 0.8 \times 1.15$ and $\delta_{alt} = 0.2$.

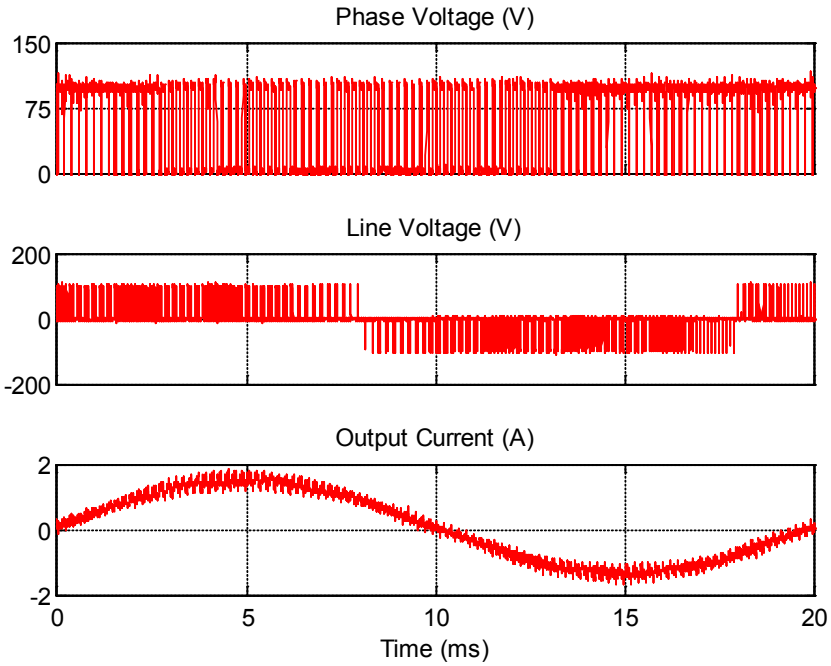


Fig. 4.18. Experimental ac waveforms of a two-level, two-network inverter realized by dc-link-cascading with $M = 0.8 \times 1.15$ and $\delta_{dcl} = 0$.

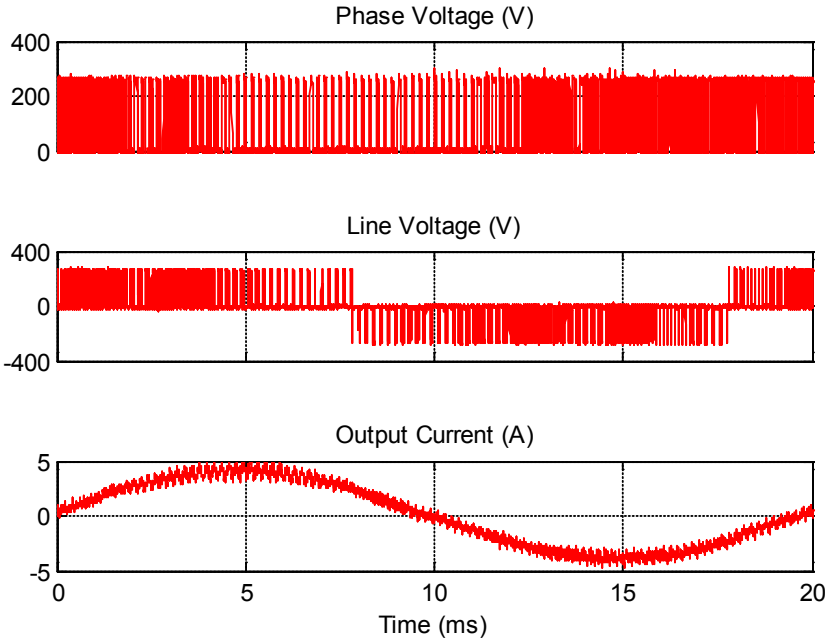


Fig. 4.19. Experimental ac waveforms of a two-level, two-network inverter realized by dc-link-cascading with $M = 0.8 \times 1.15$ and $\delta_{dcl} = 0.2$.

To demonstrate its unbalanced front-end dc behavior caused by the uneven distribution of sources (V_{dc1} = 50 V in networks 1 and 3, while V_{dc1} = 0 V in network2), Fig. 4.16 shows the capacitive voltages measured within the three networks, and the dc-link voltage under voltage-buck operation. As anticipated, the capacitive voltages of networks 1 and 3 remain the same as their input voltages, while that of network 2 is kept at zero since no source is tied to it. The dc-link voltage is noted at 100 V without switching, which again is expected since no shoot-through state is inserted during voltage-buck operating mode. When commanded to enter the voltage-boost mode, Fig. 4.17 shows the recaptured waveforms at the dc front-end, which again reflects an unequal capacitive voltage distribution among the networks. Also shown in the figure is the chopping dc-link voltage, which in principle is caused by the insertion of shoot-through states to the inverter state sequence.

The experiments were then performed a third time with the LC components rearranged to give two networks connected together by the dc-link cascading method. The 100-V source was then shifted to the V_{dc1} position of network 1 in Fig. 4.7. The same voltage-buck and boost operating conditions were re-tested with the corresponding results shown in Fig. 4.18 and Fig. 4.19. These figures clearly reflect the same voltage-buck and boost responses, hence validating the dc-link-cascading method as well.

Another common feature illustrated from the experimental observation is the flow of a much larger current through the inverter phase-legs during shoot-through insertion. Analytical value for this larger current can be determined from (4.6) for the alternate-cascading method or (4.9) for the dc-link-cascading method, which of course will deviate in practice due to parasitic influences. The current will eventually drop back to the load demanded value upon re-entering a non-shoot-through state, before repeating the cycle again. An example showing such current transition can be found in Fig. 4.20 for the dc-link-cascaded Z-source inverter. The same wave pattern is equally applicable to the alternate-cascading method except for a different shoot-through current pulse height detected.

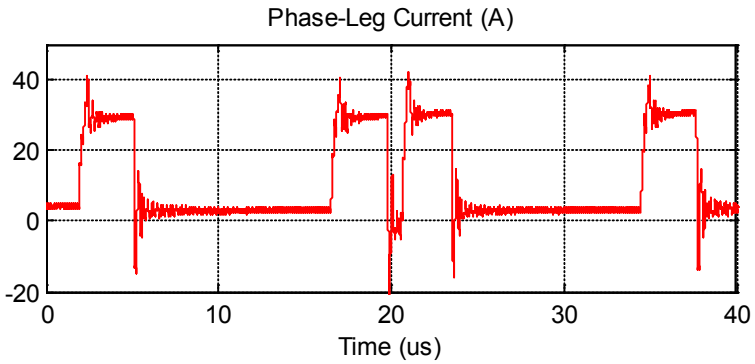


Fig. 4.20. Experimental phase-leg current waveform of a two-level, two-network inverter realized by dc-link-cascading with $M = 0.8 \times 1.15$ and $\delta_{dcl} = 0.2$.

4.6. Summary

From analyzing existing Z-source impedance networks, two generic network entities can be summarized for realizing voltage-type and current-type hybrid-source inverters. Multiple of the voltage-type entities can then be connected together by adopting either the alternate or dc-link-cascading technique. Inverters formed using these cascaded networks are capable of producing higher ac output voltage gains by inserting either the same or shorter shoot-through time duration. Even if the same input-to-output voltage gain is demanded, the multi-network inverters still have advantages over their conventional single-network counterparts. Experimental testing has already confirmed these advantages, which are likely to be beneficial for renewable energy systems, where high gain is demanded for grid interfacing.

Chapter 5 Enhanced Z-source Inverters – Non-Cascading Techniques

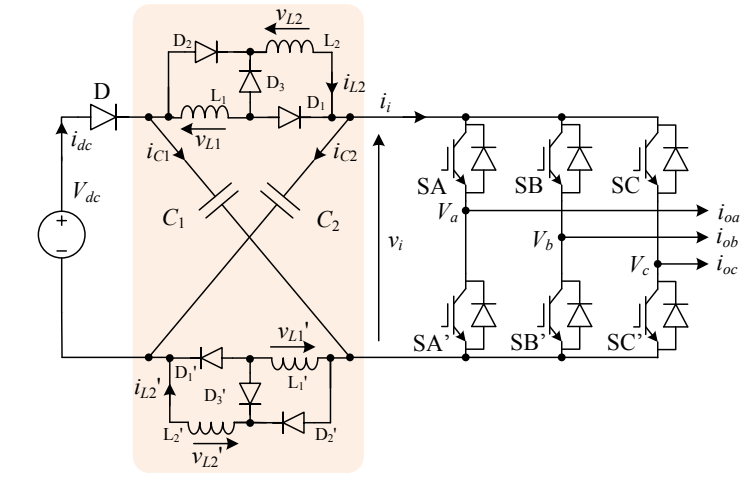
Cascading techniques for achieving enhanced voltage boost in Z-source inverters are presented in the earlier chapter. Their performances have already been verified through experimental testing. However, they are not the only techniques that can achieve enhanced voltage boosting. This chapter continues the development by presenting a few non-cascading alternatives that use lesser components, but experience higher component stresses. They are respectively named as the switched-inductor (SL), switched-capacitor (SC) and tapped-inductor (TL) techniques, and can also produce the high gains needed for tying renewable sources to the grid. Detailed operating principles of the non-cascading techniques are elaborated, before comparing them with the cascading techniques. Both non-cascading and cascading techniques can be used for renewable source voltage boosting, but for better integrated solutions with more compromised characteristics, the next two chapters should be referred to.

5.1. Generalized Multi-Cell SL and SC Z-Source Inverters

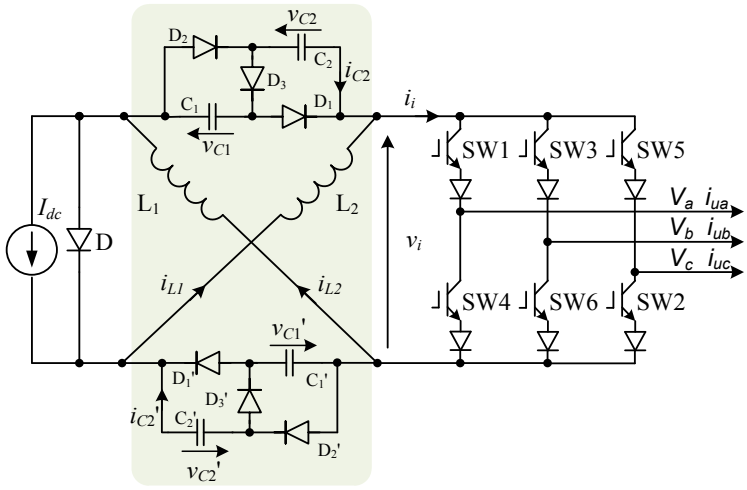
Multi-cell SL and SC techniques are discussed in this section for raising the input-to-output gains of conventional Z-source inverters. Their respective elementary cells are first discussed before generalization is applied to arrive at their multi-cell arrangements.

5.1.1. Elementary SL and SC Topologies

Fig. 5.1(a) shows the elementary voltage-type SL Z-source inverter, which when compared with the conventional voltage-type Z-source inverter shown in Fig. 2.6(a), is derived by replacing the two inductors in the conventional network with two SL cells. The SL cell was earlier proposed for various dc-dc converters [94], before it was applied



(a)



(b)

Fig. 5.1. Topologies of (a) voltage-type SL and (b) current-type SC Z-source inverters.

to the voltage-type Z-source inverter. Its generalization is to date not attempted, and is now addressed in the next section after reviewing the elementary SL cell. Strictly, it is also commented here that components of the Z-source network need not be symmetrical even though it is usually assumed to be so. That means replacing the upper or lower inductor of the conventional Z-source network by a SL cell alone will work fine, but with asymmetrical voltage and current stresses experienced by its components.

Like the conventional Z-source inverter, the voltage-type SL inverter can operate in both shoot-through and non-shoot-through states. Features and expressions accompanying these states are presented, as follows.

Shoot-Through: Introduced by turning on two switches simultaneously from at least a phase-leg of the VSI bridge. Upon doing so, diodes *D*, D_3 and D_3' reverse-bias, while diodes D_1, D_2, D_1' and D_2' conduct. The two inductors per SL cell are hence in parallel with their voltages expressed as $v_L = v_{L1} = v'_{L1} = v_{L2} = v'_{L2} = V_{C1} = V_{C2} = V_C$.

Non-Shoot-Through: Referred to any of the traditional six active and two null states of a VSI. In this state, diodes *D*, D_3 and D_3' conduct, while diodes D_1, D_2, D_1' and D_2' block. The two inductors per SL cell are thus in series, leading to $v_L = (V_{dc} - V_C)/2$.

Averaging v_L over a switching period to zero then gives rise to the following governing expressions for the capacitor voltage V_C, peak dc-link voltage $\hat{v}_i$ and peak ac output voltage $\hat{v}_{ac}$ in terms of the source voltage V_{dc} [85]:

$$V_C = \frac{1-d_{ST}}{1-3d_{ST}} V_{dc};$$
$$\hat{v}_i = \frac{1+d_{ST}}{1-3d_{ST}} V_{dc}$$
$$\hat{v}_{ac} = \frac{M(1+d_{ST})}{1-3d_{ST}} \frac{V_{dc}}{2} \quad (5.1)$$

where $M \leq 1.15$ and $d_{ST} < 1/3$ represent the modulation ratio after adding triplen offset and normalized shoot-through time per switching period, respectively. The boost ratio *B* can then be written as $B = (1 + d_{ST})/(1 - 3d_{ST})$, which is larger than $B = 1/(1 - 2d_{ST})$ of the traditional Z-source inverter with the same shoot-through duration.

From the SL cell, the dual SC cell can be derived, and is now applied to the traditional current-type Z-source inverter shown in Fig. 2.6(b). The modified SC topology is shown in Fig. 5.1(b), where unlike Fig. 2.6(b), the X-shaped network has been "twisted" with the source now directed downward and diagonal branches consisting of inductors [72]. Such "twisting" allows clearer insertion of the SC cells, while preserving the X-shaped structure. The resulting SC topology can still assume two distinct states, whose operating features and expressions are written as:

Open-Circuit: Introduced by turning off all switches of the CSI bridge, causing diodes *D*, D_3 and D_3' to conduct naturally. On the contrary, diodes D_1, D_2, D_1' and D_2' block naturally. The resulting circuit consists of two series-connected capacitors per SC cell with their currents indicated as $i_C = i_{C1} = i'_{C1} = i_{C2} = i'_{C2} = I_{L1} = I_{L2} = I_L$.

Non-Open-circuit: Referred to any of the traditional six active and three null states of a CSI. In this state, diodes *D*, D_3 and D_3' block, while diodes D_1, D_2, D_1' and D_2' conduct, hence giving rise to two parallel-connected capacitors per SC cell. Their common capacitive current is given by $i_c = (I_{dc} - I_L)/2$.

Averaging the capacitive current to zero per switching cycle then results in the following equations for relating the network inductive current I_L, peak dc-link current $\hat{\imath}_i$ and peak ac output current $\hat{\imath}_{ac}$ with the input current I_{dc}:

$$I_L = \frac{1-d_{OC}}{1-3d_{OC}} I_{dc};$$
$$\hat{\imath}_i = \frac{1+d_{OC}}{1-3d_{OC}} I_{dc}$$
$$\hat{\imath}_{ac} = \frac{M(1+d_{OC})}{1-3d_{OC}} I_{dc} \qquad (5.2)$$

where $d_{OC} < 1/3$ represents the normalized open-circuit duration per switching period. The computed current boost factor of $B' = (1 + d_{OC})/(1 - 3d_{OC})$ is again larger than that of $B' = 1/(1 - 2d_{OC})$ of the traditional current-type Z-source inverter drawn in Fig. 2.6(b).

5.1.2. Generalized SL and SC Topologies

From the denominator of (5.1), the maximum shoot-through duration is limited to $d_{ST} < 1/3$. Since the shoot-through state can only replace traditional null states of a VSI to avoid introducing volt-sec error, the range of modulation ratio is also limited to $M \leq 1.15(1 - d_{ST})$. The upper limit of *M* can be as low as 66% of a normal VSI maximum when d_{ST} is close to 1/3. This represents poor utilization of the dc-link voltage

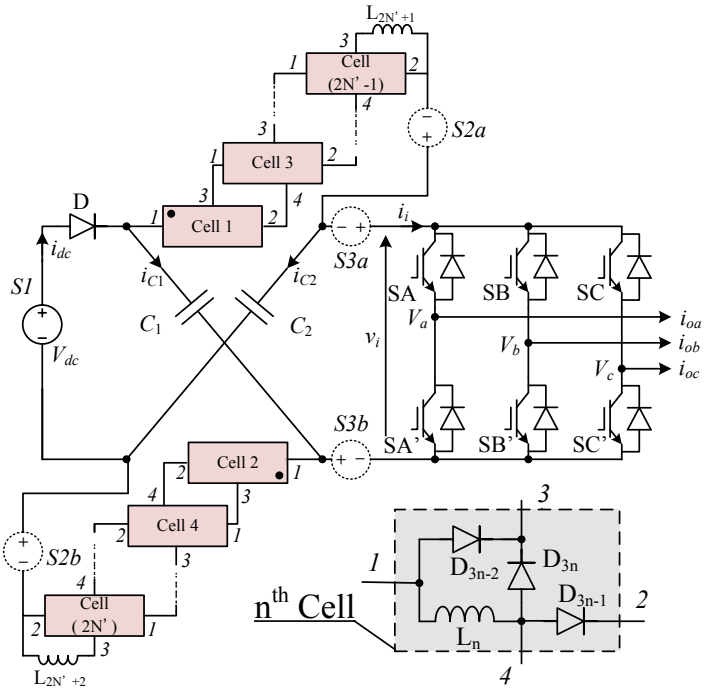


Fig. 5.2. Topologies of generalized voltage-type SL Z-source inverters.

and unnecessarily high component stresses, which contradictorily dilute the initial intention of investigating the elementary SL topology. The same limitation is faced by the elementary current-type SC inverter because of the same denominator in (5.2). To raise their modulation ratios while preserving their boosting abilities, the SL and SC concepts are generalized here for voltage and current-type Z-source inverters, respectively.

5.1.2.1. Generalized Voltage-Type SL Topology

The SL topology is generalized in Fig. 5.2, where the generic cell identified is shown at the lower right corner. It consists of one inductor L_n and three diodes D_{3n-1}, D_{3n-2} and D_{3n} for the n^{th} cell. This cell can be duplicated $2N'$ times (where N' is an integer), divided equally between the upper and lower dc rails, and connected as in Fig. 5.2. Note that inductors $L_{2N'+1}$ and $L_{2N'+2}$ are not included in the generic cells, but can rather be viewed as the original two inductors found in Fig. 2.6(a) for the conventional voltage-type Z-source inverter. It thus appears that the style of forming the generic cell allows the generalized SL topology to be viewed as adding extra cells to the original two inductors rather than to replace them. These cells must introduce additional inductors in parallel

during shoot-through charging and more inductors in series during non-shoot-through discharging. Features and expressions for the two processes are summarized, as follows:

Shoot-Through: Initiated by turning on two switches from the same phase-leg of the VSI bridge. That causes diodes D and D_{3n} to turn off, while diodes D_{3n-1} and D_{3n-2} conduct. All inductors are then charged in parallel by the two Z-source capacitors, giving rise to a common inductive voltage of $v_L = V_C$.

Non-Shoot-Through: Represented by one of the traditional active or null VSI states. In this state, diodes D and D_{3n} conduct, while diodes D_{3n-1} and D_{3n-2} block. All inductors then discharge in series to the external ac load, whose common inductive voltage is written as $v_L = (V_{dc} - V_C)/(N' + 1)$, where $N' + 1$ is the number of inductors in the upper or lower SL block.

Averaging v_L over a switching period to zero then gives the following generic expressions for governing the generalized SL Z-source inverter:

$$V_C = \frac{1-d_{ST}}{1-(N'+2)d_{ST}} V_{dc};$$
$$\hat{v}_i = \frac{1+N'd_{ST}}{1-(N'+2)d_{ST}} V_{dc}$$
$$\hat{v}_{ac} = \frac{M[1+N'd_{ST}]}{1-(N'+2)d_{ST}} \frac{V_{dc}}{2} \quad (5.3)$$

The boost factor is given by $B = (1 + N'd_{ST})/(1 - (N' + 2)d_{ST})$, which can be made higher than any of the earlier gains by adding more generic cells. The desired gain is also arrived at a reduced shoot-through duration, whose limit $d_{ST} < 1/(N' + 2)$ is derived by setting the denominator of (5.3) to be greater than zero. That allows a higher modulation ratio to be used since $M \leq 1.15(1 - d_{ST})$. Better utilization of the dc-link, lower component stresses and better spectral performance linked to a high M can therefore be achieved.

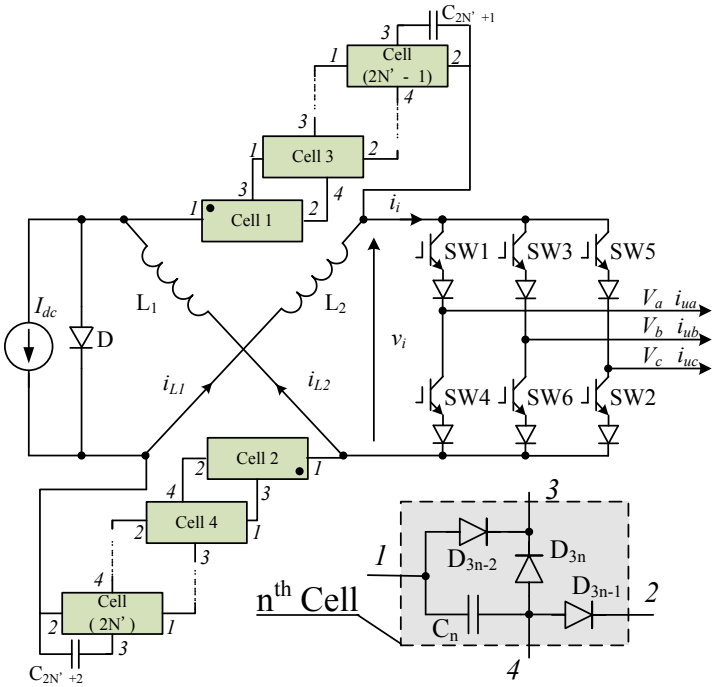


Fig. 5.3. Topologies of generalized current-type SC Z-source inverters.

5.1.2.2. Generalized Current-Type SC Topology

Similar analysis can be performed on the generalized SC topology shown in Fig. 5.3, where $2N'$ cells are duplicated and connected together. The inner layout of each generic SC cell is shown at the bottom right of Fig. 5.3, where a capacitor C_n and three diodes D_{3n-1}, D_{3n-2} and D_{3n} can clearly be seen. This style of modeling does not include capacitors $C_{2N'}$ and $C_{2N'-1}$ in the generic cells. They can rather be viewed as the original two capacitors found in the conventional current-type Z-source inverter drawn in Fig. 2.6(b). The generic cells are therefore added to complement the existing two capacitors rather than to replace them. For current-type inverter, these capacitors can generally be smaller since the more important task is to keep the inductive currents constant.

Connecting in the described manner then leads to the following two operating scenarios for the generalized SC Z-source inverter.

Open-Circuit: Introduced by turning off all switches of the CSI bridge with diodes D and D_{3n} conducting, and diodes D_{3n-1} and D_{3n-2} blocking. The capacitors are therefore charged in series with their common capacitive current written as $i_C = I_L$.

Non-Open-circuit: Represented by any of the nine traditional active and null states of a CSI. In this state, diodes D and D_{3n} block, while D_{3n-1} and D_{3n-2} conduct to discharge the capacitors in parallel so as to produce a higher dc-link current. Each capacitive current can appropriately be written as $i_c = (I_{dc} - I_L)/(N' + 1)$, where $N'+1$ is the number of capacitors per upper or lower SC block.

Performing the same averaging of capacitive current to zero then results in the following few equations for governing the inverter:

$$I_L = \frac{1-d_{OC}}{1-(N'+2)d_{OC}} I_{dc};$$

$$\hat{\imath}_i = \frac{1+N'd_{OC}}{1-(N'+2)d_{OC}} I_{dc}$$

$$\hat{\imath}_{ac} = \frac{M[1+N'd_{OC}]}{1-(N'+2)d_{OC}} I_{dc} \qquad (5.4)$$

The current boost factor of $B' = \frac{1+N'd_{OC}}{1-(N'+2)d_{OC}}$ can again be tuned higher, if intended.

5.1.3. Experimental Results

Experiments were first performed with the generalized SL Z-source inverter shown in

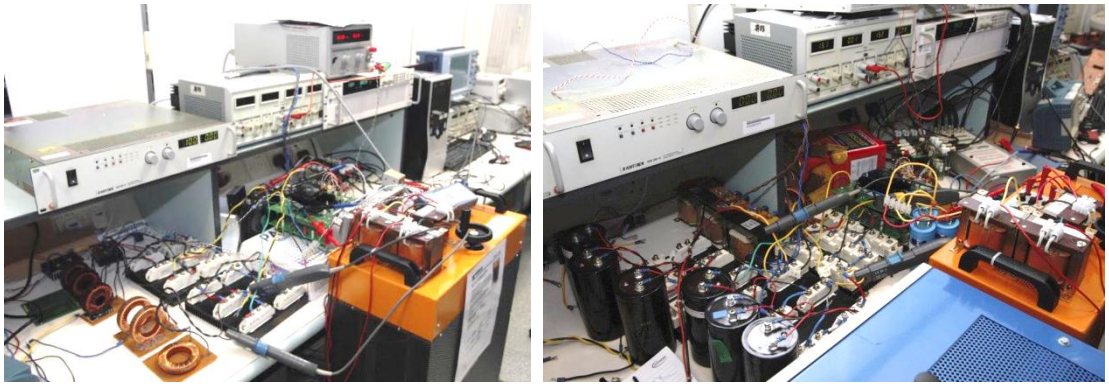


Fig. 5.4. Experimental (a) SL and (b) SC inverters.

Fig. 5.2 using the modulation technique reviewed in Section 2.4.3. In total, four generic cells with six 3-mH inductors and two 2200-μF capacitors were used. The cells were inserted equally to the upper and lower dc rails, giving $N' = 2$ and a computed boost factor of 3.25 according to (5.3) and a shoot-through duration of $d_{ST} = 0.15$. The inverter was supplied from a 100-V dc source, and was connected to a resistive-inductive load of 46 Ω and 5 mH. Photographs showing the experimental setup can be found in Fig. 5.4

Corresponding experimental waveforms are shown in Fig. 5.5 and Fig. 5.6 for a modulation ratio of $M = 0.85 \times 1.15$ (1.15 introduced by the triplen offsets). Fig. 5.5 shows a dc-link voltage that switches between 0 and 300 V, representing shoot-through and non-shoot-through states, respectively. The measured boost factor is thus 3, which is

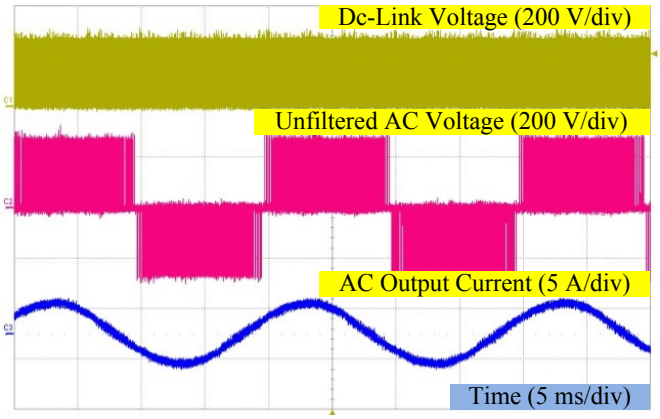


Fig. 5.5. Experimental dc-link voltage v_i, unfiltered ac line voltage v_{ab} and ac current i_{oa} for $N' = 2$, $d_{ST} = 0.15$ and $M = 0.8 \times 1.15$.

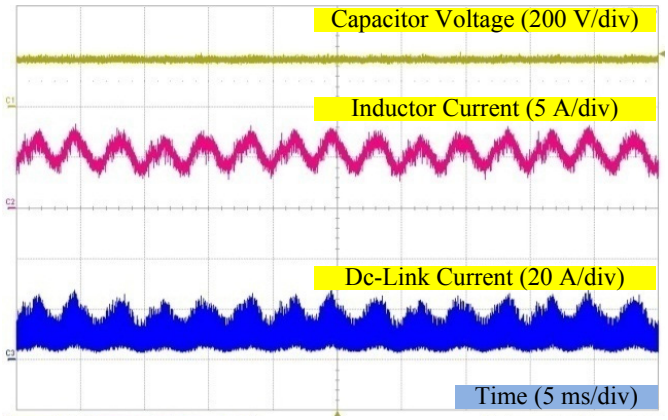


Fig. 5.6. Experimental dc capacitor voltage V_C, dc inductor current i_L and dc-link current i_i for $N' = 2$, $d_{ST} = 0.15$ and $M = 0.8 \times 1.15$.

slightly lower than the computed value of 3.25 due to switching and component parasitic. With this dc-link voltage, the measured ac peak current is 3 A, which again matches well with the computed value of $\frac{M\hat{v}_i/2}{|Z_{Load}|} = \frac{0.85 \times 1.15 \times 300}{2\sqrt{(100\pi \times 0.005)^2 + 46^2}} = 3.19$ A, where Z_{Load} is the load impedance.

Fig. 5.6 further shows the capacitor voltage, inductor current and dc-link current. As anticipated, the capacitor voltage and inductor current are smooth with common six-pulse ripple superimposed on the latter. However, the dc-link current is pulsing between a low value close to a single inductor charging current and an instantaneous high value equal to all inductor discharging currents.

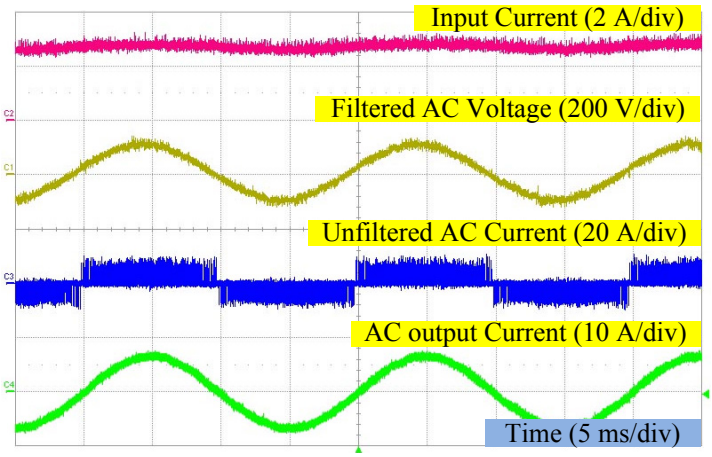


Fig. 5.7 xperimental input current I_{dc}, filtered ac voltage v_{ab}, unfiltered ac current i_{oa} and filtered ac current i'_{oa} for $N' = 2$, $d_{OC} = 0.15$ and $M = 0.8 \times 1.15$.

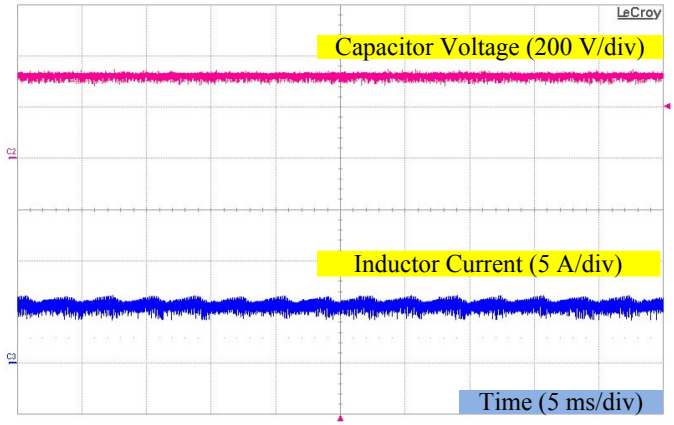
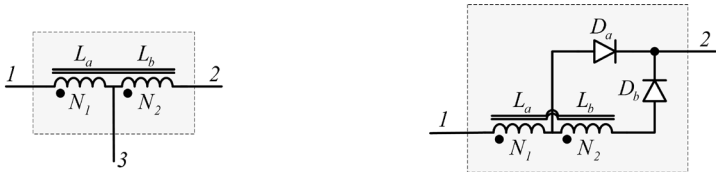


Fig. 5.8 Experimental dc capacitor voltage v_C and dc inductor current I_L for $N' = 2$, $d_{OC} = 0.15$ and $M = 0.8 \times 1.15$.

The experimental setup was next arranged as a generalized SC inverter (see Fig. 5.3) with two 20-mH inductors and six 2200-μF capacitors for forming four generic cells. Two cells each were placed at the upper and lower rails, giving $N' = 2$. The setup was eventually tied to a dc voltage source with an inductor in series to emulate a dc current source, and an ac RL load of 16 Ω and 2 mH, in parallel with a filter capacitor of 15 μF. With this rearrangement and the same control parameters, Fig. 5.7 and Fig. 5.8 show the captured experimental results. As noted from Fig. 5.7, the input and peak dc-link currents are 2.7 A and 8 A (observed from the unfiltered phase current waveform), respectively. That gives a gain of about 3, which is close to the theoretical value of 3.25. The measured ac current peak of about 7 A is also close to its theoretical value of $M \times I_{dc}$ = 0.8 × 1.15 × 8 = 7.36 A. This current, when flows through the load, produces a theoretical peak ac voltage of $MI_{dc}|Z_{Load}| = 7.36 \times \sqrt{16^2 + (100\pi \times 0.002)^2}$ = 118 V, which is close to the value read from the second trace in Fig. 5.7. Corresponding dc waveforms are shown in Fig. 5.8, where the dc inductive current of about 5.5 A is observed to be close to its theoretical value of 5.74 A, calculated by using the first expression in (5.4).

5.2. TL Z-source Inverters

Proposing another non-cascading possibility, this section investigates on a new TL Z-source impedance network, which is generally less complex, but yet able to produce the same high gain as for the SL inverter. Dating back to some previous dc-dc conversion concepts, the TL cell shown in Fig. 5.9(a) with three separate terminals is usually used to achieve extreme high or low voltage conversion ratios in a compact and



(a) (b)

Fig. 5.9. Illustrations of (a) three-terminal and (b) two-terminal TL cells.

low-cost structure [83][84]. Its energy storing and transferring mechanism is also no different from those of an auto-transformer and a two-winding coupled inductor. Its three-terminal structure is however not suitable for insertion to the usual Z-source impedance network. That then leads to the development of the new two-terminal TL cell proposed in this section and shown in Fig. 5.9(b).

Compared with the SL cell documented in [85] and shown in Fig. 5.1(a), the proposed TL cell is more compact with its turns ratio freely adjustable to produce any desired voltage gain. Inverters designed using this new TL cell are therefore more flexible, and are collectively named as the TL Z-source inverters with an example voltage-type topology shown in Fig. 5.10. Through thorough analysis of Fig. 5.10, the TL Z-source inverter can promptly be proved to have the following favorable operating features, which are either comparable or better than the conventional voltage-type Z-source inverter.

- The basic X-shaped structure is retained.
- Only five diodes and two TL cells are needed for producing voltage gain that is much higher than those of any existing techniques. Compromises in weight, size, complexity and cost are therefore less impactful here.
- The boost factor can be increased by simply changing the tap positions of the TLs.

5.2.1. Operational Analysis

As seen from Fig. 5.10, the proposed TL impedance network consists of two TL cells (L_{11}-L_{12}-D_{TL1}-D_{TL3} forming the first cell, and L_{21}-L_{22}-D_{TL2}-D_{TL4} forming the other), two capacitors (C_1 and C_2) and an input diode (D). The resulting network is symmetrical, but strictly, it is not necessary to be so. That means only one of the TL cells needs to be there, while the other can be replaced by a single-winding inductor like in the conventional Z-source impedance network. The only complexity linked with an asymmetrical network is the presence of asymmetrical voltage stresses within it, which at times can create single points of failure.

Together, the TL cells and capacitors help to temporary store, and then transfer energy from the input dc source to the inverter dc bus. This transfer, triggered by the inverter switching, is the main mechanism that gives the inverter its voltage buck-boost feature. To further avoid uneven stressing within the TL network, impedance values of the reactive components are usually chosen to be equal. That means $L_{11} + L_{12} = L_{21} + L_{22} = L$ and $C_1 = C_2 = C$. For the TL cells, their turns ratios are also set to be the same, and are conveniently written as γ_{TL}. With these inductive symbols defined, a few more expressions relating them can be written, as follows.

$$L_1 = L_2 = L$$
$$L_{11} = L_{21} = \left(\frac{1}{1+\gamma_{TL}}\right)^2 L$$
$$L_{12} = L_{22} = \left(\frac{\gamma_{TL}}{1+\gamma_{TL}}\right)^2 L \qquad (5.5)$$

Besides self-inductances, mutual inductance L_M of the TL cells should also be considered since it provides a means for measuring energy coupling efficiency within each TL cell. For an ideal TL cell whose coupling coefficient k is 1, L_M can be simplified to:

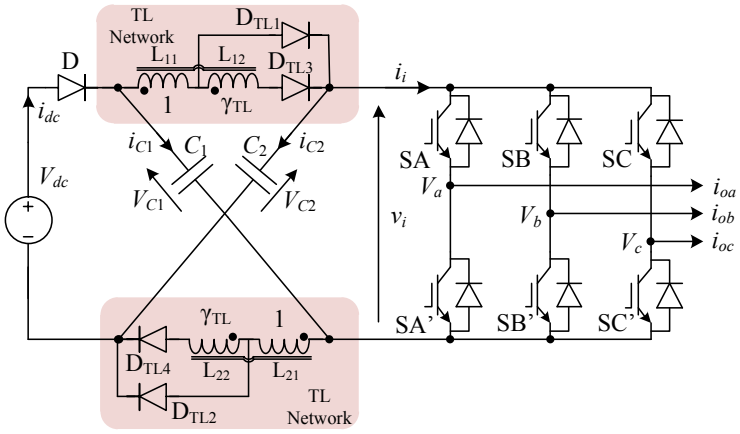


Fig. 5.10. Proposed TL Z-source inverter.

$$L_M = k\sqrt{L_{11}L_{12}} = \frac{\gamma_{TL}}{(1+\gamma_{TL})^2}L \tag{5.6}$$

Considering now its shoot-through operating state, the TL inverter will have its diodes D_{TL1} and D_{TL2} conducting, and D_{TL3} and D_{TL4} blocking, leading to the charging of the W_1 winding and the open-circuiting of the W_2 winding. On the other hand, when in its non-shoot-through state, diodes D_{TL3} and D_{TL4} conduct, while D_{TL1} and D_{TL2} block to discharge the two windings in series. Currents flowing through the two halves of the tapped inductor therefore experience step transitions. This will not happen with a normal single-winding inductor, whose current is always continuous. Such step transitions are fine so long as magnetic energy stored in the interrupted winding can be transferred to the other winding through perfect coupling.

Returning back to the non-shoot-through state, since the windings are discharged in series, the inverter ac output is again boosted higher than the conventional Z-source inverter. Its corresponding voltage expressions can easily be derived by applying state averaging, whose eventual expressions are written as follows [80].

$$V_C = \frac{1-d_{ST}}{1-(\gamma_{TL}+2)d_{ST}}V_{dc}$$
$$\hat{v}_i = \frac{1+\gamma_{TL}d_{ST}}{1-(\gamma_{TL}+2)d_{ST}}V_{dc}$$
$$\hat{v}_{ac} = M\frac{\hat{v}_i}{2} = \frac{1+\gamma_{TL}d_{ST}}{1-(\gamma_{TL}+2)d_{ST}}\left(\frac{MV_{dc}}{2}\right) \tag{5.7}$$

5.2.2. Experimental Results

A hardware prototype was assembled for verifying the feasibility of the TL inverter. Component values chosen were γ_{TL} = 2 for the TL, $C_1 = C_2$ = 2200 μF for the Z-source capacitors, and L_f = 5 mH and R = 40 Ω for the external ac load. The TL was wound on a molybdenum permalloy powder (MPP) core *C055906A2* following the pattern shown in Fig. 5.11. The assembled inverter was eventually powered from a 100-V dc source, and

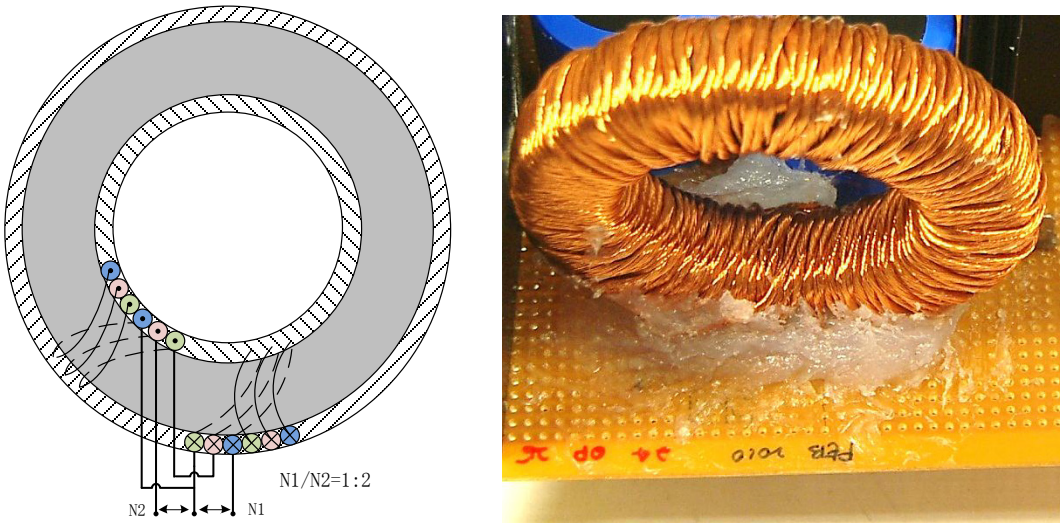


Fig. 5.11. Illustration of TL with $\gamma_{TL} = 2$.

was modulated by the modified reference scheme reviewed in Section 2.4.3 at a switching frequency of 20 kHz.

With this assembled system, Fig. 5.12 and Fig. 5.13 show the captured experimental results for the TL Z-source inverter for $M = 0.85 \times 1.15$ and $d_{ST} = 0.15$. The measured dc-link voltage is 300 V, which means a dc gain of 3, as compared to the calculated value of 3.25 from the second equation in (5.7). The lower gain is caused by parasitic resistances and not yet optimized circuit conditions, which nonetheless still shows a higher demanded boost, as compared to the conventional Z-source inverters. Fig. 5.13

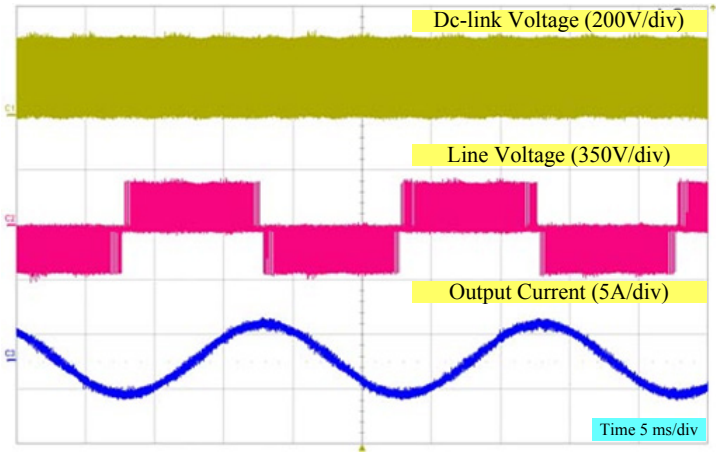


Fig. 5.12. Experimental dc-link voltage, line voltage and output current of TL Z-source inverter with $M = 0.85\times 1.15$ and $d_{ST} = 0.15$

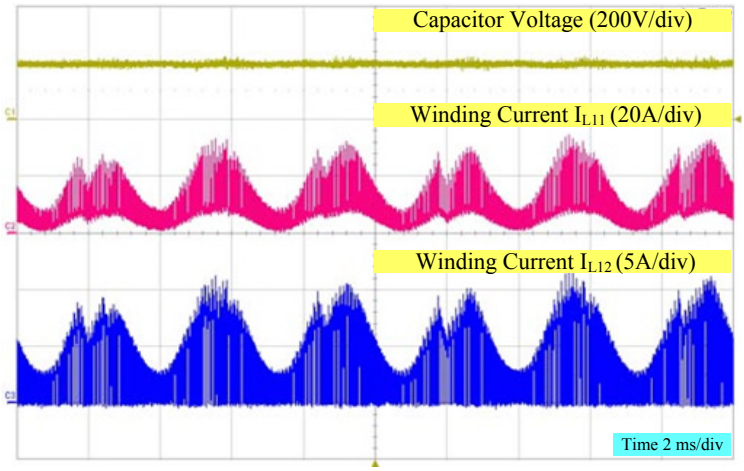


Fig. 5.13 Experimental capacitive voltage, currents through low-voltage and high-voltage windings of TL Z-source inverter with $M = 0.85\times 1.15$ and $d_{ST} = 0.15$.

shows the capacitor voltage and currents through the TL windings. It is observed that the low-voltage winding experiences a high current stress, which is inversely proportional to the TL turns ratio.

5.3. Embedded and DC-Link Embedded Variants

As understood from Section 4.1 on hybrid impedance networks, source locations shown in Fig. 5.2 and Fig. 5.3 for the generalized SL and SC topologies, and Fig. 5.10 for the TL topology are not fixed. Instead, they can be shifted to other places to gain advantages that the embedded and dc-link embedded Z-source inverters have over its conventional precedence [86][87][88][89][95]. This can be illustrated by considering the generalized SL topology drawn in Fig. 5.2 as an example. Conclusions drawn for the SC and TL topologies will be closely similar, and therefore will not be duplicated without compromising understanding.

Referring to Fig. 5.2, the source at S1 can in principle be divided and shifted to positions S2a and S2b, or S3a and S3b for symmetrical placements. Alternatively, it can be shifted

fully without dividing to any of the shown positions for asymmetrical placement. Such shifting will not alter the inverter boost factor and eventual input-to-output voltage gain. Their capacitor voltages are however different, and are respectively represented by (5.8) and (5.9) for the two example shifted cases of the generalized SL inverter shown in Fig. 5.2.

$$V_C = \frac{1+N'd_{ST}}{1-(N'+2)d_{ST}} \frac{V_{dc}}{2} \qquad \text{(Symmetrically placed at S2a and S2b)} \qquad (5.8)$$

$$V_C = \frac{(N'+1)d_{ST}}{1-(N'+2)d_{ST}} V_{dc} \qquad \text{(Placed at either S3a, S3b or both)} \qquad (5.9)$$

Both (5.8) and (5.9) give smaller values than (5.3), which are in agreement with earlier studies for the conventional voltage-type Z-source inverter. Asymmetrical placement of source at only S2a or S2b is also possible, but with two different capacitor voltages produced. The first is given by V_C in (5.3), and the second is given by (5.9). Another consideration to note is the flow of smooth source current when placed at S2a, S2b or both for the conventional Z-source inverter. This advantage is however not shared by the generalized SL topology, whose source current is pulsing with a high instantaneous maximum when the inductors charge in parallel. The instantaneous source current drawn is in fact the highest at positions S3a and S3b, through which charging currents from $2(N' + 1)$ paralleled inductors flow. It might therefore not be as favorable to locate the source at these positions, unlike the conventional Z-source inverter.

5.4. SL versus TL Inverter

The generalized voltage-type SL inverter shown in Fig. 5.2 obviously requires more inductors and diodes if a higher voltage gain is demanded. The same would apply to the generalized current-type SC inverter shown in Fig. 5.3, but since the purpose here is to compare with the TL inverter whose current-type dual does not exist, the SC inverter will not be considered further. Returning back to the SL inverter, its added inductors will always charge in parallel and discharge in series, hence enduring evenly distributed

stresses. Its diodes, on the other hand, will endure different blocking voltages depending on which of the two groups they belong to. For the illustration shown in Fig. 5.2, diodes labeled as D_{3n-1} and D_{3n-2} form one group, while diodes labeled as D_{3n} form the second group. Their respective blocking voltages can be determined, and written together with that for the input diode D in (5.10), which are found to be independent of the source placement.

$$\begin{aligned}
&\text{Diode } D\text{: } V_D = -\hat{v}_i = -\frac{1+N'd_{ST}}{1-(N'+2)d_{ST}}V_{dc} \\
&\text{Diodes } D_{3n-1}, D_{3n-2}\text{: } V_{D1} = -\frac{d_{ST}}{1-(N'+2)d_{ST}}V_{dc} \\
&\text{Diode } D_{3n}\text{: } V_{D2} = -\frac{1-d_{ST}}{1-(N'+2)d_{ST}}V_{dc}
\end{aligned} \tag{5.10}$$

On the contrary, the TL inverter uses lesser components even for significantly raised voltage gain [80]. It relies solely on the turns ratio of the tapped inductor for its voltage boost, and can produce the same gain and capacitor voltage as the generalized SL inverter. This is clear upon comparing (5.3) with (5.7) after setting $N' = \gamma_{TL}$ to get roughly the same number of inductor turns.

However, like most magnetically coupled devices, the TL topology experiences high concentrated current stress at its low-voltage windings L_{11} and L_{21} in Fig. 5.10. This is especially true for the TL inverter since its shoot-through state causes diodes D_{TL3} and D_{TL4} in Fig. 5.10 to block, and hence forcing energy from the high-voltage L_{12} and L_{22} to low-voltage L_{11} and L_{21} windings. The latter thus experiences a surge in instantaneous current. In addition to that, diodes of the TL inverter, although lesser in number, have to block higher voltages, whose expressions are written as:

$$\begin{aligned}
&\text{Diode } D\text{: } V_{D_TL} = V_D \\
&\text{Diodes } D_{TL1}, D_{TL2}\text{: } V_{D1_TL} = -\frac{\gamma_{TL}d_{ST}}{1-(\gamma_{TL}+2)d_{ST}}V_{dc} \\
&\text{Diodes } D_{TL3}, D_{TL4}\text{: } V_{D2_TL} = -\frac{\gamma_{TL}(1-d_{ST})}{1-(\gamma_{TL}+2)d_{ST}}V_{dc}
\end{aligned} \tag{5.11}$$

Equations in (5.11) are found to be independent of the source positions with the last two also found to be γ_{TL} times larger than their correspondences in (5.10). The TL inverter therefore endures high stresses that are concentrated to its much reduced pool of only four diodes. The eventual outcome might be a prominent limitation on its gain if appropriately rated components are not available or too costly.

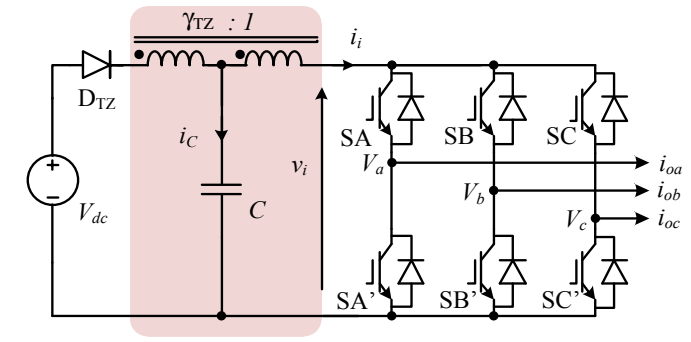
Common to both SL and TL inverters though, their capacitors in the impedance networks are experiencing high stresses according to (5.3) and (5.7) as N' and γ_{TL} increase. Series connection of smaller capacitors is an option for consideration, but its voltage sharing usually varies with internal parameters. The smallest capacitor is also naturally made to endure the highest voltage stress, which might then create a single point of failure. Better sharing techniques are therefore needed and discussed in the following chapter.

5.5. Comparison with Other High-Gain Techniques

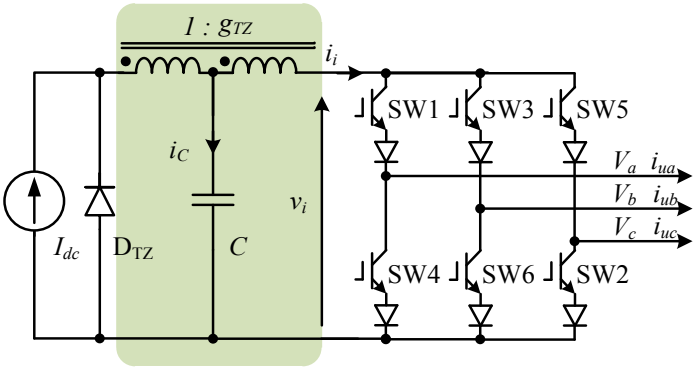
While investigating on the SL, SC and TL techniques, an alternative trans-Z-source technique was reported in the literature [82]. Since it does not involve the cascading of multiple networks, the trans-Z-source technique should appropriately be classified under the non-cascaded category, and will now be compared with those techniques proposed in this thesis. Upon doing so, the non-cascaded techniques will be compared with the alternate-cascading technique to bring forward their respective unique advantages for merging in the next two chapters.

5.5.1. Trans-Z-Source Inverters

The voltage-type trans-Z-source inverter is shown in Fig. 5.14(a), where only a coupled transformer / inductor with turns ratio γ_{TZ}, a capacitor and an input diode are used. It clearly uses much lesser components than the SL and TL topologies, and from [82], its governing equations are given as [82]:



(a)



(b)

Fig. 5.14. Topologies of (a) voltage and (b) current-type trans-Z-source inverters.

$$V_C = \frac{1-d_{ST}}{1-(\gamma_{TZ}+1)d_{ST}} V_{dc}$$

$$\hat{v}_i = \frac{1}{1-(\gamma_{TZ}+1)d_{ST}} V_{dc}$$

$$\hat{v}_{ac} = \frac{M}{1-(\gamma_{TZ}+1)d_{ST}} \frac{V_{dc}}{2} \tag{5.12}$$

To make (5.12) share the same denominator as (5.3) and (5.7) derived earlier for the SL and TL inverters, respectively, γ_{TZ} must be set equal to $N + 1$ or $\gamma_{TL} + 1$, which means a larger turn ratio for the trans-Z-source inverter. Even after the equalization, gain produced by the trans-Z-source inverter is lower by a factor of $\{1 + (\gamma_{TZ} - 1)d_{ST}\}$, which can further be simplified to:

$$1 + (\gamma_{TZ} - 1)d_{ST} < 1 + \frac{\gamma_{TZ}-1}{\gamma_{TZ}+1} < 2 \quad \text{since} \quad d_{ST} < 1/(\gamma_{TZ} + 1) \tag{5.13}$$

Equation (5.13) explains that the reduction in gain for the trans-Z-source inverter is usually less than half since the shoot-through time is rarely close to its upper limit of $1/(\gamma_{TZ}+1)$. This reduction is hence easily overridden by its much lower component count, even though its turn ratio is higher. The trans-Z-source topology is therefore an attractive alternative if higher stresses can be tolerated by its input diode and low-voltage winding. For the former, it experiences a high blocking voltage during shoot-through given by:

$$V_{D\_TZ} = -\frac{\gamma_{TZ}}{1-(\gamma_{TZ}+1)d_{ST}}V_{dc} \tag{5.14}$$

which is higher than those of the TL inverter and much higher than those of the generalized SL inverter listed in (5.11) and (5.10), respectively. The low-voltage winding of the trans-Z-source topology also experiences a surge in instantaneous current when entering the shoot-through state. During that time interval, input diode D_{TZ} blocks naturally, causing energy from the high-voltage winding to be transferred to the low-voltage winding, whose current surges instantaneously. Therefore, as per the TL inverter, the trans-Z-source inverter reduces its component count by "squeezing" higher stresses to its remaining components.

Unlike the TL inverter though, current-type trans-Z-source inverter exists, and is represented in Fig. 5.14(b). Its operating principles are based on transformer coupling, which is different from the multiple-capacitor approach demonstrated by the generalized SC topology. Despite this fundamental difference, features discussed earlier for the voltage-type inverters are still valid here. That means the current-type trans-Z-source inverter still produces a gain that is $\{1+(\gamma_{TZ}-1)d_{OC}\}$ times smaller than its SC companion. Its stresses are also concentrated to only a few remaining components.

5.5.2. Alternate-Cascaded Topology

The discussions above have clarified that the generalized SL and SC inverters produce the highest gains and have better spread of stresses among their components. Spreading of stresses however does not happen with capacitors C_1 and C_2 drawn in Fig. 5.2 for the SL topology, and inductors L_1 and L_2 in Fig. 5.3 for the SC topology. According to (5.3) and (5.4), the mentioned capacitors and inductors must withstand high voltages and currents, respectively, as the number of generic cells N' increases. They should therefore be implemented using higher rated components or series-parallel combinations of lower rated components.

Unfortunately, for series connection of capacitors in the SL topology, voltage sharing varies with internal parameters with the smallest capacitance enduring the largest voltage drop. It is therefore not as attractive as the alternate-cascaded Z-source inverter shown in Fig. 4.6, where according to expressions derived in Section 4.2.1 [95], better balances voltages among the capacitors, inductors and diodes. Instead of alternate-cascading, the dc-link-cascading technique can also be considered, but is not recommended here because of its high inductor and diode counts, which would further worsen the already high component counts of the non-cascaded inverters.

Referring now to the gain of the alternate-cascaded inverter listed in (4.5), it is noted to be the same as that of the voltage-type trans-Z-source inverter, but lower than those of the SL and TL inverters. That means the same as (5.12) after replacing γ_{TZ} with the number of networks in cascade N. To produce the same denominator as in (5.3) and (5.7) for the SL and TL topologies, respectively, N should correspondingly be set equal to $N' + 1 = \gamma_{TL} + 1$. That gives $N + 1 = N' + 2$ inductors for the alternate-cascaded topology, and $2 \times (N' + 1)$ inductors for the SL topology. The former uses N' lesser inductors, and is therefore more attractive if its gain reduction of usually lesser than half is acceptable. Performing the same comparison for the current-type generalized SC inverter is unfortunately not possible here since the alternate-cascading technique does not apply to

the current-type inverter.

5.6. Performance Comparison in Simulation

Simulations in Matlab/Simulink were performed for the four variants of voltage-type Z-source inverters compared in Sections 5.4 and 5.5. Input voltage to each inverter was set to 100 V for eventually powering a three-phase ac RL load of 20 Ω and 5 mH. The same modulation scheme in Section 2.4.3, and control parameters of $d_{ST} = 0.15$ and $M = 0.8 \times 1.15$ were used for all four cases with their results shown from Fig. 5.15 to Fig. 5.18. Observations noted from these figures are summarized, as follows.

- Peak dc-link voltages of the SL (Fig. 5.15) and TL (Fig. 5.16) inverters are higher than those of the trans-Z-source (Fig. 5.17) and alternate-cascaded (Fig. 5.18) topologies even after setting $N = N' + 1 = \gamma_{TL} + 1 = \gamma_{TZ} = 3$ to equalize their denominators in (5.3), (5.7), (5.12) and (4.5), respectively. The amount higher is less than twice, as predicted from (5.13).

- The single diode found in the trans-Z-source inverter (Fig. 5.17) has to sustain the highest reverse voltage. Blocking voltages of the diodes in the TL inverter (Fig. 5.16) are also comparably higher than the SL (Fig. 5.15) and alternate-cascaded inverters (Fig. 5.18).

- Low-voltage windings of the TL (Fig. 5.16) and trans-Z-source (Fig. 5.17) inverters are observed to carry high instantaneous currents caused by the interruptions of their companion high-voltage windings.

- Capacitor and diode voltages of the alternate-cascaded topology (Fig. 5.18) are comparably lower, allowing more lower-rated components to be used if higher-rated ones are not obtainable.

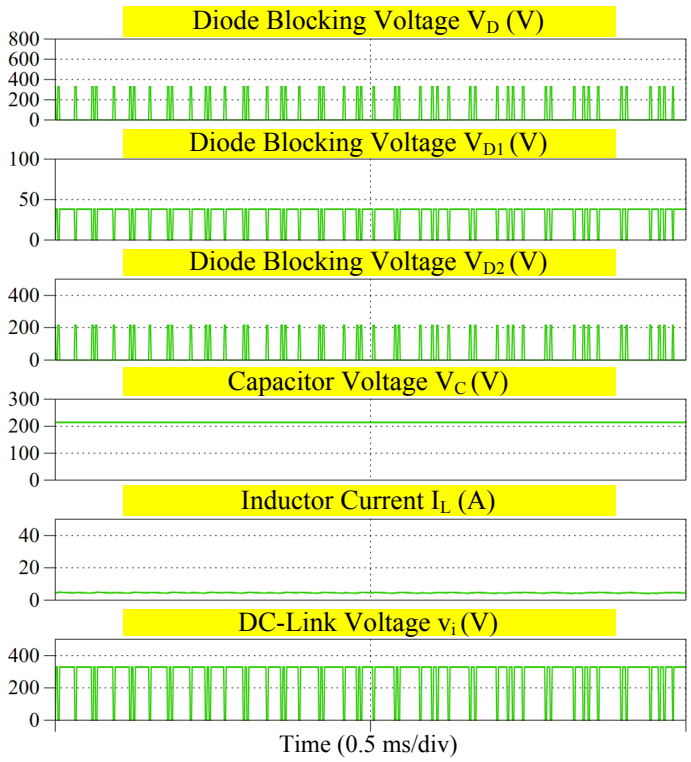


Fig. 5.15. Simulation results obtained for generalized SL Z-source inverter (see Fig. 5.2).

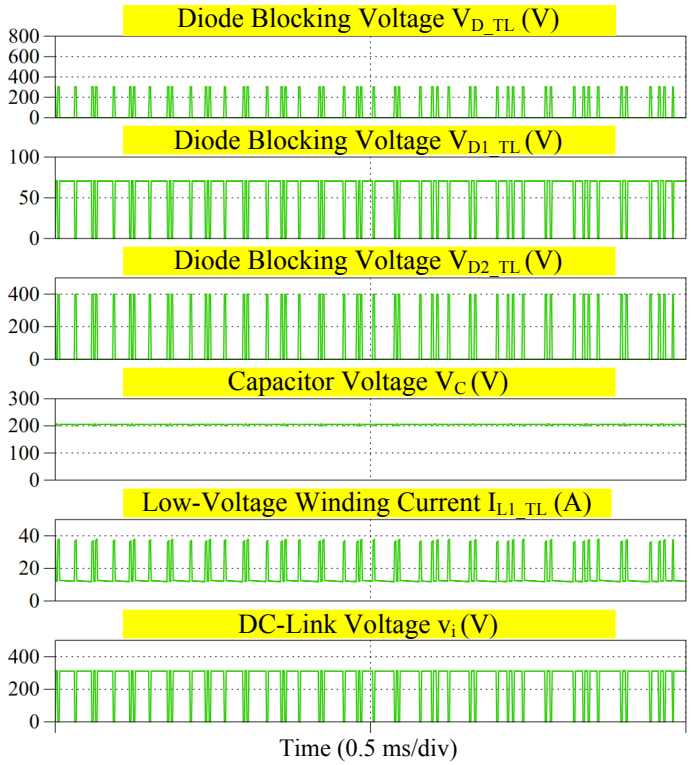


Fig. 5.16. Simulation results obtained for TL Z-source inverter (see Fig. 5.10).

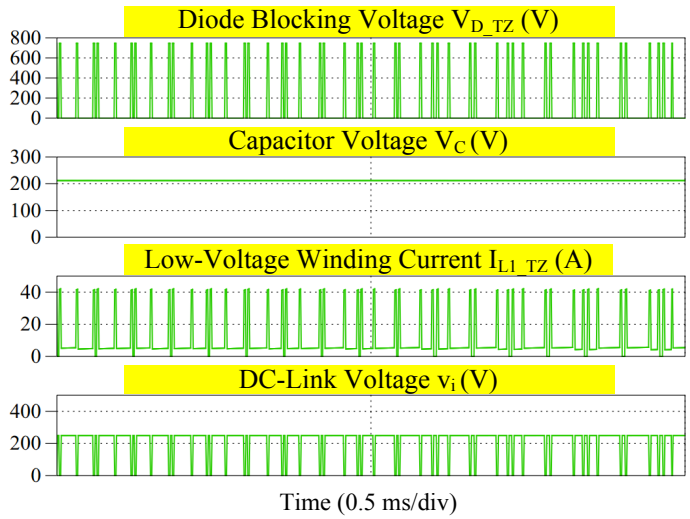


Fig. 5.17. Simulation results obtained for trans-Z-source inverter (see Fig. 5.14(a)).

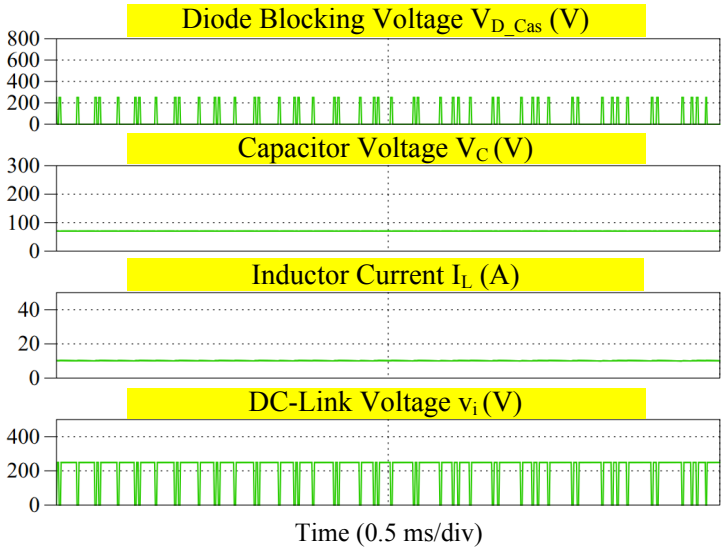


Fig. 5.18. Simulation results obtained for alternate-cascaded Z-source inverter (see Fig. 4.6).

These observations are in agreement with earlier predictions, and have demonstrated the higher gain of the generalized SL Z-source inverter, while not over-stressing most of its components. Similar observations would be applicable to the generalized SC inverter even though its comparison with the other techniques is not possible because of non-existent or different operating principles, as highlighted in Sections 5.4 and 5.5.

5.7. Summary

From understanding the elementary SL topology, the generalized SL and SC Z-source inverters are derived. Their operating principles are explained with their gains proven to be much higher than those of the conventional Z-source inverters. To reduce the number of components while not compromising gain, the TL Z-source inverter is proposed. Unlike the SL method, only voltage-type inverter can be created using the TL method. Comparison between the SC and TL methods is therefore not realistic since the former uses a current-type inverter for its operation. On the other hand, comparison between the SL and TL topologies reveals that they produce the same enhanced gain if their inductor turns are set roughly equal. Voltage and current stresses experienced by components within the TL networks are however much higher.

Comparisons are next performed with the trans-Z-source and alternate-cascading techniques, where it is shown that gains produced by the SL and TL inverters are higher, but usually less than double. Stresses endured by them are also much lower than within the trans-Z-source network, except for their capacitive voltages which can get too high if a very high boost is demanded. A better technique to distribute stresses among the components would therefore be the alternate-cascading technique. These findings have already been verified in theories, simulations and experiments.

Chapter 6 Enhanced Z-Source Inverters – Integrated Techniques

A conclusion drawn from Chapter 5 is that most, if not all, non-cascaded techniques share the common complexity of uneven stress distribution within their impedance networks. Better stress distribution can be achieved by the cascading techniques, whose gains might not be as high. A thought then is to combine their operating traits and advantages to create a few integrated techniques that can raise the gains of Z-source inverters, while not overstressing their components. These are important features that should preferably be in coexistence, and not compromised for practical renewable energy systems.

In total, three integrated techniques are presented with each having its own compromised advantages and disadvantages. Two techniques are presented here, while the third technique is presented in the next chapter. This division is deemed as appropriate since the first two techniques result in the same higher gain and use the same number of capacitors. In contrast, the third technique produces a lower gain but still higher than that of a conventional Z-source inverter. It uses half the number of capacitors, and is therefore a more economical compromise if lower gain is acceptable.

Regardless of their division, all techniques rely on the alternate-cascading technique, rather than the dc-link-cascading technique, to keep their component counts low. Dependent on alternate-cascading also helps to create inverters without direct series connection, and hence avoids unbalanced voltage sharing problem across components and losses linked to balancing circuits. Reliabilities of the inverters are therefore higher, which together with their higher gains, make them suitable alternatives for renewable energy systems.

6.1. Overview of Non-Cascaded Concepts

Non-cascaded concepts developed in Chapter 5 can broadly be summarized in Fig. 6.1, where an X-shaped impedance network tied to a VSI bridge is shown. Similar representation can be done for current-type inverter, but is not attempted here since alternate-cascading, to be discussed in this chapter, is not applicable to current-type inverter. The integrated approaches discussed from the next section onwards are therefore only for voltage-type inverter.

Referring now to Fig. 6.1(a), its non-cascaded impedance network has two generalized inductive blocks, which for conventional voltage-type Z-source inverter, are replaced by single-winding inductors. The same replacement can be performed with the SL and TL modules shown from Fig. 6.1(b) to (d) to develop the SL and TL inverters with higher voltage boost and modulation ratio. Chapter 5 has already discussed them, and has brought out the concern that high voltages and currents will surface at certain components. This however is not the case for the alternate-cascaded Z-source inverter

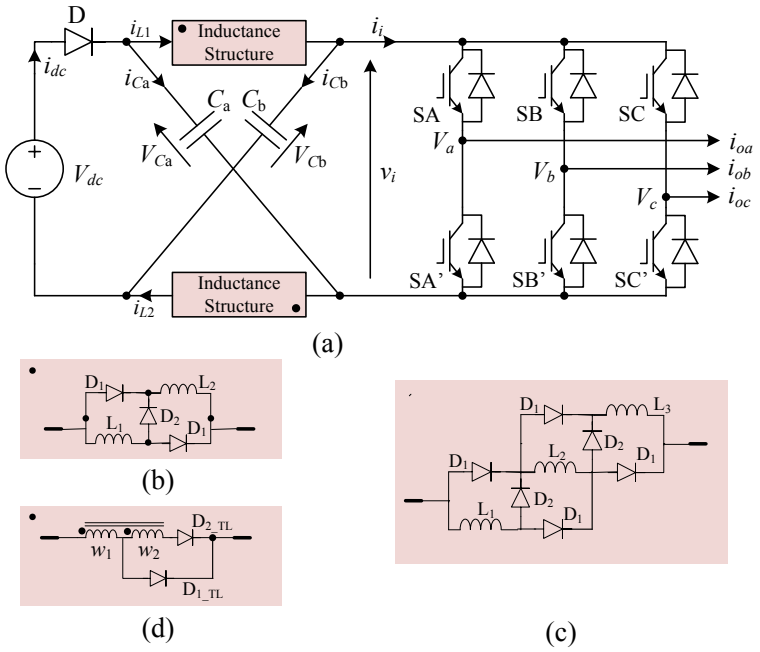


Fig. 6.1. Voltage-type Z-source inverter (a) overall circuit, (b) SL cell with two inductors, (c) SL cell with three inductors and (d) TL cell.

shown in Fig. 4.6, whose stress distribution is more even, but at the expense of a slightly lower gain.

The thought of merging non-cascaded and alternate-cascading techniques to arrive at integrated Z-source inverters with more customized performances might therefore be interesting to explore. This, in fact, is the theme set for the chapter, where alternate cascading is briefly reviewed first to identify a modification needed before effecting the integration.

6.2. Modification to Alternate-Cascading

In Chapter 4 and [95], cascading techniques applied to Z-source inverters for producing higher voltage gains are introduced. Among them, the alternate-cascading technique is more promising since it uses comparably lesser inductors. It is now briefly described before explaining a modification needed to allow the insertion of either SL or TL modules.

6.2.1. Simple Example

Fig. 6.2 shows two conventional Z-source impedance networks with the second flipped vertically. For easier referencing, they are respectively referred to as networks 1 and 2. As seen, the lower inductor of network 1 and the upper inductor of network 2 can be merged to give the alternate-cascaded network shown on the right of the figure. The cascaded network uses one lesser inductor, and for the general case of N networks in cascade, its governing expressions have already been derived and found in (4.5). Equations found in (4.5) are however lower than those in (5.3) and (5.7) for the SL and TL topologies, even after equating their denominators by setting $N = N' + 1 = \gamma_{TL} + 1$.

Besides lower gain, the alternate-cascaded inverter requires more capacitors ($2N$ in total) than the SL and TL topologies. These capacitors, as understood from comparing (4.5) with (5.3) and (5.7), sustain voltages that are N times smaller with no (or minimal)

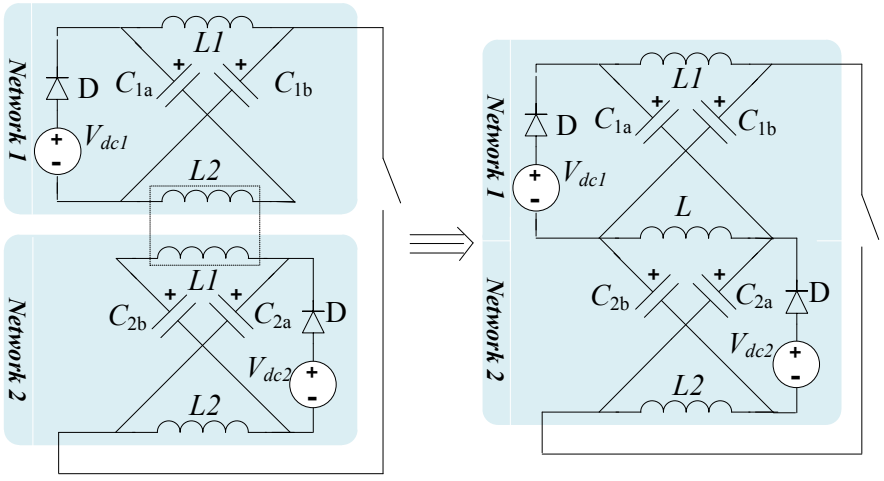


Fig. 6.2. Alternate-cascading technique illustrated with two networks.

sharing problems expected, unlike direct series connection. That means proportionally lower rated capacitors can be used for better stress distribution or simply when higher rated ones are not available. Other components like its input diodes are also not experiencing higher stresses. Alternate-cascading is thus an effective technique for distributing stresses at a higher boost level.

Referring again to Fig. 6.2 where two sources are explicitly shown, it should be noted that their presence are not compulsory. That means if one of them is removed and the other is set to the same total voltage V_{dc}, the same ac output amplitude would be produced, but with asymmetrical distribution of voltages between the networks. For a more reliable and symmetrical distribution, two sources should be used and their values must be set as closely as possible (V_{dc} / 2 if the total voltage is V_{dc}).

6.2.2. Modification Needed

In Chapter 4 where alternate-cascading is discussed, all capacitors are kept similar. That means $C_{1a} = C_{1b} = C_{2a} = C_{2b}$ in Fig. 6.2. This cannot be the case in theory, as demonstrated here through simple charging / discharging circuit analyses. Although its influences on the basic alternate-cascaded inverter shown in Fig. 6.2 are not prominent and thus not strictly necessary, it cannot be ignored when more advanced

alternate-cascaded inverters are dealt with. Relevant details are explained as follows.

Referring to Fig. 6.2 as an example, the appropriate capacitance relation can be derived by considering the shoot-through state. During this period, the uppermost inductor is charged by capacitors C_{1a} and C_{2a}, while the lowermost inductor is charged by C_{1b} and C_{2b}. For the middle inductor, its charging energy is drawn from C_{2a} and C_{1b}, which rightfully should discharge two times more energy than C_{1a} and C_{2b}, if the three inductors are similar. That means C_{2a} and C_{1b} must draw two times more energy from the dc sources during their charging process when in the non-shoot-through state.

Since the charging and discharging paths of all capacitors are the same, doubling of energy to and from C_{2a} and C_{1b} over the same time interval can only be achieved by doubling their capacitances. The proper capacitance relation should therefore be $C_{2a} = C_{1b} = 2C_{1a} = 2C_{2b}$, and not the equal relation read from Chapter 4 and [95].

6.3. Alternate-Cascaded SL Z-Source Inverters.

So far, it has been identified that:

- The SL and TL Z-source inverters produce the same higher gain, but with some of their components stressed by high voltages and currents.
- The alternate-cascaded Z-source inverter produces a lower gain, but has more even distribution of stresses among its components.

It might therefore be of interest to merge different techniques to develop inverters, whose performances lie between boundaries set by the individual techniques. The following explains how the merging can be done for the alternate-cascaded SL Z-source inverters, before the next section continues on the alternate-cascaded TL Z-source inverter.

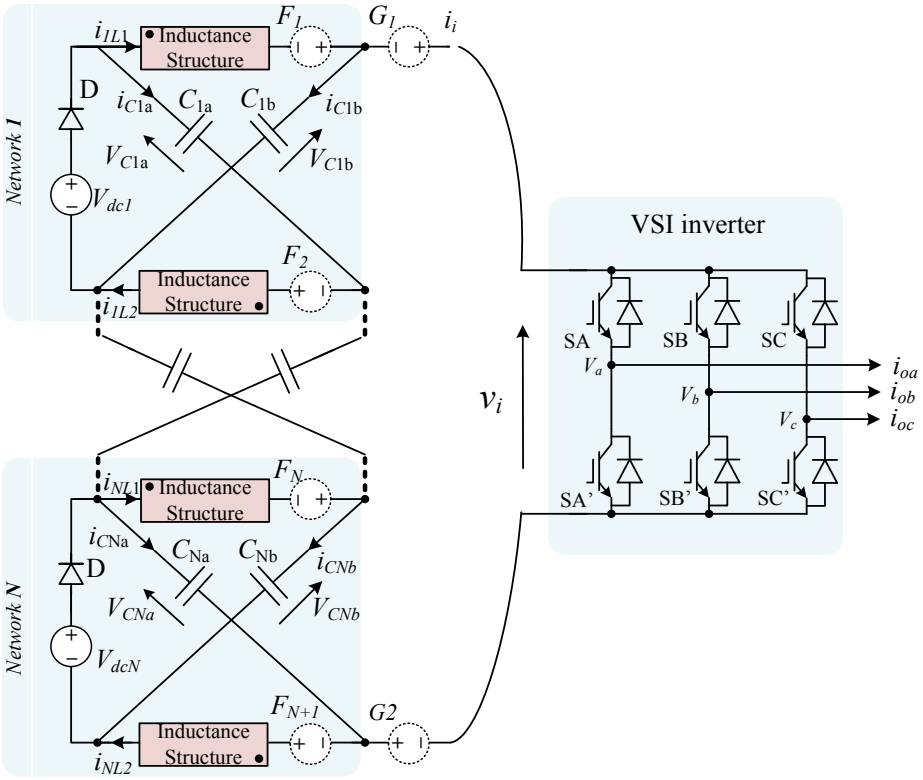


Fig. 6.3. Alternate-cascaded topology with N networks.

Referring to Fig. 6.3, the alternate-cascaded SL Z-source inverter is formed by replacing those inductive blocks shown in the figure with multiple SL modules. If each SL module has N' generic cells (see the lower right corner of Fig. 5.2) and there are N networks in cascade, entering a shoot-through state would cause the $N' + 1$ inductors to charge in parallel with a common voltage given by:

$$v_L = NV_C \tag{6.1}$$

On the contrary, when in a non-shoot-through state, the inductors discharge in series, leading to:

$$v_L = \frac{(V_{dc}/N) - V_C}{N'+1} \tag{6.2}$$

Performing state space averaging on v_L then gives rise to the following expressions for calculating the capacitor voltage V_C, peak dc-link voltage $\hat{v}_i$ during non-shoot-through state and peak ac output voltage $\hat{v}_{ac}$:

$$V_C = \frac{1-d_{ST}}{1-(1+N(N'+1))d_{ST}} \frac{V_{dc}}{N}$$

$$\hat{v}_i = \frac{1+N'd_{ST}}{1-(1+N(N'+1))d_{ST}} V_{dc}$$

$$\hat{v}_{ac} = \frac{1+N'd_{ST}}{1-(1+N(N'+1))d_{ST}} \left(\frac{MV_{dc}}{2}\right) \quad (6.3)$$

Voltage gain can now be flexibly tuned with two control variables N' and N, while yet meeting the imposed component ratings. In the extreme cases of $N' = 0$ and $N = 1$, (6.3) simplifies to (4.5) and (5.3) for representing the alternate-cascading and SL techniques separately.

As mentioned previously, the sources in Fig. 6.3 are neither fixed nor compulsory. They can either be set to zero or shifted to places indicated by symbols F_1 to F_{N+1}, G_1 and G_2 in the figure. Such shifting will not alter the expressions for $\hat{v}_i$ and $\hat{v}_{ac}$ so long as the total input voltage is kept at V_{dc}. It merely results in different capacitor voltages, as demonstrated by the following two examples:

$$V_C = \frac{1+N'd_{ST}}{1-(1+N(N'+1))d_{ST}} \frac{V_{dc}}{N+1}$$

(Sources equally placed at F_1 to F_{N+1}) (6.4)

$$V_C = \frac{(N'+1)d_{ST}}{1-(1+N(N'+1))d_{ST}} \cdot V_{dc}$$

(Sources placed at G_1, G_2 or equally among them) (6.5)

6.4. Alternate-Cascaded TL Z-Source Inverters

Instead of the SL modules, the inductive blocks shown in Fig. 6.3 can be replaced by TL modules to form the alternate-cascaded TL Z-source inverter. When in the shoot-through state, diode D_{1_TL} in each TL cell in Fig. 6.1(d) conducts, while diode D_{2_TL}, together with all D-labeled diodes in Fig. 6.3, blocks. Low-voltage W_1 winding of each TL cell is therefore charged by N capacitors in series, while its companion W_2 winding remains opened. The winding voltages can then be written as:

$$v_{W1} = NV_C$$

$$v_{W2} = \gamma_{TL} v_{W1} = \gamma_{TL} NV_C \quad (6.6)$$

On the other hand, when in the non-shoot-through state, diode D_{1_TL} blocks, while diodes D_{2_TL} and all D-labeled diodes in Fig. 6.3 conducts to give the following winding voltages:

$$v_{W1} = \frac{(V_{dc}/N) - V_C}{\gamma_{TL}+1}$$
$$v_{W2} = \frac{\gamma_{TL}(V_{dc} - V_C)}{\gamma_{TL}+1} \tag{6.7}$$

Averaging the winding voltages to zero per switching period then results in:

$$V_C = \frac{1-d_{ST}}{1-[1+N(\gamma_{TL}+1)]d_{ST}} \frac{V_{dc}}{N}$$
$$\hat{v}_i = \frac{1+\gamma_{TL}d_{ST}}{1-[1+N(\gamma_{TL}+1)]d_{ST}} V_{dc}$$
$$\hat{v}_{ac} = \frac{1+\gamma_{TL}d_{ST}}{1-[1+N(\gamma_{TL}+1)]d_{ST}} \left(\frac{MV_{dc}}{2}\right) \tag{6.8}$$

where two tuning variables represented by the TL turns ratio γ_{TL} and number of networks N in cascade can clearly be seen.

Setting $N = 1$ will reduce (6.8) to the TL expressions in (5.7), while eliminating γ_{TL} (= 0) will simplify it to the alternate-cascaded expressions in (4.5). Equating $\gamma_{TL} = N'$ will also lead to those expressions in (6.3) for representing the alternate-cascaded SL inverter with roughly the same number of winding turns. These cases are mentioned for illustrative purposes only. In general, the control variables should be chosen to produce the demanded gain, while not over-stressing any of the components available for implementing the inverter.

The same analytical approach can be applied to the circuit even when some of its sources are set to zero or shifted to any of the positions indicated in Fig. 6.3. Expressions for $\hat{v}_i$ and $\hat{v}_{ac}$ would remain unchanged so long as the total source voltage is kept at V_{dc}. The only expression expected to change is that for V_C, as illustrated by the following two source-shifting examples:

$$V_C = \frac{1+\gamma_{TL} d_{ST}}{1-[1+N(\gamma_{TL}+1)]d_{ST}} \frac{V_{dc}}{N+1}$$

(Sources equally placed at F_1 to F_{N+1}) (6.9)

$$V_C = \frac{(\gamma_{TL}+1)d_{ST}}{1-[1+N(\gamma_{TL}+1)]d_{ST}} V_{dc}$$

(Sources placed at G_1, G_2 or equally among them) (6.10)

6.5. Performance Comparison in Simulation

The proposed alternate-cascaded SL and TL Z-source inverters were first simulated in Matlab / Simulink for comparison with their non-cascaded correspondences. The same modulation scheme in Section 2.4.3 was used for both inverters, whose other parameters are summarized in Table 6.1 for easier reference.

TABLE 6.1 PARAMETERS USED FOR SIMULATIONS AND EXPERIMENTS

Parameter	Non-Cascaded SL	Alternate-Cascaded SL		Non-Cascaded TL	Alternate-Cascaded TL	
	Simulation	Simulation	Experiment	Simulation	Simulation	Experiment
N	1	2	2	1	2	2
V_{dc1}	NA	50 V	160 V (G2)	NA	50 V	200 V (G2)
V_{dc2}	NA	50 V	0 V	NA	50 V	0 V
Total V_{dc}	100 V	100 V	160 V	100 V	100 V	200 V
γ_{SL} or γ_{TL}	γ_{SL} = 4	γ_{SL} = 2	γ_{SL} = 2	γ_{TL} = 3	γ_{TL} = 1	γ_{TL} = 1
Inductor or Winding L	1.35 mH	1.35 mH	1.35 mH	500 µH	500 µH	500 µH
$C_a = C_b$	220 µF	NA	NA	220 µF	NA	NA
$C_{1b} = 2C_{1a}$ $C_{Na} = 2C_{Nb}$	NA	C_{1a}=220 µF C_{1b}=440 µF	C_{1a}=220 µF C_{1b}=440 µF	NA	C_{1a}=220 µF C_{1b}=440 µF	C_{1a}=220 µF C_{1b}=440 µF
AC Filter L	5 mH	5 mH	5 mH	5 mH	5 mH	5 mH
AC Load R	30 Ω	30 Ω	30 Ω	30 Ω	30 Ω	30 Ω
M	0.9 × 1.15	0.9 × 1.15	0.9 × 1.15	0.9 × 1.15	0.9 × 1.15	0.9 × 1.15
d_{ST} (boost)	0.1	0.1	0.1	0.1	0.1	0.1
d_{ST} (buck)	0	0	0	0	0	0
Modulating Frequency	50 Hz	50 Hz	50 Hz	50 Hz	50 Hz	50 Hz
Carrier Frequency	5 kHz	5 kHz	8.6 kHz	5 kHz	5 kHz	8.6 kHz

6.5.1. Alternate versus Non-Cascaded SL Topologies

The alternate-cascaded SL Z-source inverter was simulated with two networks ($N = 2$) and one generic cell ($N' = 1$) per SL module. Each network was powered by a 50-V dc source placed in series with its input diode, hence giving a total of $V_{dc} = 100$ V for the two networks. The non-cascaded correspondence was simulated with one network and three generic cells per SL module ($\bar{N} = 1$ and $\bar{N}' = 3$, where the bar over each symbol is added to represent the non-cascaded case). Its dc source was set to 100 V, and placed in series with the input diode shown in Fig. 6.1(a). With these circuit parameters decided, the gain equations in (5.3) and (6.3) for the non-cascaded and alternate-cascaded inverters have the same denominators. Boost factor of the alternate-cascaded inverter is however lower at 2.2, as compared to 2.6 for the non-cascaded inverter, if the same control parameters of $d_{ST} = 0.1$ and $M = 0.9 \times 1.15$ are considered.

Using these simulation models and parameters, Fig. 6.4 and Fig. 6.5 show the waveforms obtained for the non-cascaded and alternate-cascaded SL topologies. The

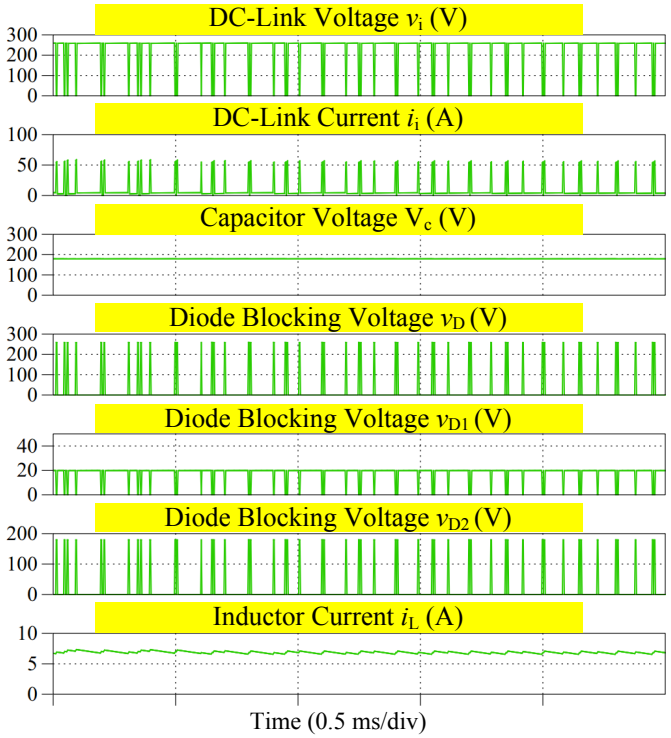


Fig. 6.4. Simulation results obtained for non-cascaded SL Z-source inverter with $\bar{N} = 1$, $\bar{N}' = 3$, $d_{ST} = 0.1$ and $M = 0.9 \times 1.15$.

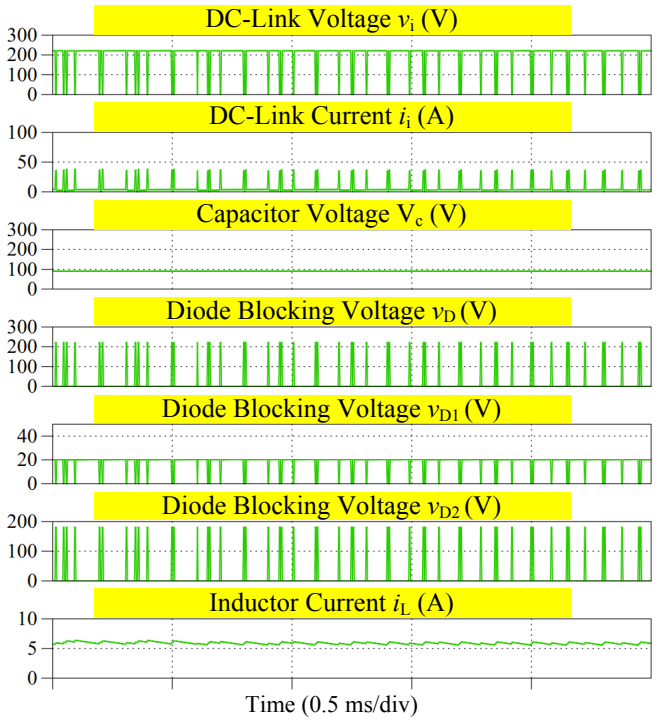


Fig. 6.5. Simulation results obtained for alternate-cascaded SL Z-source inverter with $N = 2$, $N' = 1$, $d_{ST} = 0.1$ and $M = 0.9 \times 1.15$.

displayed waveforms are closely similar except for a lower dc-link voltage of 220 V and a nearly halved capacitor voltage of 90 V experienced by the latter. Corresponding values for the non-cascaded inverter are 260 V and 180 V for the dc-link and capacitor voltages, respectively. The advantage of lower capacitor voltage for the alternate-cascaded inverter is in addition to its requirement for two lesser inductors (six in total compared to eight demanded by the non-cascaded inverter).

6.5.2. Alternate versus Non-Cascaded TL Topologies

Comparison was next performed for the alternate-cascaded and non-cascaded TL Z-source inverters. The alternate-cascaded inverter was realized with two networks ($N = 2$) and a unity turns ratio ($\gamma_{TL} = 1$) for the TL cell shown in Fig. 6.1(d). Each network had a 50-V dc source connected in series with its input diode, hence giving a total V_{dc} of 100 V. On the contrary, the non-cascaded variant was implemented with $\bar{N} = 1$, $\bar{\gamma}_{TL} = 3$ and a dc source of 100 V connected in series with its input diode. Denominators in (5.7) and (6.8) for the two inverters are thus the same. Their ac boost factors are however different,

and are respectively computed as 2.2 for the alternate-cascaded topology and 2.6 for the non-cascaded topology, if the same control parameters of $d_{ST} = 0.1$ and $M = 0.9 \times 1.15$ are considered.

Repeating the simulations then results in Fig. 6.6 and Fig. 6.7, showing waveforms obtained for both topologies. Unlike the SL techniques compared earlier, more advantages are achieved here by alternate-cascading. More precisely, lower voltages now appear across the capacitors, diodes D_{1_TL} and D_{2_TL} in the TL cell, and lower current flows through the W_1 winding of the tapped-inductor after alternate-cascading has been applied. It should however be noted that the dc-link voltage of the alternate-cascaded inverter is raised to a lower value of 220 V, as compared to 260 V of the non-cascaded topology. This is an expected tradeoff since as mentioned earlier, gain of the alternate-cascaded TL inverter is bounded between limits set by the individual techniques.

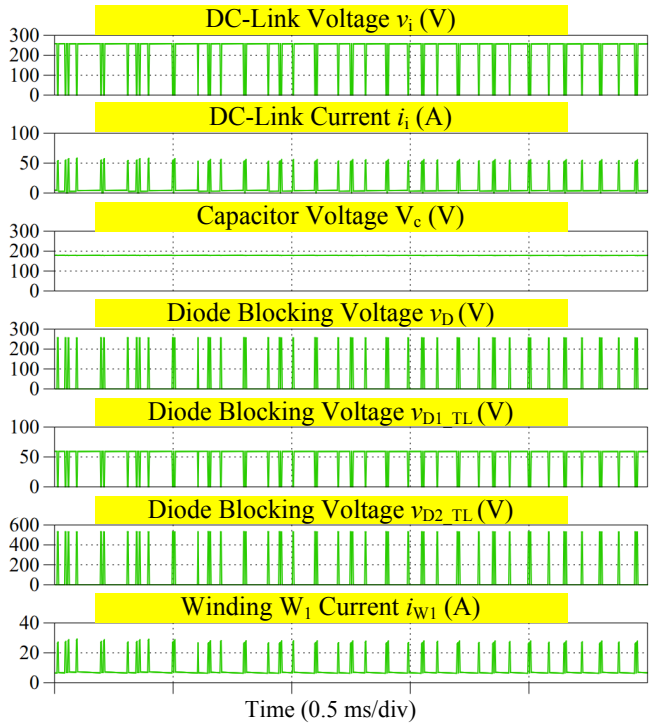


Fig. 6.6. Simulation results obtained for non-cascaded TL Z-source inverter with $\bar{N} = 1$, $\bar{\gamma}_{TL} = 3$, $d_{ST} = 0.1$ and $M = 0.9 \times 1.15$.

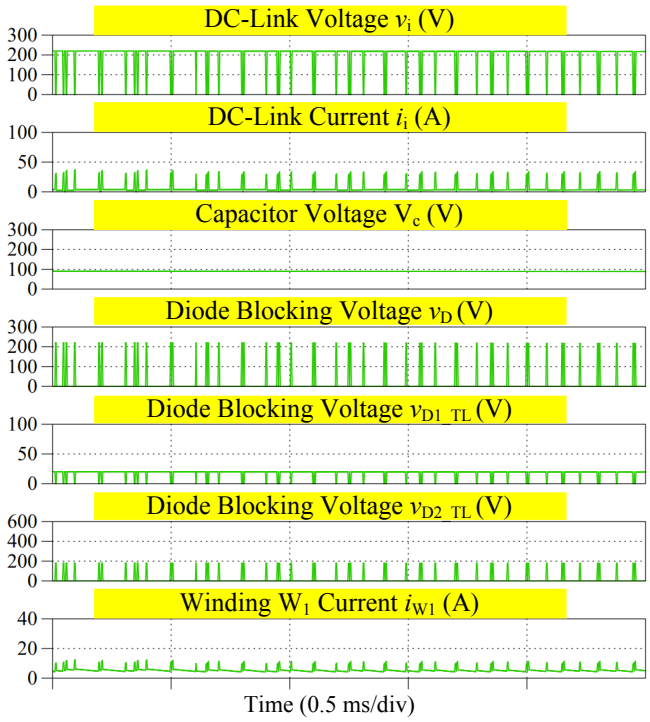
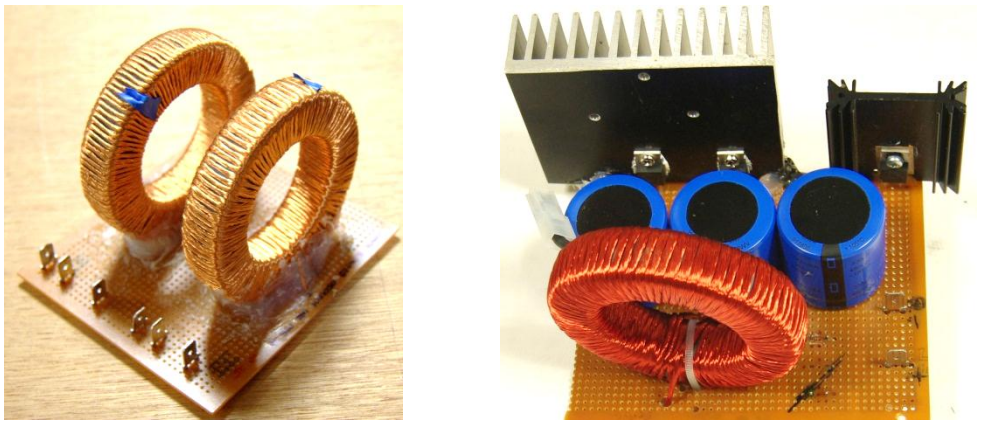


Fig. 6.7. Simulation results obtained for alternate-cascaded TL Z-source inverter with $N = 2$, $\gamma_{TL} = 1$, $d_{ST} = 0.1$ and $M = 0.9 \times 1.15$.

6.6. Experimental Results

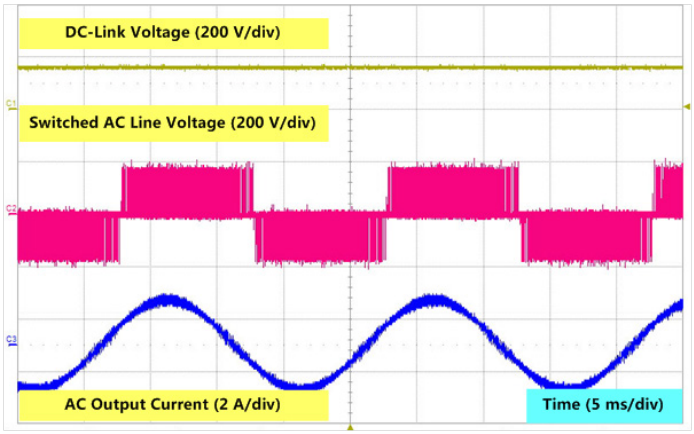
The advantages of the alternate-cascaded SL and TL Z-source inverters have already been clarified with reference to their non-cascaded correspondences. Experimental



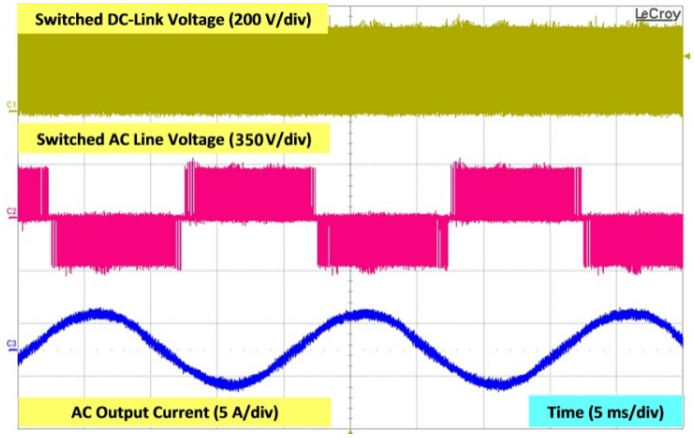
(a) (b)

Fig. 6.8. Inductor cells for alternate-cascaded (a) SL and (b) TL inverters.

results are now presented for validating their practicalities. For the alternate-cascaded SL inverter, two impedance networks and three SL modules with one generic cell each were built, giving rise to $N = 2$ and $N' = 1$. Control parameters used were arbitrarily set as $d_{ST} = 0$ and $M = 0.9 \times 1.15$ for voltage-buck mode, and $d_{ST} = 0.1$ and the same M for voltage-boost mode. The latter gave an anticipated boost factor of $\frac{1+0.1}{1-5\times0.1} = 2.2$. The inductor used in the alternate-cascaded SL and the impedance network cell for alternate-cascaded TL are shown in Fig. 6.8(a) and Fig. 6.8(b). Other system parameters used were kept the same as in the simulations and listed in TABLE 6.1 unless stated otherwise.

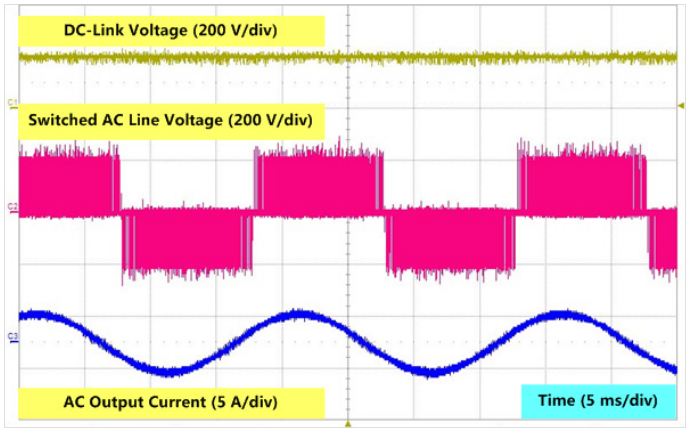


(a)

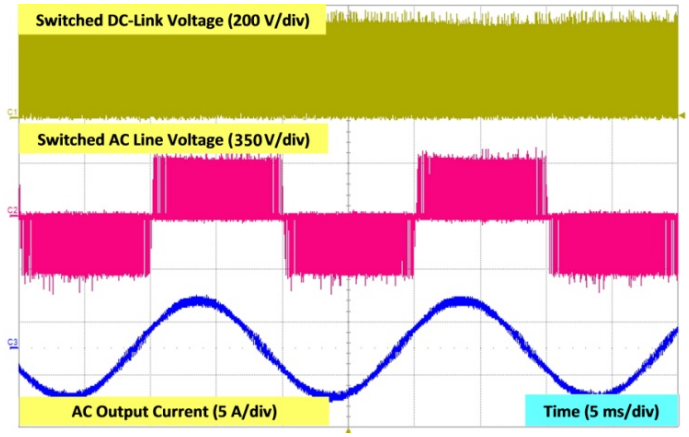


(b)

Fig. 6.9. Experimental results obtained for alternate-cascaded SL Z-source inverter with $N = 2$, $N' = 1$, (a) $d_{ST} = 0$ or (b) $d_{ST} = 0.1$, and $M = 0.9 \times 1.15$.



(a)



(b)

Fig. 6.10. Experimental results obtained for alternate-cascaded TL Z-source inverter with $N = 2$, $\gamma_{TL} = 1$, (a) $d_{ST} = 0$ or (b) $d_{ST} = 0.1$, and $M = 0.9 \times 1.15$.

With the alternate-cascaded SL inverter powered by a dc source of 160 V placed at the dc-link (G2 in Fig. 6.3), Fig. 6.9 shows the captured results. Under voltage-buck mode, the dc-link voltage in Fig. 6.9(a) is not chopped, but remains constant at 160 V, from which an ac peak current of 1.8 A is obtained. When boosted, the dc-link voltage in Fig. 6.9(b) switches between zero and a peak of 320 V. This represents a boost factor of 2, which is close to the computed value of 2.2 after accounting for parasitic losses in a real system. The boosted ac peak current is read as 3.5 A, which again represents a gain close to 2 (ac and dc gains are the same because of the same M used).

The experimental setup was next configured as an alternate-cascaded TL Z-source

inverter with two networks in cascade ($N = 2$) and three 1:1 tapped inductors ($\gamma_{TL} = 1$). Control and system parameters used were kept unchanged, meaning that the same boost factor of 2.2 was anticipated. The inverter was powered from a dc source of 200 V placed at the dc-link (G2 in Fig. 6.3). Results obtained are shown in Fig. 6.10(a) for voltage-buck mode, where the dc-link voltage and ac peak current are read as 200 V and 2.5 A, respectively. This voltage is boosted to 380 V in Fig. 6.10(b), representing a boost factor of 1.9, which is close to the computed value of 2.2. The boosted ac peak current is also read as 5 A, which when divided by the 2.5 A read from Fig. 6.10(a), gives an ac gain of 2 (close to the dc gain because of the same M used).

6.7. Summary

This chapter presents a new family of alternate-cascaded SL and TL Z-source inverters with enhanced voltage-boost in addition to their usual voltage-buck ability. Unlike other Z-source inverters, the inverters proposed here allow voltage gains to be freely set by tuning two control parameters that can also be used to minimize voltage and current stresses endured by their components. Mathematical proofs, simulation and experimental results have demonstrated these advantages, as well as confirmed the practicalities of the inverters.

Chapter 7 Enhanced Boost Z-Source Inverters – Integrated Technique with Lower Component Count

Two integrated techniques for building advanced Z-source inverters are presented in the earlier chapter. They give rise to the maximum possible gain, while not compromising on component stresses. However, their component counts might still be high. To reduce components further, a third integrated technique is proposed, where alternate-cascading and trans-Z-source (earlier named as T-source in [81], but later generalized as trans-Z-source in [82]) techniques are merged. Trans-Z-source technique is a recently proposed boosting technique implemented with a high frequency, magnetically coupled transformer. The amount of boosting obtained can be adjusted by changing the transformer turns ratio instead of adding more components. It is therefore a better way of realizing enhanced boost inverter with lower component count, given too that it requires only one dc-side capacitor. Voltage stress experienced by this single capacitor is however high, which can then create a single point of failure.

To understand the trans-Z-source technique better, its operating features are discussed in Section 7.1, before it is combined with the alternate-cascading technique. Inverters created with this combined third technique are named as alternate-cascaded trans-Z-source inverters. Their gains are slightly lower, which undeniably are tradeoffs for their lower component counts. The overall gains are however still high enough for grid interfacing, meaning that it can an attractive alternative for creating renewable systems with lower costs.

7.1. Trans-Z-Source Inverters

Topologies of the voltage-type trans-Z-source inverters are shown in Fig. 7.1(a) and (b), where the only difference noted between them is their different source placements. This position difference leads to different voltage and current stresses experienced by their

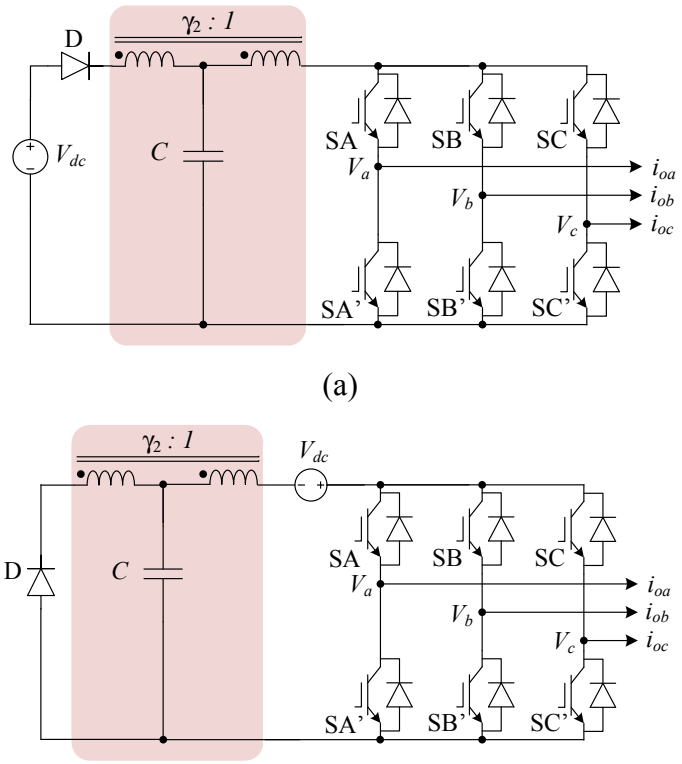


Fig. 7.1. Trans-Z-source inverters with source placed in series with either (a) diode or (b) VSI bridge.

capacitors and input sources, but not their basic gain-boosting principles, which rely heavily on perfect magnetic coupling. That means leakage inductances and parasitic resistances must be small, and coupling coefficient must be high, while meeting the required turns ratio for voltage boosting.

For even higher gain with higher turns ratio, precaution must also be taken to ensure that the transformer windings and components are not over-stressed by high voltages and currents. These concerns can be resolved by introducing alternate-cascading to the trans-Z-source inverters, which must be voltage-type since alternate-cascading does not have a current-type dual. The following therefore reviews the voltage-type trans-Z-source inverters thoroughly to complement those brief descriptions found in Section 5.5.1. Upon understanding them fully, alternate-cascading would be introduced in the next section.

7.1.1. Operating Principles

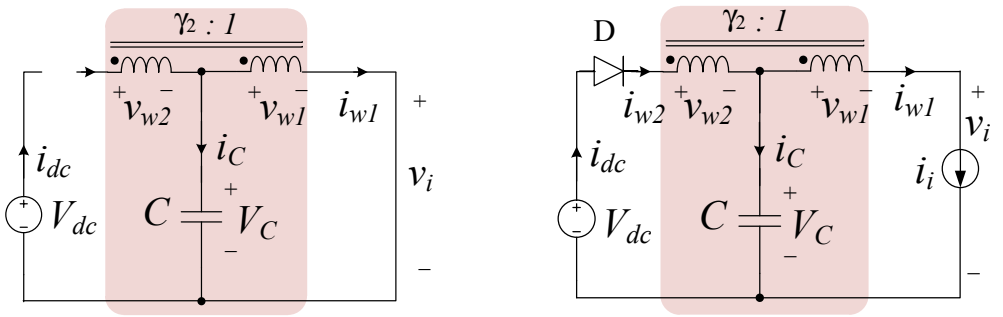
Fig. 7.1 shows two voltage-type trans-Z-source inverters, whose operating principles are closely similar. Because of that, only Fig. 7.1(a) is considered with its operating states shown in Fig. 7.2. In the shoot-through state, the trans-Z-source inverter has two of its switches from the same phase-leg (e.g. *SA* and *SA'* in Fig. 7.1(a)) turned on to create a short circuit. Simultaneously, input diode *D* reverse-biases to form an open circuit. Voltages v_{W1} and v_{W2} across the coupled windings *W1* and *W2* can then be written as:

$$v_{W1} = V_C;\ v_{W2} = \gamma_2 v_{W1} \tag{7.1}$$

where V_C is the capacitor voltage, and γ_2 is the turns ratio of *W2* to *W1*.

Upon removing the short circuit, a non-shoot-through state is entered, whose equivalent circuit is shown in Fig. 7.2(b). Unlike Fig. 7.2(a), the right of Fig. 7.2(b) is replaced by a current source for representing the VSI bridge and external ac load. The value of this current source can either be non-zero when in a traditional VSI active state or zero when in a null state (six active and two null states in total). Also shown in Fig. 7.2(b) is the conduction of input diode *D* to firmly connect the input source V_{dc} to the rest of the circuit. Based on this representation, voltages v_{W1} and v_{W2} can follow up be written as:

$$v_{W1} = v_{W2}/\gamma_2;\ v_{W2} = V_{dc} - V_C \tag{7.2}$$



(a) (b)

Fig. 7.2. Equivalent circuits of Fig. 7.1(a) when in (a) shoot-through and (b) non-shoot-through states.

Since winding voltages per switching period would average to zero, (7.1) and (7.2) can be combined as:

$$d_{ST}V_C + (1 - d_{ST})\,(V_{dc} - V_C)/\gamma_2 = 0 \tag{7.3}$$

where d_{ST} is the fractional shoot-through time. This time is usually kept constant to avoid introducing low-order ripples to the inverter voltages and currents. Simplifying then leads to:

$$V_C = V_{dc}(1 - d_{ST})/(1 - (\gamma_2 + 1)d_{ST}) \tag{7.4}$$

In the non-shoot-through state, the dc-link voltage applied to the load when in an active state is written as $\hat{v}_i = V_C - v_{W1}$, which when substituted by (7.2) and (7.4), leads to:

$$\hat{v}_i = V_{dc}/(1 - (\gamma_2 + 1)d_{ST}) \tag{7.5}$$

This dc-link voltage, when modulated appropriately, gives rise to the following peak ac amplitude $\hat{v}_{ac}$ [82]:

$$\hat{v}_{ac} = M\hat{v}_i/2 = 0.5MV_{dc}/(1 - (\gamma_2 + 1)d_{ST}) \tag{7.6}$$

where M is the modulation index. Noting that the denominator of (7.6) must be greater than zero and the shoot-through state can only replace the traditional null state, d_{ST} and M are restricted by the following inequalities:

$$\begin{aligned} &d_{ST} < 1/(\gamma_2 + 1) \\ &M \leq 1.15(1 - d_{ST}) \end{aligned} \tag{7.7}$$

Assuming that $M = 1.15(1 - d_{ST})$ for producing the greatest voltage boost, (7.6) can be

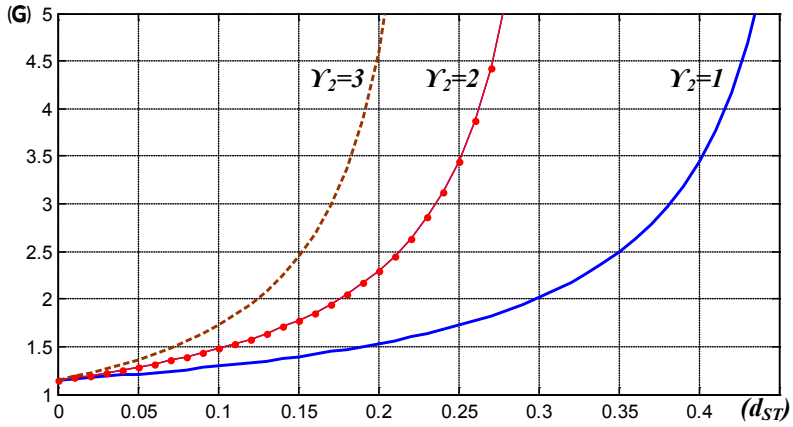


Fig. 7.3. Variations of normalized peak ac voltage $G = \hat{v}_{ac}/(0.5V_{dc})$ with d_{ST} and γ_2.

plotted as in Fig. 7.3 for different d_{ST} and γ_2 values. The demanded voltage gain can clearly be raised by increasing d_{ST} or γ_2. The former means lowering M, which generally is not preferred since it leads to poor dc-link utilization and hence unnecessarily high voltage stresses across components. Increasing γ_2 is therefore a better alternative if the transformer can be designed accordingly, while yet maintaining excellent coupling.

The same averaging process can be applied to the second trans-Z-source circuit drawn in Fig. 7.1(b) with the same voltage expressions in (7.5) and (7.6) produced. Its different source placement mainly leads to a lower capacitor voltage written as:

$$V_C = V_{dc}\gamma_2 d_{ST}/(1-(\gamma_2+1)d_{ST}) \tag{7.8}$$

Since its source is in series with the lower-voltage winding *W1*, the circuit in Fig. 7.1(b) also experiences a higher instantaneous source current, which can either damage the source or demand for a larger low pass filter.

7.1.2. Precautions at Higher Turns Ratio

The main reason for recommending the trans-Z-source circuits is to produce a high voltage boost by simply using a high transformer turns ratio γ_2. As per most transformer circuits, some components would then experience high steady-state voltage or current

stresses depending on the windings to which they are connected. The transformer itself might be tougher to design too with perfect magnetic coupling, low leakage inductances and resistances still being the goals to achieve. Any deviation from perfect coupling will lead to large transient over-voltages caused by breaking of current through *W1* when entering a non-shoot-through null state or current through W2 when entering a shoot-through state. Avoiding the over-voltages would require interrupted energy from one winding to be transferred to the other through perfect coupling. Compactly coupled transformer is therefore a basic necessity for trans-Z-source inverters.

Besides over-voltages, extreme high instantaneous current will flow through winding *W1* and capacitor *C* when in the shoot-through state (not experienced by *W2* and diode *D*). Such high current is caused by the sudden transfer of energy from *W2* to *W1* when the input diode *D* reverse-biased. A simple way to resolve it is to connect multiple capacitors and windings in parallel, which unlike series connection, will not overly complicate the circuit operation in practice. More discussion about multiple components is continued in the following section with both series and parallel connections taken into consideration.

7.2. Alternate-Cascaded Trans-Z-Source Inverters

An alternative way of realizing trans-Z-source inverters with high gains is shown in Fig. 7.4. Instead of a transformer with high turns ratio as in Fig. 7.1(b), multiple smaller

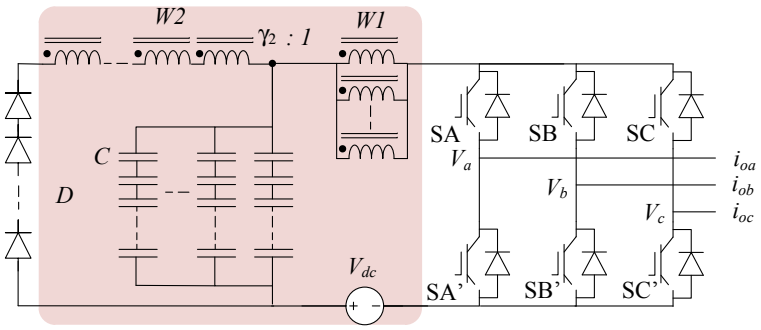


Fig. 7.4. Trans-Z-source inverter realized with multiple transformers having lower turns ratios.

transformers with lower turns ratios are used. Their *W1* windings are connected in parallel to share the extreme high instantaneous current stress, while their *W2* windings are connected in series to form the high voltage demanded. Turns ratios of these smaller transformers should be chosen based on available cores and wire sizes that can more readily produce better coupling. At times, layout and packaging of the application considered might also have a role in deciding the transformer sizes.

Besides transformers, the circuit in Fig. 7.4 shows multiple diodes and capacitors connected in series and parallel instead of using single higher rated entities. Such connections are not strictly necessary, but might at times be needed if higher rated components are not readily available, are too costly or do not fit nicely to the layout of an application (e.g. height of an electrolytic capacitor). When attempting series connection though, it is necessary to be doubly cautious especially for cases where component parameters drifted greatly. With capacitors, it should also be noted that the smallest capacitance endures the highest voltage stress, which might unintentionally create a single point of failure. Balancing resistors for capacitors (and diodes), together with their losses, are therefore almost always added to the circuit for long term usage.

To avoid direct series connection, alternate-cascading is introduced next, but before doing that, the generic trans-Z-source cell shown in Fig. 7.5 is discussed. Unlike Fig. 7.1, the generic cell in Fig. 7.5 has two dc sources labeled as V'_{dc} and V''_{dc}. When they are set

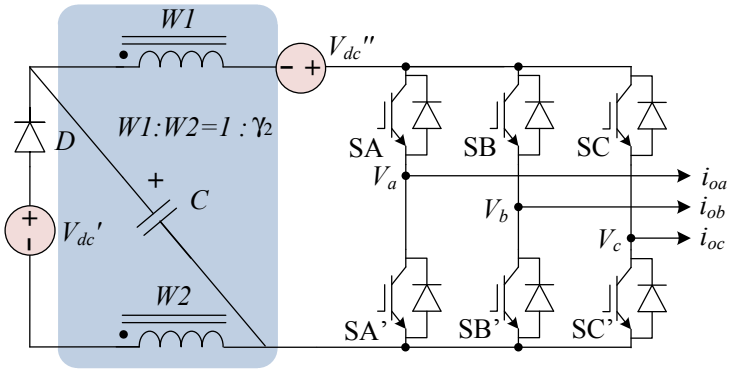


Fig. 7.5. Generic trans-Z-source cell.

as $V'_{dc} = V_{dc}$ and $V''_{dc} = 0$, the network in Fig. 7.1(a) is obtained. Inversely, for $V'_{dc} = 0$ and $V''_{dc} = V_{dc}$, the network in Fig. 7.1(b) is produced. Fig. 7.5 is therefore a generic representation of the two networks shown in Fig. 7.1, and is intentionally drawn with an X-shaped structure that resembles the original Z-source network proposed in [45]. With this X-shaped cell, alternate cascading can be performed based on the following few steps to form the alternate-cascaded trans-Z-source inverter shown in Fig. 7.6:

- Begin with cell 1 with its windings labeled as $W1_1$ and $W2$.
- Duplicate a copy of cell 1, naming it as cell 2 with its windings labeled as $W1_2$ and $W3$, and turns ratio labeled as γ_3.
- Flip cell 2 vertically and place it below cell 1.
- Merge cell 1 and cell 2 with $W2$ of cell 1 replacing $W1_2$ of cell 2.
- Shift $W1_2$ of cell 2 to be in parallel with $W1_1$ of cell 1.
- Duplicate cell k with windings $W1_k$ and Wk, and turn ratio γ_{k+1}.
- Repeat the flipping and merging until all N cells are cascaded (until $k = N$).

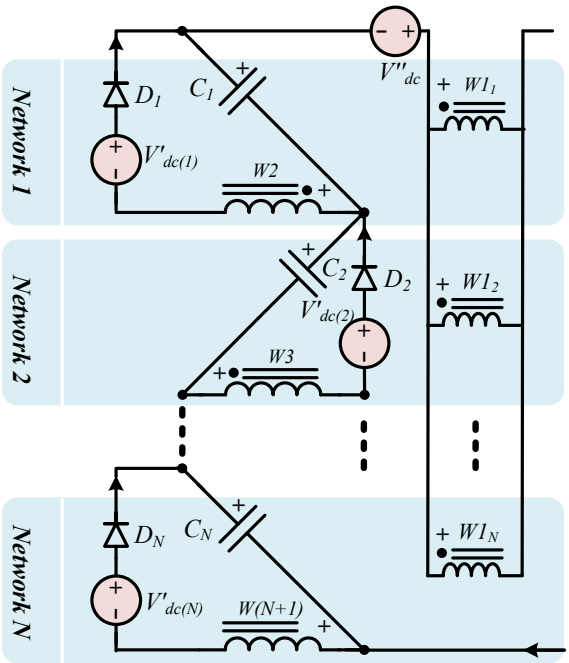


Fig. 7.6. Alternate-cascaded trans-Z-source inverter.

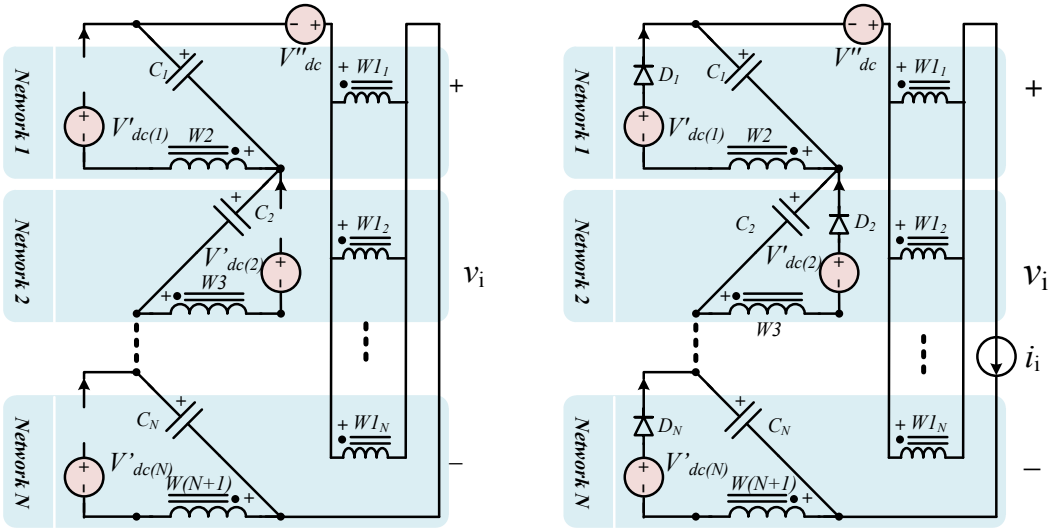


Fig. 7.7. Equivalent circuits of alternate-cascaded trans-Z-source inverter when in (a) shoot-through and (b) non-shoot-through states.

The resulting alternate-cascaded trans-Z-source inverter is shown in Fig. 7.6, which when compared with Fig. 7.4, does not have any direct series connection. The alternate-cascaded trans-Z-source would however still require parallel connections of windings $W1_k$ (k = 1 to N) and capacitors (not shown in Fig. 7.6 for clarity) to manage the flow of high instantaneous current during shoot-through, which in practice, will not be a concern unlike series connections.

Corresponding gain expressions for the alternate-cascaded trans-Z-source inverter can then be determined by analyzing the shoot-through and non-shoot-through states separately, before averaging them to arrive at the final expressions. Beginning with the shoot-through state with the VSI bridge shorted and all diodes reverse-biased (see Fig. 7.7(a)), the governing winding expressions can be written as:

$$v_{W1} = \sum_{\sigma=1}^{N} V_{C\sigma} + V''_{dc}$$

$$v_{W(k+1)} = \gamma_{k+1} v_{W1} \tag{7.9}$$

Their correspondences when in the non-shoot-through state with all diodes conducting

can be written as (see Fig. 7.7(b)):

$$v_{W1} = v_{W(k+1)}/\gamma_{k+1}$$
$$v_{W(k+1)} = V'_{dc(k)} - V_{Ck} \tag{7.10}$$

Averaging (7.9) and (7.10) for each winding then gives:

$$V_{Ck} = \gamma_{k+1} d_{ST} \left(\frac{V'_{dc}+V''_{dc}}{1-(\gamma_T+1)d_{ST}}\right) + V'_{dc(k)}$$
$$\gamma_T = \sum_{\sigma=1}^{N} \gamma_{\sigma+1}$$
$$V'_{dc} = \sum_{\sigma=1}^{N} V'_{dc(k)} \tag{7.11}$$

Considering the non-shoot-through state, the peak dc-link voltage and peak ac voltage amplitude can be written as:

$$\hat{v}_i = \frac{V'_{dc}+V''_{dc}}{1-(\gamma_T+1)d_{ST}}$$
$$\hat{v}_{ac} = M\hat{v}_i/2 = \frac{0.5M(V'_{dc}+V''_{dc})}{1-(\gamma_T+1)d_{ST}}$$
$$d_{ST} < 1/(\gamma_T + 1), \quad M \le 1.15(1 - d_{ST}) \tag{7.12}$$

Note again that Fig. 7.6 is a generic representation of the alternate-cascaded trans-Z-source inverter with all possible source locations shown. These sources can be set to zero, where desired, with only one of them needed to be non-zero for powering the inverter. Considered as an example $V'_{dc(1)} = \cdots = V'_{dc(N)} = 0$ and $V''_{dc} \neq 0$, $\hat{v}_i$ in (7.12) then simplifies to (7.6) except with γ_T replacing γ_2. The circuit in Fig. 7.6 is therefore equivalent to that in Fig. 7.1(b) in terms of overall voltage gain, but can be realized using lower rated components that might be more readily available or fit the layout of an application better. Unlike those uncontrollable distributions of voltages in Fig. 7.4 , the circuit in Fig. 7.6 also realizes more deterministic distributions of voltages across the

diodes and capacitors that have no dependence on their internal parameters, as demonstrated by (7.11).

Instead, they depend solely on the chosen divisions of transformer turns ratio γ_{k+1} and source voltage $V'_{dc(k)}$, which can freely be decided by the designer, depending on the scenario under consideration. (At least a larger capacitance can now be made to share a higher voltage stress unlike in direct series connection). However, the total capacitive voltage stress remains unchanged, and can be determined as:

$$\sum_{\sigma=1}^{N} V_{C\sigma} = \frac{(1-d_{ST})V'_{dc}+\gamma_T d_{ST} V''_{dc}}{1-(\gamma_T+1)d_{ST}} \tag{7.13}$$

where (7.13) clearly simplifies to (7.4) or (7.8), depending on whether V'_{dc} or V''_{dc} is set to zero (not compulsory though).

7.3. Simulation Results

Simulation was performed using the modulation scheme reviewed in Section 2.4.3 with triplen offset added to give a maximum *M* of 1.15. The scheme was originally proposed for the conventional Z-source inverter, but since it produces the same shoot-through and non-shoot-through states, it can surely be used for modulating the alternate-cascaded trans-Z-source inverter without changes. References and carrier of the chosen modulation scheme were then assembled in Matlab / Simulink, and were used to modulate the alternate-cascaded trans-Z-source inverter drawn in PSIM with $N = 2$ (two networks in cascade). Interface between the two software platforms was through Simcoupler from PSIM, and parameters used for the simulation are listed in Table 7.1.

Expected dc and ac gains from (7.12) can conveniently be determined as $1/(1-(\gamma_T+1)d_{ST}) = 2.5$ and $M \times 2.5 = 2.3$ using the indicated turns ratio of $\gamma_{k+1} = 1$ for each transformer, shoot-through duration of $d_{ST} = 0.2$ and modulation ratio of *M*

= 0.8 × 1.15. From (7.11), the capacitor voltages can also be computed as V_{C1} = 240 V and V_{C2} = 80 V.

TABLE 7.1. SIMULATION AND EXPERIMENTAL PARAMETERS

Parameter	Simulation	Experiment
N	2	2
$V'_{dc(1)}$	160 V	160 V
$V'_{dc(2)}$	0 V	0 V
V'_{dc}	160 + 0 = 160 V	160 + 0 = 160 V
V''_{dc}	0 V	0 V
$\gamma_2 = \gamma_3$	1	1
γ_T	1 + 1 = 2	1 + 1 = 2
Coupling Coefficient	1	0.99
Winding L	250 μH	143 μH
$C_1 = C_2$	660 μF	660 μF
AC Filter L	10 mH	10 mH
AC Load R	30 Ω	30 Ω
M	0.8×1.15	0.8×1.15
d_{ST} (boost)	0.2	0.2
d_{ST} (buck)	0	0
Modulating frequency	50 Hz	50 Hz
Carrier frequency	5 kHz	8.3 kHz

The expected dc gain and capacitor voltages are verified in Fig. 7.8, where the first three traces clearly show values of $2.5(V'_{dc} + V''_{dc}) = 400$V, 240 V and 80 V, respectively. Currents flowing through windings $W1_1$, $W2$ and $W3$ are also shown. They are respectively indicated as $i_{W1(1)}$, i_{W2} and i_{W3}, whose instantaneous peaks are 15 A, 12 A and 12 A. Current flowing through the second low-voltage winding $W1_2$ shares the same wave pattern as $i_{W1(1)}$, hence giving a total peak current of 30 A for i_{W1} when it is in the shoot-through state.

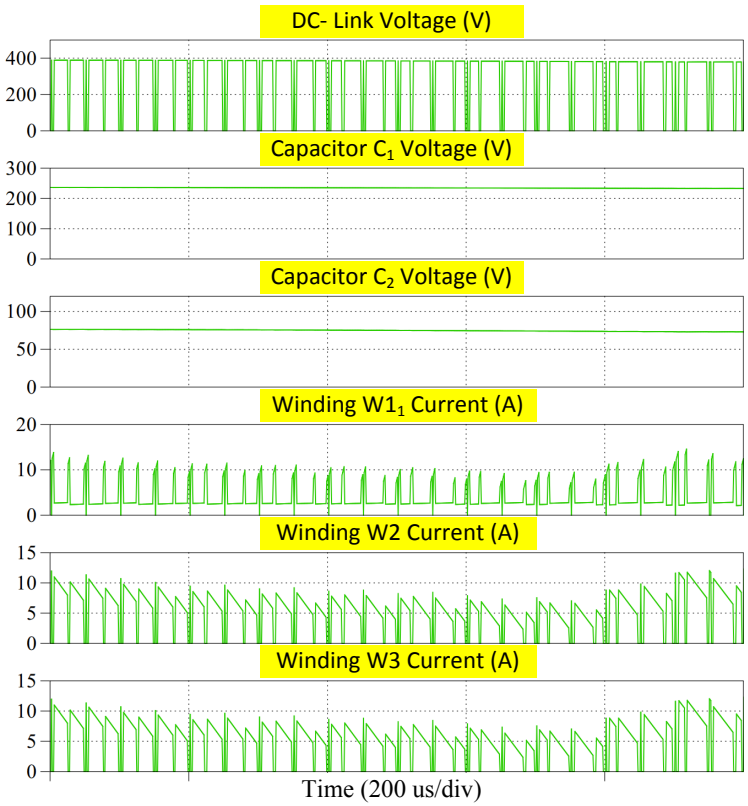


Fig. 7.8. Simulated dc-link voltage v_i, capacitor voltages V_{C1} and V_{C2}, winding currents $i_{W1(1)}$, i_{W2} and i_{W3}.

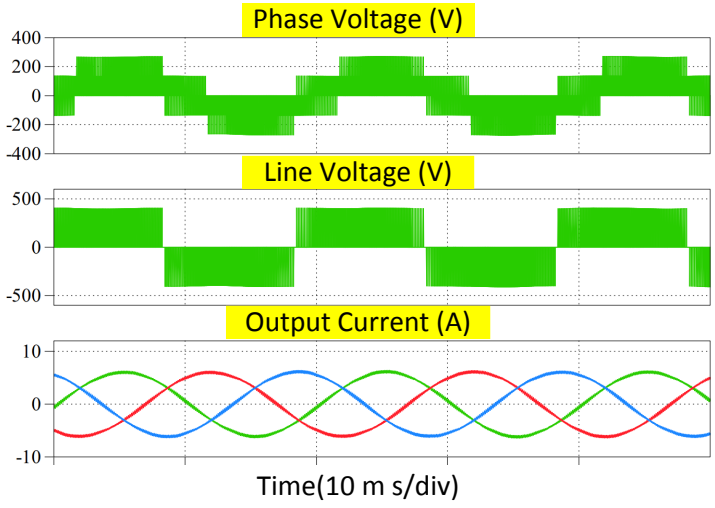


Fig. 7.9. Simulated ac unfiltered phase voltage v_a, unfiltered line voltage v_{ab} and three-phase filtered current.

Peak currents of *W2* and *W3*, on the other hand, flow during the non-shoot-through state to re-charge their corresponding capacitors. Together, these dc quantities give rise to those ac waveforms shown in Fig. 7.9. The sensed peak current of 6 A in the figure is noted to agree well with its computed value of $\frac{MB\times V_{dc}/2}{|Z|} = \frac{2.3\times 160}{2\times\sqrt{30^2+(100\pi\times 0.01)^2}} = 6.1$ A, where Z is the load impedance.

7.4. Experimental Setup and Results

The alternate-cascaded trans-Z-source inverter shown in Fig. 7.6 was constructed in the laboratory using the parameters listed in Table 7.1. Its modulation scheme with triplen offset added was realized using an external modulator with discrete comparator chips. All circuit components, especially the coupled transformers, were placed as close as possible to minimize imperfections that can lead to huge spikes in the switched voltages. Being important, details of the transformers are given first before describing the experimental results.

7.4.1. Coupled Transformer Design

The coupled transformers were wound on *C055866A2* cores with 142 nH/T^2 (T stands for turn) from *Magnetics*. The wire size chosen was AWG32 with a resistance of 0.537 Ω/m. Forty-four strings with 18 m each were then twisted by a handheld drilling machine to raise the current-carrying capability of the windings without significantly increasing skin and proximity effects. Note that where possible, Litz wire should be used since it follows a more carefully prescribed pattern with better equalization of length over which each strand is at the surface of the wire. The twisted wire was then divided into two and wound like in a bifilar coil (also called bifilar winding), where two closely

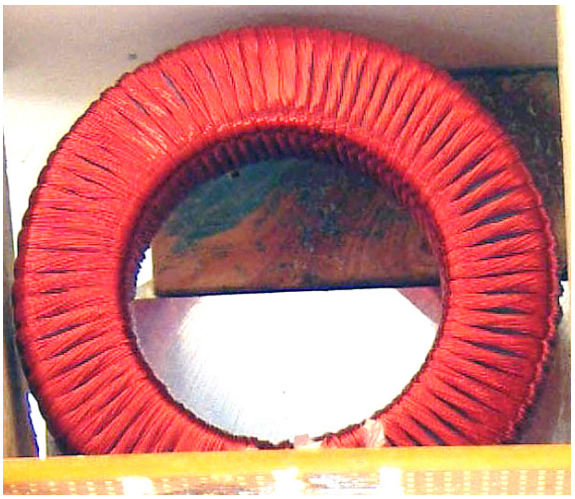


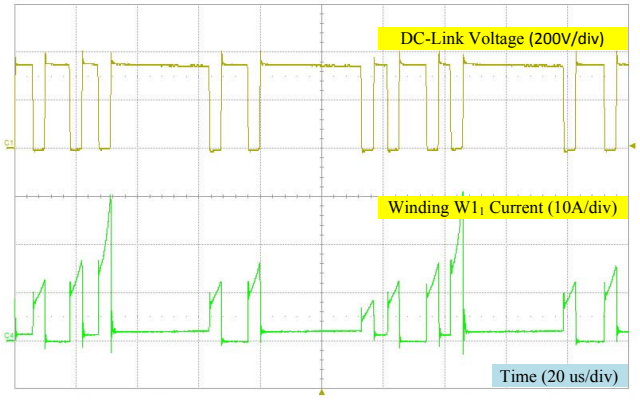
Fig. 7.10. Illustration of coupled transformer.

spaced, parallel windings were wound on the core [21]. The eventual transformer built is shown in Fig. 7.10 for illustration.

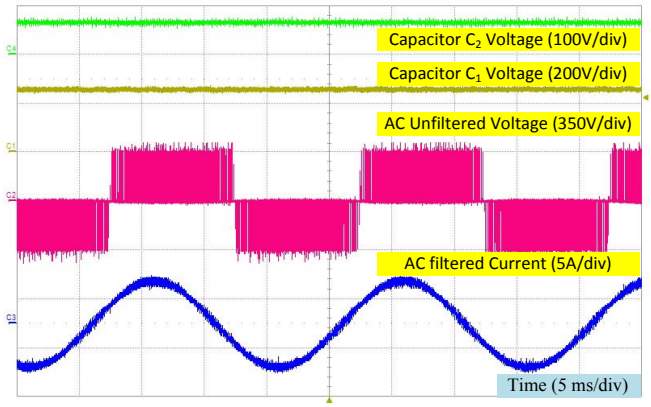
In total, each winding has thirty-one turns, which gives a computed total inductance of $L_{T(c)} = 31^2 \times 142 \times 10^{-6} = 0.136$ mH and a total resistance of $R_{T(c)} = 0.537 \times 1.8 / 44 = 0.022$ Ω per winding. These values were compared with measurements taken with an RLC meter, which read $L_{T(m)} = 0.145$ mH and $R_{T(m)} = 0.03$ Ω per winding. The series aiding inductance was also measured as $L_{aid} = 0.577$ mH, which was subsequently used to calculate the mutual inductance $L_M = (L_{aid} - 2L_T) / 2 = 0.1435$ mH and coupling coefficient $k = L_M / L_T = 0.990$. Such high coupling close to unity and low wire resistance helped to minimize transient over-voltages caused by winding current interruptions during the testing.

7.4.2. Experimental Results

Fig. 7.11(a) and (b) show the experimental dc and ac waveforms obtained with $d_{ST} = 0.2$ and $M = 0.8 \times 1.15$. The following summarizes the observed features and explains slight mismatches.



(a)



(b)

Fig. 7.11. Experimental (a) dc-link voltage v_i, winding current $i_{W1(1)}$, (b) capacitor voltages V_{C1} and V_{C2}, ac unfiltered line voltage v_{ab} and filtered current i_{oa}.

- Peak dc-link voltage measured during non-shoot-through state is 360 V, which when divided by the input of 160 V, gives a dc gain of 2.25. This value is slightly lower than the simulated gain of 2.5, which is caused by semiconductor and wire parasitic not modeled in simulation.
- The current through $W1_{(1)}$ is zero when in the non-shoot-through null state.
- DC-link voltage drops to zero, while the current through $W1_{(1)}$ surges instantaneously to a high value of 30 A when it is in the shoot-through state. This current value is already halved by the parallel winding connection, but it is still higher than that observed in simulation. The reason is likely due to imperfect semiconductor switching, which has not been modeled in simulation.

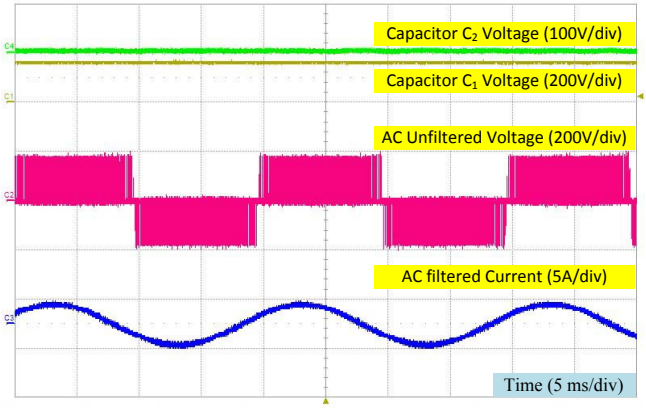


Fig. 7.12. Experimental measured dc capacitor voltages V_{C1} and V_{C2}, ac unfiltered line voltage v_{ab} and filtered current i_{oa}.

- Currents through windings *W2* and *W3* are not shown because they are not accessible from the compactly packed setup with *W2* and *W3* each placed closely between a capacitor and a diode (see Fig. 7.6 for schematic).
- Capacitor voltages $V_{C1} \approx 240$ V and $V_{C2} \approx 70$ V are noted to be close to those obtained from simulation.
- Measured ac peak current of 5 A is 1 A lesser than that obtained from simulation. The mismatch is due to temperature-related drifting of the load during testing.

For comprehensiveness, waveforms obtained during voltage-buck operation were also captured and shown in Fig. 7.12 with $d_{ST} = 0$ and $M = 0.8 \times 1.15$. Since no shoot-through state was inserted, the dc-link voltage was no different from the input voltage, and therefore not illustrated. Only shown in the figure are the capacitor voltages at $V_{C1} = 160$ V and $V_{C2} = 0$ V. These values are again different, as can be deduced from (7.11) and the source values written in Table 7.1. These dc quantities give rise to an eventual ac peak current of 2.4 A, which agrees well with the computed value of $\frac{M \times V_{dc}/2}{|Z|} = \frac{1.15 \times 0.8 \times 160}{2 \times \sqrt{30^2 + (100\pi \times 0.01)^2}} = 2.44$ A.

7.5. Summary

This chapter reviews trans-Z-source inverters, and presents a generic trans-Z-source cell. The generic cell can then be duplicated and alternately cascaded to form various alternate-cascaded trans-Z-source inverters depending on which source units are present. Although the inverters use multiple components to tolerate higher voltage gains, they do not rely on direct serious connections of the components. Common voltage sharing problems that vary randomly with parameters are therefore not experienced by the proposed alternate-cascaded trans-Z-source inverters. Moreover, by using smaller coupled transformers with lower turns ratios, the proposed inverters can better divide instantaneous current stresses experienced per winding. Performances and practicalities of the inverters have already been verified in simulation and experiment.

Chapter 8 Enhanced Boost Photovoltaic Systems

To demonstrate how the earlier proposed enhanced boost topologies can be used for renewable energy harnessing, an example PV system is simulated in this chapter. Only one of the inverters is chosen for demonstration, since application of another is just a straightforward replacement of the inverter topology. Control and modulation of the system remain unchanged, and are in fact the same as those found in a typical PV system. The intention of this chapter is therefore more to provide an example, and not to contribute new concepts.

8.1. PV Characteristics

For the simulation, a model representing the PV characteristics is needed. This model

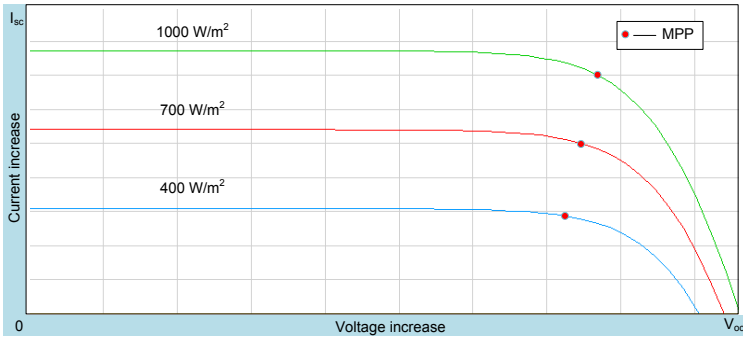


Fig. 8.1 Non-linear I-V curve of PV module.

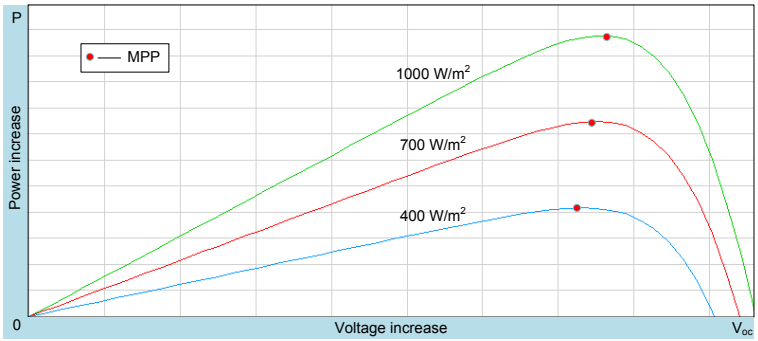


Fig. 8.2 Non-linear P-V curve of PV module.

is described here before moving on to discuss the simulation setup and results.

8.1.1. Nonlinear I-V and P-V characteristics

The nonlinear characteristics of the solar array significantly influence the design of the converter system and its corresponding control scheme. It is therefore necessary to briefly describe the features of the PV array. In general, a PV module converts solar irradiance into dc power directly. The amount of power generated varies with the solar irradiance and temperature. An example illustration of the variation can be found in Fig. 8.1 and Fig. 8.2 under different levels of solar irradiance. Particularly in Fig. 8.1, those highlighted dots on the current-voltage (I-V) curves show the increase in maximum power as the irradiance increases. Although not shown, the maximum power will increase with lower temperature too. It is thus important to implement a MPPT algorithm that can follow the changes in maximum power. To test the developed algorithm, it is also necessary to have a mathematical model of the PV characteristics, which will be described next.

8.1.2. Mathematical Model

A solar cell is effectively a p-n junction, whose equivalent circuit can be found in Fig. 8.3 [98]. The circuit consists of a diode, light-dependent current source and two resistances for representing internal parallel resistance R_p and series resistance R_s. The series resistance should be as low as possible and the shunt resistance should be comparably higher so that most of the generated power can be directed to the externally connected load.

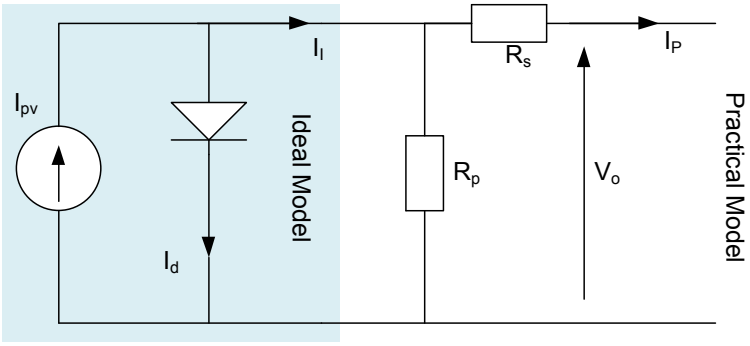


Fig. 8.3 Ideal and practical model of PV cell

For an ideal PV cell, its basic equation derived from relevant semiconductor theories can further be expressed as [98]:

$$I_{I,cell} = I_{pv,cell} - I_{0,cell}\left[exp\left(\frac{qV}{akT}\right) - 1\right] \tag{8.1}$$

$$I_{d,cell} = I_{0,cell}\left[exp\left(\frac{qV}{akT}\right) - 1\right] \tag{8.2}$$

where $I_{pv,cell}$ is the current generated by the incident light (directly proportional to the irradiance), $I_{d,cell}$ is the Schottky diode current, $I_{0,cell}$ is the reverse saturation or leakage current of the diode, q is the electron charge ($1.60217646e^{-19}$ C), k is the Boltzmann constant ($1.3806503 \times 10^{-23}$ J/K), T (in Kelvin) is the temperature of the p–n junction, and a is the diode ideality constant.

Equation (8.1) however does not represent the I-V characteristic of a practical PV array. A practical array is composed of several connected PV cells, whose characteristic at the array terminals must include some additional parameters to the basic equation. The resulting equation is written as follows [98]:

$$I_{P,cell} = I_{pv,cell} - I_{0,cell}\left[exp\left(\frac{V+R_SI}{akT/q}\right) - 1\right] - \frac{V+R_SI}{R_P} \tag{8.3}$$

Cells connected in parallel will in theory increase their total short-circuit current and cells connected in series will contribute a larger total open-circuit voltage. When the array has N_p parallel connected cells, the PV and saturation currents may then be expressed as:

$$I_{pv} = I_{pv,cell} \times N_p, \quad I_0 = I_{0,cell} \times N_p \tag{8.4}$$

Equation (8.3) is the PV model equation used in the simulation for verifying the system performance when conditioned by an enhanced boost Z-source inverter. It can be programmed in Matlab or other software as a current-controlled voltage source or voltage-controlled current source.

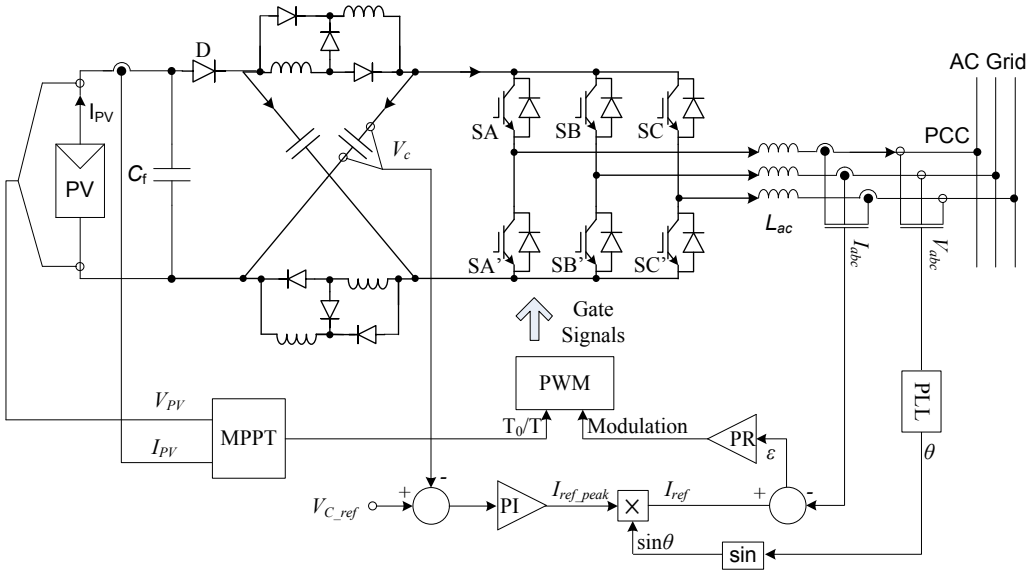


Fig. 8.4 Overall control diagram of grid-tied inverter.

8.2. Simulation of Grid-Tied Non-Cascaded SL PV System

To demonstrate how an enhanced boost Z-source inverter can be used in a PV system, a grid-tied 5-kW PV example is simulated with a non-cascaded multi-cell SL Z-source inverter. The overall schematic is shown in Fig. 8.4. Its control implementation and results are described as follows.

8.2.1. Control Implementation

As per existing practice, the dc-ac inverter bridge is regulated to keep a constant dc-side voltage, which is now chosen as one of the Z-source capacitor voltages [99]. An appropriate constant reference voltage V_{C_ref} is therefore provided for the Z-source capacitor V_C to track. The voltage regulator chosen here is a simple proportional-integral (PI) controller, whose output I_{ref_peak} is the ac active current magnitude to be drawn or supply to the grid. This value is multiplied by a set of three-phase unit sine waves synchronized with the grid voltages V_{abc} by a phase-locked-loop (PLL). The resulting sinusoidal references are tracked by the ac line currents I_{abc} using an established proportional-resonant (PR) controller. The PR controller output is a set of three-phase modulating references without shoot-through

duration included yet.

The required shoot-through time is produced by a classical perturb and observe (P&O) MPPT scheme [100], whose purpose is to vary the PV terminal voltage along the P-V curve in Fig. 8.2 to arrive at the maximum power point. Varying of the PV terminal voltage is not done directly, but indirectly through changing the shoot-through time. Relationship between them can be written as (8.5), which immediately shows the inverse relationship between terminal voltage V_{PV} and shoot-through time T_0/T since V_C is kept constant.

$$V_{PV} = \frac{1-3T_0/T}{T_0/T} V_C \tag{8.5}$$

With the above reasoning, the overall P&O flowchart is shown in Fig. 8.5, where the PV terminal voltage V_{PV} and current I_{PV} are first measured to compute the PV output power P. Power P is then compared with its earlier stored value to decide whether to increase or decrease V_{PV}, which for the example system, is realized by inversely changing T_0/T. The incremental changes made to V_{PV} and T_0/T stop only when P is close to its maximum power point [100].

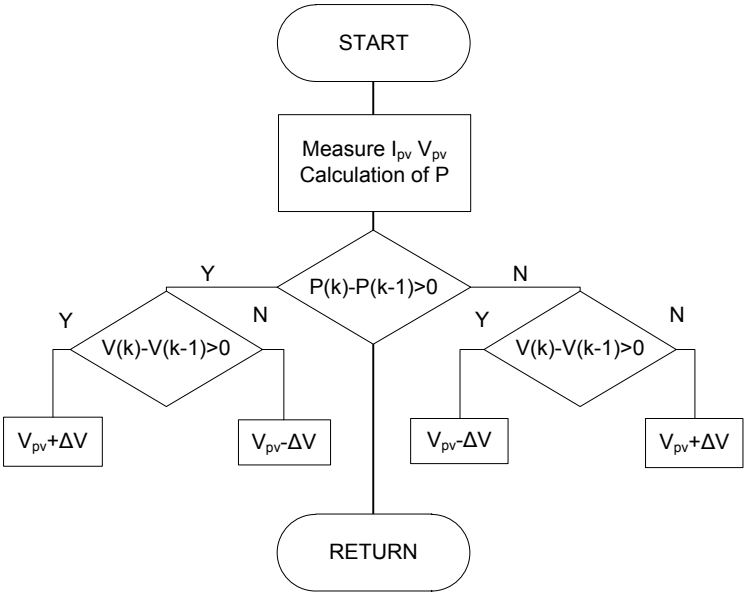


Fig. 8.5 Flow chart of P&O MPPT algorithm

8.2.2. Simulation Results

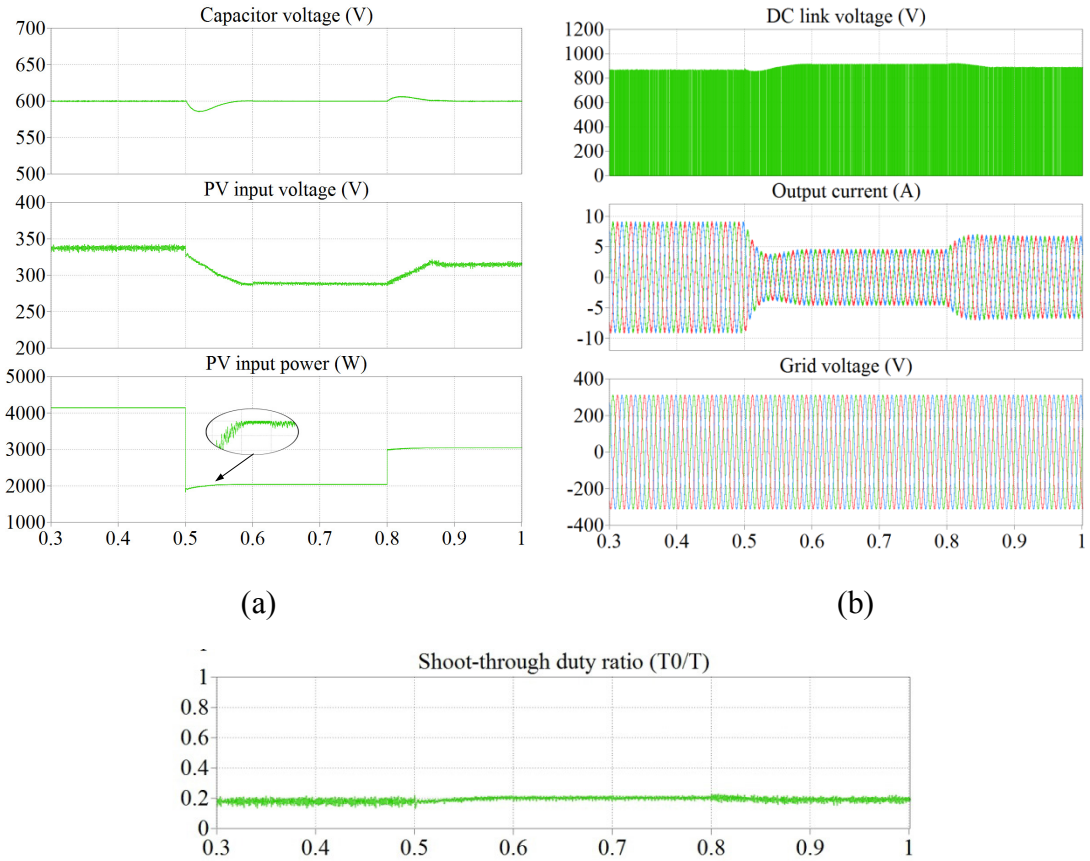


Fig. 8.6 Simulation results of grid-tied inverter

For the simulation, the following PV and inverter circuit parameters are assumed:

- PV open-circuit voltage = 464.4 V, short-circuit current = 14.31A, and maximum power = 4.1 kW at voltage of 337.9 V.
- PV filtered capacitance = 1000 μF, Z-source inductance = 1 mH per inductor and capacitance = 1000 μF per capacitor, inverter ac filter inductance = 2 mH, and ac phase RMS voltage = 220 V (see Fig. 8.6(b)).

The reference capacitor voltage is set to the 600 V, which from Fig. 8.6(a), is tracked properly. The irradiance is then changed from 1000 W/m^2 to 600 W/m^2 at 0.5 s, and then increased to 800 W/m^2 at 0.8 s. According to Fig. 8.6(a), the PV terminal voltage

V_{PV} is able to track the maximum power point even with irradiance changes. The required tracking is done by varying the shoot-through time T_0/T, which varies only slightly around 0.2, as shown in Fig. 8.6(c). That gives a comparably high maximum modulation index of 1.15-0.2=0.95, which can then guarantee better spectral performance. Other results captured are shown in Fig. 8.6(b), which shows the switched dc-link voltage unique to a Z-source inverter and the sinusoidal line currents injected to the grid.

8.3. Summary

An example PV system is simulated with a multi-cell SL Z-source inverter to show how the presented enhanced Z-source inverters can fix into a renewable energy system. The tracking, control and modulation schemes used are the same as those commonly found in a typical PV system. Using an enhanced Z-source inverter for renewable grid interfacing is thus demonstrated to be a simple replacement of inverter circuitry. Modifications to the control schemes, even if needed, are usually kept to a minimum. This claim has already been verified in the chapter.

Chapter 9 Conclusions and Recommendations

9.1. Conclusions

Growing interest in renewable energy has brought along an equal interest in power conditioning systems, whose main responsibility is to process energy to a condition suitable for grid interfacing. To realize that, a power flow controller and a suitably rated power converter are important building blocks that cannot be compromised. For the power flow controller, its main duties are to enforce maximum power point tracking, fast dynamic response and robust riding through of fault conditions. The power flow controller alone is however not capable of implementing the necessary control actions.

That then demands the inclusion of a power converter for realizing the control actions at elevated grid voltage and power levels, which certainly would require some amount of voltage boosting. To meet that requirement, the most common approach is to connect a dc-dc boost converter to a dc-ac inverter without much merging of functionalities. Although robust, there certainly is not much research content linked to such a straightforward connection, unlike those few single-stage inverters proposed with merged functionalities.

Among them, the most recent and among the most popular are the Z-source inverters. However, present Z-source inverters are limited by high component stresses and poor power quality linked to their low modulation ratios at high voltage boost. That then motivates the development of a few Z-source alternatives with raised voltage boost. Contributing to that effort, a few enhanced voltage boost Z-source inverters are also proposed in this thesis, which generally can be classified as either cascading or non-cascading techniques.

For the first category, two generic impedance networks are introduced, which in theory, can be used for representing the conventional, embedded and dc-link embedded topologies of either voltage or current-type. Multiple copies of the voltage-type network are then duplicated and cascaded to raise the output voltage gain. In total, two cascading techniques are introduced, and named as the alternate-cascading and dc-link-cascading techniques. Both techniques produce much higher gains, and use more components, which fortunately are of lower power ratings. They are therefore comparable, but if lower component count and higher modulation ratio are the main deciding factors, the alternate-cascading technique would be the better option.

Other than cascading techniques, non-cascading techniques are also explained. They include the generalized SL, SC and TL techniques, which produce even higher gain than the alternate-cascading technique. However, their component stresses and hence ratings are high, which might seriously limit their practical gains and applications. Direct series and parallel connections of components can address the rating issues, but will bring out common problems like unbalanced series voltage sharing and losses produced by balancing circuits.

Better techniques for distributing stresses are therefore of interest. A relevant thought then is to merge alternate-cascading with the SL or TL technique. The created inverters have slightly lower gains than the individual SL or TL technique, but exhibit better distribution of stresses like the alternate-cascading technique. For even greater saving of components, integration of alternate-cascading with the trans-Z-source technique is proposed, which together with all earlier discussed techniques, will likely result in inverters with the right amount of boosting needed for renewable energy systems. All findings have already been proven in theory, simulation and experiment.

9.2. Recommendations for Further Research

Indeed, many topologies have already been proposed in this Ph.D. thesis, but like most

other investigations, possibilities for future research are always there. A number of immediate topics that can be thought of for sharing are now briefly summarized here.

1. As discovered through experimental testing, stray resistances and inductances of the circuit components can significantly degrade performances of the proposed inverters with enhanced voltage boost. This is especially so for inverters that use magnetically coupled inductors or transformers. Their designs are therefore important, and should be further explored if greater improvement in performance and reduction in size are demanded.

2. Concepts proposed in the thesis are mainly related to the inverter topological layouts and steady-state analyses. In a final physical system, suitable closed-loop control schemes are usually demanded, but are presently lacking for Z-source inverters, in general. Although some researchers have earlier proposed a few control schemes for Z-source inverters, they are not optimized. Those schemes are merely taken from the two-stage buck-boost inverters and applied directly to Z-source inverters without much innovation. Surely, better schemes are preferred, including those fine-tuned to harness the full potentials of the proposed Z-source inverters.

3. Not all techniques proposed in the thesis have existing current-type correspondences. Based on present understanding, they might not be possible, but as new knowledge surfaces as time progresses, research on current-type variants would surely be an attractive topic for investigation.

4. The inverters proposed have so far not targeted a specific application even though their enhanced voltage boost is likely to benefit renewable energy systems (an example case study has been included in Chapter 8 to demonstrate that feasibility). An area for future investigation is thus to study their relevant applications in details, and propose solutions that can solve unobvious concerns.

Author's Publications

Premium Journal Publications

1. **Ding Li**; Feng Gao; Poh Chiang Loh; Miao Zhu; Blaabjerg, F.; , "Hybrid-Source Impedance Networks: Layouts and Generalized Cascading Concepts," *Power Electronics, IEEE Transactions on* , vol.26, no.7, pp.2028-2040, July 2011

2. Feng Gao; Poh Chiang Loh; **Ding Li**; Blaabjerg, F.; , "Asymmetrical and symmetrical embedded Z-source inverters," *Power Electronics, IET* , vol.4, no.2, pp.181-193, February 2011

3. Feng Gao; Lei Zhang; **Ding Li**; Poh Chiang Loh; Yi Tang; Houlei Gao; , "Optimal Pulsewidth Modulation of Nine-Switch Converter," *Power Electronics, IEEE Transactions on* , vol.25, no.9, pp.2331-2343, Sept. 2010

4. **Ding Li**, Poh Chiang Loh, Feng Gao, Miao Zhu, and Frede Blaabjerg, "Cascaded Multi-Cell Trans-Z-Source Inverters", *Power Electronics, IEEE Transactions on,* 2012 early access.

5. **Ding Li**, Poh Chiang Loh, Miao Zhu, Feng Gao, and Frede Blaabjerg, " Generalized Multi-Cell Switched-Inductor and Switched-Capacitor Z-Source Inverters", *Power Electronics, IEEE Transactions on,* 2012 early access.

6. **Ding Li**, Poh Chiang Loh, Miao Zhu, Feng Gao, and Frede Blaabjerg, " Enhanced-Boost Z-Source Inverters with Alternate-Cascaded Switched and Tapped-Inductor Cells", *Industry Electronics, IEEE Transactions on,* 2012 early access.

Premium Conference Publications

1. **Ding Li**; Feng Gao; Poh Chiang Loh; Miao Zhu; Blaabjerg, F.; , "Cascaded impedance networks for NPC inverter," *IPEC, 2010 Conference Proceedings*, vol., no., pp.1176-1180, 27-29 Oct. 2010

2. **Ding Li**; Poh Chiang Loh; Miao Zhu; Feng Gao; Blaabjerg, F.; , "Cascaded switched-inductor and taped-inductor Z-source inverters," *Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE* , vol., no., pp.1661-1666, 6-11 March 2011

3. Feng Gao; **Ding Li**; Poh Chiang Loh; Yi Tang; Peng Wang; , "Indirect dc-link voltage control of two-stage single-phase PV inverter," *Energy Conversion*

Congress and Exposition, 2009. ECCE 2009. IEEE , vol., no., pp.1166-1172, 20-24 Sept. 2009

4. **Ding Li**; Feng Gao; Poh Chiang Loh; Peng Wang; Yi Tang; , "Transient maximum power point tracking for single-stage grid-tied inverter," *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE* , vol., no., pp.313-318, 20-24 Sept. 2009

5. Miao Zhu; **Ding Li**; Feng Gao; Poh Chiang Loh; Blaabjerg, F.; , "Extended topologies of tapped-inductor Z-source inverters," *Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on* , vol., no., pp.1599-1605, May 30 2011-June 3 2011

6. **Ding Li**; Poh Chiang Loh; Miao Zhu; Feng Gao; Blaabjerg, F.; , "Cascaded trans-z-source inverters," *Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on* , vol., no., pp.1976-1980, May 30 2011-June 3 2011

7. **Ding Li**; Feng Gao.; Poh Chiang Loh; Blaabjerg, F.; Zhang, L.; , "Operational analysis and performance comparison of current-type Z-source inverters," *Sustainable Energy Technologies, 2008. ICSET 2008. IEEE International Conference on* , vol., no., pp.798-803, 24-27 Nov. 2008

8. Miao Zhu; **Ding Li**; Poh Chiang Loh; Blaabjerg, F.; , "Tapped-inductor Z-source inverters with enhanced voltage boost inversion abilities," *Sustainable Energy Technologies (ICSET), 2010 IEEE International Conference on* , vol., no., pp.1-6, 6-9 Dec. 2010

9. **Ding Li**; Poh Chiang Loh; Miao Zhu; Feng Gao; Blaabjerg, F.; , "Cascaded switched-inductor and taped-inductor Z-source inverters," *Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE* , vol., no., pp.1661-1666, 6-11 March 2011

10. **Ding Li**; Feng Gao; Poh Chiang Loh; Blaabjerg, F.; Kuan Khoon Tan; , "Hybrid-source impedance network and its generalized cascading concepts," *Power Electronics and Drive Systems, 2009. PEDS 2009. International Conference on* , vol., no., pp.1233-1238, 2-5 Nov. 2009

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