CARBON NANOTUBES BASED MEMORY DEVICES

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The contributions of the co-authors are as follows:

- Prof Zhang Qing and Prof Paolo Lugli provided the initial project direction and edited the manuscript drafts.
- I prepared the manuscript drafts. The manuscript was revised together by Dr Zhang Kang and Prof Zhang Qing.
- I performed all the material synthesis and device fabrication at the School of Electrical and Electronic Engineering. I also analyzed the data.
- All microscopy, including sample preparation, was conducted by me in the N2FC Cleanroom 2 and Characterization laboratory.
- Dr Zhang Kang assisted in the interpretation of the electrical characterization measurement data.

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Summary

Carbon nanotubes (CNTs) have been researched and investigated due to their exceptional electrical, thermal and mechanical properties which make CNTs a promising material for the next generation electronic memories. CNT based memories can mainly be classified into 3 categories. In the first category, semiconducting CNTs are utilized to emulate silicon-based memories, while in the second category the mechanical properties of CNTs are employed to create bi-stable devices for the memory function. In the third category, CNTs are used as the electrodes with a resistive switching material in between two CNTs electrodes to form a memory structure which is similar to conventional resistive random-access memory (RRAM). At the sub-nanometer scale, conventional silicon-based memories are reaching their scaling limits. CNT based memories possess a great advantage over traditional silicon-based memories due to their smaller size and also their superior thermal and mechanical properties. CNT based memories can potentially offer higher density memory as CNT is in the range of a few nanometer size. This allows more data stored into the same spaces as compared with silicon-based memories. In addition, CNT based memories consume lower power compared with silicon counterparts due to smaller active areas. Furthermore, CNT's exceptional properties provide a greater resistance to radiation, magnetism as well as electromigration which affect largely silicon-based memories.

In this dissertation, CNTs based memory devices in particularly using CNTs as the electrode for RRAM have been studied. By using CNTs to replace conventional metal as electrodes for RRAM, the memory device dimension can be reduced, the packing density can be increased and the electromigration in the electrodes can be eliminated. The objectives of this thesis are to develop and analyze the CNT based RRAM devices and compare their performances with conventional metal electrode RRAM devices in order to improve the devices' performance.

The thesis is divided into three parts. In the first part, the metal electrode RRAM was focused. To have a better understanding of RRAM working mechanism and performance, metal electrode RRAM devices were fabricated and analyzed. Several metal oxides were used as the resistive switching material including hafnium oxide (HfO_2), aluminum oxide (Al_2O_3) and zirconium oxide (ZrO_2) to achieve a better memory performance.

In the second part of the thesis, CNTs based RRAM devices were fabricated. Random network CNTs and aligned CNTs were synthesized to fabricate random network CNTs electrode RRAM and aligned CNTs electrode RRAM devices. The electrical characterization was performed to analyze the device performance.

In the last part of the thesis, RRAM devices with a bi-layer resistive switching material and aligned CNTs electrodes were developed. The devices showed several key advantages over the metal electrode RRAM devices where the devices established a forming-free process and low reset current down to 10nA. Furthermore, the devices exhibited lesser variation in term of the operating voltages from cycle to cycle performance for the same device as well as from device to device.

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Abbreviations

CNTs	Carbon nanotubes
SWCNTs	Single-walled carbon nanotubes
DWCNTs	Double-walled carbon nanotubes
MWCNTs	Multi-walled carbon nanotubes
Al_2O_3	Aluminum oxide
HfO_2	Hafnium oxide
ZrO_2	Zirconium oxide
ROM	Read-only memory
RAM	Random access memory
SRAM	Static random access memory
DRAM	Dynamic random access memory
RRAM	Resistive random access memory
PCM/PRAM	Phase change memory
NRAM	Nano-RAM
MRAM	Magnetoresistive random access memory
FeRAM	Ferroelectric random access memory
FET	Field effect transistor
CNTFET	Carbon nanotube field effect transistor
CMOS	Complementary metal oxide semiconductor
XPS	X-ray photoelectron spectroscopy
PDMS	Polydimethylsiloxane
DI	Deionized
SEM	Scanning electron microscope
ALD	Atomic layer deposition

Chapter 1 Introduction

1.1 Background and Motivations

Carbon nanotubes (CNTs), a prominent member of carbon family, are essentially a cylinder rolled by graphene sheets in nanometer scale diameters. CNTs have been widely used in research for many electronics area including transistors, memories, energy storages, sensors, solar cells etc. [154]. With the exceptional electrical, thermal and mechanical properties and better scalability, CNTs are considered to be currently one of the most promising candidates for the future memory devices. CNTs based memories have a great advantage over traditional silicon-based memories due to their small size and also their superior properties. CNTs based memories can be categorize into 3 main types. First type of CNTs based memories utilizes semiconducting CNTs to emulate conventional silicon-based memories such as floating gate transistor memories. Second type of CNTs based memories use the mechanical properties of CNTs to create bi-stable devices for memories function, for examples, the most notable Nano-RAM (NRAM). The last type of CNT based memories replace the metal electrodes in resistive RAM (RRAM) with CNTs and sandwich a resistive switching material in between two CNTs electrode to form a CNTs based RRAM.

CNTFET based memories are similar to conventional silicon-based memories. CNTFET based memories use CNT transistor as their basic structure to trap and hold charges to realize the memory effect. By applying a voltage to the gate, electrons can tunnel through and trap inside the oxide layer or release from the oxide layer. The charges trapped into or released from the oxide gate dielectric layer to create the ‘on’ and ‘off’ states of the CNTFETs.

An NRAM uses CNTs network to create a bi-stable device for memories function. An NRAM is formed by sandwiching a CNTs network fabric with two electrodes. When voltage is applied, the CNTs in the network are brought into contact and the overall resistance is hence reduced. By applying a voltage greater than the read voltage, it will generate CNT phonons to separate the CNTs junction.

In contrast, CNT based RRAM is almost identical to conventional RRAM in which a resistive switching oxide layer is sandwich between two electrodes to form a memory device. For conventional RRAM, metals are usually used as the electrodes. While for CNTs based RRAM, the metal electrodes are replaced with CNTs electrodes. By applying a voltage across the two CNTs electrodes, a conduction path is formed in the oxide layer. This conduction path formation reduces the resistance of the oxide and creates a low resistance state. When a large bias is applied, the conduction path can be annihilated and the resistance returns to a high resistance state.

In this project, the main focus is to make use of CNTs as the electrodes to develop and study CNTs based RRAM devices. Metal electrode RRAM devices were first fabricated and analyzed to have a better understanding of the RRAM performance and the conduction path formation mechanism. Next, CNTs electrode RRAM devices were fabricated and analyzed. Several metal oxides were used as the resistive switching layer to compare and optimize the performance for the CNTs based RRAM memories.

1.2 Objectives

The objectives of this project are to develop novel CNT based memory devices by introducing new designs and optimizing the processes. Several memory devices with different oxide layers were to be fabricated for performance analysis and memory performance optimization. Different structures were to be developed to maximize the memory device performance. The physical mechanism of the conduction path formation in the metal oxide layer and the charge transfer between CNTs electrodes and the dielectric layer were to be studied and analyzed.

1.3 Major contributions of the Thesis

The main contribution of this thesis is developing a novel CNTs based memory devices by analyzing several different structures and several oxide layers as the resistive switching layer in the CNTs based RRAM devices. CNTs based RRAM were fabricated and demonstrated for both random network CNTs as well as aligned CNTs as electrodes (in Chapter 5). Several different device structures and different oxide layers as the resistive switching layers were compared in terms of the device performance. A novel bi-layer resistive switching memory using aligned SWCNTs as electrodes are demonstrated (in Chapter 6). The bi-layer resistive switching memory using aligned SWCNTs as electrodes showed forming-free properties and exhibited a low reset current down to 10nA. The device also showed improvement in stability in terms of operating voltage. The device demonstrated lesser variation from cycle to cycle within the same device as well as from device to device for operating voltage.

1.4 Organization of the Thesis

This thesis presents the systematic study of RRAM devices using CNTs as the electrodes. Several structures and oxide layers were demonstrated and analyzed. A novel bi-layer resistive switching memory using SWCNTs as the electrodes were developed and investigated in coordination with comprehensive experimental results.

In Chapter 1, three categories of CNTs based memories are reviewed. This chapter includes the motivations and the main objectives of this thesis and summarizes the major contribution of this Master project.

Chapter 2 provides the background knowledge and an overview of carbon nanotubes. A review of conventional as well as new emerging memories are presented. Comparison between current memory technologies and new emerging memories are discussed. Finally, different CNTs based memories are reviewed and compared.

Chapter 3 focuses on the device fabrication and CNTs synthesis process. The detailed device fabrication processes are presented and discussed. The fundamental of CNTs growth is reviewed and the growth process for random network CNTs and aligned CNTs are discussed.

In Chapter 4, metal electrode-based RRAM devices is presented. Several different metal oxides with several different thicknesses were used as resistive switching materials for comparison. The mechanism and performance are discussed here.

Chapters 5 introduces the CNTs based RRAM. Random network CNTs and aligned CNTs memory devices are characterized. Metal-CNT electrode RRAM and CNT-CNT electrode RRAM are studied and analyzed. Several oxide layer and thicknesses were fabricated and investigated. The mechanism and performance are discussed.

Chapter 6 introduces a novel bi-layer resistive switching memory using aligned CNTs as electrodes. Bi-layer resistive switching memory using metal as electrode are discussed as well. The proposed mechanism and performance are analyzed and discussed here.

Lastly, Chapter 7 summarizes the main results that have been obtained in the thesis. Also, it recommends opportunities for future researches and suggests some research directions based on the contributions in this thesis.

Chapter 2 Literature Review

2.1 Overview of carbon nanotubes

Carbon nanotubes, a prominent member of the carbon family, are essentially seamless cylinders rolled by graphene sheets in nanometer scale diameters and micro scale lengths. Multi-walled carbon nanotubes (MWCNT) were first discovered by Oberlin et al in 1976[4] while single-walled carbon nanotubes (SWCNT) were discover ed 17 years later in 1993 by Iijima [55] and Bethune [28] independently.

As the simplest case of CNTs, SWCNTs are widely investigated and usually discussed in terms of the structure of a graphene sheet [7, 90]. As shown in Figure 2.1 and Figure 2.2, the basis vectors $a_1 = a(\sqrt{3}, 0)$ and $a_2 = a(\sqrt{3}/2, 3/2)$ generate the graphene lattice, where a = 0.142nm is the carbon-carbon bond length. A and B are the two atoms in the unit cell of graphene [7, 90]. In cutting the rectangular strip, one defines a circumferential vector, or known as chirality vector (n, m) where $Ch = na_1 + ma_2$, from which the CNT radius can be obtained: $R= Ch/2\pi = (\sqrt{3}/2\pi)a\sqrt{n^2+m^2+nm}$. There are two special cases showed in Figure 2.2 that deserve special mention [90]. First, when the circumferential vector lies purely along one of the two basis vectors, the CNT is said to be of the ‘zigzag’ type. Second, when the circumferential vector is along the exact direction between the two basis vectors (n = m), the CNT is said to be of ‘armchair’ type. The transport properties of CNTs are closely defined by the chirality vectors, e.g. ‘armchair’ CNTs (n = m) are metallic while ‘zigzag’ CNTs are semiconducting. If n – m is a multiple of 3, then the CNTs are semiconducting with a very small band gap, otherwise the CNTs are moderate semiconductor.

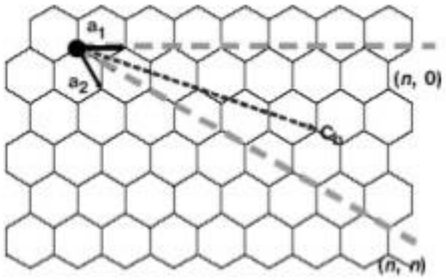


Figure 2.1: Two basis vectors of CNT a_1 and a_2 generate the graphene lattice where a is the carbon-carbon bond length. Ch is the chiral vector connecting the center of two hexagons and it determines the structure of a SWCNT [88].

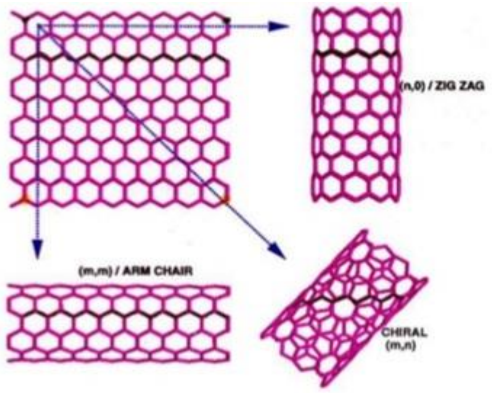


Figure 2.2: CNT rolled up in three different configurations: armchair, zigzag and chiral. They differ in chiral angles and diameter. Armchair CNTs are metallic while zigzag CNTs are semiconducting. Semiconducting CNTs possess an energy band gap and their electrical properties are similar to the semiconductors. In contrast, metallic CNTs possess no energy band gap and their electrical properties are similar to the metals [88].

A SWCNT bundle or network is formed when SWCNTs are packed together closely. The individual nanotubes in the network are attracted to each other via Van der Waals force, with typical distances between the nanotubes being comparable to the inter planar distance of graphite which is 3.1Å. The cross section of an individual nanotube is circular if the diameter is less than 15Å and it deforms into a hexagon as the diameter of nanotube gradually increases. On the other hand, a multi-walled carbon nanotube (MWCNT) consists of several graphene seamless cylinders. As a special type of MWCNTs, double-walled carbon nanotube (DWCNT) consist only two cylinders [111] which offer a good platform for inter-shell effects investigations. Figure 2.3 shows SWCNT and MWCNT atomic structures [16] while Figure 2.4 shows typical TEM images for a MWCNT and a DWCNT [43].

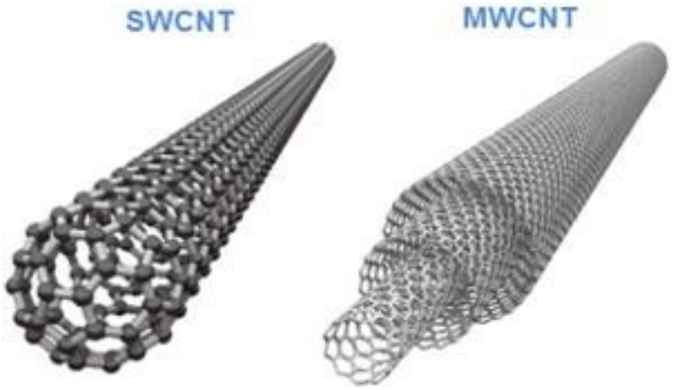


Figure 2.3: SWCNT and MWCNT structure [16].

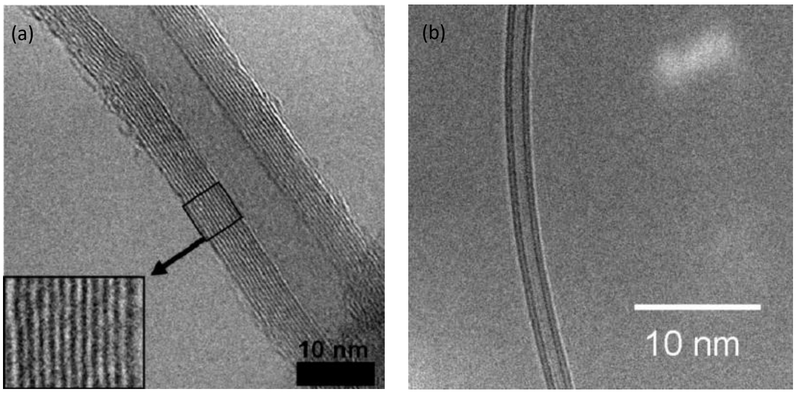


Figure 2.4: TEM images for MWCNT and DWCNT. (a) The cross-section shows MWCNT consist of multiples cylinders and (b) DWCNT consist of two cylinders [43].

2.2 Electronic structure of CNTs

The electronic structure of carbon nanotubes can be understood from graphene electronics. However, SWCNTs show unique behaviors such as definite band gap due to quantum confinement in the lateral directions. These properties can be explained from the graphene energy-momentum relationship shown below.

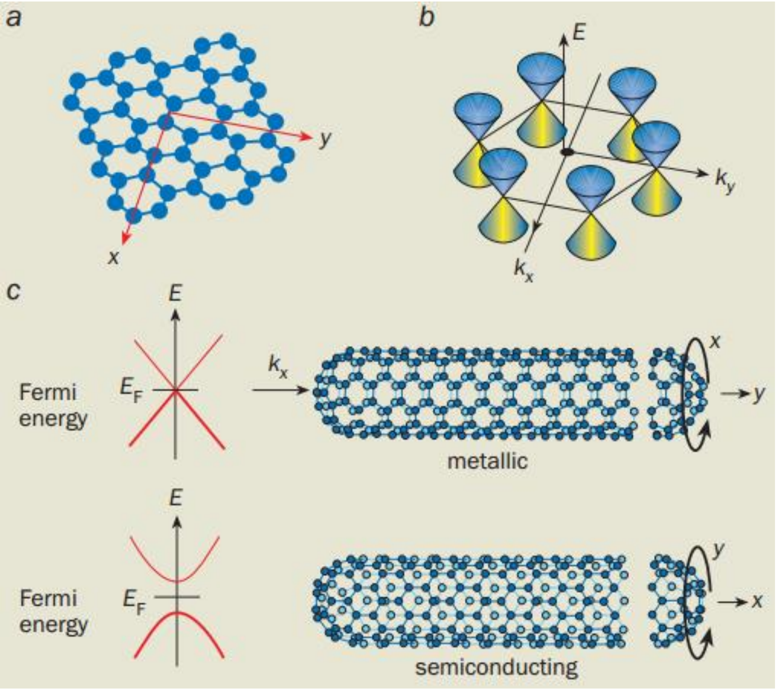


Figure 2.5: Rolling up a graphene sheet to form carbon nanotube [87]. (a) showed the structure of graphene. (b) showed the energy dispersion relation of graphene. (c) showed two ways to roll up graphene sheet, forming metallic CNTs and semiconducting CNTs.

As shown in Figure 2.5, if the graphene sheet is rolled up along the y-direction, the axis direction K_y cut through the graphene Dirac points and the tube formed shows no band gap and the carbon nanotubes are metallic nanotubes. On the other hand, if the graphene sheet is rolled up along the x-direction, the band structure of the nanotube formed has a unique conic section and shows a bandgap. As a result, we see semiconducting behaviors. The rolling up direction, in other words, the chirality vector (n, m) as discussed in part 2.1, determine the band structure of carbon nanotubes and thus the electronic properties.

In addition to chirality vector, the diameter of nanotube determines the band gap. It is calculated that the band gap of a CNT could be in the range of 0.5eV ~ 1.5eV with a right diameter and chirality vector as shown in Figure 2.6 below [91]. Due to the confinement of the electron and holes, the band gap of semiconducting CNT decreases with the increase of CNTs tube diameter. This limits the movement of the electrons and resulted in quantization of the energy and momentum.

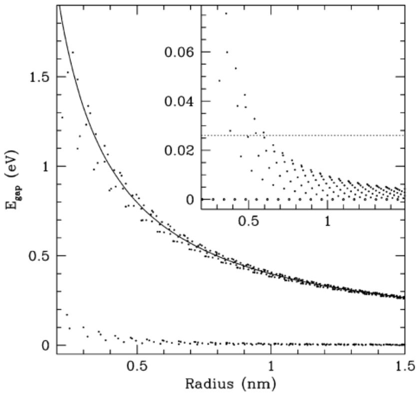


Figure 2.6: Calculated band gaps of semiconducting CNTs as a function the CNT radius. The band gaps of semiconducting CNTs decreases exponentially with the increase of CNTs tube diameters [91].

2.3 Semiconductor memories

Semiconductor memories which store data have been an essential electronic component in various machines or computers that require for data processing and storage. In addition to these, memory card or a portable flash memory card are widely used in all electronic gadgets such as smartphone, camera, tablet, etc. for storing and transferring files. Memory are mainly classified into two kinds, i.e. volatile and non-volatile memory. A volatile memory requires power to maintain the stored data. When the power is turn off, all data stored will be lost. While for non-volatile memory, the memory can retain the data stored even when the power is turn off. The data stored remained in the memory for a considerably long period of time. Example for volatile memory are random access memory (RAM) such as dynamic RAM (DRAM) and static

RAM (SRAM). Both RAM are fast in processing data typically used as computer cache memory. Example for non-volatile memory includes read-only memory (ROM), PROM, EPROM, EEPROM and flash memory. Emerging new memory technology like resistive RAM (RRAM), phase change memory (PCM/PRAM), magnetoresistive RAM (MRAM), ferroelectric RAM (FeRAM) and nano-RAM (NRAM) are also considered as non-volatile memory as they able to maintain its stored data even when the power is turn off. These memories typically store one bit, either a ‘1’ or ‘0’ in a memory cell or a bi-stable flip-flop.

2.3.1 Volatile memory – SRAM and DRAM

SRAM is constructed using the complementary metal oxide semiconductor (CMOS) technology. It uses 6 transistors for each memory cell. The transistors are arranged in such that two cross-coupled inverters are formed. They store data like flip-flops with the other 2 transistors used as access control. SRAM process data very fast and it consume much lower power. SRAM can hold the data as long as the power is turn on and will lose it when the power is turn off [1].

4 transistors are used for generating the logic states which are T1, T2, T3 and T4 as shown in Figure 2.7 [1]. These 4 transistors are assembled in a cross-connected method. To generate logic state ‘1’, C1 is set to high and C2 is set to low. T1 and T4 will turn off while T2 and T3 will turn on. For reset the logic state to ‘0’, C1 is set low and C2 is set to high. In this state, T1 and T4 will turn on while T2 and T3 will turn off. This memory cells will function as long as the DC voltage is supplied.

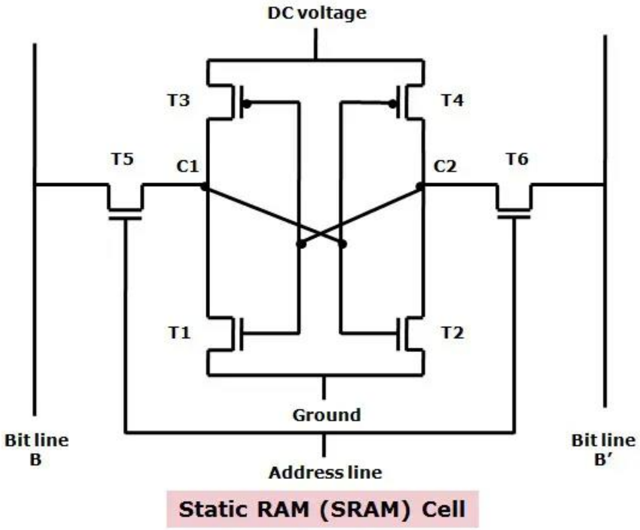


Figure 2.7: A SRAM cell consist of 6 transistors. T1, T3 and T2, T4 formed two cross-coupled inverters which store data like flip-flops. T5 and T6 controlled the access to these two inverters [1].

DRAM is another type of RAM. It constructed with a transistor and a capacitor for a single memory cell. The capacitor is used to store charges which translate as the data. A charged capacitor indicates a stored ‘1’ while a discharged capacitor indicates a store ‘0’. As capacitor will gradually losses its charges over time even when the power is turn on, a refresh is required for DRAM to constantly refresh the capacitor. Hence, the power required for DRAM is higher than the SRAM. While DRAM requires more power due to constant refresh, DRAM is used for larger memory storage as it is cheaper compared with SRAM because it consists of only one transistor for one memory cell compared with SRAM which used 6 transistors. To read or write in DRAM, the address line is activated. The transistor in the memory cell acts as a switch. When it is closed, the current is flowing through and when it is open, no current can flow through. To perform a write, a voltage is sent to bit line, high voltage as ‘1’ and low voltage as ‘0’. Another voltage is sent to address line to enable the transferring of the charge to the capacitor. To perform a read, capacitor is discharged by the cells and then restored back to complete the operation. Figure 2.8 shows a simplified single DRAM cell [1].

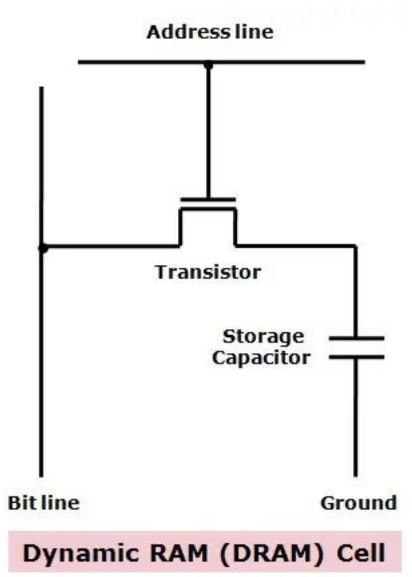


Figure 2.8: A DRAM cell consists of one transistor and one capacitor. The transistor in the memory cell acts as a switch while the capacitor store charges which translate as the data (charged capacitor as ‘1’ and discharged capacitor as ‘0’) [1].

Table 2.1 shows the comparison between SRAM and DRAM in various factors.

	SRAM	**DRAM**
Speed	Faster speed	Slower speed
Refresh	No refresh required	Refresh required
Circuitry	Complex circuit	Simple circuit
Access time	Faster access time	Slower access time
Data storage	Uses flip-flops	Use a transistor and capacitor
Density	Low density	High density
Cost	Expensive	cheap

Table 2.1 shows comparison between SRAM and DRAM [1].

2.3.2 Non-volatile memory – ROM

ROM or read-only memory as the name indicates, generally refer to storage medium that can only be read. The information stored in ROM is permanently during manufacture such as firmware in computer or electronic gadgets. There are other types of ROM such programmable ROM (PROM), erasable and programmable ROM (EPROM) and electrically erasable and programmable ROM (EEPROM). PROM is memory that can only be modified once by the user. The user purchases a blank PROM and can program the PROM once. Once it is programmed, it cannot be erased. EPROM can be erased by exposing it under ultra-violet light for a certain duration. EEPROM can be erased and programed electrically. Another type of memory which is flash memory is also a non-volatile memory has been widely used in daily life machines and electronic gadgets. A flash memory incorporates the use of floating gate transistor, or floating gate MOSFET to store data. Flash memory works by charging or discharging electron into the floating gate. The memory can be '1' or '0' depending on whether the floating is charged or uncharged. When electrons are trapped in the floating gate, current cannot flow through the transistor and the bit state is '0'. When the electrons are released from the floating gate, the current is allowed to flow through and thus the bit state is '1'. Flash memory can be classified into two kinds, the NAND and NOR logic gates. NAND-type flash memory can be erased, written and read in blocks. While NOR-type flash memory can configure each single byte independently. The NAND-type flash memory is mostly used for memory cards, USB flash drive etc. for storage and transfer of data. Figure 2.9 shows a simplified floating gate transistor structure [108].

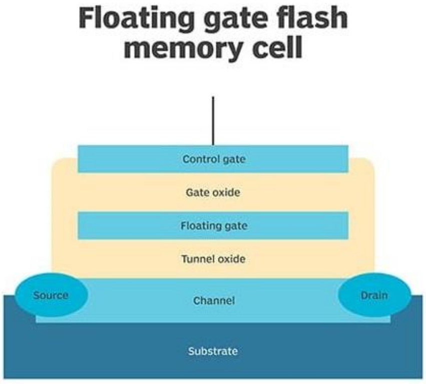


Figure 2.9: The structure of a typical floating gate transistor. Electrons with sufficient energy tunneled through the tunnel oxide and trapped in the floating gate when a positive voltage applied on control gate. The oxide layers surrounded the floating gate keep the electrons trapped inside floating gate, enabled data storage with or without power. [108].

2.3.3 Non-volatile memory – New emerging memory

Besides those mentioned memories, several new emerging memories have been researched and studied to potentially replace current memory technology which are mainly dominated by flash memory. Among those new emerging memories, there are resistive RAM (RRAM), phase change memory (PCM/PRAM), magnetoresistive RAM (MRAM), nano-RAM (NRAM) and ferroelectric RAM (FeRAM).

RRAM is constructed by sandwiching a resistive switching layer such as metal oxide between two electrodes. By applying a voltage across the two electrodes, a conductive path can be formed by electrochemical metallization mechanism or oxygen vacancy mechanism in the oxide layer. This creates a low resistance state (LRS) and it can maintain its resistance for a substantial period of time. By applying another voltage, the conductive path can be annihilated and the oxide layer returns to high resistance state (HRS). RRAM switching operation can classified into two behavior, i.e. unipolar and bipolar. For unipolar switching operation, the switching procedure does not depend on the polarity of the applied voltage. The set and reset operation can both occurred on positive voltage or negative voltage. For bipolar switching operation, when the device set to LRS at one voltage polarity, the reset process to HRS have to occur at the opposite voltage polarity. Figure 2.10 shows the switching operation of RRAM for unipolar and bipolar [6]. Figure 2.11 shows the RRAM cross point structure and its cross-section view [124].

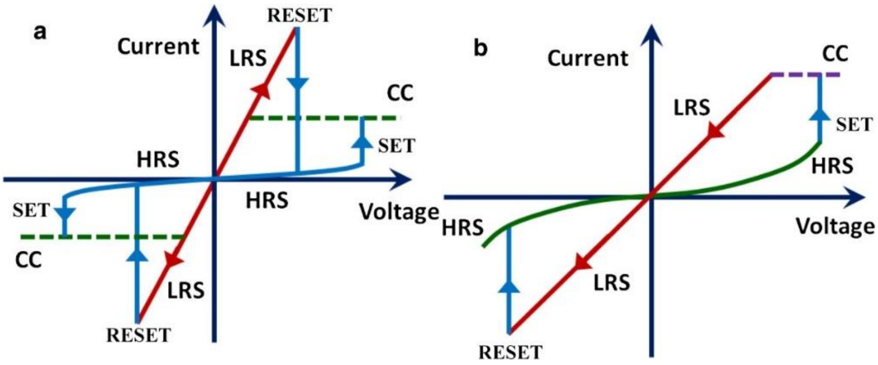


Figure 2.10: Switching operation of RRAM. (a) I-V characteristic for unipolar. Set and reset occurred in the same polarity. (b) I-V characteristic for bipolar. Set and reset occurred in the opposite polarity [6].

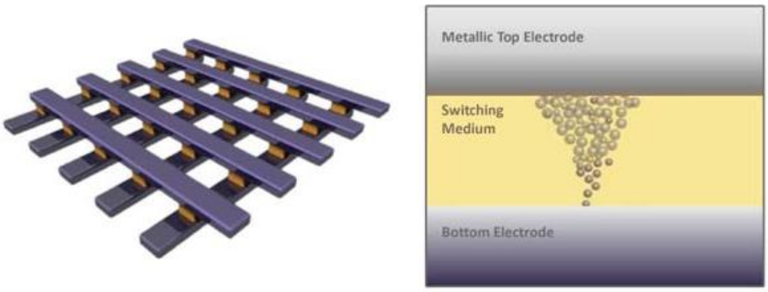


Figure 2.11: RRAM cross point structure and cross section view. Two electrodes sandwiched a switching medium in between. A conductive path is formed in the switching medium when a sufficient voltage is applied [124].

Phase change memory (PCM) typically consisted of chalcogenide glass as phase change material, can be utilized to achieve a memory functionality. Traditionally for PCM mechanism, a current flow through the phase change material produces heat. The heat is able to alter the phase change material from non-crystalline or amorphous to crystalline state and vice versa. By changing the crystallization, the device can achieve HRS when in amorphous state or LRS when in crystalline state. New researches on PCM based memories are concentrated on the use of GeTe-Sb_2Te_3 superlattice to create a non-thermal phase change memory by simply changing the coordination state of the Ge atoms with a laser pulse. Figure 2.12 shows a typical PCM structure [33].

Figure 2.12: A typical PCM structure consists of two electrodes sandwiched a phase change material e.g. GeSbTe (GST) in between. When a voltage is applied, the localized area heated, and its crystallinity can be altered [33].

Unlike conventional RAM like RRAM and PCM, MRAM does not stored data as electron or current flows but by magnetic storage elements. MRAM consisted of 2 ferromagnetic plates, isolated each other by an insulating layer. One of the ferromagnetic plates is a permanent magnet which set to a designed polarity, while the other plate magnetization can be changed to alter its polarity. When the two plates are in same magnetization polarity, it becomes LRS or a ‘1’. On the other hands, if the polarity is anti-parallel, it becomes HRS or a ‘0’. Figure 2.13 shows a simplified MRAM structure [2].

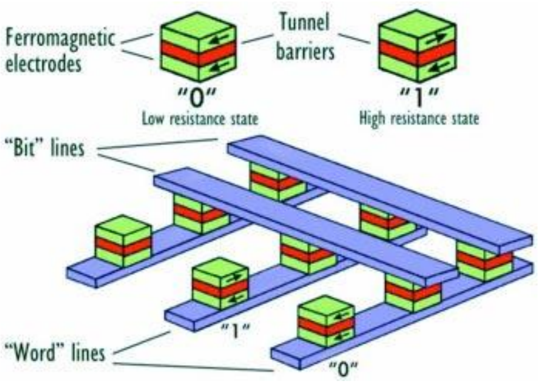


Figure 2.13: A simplified MRAM structure consists of two ferromagnetic electrodes and an insulating layer. The polarity of one of the ferromagnetic electrodes can be manipulated to form parallel or anti-parallel magnetization polarity with the other permanent ferromagnetic electrode [2].

NRAM is a new type of memory created by Nantero company. NRAM uses the mechanical properties of CNTs to create bi-stable devices for memories function. The CNTs network is sandwiched between two electrodes. Detailed explanation on NRAM working principle will be discussed in later section. Figure 2.14 shows the first publication on NRAM [109].

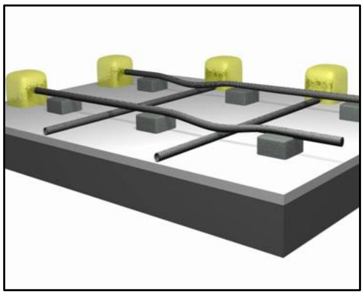


Figure 2.14: The structure of an NRAM array. When a voltage is applied across the top and bottom CNTs, the two CNTs attracted to each other and the resistance between the two CNTs is reduced [109].

FeRAM is similar to construction of floating gate transistor of DRAM, but the dielectric layer is replaced with a ferroelectric layer for memory functionality. When an electric field is applied across the ferroelectric, the dipoles will tend to align themselves with the field direction. The dipoles retained its polarity even when the electric field is removed. Binary state of ‘1’ and ‘0’ can be stored in the two polarization, either ‘up’ or ‘down’ orientation of the dipoles. Figure 2.15 shows the simplified version of FeRAM structure [57].

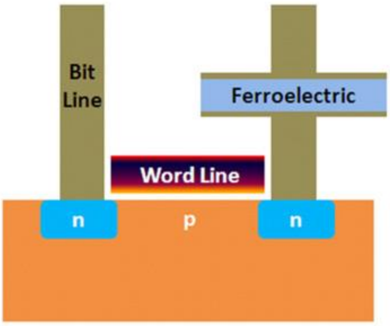
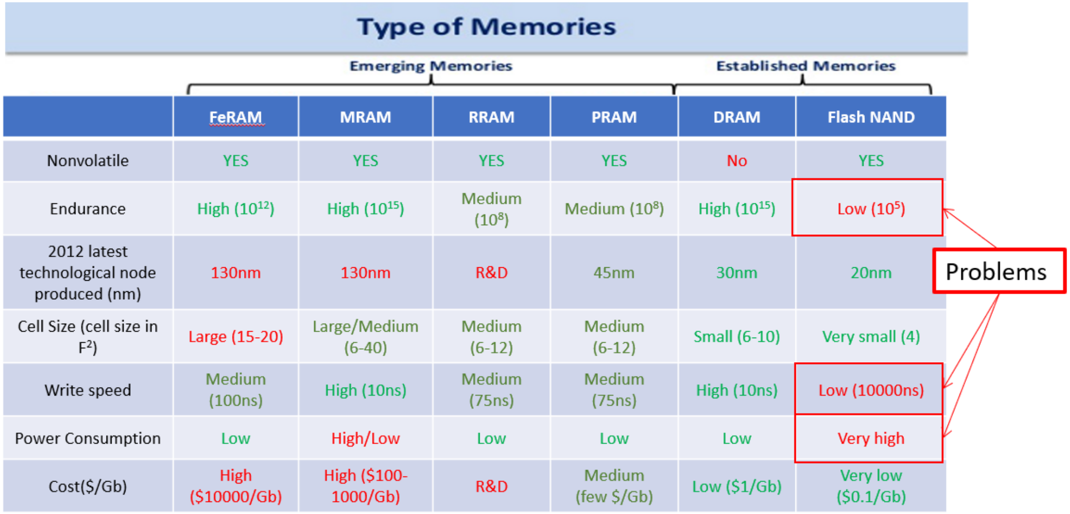


Figure 2.15: A simplified FeRAM structure. Dipole of ferroelectric layer aligned themselves with the electric field direction applied to form binary state of ‘1’ and ‘0’ [57].

2.3.4 Comparison between different type of memories

Table 2.2 compares various types of memories in different aspects. Flash NAND memories which are dominating the current market have several advantages over the others such as very small in the cell size which lead to a higher density, and a very low cost. However, they are suffered from a few disadvantages, like low endurance only in a range of 10^5, slow writing speed and much higher power consumption compared with the others new emerging memory technologies. Most of the new emerging memories have showed their advantages over the flash NAND memories in endurance, writing speed and power consumption, which make these memory technologies very attracting. However, there are still several issues that need to be solved for these new emerging memory technologies. These issues including compatibility of fabrication process to the mainstream CMOS fabrication technology and one of the most important things is the production cost for the memories. As the new emerging memories require some new fabrication processes, it is essentially important to carefully study the new processes fitting into the current CMOS fabrication process [17].



Type of Memories

	Emerging Memories				Established Memories	
	FeRAM	MRAM	RRAM	PRAM	DRAM	Flash NAND
Nonvolatile	YES	YES	YES	YES	No	YES
Endurance	High (10^{12})	High (10^{15})	Medium (10^{8})	Medium (10^{8})	High (10^{15})	Low (10^{5})
2012 latest technological node produced (nm)	130nm	130nm	R&D	45nm	30nm	20nm
Cell Size (cell size in F^2)	Large (15-20)	Large/Medium (6-40)	Medium (6-12)	Medium (6-12)	Small (6-10)	Very small (4)
Write speed	Medium (100ns)	High (10ns)	Medium (75ns)	Medium (75ns)	High (10ns)	Low (10000ns)
Power Consumption	Low	High/Low	Low	Low	Low	Very high
Cost($/Gb)	High ($10000/Gb)	High ($100-1000/Gb)	R&D	Medium (few $/Gb)	Low ($1/Gb)	Very low ($0.1/Gb)

Table 2.2: Comparison between different types of memories in different aspects [17].

2.4 CNT based memories

CNTs have been investigated and researched in various applications, such as transistors, memories, energy storages, sensors, solar cells and etc [154]. Among these applications, CNTs based memories have drawn a lot of research attention. CNTs based memories possesses a great advantage over traditional silicon based memories due to their smaller size and also their superior electrical, thermal and mechanical properties. CNTs based memories can potentially offer higher memory unit density as CNTs is in the range of few nanometers. This allows more data stored per unit space as compared with silicon-based memories. With their smaller active areas, CNTs based memories have lower power consumption compared with silicon based memories. CNTs based memories also show good stability in maintaining theirs on and off state in the nanometer size and the bi-stable states showed non-volatile properties. Moreover, CNTs' excellence in resistance to radiation, magnetism as well as electromigration proved its advantages over silicon-based memories in degradation. CNTs based memories can be mainly sort into 3 main types. First type of CNTs based memories utilize semiconducting CNTs as channel in floating gate transistor to function as a memory device. Second type of CNTs based memories use CNTs network as the resistive switching medium to create a bi-stable memory device. Finally, the last type of CNT based memories are similar in construction to conventional RRAM but utilized CNTs as electrodes instead of metal electrodes with a resistive switching material sandwiched in between the two CNTs electrodes to form a memory cell.

2.4.1 CNTFET based memories

Similar to conventional silicon-based memories, CNTFET based memories use CNT transistors as their basic building block. By applying a gate voltage, charge transferred from CNT channels to the oxide layer and trap inside. The trapped positive (negative) charges cause the local electric potential increase (decrease). The local electric potential increase has a distinct impact on the CNT channel conductance in comparison with the local electric potential decrease, leading to the memory effect. To release the charges, an opposite polarity voltage is applied to the gate. Figure 2.16(a) shows the flat band condition without considering the voltage drops within the dielectric. Figure 2.16(b) and (c) show the band profile of electrons tunnel from the conduction band and the valence band of CNT to the defect state in HfO_2 respectively when writing with a positive gate voltage. Figure 2.16(d) shows the band profile with the stored electrons removed from the HfO_2 by applying a negative gate voltage. The band bending induced by the gate operation in Figure 2.16(b), (c) and (d) is omitted for simplicity, and the energy band diagram is not in exact scale [106].

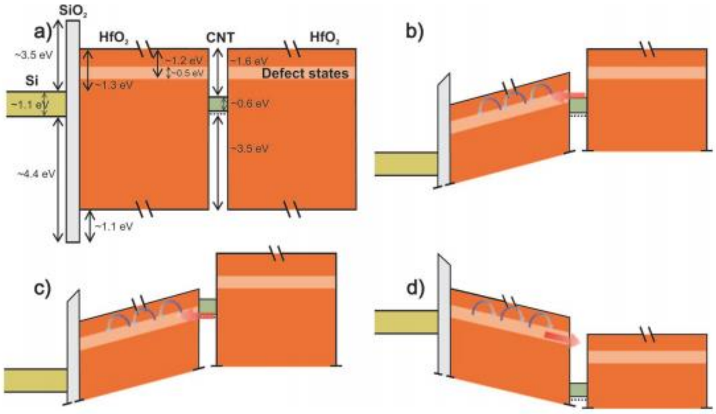


Figure 2.16: Schematic energy band diagram for a Si/SiO$_2$/HfO$_2$/CNT/HfO$_2$ gate stack. (a) The flat band condition without considering the voltage drops within the HfO$_2$ layer. (b) The band diagram of the device shown in (a). Electrons tunnel from the conduction band of the CNTs into the HfO$_2$ layer and (c) the valence band of the CNTs is aligned to the defect states in the HfO$_2$ when applying a positive gate voltage. (d) The band diagram when the stored electrons removed from the HfO$_2$ layer by applying a negative gate voltage. The band bending induced by the gate operation in (b), (c) and (d) is neglected for simplicity [106].

CNTFET memory is fabricated by first depositing and patterning of a back-gate on a substrate or using a substrate itself as a back gate. Then followed by gate dielectric deposition and patterning on top of the back gate. After that, CNTs are deposited on the gate dielectric followed by formation of the source and drain. Finally, another layer of oxide thin film is deposited as a passivation layer. Figure 2.17 shows schematic view of a CNTFET memory with the bottom gate [38].

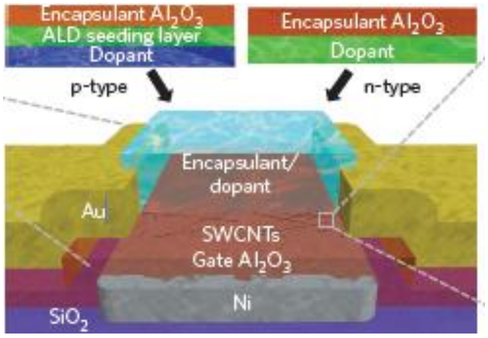


Figure 2.17: Schematic cross-section view of a CNTFET memory with bottom gate. For p-type transistor, the layers on top of CNTs consist of the p-type dopant, an ALD seeding layer and a final encapsulation layer of Al_2O_3. For the n-type transistor, the top layers consist of n-type dopant and the final encapsulation layer of Al_2O_3 [38].

CNTFET memories typically show a moderate endurance performance of 10^4. The on/off ratio for CNTFET memory is reasonably high at 3000. The threshold voltage for CNTFET memories is typically at 1.25V. Figure 2.18 shows a typical CNTFET memory characteristic [106].

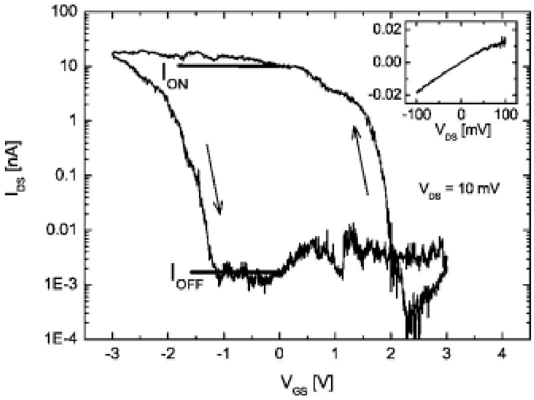


Figure 2.18: CNTFET memories characteristic. The device has a hysteresis window of 3.2V, subthreshold of 120mV/dec and an on/off ratio at around 10^3. The arrows indicate the backgate scan direction within the loop. The inset shows the I-V curve in the off state [106].

2.4.2 Nano-RAM (NRAM)

A NRAM makes use of the mechanical properties of CNTs to create bi-stable states for memory functions. A NRAM is fabricated by depositing the bottom electrode, followed by CNTs network deposition and finally top electrode deposition and patterning. When CNTs in the network are not in contact, the resistance between the two electrodes is high which represents an ‘off’ or ‘0’ state. When the CNTs are brought into contact, the resistance is low which represents an ‘on’ or ‘1’ state. To switch between these two states, a voltage greater than the read voltage is applied between the two electrodes. If the NRAM is in ‘0’ state, the voltage applied will cause electrostatic attraction between the CNTs so that the CNTs can come in contact with each other. After the applied voltage is removed, the device remains in a ‘1’ or low resistance state due to physical adhesion by Van der Waals force. If the NRAM is in the ‘1’ state, by applying a voltage greater than the read voltage, it generates CNT phonon with sufficient energy to separate the CNT junctions. Thus, the RESET operation is phonon driven. These two states are very stable and sustain even after power off. Figure 2.19 shows how CNTs perform the on and off states [109] and Figure 2.20 shows a simplified NRAM and its cross-section view [29].

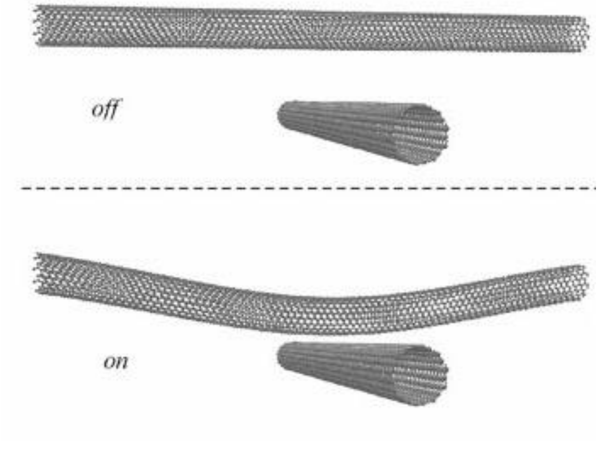


Figure 2.19: CNTs contact for on and off states [109].

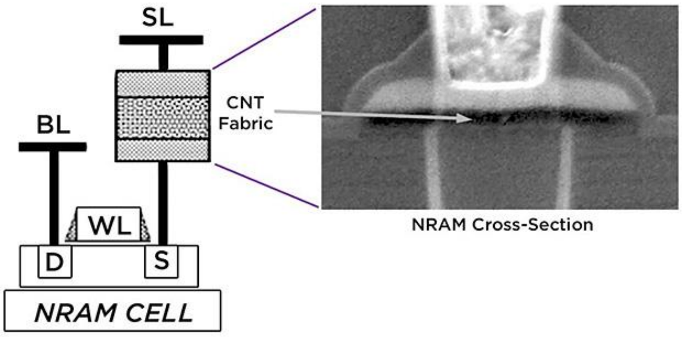


Figure 2.20: A simplified NRAM structure with a select transistor and cross-section view of the memory in SEM [29].

CNT NRAMs have a high endurance at 10^{12} due to very stable of on and off state. The On/off ratio for NRAM however is relatively low at 10 – 100 due to the compensation for lower set and reset voltage. Set and reset voltage are at around -2V / +3V respectively. Figure 2.21 shows a typical memory characteristics and endurance performance for an NRAM [93].

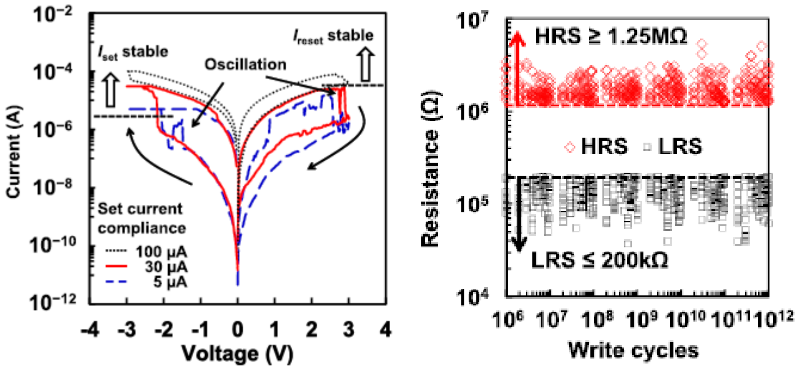


Figure 2.21: NRAM I-V characteristics with different set compliance currents and endurance performance for an NRAM with HRS greater than 1.25MΩ while LRS lower than 200kΩ [93].

Figure 2.22 shows the SEM images of the cross-section view for an NRAM which is integrated into CMOS back-end metal process [107].

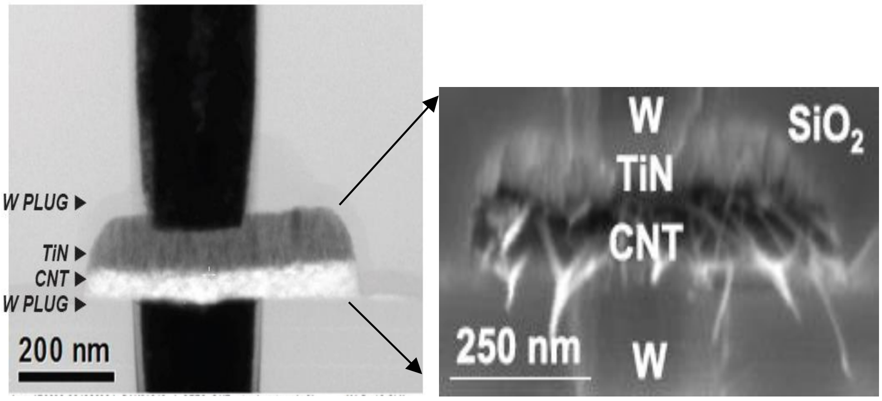


Figure 2.22: SEM images of cross section view for an NRAM [107].

2.4.3 CNT based RRAM

RRAM technology is one of the most promising non-volatile memory technologies and it has been researched extensively. RRAM has attracted a lot of attention as it shows good cycling endurance (> 10^{12} switching cycles), high read/write speed (tens of nanoseconds), long retention time (> 10 years), simple fabrication process and good scaling behavior [7]-[10]. One of the most notable advantages of RRAM over the other emerging memories is its simple metal-insulator-metal (MIM) structure to form a memory cell. Conventionally, metal such as gold (Au), platinum (Pt), aluminum (Al), palladium (Pd) and tungsten (W) were used as the metal electrodes for RRAM devices. However, as the devices shrink down to nanometer sizes, metals exhibit high resistance and are greatly prone to electromigration. In contrast, SWCNTs are of extremely thin diameters in few nm ranges and SWCNTs has excellent thermal, mechanical and electrical properties. SWCNTs exceptional properties provide them a great resistance against electromigration which suffered by metal electrode RRAM. A CNT based RRAM is similar to a conventional RRAM in which a resistive switching layer is sandwiched between two metal electrodes to form a RRAM device. In CNT based RRAM, CNTs are used as the two electrodes with a resistive switching material in between the two CNT electrodes. The basic working principle of RRAM is that the resistive switching material (or dielectric), which is normally insulating, can be made to conductive state through a conductive path formed after a sufficient high electric field is applied. The conduction path can arise from different mechanisms, including oxygen vacancies or metal defect migration [27, 86]. Once the conduction path is formed, it may be reset (broken, resulting in high resistance state) or set (re-formed, resulting in low resistance state) by another applied electric field. Many current paths, rather than a single path, are possibly involved. Figure 2.23 shows a carbon nanotube crossbar electrodes-based RRAM [122].

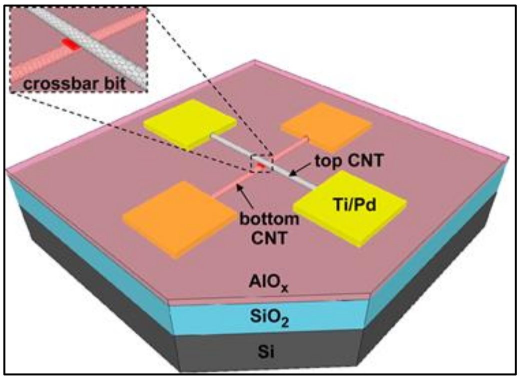


Figure 2.23: Carbon nanotube crossbar electrodes-based RRAM with Al_2O_3 as resistive switching layer [122].

A CNTs based RRAM is fabricated by first transferring the bottom CNTs to a substrate. Then the bottom contacts are formed followed by resistive switching material deposition. Next, top CNTs are transferred onto the switching material and top contacts are formed to complete the RRAM device. Figure 2.24 shows a SEM image of a CNTs based RRAM [122].

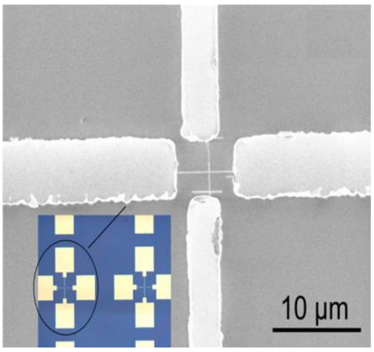


Figure 2.24: A SEM image of a CNT based RRAM [122].

CNT based RRAMs show a moderate endurance performance of 10^4. They have a high on/off ratio around 4000 due to large resistance difference between high resistance state and low resistance state. However, CNT based RRAMs require higher set and reset voltages at +8V / -8V, respectively as they need a higher electric field to break and form the conduction filaments. Figure 2.25 shows the typical memory characteristics curves for CNT based RRAM [122]. Figure 2.26 shows the memory structure and I-V characteristic for the RRAM device with aligned CNTs as bottom electrode [133].

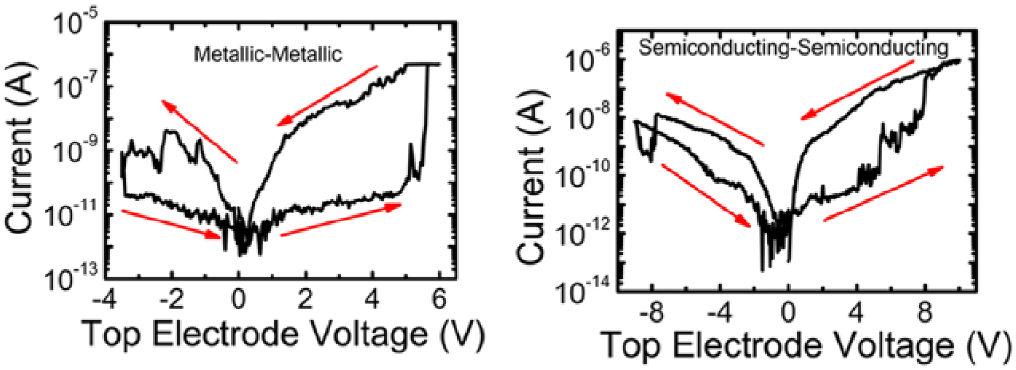


Figure 2.25: CNT based RRAM memory characteristics for metallic and semiconducting CNTs. Arrows indicate the voltage sweeping direction from set to reset [122].

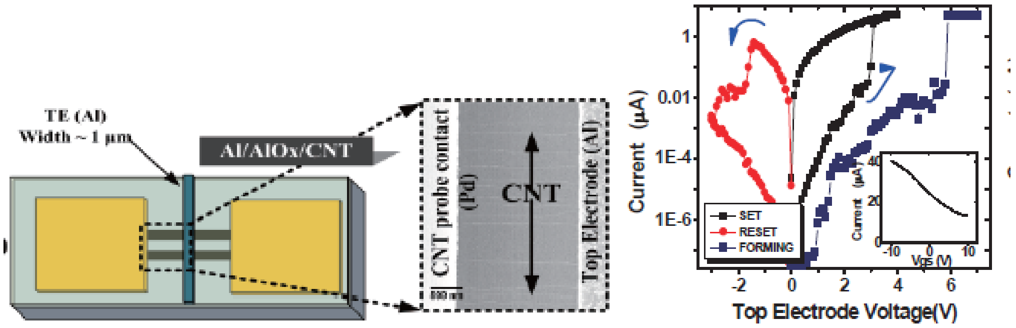


Figure 2.26: Memory structure and I-V characteristic for the RRAM device with aligned CNTs as bottom electrode [133].

2.4.4 RRAM resistive switching mechanism

There are several resistive switching mechanisms for RRAMs. The most prevalent mechanisms are the oxygen vacancy mechanism and the electrochemical metallization mechanism.

2.4.4.1 Oxygen vacancy mechanism

When the voltage is applied through the two electrodes reaches a critical value that is sufficient to create oxygen vacancy, oxygen ions moved towards electrodes and the interstitial positions, hence, form a conductive path. This leads to a sharp decrease in the resistance of the resistive switching materials and the devices change from their initial HRS to a LRS. By applying another voltage depending on unipolar or bipolar characteristic, oxygen ions move back to fill up partial interstitial positions left by the oxygen ions, annihilating the conductive path and turning the devices back to their HRS. Figure 2.27 illustrates the resistive switching mechanism in different states [86].

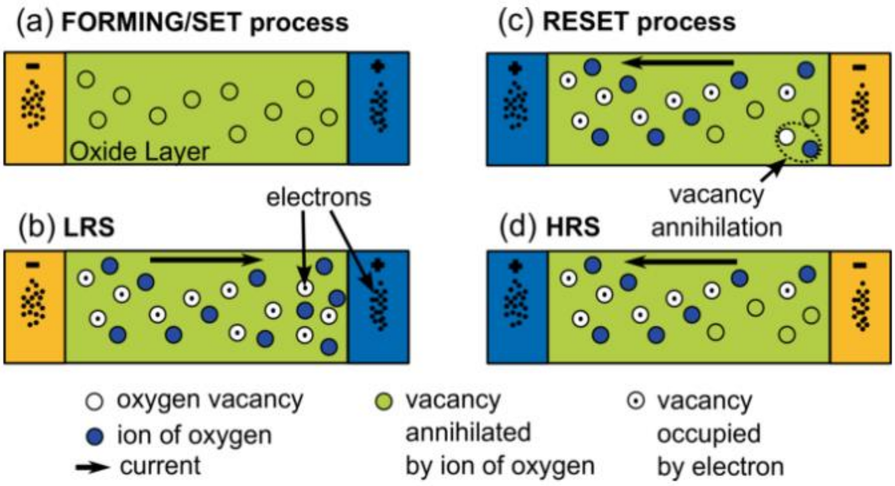


Figure 2.27: Schematic illustration for resistive switching mechanism in bipolar oxide-based memory. Schematic illustration (a) during forming/set process and (b) during reset process. Schematic view (c) in LRS and (d) in HRS [86].

2.4.4.2 Electrochemical metallization mechanism

For electrochemical metallization mechanism, the conductive path is formed by redox reactions in the oxide layer, which is especially sandwiched between an oxidizable electrode (Ag or Cu) and an inert electrode (Pt or W). When a voltage is applied on the oxidizable electrode, electrochemical reaction occurs in which the metal atoms are oxidized into metal ions which could drift into the oxide layer toward the inert electrode under the electrical field. This results in a conductive path formed between the two electrodes, leading to the LRS. By changing the polarity of the voltage, the process is reversed and the conductive path can be ruptured, making the device returning to the HRS. Figure 2.28 shows the schematic illustration of electrochemical metallization mechanism [27].

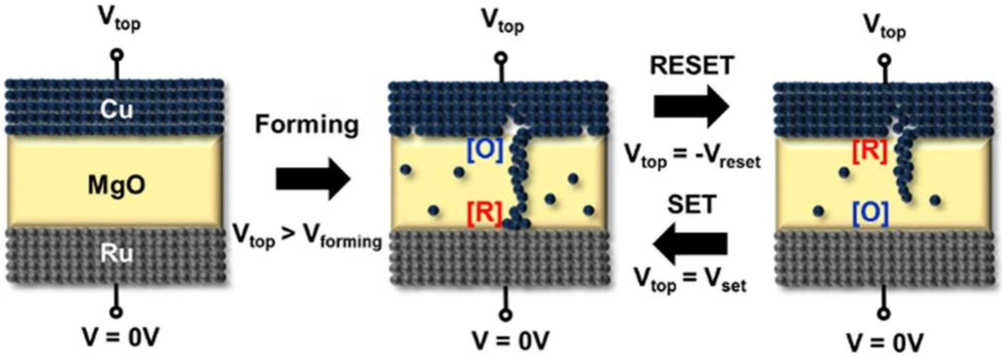
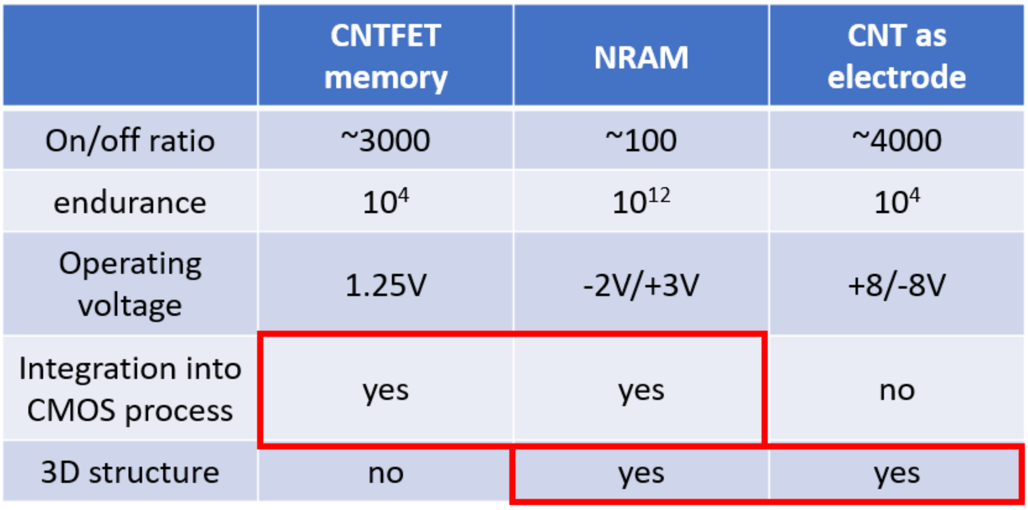


Figure 2.28: Schematic illustration of electrochemical metallization mechanism. When a voltage applied to the top Cu electrode, the Cu metal ions drift into the oxide layer and form a conductive path. When a reversed polarity voltage applied to the top Cu electrode, partial of the Cu metal ions drift back and the device return back to HRS [27].

2.4.5 Comparison between different CNTs based memories

Table 2.3 compares several CNTs based memories, i.e. CNTFET memories, NRAMs and CNTs based RRAMs. In general, CNTFET memories and CNTs based RRAMs are able to achieve a higher on/off ratio as compared with NRAMs. While NRAMs show their advantage in a high endurance in comparison with CNTFET memories and CNTs based RRAMs. This means that NRAMs are able to perform much more switching cycles. CNTFET memories and NRAMs require a much lower operating voltage in the range of 1V to 3V, while CNTs based RRAMs require a much higher operating voltage due to inherent internal resistance. CNTFET memories and NRAMs can be integrated into CMOS process but CNTs based RRAMs still in the research stage. NRAMs and CNTs based RRAMs have showed their potentials to stack the memory devices in 3D structure which can further improve the packing density in vertical stacks. Although CNTs based RRAMs still have some issues to be resolved, they are demonstrated with significant advantages over the other two types of CNT based memories.



	CNTFET memory	NRAM	CNT as electrode
On/off ratio	~3000	~100	~4000
endurance	10^4	10^{12}	10^4
Operating voltage	1.25V	-2V/+3V	+8/-8V
Integration into CMOS process	yes	yes	no
3D structure	no	yes	yes

Table 2.3: A comparison between several CNTs based memories in different aspects.

Chapter 3 CNTs Synthesis and CNT RRAM Fabrication

In this chapter, the processes for growing random network CNTs as well as aligned CNTs will be explained. CNT suspension and CNTs transfer process will also be discussed in detail.

Subsequently, RRAM device fabrication will be discussed including metal electrode RRAM devices, random network CNTs electrode RRAM devices, Metal-CNT electrode RRAM devices and CNT-CNT electrode RRAM devices.

3.1 Substrate preparation for random network CNT growth

Before random network CNT growth, the silicon substrates were clean and surface treatment was performed to make the substrate surface hydrophilic. First, the blank substrates were immersed in the acetone solution and ultrasonic for 10 minutes. After that the substrates were immersed in the isopropyl alcohol (IPA) solution and ultrasonic for another 10 minutes. Next, clean the substrates with deionized water (DI water) and dry them. Piranha solution consists of sulfuric acid (H_2SO_4) and hydrogen peroxide and (H_2O_2) with 3:1 ratio was prepared and heated up to 120°C. When the temperature reached 120°C, the cleaned substrates were immersed in the piranha solution for 20 minutes for surface treatment. After 20 minutes, the substrates were removed from the solution and cleaned with DI water and then blow dry. Finally, ferritin catalyst was spin coated onto the substrates with 4000 rpm spinning speed until no color change.

3.2 Growth of random network CNTs

Random network CNTs were grown using the thermal chemical vapor deposition (TCVD) method. Figure 3.1 shows the SEM images of two random network CNTs prepared with the following procedures.

First, the substrates coated with ferritin catalyst were inserted into a quartz tube and heated up to 800°C in the air and maintained for 1 minute. After that, the samples were cooled down to around 200°C. The quartz tube was then enclosed and argon gas of 200 sccm flow rate was turned on for 1 minute to eliminate the air inside the quartz tube. After 1 minute, argon gas was turned off and hydrogen gas of 100 sccm flow rate was turned on and start to heat up to 925°C and then maintained for 5 minutes. Next, the hydrogen gas flow rate was changed to 30 sccm and argon gas of 50 sccm was turned on by flowing through a bubbler filled with ethanol for 15 minutes. After 15 minutes, the heater and bubbler were turned off and let the quartz tube and the samples inside cooled down to room temperature before taken out.

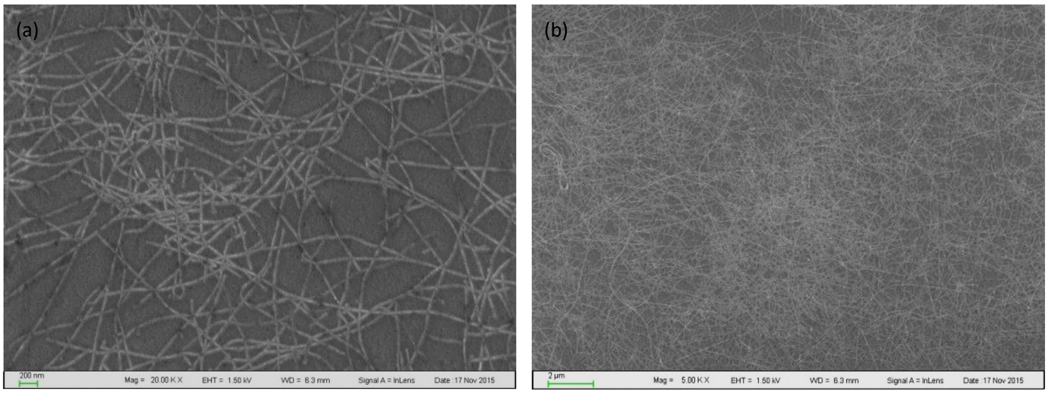


Figure 3.1: The SEM images of random network CNTs. Random network CNTs under (a) x20000 magnification and (b) x5000 magnification in SEM.

3.3 Substrate preparation for Aligned CNT growth

Before aligned CNT growth, the quartz substrates were cleaned and prepared as the following procedures. The quartz substrates were first cleaned by immersing in the acetone solution and ultrasonic for 10 minutes. Then, the quartz substrates were immersed in the IPA solution and ultrasonic for another 10 minutes. The quartz substrates were then cleaned with DI water and blew dry. Next, the quartz substrates were annealed in the air at 925°C for 8 hours. After annealing process, lithography process was performed to create the line patterns on the quartz substrates. O_2 plasma was applied on the quartz substrates for 1 minute to create hydrophilic surface and remove remaining photoresist on the exposed area. The quartz substrates were then immersed in the APTES solution with a ratio of 0.4ml APTES to 100ml DI water and left overnight. On the next day, the quartz substrates were removed from the solution and cleaned with DI water and blow dry. Ferritin catalyst was then drop cast onto the quartz substrates and left them for 3 hours. Afterwards, the quartz substrates were washed with DI water and blew dry and then immersed in the IPA solution for 10 minutes to clean the catalyst on top of photoresist pattern. After 10 minutes, the quartz substrates were washed with acetone solution followed IPA solution and finally DI water rinse.

3.4 Growth of aligned CNTs

Aligned CNTs were grown using thermal chemical vapor deposition (TCVD) method. Figure 3.2 shows the SEM images of aligned CNTs prepared using the following procedures. The quartz substrates coated with patterned ferritin catalyst were inserted into quartz tube and heated up to 800°C in the air and maintained for 5 minutes. It was important to take note that the gas flow direction must be perpendicular to the patterned line on the quartz substrates for successful growth of highly horizontal aligned CNTs. After 5 minutes, the quartz samples were cooled down to around 200°C. Next, quartz tube was enclosed and argon gas of 200 sccm flow rate was turned on for 1 minute to eliminate the air inside the quartz tube. Subsequently, argon gas was turned off and hydrogen gas of 100 sccm flow rate was turned on and the quartz samples inside the quartz tube are heated up to 925°C and maintained for 3 minutes. After maintaining for 3 minutes at 925°C, hydrogen gas flow rate was changed to 30 sccm and argon gas of 50 sccm flow rate was turned on by flowing through a bubbler filled with ethanol for 40 minutes to 1 hour. After process finished, the heater and bubbler were turned off and the quartz samples were cooled down to room temperature before taken out from the quartz tube.

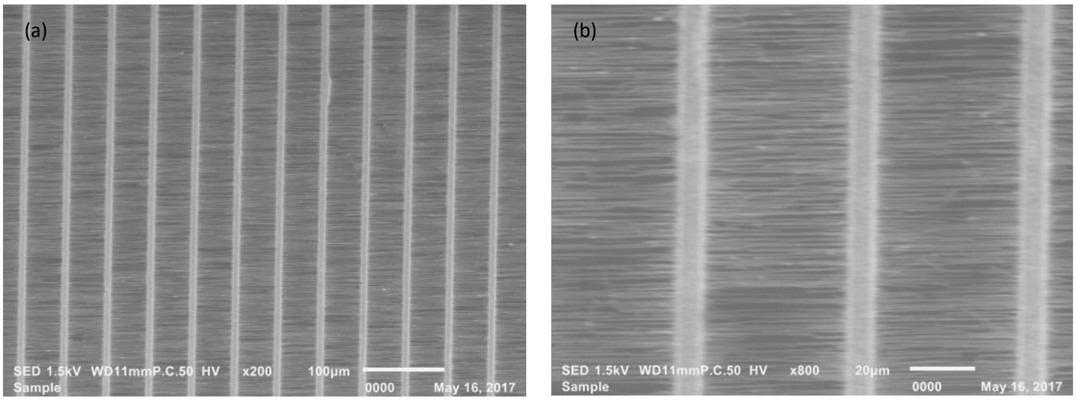


Figure 3.2: The SEM images of aligned CNTs. Aligned CNTs under (a) x200 magnification and (b) x800 magnification in SEM.

3.5 Preparation of CNT suspension

CNT can be delivered using costing CNT suspension. First, sodium dodecyl sulphate (SDS) surfactants 1%wt with DI water was prepared. SWCNTs powder was then mixed into SDS surfactants and tip-sonication for 1 hour. Blank substrates were clean by immersed into the acetone solution and ultrasonic for 10 minutes followed by IPA solution and ultrasonic for another 10 minutes. Then, the substrates were treated with piranha solution for 20 minutes to make the surface hydrophilic. APTES solution with ratio of 1:10 to IPA solution was prepared. After piranha solution treatment, the substrates were cleaned with DI water and immersed into the APTES solution for 1-2 hours. Next, the substrates were removed from the APTES solution and cleaned with IPA solution and blew dry. This was followed by immersing the substrates into the CNTs suspension prepared for 1-2 hours. Lastly, the samples with CNTs suspension were removed from the solution and cleaned gently with DI water and blew dry. Figure 3.3 shows the SEM image of the CNT network prepared using CNT suspension and the Raman spectrum of the CNT network proved that SWCNTs are deposited on the substrate.

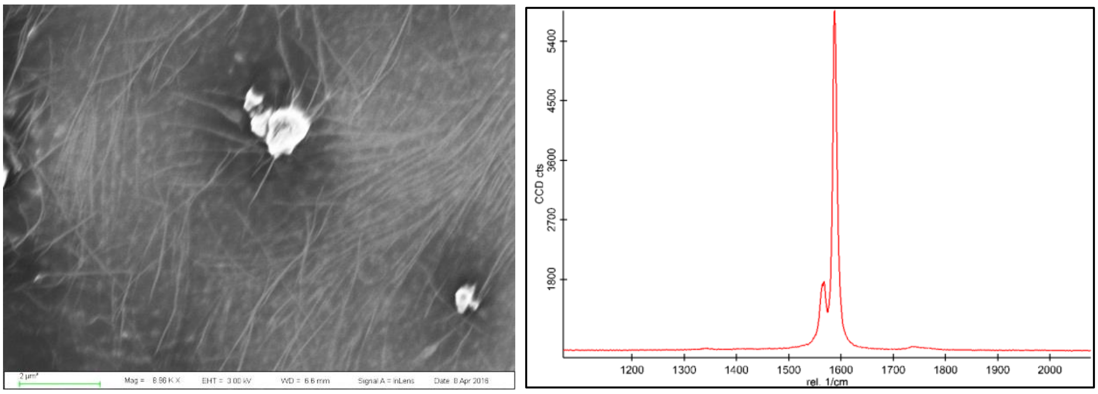


Figure 3.3: The SEM image of CNTs network deposited using the CNT suspension and the Raman spectral of the SWCNTs network deposited.

3.6 CNT transfer process

To make the top CNT electrode of CNTs based RRAM devices, we need to transfer the CNTs to the top of the resistive switching layer. The procedures were started by first spin coat PMMA onto the samples with TCVD grown CNTs or CNTs suspension. The samples with PMMA were then baked for 1 minutes on a hotplate of 105°C. Afterwards, the PMMA on the four sides of the samples were cleaned for better transfer of CNTs. Potassium hydroxide (KOH) solution with ratio of 5.6g KOH to 100 ml DI water was prepared and the samples were immersed into the KOH solution for several hours to etch away the SiO_2 underneath the CNTs network to separate the CNTs network from the substrate. The PMMA layer with the CNTs network will be lifted off and then it was transferred to the desired sample. The samples with PMMA were dried in the air until no water drops were seen in between the PMMA layer and the substrate. The samples were then heated up to 80°C and increased the temperature by 10°C for every 2 minutes until 160°C for better adhesion of the CNTs network to the substrate. The samples stayed at 160°C for 10 minutes and then decreased the temperature by 10°C for every 2 minutes until 80°C and cooled down to room temperature. The PMMA layer was then removed by acetone solution and the CNTs network were transferred to the new substrate. Figure 3.4 shows the SEM images of the transferred top CNTs on top of bottom CNTs and contacts separated by resistive switching layer.

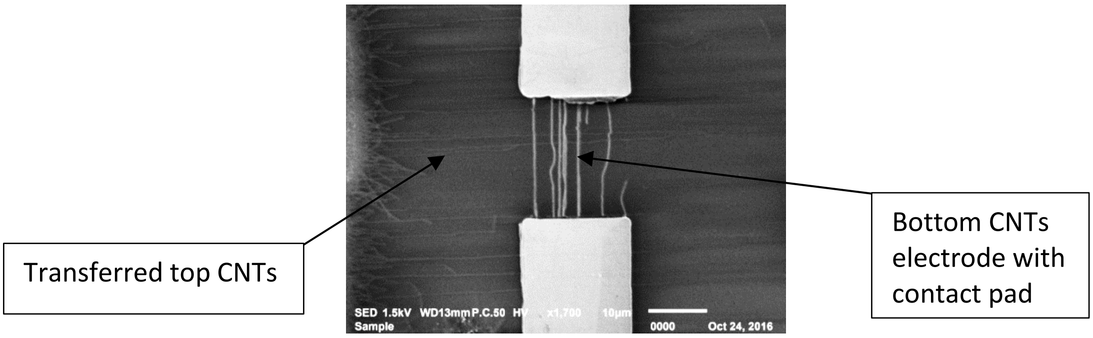


Figure 3.4: The transferred top CNTs on the samples with the bottom CNTs and contacts.

3.7 Fabrication of metal electrode RRAM devices

Metal electrode RRAM were fabricated and tested for better understanding of the conduction path formation in the resistive switching layer and a better comparison with CNTs electrode RRAMs. In these experiments, titanium/gold electrodes were used as the metal electrodes. The metal electrodes fabricated were 10um width and the active area was 10um x 10um. 10nm and 15nm thick Al_2O_3 layers were deposited using e-beam evaporation and ALD techniques as the resistive switching material to study the effects of the layer deposition condition and thickness on conduction path formation. First, photoresist was spin coated onto the blank SiO_2/Si samples for patterning the bottom metal electrode. Next, lithography was performed to create the photoresist openings. Titanium/gold electrode was deposited onto the samples with the photoresist openings using e-beam evaporation. The metal deposited on top of photoresist was removed by lift-off process. Another photoresist was spin coated onto the samples for bottom metal contact pad. Lithography was performed to create the contact pad pattern for e-beam evaporation deposition of titanium/gold. Titanium/gold was then deposited using e-beam evaporation and followed by lift-off process to remove the metal deposited on top of photoresist. After the completion of bottom electrode, a thin layer of aluminum oxide (Al_2O_3) which used as the resistive switching layer was deposited using atomic layer deposition (ALD). The ALD used Trimethylaluminum (TMA) precursor as the source together with water pulse for Al_2O_3 deposition. One cycle of TMA precursor pulse and water pulse was approximately equal to 1Å. After resistive switching layer deposition, bottom electrode formation was done by first spin coated the photoresist and followed by lithography process to create the electrode patterning for e-beam evaporation deposition of titanium/gold. Titanium/gold was then deposited on the samples using e-beam evaporation and the metal deposited on top of photoresist was removed by lift-off process. Finally, photoresist spin coat and lithography process were performed for top metal contact pad. This was followed by top metal electrode titanium/gold deposition using e-beam evaporation and unwanted metal deposited was removed by lift-off process. Figure 3.5 shows the optical images and cross section for metal electrode RRAM.

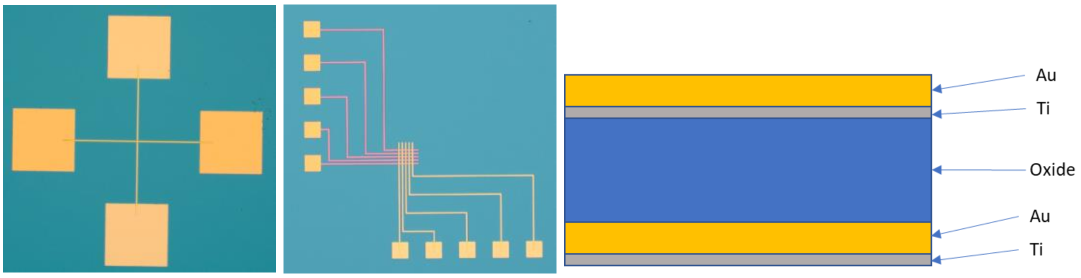


Figure 3.5: The optical images and cross section for single crossbar metal electrode RRAM (10um electrode width) and 5x5 array metal electrode RRAM (10um electrode width).

3.8 Fabrication of metal-CNT electrode RRAM devices

In this work, aligned CNTs were used as the bottom electrode and metal electrode was used as the top electrode for RRAMs. The fabrication processes were started with photoresist spin coating for bottom metal contact pad on quartz samples with TCVD grown aligned CNTs. Lithography was then performed to create the photoresist openings and titanium/gold contact was deposited using e-beam evaporation. Lift-off process was performed to remove the metal on top of photoresist. Next, palladium was deposited as a mask for bottom CNTs etching using e-beam evaporation. Lithography was performed to create the electrode pattern for palladium etching. Palladium etchant was then used to etch away unwanted palladium. The samples were then proceeded to O_2 plasma etching to remove CNTs outside of the electrode. After that, a thin layer of Al_2O_3 was deposited using ALD system as the resistive switching layer. Lithography was then performed to create the top metal electrode and contact pad after spin coated photoresist on the samples. Titanium/gold was then deposited using e-beam evaporation and the processes were finished with the lift-off process to remove metal on top of the photoresist. Figure 3.6 shows the SEM images of bottom CNT electrode. Optical image and cross section for metal-CNT electrode RRAM are shown in Figure 3.7.

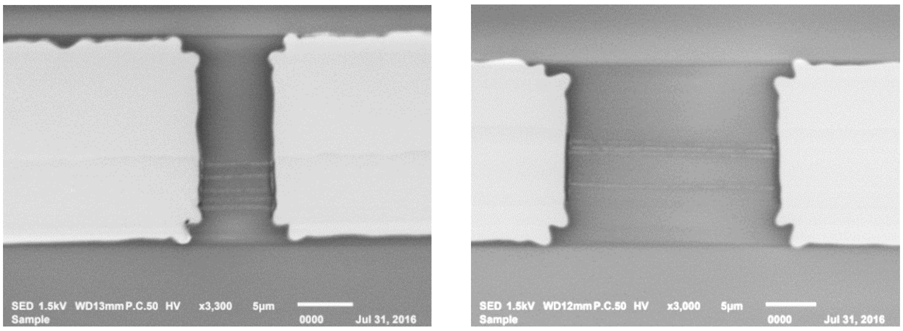


Figure 3.6: The SEM images for bottom aligned CNTs electrode. The aligned CNTs electrode is formed by deposited the metal contact pad onto the aligned CNTs and then followed by the O_2 plasma to etch away unwanted CNTs outside of the electrode.

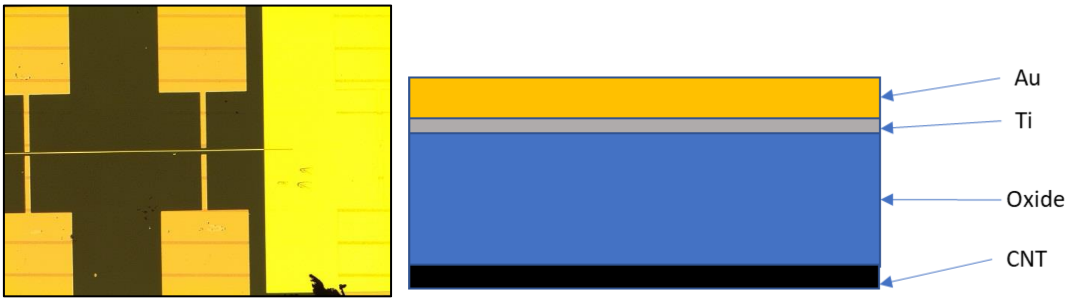


Figure 3.7: The optical image and cross section for metal-CNT electrode RRAM devices.

3.9 Fabrication of random network CNTs electrode RRAM devices

In this work, random network CNTs were used as the electrodes for RRAM. Different widths of CNTs electrodes including 10um, 15um and 100um were fabricated and tested. 10nm and 15nm thick Al_2O_3 films were deposited as the resistive switching material using E-beam evaporation and ALD deposition. The procedures were started by first spin coated the photoresist on top of SiO_2/Si substrates with TCVD grown CNTs network or CNTs suspension. Lithography was the performed to create the photoresist openings for metal contact pad. Subsequently, titanium/gold contact were deposited using e-beam evaporation and followed by lift-off process to remove unwanted metal on top of the photoresist. Next, palladium was deposited as a mask for bottom CNTs etching using e-beam evaporation. Lithography was performed to create the electrode pattern for palladium etching. Palladium was etched using palladium etchant to form the mask for CNTs etching. O_2 plasma was then used to etch away unwanted CNTs outside of the electrode area and remaining photoresist and palladium were removed. After that, a thin layer of Al_2O_3 was deposited as the resistive switching layer using ALD system. Top CNTs was transferred to the samples and photoresist was spin coated onto the samples for top metal contact pad lithography. Lithography was then performed to create the photoresist openings followed by titanium/gold contact deposition using e-beam evaporation and lift-off process was done to remove unwanted metal on top of the photoresist. Palladium again was deposited as a mask for top CNTs etching using e-beam evaporation. Lithography was performed to create the electrode pattern for palladium etching. Palladium was then etched using palladium etchant to create a mask for CNTs etching. O_2 plasma was done to etch away unwanted CNTs and finally remaining photoresist and palladium were removed. Figure 3.8 shows the optical images and cross section of a random network CNT electrode RRAM.

Figure 3.8: The optical image and cross section for CNT electrode RRAM (10um electrode width).

3.10 Fabrication of CNT-CNT electrode RRAM devices

In this work, aligned network CNTs were used as the electrodes for RRAMs. E-beam evaporation and ALD deposition of thin Al_2O_3 films were fabricated for testing as well. 10nm and 15nm thick Al_2O_3 films were deposited as the resistive switching material. First, photoresist was spin coated onto the quartz samples with TCVD grown aligned CNTs. Lithography was then performed to create the photoresist openings. Titanium/gold was deposited using e-beam deposition and followed by lift-off process to remove the metal on top of the photoresist. Then, palladium was deposited as a mask for bottom CNTs etching using e-beam evaporation and lithography was performed to create the electrode pattern for palladium etching. Palladium was etched with palladium etchant and O_2 plasma was performed to etch away unwanted CNTs. After photoresist and palladium removal, a thin layer of Al_2O_3 was deposited using ALD system. Next, top CNTs was transferred to the samples. Lithography was performed after spin coated photoresist for top metal contact pad. Titanium/gold was then deposited using e-beam evaporation and the metal on top of photoresist was removed by lift-off process. Palladium was deposited as a mask for top CNTs etching using e-beam evaporation and lithography was performed after photoresist spin coated to create the electrode pattern. Palladium was etched with palladium etchant to create a mask for CNTs etching. O_2 plasma was then performed to etch away unwanted CNTs and the processes finished with the removal of remaining photoresist and palladium. Figure 3.9 shows the SEM image for aligned network CNT RRAM.

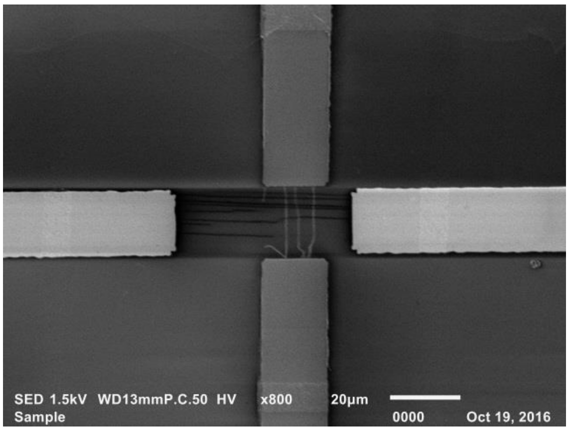


Figure 3.9: The SEM image for aligned network CNT RRAM.

Chapter 4 Characterization of Metal Electrode RRAM

In this chapter, the metal electrode RRAM devices were characterized and discussed. Single and bi-layer metal oxide layers were employed as the resistive switching dielectric. The influences of dielectric materials and their thickness on the memory performance were discussed. Figure 4.1 shows the fabrication process for the metal electrode RRAM.

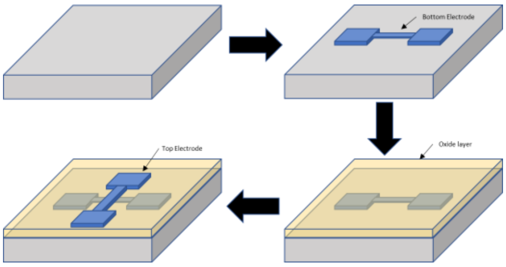


Figure 4.1: Fabrication process for the metal electrode RRAM.

4.1 Metal electrode RRAM with Al_2O_3 oxide layer

In the metal electrode RRAM devices, titanium/gold with thickness of 10 nm/30 nm respectively were used as the bottom and top electrode. The width of the electrodes was 10 um and the dimension of the RRAM devices was 10x10 um^2. Figures 4.2 to 4.9 show the memory I-V characteristics for the metal electrode RRAM devices with a single 10 nm thick ALD grown Al_2O_3 layer.

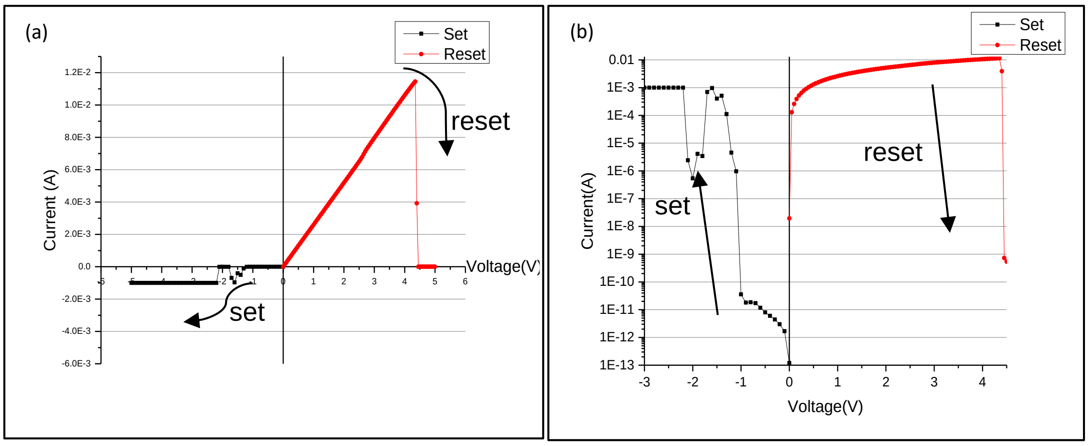


Figure 4.2: The 1st set and reset cycle for metal electrode RRAM. (a) Linear scale I-V characteristic and (b) $\log_{10}$ scale I-V characteristic for the first cycle.

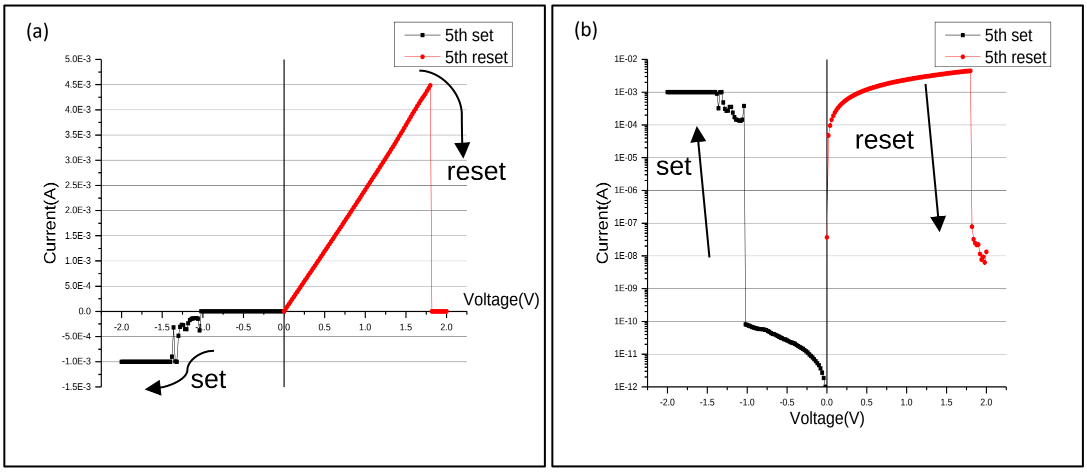


Figure 4.3: The 5th set and reset cycle for the same metal electrode RRAM. (a) Linear scale I-V characteristic and (b) $\log_{10}$ scale I-V characteristic for the 5th cycle.

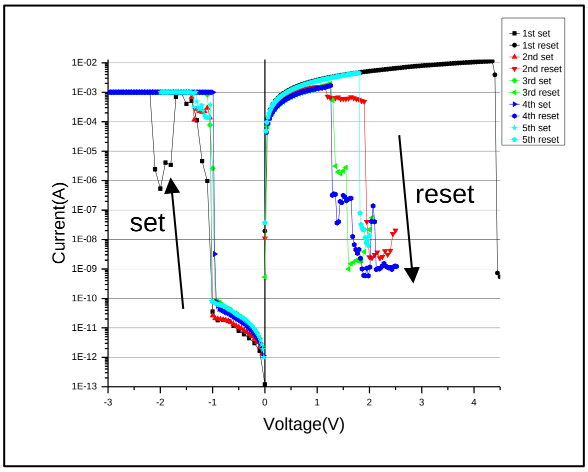


Figure 4.4: The memory I-V characteristic shows the 1st to 5th set and reset cycles. First set (black curve) requires higher voltage to switch to LRS as this is the forming process. The set and reset voltage occurred at around -1V and 1.5-2V respectively.

Figure 4.2 shows the 1st set and reset cycle for a metal electrode RRAM device with a single 10 nm thick ALD grown Al_2O_3 layer. The initial resistance was ~50GΩ which was the high resistance state (HRS). After setting at -2.2V, the resistance reduced to ~404Ω which was the low resistance state (LRS). The device could be reset at +4.5V.

On/off ratio was ~1 x 10^8. Figure 4.3 shows the 5th set and reset cycle. HRS was ~20GΩ. After set at -1.4V, the resistance changed to 420Ω. Reset voltage was +1.82V and on/off ratio is ~4 x 10^7. From Figure 4.4, one can see that after 1st set and reset cycle, the set and reset voltage was relatively stable at ~ -1V and 1.5V-2V, respectively.

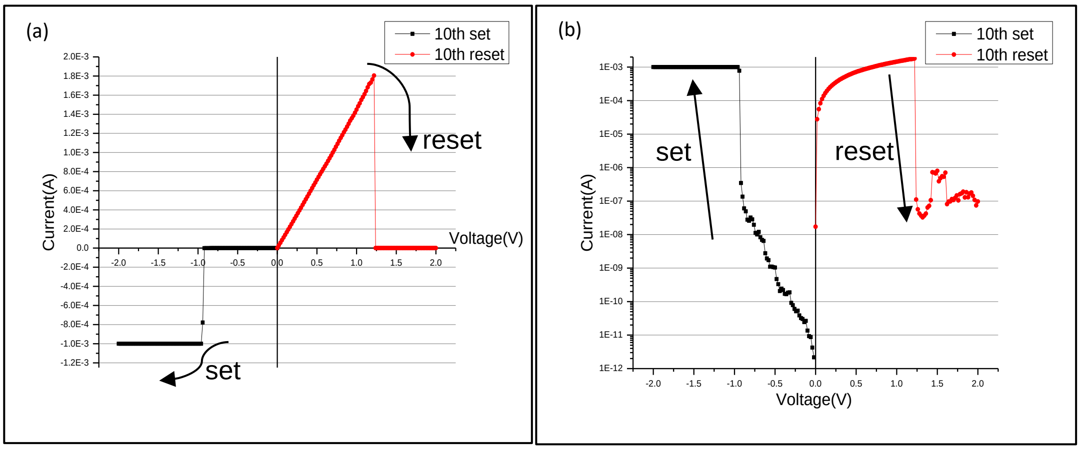


Figure 4.5: The 10th set and reset cycle for the same metal electrode RRAM. (a) Linear scale I-V characteristic and (b) $\log_{10}$ scale I-V characteristic for the 10th cycle.

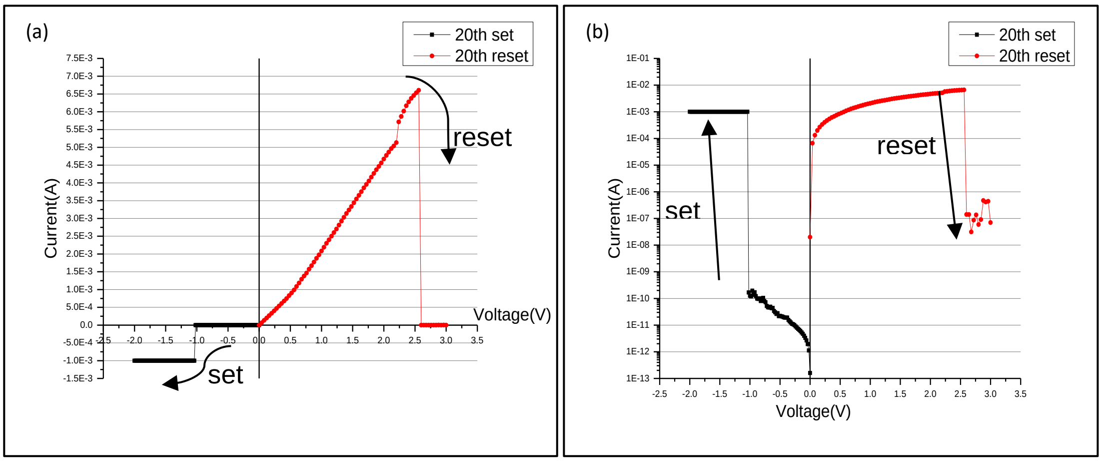


Figure 4.6: The 20th set and reset cycle for the same metal electrode RRAM. (a) Linear scale I-V characteristic and (b) $\log_{10}$ scale I-V characteristic for the 20th cycle.

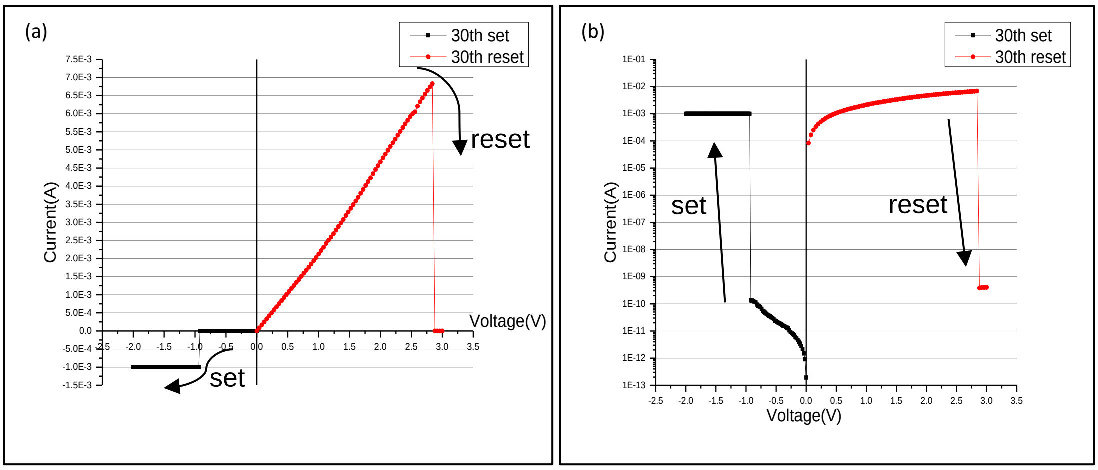


Figure 4.7: The 30th set and reset cycle for the same metal electrode RRAM. (a) Linear scale I-V characteristic and (b) $\log_{10}$ scale I-V characteristic for the 30th cycle.

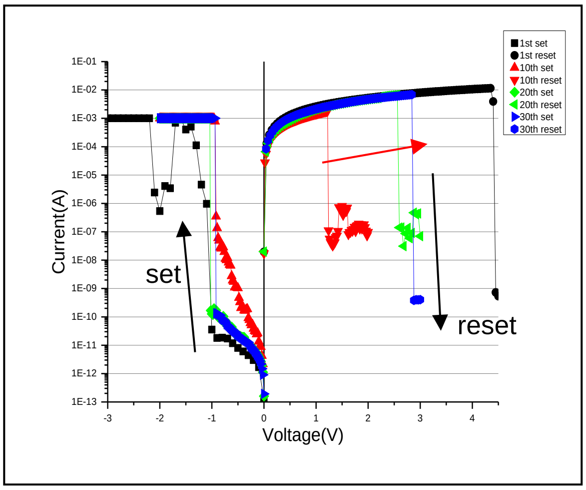


Figure 4.8: The memory I-V characteristic shows the 1st, 10th, 20th and 30th set and reset cycles. The reset voltage gradually increases as more cycles performed (red arrow). The 1st cycle (black curve) is omitted as it is the forming process.

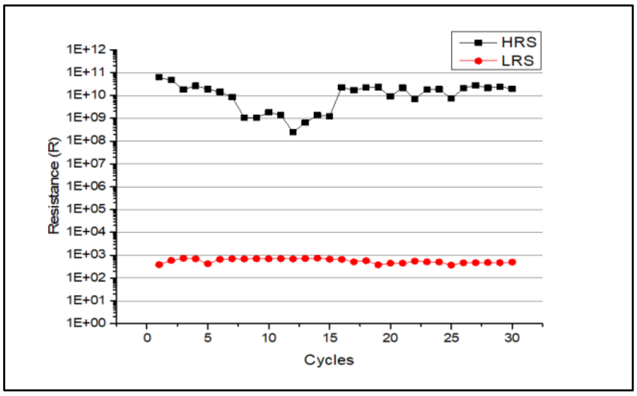


Figure 4.9: The HRS and LRS vs the switching cycles of the metal electrode RRAM

device. The metal electrode RRAM device shows relatively stable LRS and a slight fluctuation on the HRS over 30 switching cycles.

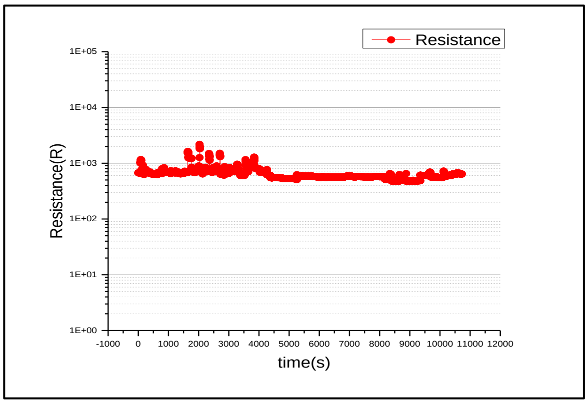


Figure 4.10: The retention performance of the metal electrode RRAM device shown in Figure 4.2-4.8.

From Figure 4.5 to Figure 4.7, one can see that the set and reset voltages slightly increased while the on/off ratio maintained at ~10^7. Figure 4.8 shows the reset voltage slowly increased from about 1.2V for the 10th cycle to about 3V for the 30th cycle. Figure 4.9 shows the HRS and LRS vs the switching cycles. The metal electrode RRAM showed relatively stable for the LRS while a slight fluctuation for the HRS. The fluctuation of the HRS could result from the conductive path formed in the oxide layer. As the device reset back to HRS, the conductive path is not completely vanished. Instead, part of the conductive path remained in the oxide layer while only a fraction of the conductive path is annihilated. The remained conductive path distance would affect the overall resistance. Hence, when the remained conductive path distance is varied for every cycle, the HRS will varied as well. Figure 4.10 shows the retention of the metal electrode RRAM. The device could maintain its LRS stable for 1 x 10^4s without any problem.

E-beam deposited single Al_2O_3 layer was also tested and showed similar set and reset voltages as those with ALD deposited single Al_2O_3 layer. However, the e-beam deposited Al_2O_3 could only last for a few cycles before the devices burned out. This could be due to poor quality of e-beam Al_2O_3 as compared to ALD Al_2O_3. 15nm thick Al_2O_3 layer was engaged, as shown in Figure 4.11. The set and reset voltage were at -12V and +10V, respectively, and were much higher than that of 10nm thick Al_2O_3 devices. This is due to thicker Al_2O_3 required higher voltages to annihilate and re-form the conductive path in the single Al_2O_3 layer.

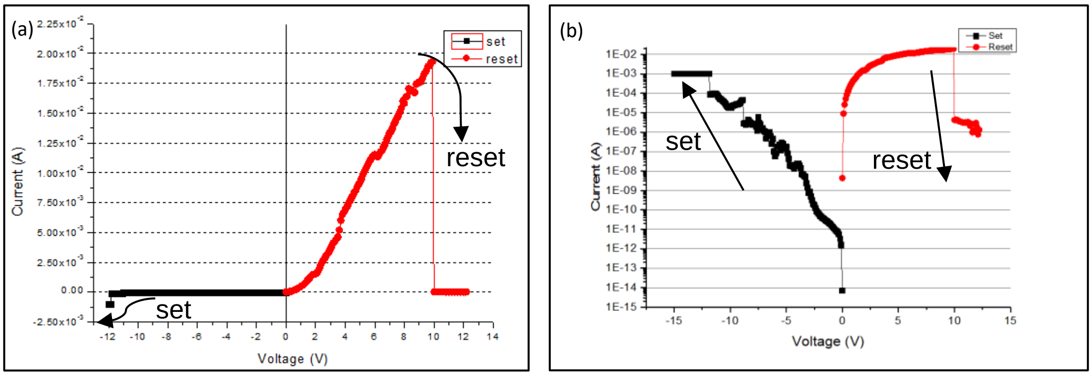


Figure 4.11: The 1st set and reset cycle I-V characteristic for the 15nm ALD grown Al_2O_3 RRAM in (a) linear scale and (b) $\log_{10}$ scale.

4.2 Comparison between different metal oxide layers

The impacts of the oxide layer thickness and different oxide materials on the resistive switching performance were examined to achieve a better understanding on the influence of oxide layer on the memory performance and improve the device performance. Three single layer hafnium oxide (HfO_2), aluminum oxide (Al_2O_3) and zirconium oxide (ZrO_2) deposited using the ALD system were engaged. For each oxide layer, three different thickness, 3nm, 5nm and 10nm were fabricated. The I-V characteristics of each oxide layer of different thickness are compared in the table 4.1.

4.2.1 Metal electrode RRAM with Al_2O_3 oxide layer

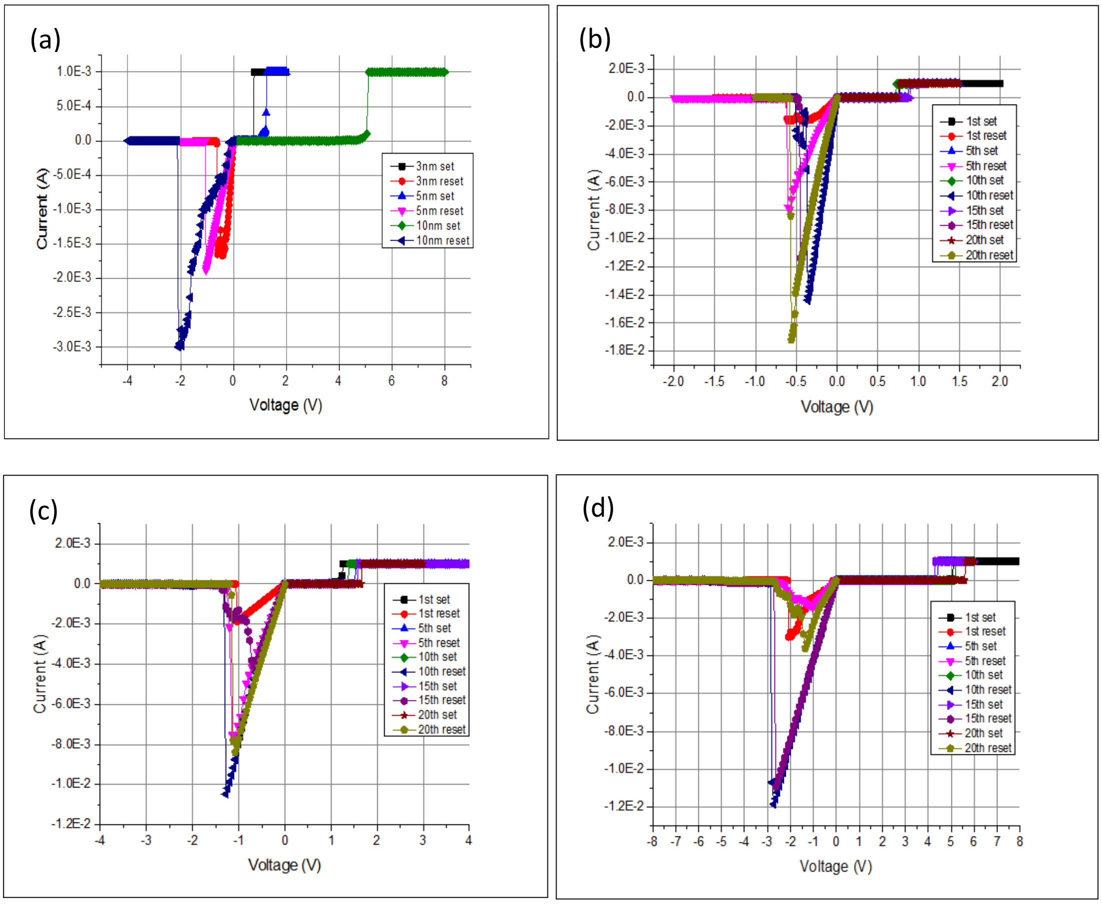


Figure 4.12: (a) The I-V characteristics of the metal electrode RRAM devices in which the Al_2O_3 layer thickness was 3nm, 5nm and 10nm, respectively. (b) The I-V characteristics of the RRAM device with 3nm thick Al_2O_3 layer. (c) The I-V characteristics of the RRAM device with 5nm thick Al_2O_3 layer. (d) The I-V characteristics of the RRAM device with 10nm thick Al_2O_3 layer.

Figure 4.12(a) shows the I-V characteristic of metal electrode RRAM devices in which the Al_2O_3 layer thickness was 3nm, 5nm and 10nm, respectively. As the Al_2O_3 layer thickness increased from 3nm to 10nm, the set and reset voltage increase from 0.6V to 2.5V and from -0.6V to -2.1V, respectively. Thus, the thicker the Al_2O_3 layer was, higher the voltage was required to form and annihilate the conductive paths in the oxide layers. Figures 4.12(b), (c) and (d) show the cycle performance of the metal electrode

RRAM devices with Al_2O_3 layer thickness of 3nm, 5nm and 10nm, respectively. The set voltage was found to be relatively stable while the reset voltage showed slight fluctuation from cycle to cycle.

4.2.2 Metal electrode RRAM with HfO_2 oxide layer

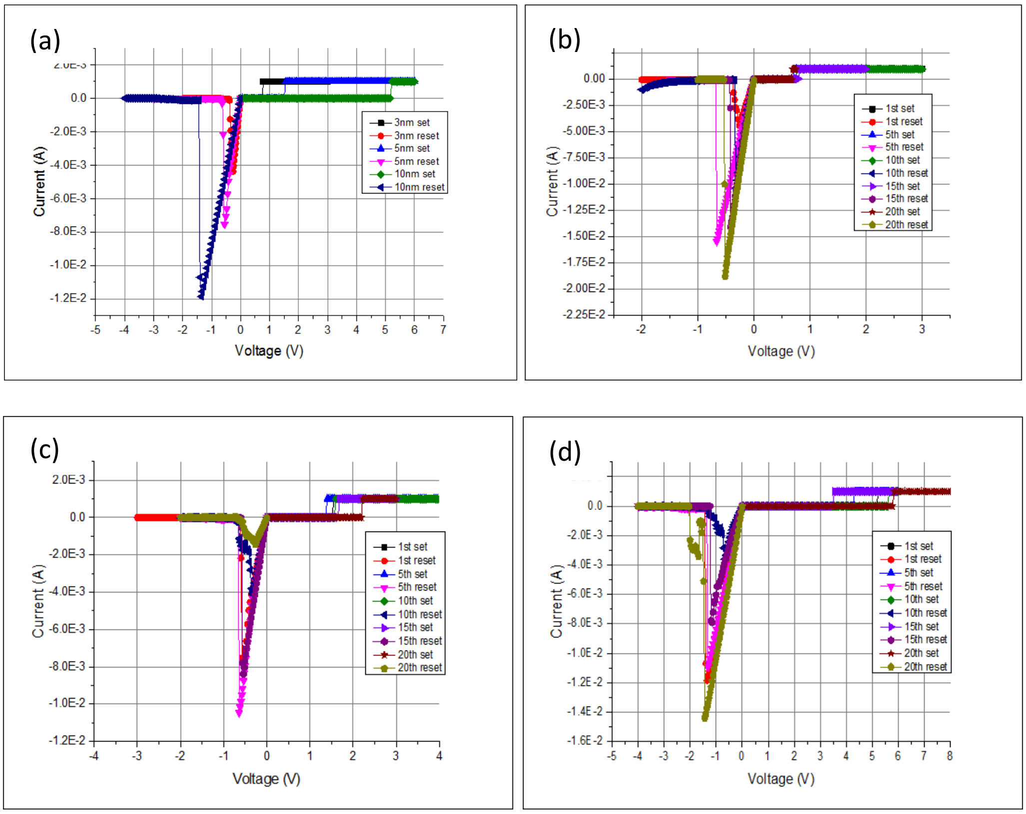


Figure 4.13: (a) The I-V characteristics of the metal electrode RRAM devices in which the HfO_2 layer thickness was 3nm, 5nm and 10nm, respectively. (b) The I-V characteristics of the RRAM device with 3nm thick HfO_2 layer. (c) The I-V characteristics of the RRAM device with 5nm thick HfO_2 layer. (d) The I-V characteristics of the RRAM device with 10nm thick HfO_2 layer.

Figure 4.13(a) shows the I-V characteristic of the metal electrode RRAM devices in which the HfO_2 layer thickness was 3nm, 5nm and 10nm, respectively. As the HfO_2 layer thickness increased, the set and reset voltage increased from 0.8V to 5.0V and from -0.4V to -1.5V, respectively. Figures 4.13(b), (c) and (d) show the cycle performance of the three metal electrode RRAM devices. The set voltage was relatively stable except slight increasing for the 10nm thick HfO_2 layer. The reset voltage showed slight fluctuation from cycle to cycle.

4.2.3 Metal electrode RRAM with ZrO_2 oxide layer

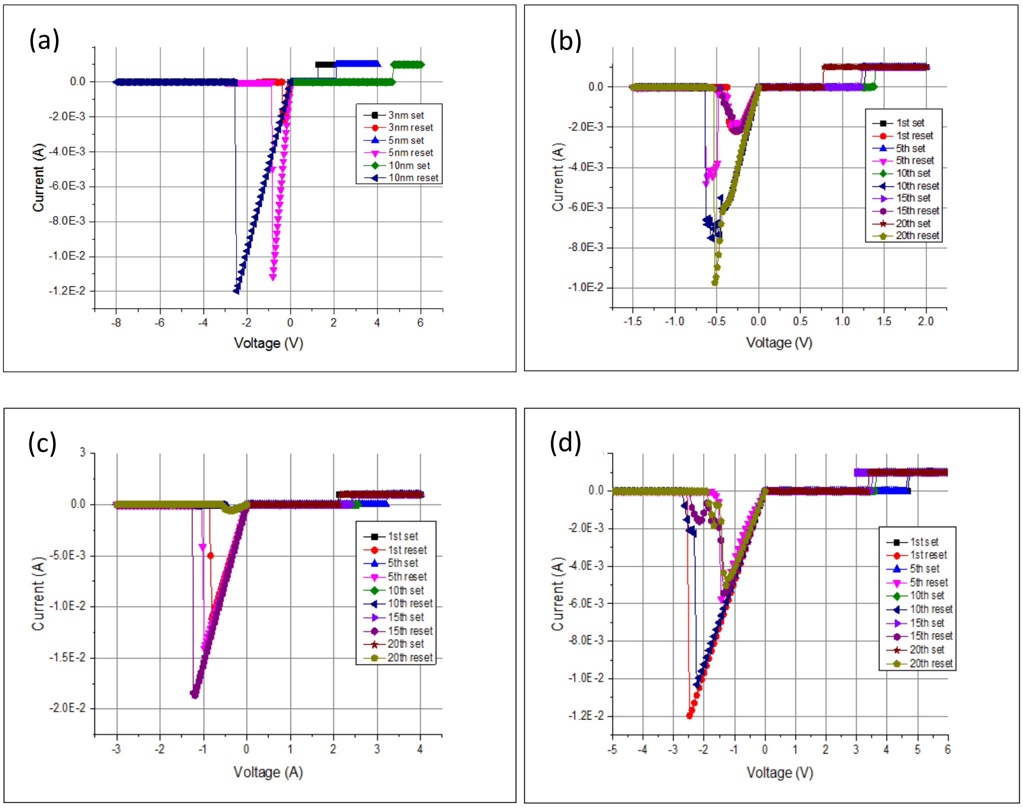


Figure 4.14: (a) The I-V characteristics of the metal electrode RRAM devices in which the ZrO_2 layer thickness was 3nm, 5nm and 10nm, respectively. (b) The I-V characteristics of the RRAM device with 3nm thick ZrO_2 layer. (c) The I-V characteristics of the RRAM device with 5nm thick ZrO_2 layer. (d) The I-V characteristics of the RRAM device with 10nm thick ZrO_2 layer.

Figure 4.14(a) shows the I-V characteristic of the metal electrode RRAM devices in which the ZrO_2 layer thickness was 3nm, 5nm and 10nm, respectively. As the ZrO_2 layer thickness increased, the set and reset voltage increased from 1.2V to 4.8V and from -0.4V to -2.5V, respectively. Figure 4.14(b), (c) and (d) show the cycle performance of the three metal electrode RRAM devices. The set voltage was relatively stable while the reset voltage showed slight fluctuation from cycle to cycle.

4.2.4 Comparison between different oxide layer and thickness

The set and reset voltages for metal electrode RRAM devices in which Al_2O_3, HfO_2 or ZrO_2 oxide layer was employed as the resistive switching layer are summarized in table 4.1.

Oxide layer	Thickness	Set voltage	Reset voltage
Al_2O_3	3nm	0.6V	-0.6V
	5nm	1.2V	-1.1V
	10nm	2.5V	-2.1V
HfO_2	3nm	0.8V	-0.4V
	5nm	1.5V	-0.6V
	10nm	5.0V	-1.5V
ZrO_2	3nm	1.2V	-0.4V
	5nm	2.1V	-0.9V
	10nm	4.8V	-2.5V

Table 4.1: Comparison of the set and reset voltages for the metal electrode RRAM devices with Al_2O_3, HfO_2 or ZrO_2 layer as the resistive switching layer.

All memory devices have showed a bipolar switching behavior. As explained in chapter 2.3.3, the set and reset voltages are in the opposite polarity for bipolar switching. Hence, all memory devices using Al_2O_3, HfO_2 or ZrO_2 layer as the resistive switching layer which set at positive voltage and reset at negative voltage exhibit a bipolar switching behavior.

Chapter 5 Characterization of CNTs Electrode RRAM

CNTs electrode RRAM are characterized and discussed in this chapter. The CNTs electrode RRAM devices contain metal-CNT electrode RRAMs, random network CNTs electrode RRAMs and aligned CNTs electrode RRAMs.

5.1 Metal-CNTs electrode RRAM

In Chapter 3.8, fabrication of the metal-CNT electrode RRAM devices was discussed. In this section, the I-V characteristics for metal-CNT electrode RRAM device with 10um CNTs electrode channel width, 10um metal electrodes width and 10nm thick single ALD grown Al_2O_3 layer is shown in Figure 5.1 to Figure 5.4.

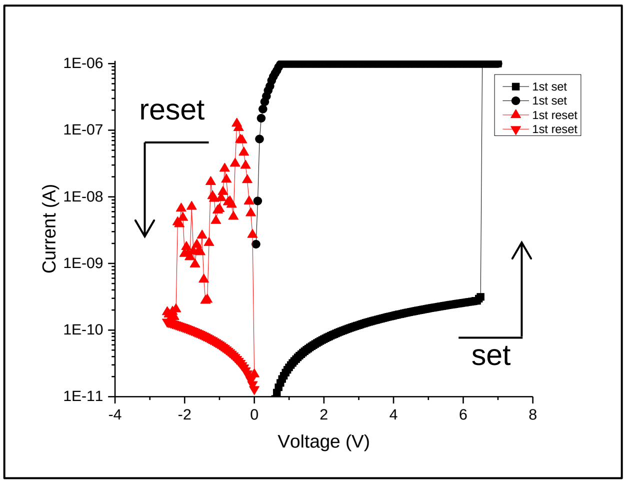


Figure 5.1: The I-V characteristic of the metal-CNT electrode RRAM device shows the 1st set and reset cycle in $\log_{10}$ scale.

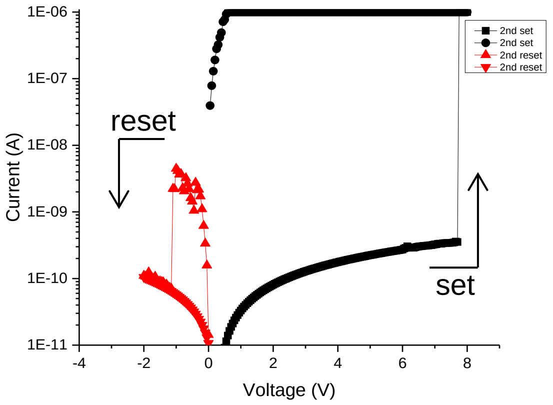


Figure 5.2: The I-V characteristic of the metal-CNT electrode RRAM device shows the 2nd set and reset cycle in $\log_{10}$ scale (the same device as shown in Figure 5.1).

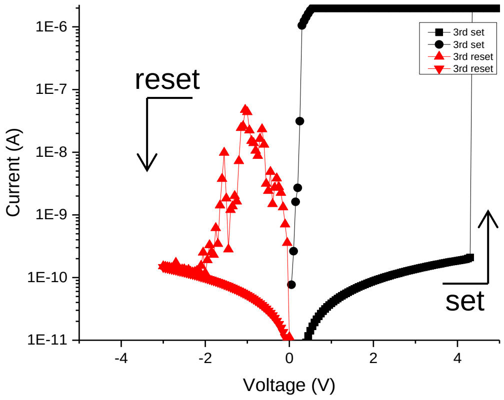


Figure 5.3: The I-V characteristic of the metal-CNT electrode RRAM device shows the 3rd set and reset cycle in $\log_{10}$ scale (the same device as shown in Figure 5.1).

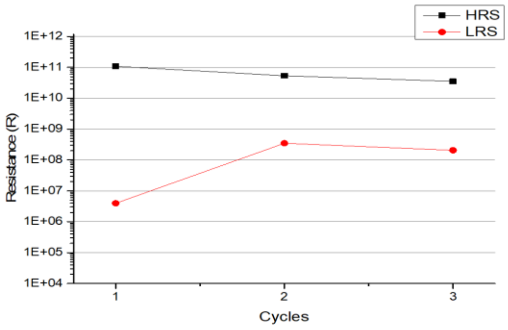


Figure 5.4: The HRS and LRS vs the switching cycles for the metal-CNT electrode

RRAM device.

Figure 5.1 shows the 1st set and reset cycle for a metal-CNT electrode RRAM device. The initial resistance for the RRAM device was ~20GΩ which was the HRS. When the voltage increased to +6.5V, the device switched to the LRS with resistance of few mega ohms. The device could be reset at -2.2V. The On/off ratio was ~1.7 x 10^3. Figure 5.2 shows the 2nd set and reset cycle for the same RRAM device. The HRS was ~20GΩ. After setting at +7.7V, the resistance changed to the LRS with resistance of few mega ohms. The reset voltage was -1.1V and the on/off ratio was ~1 x 10^2. Figure 5.3 shows the 3rd set and reset cycle for the same RRAM device. The HRS was ~20GΩ. When the applied voltage increased to +4.3V, the resistance changed to the LRS with resistance of few mega ohms. The reset voltage was -2V and the on/off ratio was ~1 x 10^2. After few switching cycles, the resistance of the LRS could return back to the initial high resistance indicating that the conductive path had poor stability in the Al_2O_3 layer. Figure 5.4 shows the HRS and LRS vs the switching cycles for the metal-CNT electrode RRAM device.

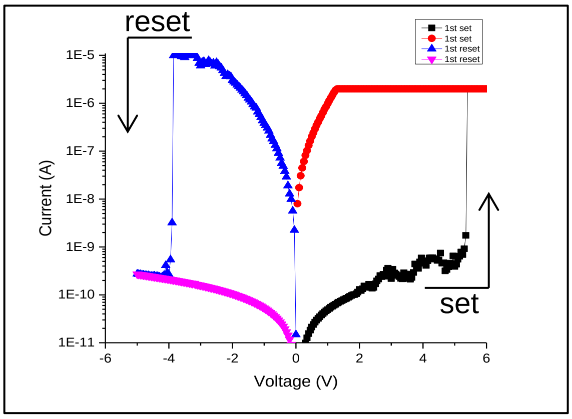


Figure 5.5: The I-V characteristic of the metal-CNT electrode RRAM device shows the 1st set and reset cycle in $\log_{10}$ scale.

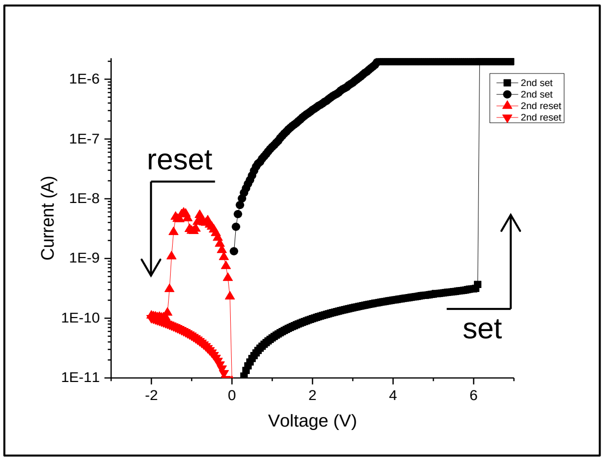


Figure 5.6: The I-V characteristic of the metal-CNT electrode RRAM device shows the 2nd set and reset cycle in $\log_{10}$ scale (the same device as shown in Figure 5.5).

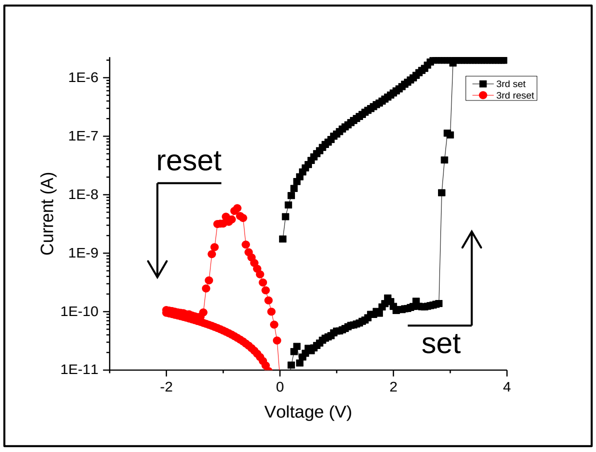


Figure 5.7: The I-V characteristic of the metal-CNT electrode RRAM device shows the 3rd set and reset cycle in $\log_{10}$ scale (the same device as shown in Figure 5.5).

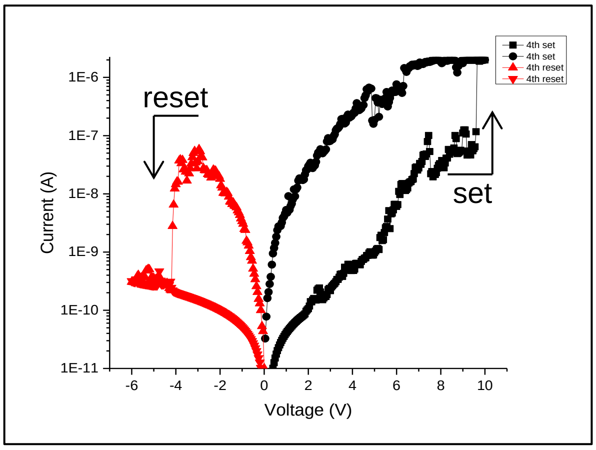


Figure 5.8: The I-V characteristic of the metal-CNT electrode RRAM device shows

the 4th set and reset cycle in $\log_{10}$ scale (the same device as shown in Figure 5.5).

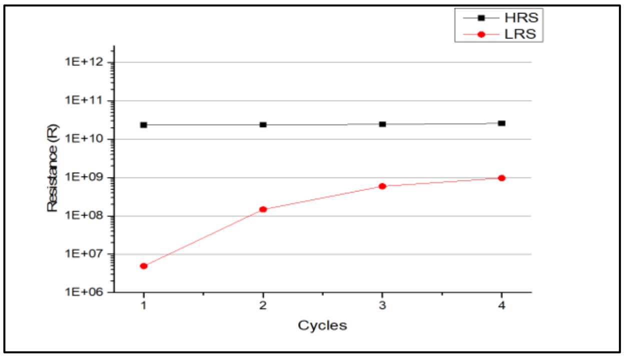


Figure 5.9: The HRS and LRS vs the switching cycles for the metal-CNT electrode RRAM device.

Figures 5.5 to 5.8 show the I-V characteristics for another metal-CNT electrode RRAM with 5um CNT electrode width, 10um metal electrode width and 10nm thick single ALD grown Al_2O_3 layer. During the first cycle, the initial resistance is ~10GΩ. When the voltage was set at +5.4V and the resistance changed to the LRS with resistance of few mega ohms. The device could be reset at -4V. The on/off ratio for first cycle was ~1 x 10^4. The second set and reset cycle occurred at +6.1V and -1.5V, respectively and the on/off ratio was ~2 x 10^2. The third cycle occurred at +3V and -1.2V, respectively for the set and reset voltage. The on/off ratio was ~1.5 x 10^2. The next set and reset cycle took place at +9.6V and -4.2V, respectively and the on/off ratio was ~1.5 x 10^2. After a few cycles, the resistance returned back to the initial high resistance. Figure 5.9 shows the HRS and LRS vs the switching cycles for the metal-CNT electrode RRAM device. The LRS gradually increased in resistance and thus reduced in the on/off ratio.

5.2 Random network CNTs electrode RRAM

In Chapter 3.9, fabrication of the random network CNTs electrode RRAM devices were discussed. The I-V characteristics showing the set and reset voltages are shown in Figure 5.10.

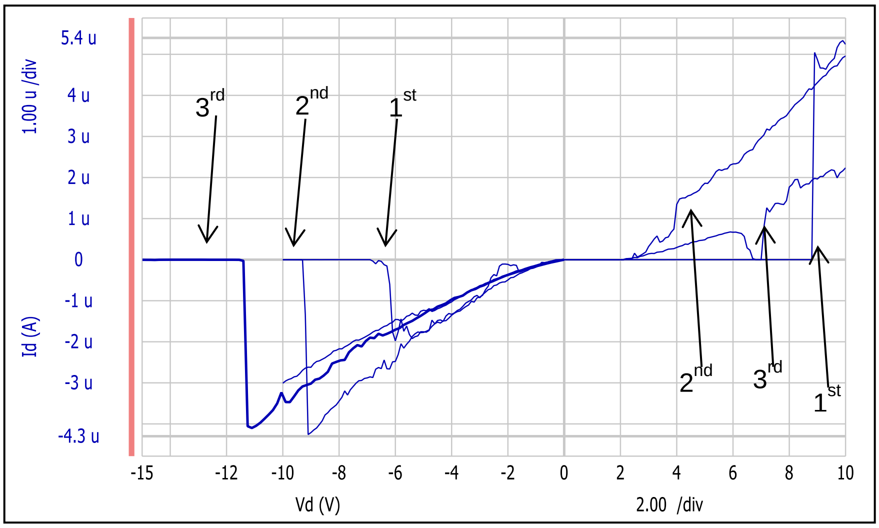


Figure 5.10: The I-V characteristic of the random network CNTs electrode RRAM device (The same device as described in Chapter 3.9).

From Figure 5.10, it can be seen that the initial resistance was at ~20GΩ. After increasing the voltage up to +8.9V, the resistance reduced to 2MΩ. The resistance of the LRS was still in the mega ohms range, much higher than that for the LRS of the metal electrode RRAM device. This could be due to the high resistance of random network CNTs electrode which were typically of few mega ohms. The on/off ratio was ~1 x 10^4. The device could be reset at -6.9V. The 2nd and 3rd reset voltage occurred at -9.4V and -11.5V, respectively. The increasing reset voltage and the gradual transition from HRS to LRS and from LRS to HRS could be due to poor uniformity of random network CNTs and the contact between random network CNTs electrode and Al_2O_3 layer. As the random network CNTs consisted of CNTs overlapped on each other, this resulted in the non-uniformity of the random network CNTs top surface which was in contacted with the Al_2O_3 layer. Hence, the random network CNTs electrode RRAM device unable to maintain a stable operating voltage and a sharp transition on the switching process.

5.3 CNT-CNTs electrode RRAM

Figure 5.11 shows an optical image of a CNT-CNT electrode RRAM device and Figure 5.12 shows the SEM image of the CNT-CNT electrode RRAM device. The pair of the Au contact pads (in dark yellow) were patterned on the two terminals of the bottom CNTs electrode. While, the pair of the Au contact pads (in bright yellow) were patterned on the two terminals of the top CNTs electrode. A resistive switching layer of 5nm thick Al_2O_3 was introduced by ALD technique in between the two CNTs electrodes. The fabrication processes of the device were discussed in Chapter 3.10. Figure 5.13 shows the I-V characteristic for a CNT-CNT electrode RRAM device which had a CNT electrode width of 10um and a resistive switching layer of 5nm thick Al_2O_3.

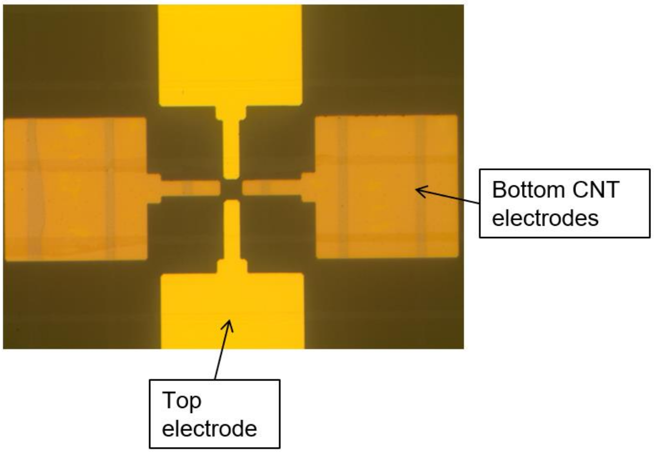


Figure 5.11: The optical image of the CNT-CNT electrode RRAM.

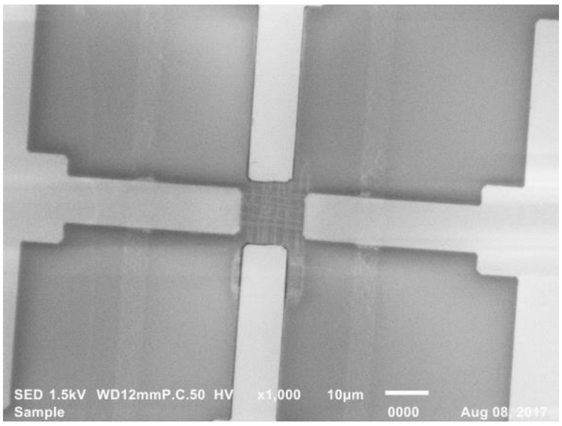


Figure 5.12: The SEM image of the CNT-CNT electrode RRAM (the same device as shown in Figure 5.11).

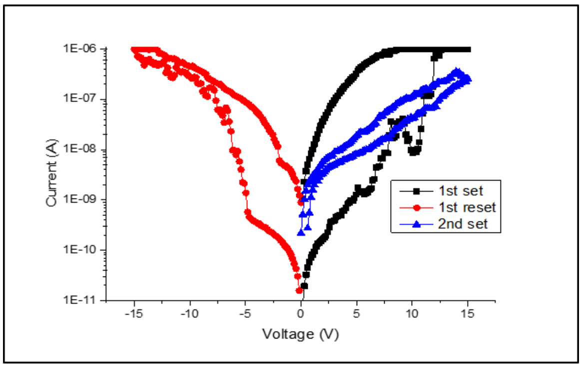
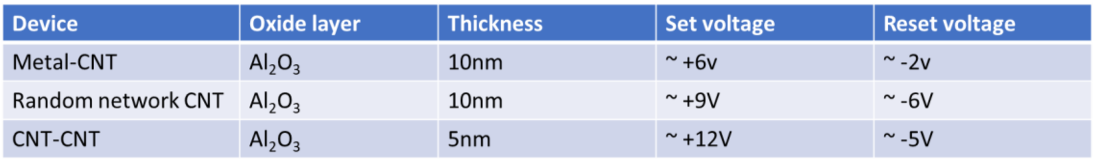


Figure 5.13: The I-V characteristic of the CNT-CNT electrode RRAM device with single Al_2O_3 resistive switching layer.

Figure 5.13 shows the I-V characteristic of the CNT-CNT electrode RRAM device. The initial resistance was roughly few GΩ. When a voltage was applied across the two CNT electrodes, the device gradually changed to LRS with a resistance of few MΩ. Subsequently, the device could be reset back to the HRS. Unfortunately, after the first cycle, the device was no longer able to be set to LRS again.



Device	Oxide layer	Thickness	Set voltage	Reset voltage
Metal-CNT	Al_2O_3	10nm	~ +6v	~ -2v
Random network CNT	Al_2O_3	10nm	~ +9V	~ -6V
CNT-CNT	Al_2O_3	5nm	~ +12V	~ -5V

Table 5.1: Comparison of the set and reset voltages for the metal-CNT, random network CNT and CNT-CNT electrode RRAM devices with Al_2O_3 layer as the resistive switching layer.

Table 5.1 shows the comparison between metal-CNT, random network CNT and CNT-CNT electrode RRAM for the set and reset voltage using Al_2O_3 layer as the resistive switching layer.

Chapter 6 Characterization of Bi-layer Resistive Switching RRAM

It has been showed that bi-layer metal oxide can improve the RRAM performance [5]. In this work, we demonstrated RRAM devices with a bi-layer resistive switching layer using metal as well as aligned SWCNTs as the electrodes. For RRAM devices with bi-layer resistive switching layer using metal electrode, Au/Ti was used as the top and bottom electrode.

6.1 Bi-layer resistive switching RRAM with metal electrodes

In this work, three different bi-layer resistive switching RRAM devices were fabricated and characterized.

Figure 6.1 shows the I-V characteristic of a metal electrode RRAM device with HfO_2/Al_2O_3 bi-layer. The 5nm thick bi-layer oxide layer consisted of 2.5nm thick HfO_2 and 2.5nm thick Al_2O_3 was deposited using ALD system. The first cycle was the forming process to establish the conductive path. The set and reset voltages were in the range from +1 to +3V and from -1V to -2V respectively. Figure 6.2 shows the HRS and LRS vs the switching cycles of the metal electrode RRAM device with HfO_2/Al_2O_3 bi-layer as the resistive switching layer. From the graph, the RRAM device shows relative stable for the LRS while a slight fluctuation for the HRS. Figure 6.3 shows the operating voltage vs the switching cycles of the metal electrode RRAM device with HfO_2/Al_2O_3 bi-layer as the resistive switching layer. Both set and reset voltages for the RRAM device showed a slight fluctuation. The device has an on/off ratio of $\sim 1x10^2$.

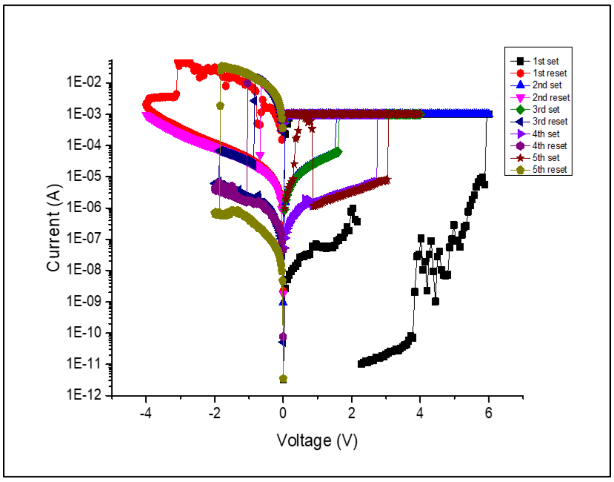


Figure 6.1: The I-V characteristic shows the 1st to 5th switching cycles of the RRAM device with a HfO_2/Al_2O_3 bi-layer as the resistive switching layer.

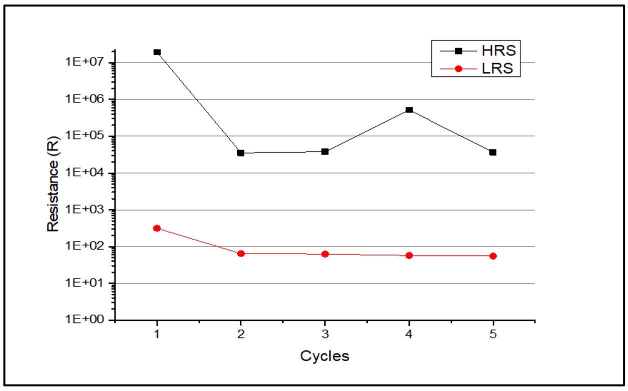


Figure 6.2: The HRS and LRS vs the switching cycles of the metal electrode RRAM device with HfO_2/Al_2O_3 bi-layer as the resistive switching layer. The metal electrode RRAM device shows relative stable for the LRS and a slight fluctuation for the HRS.

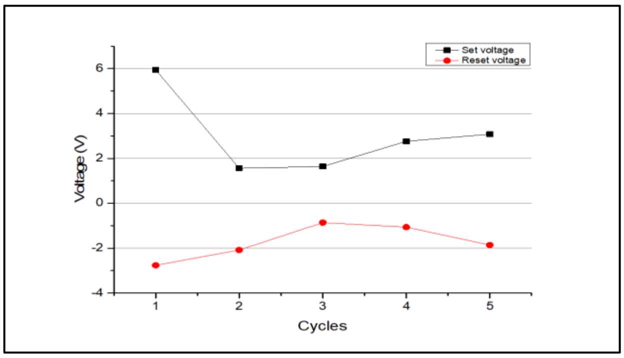


Figure 6.3: The operating voltage vs the switching cycles of the metal electrode RRAM device with HfO_2/Al_2O_3 bi-layer as the resistive switching layer. The metal

electrode RRAM shows a slight fluctuation for both set and reset voltages.

Figure 6.4 shows the I-V characteristic of a metal electrode RRAM device with ZrO_2/HfO_2 bi-layer. The 5nm thick bi-layer oxide consisted of 2.5nm ZrO_2 and 2.5nm HfO_2 was deposited using ALD system. The first switching cycle was the forming process to establish the conductive path. The set and reset voltages were +1.4V and -1V respectively. Figure 6.5 and figure 6.6 show the HRS and LRS vs the switching cycles and the operating voltage vs the switching cycles of the metal electrode RRAM device with ZrO_2/HfO_2 bi-layer as the resistive switching layer, respectively. From the two figures, it can be seen that the RRAM device with ZrO_2/HfO_2 bi-layer showed the best consistency for both HRS and LRS as well as the operating voltage compared with the other two bi-layer RRAM devices. The device has an on/off ratio of ~1x10^5.

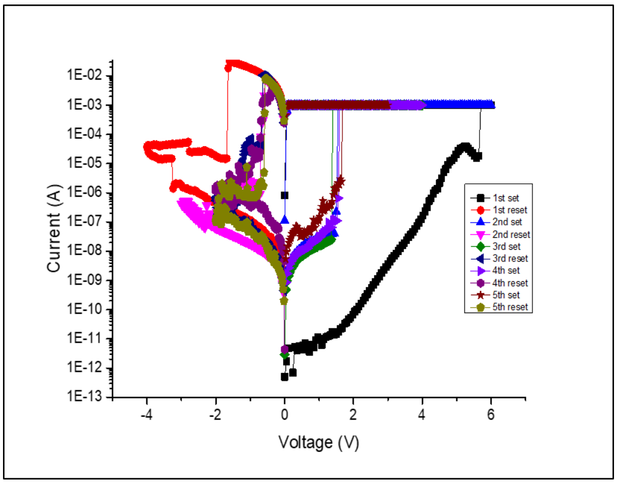


Figure 6.4: The I-V characteristic of the RRAM device with a ZrO_2/HfO_2 bi-layer as the resistive switching layer.

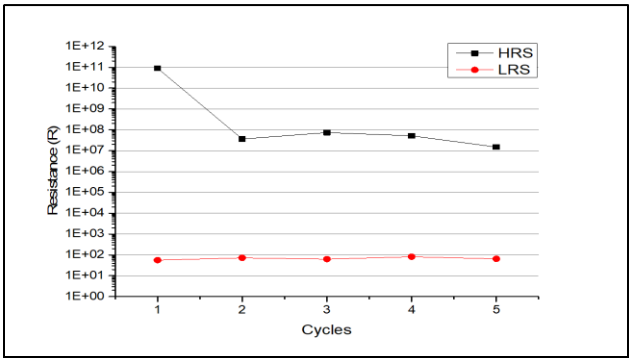


Figure 6.5: The HRS and LRS vs the switching cycles of the metal electrode RRAM device with ZrO_2/HfO_2 bi-layer as the resistive switching layer. The metal electrode RRAM device shows good stability for both HRS and LRS.

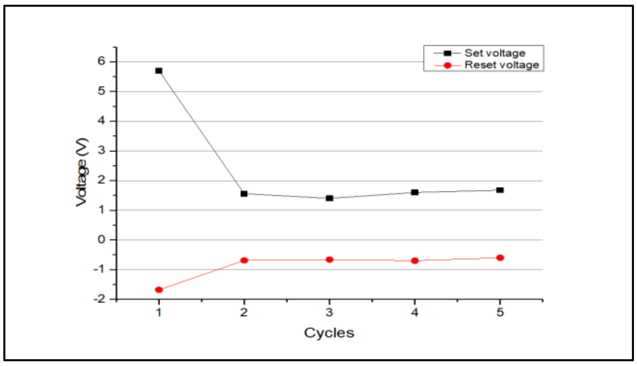


Figure 6.6: The operating voltage vs the switching cycles of the metal electrode RRAM device with ZrO_2/HfO_2 bi-layer as the resistive switching layer. The metal electrode RRAM device shows good consistency for both set and reset voltages.

Figure 6.7 shows the I-V characteristic of a metal electrode RRAM device with ZrO_2/Al_2O_3 bi-layer. The 5nm thick bi-layer oxide consisted of 2.5nm thick ZrO_2 and 2.5nm thick Al_2O_3 was deposited using ALD system. The first cycle was the forming process to establish the conductive path. The set and reset voltages were in the range of from +2.5V to +4.5V and from -1V to -1.5V respectively. Figure 6.8 shows the HRS and LRS vs the switching cycles of the metal electrode RRAM device with ZrO_2/Al_2O_3 bi-layer as the resistive switching layer. The metal electrode RRAM device shows good stability for the LRS but a slight fluctuation for the HRS. Figure 6.9 shows the operating voltage vs the switching cycles of the metal electrode RRAM device with ZrO_2/Al_2O_3 bi-layer as the resistive switching layer. From the graph, it showed that the metal electrode RRAM device had a slight fluctuation for set voltage and relative stable for the reset voltages. The device has an on/off ratio of ~$1x10^5$.

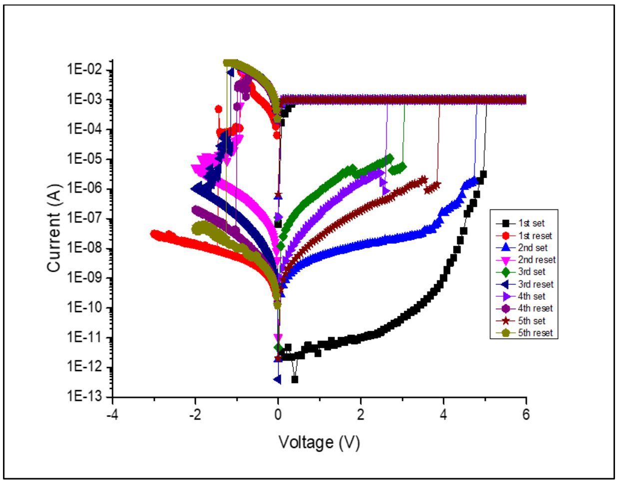


Figure 6.7: The I-V characteristic of the RRAM device with a ZrO_2/Al_2O_3 bi-layer as the resistive switching layer.

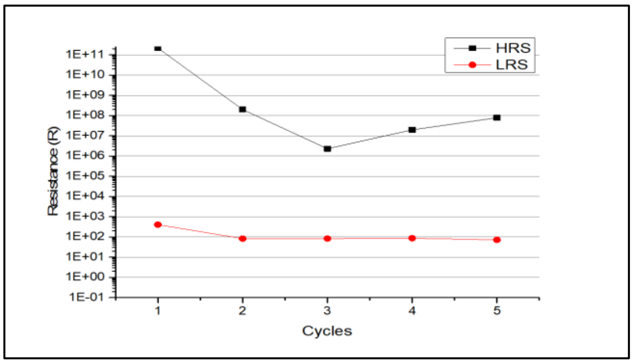


Figure 6.8: The HRS and LRS vs the switching cycles of the metal electrode RRAM device with ZrO_2/Al_2O_3 bi-layer as the resistive switching layer. The metal electrode RRAM device shows good stability for the LRS and a slight fluctuation for the HRS.

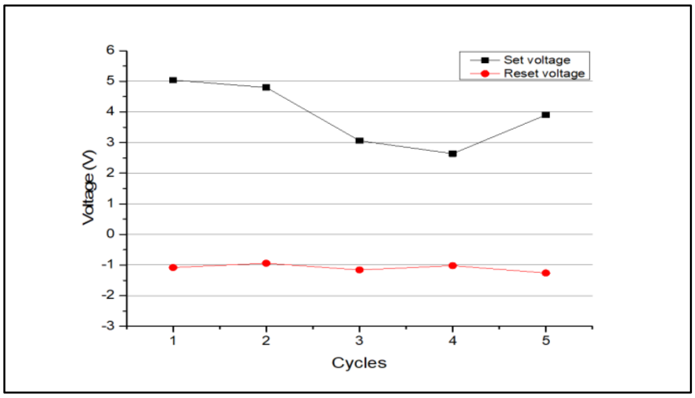


Figure 6.9: The operating voltage vs the switching cycles of the metal electrode RRAM device with ZrO_2/Al_2O_3 bi-layer as the resistive switching layer. The metal electrode RRAM device shows a slight fluctuation for set voltage and relative stable for the reset voltages.

Comparing these three bi-layer metal oxide RRAM from figure 6.1 to figure 6.9, metal electrode RRAM device with ZrO_2/HfO_2 bi-layer shows the best stability for the set and reset voltage as well as HRS and LRS.

6.2 Bi-layer resistive switching RRAM with metal-CNT electrodes

Figure 6.10(a) shows the schematic drawing of the top view and cross-section view of the memory device. The aligned SWCNTs were grown by thermal chemical vapor deposition (TCVD) on quartz substrate at 925 ºC with patterned ferritin as catalyst precursor. Figure 6.10(b) shows the aligned SWCNTs network grown using TCVD method. Figure 6.10(c) shows the aligned CNTs electrode after etched away unwanted CNTs. Figure 6.10(d) shows the optical image of the final device. Figure 6.11 shows the device fabrication process for the RRAM device with bi-layer resistive switching using aligned SWCNTs as the bottom electrodes. The device fabrication starts with patterning the bottom contact pads connecting to the aligned SWCNTs. The contact pads with 10nm Ti and 30nm Au film were fabricated on the aligned SWCNTs using standard photolithography and lift-off method as shown in figure 6.10(c). The aligned SWCNTs outside the channel area were removed through photolithography and oxygen plasma etching process. Then the bi-layer metal oxides of 2.5 nm HfO_2 and 2.5 nm Al_2O_3 were deposited using ALD system to the entire devices. The bi-layer metal oxides served as the resistive switching materials. The top electrode (10 nm Ti and 30nm Au) was then deposited using standard photolithography and lift-off process.

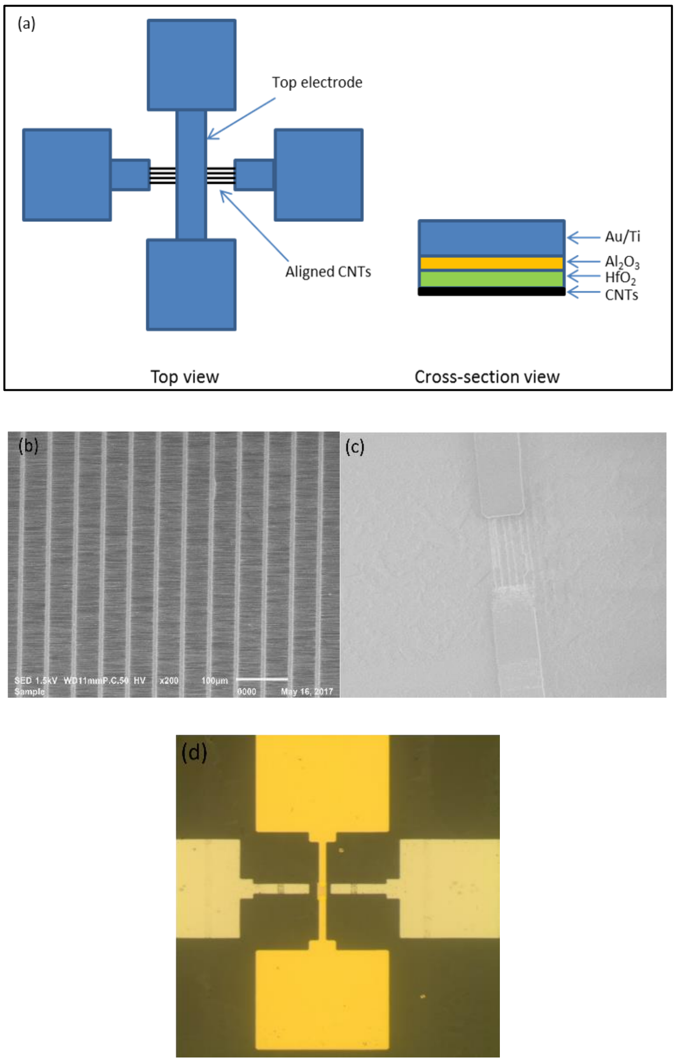


Fig. 6.10: (a) Schematic drawing of our memory device. (b) SEM image of the grown aligned SWCNTs network using TCVD. (c) SEM image of the bottom aligned SWCNT electrode. (d) Optical image of the final memory device.

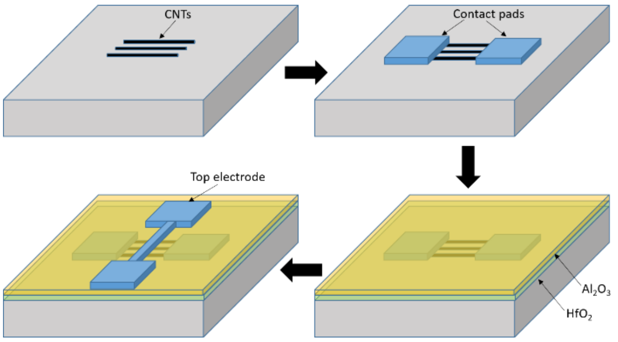


Figure 6.11: Fabrication process for the bi-layer resistive switching memory using aligned SWCNTs as electrodes.

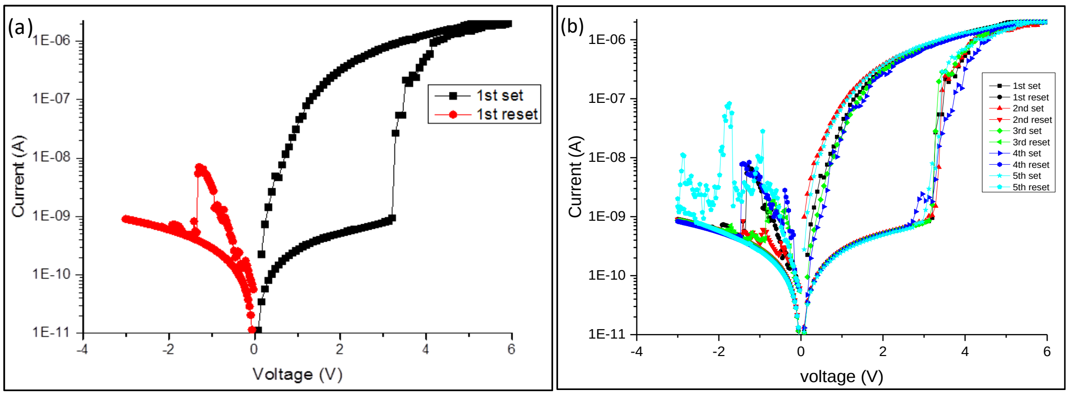


Figure 6.12: The I-V characteristic of the RRAM device with bi-layer resistive switching layer using aligned CNTs as bottom electrode. (a) The 1st set and reset cycle and (b) the first five set and reset cycles of the same device. (Our results published in IEEE 12th NMDC)

Figure 6.12(a) shows the first cycle I-V characteristics of the RRAM device with bi-layer resistive switching layer using aligned CNTs as bottom electrode with a bipolar switching behavior. The compliance current is set at 2 µA to prevent the device from breakdown. The four-contact pad configuration allows us to measure the I-V characteristic of the bottom aligned CNTs separately. The bottom aligned CNTs electrode was measured at around ~15MΩ. Initially the device was in the HRS measured at ~15GΩ. When the positive sweeping voltage reached the set value at +4V, a conductive path was formed across the oxide layers through oxygen vacancies. This conductive path offered a low resistance of ~15 MΩ, the LRS. To reset the device back to the HRS, a negative voltage was applied to the two electrodes. When the negative sweeping voltage reached -1.3V, the conduction path was annihilated and hence, the device was reset and returned back to the HRS. Figure 6.12(b) shows the first 5 cycles of the same device. One can see that the set and reset voltage had a very small variation.

Within the measurement time of 1x10^4s, good retention was demonstrated for the same device, as shown in figure 6.13(a). The device could maintain the HRS and LRS without any degradation. The device was successfully performed for 50 cycles with an average on/off ratio ~ 1x10^2, as shown in figure 6.13(b).

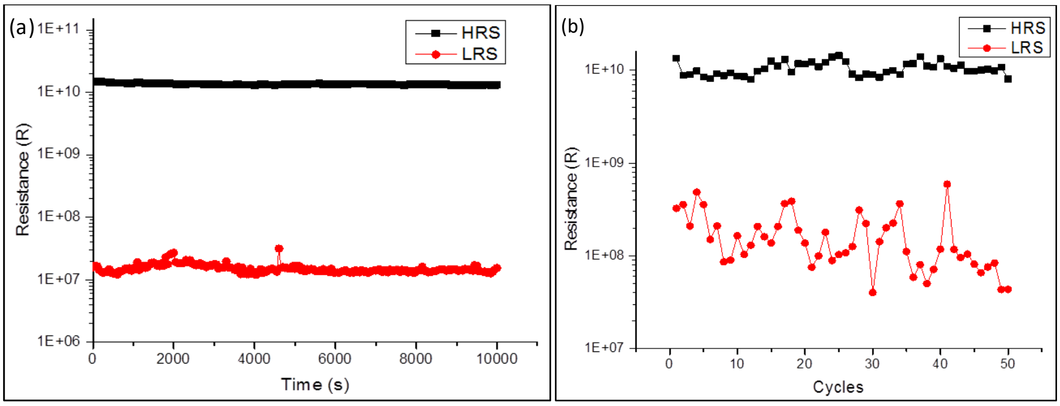


Figure 6.13: (a) Retention performance and (b) cycles performance of the RRAM device with bi-layer resistive switching layer using aligned CNTs as bottom electrode. (Our results published in IEEE 12th NMDC)

Figure 6.14(a) shows the cycle's performance of the same device from 1st to 20th cycles. The set and reset voltage were relatively stable from the cycle to cycle performance. Fig6.14(b) shows the device to device variation for set and reset voltages. The set voltage and reset voltage had very small variations of less than one volt at around 4~5V and 1~2V, respectively. These could be attributed to the bi-layer metal oxides resistive switching layer. For a single layer metal oxide resistive switching memory, the conductive path is typically formed at the interface between the metal and oxide film. This is one of the factors that affecting the variation of the set and reset voltage from the device to device and also from the cycle to cycle of the same device [5, 11]. By using two metal oxide layers, the interface of the conduction path may have shifted to the interface between two different oxide layers [5, 11]. Figure 6.15 illustrates that when voltage applied across the two electrodes, oxygen vacancies could accumulate at a specific location and a conduction path could formed at the interface between the two metal oxide layers. The oxygen vacancies inside the two metal oxide layers could help to create a conduction path across them. This reduces the variation of the conduction path forming process.

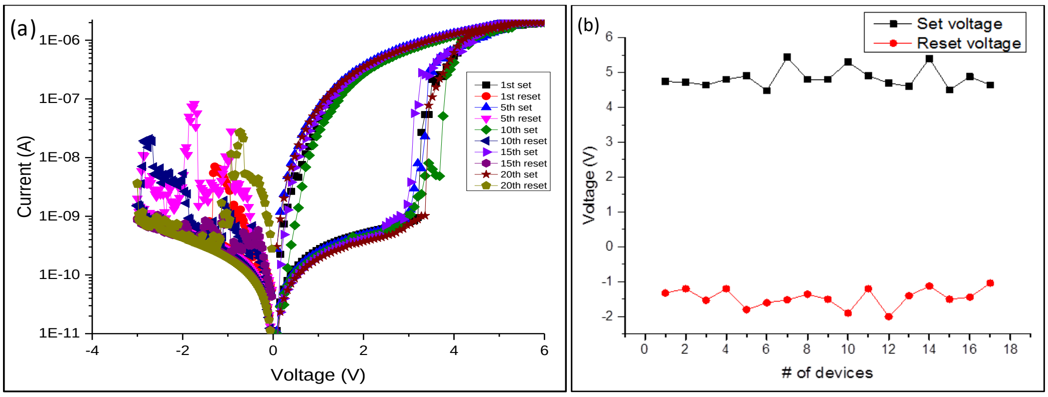


Figure 6.14: (a) 1st to 20th cycles of the SWCNTs memory device. (b) Device to device variation for the set and reset voltages. (Our results published in IEEE 12th NMDC)

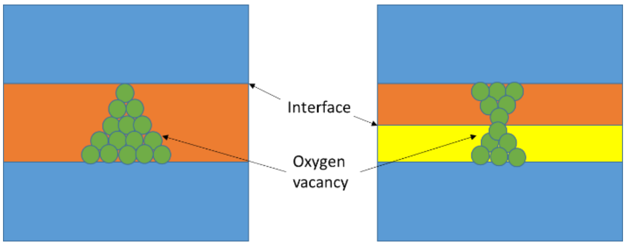


Figure 6.15: Illustration of oxygen vacancies create a conduction path at the interface between the metal and oxide layers for a single metal oxide layer and between the oxide and oxide for a bi-layer metal oxide. (Our results published in IEEE 12th

NMDC)

Compared with our another RRAM device in which aligned CNTs were utilized as the bottom electrode with a single metal oxide layer, the RRAM device with the bi-layer resistive switching layer showed several advantages. The RRAM device with a single metal oxide layer required a forming process to initiate the device and the reset current was as high as ~1uA. In contrast, the RRAM device with the bi-layer resistive switching material did not require a higher initial voltage to form the conduction path. The device also required a very low reset current down to 10nA to reset the device. Furthermore, the device showed significant less variation from cycle to cycle as well as from device to device for the set and reset voltage.

6.3 Bi-layer resistive switching RRAM with CNT-CNT electrodes

In this work, RRAM devices with bi-layer resistive switching layer using aligned as both top electrode and bottom electrode were fabricated and characterized. A bi-layer of 2.5nm ALD HfO_2/2.5nm Al_2O_3 was introduced in between the two CNTs electrodes. Figures 6.16 and Figure 6.18 show the I-V characteristics of the CNT-CNT electrode RRAM device with the bi-layer.

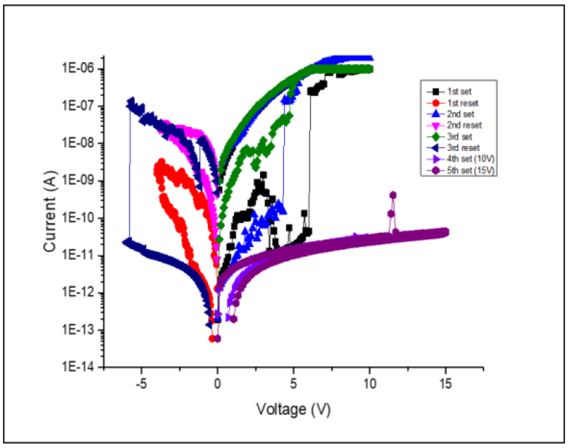


Figure 6.16: The I-V characteristic of the CNT-CNT electrode RRAM device with

the HfO_2/Al_2O_3 bi-layer (device#1).

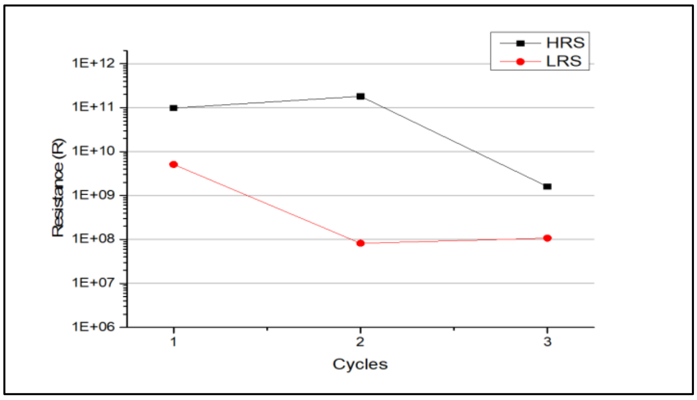


Figure 6.17: The HRS and LRS vs the switching cycles for the CNT-CNT electrode RRAM device#1.

Figure 6.16 shows one of the CNT-CNT electrode RRAM devices using the bi-layer of HfO_2/Al_2O_3 as the resistive switching material. The initial resistance was roughly few GΩ. The device changed to the LRS with a resistance of few MΩ at roughly +6V. The device on/off ratio was about one order. The device was then reset to the HRS at around -4V. The second set and reset voltages occurred at +5V and -4V, respectively and the on/off ratio was ~1 x 10^3. The third cycle occurred at +5V and -5.2V, respectively. The on/off ratio was about one order. Unfortunately, after the third cycles, the device was unable to set to the LRS again. Figure 6.17 shows the HRS and LRS vs the switching cycles for the CNT-CNT electrode RRAM device#1.

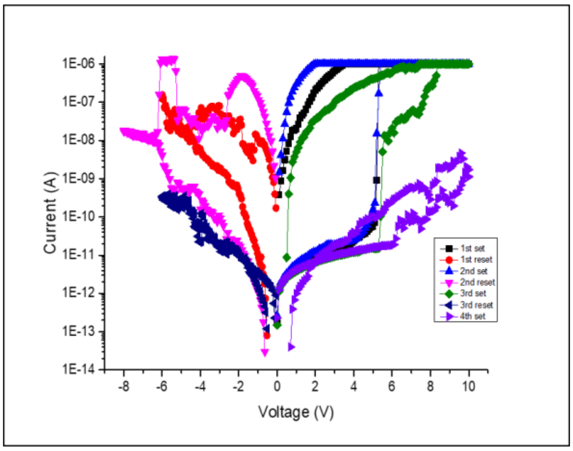


Figure 6.18: The I-V characteristic of the CNT-CNT electrode RRAM device with the HfO_2/Al_2O_3 bi-layer (device#2).

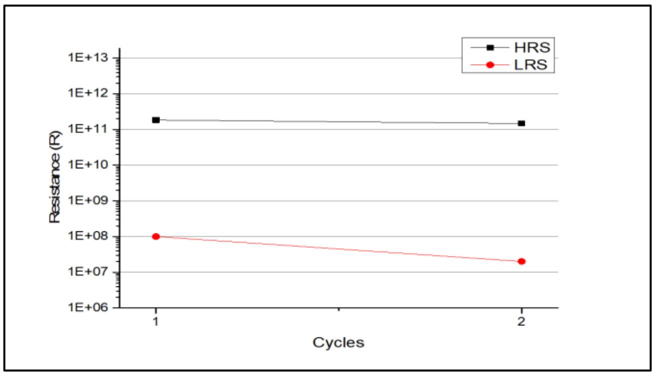


Figure 6.19: The HRS and LRS vs the switching cycles for the CNT-CNT electrode RRAM device#2.

Figure 6.18 shows another device of CNT-CNT electrode RRAM using the bi-layer of HfO_2/Al_2O_3 as the resistive switching material. The initial resistance was roughly few GΩ. The device could be set to LRS with a resistance of few MΩ at roughly +5V. The device on/off ratio was about $2x10^3$. The device was then reset to the HRS at around -4V. The second set and reset voltages occurred at +5V and -5V, respectively and the on/off ratio was ~5×10^3. Unfortunately, after the second cycles, the device was unable to set to LRS again. Figure 6.19 shows the HRS and LRS vs the switching cycles for the CNT-CNT electrode RRAM device#2.

Although CNT-CNT electrode RRAM devices were able to perform the memory function, the devices were only able to perform a few cycles. As the devices remained at the HRS, it is unlikely that the devices were breakdown and burned off due to excessive current. If breakdown occurred, the RRAM device will be stayed in the LRS instead of the HRS because the two electrodes had short circuited. Hence, it can be concluded that the devices unable to function as a memory again were not due to breakdown. The possible cause could be the device could not form a stable conductive path in between the two CNT electrodes due to the conductive path formed was too narrow and the distance between the two electrodes are much greater compared with the active area which was less than 2nm (SWCNT's diameter in the range of 1nm-2nm).

Bi-layer Device	Oxide layer	Thickness	Set voltage	Reset voltage
Metal electrode	HfO_2/Al_2O_3	5nm	~ +2v	~ -2v
	ZrO_2/HfO_2	5nm	~ +1.5V	~ -1V
	ZrO_2/Al_2O_3	5nm	~ +3V	~ -1V
Metal-CNT	HfO_2/Al_2O_3	5nm	~ +4.5V	~ -1.3V
CNT-CNT	HfO_2/Al_2O_3	5nm	~ +5V	~ -5V

Table 6.1: Comparison of the set and reset voltages for the metal, metal-CNT and CNT-CNT electrode RRAM devices with bi-layer oxide as the resistive switching layer.

Table 6.1 shows the comparison of the set and reset voltages for the metal, metal-CNT and CNT-CNT electrode RRAM devices with bi-layer oxide as the resistive switching layer.

Chapter 7 Conclusions

7.1 Conclusion

In the first part of the thesis, the study of metal electrodes RRAM was focused. Al_2O_3 oxide layer was used as the resistive switching material. The Al_2O_3 oxide layers were deposited either by ALD or e-beam evaporation. The RRAM devices with the ALD Al_2O_3 layer were able to perform a few tens of cycles but the RRAM devices with e-beam evaporated Al_2O_3 layer only lasted for a few cycles. ALD Al_2O_3 oxide layer showed much better quality than the e-beam evaporated Al_2O_3 oxide layer. In addition, other oxide layers were also used as resistive switching layer, these include HfO_2 and ZrO_2 oxide layers. By studying the influences of the resistive switching layers and their thickness on the memory performance, we find that the metal electrode RRAM with Al_2O_3 oxide layer showed the most stable set and reset voltage across all the three different oxide thickness. The metal electrode RRAM with HfO_2 oxide layer had very stable set and reset voltage for the 3nm thickness devices but a slight fluctuation for the 5nm and 10nm thickness devices. The set and reset voltage for the metal electrode RRAM with ZrO_2 oxide layer showed fluctuation across all the three different oxide thickness. Three different bi-layer metal oxide combination, HfO_2/Al_2O_3, ZrO_2/HfO_2 and ZrO_2/Al_2O_3 bi-layers were also engaged into the RRAM devices. From the I-V characteristics, ZrO_2/HfO_2 bi-layer had shown a significant improvement in the stability of operating voltage. The set and reset voltages were very stable with a very small fluctuation.

For the second part, random network CNTs and aligned CNTs were used as electrodes for RRAM devices. Random network CNTs electrode RRAM devices were able to perform the set and reset operations. However, the devices were only able to last for

2-3 cycles. The operating voltage was found to be gradually increased with the number of cycles. The increasing reset voltages and poor performance of switching cycle were possibly due to poor uniformity of CNTs and contact between CNT electrode and Al_2O_3. Next, aligned CNTs were also used as the electrodes for RRAM devices in which the bottom electrode was aligned CNTs while the top electrode was metal. The devices were able to perform better than the random network CNTs electrode RRAM devices. The devices showed distinct abrupt change in the resistance during switching from the HRS to the LRS and vice versa as compared with the gradual change of the resistance in the random network CNTs electrode RRAM devices. However, the devices were only able to perform a few switching cycles. Aligned CNTs electrode was used as the bottom and top electrode for the CNT-CNT electrode RRAM devices. The devices showed abrupt change in the resistance during the switching as well. Although the cycle performance was better than the metal-CNT electrode RRAM devices, the devices were still unable to perform for a high switching cycle number.

In the third part of the thesis, the first reported CNTs electrode RRAM devices using bi-layer as resistive switching layers were studied. The device exhibited several advantages, such as forming-free process, a high on/off ratio at 1×10^3 and a low reset current down to 10nA. Furthermore, the devices showed stable memory performance from the cycle to cycle as well as from the device to device. These improvements may be attributed to the bi-layer metal oxides resistive switching layer. For a single layer metal oxide RRAM device, the conductive path is typically formed at the interface between the metal electrode and oxide layer. By using bi-layers structure, the interface of the conduction path may have shifted to the interface between two different oxide layers.

7.2 Future work

In this thesis, CNTs electrode RRAM devices showed their potentials and advantages as non-volatile memory. The CNT RRAM devices with bi-layer resistive switching oxides showed forming-free process, a high on/off ratio, low reset current and lesser variation in the set and reset voltages from cycle to cycle as well as from device to device. However, some issues still require more research attention. One is to improve the switching cycle performance. The devices were only able to perform few tens of switching cycles. For a stable memory device, its endurance should achieve at least 10^4 cycles. Future work may focus on improving the endurance of the devices to match conventional flash memories and even better. One of the possible solutions is to employ other bi-layer metal oxides as the resistive switching materials. ZrO_2/HfO_2 bi-layer has showed a very stable performance in the metal electrode RRAM. ZrO_2/HfO_2 bi-layer may also works well in in the CNTs electrode RRAM devices.

Ultimately, the final goal is to achieve high performance CNT-CNT electrode RRAM devices. By using both aligned CNT as the electrodes, the active area can be significantly reduced to less than 2nm x 2nm. This can definitely increase the packing density of the device. Although our CNT-CNT electrode RRAM devices showed some memory characteristics, the stability as well as endurance of the device need to be improved in order to be useful.

Finally, more attention should be focused on the switching mechanism in the CNTs electrode RRAM devices. The resistive switching mechanism may be closely related or similar to the oxygen vacancy mechanism. A systematic experiment should be carried out to figure out the mechanism. With a better understanding of the switching mechanism and the charges transfer process between CNTs electrode and resistive switching layer, we could achieve a high performance and endurance CNTs electrode RRAM device.

Author’s Publication

Conference paper

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Bibliography

1. (n.d.). Retrieved from Microcontrollerslab: https://microcontrollerslab.com/difference-of-sram-and-dram/
2. (n.d.). Retrieved from University of Minnesota: http://license.umn.edu/technologies/z09007_lower-switching-current-for-spin-torque-transfer-in-magnetic-storage-devices-such-as-magnetoresistive-random-access-memory-mram
3. (n.d.). Retrieved from Wikipedia: https://en.wikipedia.org/wiki/Nano-RAM
4. A. J. Oberlin, M. E. (1976). Filamentous Growth of Carbon through Benzene Decomposition. *Journal of Crystal Growth*.
5. Akbari, M. (2017). Reproducible and reliable resistive switching behaviors of AlOX/HfOX bilayer structures with Al electrode by atomic layer deposition†. *RSC advances*.
6. Amit Prakash, D. J. (2013). TaOx-based resistive switching memories: prospective and challenges. *Nanoscale research letters*.
7. Anantram, M. P. (2006). Physics of carbon nanotube electronic devices. *Reports on Progress in Physics*.
8. Azzaz, M. (2015). Benefit of Al2O3/HfO2 bilayer for BEOL RRAM integration through 16kb memory cut characterization. *IEEE*.
9. Azzaz, M. (2016). Endurance/retention trade off in HfOx and TaOx based RRAM. *IEEE*.
10. Bai, Y. (2015). Stacked 3D RRAM Array with Graphene/CNT as Edge Electrodes. *Scientific Reports*.
11. BARCI, M. (2016). Bilayer Metal-Oxide Conductive Bridge Memory Technology for Improved Window Margin and Reliability. *journal of the electron devices society*.
12. Basnet, P. (2020). Substrate dependent resistive switching in amorphous-HfOx memristors: an experimental and computational investigation. *Journal of materials chemistry c*.
13. Behnam, A. (2015). Nanoscale phase change memory with graphene ribbon electrodes. *Applied Physics Letters*.
14. Bersuker, G. (2010). Metal Oxide RRAM Switching Mechanism Based on Conductive Filament Microscopic Properties. *IEEE*.
15. Bhattacharjee, S. (2020). Insights into Multilevel Resistive Switching in Monolayer MoS2. *ACS applied materials and interfaces*.
16. Borgert, M. (2014). Influence of Carbon Nanotubes on Epoxy Resin Cure Reaction Using Different Techniques: A Comprehensive Review. *Polymer Engineering and Science*.

17. Bowers, N. (2014). Retrieved from electronicspecifier: https://www.electronicspecifier.com/news/analysis/patent-analysis-for-non-volatile-memories
18. Brunel, D. (2013). Integrating Multiple Resistive Memory Devices on a Single Carbon Nanotube. *Advanced Functional Materials*.
19. Chai, Y. (2011). Nanoscale Bipolar and Complementary Resistive Switching Memory Based on Amorphous Carbon. *IEEE TRANSACTIONS ON ELECTRON DEVICES*.
20. Chand, U. (2015). Mechanism of Nonlinear Switching in HfO2-Based Crossbar RRAM With Inserting Large Bandgap Tunneling Barrier Layer. *IEEE TRANSACTIONS ON ELECTRON DEVICES*.
21. Chang, W.-Y. (2010). Resistive switching behaviors of ZnO nanorod layers. *Appl. Phys. Lett.*
22. Chen, B. (2016). Highly Uniform Carbon Nanotube Field-Effect Transistors and Medium Scale Integrated Circuits. *Nano letters*.
23. Chen, M. (n.d.). Abnormal Multiple Charge Memory States in Exfoliated Few-Layer WSe2 Transistors. *ACS nano 2017*.
24. Chen, Y. (2020). Electroforming-Free, Flexible, and Reliable Resistive Random-Access Memory Based on an Ultrathin TaOx Film. *ACS Applied materials and interfaces*.
25. Choi, W. B. (2003). Carbon-nanotube-based nonvolatile memory with oxide–nitride–oxide film and nanoscale channel. *Applied Physics Letters*.
26. Ciocchini, N. (2016). Bipolar switching in chalcogenide phase change memory. *Scientific reports*.
27. D. J. J. Loy, P. A. (2018). Conduction Mechanisms on High Retention Annealed MgO-based Resistive Switching Memory Devices. *Scientific Reports*.
28. D. S. BETHUNE, C. H. (1993). Cobalt-catalysed growth of carbon nanotubes with single-atomic-layer walls. *Nature*.
29. D.C. Gilmer, T. R. (2017). NRAM Status and Prospects. *IEEE International Conference on IC Design and Technology*.
30. Dhahi, T. S. (2011). Fabrication of Lateral Polysilicon Gap of Less than 50nm Using Conventional Lithography. *Journal of Nanomaterials*.
31. Dias, n. (2017). Bipolar resistive switching in Si/Ag nanostructures . *Applied Surface Science*.
32. Ding, L. (2008). Growth of High-Density Parallel Arrays of Long Single-Walled Carbon Nanotubes on Quartz Substrates. *American Chemical Society*.
33. Dr. Joe Katz, D. A. (n.d.). Retrieved from Stanford nanoheat: https://nanoheat.stanford.edu/projects/phase-change-memory-and-electrothermal-transport-chalcogenides
34. Du, C. (2015). Biorealistic Implementation of Synaptic Functions with Oxide Memristors through Internal Ionic Dynamics. *Advanced functional materials*.

35. Fu, W. (2009). Intrinsic Memory Function of Carbon Nanotube-based Ferroelectric Field-Effect Transistor. *NANO letters*.
36. Gao, L. (2017). Enhanced resistive switching characteristics in Al2O3 memory devices by embedded Ag nanoparticles. *Nanotechnology*.
37. Ge, R. (2018). Atomristor: Nonvolatile Resistance Switching in Atomic Sheets of Transition Metal Dichalcogenides. *Nano letters*.
38. Geier, M. L. (2015). Solution-processed carbon nanotube thin-film complementary static random access memory. *NATURE NANOTECHNOLOGY*.
39. Goux, L. (2014). On the bipolar resistive-switching characteristics of Al2O3- and HfO2-based memory cells operated in the soft-breakdown regime. *Journal of Applied Physics*.
40. Guerra, L. M. (2017). Unipolar Nonvolatile Resistive Switching in Pt/MgO/Ta/Ru Structures Deposited by Magnetron Sputtering. *Journal of Nanoscience and Nanotechnology*.
41. Guo, A. (2007). Two-bit memory devices based on single-wall carbon nanotubes: demonstration and mechanism. *Nanotechnology*.
42. Han, S.-T. (2016). Hybrid Flexible Resistive Random Access Memory-Gated Transistor for Novel Nonvolatile Data Storage. *Flexible Electronics*.
43. Hanelt, S. (2011). Differentiation and quantification of surface acidities on MWCNTs by indirect potentiometric titration. *Carbon*.
44. Hayat, H. (2017). Can conventional phase-change memory devices be scaled down to single-nanometre dimensions? *Nanotechnology*.
45. He, C. (2012). Multilevel Resistive Switching in Planar Graphene/SiO2 Nanogap Structures. *ACS Nano*.
46. Hossain, N. M. (2014). Multilayer Graphene Nanoribbon Floating Gate Transistor for Flash Memory. *2014 IEEE International Symposium on Circuits and Systems (ISCAS)* (pp. 806 - 809). Melbourne VIC: IEEE.
47. Hu, C. (2017). The effect of oxygen vacancy on switching mechanism of ZnO resistive switching memory. *Appl. Phys. Lett.*
48. Huang, C.-H. (2017). Resistive switching of Sn-doped In2O3/HfO2 core–shell nanowire: geometry architecture engineering for nonvolatile memory†. *Nanoscale*.
49. Huang, J.-W. (2013). The effect of high/low permittivity in bilayer HfO2/BN resistance random access memory. *Appl. Phys. Lett.*
50. Huang, X.-D. (2020). Forming-Free, Fast, Uniform, and High Endurance Resistive Switching From Cryogenic to High Temperatures in W/AlOx/Al2O3/Pt Bilayer Memristor. *IEEE ELECTRON DEVICE LETTERS*.
51. Huber, B. (2017). Fully inkjet printed flexible resistive memory. *Appl. Phys. Lett.*
52. Hwang, S. K. (2012). Flexible Multilevel Resistive Memory with Controlled Charge Trap B- and N-Doped Carbon Nanotubes. *NANO letters*.

53. Ibrahim, I. (n.d.). CVD-Grown Horizontally Aligned Single-Walled Carbon Nanotubes: Synthesis Routes and Growth Mechanisms. *Micro and Nano: No Small Matter. Science*.
54. Ielmini, D. (2011). Modeling the Universal Set/Reset Characteristics of Bipolar RRAM by Field- and Temperature-Driven filament growth. *IEEE TRANSACTIONS ON ELECTRON DEVICES*.
55. IIJIMA, S. (1993). Single-shell carbon nanotubes of 1-nm diameter. *Nature*.
56. Ismail, M. (2020). Stabilized and RESET-voltage controlled multi-level switching characteristics in ZrO2-based memristors by inserting a-ZTO interface layer. *Journal of Alloys and Compounds*.
57. Jagan Singh Meena, S. M.-Y. (2014). Overview of emerging nonvolatile memory technologies. *Nanoscale research letters*.
58. Jin, Z. (2017). Graphdiyne for multilevel flexible organic resistive random access memory devices. *MATERIALS CHEMISTRY FRONTIERS*.
59. Jo, S. H. (2010). Nanoscale Memristor Device as Synapse in. *Nano letters*.
60. Khiat, A. (2016). High Density Crossbar Arrays with Sub- 15 nm Single Cells via Liftoff Process Only. *scientific reports*.
61. Kianian, S. (2010). A 3D Stackable Carbon Nanotube-based Nonvolatile Memory (NRAM). *2010 Proceedings of the European Solid State Device Research Conference* (pp. 404 - 407). Sevilla: IEEE.
62. Kim, C. H. (2015). SrTiO3-Based Resistive Switching Memory Device with Graphene Nanoribbon. *The American Ceramic Society*.
63. Kim, S. (2015). Experimental Demonstration of a Second-Order Memristor and Its Ability to Biorealistically Implement Synaptic Plasticity. *Nano letters*.
64. Kim, S. (2017). Nano-cone resistive memory for ultralow power operation. *nanotechnology*.
65. Kim, S. (2017). Pattern Recognition Using Carbon Nanotube Synaptic Transistors with an Adjustable Weight Update Protocol. *ACS nano*.
66. Kim, W.-H. (2014). Nanoscale resistive switching memory device composed of NiO nanodot and graphene nanoribbon nanogap electrodes. *Carbon*.
67. Kocabas, C. (2007). Improved Synthesis of Aligned Arrays of Single-Walled Carbon Nanotubes and Their Implementation in Thin Film Type Transistors. *J. Phys. Chem.* .
68. Kong, B.-S. (2007). Single-Walled Carbon Nanotube Gold Nanohybrids: Application in Highly Effective Transparent and Conductive Films. *Journal of Physical Chemistry C*.
69. Kumar, S. (2017). Oxygen migration during resistance switching and failure of hafnium oxide memristors. *Appl. Phys. Lett.* .
70. Lanza, M. (2019). Recommended Methods to Study Resistive Switching Devices. *advanced electronic materials*.
71. Lee, B.-H. (2016). Foldable and Disposable Memory on Paper. *scientific reports*.

72. Li, G. (2015). Demonstration of nonvolatile multilevel memory in ambipolar carbon nanotube thin-film transistors. *Applied Physics Express 8*.
73. Li, L. (2014). Facile Synthesis of MnO2/CNTs Composite for Supercapacitor Electrodes with Long Cycle Stability. *J. Phys. Chem. C*.
74. Li, L. (2016). Memory behavior of multi-bit resistive switching based on multiwalled carbon nanotubes. *Organic Electronics*.
75. Li, R. (2015). Towards formation of fibrous woven memory devices from all-carbon electronic fibers. *Physical Chemistry Chemical Physics*.
76. Li, X. (2017). Quantifying Single-Carbon Nanotube−Electrode Contact via the Nanoimpact Method. *The journal of physical chemistry letters*.
77. Liang, J. (2011). A 1.4μA Reset Current Phase Change Memory Cell with Integrated Carbon Nanotube Electrodes for Cross-Point Memory Application. *VLSI Technology (VLSIT), 2011* (pp. 100 - 101). Honolulu, HI: IEEE.
78. Liang, J. (2012). An Ultra-Low Reset Current Cross-Point Phase Change Memory With Carbon Nanotube Electrodes. *IEEE TRANSACTIONS ON ELECTRON DEVICES*.
79. Liao, A. (2010). Thermal dissipation and variability in electrical breakdown of carbon nanotube devices. *The American Physical Society*.
80. Liao, A. D. (2014). Carbon nanotube network-silicon oxide non-volatile switches. *nature communications*.
81. Liu, C. (2017). Atomic crystals resistive switching memory. *Chin. Phys. B*.
82. Liu, W. (2019). Growth of high-density horizontal SWNT arrays using multi-cycle in-situ loading catalysts. *Carbon*.
83. Lugli, P. (2016). Fabrication, characterization and modeling of flexible electronic components based on CNT. *IEEE*.
84. Ma, G. (2016). Ultra-high ON/OFF ratio and multi-storage on NiO resistive switching device. *J Mater Sci*.
85. Mahata, C. (2020). Resistive switching and synaptic behaviors of an HfO2/Al2O3 stack on ITO for neuromorphic systems. *Journal of Alloys and Compounds*.
86. Makarov, A. (n.d.). Retrieved from https://www.iue.tuwien.ac.at/phd/makarov/dissertationch3.html
87. McEuen, P. L. (2000). Single-wall carbon nanotubes. *Physics World*.
88. Mehta, J. (n.d.). *SlideShare*. Retrieved from SlideShare: http://www.slideshare.net/SagarPatel55/carbon-nanotube-33801296
89. Mikhaylov, A. (2020). Multilayer Metal-Oxide Memristive Device with Stabilized. *Advanced materials technologies*.
90. Mildred S. Dresselhaus, G. D. (2001). *Carbon Nanotubes: Synthesis, Structure, Properties, and Applications.* Berlin: London: Springer.
91. Mintmire, C. T. (2005). Fundamental Properties of Single-Wall Carbon Nanotubes. *The Journal of Physical Chemistry B*.

92. Naitoh, Y. (2006). Resistance switch employing a simple metal nanogap junction. *Nanotechnology*.
93. Ning, S. (2015). Investigation and Improvement of Verify-Program in Carbon Nanotube-Based Nonvolatile Memory. *IEEE TRANSACTIONS ON ELECTRON DEVICES*.
94. Nukala, P. (2015). Ultralow-power switching via defect engineering in germanium telluride phase-change memory devices. *Nature communications*.
95. Olin-Ammentorp, W. (2015). Resistive Transition Metal Oxide Memory. *MICROELECTRONIC ENGINEERING*.
96. Olmedo, M. (2011). Carbon Nanotube Memory by the Self-Assembly of Silicon Nanocrystals as Charge Storage Nodes. *ACS Nano*.
97. Pan, C. (2017). Coexistence of Grain-Boundaries-Assisted Bipolar and Threshold Resistive Switching in Multilayer Hexagonal Boron Nitride. *Advanced functional materials*.
98. Park, J. (2011). Improved Switching Uniformity and Speed in Filament-Type RRAM Using Lightning Rod Effect. *IEEE ELECTRON DEVICE LETTERS*.
99. Puglisi, F. M. (2016). 2D h-BN based RRAM devices. *IEEE*.
100. Qian, K. (2016). Direct Observation of Conducting Filaments in Tungsten Oxide Based Transparent Resistive Switching Memory. *ACS applied materials and interfaces*.
101. Qian, K. (2016). Novel concepts in functional resistive switching memories. *Journal of Materials Chemistry C*.
102. Qian, K. (2017). Direct Observation of Indium Conductive Filaments in Transparent, Flexible, and Transferable Resistive Switching Memory. *ACS Nano*.
103. Qiao, Q. (2016). Detection of resistive switching behavior based on the Al2O3/ZnO/Al2O3 structure with alumina buffers. *Thin Solid Films*.
104. Radosavljević, M. (2003). Electrical properties and transport in boron nitride nanotubes. *Appl. Phys. Lett.*
105. Ranjan, A. (2016). Analysis of quantumconductance, read disturb and switching statistics in HfO2 RRAM using conductive AFM. *Microelectronics Reliability*.
106. Rinkio, M. (2008). High-Speed Memory from Carbon Nanotube Field-Effect Transistors with High-K Gate Dielectric. *NANO letters*.
107. Rosendale, G. (2010). A 4 Megabit Carbon Nanotube-based Nonvolatile Memory (NRAM). *ESSCIRC, 2010* (pp. 478 - 481). Seville: IEEE.
108. Rouse, M. (2018, April). Retrieved from SearchStorage: https://searchstorage.techtarget.com/definition/floating-gate
109. Rueckes, T. (2000). Carbon Nanotube Based Nonvolatile Random Access Memory for Molecular Computing. *SCIENCE*.

110. Russo, P. (2017). Carbon nanowalls: A new material for resistive switching memory devices. *Carbon*.

111. S. Wang, X. L.-M. (2005). Field-Effect Characteristics and Screening in Double-Walled Carbon Nanotube Field-Effect Transistors. *The Journal of Physical Chemistry Letters B*.

112. S.Alshammari, A. l. (2017). Inkjet printing of polymer functionalized CNT gas sensor with enhanced sensing properties. *Materials Letters*.

113. Sassine, G. (2019). Hybrid-RRAM toward Next Generation of Nonvolatile Memory: Coupling of Oxygen Vacancies and Metal Ions. *Advanced electronic materials*.

114. Semple, J. (2017). Semiconductor-Free Nonvolatile Resistive Switching Memory Devices Based on Metal Nanogaps Fabricated on Flexible Substrates via Adhesion Lithography. *IEEE TRANSACTIONS ON ELECTRON DEVICES*.

115. Shan, F. (2020). Enhanced Electrical Performance of Structurally Engineered Memristor Devices with Multi-Stacked Indium Zinc Oxide Films. *PSS-a*.

116. Siddiqui, G. U. (2017). A two-dimensional hexagonal boron nitride/ polymer nanocomposite for flexible resistive switching devices. *Journal of Materials Chemistry C*.

117. Son, D. (2015). Stretchable Carbon Nanotube Charge-Trap Floating-Gate Memory and Logic Devices for Wearable Electronics. *ACS Nano*.

118. Son, J. Y. (2008). Direct observation of conducting filaments on resistive switching of NiO thin films. *Appl. Phys. Lett.*

119. Sun, Y. (2016). Multilevel resistive switching and nonvolatile memory effects in epoxy methacrylate resin and carbon nanotube composite films. *Organic Electronics*.

120. Tan, C. (2015). Non-volatile resistive memory devices based on solution-processed ultrathin two-dimensional nanomaterials. *Chem Soc Rev*.

121. Tang, L. (2020). Resistive switching in atomic layer deposited HfO2/ZrO2 nanolayer stacks. *Applied Surface Science*.

122. Tsai, C.-L. (2013). Resistive Random Access Memory Enabled by Carbon Nanotube Crossbar Electrodes. *ACS Nano*.

123. Tsuruoka, T. (2016). Operating mechanism and resistive switching characteristics of two- and three-terminal atomic switches using a thin metal oxide layer. *J Electroceram*.

124. Tyson, M. (2013, August). Retrieved from Hexus: https://hexus.net/tech/news/storage/58577-resistive-ram-provides-1tb-chip-smaller-stamp/

125. Utkarsh Kumar, S. S. (2016). Carbon Nanotube: Synthesis and Application in Solar Cell. . *Journal of Inorganic and Organometallic Polymers and Materials*.

126. Vasu, K. (2011). Nonvolatile unipolar resistive switching in ultrathin films of graphene and carbon nanotubes. *Solid State Communications*.

127. Vescio, G. (2016). Inkjet Printed HfO2-based ReRAMs: first demonstration and performance characterization. *IEEE*.

128. Wang, H. (2016). Coexistence of bipolar and unipolar resistive switching characteristics of thin TiO2 film grown on Cu foil substrate for flexible nonvolatile memory device. *Journal of Alloys and Compounds*.

129. Wang, L.-G. (2015). Excellent resistive switching properties of atomic layer-deposited Al2O3/HfO2/Al2O3 trilayer structures for non-volatile memory applications. *Nanoscale research letters*.

130. Wang, X.-F. (2017). Graphene resistive random memory— the promising memory device in next generation. *Chin. Phys. B*.

131. Wu, L. (2020). Self-Compliance and High Performance Pt/HfOx/Ti RRAM Achieved through Annealing. *Nanomaterials*.

132. Wu, X. (2019). Thinnest Nonvolatile Memory Based on Monolayer h-BN. *Advanced materials*.

133. Wu, Y. (2011). Resistive Switching AlOx-Based Memory with CNT Electrode for Ultra-Low Switching Current and High Density Memory Application. *Symposium on VLSI Technology Digest of Technical Papers*.

134. Xiao, M. (2017). Reliable and Low-Power Multilevel Resistive Switching in TiO2 Nanorod Arrays Structured with a TiOx Seed Layer. *ACS applied materials and interfaces*.

135. Xiao, M. (2017). Resistive Switching Memory of TiO2 Nanowire Networks Grown on Ti Foil by a Single Hydrothermal Method. *Nano-Micro Lett.*

136. Xiong, F. (2010). Ultra-Low Power Phase Change Memory with Carbon Nanotube Interconnects. *Device Research Conference (DRC), 2010* (pp. 253 - 254). South Bend, IN: IEEE.

137. Xiong, F. (2011). Low-Power Switching of Phase-Change Materials with Carbon Nanotube Electrodes. *science*.

138. Xiong, F. (2012). Self-Aligned Nanotube−Nanowire Phase Change Memory. *Nano letters*.

139. Xiong, F. (2016). Towards Ultimate Scaling Limits of Phase-Change Memory. *IEEE*.

140. Xue, D. (2019). Flexible resistive switching device based on the TiO2 nanorod arrays for non-volatile memory application. *Journal of Alloys and Compounds*.

141. Xue, G. (2017). Water-evaporation-induced electricity with nanostructured carbon materials. *Nature nanotechnology*.

142. Yan, X. (2017). Bipolar transparent resistive switching based in a-IGZO/STO/a-IGZO structure for nonvolatile memory application. *AIP Conference Proceedings*.

143. Yao, J. (2009). Two-Terminal Nonvolatile Memories Based on Single-Walled Carbon Nanotubes. *ACS Nano*.

144. Yao, J. (2012). Highly transparent nonvolatile resistive memory devices from silicon oxide and graphene. *Nature communications*.

145. Yeom, S.-W. (2016). Transparent resistive switching memory using aluminum oxide on a flexible substrate. *Nanotechnology*.

146. Yin, L. (2020). Two-Dimensional Unipolar Memristors with Logic and Memory Functions. *Nano letters*.

147. YingTao, L. (2011). An overview of resistive random access memory devices. *Chinese Science Bulletin*.

148. Yu, M. (2016). Novel Vertical 3D Structure of TaOx based RRAM with Self-localized Switching Region by Sidewall Electrode Oxidation. *Scientific reports*.

149. Yu, S. (2011). An Electronic Synapse Device Based on Metal Oxide Resistive Switching Memory for Neuromorphic Computation. *IEEE TRANSACTIONS ON ELECTRON DEVICES*.

150. Yun, D. Y. (2015). Nonvolatile memory devices based on Au/graphene oxide nanocomposites with bilateral multilevel characteristics. *Carbon*.

151. Zahoor, F. (2020). Resistive Random Access Memory (RRAM): an Overview of Materials, Switching Mechanism, Performance, Multilevel Cell (mlc) Storage, Modeling, and Applications. *Nanoscale research letters*.

152. Zhang, E. (2015). Tunable Charge-Trap Memory Based on Few-Layer MoS2. *ACS nano*.

153. Zhang, L. (2017). Resistive switching mechanism in the one diode-one resistor memory based on p+-Si/n-ZnO heterostructure revealed by in-situ TEM. *scientific reports*.

154. Zhang, Q. (2012). *Carbon nanotubes and their applications*. Pan Stanford Publishing.

155. Zhang, S. (2017). Arrays of horizontal carbon nanotubes of controlled chirality grown using designed catalysts. *Nature*.

156. Zou, L. (2016). Uniform resistive switching properties of fully transparent TiO2-based memory devices. *Journal of Alloys and Compounds*.

157. Zou, Y. (2013). Fabrication of All-Carbon Nanotube Electronic Devices on Flexible Substrates Through CVD and Transfer Methods. *Advanced materials*.