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Energy-efficient Spread Second Capacitor Capacitive DAC for SAR ADC

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***Abstract*—An energy-efficient capacitive digital-to-analog converter (C-DAC) switching with spread second capacitor is proposed for low power successive approximation register analog-to-digital converters (SAR ADCs). In the proposed spread second capacitor capacitive digital-to-analog converter (SSC C-DAC), all capacitors except the most significant bit (MSB) capacitor are switched after the second bit decision. Because the burden of the second capacitor switching is shared with all capacitors except the MSB capacitor, the number of unit capacitors and the burden of driving V_{CM} are reduced. The proposed SSC C-DAC achieves 98.1% more efficient switching energy and can be comprised of the number of quarter unit capacitors, contrary to that in conventional schemes. The fabricated differential-type SAR ADC with SSC C-DAC has a 10-bit resolution and 10-MS/s sampling speed in 0.18-μm CMOS process. The test results show a SFDR of 60.9 dBc, a SINAD of 53.1 dB and an ENOB of 8.5 bit.**

***Index Terms*—Low power, energy efficient DAC, SAR ADC, capacitive DAC, switching energy**

I. INTRODUCTION

Successive approximation register analog-to-digital converters (SAR ADCs) are preferred for low-power applications such as wearable and biomedical sensor systems because of its simple architecture. Although the semiconductor fabrication processes have evolved considerably over the years, the analog blocks of ADCs cannot fully take advantage of the advanced technology and remains as power-hungry components because of accuracy and speed requirements. Therefore, studies for reducing the switching energy of the capacitive digital-to-analog converter (C-DAC) which is the most power consuming block of SAR ADCs have been published and these efforts have led to the development of various switching schemes of C-DAC [1-11]. These trials are based on the fact that switching energy is proportional to capacitance as expressed by the equation below (1) [1].

$$E = -CV_X\left(V[2]-V[1]\right) \tag{1}$$

The switching energy (E) is required when the potential difference of capacitor (C) is changed from $V[1]$ to $V[2]$ and Vx is reference voltage on bottom plate of each capacitor. Therefore, the effective method to decrease total switching energy of C-DAC for SAR ADCs is reducing the switching energy required by switching capacitors that have relatively larger capacitance among the capacitors array [2].

Fig. 1 shows the energy efficient switching on the first and the second conversion steps of previous C-DACs [2]. In this scheme, the most significant bit (MSB) ($2C$) capacitor is switched from ground to V_{REF} in the first conversion step and no switching energy is consumed. Subsequently, the MSB capacitor is switched from V_{REF} to $V_{CM}(V_{ref}/2)$ or the second MSB ($1C$) capacitor is switched from V_{REF} to ground in the second conversion, where a switching energy of $0.25CV^2_{REF}$ and $0.75CV^2_{REF}$

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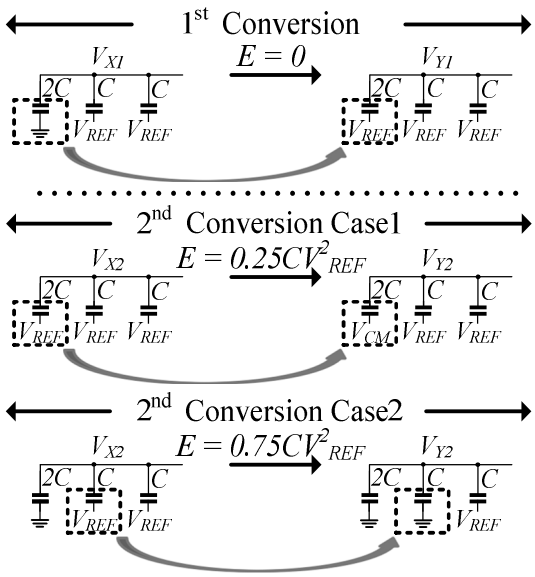


Fig. 1. Energy efficient switching on first and second conversion step in previous scheme [2].

is consumed for each case, respectively. However, switching the largest capacitor (*2C*) from V_{ref} to V_{CM} causes a large size (*W/L*) switch.

II. ARCHITECTURE

In the proposed spread second capacitor capacitive digital-to-analog converter (SSC C-DAC) scheme, all capacitors except the MSB capacitor are switched at the second conversion step. Fig. 2 shows the examples of the second conversion for the proposed SSC C-DAC. Each case shows two switching cases after the second comparison. In the second conversion step, all bottom node voltages of the capacitors except for the MSB capacitor are switched from V_{REF} to V_{CM}, which results in a $1/4V_{REF}$ voltage change at the top plate of the capacitors ($V_{Y2} = V_{X2} - 1/4V_{ref}$). Fig. 3 shows the examples of the switching procedure of a 4-bit SSC C-DAC. At the sampling phase, all capacitors except the MSB capacitors are connected to $V_{REF,}$ and the MSB capacitors are connected to ground. The sampling phase is then followed by the conversion phases. At the first conversion step, the bottom plate of the MSB capacitor in the capacitive array that has a lower top plate voltage (V_N or V_P) is switched from ground to V_{REF}. For simplicity, only one case ($V_P - V_N > 0$) is shown. The first conversion step does not require switching energy. At the second conversion step, the bottom plates of all

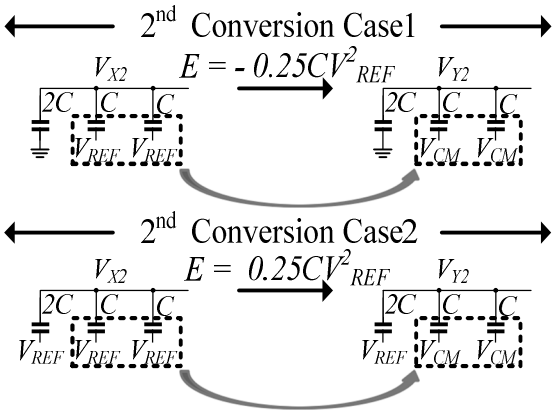


Fig. 2. Block diagram of the proposed transmitter.

capacitors except the MSB capacitor of only one side of the capacitive array that has a higher top plate voltage (V_N or V_P) are switched from V_{REF} to V_{CM}. At the third conversion steps, the merged capacitor switching (MCS) scheme [3] is partially applied to all capacitors that are connected to V_{CM}. If the capacitors that are connected to V_{CM} are in the V_P C-DAC array and $V_P > V_N$, the bottom plate of the capacitor in the V_P C-DAC array is switched from V_{CM} to ground. If $V_P < V_N$ for the same scenario, the bottom plate in the V_P C-DAC array is switched from V_{CM} to V_{REF}. If the capacitors that are connected to V_{CM} are in the V_N C-DAC array and $V_P > V_N$, the bottom plate in V_N C-DAC array is switched from V_{CM} to V_{REF}. If $V_P < V_N$ for the same scenario, the bottom plate in the V_P C-DAC array is switched from V_{CM} to ground. The switching method of remaining conversion steps is the same with that of the third conversion step. Fig. 4 shows a 10-bit C-DAC configuration of the proposed SSC scheme. Because a role of capacitors for second conversion steps are spread from *64C* to *C* with top plate sampling, the total number of unit capacitors can be reduced by a quarter compared to conventional C-DAC. As a result, the proposed switching scheme does not require to connecting the MSB capacitors to V_{CM} unlike previous switching schemes [2, 3]. Therefore, the burden of switches for driving the MSB capacitors can be reduced.

III. MEASUREMENT RESULTS

The proposed switching scheme was fabricated in a 0.18-μm process. The differential-type 10-bit SAR ADC operating at 1.8 V and 10-MS/s with an ADC core area

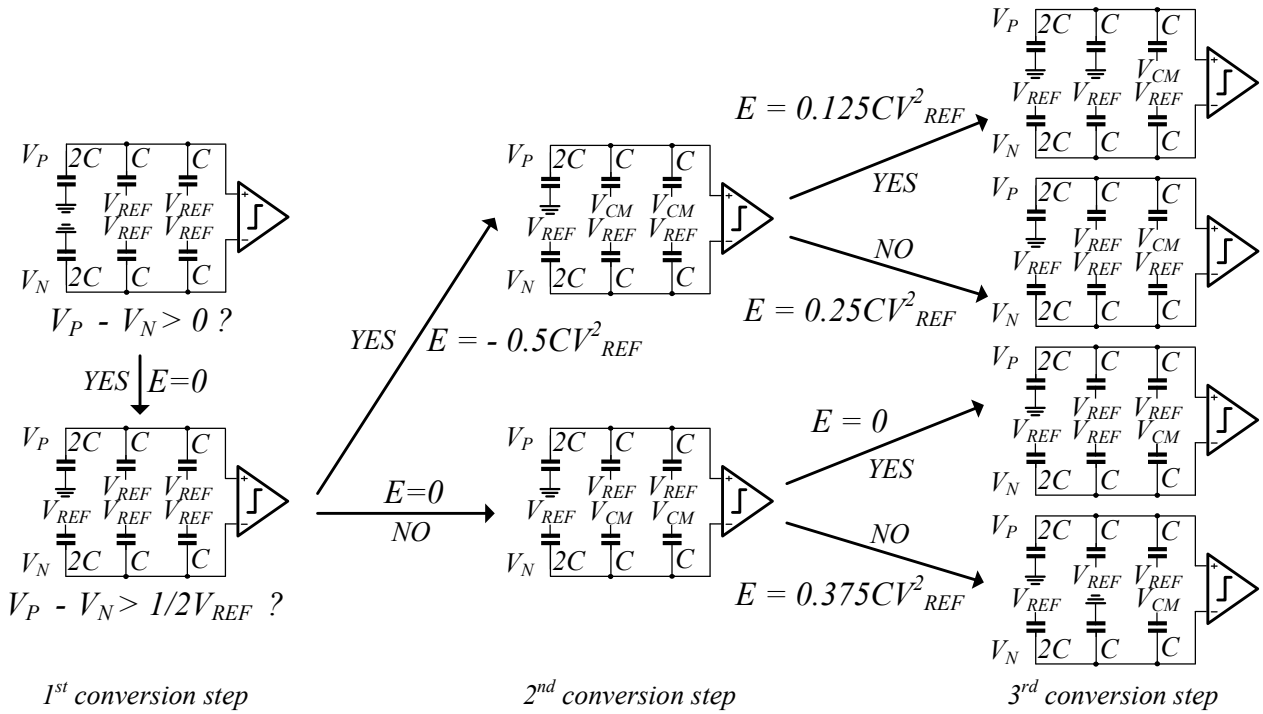


Fig. 3. Examples of switching procedure of 4-bit SSC C-DAC.

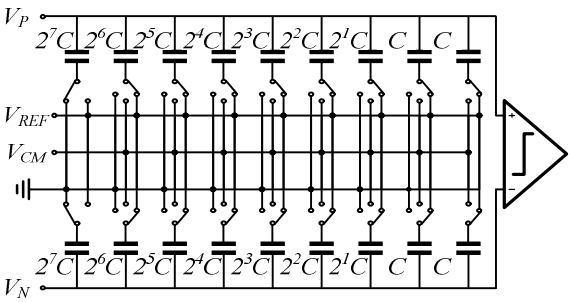
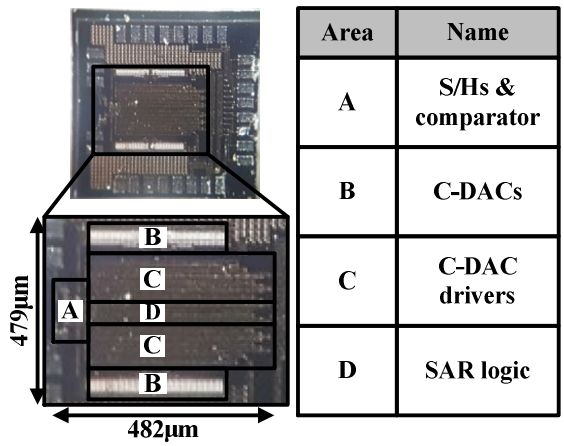


Fig. 4. C-DAC of the SSC scheme with a 10-bit SAR ADC.

occupying 0.479 × 0.482 μm^2 was fabricated. Fig. 5 shows the chip die photo of the SAR ADC. Fig. 6 shows the dynamic performance of the SAR ADC. The test result shows an SFDR of 60.9 dBc, a SINAD of 53.1 dB and an ENOB of 8.5 bit. Fig. 7 shows the ENOB trend according to the input frequency from 1 MHz to 5 MHz. Fig. 8 shows the static performance of the SAR ADC. The DNL and INL is 2.8/-1 and 3.7/-3.6 LSB, respectively. The switching energy of the proposed SSC C-DAC for SAR ADCs is verified in MATLAB. Fig. 9 compares the switching energy of the proposed SSC C-DAC with previous switching methods for C-DAC of SAR ADCs. The average switching energies reported in



Area	Name
A	S/Hs & comparator
B	C-DACs
C	C-DAC drivers
D	SAR logic

Fig. 5. SAR ADC die photo.

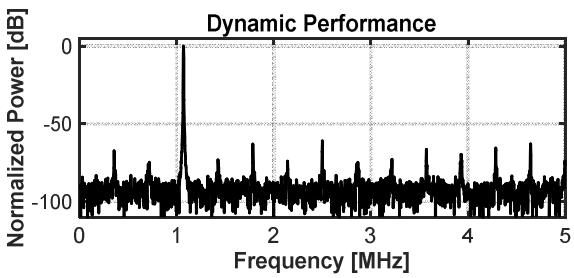


Fig. 6. Dynamic test results at 1 MHz input frequency and 4096 FFT points.

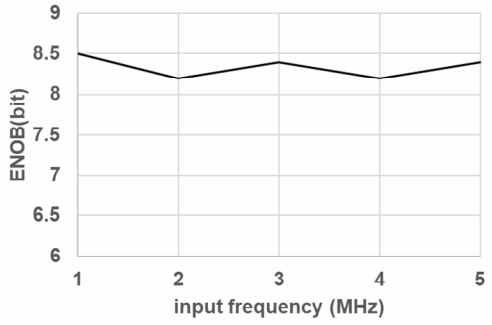


Fig. 7. Dynamic test results using 1 MHz to 5 MHz input frequency FFT points.

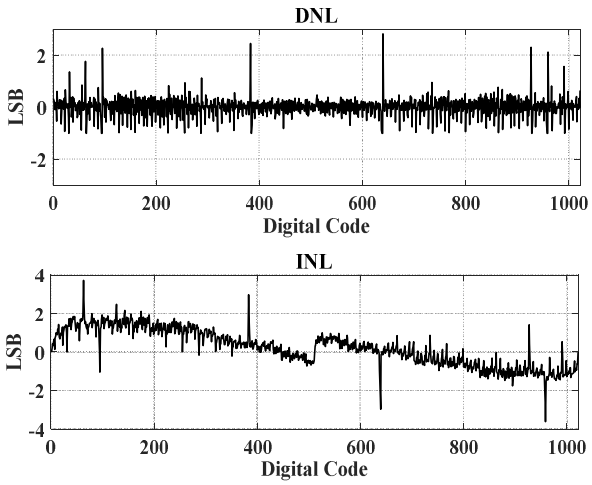


Fig. 8. Static performance of the SAR ADC.

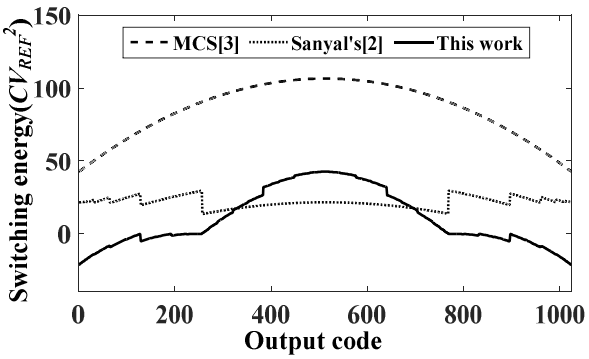


Fig. 9. Switching energy versus output code.

[2, 3] are $21.3CV_{REF}^2$ and $82.1CV_{REF}^2$, respectively. The average switching energy of the proposed scheme is $26.4CV_{REF}^2$. Compared to the conventional scheme, the proposed scheme saves switching energy by 98.1%. Table 1 shows the comparison table of the switching scheme for a 10-bit SAR ADC. The number of total unit capacitors is also reduced by 75% compared to conventional C-DAC. Table 2 shows the performance summary of an ADC.

Table 1. Comparison of switching energy for a 10-bit SAR ADC

Switching scheme	Average Energy (CV_{REF}^2)	Energy saving	Total Unit Capacitor
Conventional	1363.3	Reference	2048
MCS[3]	82.1	93.7%	1024
Sanyal[2]	21.3	98.4%	512
This work	26.4	98.1%	512

Table 2. Performance summary of an ADC

Specification	
Process	0.18 μm CMOS
Supply voltage	1.8 V
Resolution	10-bit
Sampling rate	10-MS/s
ENOB	8.5 bit
DNL/INL	2.8/-1 LSB / 3.7/-3.6 LSB
Sampling capacitor	5 pF
Active area	0.23 mm^2
Power consumption	3.8 mW

IV. CONCLUSIONS

An energy-efficient SSC C-DAC is proposed. In the proposed switching scheme for low power consumption, the burden of the switches making V_{CM} can be mitigated. The switching energy and the number of total unit capacitors are reduced by 98.1% and 75%, respectively, when compared to conventional C-DAC. This proposed switching scheme was verified with SAR ADCs operating at 1.8 V and 10-MS/s with the ADC core area of 0.479 × 0.482 μm^2, fabricated using the 0.18-μm CMOS process. The dynamic performance of the SAR ADC shows a SFDR of 60.9 dBc, a SINAD of 53.1 dB and an ENOB of 8.5 bit at a 1MHz input frequency.

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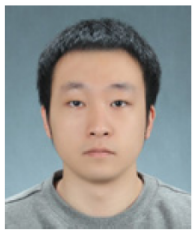

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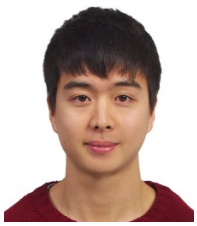

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