CHARACTERIZATION AND INVESTIGATION OF LOW-FREQUENCY NOISE IN EMERGING CMOS

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A thesis submitted to the Nanyang Technological University
in partial fulfilment of the requirement for the degree of
Doctor of Philosophy

2011

Acknowledgements

Many people have contributed and helped me during the whole course of study. It is my pleasure to express my gratitude to them.

First of all, I would like to thank A/P Dr. Zhou Xing, my research supervisor from Nanyang Technological University (NTU) Singapore. I am deeply indebted to him for his relentless effort in guiding and encouraging me during my research. By experiencing his solid and excellent review of my papers, his scientific and ethical standards are ones I really aspire to. I would also like to thank my co-supervisor Dr. Xiong Yong-Zhong from Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR) Singapore for providing me the wafers and measurement facilities. The brainstorming discussions and his patience in answering all my doubts have also helped me find solutions to numerous problems.

I also acknowledge the scholarship support from GLOBALFOUNDRIES Singapore and NTU. I have benefited tremendously from my association with GLOBALFOUNDRIES, especially with Dr. Lap Chan and Dr. Ng Chee Mang, due to their expertise in the microelectronics field. In addition, GLOBALFOUNDRIES has also provided the wafer support and invaluable process information. The progress of this research may suffer without the support from them.

I would also like to appreciate the help from the graduated seniors (Lim Khee Yong, Chiah Siau Ben, Karthik Chandrasekaran, and See Guan Huei) and current members of the group (Lin Shihuan, Zhu Guojun, Zhang Junbin, Machavolu Kamakshi Srikanth, Priti Bathla, Wang Zhihuan, Ashwin Srinivas, Chen Zuhui,

William Chandra, Yan Yafei, and Ramachandran Selvakumar) for providing valuable discussions and insights for my work at different stages of my research.

Last but not the least, I would like to express my deepest gratitude to my parents for their understanding, encouragement and mental support during the entire course of my research study. They have been, and will be my biggest strength.

Contents

Summary

In this thesis, low-frequency noise (LFN) mechanisms of multiple-gate transistors are investigated. The first-time observations and analyses, together with necessary modifications or re-derivations of LFN model equations, provide important guidance for multiple-gate transistor circuit designs and multiple-gate MOS technology optimizations. Performing meaningful LFN measurements in the presence of undesired disturbances from electronic equipments is always a difficult task. A floating-gate (FG) test structure that constructs the characterized MOSFET with an extra control gate is proposed for the MOS transistors. By using this test structure, no gate bias is required in the drain-current noise measurement. As a result, any potential disadvantages from gate-bias supply networks that would prevent accurate noise measurements are totally excluded. It is also the first experimental demonstration in MOS technology for the joint effect of a backgating noise and an instrumental disturbance observed in planar resistors. The FinFET and the nanowire transistor are both important candidates for future CMOS scaling beyond the 32-nm node. Hence, the investigation of LFN characteristics in symmetric double-gate (DG) FinFETs and gate-all-around (GAA) silicon nanowire transistors (SNWTs) from weak to strong inversion at low drain bias is performed. The dominant noise generation mechanism changing from mobility fluctuation to number fluctuation as the conduction behavior changing from volume to surface in both FinFETs and SNWTs is observed and analyzed for the first time. In weak inversion, the analytical expressions of the drain-current noise spectra for the FinFET and the SNWT are re-derived respectively based on the Hooge's theory. For SNWTs in weak inversion, the impact of the channel

orientations on the LFN is also studied for the first time. It is concluded that stronger current and mobility enhancement in <010> orientation translates to a higher LFN level in the same orientation. And the channel orientation study further confirms that the mobility fluctuation mechanism is dominant in weak inversion. In strong inversion, for FinFETs, to determine the causes of the observed deviation from the unity slope of the noise–frequency dependence, detailed measurements of the temperature dependence of the noise power spectra are performed. The model equations based respectively on the Dutta–Horn's and McWhorter's theories are both re-derived for analyzing the noise characteristics in FinFETs, and the applicability of both models is thoroughly discussed. Since the workfunction difference between the poly-Si gate and the almost-intrinsic Si-channel of the SNWT sets the threshold voltage too low, for SNWTs in strong inversion, besides the devices with poly-Si gate, the LFN characteristics of SNWTs with two other gate electrodes, namely, the doped fully-silicided (FUSI) gate and undoped FUSI gate, are also included in the discussion. This is the first time that the impact of different gate electrodes on the LFN of SNWTs is reported. FUSI metal gate shows superior suppression of correlated mobility scattering than the poly-Si gate. The SONOS-type non-volatile memory (NVM) cells fabricated based on the FinFET or the SNWT demonstrated good memory performance with the Fowler–Nordheim (FN) tunneling, a widely used programming and erasing mechanism. Hence, a comparative investigation of the degradation of LFN levels caused by FN tunneling stress for both the SNWT and the FinFET is performed. The impact of device architectures on the oxide degradation under different polarities and magnitudes of the stress voltage is studied for the first time. The SNWT with cylindrical channel induces a higher electric field at the Si/SiO_2 interface than that in the planar-channel FinFET, thus, the SNWT is more vulnerable for oxide degradation.

As the fabrication process of the multi-gate transistors investigated is bulk-CMOS compatible, the oxide and lattice quality of multi-gate transistors revealed by the LFN measurements is comparable with that of the bulk CMOS.

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List of Symbols

The following is a list of symbols used in the text.

Symbol	Description (unit, if applicable)
α	Scattering parameter in the correlated mobility fluctuation model (Vs/C)
α_C	Coulombic scattering parameter in the correlated mobility fluctuation model (Vs/C)
α_H	Hooge parameter
$\alpha_{H,j}$	Hooge parameter related to each scattering process *j*
$\alpha_{H,other}$	Hooge parameter related to the scattering processes other than the surface roughness scattering
$\alpha_{H,ph}$	Hooge parameter related only to the phonon scattering process
$\alpha_{H,sr}$	Hooge parameter related only to the surface roughness scattering process
α_t	Attenuation coefficient of the electron wave function in the oxide (cm^{-1})
$\Delta\Phi$	Work function difference between the gate electrode and the almost-intrinsic silicon body of the multi-gate field-effect transistor (eV)
Φ_B	Tunneling barrier height seen by the carriers in the channel (eV)
Φ_F	Potential difference between the midgap position and the Fermi level in the silicon body (V)
Φ_{MS}	Workfunction difference between the gate electrode and silicon body (V)
ψ	Electric potential across the silicon body of the field-effect transistor (V)
ψ_s	Surface potential of the field-effect transistor (V)
τ	Time constant for transitions (s)
τ_o	Characteristic attempt time for the random process (s)
τ_1	Lower limit of the transition time constant (s)
τ_2	Upper limit of the transition time constant (s)
τ_c	Capture time of a random-telegraph-signal noise (s)
τ_e	Emission time of a random-telegraph-signal noise (s)
τ_H	Time duration in the higher level of a two-level random-telegraph-signal noise (s)
τ_L	Time duration in the lower level of a two-level random-telegraph-signal noise (s)
$\tau_{ph\text{-}ph}$	Mean free time between the phonon-phonon scattering (s)
τ_t	Tunneling transition time constant in the classical tunneling model where the tunneling time decays exponentially with the trap depth from the interface (s)
τ_{th}	Tunneling transition time constant in the thermally activated oxide trap model where the tunneling time decays exponentially with the trap

	activation energy (s)
μ	Effective mobility of carriers in a semiconductor body ($cm^2/(Vs)$)
μ_0	Low-field mobility of channel carriers ($cm^2/(Vs)$)
μ_{ac}	Mobility limited only by the surface acoustic phonon scattering ($cm^2/(Vs)$)
μ_C	Mobility limited only by the Coulombic scattering ($cm^2/(Vs)$)
$\mu_{C,\,imp}$	Mobility limited only by the Coulombic scattering caused by impurities ($cm^2/(Vs)$)
$\mu_{C,OX}$	Mobility limited only by the Coulombic scattering caused by charges in the oxide ($cm^2/(Vs)$)
μ_j	Mobility of carriers limited by each scattering process *j* ($cm^2/(Vs)$)
μ_{other}	Mobility of carriers limited by the scattering processes other than the surface roughness scattering ($cm^2/(Vs)$)
μ_{ph}	Mobility of carriers limited only by the bulk phonon scattering process ($cm^2/(Vs)$)
μ_{sr}	Mobility of carriers limited only by the surface roughness scattering process ($cm^2/(Vs)$)
ε_{ox}	Permittivity of oxide (F/cm)
ε_{si}	Permittivity of silicon (F/cm)
λ	Tunneling attenuation length predicted by the Wentzel-Kramers-Brillouin approximation (cm)
σ	Conductivity of a semiconductor body (S/m)
θ	Mobility-degradation parameter due to the gate voltage of the field-effect transistor (V^{-1})
ω	Angular frequency (Hz)
γ	Frequency exponent of a flicker noise spectrum
C_d	Depletion capacitance per unit gate area (F/cm^2)
C_{it}	Interface state capacitance per unit gate area (F/cm^2)
C_{MIM}	Capacitance of the metal-insulator-metal capacitor used in the floating-gate test structure (F)
C_n	Gate oxide capacitance of the field-effect transistor under test (F)
C_{ox}	Gate oxide capacitance per unit gate area (F/cm^2)
C_P	Capacitance of the field-effect transistor that replaces the metal-insulator-metal capacitor in the floating-gate test structure (F)
C_T	Total capacitance seen by the floating gate of the floating-gate test structure (F)
d_{nw}	Diameter of the silicon core of the silicon nanowire transistor (cm)
E	Energy level of the oxide trap (eV) / Vertical electric field at Si/SiO_2 interface (V/cm)
E^*	Energy level corresponding to the sharp peak of the Lorentzian function in the thermal-activation low-frequency noise model (eV)
E_C	Energy level of the bottom of the conduction band (eV)
E_{fn}	Electron quasi-Fermi level (eV)
E_F	Fermi energy level (eV)
E_{ox}	Electric field level required to be across the gate oxide of the field-effect transistor under test for Fowler-Nordheim tunneling to occur (V/cm)
E_V	Energy level of the top of the valence band (eV)
f	Frequency (Hz)

f_0	Cutoff frequency of a Lorentzian spectrum (Hz)
f_1	Lower limit of the low-frequency noise measurement bandwidth (Hz)
f_2	Upper limit of the low-frequency noise measurement bandwidth (Hz)
f_t	Fermi-Dirac trap occupancy function
g_{IN}	Finite input conductance of the operational amplifier inside SR570 (S)
g_m	Transconductance of a field-effect transistor (S)
g_{offset}	Finite source conductance of the current offset source inside SR570 (S)
g_{OUT}	Output channel conductance of the field-effect transistor (S)
h	Planck's constant (4.13566733×10^{-15} (eV)s)
H_{fin}	Fin height of the FinFET (cm)
i_{DS}	Total drain current including both the dc bias current and the noise current (A)
i_{MEAS}	Measured low-frequency small-signal drain-current noise through SR570 (A)
i_{noise}	Intrinsic low-frequency small-signal drain-current noise source (A)
I	DC bias current in a semiconductor body (A)
I_d	DC bias drain current (A)
$I_{ds,final}$	Drain-current level desired during low-frequency noise measurements and input during the stage of CHARGE/DISCHARGE operations (A)
$I_{ds,present}$	Drain-current level of the field-effect transistor under the "present state" and measured during the stage of CHARGE/DISCHARGE operations (A)
k	Boltzmann constant (8.617343×10^{-5} eV/K)
L	Effective channel length (cm)
L_{mask}	Mask length of the field-effect transistor (cm)
m	Ideality factor related to the gate bias in the subthreshold current expression of the field-effect transistor
m'	Ideality factor related to the drain bias in the subthreshold current expression of the field-effect transistor
m^*	Effective mass of carriers in the oxide ($(eV)s^2/cm^2$)
n_1	Electron density across the silicon fin of a FinFET between two Si/SiO_2 interfaces at a gate voltage of 0.05 V of (cm^{-3})
n_2	Electron density across the silicon fin of a FinFET between two Si/SiO_2 interfaces at a gate voltage of 0.1 V of (cm^{-3})
n_3	Electron density across the silicon fin of a FinFET between two Si/SiO_2 interfaces at a gate voltage of 0.9 V of (cm^{-3})
n_i	Intrinsic carrier concentration (cm^{-3})
N	Total number of carriers in a semiconductor body
N^*	Number of channel carriers per unit gate area
N_t	Near-interface oxide trap density per unit volume per unit energy ($cm^{-3}eV^{-1}$)
N_t'	Near-interface oxide trap density per unit area per unit energy ($cm^{-2}eV^{-1}$)
N_T	Average total number of active traps in a semiconductor body
q	Elementary electric charge (1.6×10^{-19} C)
Q_{FG}	Charges on the floating gate of the floating-gate test structure (C)
Q_G	Charge density on the gate of field-effect transistor per unit gate area (C/cm^2)
Q_i	Charge density of the inversion layer per unit gate area (C/cm^2)

Q_{ox}	Oxide charge density per unit gate area (C/cm^2)
r	Resistance of a semiconductor body (Ω)
R	Radius of the silicon core of the silicon nanowire transistor (cm)
R_{acc}	Total access resistance by summing over the series resistances of both the source and drain sides of the field-effect transistor (Ω)
R_D	Series resistance of the drain side of the field-effect transistor (Ω)
R_{IN}	Finite input resistance of the operational amplifier inside SR570 (Ω)
R_{offset}	Finite source impedance of the current offset source inside SR570 (Ω)
R_S	Series resistance of the source side of the field-effect transistor (Ω)
S	Subthreshold slope of the field-effect transistor (mV/dec)
S_σ	Power spectral density of the fluctuations in the conductivity of a semiconductor body ($S^2/(m^2Hz)$)
S_μ	Power spectral density of the fluctuations in the effective mobility of carriers in a semiconductor body ($cm^4/(V^2s^2Hz)$)
$S_{\mu j}$	Power spectral density of the fluctuations in the mobility limited by each scattering process j ($cm^4/(V^2s^2Hz)$)
S_I	Power spectral density of the current noise (A^2/Hz)
S_{Id}	Power spectral density of the drain-current noise (A^2/Hz)
S_{Id_add}	Power spectral density of the additional drain-current noise introduced due to the floating-gate interface-induced thermal noise (A^2/Hz)
S_N	Power spectral density of the fluctuations in the number of carriers (Hz^{-1})
S_{Qox}	Power spectral density of the fluctuations in the oxide charge density ($C^2/(cm^4Hz)$)
S_r	Power spectral density of the fluctuations in the resistance of a semiconductor body (Ω^2/Hz)
S_{vn}	Power spectral density of the thermal voltage fluctuations of a capacitor under open-circuit conditions (V^2/Hz)
S_V	Power spectral density of the voltage noise (V^2/Hz)
S_{Vd}	Power spectral density of the drain-voltage-referred noise (V^2/Hz)
S_{Vfb}	Power spectral density of the fluctuations in the flatband voltage due to near-interface oxide traps (V^2/Hz)
S_{Vg}	Power spectral density of the gate-voltage-referred noise (V^2/Hz)
t	Time (s)
t_{ox}	Thickness of the gate oxide (cm)
t_{si}	Fin width of the FinFET (cm)
T	Temperature (K)
v_n	Thermal voltage fluctuations of a capacitor under open-circuit conditions (V)
v_{noise}	Low-requency small-signal voltage noise source (V)
V	Difference of the electron quasi-Fermi potential from the hole quasi-Fermi potential or just the electron quasi-Fermi potential if the silicon body is almost intrinsic (eV)
V_{ds}	Drain voltage with source grounded (V)
V_D	Voltage applied to the drain side of the field-effect transistor during the stage of CHARGE/DISCHARGE operations (V)
V_{DD}	Voltage applied to both the source and drain sides of the field-effect transistor during the DISCHARGE operation of the floating-gate test structure (V)

V_{fb}	Flatband voltage (V)
V_{FN}	Voltage level required to be across the gate oxide of the field-effect transistor under test for Fowler-Nordheim tunneling to occur (V)
V_{gs}	Gate voltage with source grounded (V)
V_G	Voltage applied to the gate of the multi-gate field-effect transistors during the constant-voltage Fowler-Nordheim tunneling stress (V)
V_{nn}	Voltage across the gate oxide of the field-effect transistor under test during the CHARGE/DISCHARGE operations (V)
V_{ox}	Voltage drop across the gate oxide of the field-effect transistor (V)
V_P	Voltage applied to the external control terminal of the floating-gate test structure (V)
V_S	Voltage applied to the source side of the field-effect transistor during the stage of CHARGE/DISCHARGE operations (V)
V_T	Threshold voltage (V)
W	Effective channel width (cm)
x	Distance along the channel length from the source side of the field-effect transistor (cm)
y	Distance along the channel width of the field-effect transistor (cm)
z	Distance perpendicular to the gate surface from the Si/SiO_2 interface of the field-effect transistor (cm)
z^*	Trap location corresponding to the sharp peak of the Lorentzian function in the conventional equi-energy tunneling low-frequency noise model (cm)

List of Acronyms

The following is a list of acronyms used in the text.

Acronyms	**Description**
BN	**B**ackground **N**oise
BOX	**B**uried **OX**ide
BSIM	**B**erkeley **S**hort-channel **I**nsulated-gate field-effect transistor **M**odel
CMOS	**C**omplementary **M**etal **O**xide **S**emiconductor
DC	**D**irect **C**urrent
DG	**D**ouble **G**ate
DSA	**D**ynamic **S**ignal **A**nalyzer
FG	**F**loating-**G**ate
FN	**F**owler-**N**ordheim
FUSI	**FU**lly-**SI**licided
GAA	**G**ate-**A**ll-**A**round
G-R	**G**eneration-**R**ecombination
IITN	**I**nterface-**I**nduced **T**hermal **N**oise
IMD	**I**nter-**M**etal-**D**ielectrics
LFN	**L**ow-**F**requency **N**oise
MIM	**M**etal-**I**nsulator-**M**etal
MOSFET	**M**etal-**O**xide-**S**emiconductor **F**ield-**E**ffect **T**ransistor
NVM	**N**on-**V**olatile **M**emory
Op-Amp	**Op**erational **Amp**lifier
PSM	**P**hase-**S**hift-**M**ask
RF	**R**adio **F**requency
RO	**R**ing **O**scillator
RTA	**R**apid-**T**hermal-**A**nnealing
RTS	**R**andom **T**elegraph **S**ignal
S/D	**S**ource/**D**rain
SIIS	**S**ilicidation-**I**nduced **I**mpurity **S**egregation
SNWT	**S**ilicon **N**ano**W**ire **T**ransistor
SOI	**S**ilicon-**O**n-**I**nsulator
WKB	**W**entzel-**K**ramers-**B**rillouin

CHAPTER 1: **Introduction**

The device dimensions and thus the supply voltage are scaled down as the technology node advances. In order to suppress the short-channel effect while maintaining the device performace, more complex device structures and/or new materials have been explored. Due to its inverse dependence on the gate area, low-frequency noise (LFN) level is also elevated with device scaling. The signal-to-noise ratio is degraded and LFN beomes a showstopper in certain applications [1]. The main topic of this work is to investigate the LFN properties and understand the LFN generation mechanisms in advanced device structures that may be the candidates for future analog and digital applications. The experiences on different device structures and materials used in the investigated ones can serve as a guideline for device design and fabrication in low-noise applications. Increased LFN with the device downscaling makes it extremely important to understand the origin of the noise and to reduce it with a proper device design.

1.1. Motivations

Due to the past 40 years of continued scaling, conventional bulk MOSFETs are approaching their scaling limit. More and more issues have arisen over the years of aggressive scaling, such as the gate leakage and short-channel effects. Among the techniques explored to overcome these problems, the multiple-gate transistor architecture is a very attractive solution for ultra-scaled CMOS technologies beyond

the 45-nm technology node. The transistor with multiple gates and fully-depleted body provides an improved electrostatic control over the channel, and thus, suppresses the short-channel effects. The SOI structure is able to reduce the junction leakage and improve the electrical isolation even with a nearly undoped body. Several multiple-gate transistor architectures have been proposed, such as FinFETs [2], Omega FETs [3], and gate-all-around (GAA) nanowire transistors [4]. With the increased number of gates in the multigate transistor structures, the drive current, the electrostatic control of the channel, and the control of the short-channel effects are enhanced correspondingly.

Presently, only a few publications are available on the LFN properties of multiple-gate transistors. The process and material influence on the LFN of double-gate FinFETs including the hydrogen annealing step used during the gate oxide processing and different gate materials (Mo, poly-Si) used during the gate electrode processing were reported in [5] and [6], respectively. The general geometry dependence of LFN in the linear region was reported for trigate FinFETs [7]. For a single small-area GAA nanowire transistor, the random telegraph signal (RTS) noise characteristics was studied [8]. While the summarized LFN behaviors of multiple GAA nanowire transistors biased in the linear region were reported in [9], and the effect of source/drain series resistance on the LFN was investigated at the same time. From the above few reports on the LFN characteristics of multiple-gate transistors so far, obviously there are many issues to be explored. Therefore, further LFN investigations of multiple-gate transistors are urgently needed, which can act as part of the guidelines for novel multigate-transistor circuit designs and further optimizations of the multiple-gate CMOS technology.

1.2. Objectives

The objectives of this research are to

i. Propose a new methodology for accurate LFN characterization.

ii. Study the LFN mechanisms of double-gate FinFETs.

iii. Study the LFN mechanisms of GAA silicon nanowire transistors (SNWTs).

iv. Extract the noise parameters (e.g., Hooge parameter, oxide-trap density) of FinFETs and SNWTs with necessary modifications or rederivations of the noise model equations, and compare with those in bulk MOSFETs.

1.3. Approaches

Firstly, the current conduction behaviours of FinFETs and GAA SNWTs have to be thoroughly studied, since the difference between the volume conduction and surface conduction may affect the LFN behaviours, and the dc parameters extracted in this stage are necessary for the noise parameter extraction in a later stage. Then, the LFN characterization is carried out, which itself is a very challenging task. Before any analysis on LFN mechanisms, acquiring reliable LFN data without disturbances from the power supply and environment is very important. After obtaining all the necessary noise data, through the bias, geometry, temperature, and frequency dependences of the LFN data, it could be concluded whether the LFN is generated from mobility fluctuations or number fluctuations or correlated. After that, the noise parameters like Hooge parameter and oxide-trap density could be extracted correspondingly in the respective case. Note that for noise parameter extractions, the model equations of LFN

in bulk MOSFETs have to be modified whenever necessary for their applications in FinFETs or SNWTs.

1.4. Major contributions of the thesis

The major contributions of this thesis are listed below:

i. Proposed a new test structure for accurate LFN characterization of CMOS devices, which could totally exclude the noise contribution from the bias network at the gate side. And this method could easily be used in the non-volatile memory floating-gate structures.

ii. Investigated LFN mechanisms of double-gate FinFET transistors from weak to strong inversion. The different conduction behaviours in different operation regions were discussed together with the different noise mechanisms observed.

iii. Studied the temperature dependence of LFN in the double-gate FinFET biased in the strong-inversion region. Applicability of McWhorter model and thermal-activation model were then discussed.

iv. Investigated the LFN mechanism of GAA SNWTs biased in the subthreshold region. Similar to the FinFET case, the volume-inversion effect on LFN in this region was discussed.

v. Studied the channel orientation dependence of the LFN in SNWTs biased in the subthreshold region to further confirm the noise generation mechanisms in this region.

vi. Investigated the LFN mechanisms of GAA SNWTs biased in the strong-inversion region. The impact of different gate electrodes on the LFN was observed and studied.

vii. Performed the constant-voltage Fowler–Nordheim (FN) tunnelling stress on both FinFETs and SNWTs with different magnitudes and polarities of the stress voltage. And the impact of the device architectures on the LFN was clearly oberserved by this comparative study.

1.5. Organization of the thesis

This thesis is written in six chapters. Chapter one introduced the motivations, objectives, approaches, and major contributions of this work.

Chapter two briefly reviews the fundamental 1/*f* noise concepts, namely, the number fluctuation and mobility fluctuation theories. The most powerful description available so far for LFN characteristics in MOSFETs, in terms of agreement with experimental data, is the so-called correlated mobility fluctuation theory. However, for the small-area devices, only a handful of near-interface traps remain active, resulting in a specific RTS noise behaviour.

Chapter three first describes the conventional measurement setup for LFN characterization, and then introduces an alternative and accurate way of driving the CMOS device into different drain-current levels for LFN characterization. A floating-gate (FG) test structure that constructs the characterized MOSFET with an extra control gate is proposed. A metal-insulator-metal (MIM) capacitor is used to construct this control gate. Instead of applying different input DC bias supplies for the gate terminal of the MOSFET, the device is directly programmed to the drain-current levels

of interests by CHARGE/DISCHARGE operations. In this case, no gate bias is required in the drain-current noise measurement, so that any potential disadvantages from gate-bias supply networks that would prevent accurate noise measurements are totally excluded. The LFN measurement results demonstrating the feasibility of the proposed test structure are also reported.

Chapter four presents the LFN characteristics of symmetric double-gate n-FinFETs from weak to strong inversion at low drain bias. The noise generation mechanism is investigated. The measured drain-current noise spectral density shows that LFN in the weak-inversion subthreshold region can be well described by the mobility-fluctuation model due to volume-inversion conduction behavior, which is very different from those normally observed in the bulk NMOS. The analytical expression for the drain-current noise spectral density is derived, with the Hooge parameter α_H being extracted. In the strong inversion region, the gate-voltage dependence of the room-temperature noise data agrees with the number-fluctuation model, but the slope of the frequency dependence is less than one. To determine the causes of the observed deviation from the unity slope, detailed measurements of the temperature dependence of the noise power spectra are performed and results from two devices are presented in this chapter. It is found that both the magnitude and the frequency dependence of the drain-voltage noise spectral density vary greatly in the range between 223 and 383 K. The experimental results are compared with two models derived based on the Dutta–Horn and the McWhorter models. It is shown that the thermal-activation model of Dutta–Horn is more convincing than the latter, which shows that the noise is due to the capture and emission of carriers by oxide traps through thermal activation. The surface-trap density at a specific activation energy is extracted.

Chapter five first investigates the LFN in the subthreshold region of both n- and p-type GAA SNWTs. The measured drain-current noise spectral density shows that LFN in this regime can be well described by the mobility-fluctuation model due to volume-inversion conduction behavior and the Hooge parameter is extracted. LFN in the SNWTs with channel oriented in <010> and <110> directions is compared. It shows that the observed mobility enhancement in the <010> direction for p-type transistors leads to a corresponding increase of the LFN level in the <010> direction compared to that in the <110> direction. Then the LFN of GAA SNWTs with different gate electrodes (poly-Si gate, doped fully-silicided (FUSI) gate, and undoped FUSI gate) is studied in the strong-inversion region. It shows that gate electrodes have a strong impact on the LFN of SNWTs. The highest noise is observed in SNWTs with poly-Si gate, compared to their FUSI-gate counterparts. The observations are explained according to the number fluctuation with correlated-mobility fluctuation theory by assuming that the correlated mobility scattering is better screened in the case of undoped-FUSI gate. Finally, the degradation of 1/*f* noise levels caused by FN tunneling stress for both SNWTs ang FinFETs is investigated. The oxide-traps generated under constant voltage FN stress are extracted from the 1/*f* noise characteristics. Under the same FN stress voltage and stress time, the amount of oxide-traps generated in the cylindrical-channel SNWT is much larger than that in the planar-channel FinFET, which is due to the increased electric field at the SiO_2/Si interface caused by the cylindrical architecture of the SNWT.

Finally, Chapter six summarizes and concludes the LFN characteristics observed in both FinFETs and SNWTs with suggestions and recommendations for future investigations.

CHAPTER 2: **Fundamental Low-Frequency Noise Mechanisms in MOSFETs**

Noise is an internally generated small signal in the device, and can be modeled as an additional voltage source or current source to the small-signal equivalent circuits. For example, for a drain-current noise source $i_{\text{noise}}(t)$ in the MOSFET, the total drain current can be expressed as $i_{\text{DS}}(t) = I_{\text{d}} + i_{\text{noise}}(t)$, where I_{d} is the ideal noiseless dc bias current. The noise component $i_{\text{noise}}(t)$ has zero average value. In the noise measurement, the noise current is characterized as the mean square value, denoted by $\overline{i_{noise}^2(t)}$. However, the amount of noise measured depends on the bandwidth of the measurement instrument, and commonly a very narrow bandwidth Δf centered at a frequency f is involved. The ratio of the mean square value $\overline{i_{noise}^2(t)}$ to this bandwidth Δf as Δf approaching zero is defined as the power spectral density of the current noise, denoted by $S_{\text{I}}(f)$ with unit of A^2/Hz. Thus, the mathematical relationship between $\overline{i_{noise}^2(t)}$ and $S_{\text{I}}(f)$ can be expressed as: $\overline{i_{noise}^2} = \int_{f_1}^{f_2} S_I(f)df$, where f_1 and f_2 are the lower and upper limits of the measurement bandwidth, respectively. Similarly, for a voltage noise source $v_{\text{noise}}(t)$, the power spectral density of the voltage noise source is denoted by $S_{\text{V}}(f)$ with unit of V^2/Hz and $\overline{v_{noise}^2} = \int_{f_1}^{f_2} S_V(f)df$. The low-frequency noise (LFN) is the noise signal dominant in the frequency range around 1 Hz to 10 kHz. Random telegraph signal (RTS) noise and $1/f$ noise are the two commonly observed noise signals in this frequency regime and are briefly reviewed below [1].

CHAPTER 2: Fundamental LFN Mechanisms in MOSFETs

2.1. Fundamental noise sources

2.1.1. Generation-recombination noise

Generation-recombination (g-r) noise in semiconductors is the fluctuations in the number of carriers for current transport originated from the random capture and emission of carriers by traps. Traps in this case mean the electronic states within the forbidden bandgap, and are related to various defects or impurities in the semiconductor and at its surfaces. The interactions between traps and transport carriers include generations and recombinations of free electrons and holes at the trap sites or free electrons (or holes) bound to and emission from the empty traps. The electronic charge of the trapped carriers can also induce fluctuations in the carrier mobility, the electric field, and the width of the space charge region etc. G-r noise is only significant when the difference between the Fermi energy level E_F and the trap energy level is within a few kT. Otherwise, few transitions will occur to produce g-r noise.When the trap level is far below the Fermi level, the trap will be filled most of the time. When the trap level is far above the Fermi level, the trap will be empty most of the time. The power spectral density of the g-r current noise S_I has the shape shown in Figure 2.1 and is called a Lorentzian. The mathematical expression of S_I is given by [10], [11]

$$S_I = \frac{S_N}{N^2} I^2 = I^2 \frac{N_T}{N^2} \frac{\tau}{1 + (2\pi f)^2 \tau^2} \tag{2.1}$$

where S_N is the power spectral density of the fluctuations in the number of carriers N, N_T is the average number of active traps, and τ is the time constant for transitions, which is related to the average capture time τ_c and emission time τ_e of a trap as $1/\tau = 1/\tau_c + 1/\tau_e$. It is seen from (2.1) that S_I is proportional to the number of traps N_T and inversely proportional to the square of the number of carriers N. The magnitude of the

time constant τ depends on the trap energy level and the spatial position of the trap. For an appropriate distribution of the time constants of multiple traps, the power spectral density may become proportional to 1/*f*.

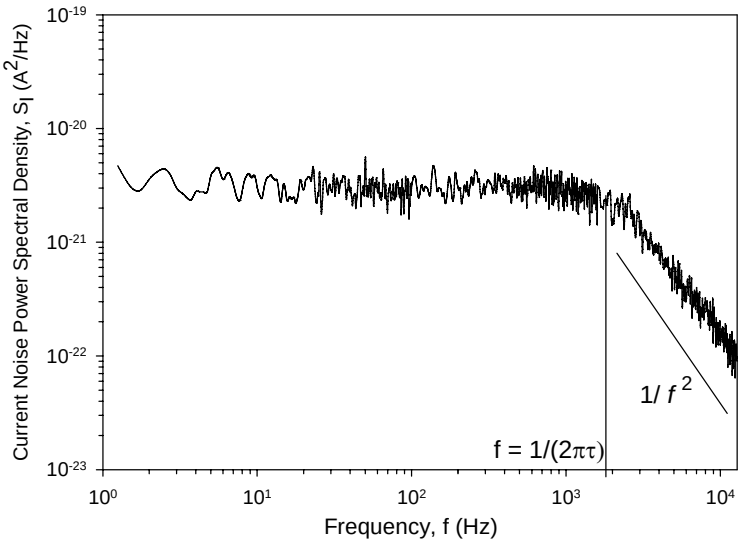

Figure 2.1: A Lorentzian shaped power spectral density in the frequency domain.

2.1.2. Random-Telegraph-Signal (RTS) noise

The RTS noise is just a special case of the g-r noise mentioned above. The summation of the RTS noise from one or more traps with identical time constants leads to the g-r noise. If the number of traps is small so that the discrete switching events are observable in the time domain, it can be viewed as the RTS noise. The current switching events between two or more states in the RTS waveform are the result of random trapping and detrapping of carriers into and out of the active traps involved. The two-level RTS noise waveform is displayed in Figure 2.2 with the switching amplitude ΔI and time durations in the lower (τ_L) and higher (τ_H) states indicated. Generally, the higher-state and lower-state time constants (τ_H and τ_L) of an RTS follow a Poisson distribution, according to [12] as Number of Occurrence (τ_H) ~

exp(–τ_H/<τ_H>) with <τ_H> the average time constant in the higher state. A similar expression holds for τ_L. These time constants can generally be identified as the capture and emission times for the corresponding traps. This two-level time-domain current noise signal can be transformed into the power spectral density form with the expression derived as [13]

$$S_I(f) = \frac{4(\Delta I)^2}{(\tau_L + \tau_H)[(1/\tau_L + 1/\tau_H)^2 + (2\pi f)^2]}. \tag{2.2}$$

Hence, the power spectral density for the RTS noise is also of the Lorentzian type. Figure 2.1 is the Lorentzian power spectral density in the frequency domain for the RTS noise signal in the time domain in Figure 2.2.

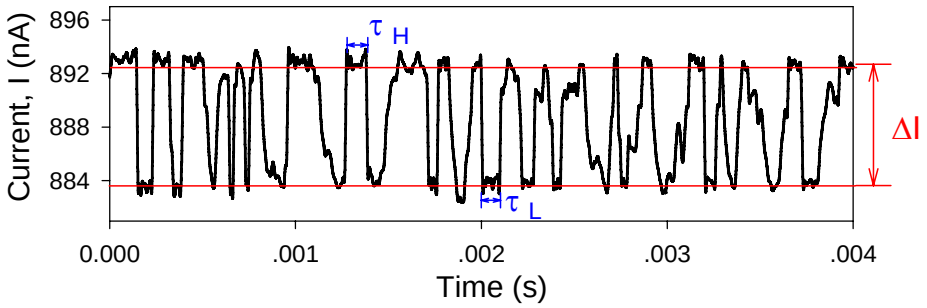

Figure 2.2: The current switches between two discrete levels when an electron moves in and out of a trap. This RTS noise waveform in the time domain corresponds to a Lorentzian in the frequency domain in Figure 2.1.

The random interaction between a single carrier and a single trap observed as a two-level RTS noise signal in the time domain is a very interesting and important phenomenon for extraction of the trap information. In the MOSFET, those DC parameters important for the noise characteriscs, such as the number of carriers for current transport and the position of the Fermi level, have a strong dependence on the bias conditions. Hence, the trap information, such as the trap energy level, capture and emission time constants, and the spatial location of the trap, can be acquired from the

bias dependence of the RTS noise signal together with the help of the temperature dependence studies [12], [14]–[16].

2.1.3. 1/*f* noise

1/*f* noise, also called flicker noise, is another important noise signal dominant in the low-frequency range. The power spectral density of such noise fluctuations is normally proportional to $1/f^{\gamma}$ with the frequency exponent γ close to 1 (0.8 ~ 1.4), which leads to the name '1/*f* '. The general form of the power spectral density for 1/*f* noise can be expressed as [10], [17]–[19]

$$S_I = \frac{KI^{\beta}}{f^{\gamma}} \tag{2.3}$$

where K is a constant and β is a current exponent.

In the earliest explanation of 1/*f* noise spectra in semiconductors in 1950 [20], [21], it was believed that 1/*f* noise was generated by the carriers trapping into and detrapping from the traps. Every single trap leads to a Lorentzian noise power spectrum. The superposition of Lorentzians of g-r noise from a large number of traps gave rise to the 1/*f* spectrum, if the distribution of the transition time constants of the traps follows [22]

$$g(\tau) = \frac{1}{\tau \ln(\tau_2 / \tau_1)} \; for \tau_1 < \tau < \tau_2 \tag{2.4}$$

where $1/\ln(\tau_2/\tau_1)$ is the normalization factor.

However, in 1969, the second mechanism in explaining the 1/*f* noise was proposed by Frits Hooge with the following empirical expression for the fluctuations of conductivity σ, mobility μ and resistance r [23]:

$$\frac{S_\sigma}{\sigma^2} = \frac{S_\mu}{\mu^2} = \frac{S_r}{r^2} = \frac{\alpha_H}{fN}. \tag{2.5}$$

It can be seen that these fluctuations were inversely proportional to the total number of charge carriers N in the sample. The independent mobility fluctuation of each of the N carriers contributes to the factor $1/N$ in (2.5) [24]. The parameter α_H is the dimensionless parameter, named the Hooge parameter. It was found that α_H depends on the crystal quality with a maximum value around 2×10^{-3} and 2–3 orders of magnitude lower for good quality materials. It was also suggested that the mobility fluctuation is mainly caused by the phonon scattering [25]. The Hooge formulation has been supported by a large amount of experimental $1/f$ noise data in metals and bulk semiconductors [18]. The weak point of the Hooge formulation is the lack of physical principles to support this mobility fluctuation assertion. Several theoretical mobility fluctuation $1/f$ noise models have been proposed [26]–[31], but there are controversies surrounding them and none of them is widely accepted so far.

There has been a long-term number fluctuation versus mobility fluctuation debate in the noise research community about the source of the $1/f$ noise. Either of the two sources has been supported as the principal noise source by an abundant experimental data. The dominant $1/f$ noise source may vary as the material of devices, the type of devices, or the operation region, etc., varies. For the MOS device, a noise generation mechanism called number fluctuations with correlated mobility fluctuations is proposed from a fresh angle by *Jayaraman* and *Sodini* [32]. The dominant noise source in this mechanism is still the trapping and detrapping interactions of the channel carriers with the oxide traps, but the mobility fluctuation induced by the coulombic scattering of channel carriers by the fluctuating trapped charges in the gate oxide is also taken into account. Apparently, these mobility fluctuations have the same

origin as the number fluctuations, thus called 'correlated' mobility fluctuations. This noise generation mechanism has been applied in the BSIM 3v3 as the compact 1/*f* noise models for both n- and p-channel MOS devices.

2.2. Number fluctuation noise in MOSFETs

In this section, the discussions will be focused on the 1/*f* noise in the MOS transistor, which is the fluctuation of drain current due to channel carriers trapping into and out of the traps inside the gate oxide, i.e., number fluctuations of channel carriers. The interactions between channel carriers and oxide traps are explained by the 1/*f* noise model proposed by McWorther in 1957 based on the quantum mechanical tunneling mechanism [33]. In this model, the tunneling time varies exponentially with the distance of the trap from the Si/SiO_2 interface. For the superposition of g-r noise with different time constants to produce 1/*f* noise, the spatial distribution of time constants must be uniform. The McWorther model agrees very well with the experimental noise data, especially for nMOS transistors [16], [34]. For pMOS transistors, deviations between number-fluctuation noise model and experimental data were often observed [35]–[37]. Later the correlated mobility fluctuation model is proposed by taking into account the Coulombic scattering effect of the oxide-trapped carriers on the mobilities of the channel carriers, in addition to the number fluctuation of channel carriers [38]. The limitation of the number-fluctuation noise model on resolving the discrepant bias dependence observed in n- and p-type MOS transistors is conquered by this correlated mobility fluctuation model. However, the effect of correlated mobility fluctuations was criticized for being overestimated without considering the screening effect of channel carriers on the Coulombic scattering [39].

The dynamic interaction between oxide traps within 3 nm from the Si/SiO_2 interface and the carriers in the channel is illustrated in Figure 2.3. Such fluctuations in the number of inversion channel carriers are translated to the fluctuations in the drain current, which can be collected by the low-frequency noise measurements.

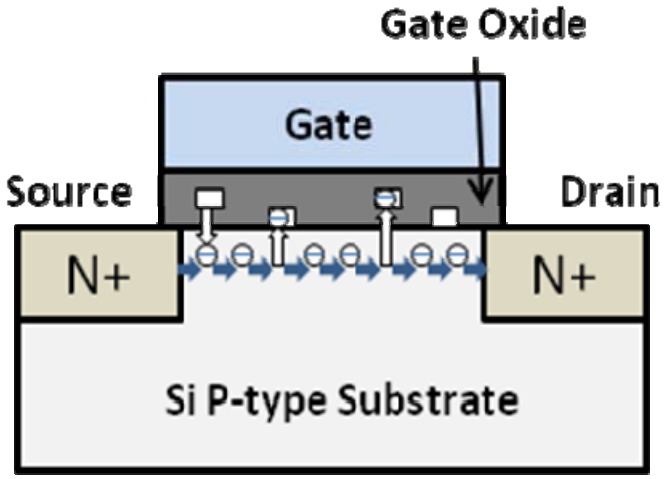

Figure 2.3: Schematic illustration of channel electrons in an nMOS trapping in and out of oxide traps, leading to fluctuations in the number of channel carriers and therefore the drain current.

2.2.1. The McWorther model

In McWorther's theory [33], the tunneling transition of carriers into and out of the gate-oxide traps is proposed as the exact mechanism behind the number fluctuations, and this theory has been widely recognized as one of the major principles for 1/*f* noise in MOSFETs.

The g-r noise S_{Qox} of the oxide charge density Q_{ox} generated by the random capture and emission of channel carriers by a single oxide trap can be written as

$$S_{Q_{OX}} = S_{V_{fb}} C_{OX}^2 = \frac{q^2}{W^2 L^2} 4 f(E)(1 - f(E)) \frac{\tau}{1 + (2\pi f \tau)^2} \tag{2.6}$$

where S_{Vfb} is the power spectral density of the fluctuations in the flatband voltage V_{fb}. $f(E)$ is the Fermi-Dirac distribution function and represents the probability that the trap at energy E is occupied

$$f(E) = \frac{1}{1 + \exp(\frac{E - E_F}{kT})}. \tag{2.7}$$

The total power spectral density of the fluctuations in the oxide charge density is found by summing over the contributions from all the active oxide traps [38], [40]:

$$S_{Q_{OX}} = \frac{q^2}{W^2 L^2} \int_{E_V}^{E_C} \int_0^W \int_0^L \int_0^{t_{OX}} 4 N_t f(E)(1 - f(E)) \frac{\tau}{1 + (2\pi f \tau)^2} dx dy dz dE \tag{2.8}$$

where $N_t = N_t(x, y, z, E)$ is the trap density per unit volume and unit energy. N_t is assumed to have a uniform spatial and energy distribution near the interface and the product $f(E)(1 - f(E)) = -kT\mathrm{d}f(E)/\mathrm{d}E$. Thus, we have

$$S_{Q_{OX}} = \frac{q^2 kT}{WL} \int_0^{t_{OX}} 4 N_t(E_F) \frac{\tau}{1 + (2\pi f \tau)^2} dz. \tag{2.9}$$

The product $f(E)(1 - f(E)) = -kT\mathrm{d}f(E)/\mathrm{d}E$ is sharply peaked around the quasi-Fermi level E_F; thus, only the trap density at E_F, i.e., $N_t(E_F)$, is considered. Other traps are either permanently filled or permanently empty. The tunneling transition time constant in the McWorther model is given as

$$\tau = \frac{1}{2\pi f} = \tau_t = \tau_o \exp(z / \lambda) \tag{2.10}$$

for an electron tunneling from the channel to a trap located at a distance z from the interface, as indicated in Figure 2.4(a). The time constant τ_o is often taken as 10^{-10} s. By assuming the rectangular barrier, the tunneling attenuation length λ predicted by the Wentzel-Kramers-Brillouin (WKB) approximation is given as [40]

$$\lambda = \left[\frac{4\pi}{h} \sqrt{2m^* \phi_B} \right]^{-1} \tag{2.11}$$

where Φ_B is the tunneling barrier height seen by the carriers in the channel and h is Planck's constant. $\lambda \approx 1$ Å for the Si/SiO_2 system. By substituting (2.10), the integral in (2.9) can be evaluated, and together with (2.6), the gate-voltage-referred noise spectral density S_{Vg} is derived as

$$S_{V_g} = S_{V_{fb}} = \frac{q^2 kT \lambda N_t}{f^\gamma WLC_{OX}^2}. \tag{2.12}$$

(2.12) predicts no explicit gate bias dependence of the $1/f$ noise in the linear region with quite a uniform channel-carrier distribution at low V_{ds} values. Based on (2.12), the density of the near-interface oxide-traps, N_t, can be derived from the measured $1/f$ noise magnitude. The variation of the frequency exponent γ can be explained by considering a nonuniform trap distribution. The exact $1/f$ spectrum with $\gamma = 1$ is only obtained when the trap density is uniformly distributed in the z direction. If the trap density increases as its position moves closer to the Si/SiO_2 interface, $\gamma < 1$ is expected; and $\gamma > 1$ is expected for the opposite case [32].

Strictly speaking, (2.12) is only valid above threshold, i.e., for $V_{gs} > V_T$. A more general expression derived in the number-fluctuation framework has been proposed by *Reimbold*, which is valid from weak to strong inversion at low V_{ds} values [34], [41]. The resulting normalized drain-current noise spectral density is given by

$$\frac{S_{I_d}}{I_d^2} = \frac{q^4 \lambda}{kTWL} \frac{1}{f^\gamma} \frac{N_t}{\left(C_{ox} + C_d + C_{it} - \beta Q_i\right)^2} \tag{2.13}$$

with $\beta = q/kT$, C_d the depletion capacitance per unit gate area, C_{it} the interface state capacitance per unit gate area, and Q_i the surface charge density of the inversion layer.

In weak inversion, the condition $|\beta Q_i| < C_{ox} + C_d + C_{it}$ can be assumed; thus, (2.13) gives a constant plateau for S_{Id}/I_d^2 at small values of I_d.

Equation (2.12) and (2.13) are derived from Equation (2.8) based on the assumption that the oxide trap density per unit volume per unit energy has a uniform spatial and energy distribution near the interface. The γ in the equation is to indicate the possible deviation of the slope from the exact 1 in real situation. As long as γ is within the range of 0.8~1.4, the noise is considered as generic 1/*f* noise.

In the McWhorter model, the distribution of tunneling times comes from the reduction of the tunneling time (see (2.10)) with distance z in the oxide. For the frequency range of interests and the measurement setup (1 Hz ~ 100 kHz), only traps within a certain distance from the interface will contribute. For a given frequency f, the depth of the oxide trap probed is based on a particular value of τ_o, and the value of τ_o reported in the literature is between 10^{-10} and 10^{-14} s. It can be calculated based on (2.10), even for the smallest probing frequency applied in this study, f = 1 Hz and the smallest value of τ_o reported, $\tau_o = 10^{-14}$ s, the depth of the oxide trap probed is not beyond 3 nm with respect to the Si/SiO_2 interface. However, to explain the 1/*f* noise in the subthreshold region, a variant of the original McWhorter model was proposed by Fu and Sah [35]. In that case, it is assumed that the free carriers interact with a fast interface trap, through thermal capture and emission at a rate of $\sim 10^6$ s^{-1}. Then the carrier trapped at the interface will be able to tunnel at constant energy to a near-interface oxide trap and subsequently tunnel back, which again results in drain-current fluctuations at low frequencies.

2.2.2. The thermal-activation model

Besides the McWorther tunneling model outlined above, the thermal-activation model [Figure 2.4(b)] with transition time constants exponentially depending on the trap activation energy E as [43]

$$\tau = \tau_{th} = \tau_o \exp(E / kT) \tag{2.14}$$

can also give rise to the $1/f^{\gamma}$ fluctuations with an appropriate distribution of the time constant τ_{th}. The exact $1/f$ spectrum with the frequency exponent $\gamma = 1$ is only obtained when the trap density is uniformly distributed in the activation energy E. If the trap density increases as the energy level E increases, $\gamma > 1$ is expected; and $\gamma < 1$ is expected for the opposite case. Experimental evidences of thermally-activated phonon-assisted capture and emission of channel carriers by oxide traps are shown in the RTS noise studies in MOSFETs [12], [14]. The discussion and application of the thermal-activation model is detailed in Chapter 4.

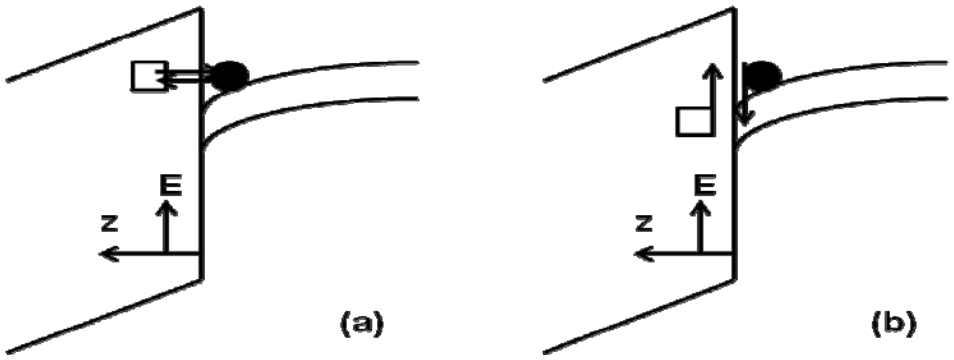

Figure 2.4: Schematic representation of two major number-fluctuation based $1/f$ noise models: (a) the classical tunneling model where the tunneling time decays exponentially with the trap depth from the interface; (b) the thermally activated oxide trap model where the tunneling time decays exponentially with the trap activation energy.

In the recent decade, the strong support for the number-fluctuation model comes from the behavior of RTS noise in submicron MOSFETs [44]–[48]. The relative amplitude of a drain-current RTS in the linear region by neglecting the possible impact of the mobility scattering can be expressed as [34], [47]

$$\frac{\Delta I_d}{I_d} = \frac{g_m}{I_d}\frac{q}{WLC_{ox}}\left(1-\frac{z}{t_{ox}}\right) \tag{2.15}$$

for an oxide trap at a distance z from the interface, with t_{ox} being the gate oxide thickness. A proportionality of $\Delta I_d/I_d$ with g_m/I_d can be easily seen from (2.15). Since g_m/I_d tends to be constant for small I_d values in weak inversion with $V_{gs} < V_T$, a constant value of $\Delta I_d/I_d$ is predicted from (2.15) as [34], [44], [46]

$$\frac{\Delta I_d}{I_d} = \frac{1}{WL}\frac{q^2/kT}{C_{ox}+C_d+C_{it}}\left(1-\frac{z}{t_{ox}}\right) \tag{2.16}$$

which is the counterpart of (2.13) derived by *Reimbold* for the 1/*f* noise in large-area MOSFETs.

2.3. Mobility fluctuation noise in MOSFETs

2.3.1. The Hooge noise model

The Hooge mobility-fluctuation model is purely empirical in nature and was first proposed to explain the 1/*f* noise in homogeneous semiconductors [18], [23]. According to Hooge's empirical formulation, the drain-current noise generated by carrier mobility fluctuations in the channel is given as

$$\frac{S_{I_d}}{I_d^2} = \frac{\alpha_H}{fN} = \frac{q\alpha_H}{fWLQ_i} \tag{2.17}$$

where the total number of channel carriers N is expressed as WLQ_i/q. The Hooge parameter α_H is often considered as a constant and the typical values of α_H range between 10^{-3} and 10^{-6} for silicon. The relationship in (2.17) is only valid when the carrier density is uniformly distributed along the channel.

If the drain-to-source voltage across the channel is very large, the carrier density is no longer uniform along the channel. Then the total drain-current noise is evaluated by integrating the noise contribution from each small segment of the channel over the entire channel, because the carrier density in each small channel segment can be assumed uniform:

$$\frac{S_{I_d}}{I_d^2} = \frac{q\alpha_H}{fWL^2}\int_0^L \frac{dx}{Q_i(x)} = \frac{q\alpha_H \mu V_{ds}}{fL^2 I_d} \tag{2.18}$$

where $I_d = W\mu Q_i(x)\mathrm{d}V(x)/\mathrm{d}x$.

In the subthreshold region, the drain current is dominated by the diffusion current expressed as

$$I_d = \frac{WkT\mu}{q}\frac{dQ_i(x)}{dx}. \tag{2.19}$$

Rearrange (2.19) and substitute it into the integral in (2.18), the same final expression of S_{Id}/I_d^2 is obtained. However, for $V_{ds} >> kT/q$ in the subthreshold region, the V_{ds} dependence of the drain current and the surface charge density Q_i is negligible. The final expression of S_{Id}/I_d^2, which is also independent of the V_{ds} value, is thus derived as [49]

$$\frac{S_{I_d}}{I_d^2} = \frac{2kT\alpha_H \mu}{fL^2 I_d}. \tag{2.20}$$

A common practice to determine the dominant LFN source in a MOSFET is to compare the plot of the measured normalized drain-current noise spectra S_{Id}/I_d^2 versus

drain current I_d in log-log scale with the plot of $(g_m/I_d)^2$ and $1/I_d$ versus I_d. As seen from (2.15), if the number-fluctuation mechanism is dominant, S_{Id}/I_d^2 will be parallel with $(g_m/I_d)^2$, whereas if the Hooge mobility-fluctuation mechanism is dominant, S_{Id}/I_d^2 will be parallel with $1/I_d$ as seen from (2.18) and (2.20). However, both mechanisms may fail to accurately describe the LFN characteristics over the entire operation regions.

2.3.2. Mobility fluctuations caused by the phonon scattering

The channel carrier mobility μ in a MOSFET is limited by different scattering mechanisms and has a strong dependence on the vertical electric field and the channel charge density. If each scattering process j is independent from one another, Matthiessen's rule can be applied as

$$\frac{1}{\mu} = \sum_j \frac{1}{\mu_j}. \tag{2.21}$$

The mobility fluctuation caused by each scattering process j is also assumed independent, with

$$\frac{\Delta\mu}{\mu^2} = \sum_j \frac{\Delta\mu_j}{\mu_j^2}. \tag{2.22}$$

Applying the Hooge mobility fluctuation formulation to each scattering process j with the corresponding Hooge parameter denoted as $\alpha_{H,j}$, the total normalized drain-current noise spectra can be expressed as

$$\frac{S_{I_d}}{I_d^2} = \frac{S_\mu}{\mu^2} = \sum_j \left(\frac{\mu}{\mu_j}\right)^2 \frac{S_{\mu_j}}{\mu_j^2} = \sum_j \left(\frac{\mu}{\mu_j}\right)^2 \frac{q\alpha_{H,j}}{fWLQ_i}. \tag{2.23}$$

Thus,

$$\alpha_H = \sum_j \frac{\mu^2}{\mu_j^2} \alpha_{H,j}. \tag{2.24}$$

The Hooge mobility-fluctuation dominant 1/*f* noise is suggested to be primarily due to the acoustic phonon (lattice) scattering that is always present, while other types of scattering (Coulombic, surface roughness scattering, etc.) suppress the 1/*f* noise at low frequencies [25], and (2.24) becomes

$$\alpha_H = \frac{\mu^2}{\mu_{ph}^2} \alpha_{H,ph} \tag{2.25}$$

with $\alpha_{H,\,ph}$ a constant ~2×10^{-3}, and μ_{ph} the mobility due to acoustic phonon (lattice) scattering only. Thus, in the mobility fluctuation noise model, the bias dependence of α_H can either be explained by the bias dependent factor $(\mu/\mu_{ph})^2$ influenced by other scattering mechanisms such as the surface roughness scattering, or by a non-constant $\alpha_{H,\,ph}$ assumed.

In MOSFETs, the number-fluctuation mechanism is still considered as the primary explanation for 1/*f* noise. The Hooge mobility-fluctuation noise model agrees better with the 1/*f* noise data in pMOS, whereas for 1/*f* noise data in nMOS, sometimes a gate-voltage dependence of Hooge parameter α_H must be assumed. A roll-off in the plot of S_{Id}/I_d^2 versus I_d is often observed when the transistor is biased in the subthreshold region. If Hooge's model is applicable, it is apparent from (2.18) and (2.20) that the Hooge parameter α_H must decrease with decreasing current in the subthreshold region. If we assume that the 1/*f* noise is due to mobility fluctuations caused by different scattering mechanisms and the phonon scattering is the dominant source, the decrease in α_H at decreasing subthreshold current may be explained by the stronger influence of the Coulombic scattering as the number of channel carriers

decreases, which dilutes the 1/*f* noise contribution from the phonon scattering as seen from (2.25).

An expression relating the Hooge parameter α_H to the phonon-phonon scattering rate was proposed by *Melkonyan et al.* as [31]

$$\alpha_H = \frac{K}{\tau_{ph-ph}} \tag{2.26}$$

where K is a constant and $1/\tau_{ph\text{-}ph}$ is the phonon-phonon scattering rate. The mobility-fluctuated 1/*f* noise is qualitatively explained to be due to random fluctuations in the phonon-electron scattering and in the electron distributions introduced by the random phonon-phonon scattering. The more significant the phonon-phonon scattering is, the shorter the mean free path of the phonon scattering will be, and in turn, the stronger the mobility fluctuation will be as seen from (2.26). The mean free path is very sensitive to lattice imperfections and defects [50]. The dominance of the phonon scattering in the generation of the mobility-fluctuation noise is experimentally evidenced by the relationship between the 1/*f* noise and the lattice quality of the crystalline. Increased 1/*f* noise level is observed in the presence of lattice defects created by ion irradiations, while after annealing the damaged material, the 1/*f* noise level is reduced [51]. A good material has a lower α_H value and thus corresponds to a lower 1/*f* noise, and vice versa. As such, the α_H-parameter and 1/*f* noise can be used to investigate the structural quality in a semiconductor technology.

2.3.3. Impact of the channel position on mobility fluctuations

The buried-channel field-effect transistors, such as the buried-channel Si MOSFETs [52]–[54] and the SOI four-gate transistors [55], often show significantly lower 1/*f* noise than that for the surface-channel transistors. Lower 1/*f* noise can be

obtained when the conduction channel is separated from any oxide interfaces, because the channel carriers are isolated from the Si/SiO_2 interface, and thus, the interactions between channel carriers and oxide traps are suppressed. Therefore, the $1/f$ noise generated by number fluctuations is excluded, and the $1/f$ noise observed in this case is believed to be caused by Hooge mobility fluctuations.

However, the Hooge parameter α_H that is sensitive to the crystalline quality is reported to be deteriorated close to the Si/SiO_2 interface. Hence, the higher $1/f$ noise observed for transistors with current transporting close to the Si/SiO_2 interface may also be explained by increased mobility fluctuations due to deteriorated crystal quality close to the Si/SiO_2 interface. Another origin of the variations in α_H is thought to be from the surface roughness scattering that takes over the role of the dominant mobility-fluctuation noise generation mechanism [37]. According to (2.24), in this case the following relationship for α_H can be expressed

$$\alpha_H = \mu^2 \left(\frac{\alpha_{H,sr}}{\mu_{sr}^2} + \frac{\alpha_{H,other}}{\mu_{other}^2} \right) \tag{2.27}$$

where μ_{sr} is the mobility limited by the surface roughness scattering, μ_{other} represents the mobility limited by scattering mechanisms other than the surface roughness scattering, and the constants $\alpha_{H,sr}$ and $\alpha_{H,other}$ are the Hooge parameters for the corresponding scattering processes. The carrier conducting distance from the Si/SiO_2 interface can be modified by the bias conditions. For example, a large negative bias applied to the p-type substrate of a bulk nMOS may push the carriers towards the gate oxide. If the surface roughness scattering is considered to be dominant for the mobility-fluctuated $1/f$ noise generation, the gate and substrate bias dependence as well as the channel position dependence of α_H could be explained.

2.4. Correlated mobility fluctuations in MOSFETs

The models described above can be categorized as "pure-number" or "pure-mobility" fluctuation theory. A universal 1/*f* noise theory for MOSFETs by combining the two effects is reviewed in this section. The study of RTS noise in small-area MOSFETs has greatly helped in understanding this combined effect [56], [57] and in developing the so-called correlated mobility fluctuation theory [38], [42], [58].

The mobility scattering relating to charged traps could play a role in generating low-frequency fluctuations as evidenced from RTS noise studies on small-area devices [56], [59]. The relative amplitude of RTS fluctuations by considering oxide-trap scattering on the mobility is given by [57]

$$\frac{\Delta I_d}{I_d} = \frac{1}{N}\left(1 \pm \alpha \mu q \frac{N}{WL}\right) \tag{2.28}$$

with α being a scattering parameter in Vs/C. The sign in the bracket depends on the trap nature. For a donor-type trap, it becomes neutral when occupied; therefore the mobility will increase and the minus-sign will be valid. For an acceptor-type trap, it becomes charged when occupied; therefore the Coulombic scattering will reduce the mobility and the plus-sign applies in (2.28). The basic concept of the correlated mobility fluctuation model is the same as that in (2.28). Besides the interaction of the oxide traps with the channel through carrier capture and emission, different scattering effects as the trap occupancy changes have also been taken in account. The change in the charge state of the scattering centre strongly affects its impact on the mobility and, in turn, the drain current.

The final expression of the drain-current noise power spectral density by including the correlated mobility scattering caused by oxide-trapped charges is derived by *Ghibaudo et al.* as [42]

$$S_{I_d} = S_{V_{fb}} \left(1 \pm \frac{\alpha \mu C_{OX} I_d}{g_m} \right)^2 g_m^2 . \tag{2.29}$$

The first term in the parentheses corresponds to the number fluctuations of channel carriers and the second term corresponds to the mobility fluctuations induced by the Coulombic scattering effect of the charges trapped in the gate oxide. The scattering parameter α can be negative or positive depending on whether the mobility increases or decreases due to the effect of trapped charges. The normalized drain-current noise spectral density expressed as S_{Id}/I_d^2 is often used in the LFN analysis, since S_{Id}/I_d^2 is inversely proportional to the signal-to-noise ratio. The equation (2.29) yields a satisfactory fit to the noise data of both n- and p-MOSFETs [60]. The resulting gate-voltage-referred noise spectral density becomes

$$S_{V_g} = S_{V_{fb}} \left[1 \pm \alpha \mu_0 C_{OX} \left(V_{gs} - V_T \right) \right]^2 \tag{2.30}$$

where $S_{Vg} = S_{Id}/g_m^2$ and S_{Vfb} is the flatband-voltage noise spectral density. For a small α, i.e., the influence of the oxide traps on the mobility is negligible, (2.30) can be reduced to the pure number-fluctuation model, as in (2.12).

However, the strength of the correlated mobility fluctuation modeled with the scattering parameter α is under debate in the literature. Normally, a constant α is used in the noise models to explain the bias dependence of the experimental noise data, but it is argued that the screening effect of the channel carriers should be taken into account. Instead of being a constant, α is expected to decrease with increasing inversion charge density due to the screening effect [39], [61], [62].

A model for α has been derived in the literature based on the existing mobility models as follows:

$$\alpha = -\frac{1}{\mu^2}\frac{\partial \mu}{\partial Q_{OX}} = \\ -\left(\frac{1}{\mu_{ac}^2}\frac{\partial \mu_{ac}}{\partial Q_i} + \frac{1}{\mu_{ph}^2}\frac{\partial \mu_{ph}}{\partial Q_i} + \frac{1}{\mu_{sr}^2}\frac{\partial \mu_{sr}}{\partial Q_i} + \frac{1}{\mu_{C,imp}^2}\frac{\partial \mu_{C,imp}}{\partial Q_i}\right)\frac{\partial Q_i}{\partial Q_{OX}} - \frac{1}{\mu_{C,OX}^2}\frac{\partial \mu_{C,OX}}{\partial Q_i}\frac{\partial Q_i}{\partial Q_{OX}} \tag{2.31}$$

where μ_{ac} is the mobility limited by surface acoustic phonon scattering, μ_{ph} the bulk phonon mobility, and the mobility influenced by Coulombic scattering is separated into two parts as $1/\mu_C = 1/\mu_{C,\,imp} + 1/\mu_{C,\,OX}$. $\mu_{C,\,imp}$ is the part caused by impurities and $\mu_{C,\,OX}$ is the part caused by charges in the oxide. The bulk phonon mobility μ_{ph} is independent of any changes in the inversion charge density Q_i and $\partial Q_i/\partial Q_{OX} = -1$ in strong inversion, which gives

$$\alpha = \frac{1}{\mu_{ac}^2}\frac{\partial \mu_{ac}}{\partial Q_i} + \frac{1}{\mu_{sr}^2}\frac{\partial \mu_{sr}}{\partial Q_i} + \frac{1}{\mu_{C,imp}^2}\frac{\partial \mu_{C,imp}}{\partial Q_i} + \frac{1}{\mu_{C,OX}^2}\frac{\partial \mu_{C,OX}}{\partial Q_i}. \tag{2.32}$$

The first three terms are often neglected in the derivation of α. The last term will be positive or negative depending on the trap type and the channel type. A simple model for $\mu_{C,\,OX}$ is given by [63] as $\mu_{C,\,OX} = 1/(\alpha_C|Q_{OX}|)$, where α_C is a Coulombic scattering parameter. In common practice, α is just set to be equal to α_C as a contant, but it is argued that in such a case the effect of the correlated mobility scattering is overestimated at high gate voltage overdrives, because the screening of the Coulombic interactions between oxide charges and inversion carrier charges becomes more and more effective as the inversion charge density increases with the gate voltage overdrive. Hence, by taking into account the decrease of α_C with increasing inversion charge density Q_i, several expressions of α_C have been proposed. One expression is derived by *Vandamme et al.* [39] as

$$\alpha = \alpha_C = \frac{1}{q\,\mu_{C0}\sqrt{C_{OX}\left(V_{gs} - V_T\right)/q}} \tag{2.33}$$

where μ_{C0} is a fitting parameter in the unit of cm/Vs. Another expression used for α_C [64] is

$$\alpha = \alpha_C = \alpha_0 - \alpha_1 \ln(N) \tag{2.34}$$

where α_0 and α_1 are fitting constants.

The McWorther model by adding the correlated mobility fluctuation term can explain almost all the experimental 1/*f* noise data for nMOS with gate bias sweeping from subthreshold to strong inversion. However, this is not the case for 1/*f* noise data observed in pMOS. The values of α extracted from the correlated mobility fluctuation model for explaining the 1/*f* noise data in pMOS were in the range of $1 \sim 2\times10^5$ Vs/C [16], [65], [66], which are too high to be supported by the laws of physics. If the screening effect as described above is considered, the correlated mobility fluctuation model may even fail to explain the observed 1/*f* noise characteristics in pMOS. In order to solve the deviation of the model equation from the experimental data in pMOS, the oxide trap density N_t in the McWorther model is assumed to vary with energy, which means N_t varies with the gate bias due to the band bending in the oxide. *Scofield et al.* claimed that the trap density is constant near the conduction band edge for explaining the 1/*f* noise data in nMOS, while the trap density increases with energy close to the valence band edge for explaining the 1/*f* noise data in pMOS [67]. Another more commonly used distribution of the trap density is the U-shaped distribution, which assumes the trap density increases close to both the valence and conduction band edges [68]–[70].

2.5. Chapter 2 conclusion

After more than 40 years of research, there is still no unique model for 1/*f* noise in MOSFETs. In the number-fluctuation theory, 1/*f* noise in MOSFETs is considered as a surface phenomenon relating directly to the quality of the gate oxide and the Si/SiO_2 interface. A good correlation of 1/*f* noise with the density of near-interface oxide traps (N_t) has been evidenced from many experimental observations. Most of these observations can be explained under the McWhorter model. Opposite to the number-fluctuation theory is the so-called mobility-fluctuation theory, in which the mobility fluctuations induced mainly by the lattice vibration is considered as the origin of the 1/*f* noise, especially in homogeneous semiconductors. This theory depends on the material quality and assumes a bulk origin in comparison with a surface origin in the number-fluctuation theory. A general consensus is growingly reached around the so-called correlated mobility fluctuation model, which considers trapping/detrapping of channel carries into/out of the oxide traps as the basic process, and the mobility fluctuation is induced through the Coulombic scattering of the trapped charges. For the study of RTS noise, through the LFN behaviors in both small- and large-area devices, RTS noise is believed to be one of the fundamental component of 1/*f* noise. Based on all the above, 1/*f* noise can be used as a diagnostic tool for the gate oxide and interface quality and an evaluation tool for a new technology node.

CHAPTER 3: Test Structure for Low-Frequency Noise Characterizations in CMOS Technologies

Low-frequency noise is an important parameter for analog and RF applications. For example, LFN in MOS devices is up-converted to oscillator phase noise, degrading the system performance [71]. One of the important IC design challenges is to minimize the noise contribution to the system, thus the accurate and timely LFN characterization and model development for semiconductor transistors are needed. However, performing meaningful LFN measurements for the study of system performance and for the model verification is always a difficult and complex task. Because the extremely low level of current fluctuations (down to ~1 pA) has to be measured, in the presence of a much stronger DC bias current as well as undesired disturbances from electronic equipments, great care must be taken to keep the background noise (BN) of the measurement system as low as possible. A lot of effort has been devoted to developing a measurement system characterized by a sufficient low level of BN [72]–[76].

3.1. Conventional low-frequency noise measurement setup

Figure 3.1 shows the block diagram of the measurement setup normally used in the LFN study of CMOS devices with an ideal SR570 low-noise current preamplifier. The whole noise measurement setup is used in a shielded room. An input-bias network

is connected to the gate terminal of the MOSFET to adjust the gate-voltage levels. The drain terminal of the MOSFET is directly connected to the SR570 low-noise current preamplifier. The weak noise current flowing through the drain terminal is then amplified. The amplifier also provides a voltage supply, which is used to bias the drain terminal. The final amplified low-frequency drain current noise is displayed in the HP35670A dynamic signal analyzer (DSA). The measurements are usually performed in the frequency domain by measuring the power spectral density with a spectrum analyzer in the DSA. If the random telegraph signal (RTS) noise is present, the time domain analysis (sometimes with the help of an oscilloscope) is a valuable tool.

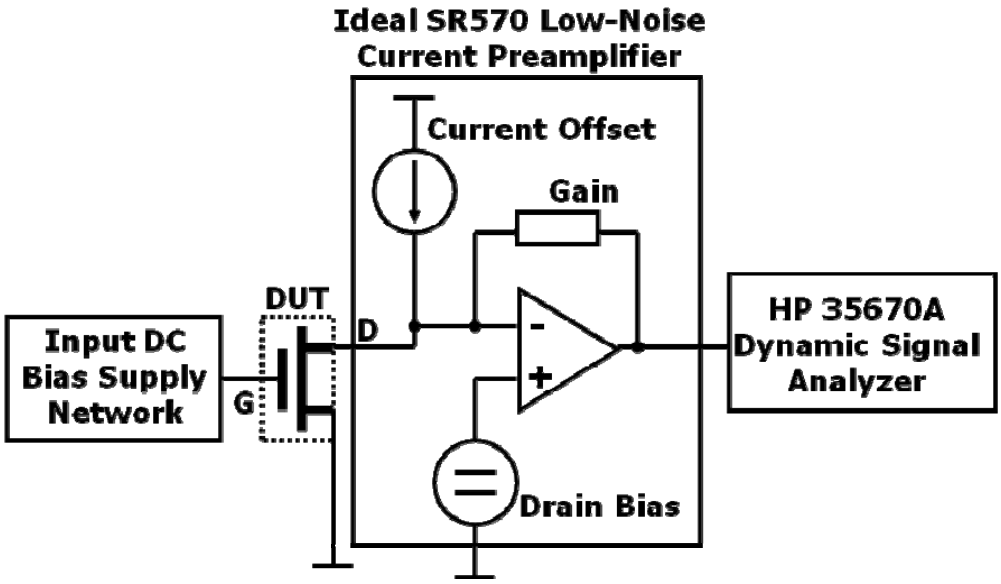

Figure 3.1: Low-frequency noise measurement setup with an ideal SR570 low-noise current preamplifier illustrated.

The internal structure of the SR570 current preamplifier shown in Figure 3.1 is an ideal one. A more practical one by including the relevant resistances is shown in Figure 3.2 below:

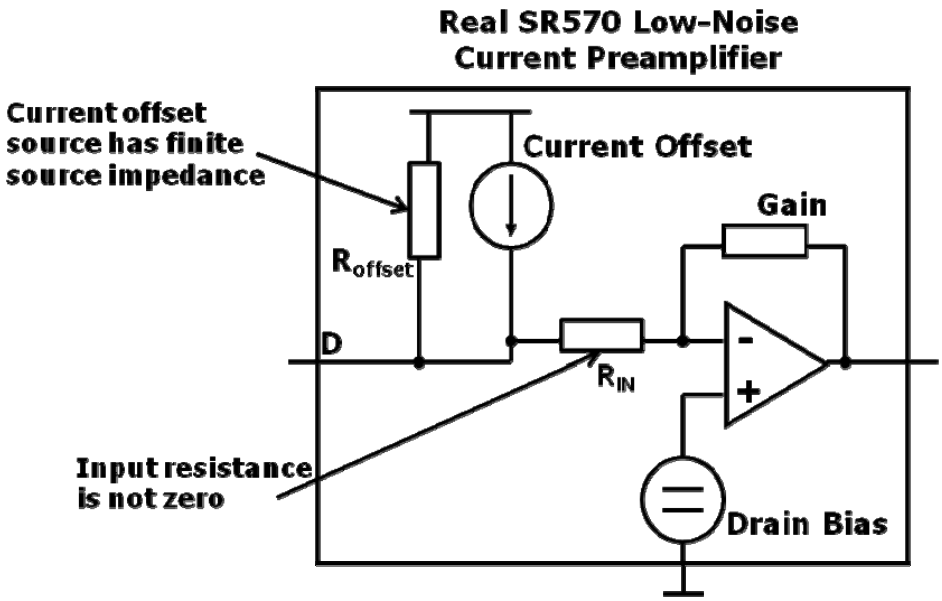

Figure 3.2: A more practical internal structure of an SR570 low-noise current preamplifier by including the relevant resistances.

The small-signal equivalent circuit of the input stage of SR570 current preamplifier can be drawn as in Figure 3.3.

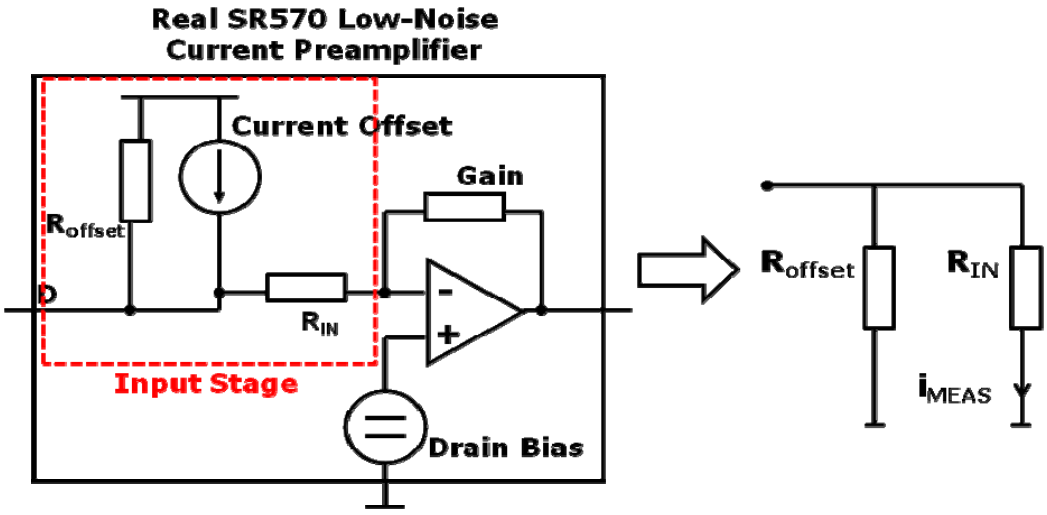

Figure 3.3: Small signal equivalent circuit of the input stage of SR570 Current Preamplifier.

Together with the small-signal equivalent circuit of the DUT, it is shown in Figure 3.4 that the measured drain-current noise i_{MEAS} is only a part of the real

intrinsic drain-current noise i_{noise}. g_{OUT} indicated in this figure is the output channel conductance, which is expressed as $g_{OUT} = \partial I_d/\partial V_{ds}$ with I_d the drain current and V_{ds} the potential difference across the channel of the MOSFET.

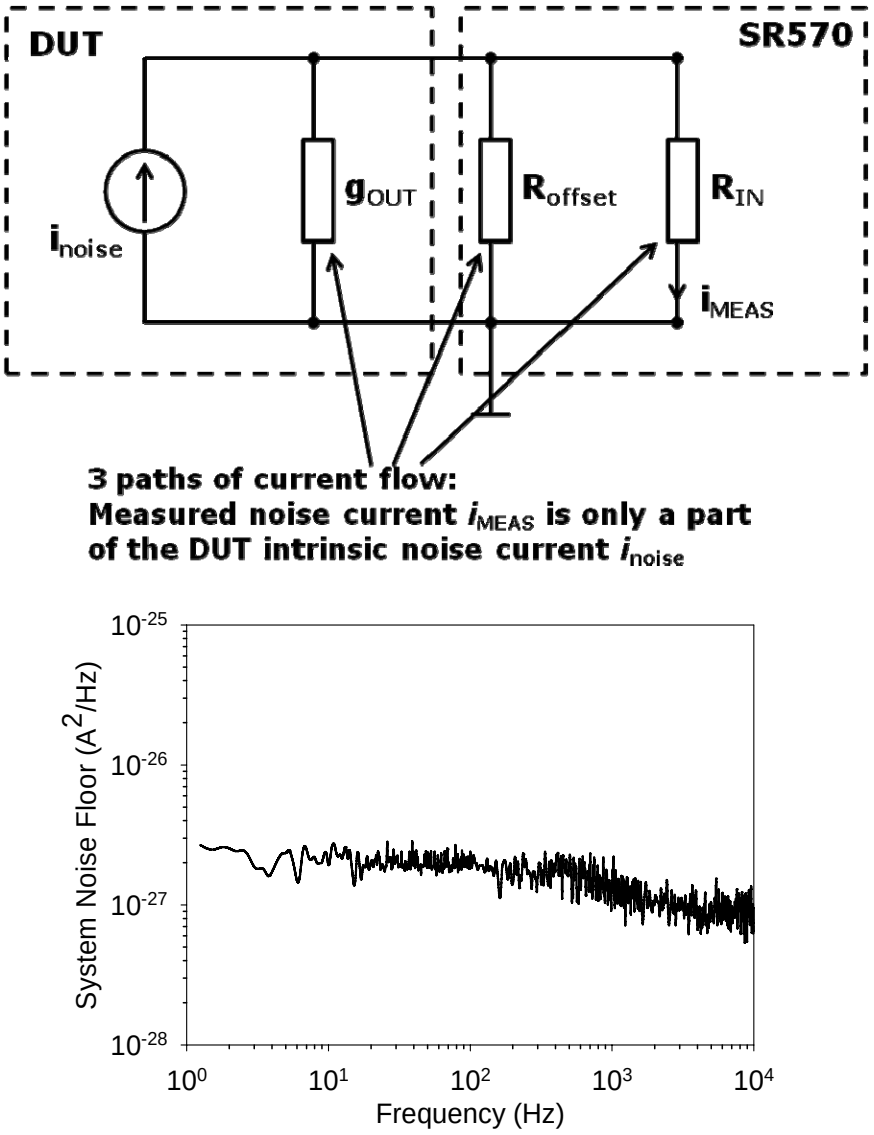

Figure 3.4: (a) Small signal equivalent circuits of the DUT and the SR570 Current Preamplifier. (b) System noise floor of the LFN measurement setup using SR570 Current Preamplifier.

From Figure 3.4(a), it is obvious that the mathematical relationship between the measured drain-current noise i_{MEAS} and the DUT intrinsic drain-current noise i_{noise} can be expressed as $i_{noise} = g_{TOTAL}(i_{MEAS}R_{IN})$, where $g_{TOTAL} = g_{OUT} + g_{offset} + g_{IN}$, $g_{offset} = 1/R_{offset}$ and $g_{IN} = 1/R_{IN}$. R_{offset} and R_{IN} are known from the settings of the

preamplifier during measurements. Since the input offset current is not needed in the present noise measurement, the connection between the drain side and the current offset source is switched off and the current path going through the impedance R_{offset} is open-circuited. In this case, $g_{TOTAL} = g_{IN} + g_{OUT}$. The input resistance R_{IN} is dependent on the sensitivity chosen during the noise measurement. For example, sensitivity = 100 nA/V used in the measurement corresponds to the input resistance R_{IN} = 10 kΩ, as stated in the manual of SR570 Current Preamplifier. In the LFN measurement of MOSFETs, the maximum output channel conductance g_{OUT} is normally two orders of magnitude smaller than g_{IN}. Hence, $g_{TOTAL} = g_{IN} + g_{OUT} \approx g_{IN}$, which leads to $i_{noise} \approx i_{MEAS}$. It means that the measured noise current can be treated approximately as the DUT intrinsic drain-current noise. One can always do a quick calculation of g_{OUT} through the DC measurement and g_{IN} through the manual of the preamplifier to get the exact and accurate intrinsic channel noise i_{noise}, especially in the case that the condition for the approximation of $i_{noise} \approx i_{MEAS}$ is not fulfilled in the devices measured. Moreover, the system noise floor measured with SR570 is around 2×10^{-27} A^2/Hz as shown in Figure 3.4(b), which is normally several orders smaller than the channel intrinsic drain-current noise and can be ignored. However, in the case that the channel intrinsic drain-current noise is comparable to the system noise floor, especially in the subthreshold region and high-frequency regime, this system noise floor should be subtracted from the measured noise current to get the intrinsic drain-current noise.

To avoid introducing additional noise sources while making LFN measurements, the power source for biasing the devices is a crucial part of any measurement system. Two major biasing schemes used as the “Input DC Bias Supply” in Figure 3.1 are battery and commercial solid-state power supply (e.g., SMU of Agilent 4142 or 4156 parameter analyzer) followed by a low-pass filter with cutoff

frequency less than 1 Hz (Figure 3.5) [72], [74]. Battery is one of the solutions for achieving such highly sensitive noise measurement system. However, the option for the available voltage level of battery is limited. Resistive voltage divider can be used to obtain those non-directly available voltages, but the resistors used in the voltage divider may introduce additional thermal noise and thus its resistance value cannot be too large [73]. For the commercial solid-state power supply, the filter eliminates the line noise within the frequency band of interest, i.e., above 1 Hz, from the power supply bias source in order to provide the cleanest possible bias. However, this may not ensure that low frequency interferences from the main power line, such as noise peaks at 50 Hz or 100 Hz, are completely blocked. The resistors and capacitors built inside the filter may introduce additional noise; therefore, appropriate types of resistors and good quality capacitors should be used to reduce the induced thermal and 1/*f* noise. In some other literature [75], a more sophisticatedly designed very low-noise programmable voltage source is reported. From the block diagram of this voltage source, it obviously showed that the realization of such ultralow-noise voltage source is not an easy task.

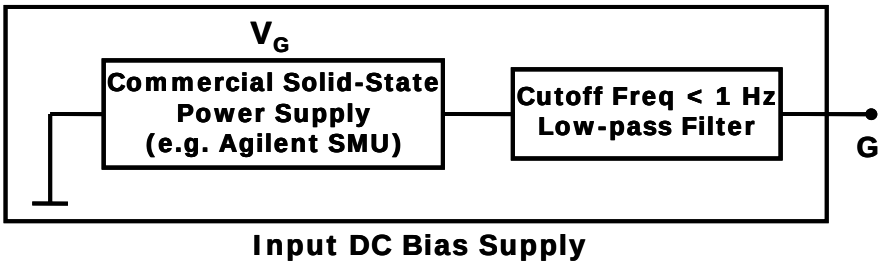

Figure 3.5: Input DC bias-supply network composed of one commercial power supply followed by one low-pass filter with cutoff frequency < 1 Hz [72], [74].

3.2. Proposed floating-gate test structure

The continuous improvement of technological processes makes available materials and devices characterized by fewer and fewer defects and, consequently, by

lower levels of excess noise. Moreover, as the devices continue scaling down, the situation in which a device contains no traps at all could happen. In such a case, the number-fluctuation related noise is thus eliminated with only the mobility-fluctuation related noise left, which obviously can lower down the LFN drastically [77]. Thus, the ratio of the intrinsic device noise to the given BN becomes smaller correspondingly, which may place challenges on the existing measurement setup in the future. Therefore, the BN of the measurement system used for the characterization of modern devices must be as small as possible. For CMOS devices, only a voltage reference is needed for the gate side, and no current supply is required. The power supply or battery supplying high current, which would introduce BN, is not necessary for the gate stage of MOSFETs. Hence in this chapter, a floating-gate (FG) test structure is proposed as a source of reference voltages for achieving the low-noise measurement system. The advantage of applying the FG test structure is due to the fact that no gate-bias networks are needed anymore during the low-frequency drain-current noise measurement, and thus, totally eliminating any noise contributions from the biasing circuitry. This concept can be applied to the low-noise circuit design, e.g., oscillator and mixer designs. It can also be easily extended to the LFN characterization of non-volatile memory (NVM) devices, because the NVM device itself has a FG structure.

3.2.1. Conceptual plot of the floating-gate test structure

Assuming LFN is to be measured in an nMOS transistor, the FG test structure can be fabricated as the nMOS transistor to be characterized with its poly-Si gate connecting to one metal side of the Metal-Insulator-Metal (MIM) capacitor, whereas the other metal side is working as the external control terminal with the applied voltage V_P. The poly-Si gate connecting to the metal side is now working as the FG.

The conceptual schematic of this test structure is shown in Figure 3.6. This test structure is easy to be fabricated, because there is an MIM capacitor option available in the standard CMOS process, the designers just need to choose the appropriate capacitor size. Even if the capacitor option is not available, this MIM capacitor can still be easily designed and fabricated by making use of the metal layers and the inter-metal-dielectrics (IMD) in the standard CMOS process. Moreover, this test structure takes up very small area of the wafer, same as that of a single transistor. For example, for a pad size of 30 μm × 30 μm, the total area of the test structure is around 90 μm × 90 μm, which is small enough to be put on the scribe line of the wafer without costing any effective wafer area.

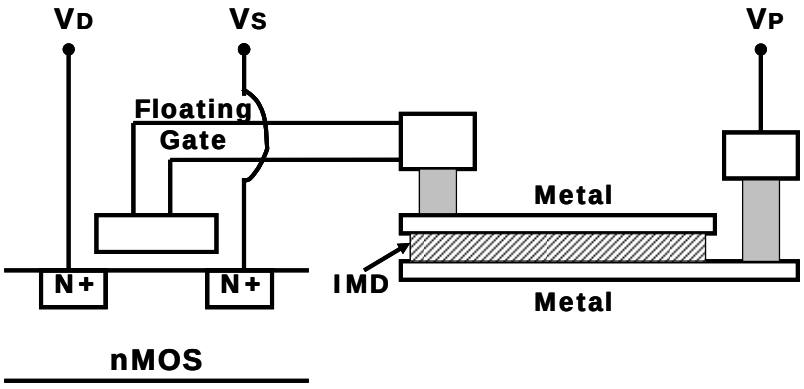

Figure 3.6: Conceptual schematic of the FG test structure by making use of the MIM capacitor.

3.2.2. Operation of the floating-gate test structure

The CHARGE operation is defined as the operation of putting electrons onto the FG, so that the voltage on the FG, i.e., the gate voltage of the nMOS transistor, will decrease; whereas the DISCHARGE operation is defined as the operation of removing electrons from the FG, so that the voltage on the FG will increase. Fowler–Nordheim (FN) tunneling between the gate and n+ diffusions of the nMOS transistor is used for CHARGE/DISCHARGE operations. In the CHARGE operation by FN tunneling

through the nMOS gate [Figure 3.7(a)], the drain and source sides of the nMOS transistor are grounded. A proper V_P is selected for electrons FN tunneling from n+ diffusions to the FG. In the DISCHARGE operation by FN tunneling through the nMOS gate [Figure 3.7(b)], V_P is grounded, the drain and source sides of the nMOS transistor are connected to the same positive voltage V_{DD}. The electric field for FN tunneling is now across the nMOS gate oxide for electrons being removed from the FG back to the n+ diffusions.

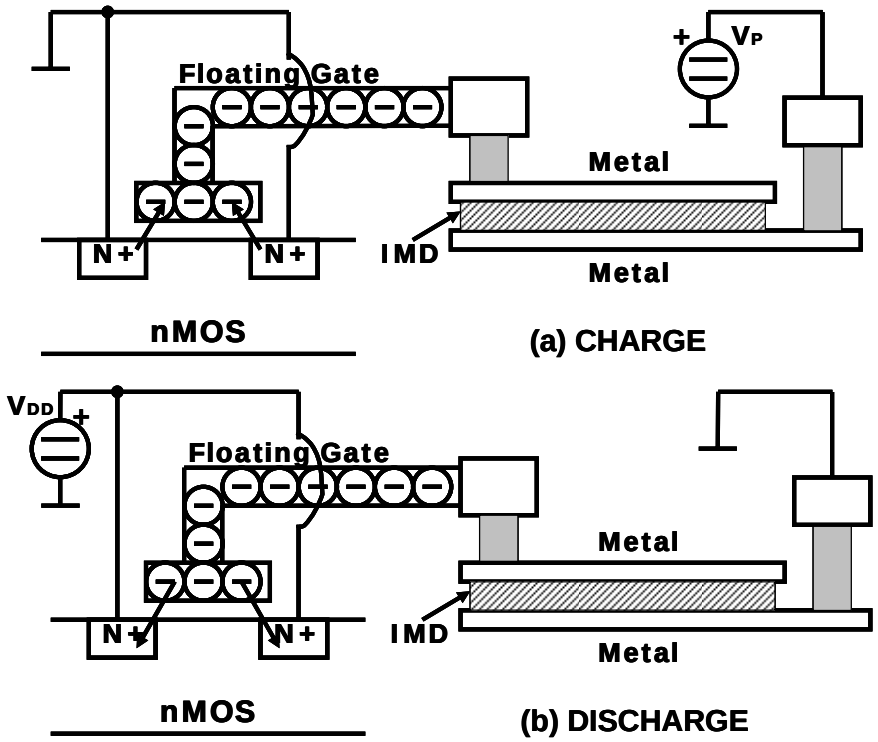

Figure 3.7: (a) CHARGE operation by FN tunneling from n^+ diffusions to the floating gate. (b) DISCHARGE operation by FN tunneling from the floating gate to n^+ diffusions.

It is suggested to have an estimate of the applied voltage level V_P (or V_{DD} in the DISCHARGE case), because blindly applying a very high voltage level may cause unwanted stress of the gate oxide and introduce extra noise. For a given V_P, the voltage V_{nn} across the gate oxide of the nMOS transistor can be approximated by [78], [79]

$$V_{nn} = \frac{C_{MIM}}{C_T} V_p + \frac{Q_{FG}}{C_T} \approx \frac{C_{MIM}}{C_T} V_p \tag{3.1}$$

where $C_T = C_{MIM} + C_n$ is the total FG capacitance, C_{MIM} the capacitance of the MIM capacitor, C_n the gate oxide capacitance of the nMOS transistor, and Q_{FG} the charges on the FG.

There is a voltage level V_{FN} across the gate oxide of the MOSFET required for FN tunneling to occur. For FN tunneling to occur in the nMOS transistor, V_{nn} has to reach V_{FN}, thus, the voltage V_p applied at the external control terminal should be approximated as

$$V_{nn} \approx \frac{C_{MIM}}{C_T} V_p = V_{FN} \tag{3.2}$$

which gives

$$V_p = \frac{C_T}{C_{MIM}} V_{FN} \approx \frac{C_T}{C_{MIM}} \left(E_{ox} \times t_{ox} \right) \approx \frac{C_T}{C_{MIM}} V_{ox}. \tag{3.3}$$

The condition for FN tunneling to happen is that the voltage drop across the gate oxide of the field-effect transistor, V_{ox}, is higher than 3.2 V, which corresponds to the band conduction offset between Si and SiO_2. Hence, V_{FN} can be chosen to be slightly above 3.2 V. The terminal voltage V_P applied by the user of this test structure should be close to the value predicted by (3.3). Moreover, for effective FG CHARGE/DISCHARGE, the most portion of the potential difference V_P should be across the nMOS gate rather than the MIM capacitor; therefore, from (3.3), C_T/C_{MIM} should be close to 1 and $C_{MIM} >> C_n$ is suggested in the designed test structure. Besides the voltage levels, to avoid any unwanted stress, the operation time of either CHARGE or DISCHARGE cycle should be as small as possible, and the operation time around 1 ms per cycle is suggested [80], [81]. Using medium voltage levels and multi-cycling with very short operation time per cycle is also easy for the user to control and adjust the device to the

desired input-current level for noise measurements without over-charging or over-discharging.

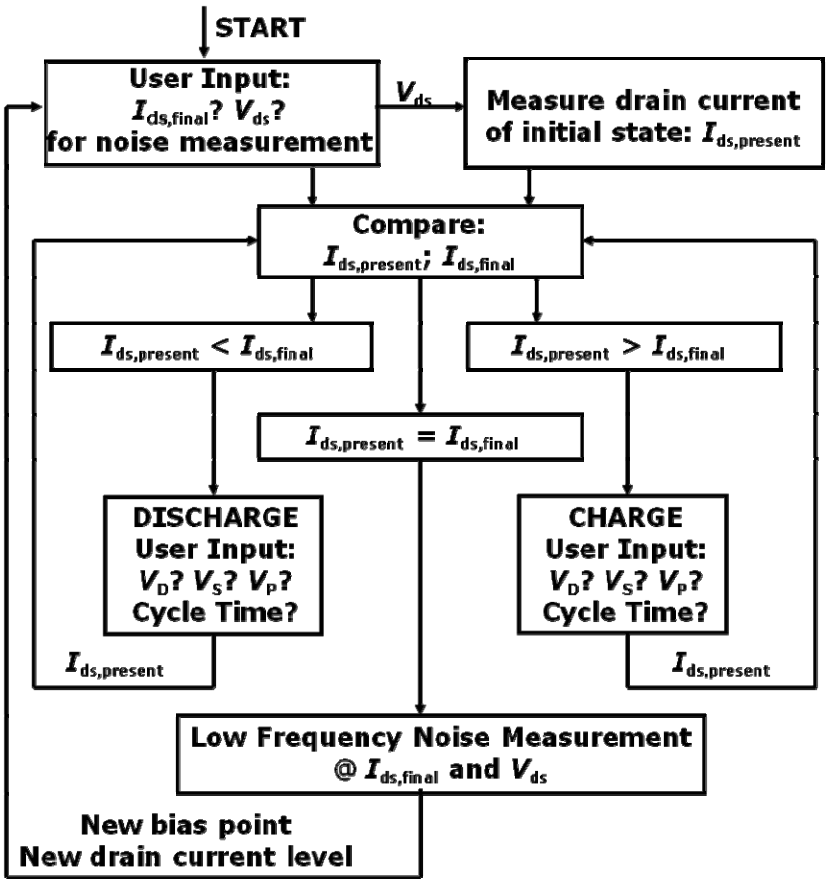

Figure 3.8: Program flow for LFN measurements.

A program is written to control the whole CHARGE/DISCHARGE process. The desired drain voltage V_{ds} and drain-current level $I_{ds,final}$ during noise measurements are first input by the user. Since the amount of electron charges on the nMOS gate (i.e., the FG) is different for different devices at the start of the measurement, the drain current $I_{ds,present}$ of the nMOS transistor under the "present state" at the given V_{ds} is measured by the HP 4156C parameter analyzer, and is compared with the current level input by the user. If $I_{ds,present} < I_{ds,final}$, DISCHARGE operation is chosen, since electrons on the FG need to be removed to increase the nMOS gate voltage. The DISCHARGE operation is cycled until the drain-current level is increased to the

desired drain-current level $I_{ds,final}$. If $I_{ds,present} > I_{ds,final}$, CHARGE operation is chosen to inject more electrons onto the FG, which leads to a lower gate voltage of the nMOS transistor and, again, the CHARGE operation is cycled until the drain-current level decreases to the desired $I_{ds,final}$. The voltages (V_D, V_S, V_P) applied to the three terminals of the test structure for CHARGE/DISCHARGE operations and the operation time of each CHARGE/DISCHARGE cycle can be input by the user. Finally, all the input-bias supply at the gate terminal is disconnected temporarily and the LFN measurement is done at the desired drain-current level. The detailed program flow is shown in Figure 3.8, and the program is iterated with the proper time interval for LFN measurements at multiple drain-current levels.

3.2.3. The other possible buildup of the floating-gate test structure

Instead of using the MIM capacitor, another FG test structure could also be built up by using a transistor of opposite type to the transistor to be characterized. For example, if the LFN is to be measured in an nMOS transistor, the test structure consisting of this nMOS transistor, together with a pMOS transistor connected by a common gate could be fabricated as shown in Figure 3.9. The shared common gate works as the FG, while the n-well of the pMOS transistor and its p^+ diffusions are connected together to work as the external terminal with the applied voltage V_P.

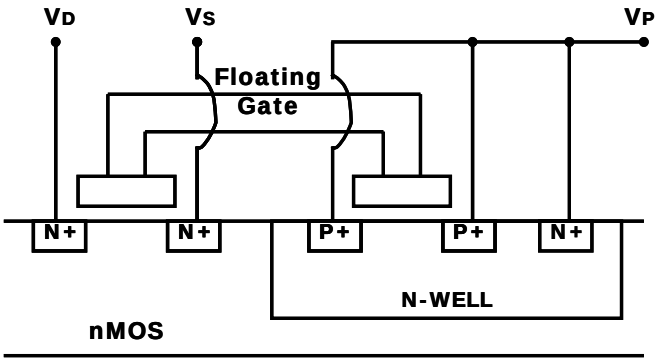

Figure 3.9: Conceptual plot of the FG test structure built up by a pMOS transistor connected to an nMOS transistor to be characterized by the shared common gate.

Similar to the case of MIM capacitor, for efficient CHARGE/DISCHARGE operations as shown in Figure 3.10, the gate oxide capacitance of the pMOS, C_P, should be much larger than the gate oxide capacitance of the nMOS, C_n, i.e., $C_P >> C_n$. This can be achieved either by larger gate area of the pMOS than that of the nMOS, or by thinner gate oxide of the pMOS than that of the nMOS. The former one is preferred, because thinner gate oxide may cause leakage problems. In the CHARGE operations, the drain and source sides of the nMOS transistor are grounded. A proper V_P approximated from (3.3) is selected for sufficient voltage to cause electrons FN tunneling from n+ diffusions to the FG. In the DISCHARGE operations, V_P is grounded, the drain and source sides of the nMOS transistor are connected to the same positive voltage V_{DD}. The high electric field across the nMOS gate oxide is for electrons FN tunnelling from the FG back to the n+ diffusions.

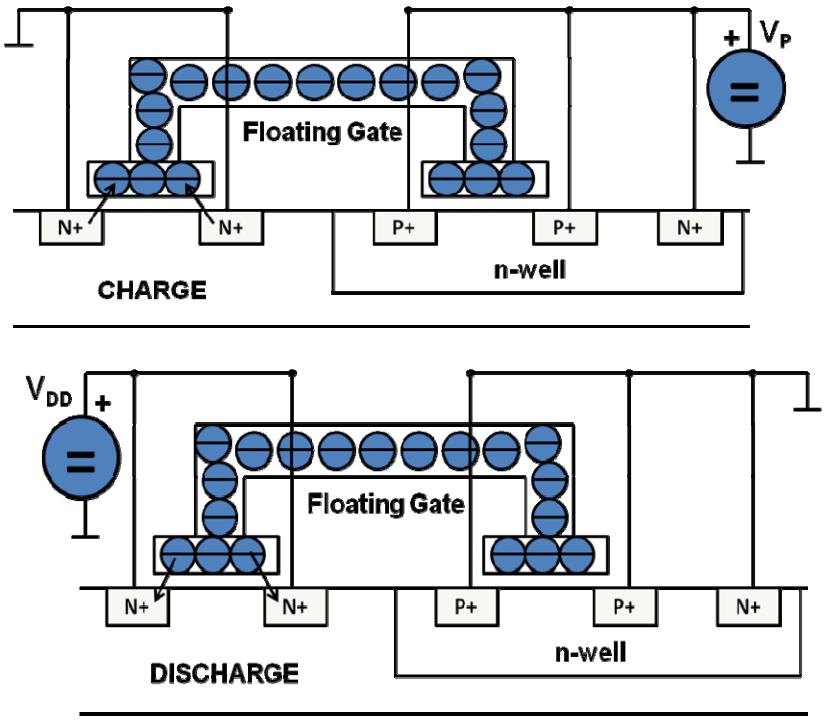

Figure 3.10: With $C_p >> C_n$, CHARGE/ DISCHARGE operation is done by FN tunneling between n+ diffusions and the floating gate.

3.2.4. Advantages of the floating-gate test structure

In summary, by using the FG test structure for LFN measurements, the gate voltage of the nMOS transistor is adjusted by injecting or removing electrons on the FG. In this setup, the device can be driven into the relevant current levels in advance before noise measurements, and the charges are maintained on the FG during noise measurements without the need for any extra input-bias supply for the gate stage in the experiment setup. The external voltage source in [76] makes use of the similar concept as that of the on-wafer FG test structure. An input capacitor is first charged by a biasing voltage, and then the switch that connects the biasing voltage to the capacitor is opened. Because of the virtual ground between the input pins of the operational amplifiers (Op-Amp), the gate voltage almost coincides with the voltage maintained by the input capacitor at the non-inverting input of the Op-Amp. It means that the Op-Amp is always present during the LFN measurement. As noticed by the author of [76], the use of Op-Amp may cause a voltage drift, e. g., the TLC071 input Op-Amp used is characterized by a typical input bias current below 2 pA and, therefore, a voltage drift at the output below 1 mV/hour. This is only acceptable for noise measurements lasting a few minutes at most and for devices with large intrinsic LFN, so that a large tolerance of the BN is allowed. Although various practices have been carried out for minimizing the noise introduced from the input supply at the gate stage, with the proposed FG test structure, such kind of noise is completely excluded. Moreover, in the implementation of the conventional LFN measurement setup, the ground path from the drain output to the gate input is extended by the cable lengths as illustrated in Figure 3.11(a). This ground loop, which acts as an antenna, may pick up parasitic noise of the environment and make the measured intrinsic device noise unreliable. Hence, the cable connections should be as short as possible to minimize the antenna

effects. By using the proposed FG test structure, the potential ground loop is only limited to the output pole, because the gate input pole is left floating and not playing any part in the LFN measurements. The path of the potential ground loop is thus reduced and the antenna effect is in turn reduced, as illustrated in Figure 3.11(b). Hence, the FG test structure gives contributions to achieve low level of BN for accurate LFN measurements.

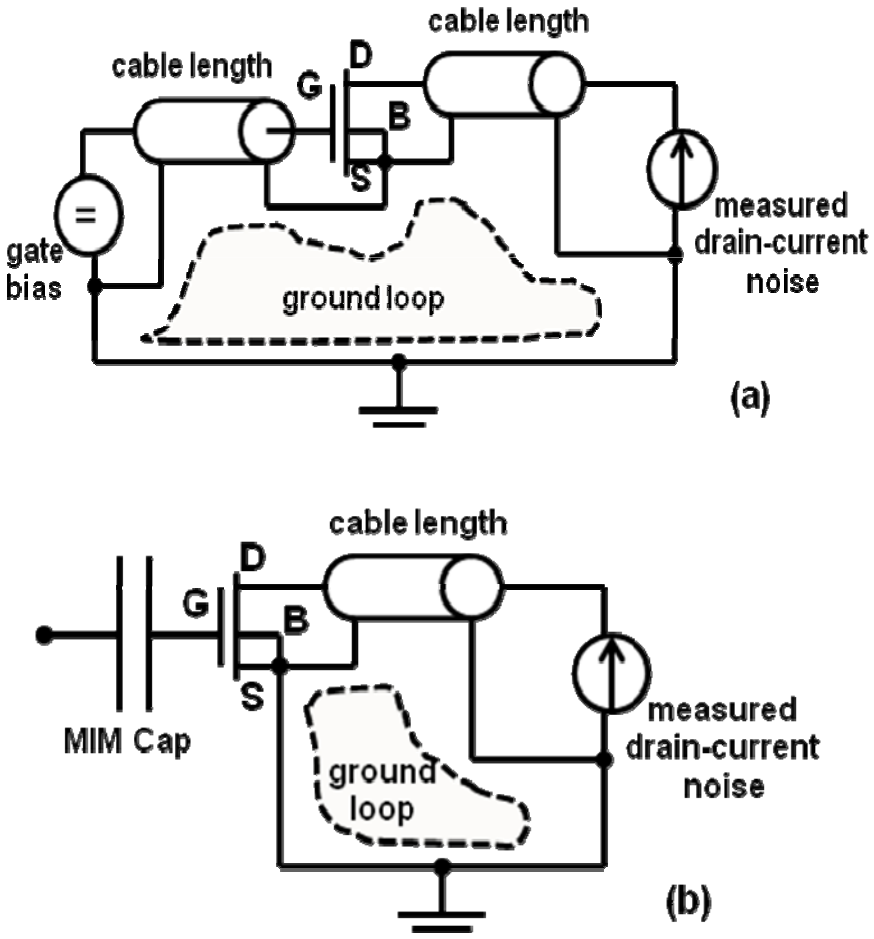

Figure 3.11: Illustrations of the potential ground loop in the (a) conventional LFN measurement schematic; (b) LFN measurement schematic using the FG test structure.

3.3. Testing the feasibility of the floating-gate test structure

3.3.1. Testing conditions

A set of measurements has been performed for testing the applicability of the FG test structure in the LFN measurement with program-controlled CHARGE/ DISCHARGE cycles for gate-voltage adjustments. The devices used in this study are nMOS transistors fabricated by 0.18-μm standard CMOS process with W = 4 μm and L = 0.35 μm for 1/f noise measurements, and W = 1 μm and L = 0.18 μm for Random Telegraph Signal (RTS) noise measurements. For the 0.35-μm and 0.18-μm nMOS transistors, the FG test structures are built by the nMOS transistors with their poly-Si gates connecting to the metal sides of the 31.5-fF and 4.5-fF MIM capacitors in the respective cases.

The LFN in the respective device is first measured by the classical measurement setup in Figure 3.1 to act as a reference. Then the LFN measurement is performed by the FG approach. The bias condition for the CHARGE operation by FN tunneling through the nMOS gate is: $V_S = V_D = 0$ V for the nMOS transistor, and V_P = 4.5 V; while that for the DISCHARGE operation is: $V_S = V_D = V_{DD} = 4.5$ V for the nMOS transistor, and $V_P = 0$ V. The operation time for each CHARGE or DISCHARGE cycle is set to 0.7 ms. $V_p = 4.5$ V is chosen according to (3.3), with C_T /$C_{MIM} \approx 3.7/2.7$, $t_{ox} = 3.9$ nm, and assuming $E_{ox} \approx 8.5$ MV/cm. The calculated V_{nn} is around 3.3 V.

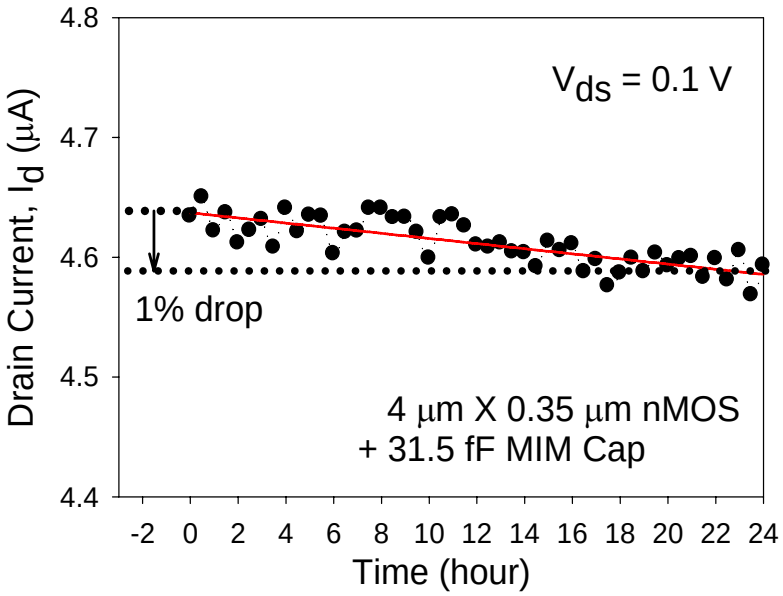

Figure 3.12: Retention capability of the FG test structure. I_d at V_{ds} = 0.1 V has only 1% drop from its initial value after 24 hours.

To ensure that the gate bias does not change due to the charge leakage from the FG during the LFN measurement, the retention capability of the test structure with the 4-μm×0.35-μm nMOS transistor connected to the 31.5-fF MIM capacitor has been tested. The nMOS transistor has initially been driven to $I_d \approx 4.6$ μA at $V_{ds} = 0.1$ V with the CHARGE/DISCHARGE method, then the gate is left floating. For LFN measurements by the 35670A DSA, the lowest measurable frequency is 195.3125 mHz, which takes the maximum measurement time of 8.19 ks, which is around 2.3 hours. It is shown in Figure 3.12 that the drain-current level has only one-percent drop after 24 hours, which is trivial. Hence even for LFN measurements at lowest measurable frequency and maximum measurement time, the retention capability of the bias capacitor is good enough to keep the gate bias constant.

3.3.2. Testing results

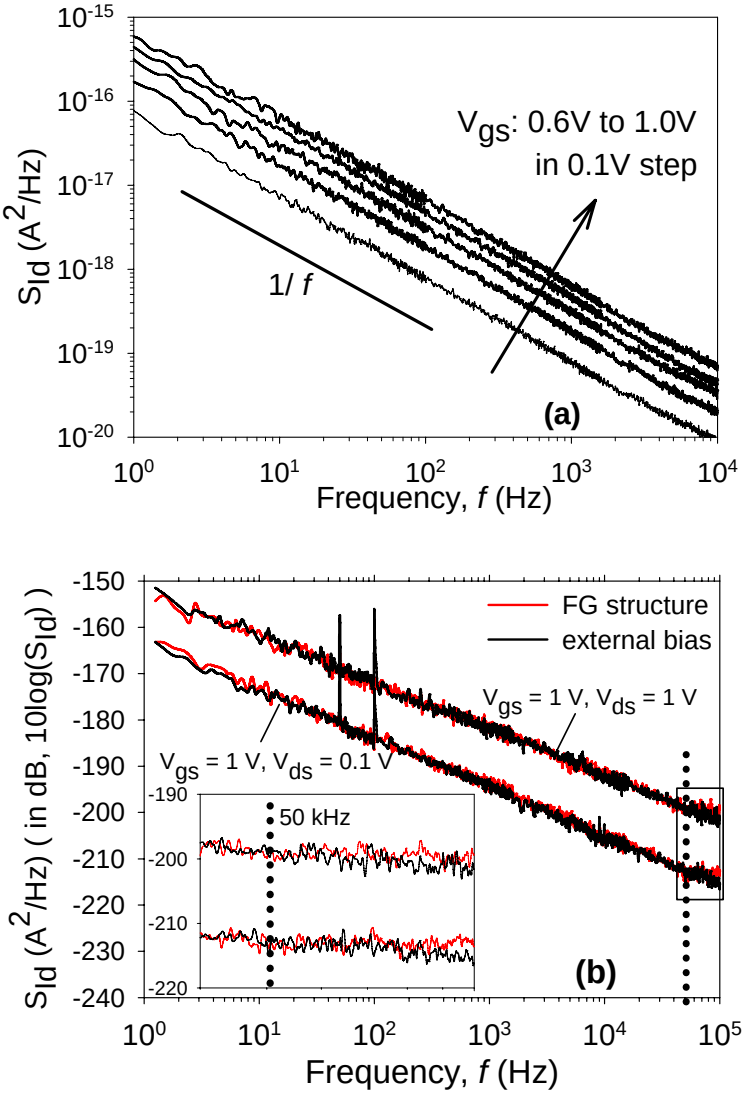

Figure 3.13: (a) Drain-current noise power spectral density in the nMOS transistor with W = 4 µm and L = 0.35 µm. Gate voltage is CHARGE/DISCHARGE from 0.6 V to 1.0 V in a 0.1 V step and V_{ds} = 1 V. (b) Comparison of S_{Id} spectrums measured at V_{gs} = 1 V and V_{ds} = 0.1 and 1 V by the FG test structure and conventional LFN measurement setup respectively. The inset shows the zoom-in plot of S_{Id} vs. f from 4×10^4 to 10^5 Hz. The thermal noise floor is observed only beyond 50 kHz for the device measured by the FG test structure.

For the 0.35-µm nMOS transistor, the drain-current noise power spectral densities S_{Id} at V_{ds} = 1 V and with gate voltage V_{gs} being CHARGE/DISCHARGE from 0.6 V to 1.0 V in a 0.1 V step are reported in Figure 3.13(a). A typical $1/f^{\gamma}$ behavior with γ close to 1 is observed. As stated in [82], [83], a capacitor of

capacitance C under open-circuit conditions has a thermal voltage fluctuation v_n, whose mean square value at a temperature T is $\langle v_n^2 \rangle = kT/C$. Thus, the open-circuited FG in this test structure during noise measurements may have this thermal fluctuations present, named as interface-induced thermal noise (IITN), with $C = (1/C_{MIM} + 1/C_n)^{-1}$. The additional drain-current noise S_{Id_add} introduced due to this FG IITN has a Lorentzian spectrum with a cutoff frequency $f_o = 1/(2\pi RC)$, because such a spectrum is the thermal noise of C having some resistance R in parallel. Let us do an approximate calculation of the IITN at low V_{ds}. The power spectral density in the flat part of the IITN Lorentzian spectrum ($f << f_o$) is $S_{vn} = (kT/C)/[(\pi/2)f_o]$ [82], thus $S_{Id\_add} = g_m^2 \times S_{vn} = (g_m^2)(kT/C)/[(\pi/2)f_o]$. For $C \approx 8.8$ fF, R on the order of 10^8 Ω, and the transconductance g_m on the order of 10^{-5} A/V of the studied device at room temperature, S_{Id_add} is on the order of 10^{-22} A^2/Hz and $f_o \approx 100$ kHz. S_{Id} spectrums measured at both low V_{ds} ($V_{ds} = 0.1$ V) and high V_{ds} ($V_{ds} = 1$ V) by the FG test structure and conventional setup with the external bias are compared in Figure 3.13(b). The noise curves measured by two different methods are almost overlapped in the entire frequency range, except that the S_{Id} curves of the device biased with the external voltage source have spikes at 50 and 100 Hz, which are interferences from the main power line. From the zoom-in plot of Figure 3.13(b) from $f = 40 \sim 100$ kHz as shown in the inset, at frequencies beyond 50 kHz, there is a thermal noise floor of the device measured by the FG test structure. As seen from the noise curve at $V_{ds} = 0.1$ V, the magnitude of the thermal noise and the frequency range where it becomes observable is consistent with the above calculation. **This is the first experimental demonstration in the MOS technology of the predictions in [82].** It can be seen that the effect of IITN on the LFN characterization is negligible, because the frequency range where it becomes observable is beyond the low frequency regime of interests.

This is why quite a pure 1/*f* noise spectrum of drain current covering more than four decades of frequency can be clearly obtained for the 4-μm × 0.35-μm large-area transistor, and as the device area reduces, a clear RTS noise signal without being covered up by the thermal noise will be observed, which will be shown below.

For the 0.18-μm nMOS transistor, the RTS noise signals are observed and collected at different drain-current levels at V_{ds} = 0.1 V, four of which are reported in Figure 3.14(a). Figure 3.14(b) shows a frequency histogram of the capture time τ_c and emission time τ_e from a particular data set at V_{gs} = 0.58 V and V_{ds} = 0.1 V. The data fit very well to an exponential distribution ~ $\exp(-\tau_{c,e}/\langle\tau_{c,e}\rangle)$, where $\langle\tau_c\rangle$ and $\langle\tau_e\rangle$ are the average capture and emission times, respectively, which indicates that the switching times correspond to a Poisson random process [13]. Hence, $\langle\tau_c\rangle$ and $\langle\tau_e\rangle$ can be extracted by fitting the measurement data to this exponential distribution at different bias points. $\langle\tau_c\rangle$, $\langle\tau_e\rangle$, and their ratios at the corresponding gate voltages are shown in Figure 3.14(c).

The measured 1/*f* and RTS noise in the respective devices with the gate bias adjusted by the FG CHARGE/DISCHARGE operations are the same as those initially measured by the conventional setup and used as the reference data for comparison, which proves the feasibility of this FG test structure. And this test structure provides a way of terminal biasing from a different angle.

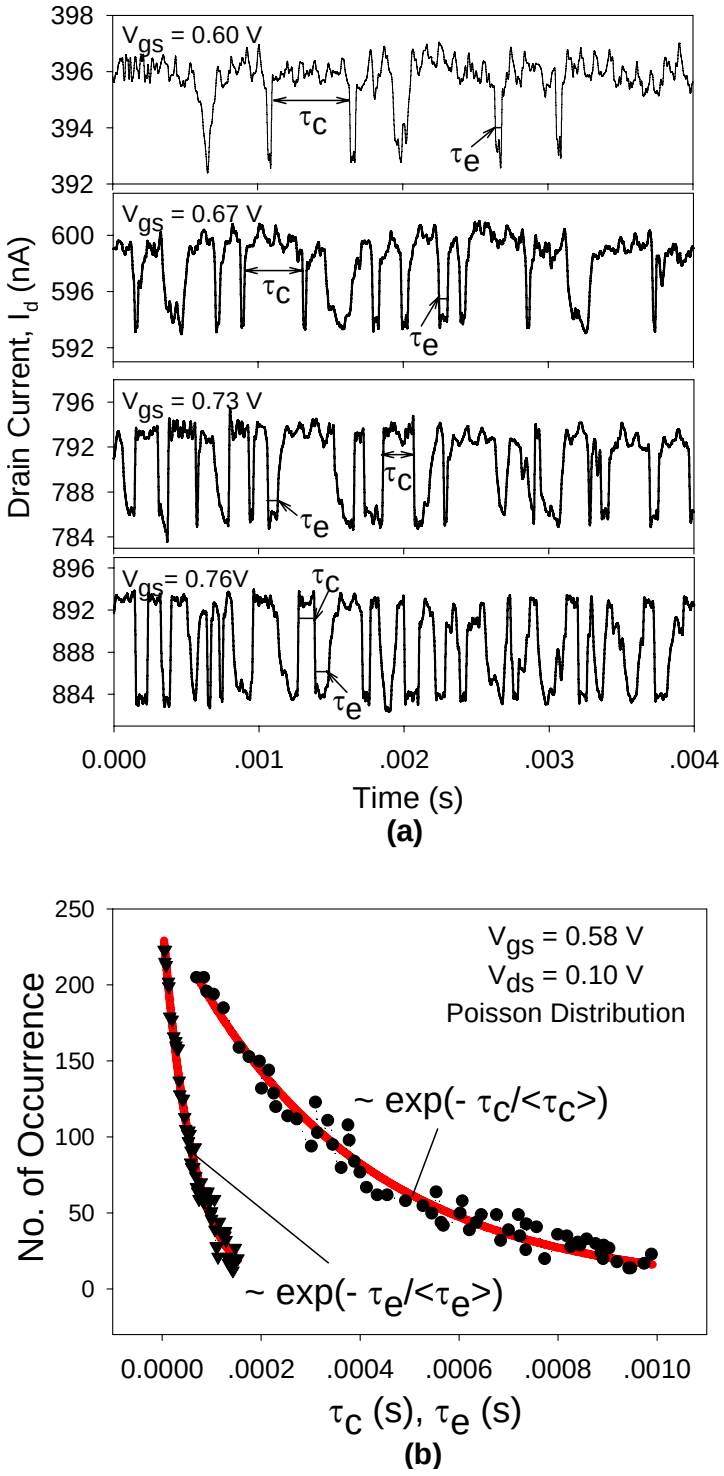

Figure 3.14: (a) RTS noise signals at four different drain-current levels of the nMOS transistor with W = 1 µm and L = 0.18 µm at V_{ds} = 0.1 V. (b) Frequency histogram of the switching times τ_c and τ_e corresponding to V_{gs} = 0.58 V and V_{ds} = 0.1 V. The lines are best fits with ~exp(–$\tau_{c,e}$/<$\tau_{c,e}$>).

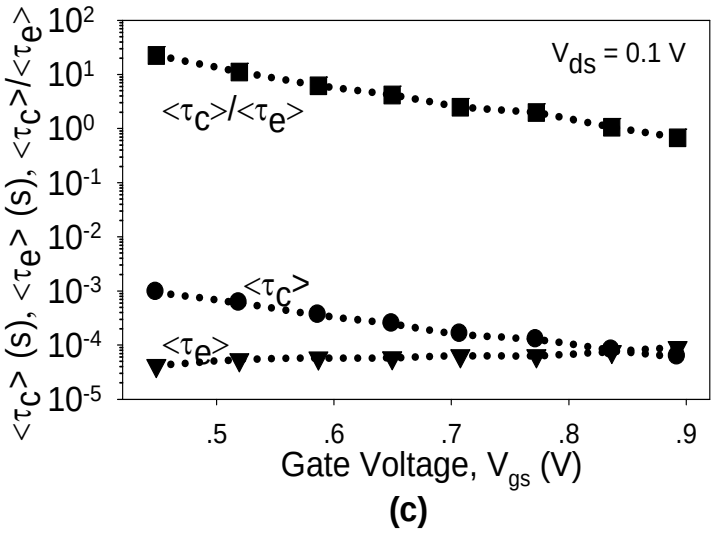

Figure 3.14 (cont.): (c) Average capture time $<\tau_c>$, average emission time $<\tau_e>$, and the mark-space ratio $<\tau_c>/<\tau_e>$ against V_{gs}: ● for $<\tau_c>$, ▼for $<\tau_e>$, and ■ for $<\tau_c>/<\tau_e>$.

3.4. Chapter 3 conclusion

In this chapter, a FG test structure for LFN measurements in CMOS devices has been presented. The guidelines for implementing the proposed test structure with a detailed program flow have been provided. The structure applicability has been tested through measurements of the nMOS transistors fabricated by 0.18-μm CMOS process and it shows that the proposed test structure works well for LFN such as 1/*f* and RTS noise measurements.

The noise measurement using the proposed FG test structure has rendered the need for elaborately designed input bias supply for the gate stage of MOSFETs unnecessary, and it demonstrates an alternative thinking for biasing the devices compared to the use of various conventional designs for the input-bias stage. No input-bias stage is needed during noise measurements and, thus, any noise introduced from the input-bias stage is totally excluded. At the same time, the whole noise measurement process for multiple biases is also programmable.

CHAPTER 4: **Low-Frequency Noise in N-Channel FinFETs from Weak to Strong Inversion**

Due to its better gate control, the double-gate (DG) FinFET is considered an important candidate for future CMOS scaling beyond the 32-nm node, with advantages of the improved drive current and better control of short-channel effects [84]–[86]. FinFET devices have been reported demonstrating the feasibility as well as the great interest for analog applications in both static and dynamic regimes up to the radio frequency [87]–[89]. However, low-frequency noise (LFN), which is an important parameter for analog and RF applications, becomes more pronounced with technology downscaling. In analog applications, LFN minimization is a key issue and often defines the sensitivity or detection limit, while in the microwave community, LFN may be up-converted to the phase noise in oscillators and mixers, degrading the system performance [90], [71]. In addition, LFN measurement offers a useful characterization method for the dielectric quality estimation and lifetime prediction due to its nondestructive and highly sensitive properties [91].

Since the current in transistors is proportional to the product of the mobility μ and the number of channel carriers N, low-frequency fluctuations occurred in the carrier transport are caused by stochastic changes in either of these two parameters. Originally, it was thought that $1/f$ noise in transistors is a surface phenomenon associated with the capture and emission of channel carriers by localized traps at or near the Si/SiO_2 interface, which falls under the number-fluctuation (ΔN) theory. A $1/f$

noise spectrum has been shown resulting from the superposition of thermally-activated processes with a distribution of activation energies [20], or from tunneling processes with a distribution of tunneling distances [33]. Opposite to the ΔN model is the so-called $\Delta\mu$ picture, which considers the mobility fluctuation as the origin of the $1/f$ noise, and for homogeneous semiconductors, it assumes a volume and not a surface origin [18], [23]. The $1/f$ noise is believed to be strongly influenced by the lattice scattering due to different lattice qualities of different materials.

In this chapter, the LFN of n-channel FinFETs is characterized from weak to strong inversion at low drain bias. The bias dependence of LFN is presented, and the noise sources are discussed in two regions of operation, respectively. The gate-voltage dependence of the $1/f$ noise in weak inversion is consistent with the mobility-fluctuation model, whereas in strong inversion it is consistent with the number-fluctuation model. However, the slope of the frequency dependence of the noise magnitude (γ in $1/f^{\gamma}$) in strong inversion is far less than 1. Therefore, the temperature dependence of $1/f^{\gamma}$ in strong inversion is examined to further confirm the origin of LFN. The thermally-activated process is found convincingly to be responsible for the number-fluctuation-induced LFN in the strong-inversion linear region. The salient point of this chapter is a demonstration of the possible transition from carrier-number fluctuations to Hooge mobility fluctuations as the conducting channel is moved from the surface towards the whole silicon volume of the FinFETs.

4.1. Device and dc measurement

The n-channel FinFET was fabricated on an 8" silicon-on-insulator (SOI) substrate composed of a 120-nm thick (100) Si film with a boron doping of 10^{15} cm^{-3}

on top of a 150-nm buried oxide. As a hard mask for the definition of a Si fin, 60 nm of SiO_2 was deposited. After patterning using the 248-nm lithography and plasma etching, a fin of ~40 nm in width was obtained (i.e. fin width t_{si} = 40 nm). The hard mask was retained for the protection of the fin in the subsequent gate-etch process. A 2-nm sacrificial oxide was then grown on the fin sidewalls to repair the damage caused by the plasma etching. Following its removal, a 4-nm SiO_2 was used as the gate dielectric before depositing a 130-nm amorphous silicon (α-Si) as the gate electrode. After gate pattering and etching, the source/drain and α-Si gate were implanted using arsenic with a dose of 4×10^{15} cm^{-2} and energy of 30 keV for n-FETs. It was followed by the standard metal contact formation and sintering processes. Figure 4.1(a) shows a schematic of the DG FinFET device with important dimensions indicated.

Prior to noise analyses, the FinFET dc characteristics were measured using an HP4156C Semiconductor Parameter Analyzer. The $I_d - V_{gs}$ characteristics of n-FinFETs with L_{mask} = 0.5 μm, H_{fin} = 0.12 μm at V_{ds} = 50 mV is shown in Figure 4.1(b). The electrical parameters (threshold voltage V_T, low-field mobility μ_0, mobility-degradation parameter θ, channel-length reduction ΔL, sum of access resistances R_{acc}, and subthreshold slope S) important for the noise-parameter extraction can be obtained using a set of transfer characteristics ($I_d - V_{gs}$) at low drain voltage V_{ds} = 50 mV on devices with various gate geometries [92].

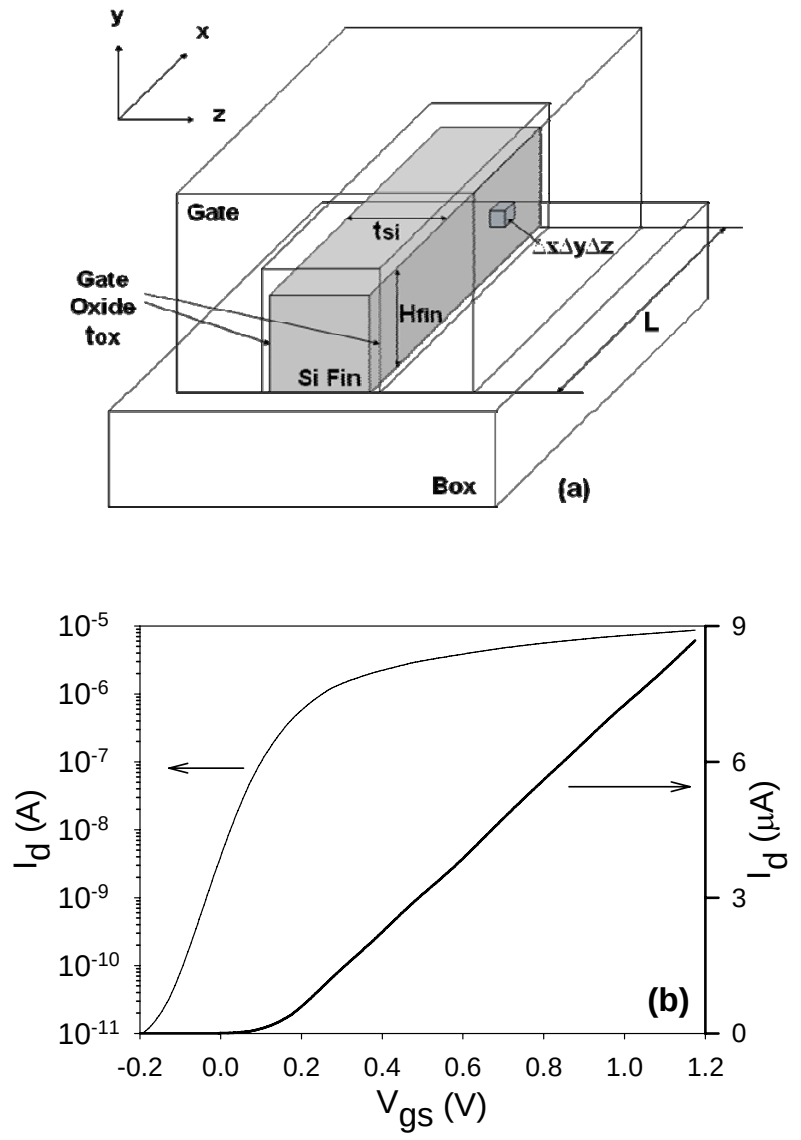

Figure 4.1: (a) Schematic of a FinFET device, showing important dimensions: fin width (t_{si}), fin height (H_{fin}), and gate length (L). (b) I_d - V_{gs} characteristics of the n-FinFET with H_{fin} = 0.12 µm and L = 0.35 µm at V_{ds} = 50 mV.

A first-order approximation of the drain-current expression for the electrical-parameter extraction of a DG n-FinFET can be borrowed from the drain-current expression of a bulk nMOS with $W = 2H_{fin}$. By taking into account the effective channel length, the effect of the series resistances R_S and R_D at the source and drain contacts and the variation of the mobility with the gate voltage overdrive ($V_{gs} - V_T$). The drain current can be expressed as

$$I_d = \mu C_{OX} \frac{W}{L}\left[\left(V_{gs} - V_T\right)V_{ds,eff} - \frac{1}{2}V_{ds,eff}^2\right] \tag{4.1}$$

with

$$\mu = \frac{\mu_0}{1+\theta\left(V_{gs} - V_T\right)} \tag{4.2}$$

$$L = L_{mask} - \Delta L \tag{4.3}$$

$$V_{ds,eff} = V_{ds} - I_d(R_S + R_D). \tag{4.4}$$

The term $V_{ds,eff}{}^2/2$ can be ignored for $V_{gs} - V_T >> V_{ds,eff}/2$ and the voltage drop I_dR_S with respect to $(V_{gs} - V_T)$ has been ignored, because the study for the electrical-parameter extraction has been done above threshold. Then (4.1) can be rearranged as

$$I_d = \mu_0 C_{OX} \frac{W}{L}\frac{\left(V_{gs} - V_T\right)V_{ds}}{1+\theta^*\left(V_{gs} - V_T\right)} \tag{4.5}$$

where

$$\theta^* = \theta + \mu_0 C_{OX} \frac{W}{L}\left(R_S + R_D\right). \tag{4.6}$$

From (4.5), the device transconductance $g_m = \partial I_d/\partial V_{gs}$ can be obtained as

$$g_m = \mu_0 C_{OX} \frac{W}{L}\frac{V_{ds}}{\left[1+\theta^*\left(V_{gs} - V_T\right)\right]^2}. \tag{4.7}$$

From (4.5) and (4.7), it is obtained that

$$\frac{I_d}{\sqrt{g_m}} = \sqrt{\mu_0 C_{OX} \frac{W}{L} V_{ds}}\left(V_{gs} - V_T\right). \tag{4.8}$$

Hence, the threshold voltage V_T can be extracted from the plot of $I_d / \sqrt{g_m}$ versus V_{gs} as shown in Figure 4.2(a). The slope of the straight line gives $\mu_0 C_{OX} W/L$ for each gate

length L_{mask}. For a constant W value, the plot of $1/(\mu_0 C_{OX} W/L) = (L_{mask} - \Delta L)/(\mu_0 C_{OX} W)$ versus L_{mask} gives μ_0 and ΔL as shown in Figure 4.2(b). Following (4.7), $1/\sqrt{g_m}$ can be expressed as

$$\frac{1}{\sqrt{g_m}} = \frac{1}{\sqrt{\mu_0 C_{OX} \frac{W}{L} V_{ds}}} + \frac{\theta^* \left(V_{gs} - V_T\right)}{\sqrt{\mu_0 C_{OX} \frac{W}{L} V_{ds}}}. \tag{4.9}$$

The plot of $1/\sqrt{g_m}$ versus V_{gs} leads to the determinations of $\sqrt{V_{ds} \mu_0 C_{OX} W / L}$ and θ^* for each gate length L_{mask}. Then from (4.6), for a constant value of W, the plot of θ^* versus $\mu_0 C_{OX} W/L$ gives θ and $R_{acc} = R_S + R_D$, as shown in Figure 4.2(c).

The reciprocal of the slope of the $\log_{10}(I_d)$ versus V_{gs} characteristics below the threshold voltage is defined as the subthreshold slope S:

$$S = \frac{dV_{gs}}{d\left(\log_{10} I_d\right)} = 2.3\left[\frac{dV_{gs}}{d\left(\ln I_d\right)}\right](V / decade). \tag{4.10}$$

Hence, the subthreshold slope S is extracted to be around 60 mV/dec from the log plot (left y-axis) of I_d versus V_{gs} below V_T in Figure 4.1(b). The extracted electrical parameters (V_T, μ_0, θ, ΔL, R_{acc}, and S) are listed in Table 1.

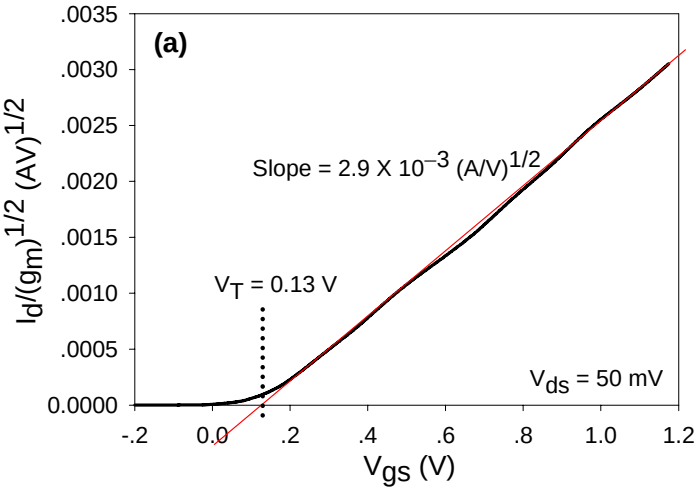

Figure 4.2: (a) Variation of $I_d/(g_m)^{1/2}$ with V_{gs} leading to $V_T = 0.13$ V and $\mu_0 C_{OX} W/L = 1.67\times10^{-4}$ A/V^2.

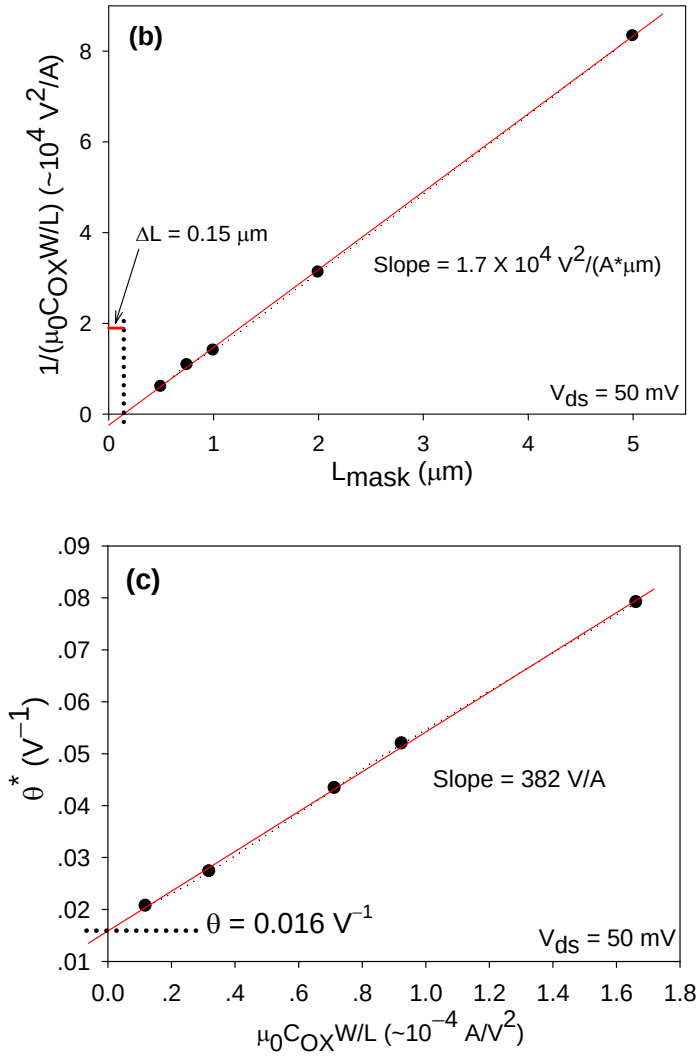

Figure 4.2 (cont.): (b) Evolution of $1/(\mu_0 C_{OX} W/L)$ as a function of L_{mask} giving μ_0 = 281 cm^2/Vs and ΔL = 0.15 µm. (c) Plot of θ^* versus $(\mu_0 C_{OX} W/L)$ giving θ = 0.016 V^{-1} and R_{acc} = 382 Ω.

Table 1: Conduction parameters extracted at V_{ds} = 50 mV for device dimensions: H_{fin} = 0.12 µm, L = 0.35 µm.

V_T (V)	μ_0 (cm^2/Vs)	ΔL (µm)	θ (V^{-1})	R_{acc} (Ω)	S (mV/dec)
0.13	281	0.15	0.016	382	60

Figure 4.3 plots the simulated one-dimensional electron density as a function of the position across the silicon fin along the middle of channel length and fin height for the symmetric DG FinFET at three different gate voltages to clarify the operation. For the case of V_{gs} = 0.05 (n_1) and 0.1 V (n_2), the device operates in the weak inversion subthreshold region. The electron concentration distributes almost uniformly across the silicon fin between two Si/SiO_2 interfaces, and starts to increase at these two interfaces when V_{gs} approaching the threshold voltage (n_2). For the case of V_{gs} = 0.9 V (n_3), the device operates in the strong-inversion linear region. The electron concentration increases, with its peak being located close to the two Si/SiO_2 interfaces.

In this work, ten samples of the same size were tested, and the bias dependence of the magnitude of the noise spectra is basically the same among all the devices studied. In strong inversion, in order to prove the applicability of the Dutta–Horn model [17], the representative results for two nominal devices, "Device 1" and "Device 2", are both shown in this chapter.

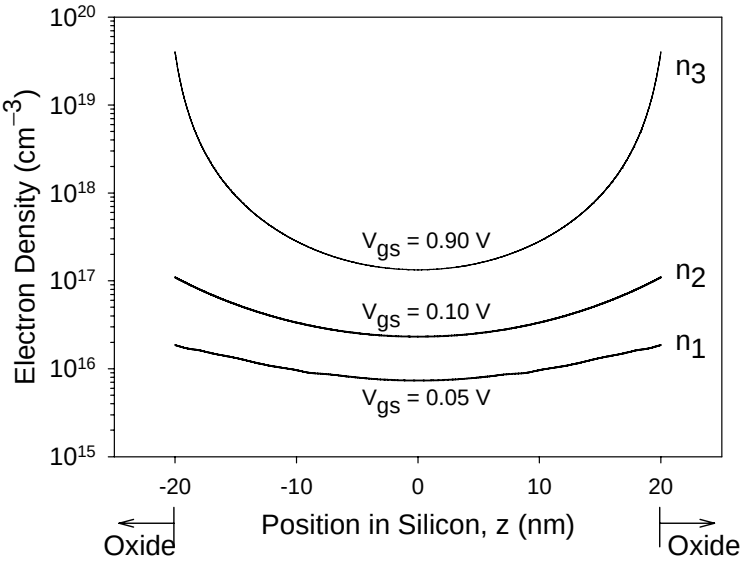

Figure 4.3: Simulated electron density as a function of the position across the silicon fin from one gate to the other gate (cutline is along the middle of channel length and fin height) for a symmetric DG FinFET at three different gate voltages. Weak inversion (n_1): V_{gs} = 0.05 V, Weak inversion (around threshold, n_2): V_{gs} = 0.1 V, Strong inversion (n_3): V_{gs} = 0.9 V.

4.2. Low-frequency noise in the weak-inversion subthreshold region

4.2.1. Measurement results and discussion

Figure 4.4 shows the typical normalized drain-current noise spectral density S_{Id}/I_d^2 at f = 10 Hz as a function of the drain current I_d when sweeping the gate voltage V_{gs} from weak to strong inversion while keeping V_{ds} constant at 50 mV for n-type FinFETs. In the weak-inversion subthreshold region, the variations of the normalized drain-current noise S_{Id}/I_d^2 vs. I_d exhibit a slope close to –1, a large slope deviation between S_{Id}/I_d^2 and $(g_m/I_d)^2$ (g_m is the transconductance, $\partial I_d/\partial V_{gs}$) is observed. If the $1/f$ noise is due to the carrier-number fluctuations, a quadratic variations of S_{Id} vs. I_d should have been observed, and the proportional correlation between S_{Id}/I_d^2 and $(g_m/I_d)^2$ should be obtained [42]. The –1 slope of the $\log(S_{Id}/I_d^2)$ vs. $\log(I_d)$ plot shows that the mobility-fluctuation model is involved in the weak-inversion subthreshold region.

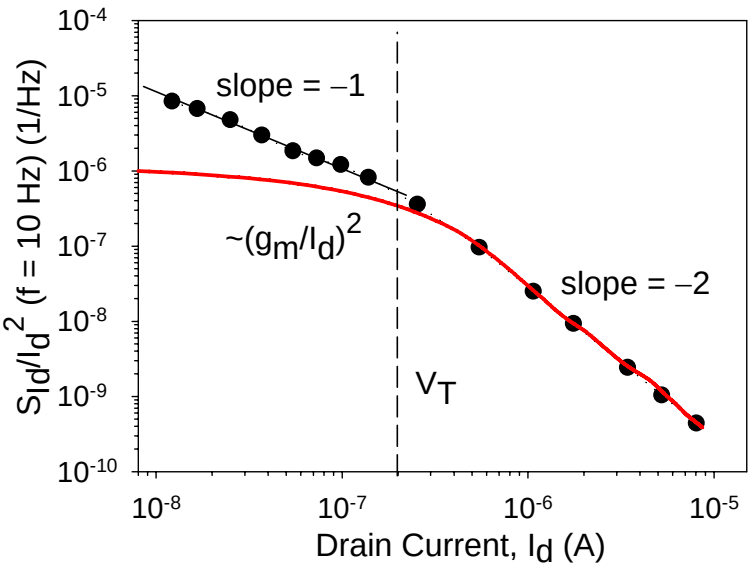

Figure 4.4: Measured normalized drain-current noise spectral density S_{Id}/I_d^2 (symbol) and (*constant* × $(g_m/I_d)^2$) (thick solid line) at f = 10 Hz and V_{ds} = 50 mV vs. drain current from weak to strong inversion for the investigated FinFETs. The thin solid line fitting the noise data in weak inversion is based on (4.18).

The frequency dependence of the drain-current noise spectral density S_{Id} at V_{ds} = 50 mV with V_{gs} sweeping from 40 to 100 mV in a 12-mV step in the weak-inversion subthreshold region is shown in Figure 4.5(a), which is the noise data source corresponding to the plot of S_{Id}/I_d^2 vs. I_d at f = 10 Hz in this region in Figure 4.4. The unitary frequency exponent $\gamma \approx 1$ of the $1/f^{\gamma}$ noise is always observed in this region. S_{Id}/I_d vs. V_{ds} for n-type devices in the subthreshold region is shown in Figure 4.5(b). A linear increase at low V_{ds} values is observed and a plateau is reached for high V_{ds} values ($S_{Id}/I_d \approx 1.3 \times 10^{-13}$ A/Hz).

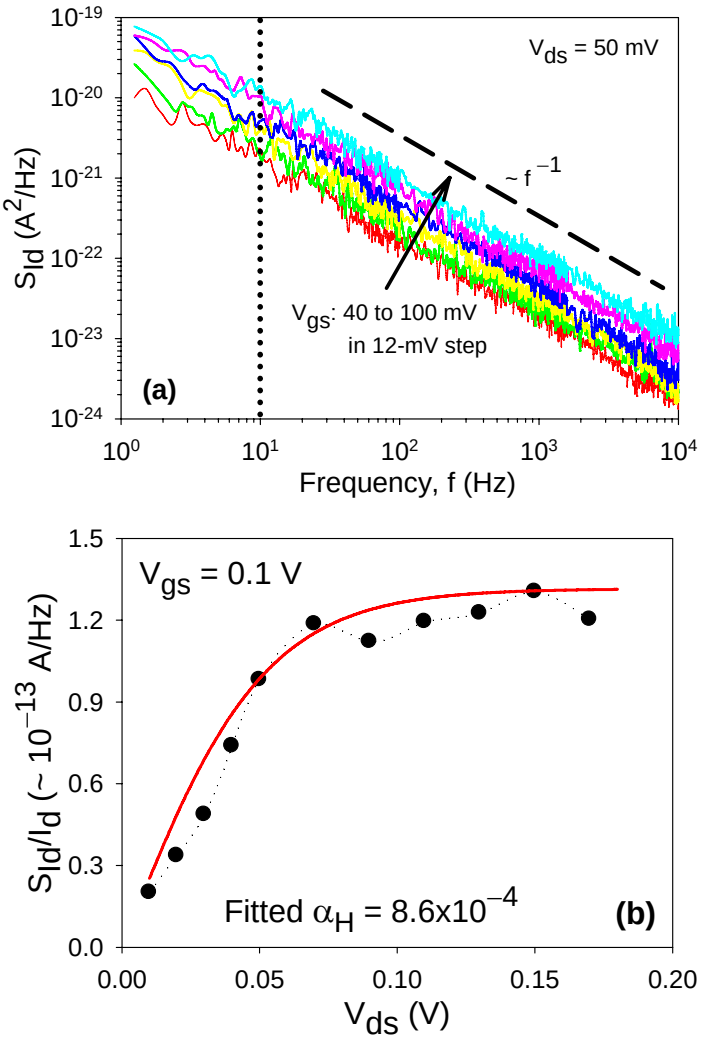

Figure 4.5: (a) Frequency dependence of the drain-current noise spectral density at various gate voltages in the weak-inversion subthreshold region. The unitary frequency exponent is always observed in this region. (b) Variations of S_{Id}/I_d vs. drain voltage V_{ds} at f = 10 Hz in the weak-inversion subthreshold region. Symbol: measurement data. Solid line: fitting by (4.18). Good agreement between experimental and computed data showing the validity of (4.18).

In the subthreshold region, the current-conduction behavior in the FinFET is very different from that in the bulk transistor. In the subthreshold region of a lightly-doped symmetric DG FinFET, both the total inversion charge and drain current are proportional to the fin width for a given bias condition, and volume inversion takes place [93], [94]. This is illustrated by the case of n_1 in Figure 4.3, where it is essentially flat within the silicon film. The channel carriers flow through the whole silicon body and, thus, can be considered as the 'bulk-conduction' as compared with the 'surface-conduction' in bulk-CMOS transistors. The interaction between the oxide traps and the conduction channel is thus suppressed due to the large separation of most carriers from the interface and the oxide traps. Hence, the generation of the exact 1/*f* noise in a single device through the carrier trapping and detrapping process near the Si/SiO_2 interface and its correlated Coulombic mobility scattering becomes less probable. However, the typical 1/*f* noise was observed in most of the investigated FinFETs in the subthreshold region. This may be due to the fact that for the volume-inverted lightly-doped FinFETs in this regime, the Fermi level is not crossing the bandgap at the depletion layer as in the case of bulk MOSFETs. The traps are about half full and half empty and inactive in the trapping/detrapping process. Thus, the number-fluctuated noise is completely eliminated due to this no-active-trap situation and the pure mobility-fluctuated 1/*f* noise is observed. But still in some devices, a single-trap random telegraph signal (RTS) noise on top of the 1/*f* noise is observed. Since the silicon channel is not completely isolated from the Si/SiO_2 interface, there may be one trap with an appropriate energy level and thus becoming active in the trapping/detrapping process. The residual signal after subtracting this RTS noise still exhibits a 1/*f* spectrum. The bias dependence of the 1/*f* noise in both cases is the same as that in Figure 4.4 and Figure 4.5. This is evident from experiments of the RTS noise

in small-area devices [77]: when the number-fluctuated noise is completely eliminated, the mobility-fluctuated noise still remains. Hence, in the weak-inversion subthreshold region, the 1/*f* noise is observed to follow the mobility-fluctuation behavior. The observation of a single-trap RTS noise on top of the mobility-fluctuated 1/*f* noise in some devices and the pure mobility-fluctuated 1/*f* noise in most of other devices actually suggests a transition from the carrier number to the mobility fluctuation as the predominant noise generation mechanism when the conduction region is moved from the surface to the volume of the FinFET.

4.2.2. Model for the channel 1/*f* noise

The empirical relation of the mobility-fluctuation model [18], [23], [95] is given by

$$\frac{S_{Id}(f)}{I_d^2} = \frac{\alpha_H}{fN} \tag{4.11}$$

with α_H the Hooge parameter and N the total number of carriers under the gate.

The subthreshold current of the lightly-doped symmetric DG FinFET can be expressed as [93]

$$I_d = \mu \frac{W}{L} kT n_i t_{si} e^{\frac{q(V_{gs}-\Delta\Phi)}{kT}} \left(1 - e^{-\frac{qV_{ds}}{kT}}\right) \tag{4.12}$$

where μ is the effective mobility, $W = 2H_{fin}$ the total channel width, L the effective channel length, n_i the intrinsic carrier concentration, t_{si} the silicon fin width, and $\Delta\Phi$ the work function difference between the gate electrode and the almost-intrinsic silicon body.

As described in [93], the electric potential ψ across the silicon body is obtained by integrating the Poisson's equation twice, and β is a constant used in the solution of ψ and to be determined from the boundary conditions in different operation regions. From both the surface-potential expression ψ_s and Gauss's law applied at the Si/SiO_2 interface, a β-dependent expression $f_r(\beta)$ is defined as [93]

$$f_r(\beta) = \frac{q}{2kT}\left(V_{gs} - V_o - V(x)\right) \tag{4.13}$$

with

$$V_o = \Delta\Phi + \frac{2kT}{q}\ln\left(\frac{2}{t_{si}}\sqrt{\frac{2\varepsilon_{si}kT}{q^2 n_i}}\right) \tag{4.14}$$

where $V(x)$ is the electron quasi-Fermi potential at x along the channel and β is a parameter used in the solution of ψ across the silicon body. In the subthreshold region, $\beta << 1$, $f_r(\beta) \sim \ln(\beta)$ [93], together with (4.13), β can be derived as

$$\beta = e^{\frac{q}{2kT}\left(V_{gs} - V_o - V(x)\right)}. \tag{4.15}$$

$Q_i(x)$, the carrier charge density per unit area in the channel at x, is derived in [93] as

$$Q_i(x) = 8\frac{\varepsilon_{si}}{t_{si}}\frac{kT}{q}\beta\tan\beta. \tag{4.16}$$

Since $\beta << 1$ in the subthreshold region, we have $\tan\beta \approx \beta$, and substituting (4.14) and (4.15) into (4.16), we have

$$Q_i(x) \approx 8\frac{\varepsilon_{si}}{t_{si}}\frac{kT}{q}\beta^2 = qn_i t_{si} e^{\frac{q}{kT}\left(V_{gs} - \Delta\phi - V(x)\right)}. \tag{4.17}$$

Following the approach described in [49] and with the help of (4.12) and (4.17), the final expression of S_{Id}/I_d^2 in the subthreshold region is given by

$$\frac{S_{Id}(f)}{I_d^2} = \frac{\alpha_H}{fN} = \frac{\alpha_H}{f}\frac{2\mu kT}{L^2}\frac{1-e^{\frac{-qV_{ds}}{kT}}}{1+e^{\frac{-qV_{ds}}{kT}}}\frac{1}{I_d}. \quad (4.18)$$

4.2.3. Model verification and Hooge parameter extraction

Based on (4.18), α_H is extracted to be $\alpha_H \approx 8.6\times10^{-4}$ for a good fitting to the noise data in the subthreshold region, as shown in Figure 4.4. The computed S_{Id}/I_d using the extracted α_H and (4.18) is plotted in Figure 4.5(b). A good agreement between the measured and calculated noise data is observed. The extracted α_H is within but close to the high end of the data range reported for bulk-CMOS devices with the SiO_2/poly-Si gate stack [96]. The fact that the α_H value critically depends on the crystalline quality has led to the following refinement: $\alpha_H = \alpha_{H,ph}(\mu/\mu_{ph})^2$ [25], with $\alpha_{H,ph}$ a constant around 2×10^{-3}, μ_{ph} the mobility limited by the phonon (lattice) scattering only. This expression follows the concept that the phonon (lattice) scattering is the dominant noise generation process for the mobility-fluctuated 1/*f* noise, while other types of scattering mechamisms, such as the impurity and surface roughness scattering, will lower the mobility μ and thus suppress the 1/*f* noise through this relationship. For the FinFET with an almost-undoped body, the impurity scattering is insignificant, and in the subthreshold region the body is volume-inverted with carriers conducting through the whole silicon fin, the surface roughness scattering is also insignificant. Hence, the phonon (lattice) scattering that always exists in the device is the dominant scattering mechanism. This explains why the extracted α_H of FinFETs is at the high end of the α_H-range reported for bulk-CMOS devices. The bulk-CMOS devices having a higher channel doping concentration and with the surface-conduction behavior may lead to the higher impurity and surface roughnesses scattering and, thus, lower the values of α_H.

4.3. Low-frequency noise in the strong-inversion region

4.3.1. Measurement results and discussion

The normalized drain-current noise S_{Id}/I_d^2 at f = 10 Hz against the drain current I_d in the strong-inversion region at V_{ds} = 50 mV is also shown in Figure 4.4. The measured S_{Id} keeps almost constant as V_{gs} sweeping in the strong-inversion region, and the observed S_{Id}/I_d^2 is largely proportional to $(g_m/I_d)^2$. The proportional correlation between S_{Id}/I_d^2 and $(g_m/I_d)^2$ shown in Figure 4.4 indicates that the $1/f^{\gamma}$ noise in the strong-inversion region is attributed to the carrier number-fluctuation model [40], [42], and the carrier trapping/detrapping process near the Si/SiO_2 interface is the origin of the $1/f^{\gamma}$ noise. For the symmetric DG FinFETs in strong inversion, as the carrier charges near the Si/SiO_2 interface increase, the gate field is screened from the center of the silicon fin. The potentials at the Si/SiO_2 interface and in the middle of the silicon fin become decoupled; there is no volume inversion anymore. For the case of n_2 in Figure 4.3, the device operates in the transition regime from weak to strong inversion. The curve of n_2 is still quite flat, but the electron densities at two interfaces are starting to rise. Entering into strong inversion, intense electrons are accumulated at two Si/SiO_2 interfaces, as illustrated in the case of n_3 in Figure 4.3. The drain-current fluctuation is dominated by the intensive interations of electrons between the near-interface oxide traps and the channel. Thus, in the above-threshold region, the bias and geometry dependence of the drain current is exactly the same as that described in the bulk-CMOS charge-sheet model, except that the drive current doubles due to two conduction channels in the DG FinFET [93], [94]. This means that the carriers conduct close to the Si/SiO_2 interface instead of spreading over the entire silicon fin and, thus, the number-fluctuation mechanism is dominant in the strong-inversion region.

For the carrier-number fluctuation model including the correlated mobility fluctuation, the gate-voltage-referred noise spectral density is given by [42]

$$S_{Vg} = \frac{S_{Id}}{g_m^2} \tag{4.19}$$

$$S_{Vg} = S_{Vfb}\left[1 + \alpha\mu_o C_{ox}\left(V_{gs} - V_T\right)\right]^2 \tag{4.20}$$

$$\sqrt{S_{Vg}} = \sqrt{S_{Vfb}}\left[1 + \alpha\mu_o C_{ox}\left(V_{gs} - V_T\right)\right] \tag{4.21}$$

where α is the Coulombic scattering coefficient, μ_o the low-field mobility, C_{ox} the gate oxide capacitance per unit area, S_{Vfb} the flatband-voltage noise spectral density associated with the near-interface charge fluctuations. The calculation of S_{Vfb} depends on the tunneling mechanism selected in explaining the number-fluctuated $1/f^{\gamma}$ noise.

Figure 4.6 shows the plot of $(S_{Vg})^{1/2}$ measured at f = 10 Hz vs. the gate voltage overdrive ($V_{gs} - V_T$), which is the same noise data source as the plot of S_{Id}/I_d^2 vs. I_d at f = 10 Hz in the strong-inversion region in Figure 4.4. The fitting curve calculated by (4.21) is also shown in Figure 4.6. The rather flat slope of the curve indicates that the correlated mobility fluctuation is insignificant. From the calculated fitting curve by (4.21), it is found that the term corresponding to the correlated mobility fluctuation in the square bracket of (4.20) and (4.21) is no more than seven percent of the term corresponding to the carrier-number fluctuation; therefore, the correlated mobility fluctuation is negligible in the studied FinFETs.

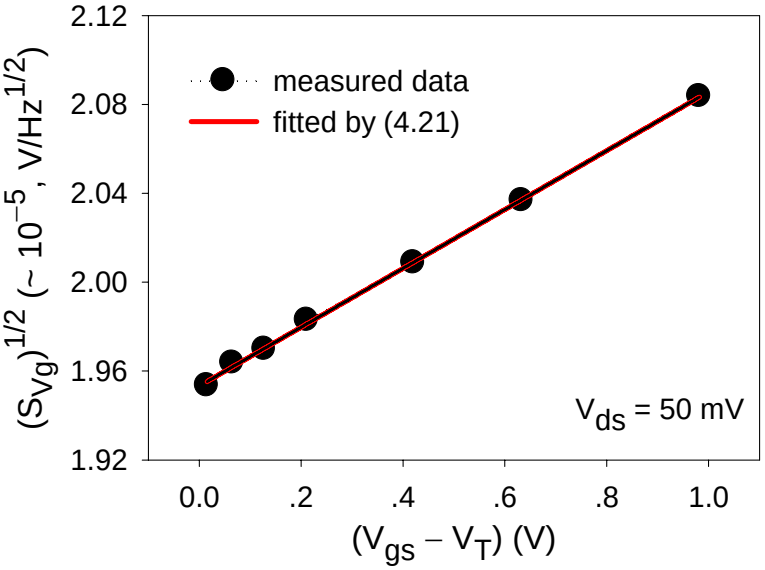

Figure 4.6: Symbols are measured $<S_{Vg}>^{1/2}$ vs. $(V_{gs} - V_T)$ at V_{ds} = 50 mV and f = 10 Hz. The solid line is the fitting curve by (4.21).

The following analyses of the $1/f^{\gamma}$ noise data are mainly based on "Device 1", but to provide an idea about the reproducibility and sensitivity of the noise results in "Device 1", the noise data in "Device 2" that is processed in a nominally identical fashion from the same wafer are also shown in Figure 4.7 to Figure 4.9.

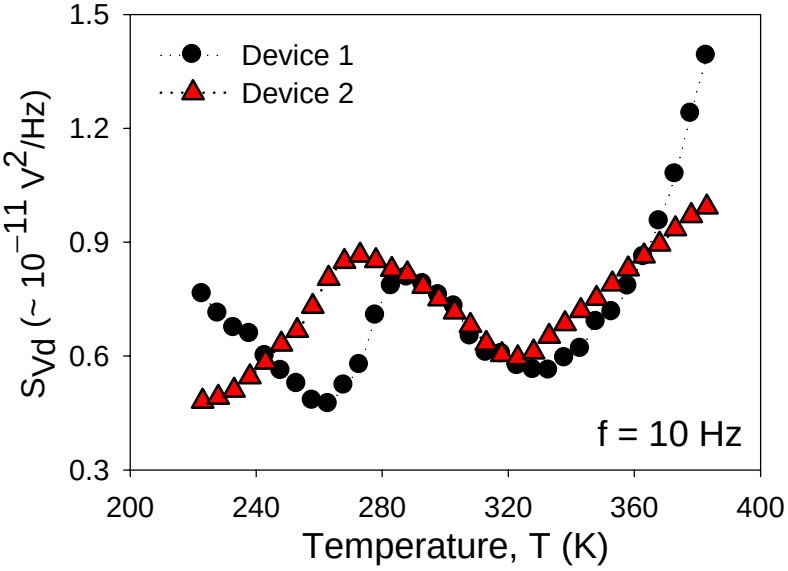

Figure 4.7: The measured drain-voltage noise spectral density at f = 10 Hz vs. temperature T for two FinFETs biased at V_{ds} = 50 mV and $V_{gs} - V_T$ is kept constant at 0.5 V at each temperature.

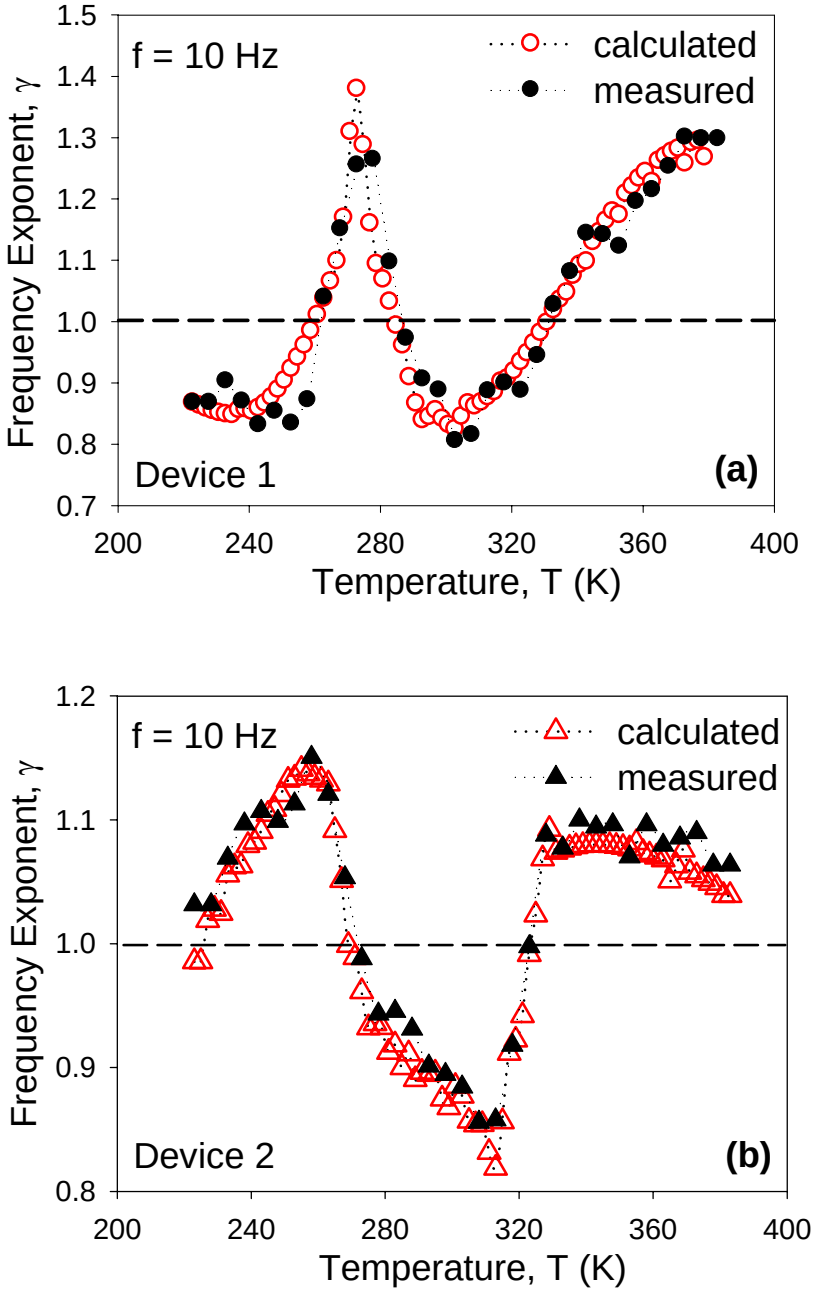

Figure 4.8: The frequency exponent γ as a function of the temperature T at f = 10 Hz. Solid symbol: measurement data, Open symbol: calculated data from Figure 4.7 through (4.39). (a) Device 1. (b) Device 2.

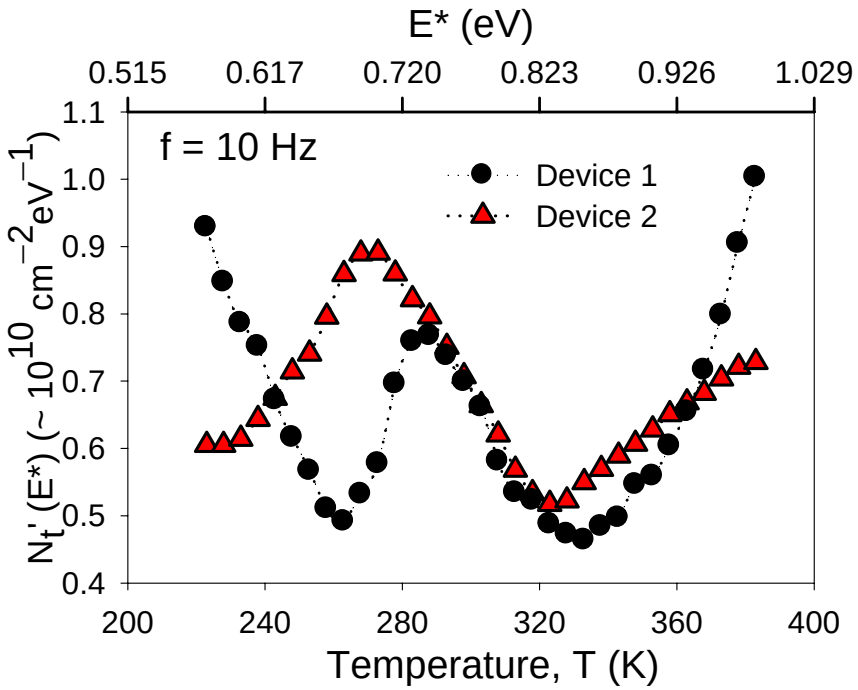

Figure 4.9: The surface trap density computed from the temperature dependence of the drain-voltage noise spectral density by (4.38), as a function of T and E^*, where the energy scale E^* is inferred from (4.32) at f = 10 Hz. Results from both devices are shown.

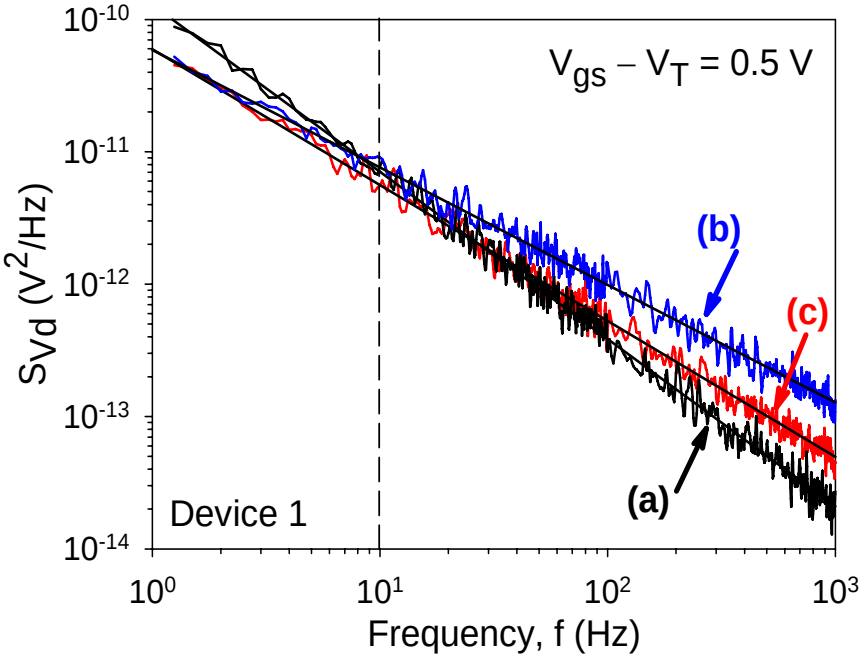

Figure 4.10: Drain-voltage noise spectral density S_{Vd} vs. frequency at three sample temperatures in "Device 1" labeled as (a) T = 278 K, γ = 1.26, (b) T = 298 K, γ = 0.89, and (c) T = 333 K, γ = 1.03. A large variations in the frequency dependence is observed as a function of the temperature between 223 K and 383 K, from which γ at each T is extracted and plotted in Figure 4.8.

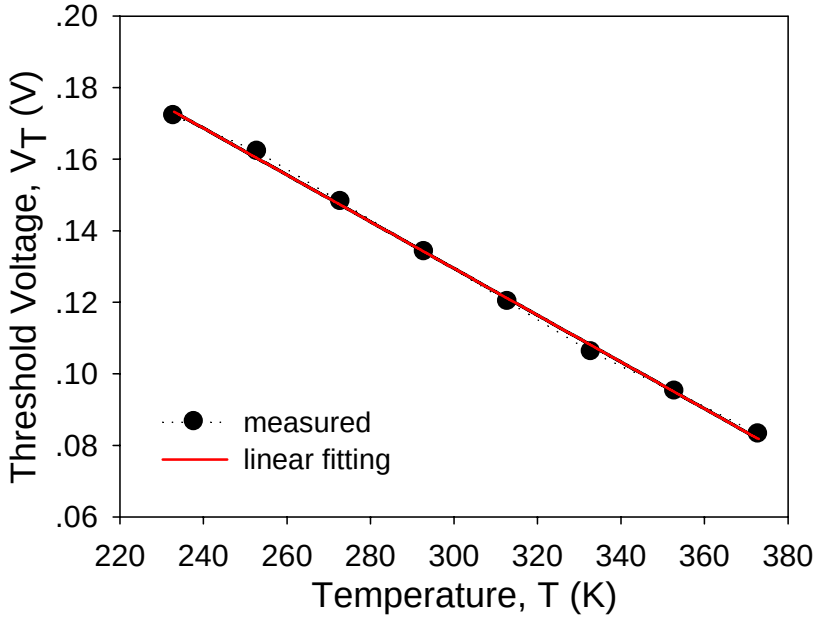

Figure 4.11: Threshold voltage as a function of the temperature *T* for n-channel FinFETs to ensure that $V_{gs} - V_T$ is constant during all noise vs. temperature measurements. Symbol: measurement data, Solid line: linear fitting.

Different frequency dependence from that in the weak-inversion subthreshold region is observed in the strong-inversion region. The frequency exponent $\gamma < 1$ is observed in the room-temperature noise data ($\gamma = 0.89$ in "Device 1", curve (b) in Figure 4.10). To determine whether the γ deviation from unity is due to the nonuniform spatial distribution of the oxide traps in the tunneling model, or the nonuniform distribution of the activation energies in the thermally-activated oxide-trap model, the drain-voltage noise spectral densities were measured at an interval of 5 K between 223 K and 383 K with the drain biased at $V_{ds} = 50$ mV. Figure 4.11 shows the threshold voltage of n-channel FinFETs as a function of the temperature *T*. As expected, V_T decreases with the increasing temperature by ~0.65 mV/K [97]. V_{gs} were adjusted as a function of the temperature to ensure that $V_{gs} - V_T$ remained constant at 0.5 V for noise measurements at different temperatures to facilitate the comparison of the noise data. Figure 4.10 shows the typical noise vs. frequency curves at three

different temperatures in "Device 1". Each curve shows a "generic" $1/f^{\gamma}$ noise with γ being close to, but not exactly equal to one. For example, at 278 K, S_{Vd} (10 Hz) = 7.07×10^{-12} V^2/Hz and γ = 1.26, while S_{Vd} (10 Hz) = 5.61×10^{-12} V^2/Hz and γ = 1.03 at 333 K, illustrating the large range of variations in the noise magnitude and frequency dependence observed at different temperatures.

In Figure 4.7, the drain-voltage noise spectral density at f = 10 Hz is plotted as a function of the temperature T for both devices. The noise levels are quite comparable over the entire temperature range for different devices, especially near the room temperature. The frequency dependence γ of the noise measurements in Figure 4.7 as a function of T is correspondingly shown in Figure 4.8. Interestingly, the peak and dip in the γ curve in Figure 4.8 occur at the temperatures where the changes in the S_{Vd} curve in Figure 4.7 have the local maximal positive and negative slopes, respectively. This qualitative correlation is observed in all the measured devices. Take "Device 1" as an example, the peak in γ at 273 K in Figure 4.8(a) corresponds to the local maximal positive differential change of S_{Vd} with respect to T in "Device 1" in Figure 4.7, while the dip in γ at 303 K corresponds to the local maximal negative differential change of S_{Vd} with respect to T. These are the qualitative correlations one would expect to see if the $1/f^{\gamma}$ noise was caused by a thermally-activated process described by the Dutta–Horn model [17], [19], [98]. Hence, the thermal-activation model is first developed and verified in sections 4.3.2 and 4.3.3. In Section 4.3.4, the applicability of the McWhorter model in explaining the noise data in Figure 4.7 and Figure 4.8 is discussed.

4.3.2. Thermal-activation model for the channel 1/*f* noise

The thermal-activation model, in which the carriers are assumed to be captured or emitted by traps located at energy levels different from the carrier quasi-Fermi level, may be used to explain the $1/f^{\gamma}$ noise. For the traps located at energy levels much higher than the carrier quasi-Fermi level, most of the traps are empty and available for the trapping and detrapping of channel carriers. The noise spectral density of the occupancy of oxide-traps within an elemental channel length Δx is given by [17], [19]

$$S_{\Delta N_t}(x,f) = \int_0^{\infty}\int_0^{t_{ox}}\int_0^{2H_{fin}} 4N_t(E)\Delta x \frac{\tau_{th}}{1+\omega^2\tau_{th}^2} dydzdE \tag{4.22}$$

where $N_t(E)$ ($cm^{-3}eV^{-1}$) is the trap density per unit volume per unit energy, E the trap activation energy, and τ_{th} the thermal activation time constant, which is dependent on the distribution of activation energies as

$$\tau_{th} = \tau_o \exp(E/kT) \tag{4.23}$$

where τ_o is a characteristic attempt time for the random process and $\tau_o \approx 1.8\times10^{-14}$ s is used [99]. Assuming $N_t(E)$ is uniformly distributed in the gate area, (4.22) can be easily integrated out in the direction of channel width (y direction) as

$$S_{\Delta N_t}(x,f) = 4\Delta x(2H_{fin})\int_0^{\infty}\int_0^{t_{ox}} N_t(E)\frac{\tau_{th}}{1+\omega^2\tau_{th}^2} dzdE. \tag{4.24}$$

Since the surface trap density per unit energy $N_t'(E)$ ($cm^{-2}eV^{-1}$) is related to the volume trap density per unit energy $N_t(E)$ ($cm^{-3}eV^{-1}$) as

$$N_t'(E) = \int_0^{t_{ox}} N_t(E)dz. \tag{4.25}$$

(4.24) can be further written as

$$S_{\Delta N_t}(x,f) = 4\Delta x\left(2H_{fin}\right)\int_0^{\infty} N_t^{'}(E)\frac{\tau_{th}}{1+\omega^2\tau_{th}^2}dE. \tag{4.26}$$

From the detailed derivation presented in [38] and neglecting the term corresponding to the correlated mobility fluctuation as explained in Figure 4.6, it is known that

$$S_{\Delta Id}(x,f) = \left(\frac{I_d}{\left(2H_{fin}\right)\left(\Delta x\right)N^*}\right)^2 S_{\Delta N_t}(x,f) \tag{4.27}$$

where $S_{\Delta Id}$ is the local drain-current noise spectral density within the elemental channel length Δx, N^* is the number of channel carriers per unit gate area.

For the number-fluctuated $1/f^{\gamma}$ noise, the total drain-current noise spectral density in the strong-inversion region at low drain biases is derived as [10], [38]

$$S_{Id}(f) = \frac{1}{L^2}\int_0^L S_{\Delta Id}(x,f)\Delta x dx. \tag{4.28}$$

Substitute (4.27) into (4.28), we have

$$S_{Id}(f) = \frac{1}{L^2}\int_0^L \frac{I_d^2}{\left(2H_{fin}\Delta x N^*\right)^2} S_{\Delta N_t}(x,f)\Delta x dx. \tag{4.29}$$

Then, substitute (4.26) into (4.29), we have

$$S_{Id}(f) = \frac{4I_d^2}{2H_{fin}L^2}\int_0^L \frac{1}{\left(N^*\right)^2}dx\int_0^{\infty}\frac{N_t^{'}(E)\tau_{th}}{1+\omega^2\tau_{th}^2}dE. \tag{4.30}$$

At very low drain biases, the carrier density can be assumed to be uniform along the channel and is given by $qN^* = C_{ox}(V_{gs} - V_T)$, where C_{ox} is the gate oxide capacitance per unit gate area. Then, (4.30) becomes

$$S_{Id}(f) = \frac{4I_d^2q^2}{2H_{fin}LC_{ox}^2\left(V_{gs}-V_T\right)^2}\int_0^{\infty}\frac{N_t^{'}(E)\tau_{th}}{1+\omega^2\tau_{th}^2}dE. \tag{4.31}$$

The Lorentzian in (4.31) is a sharply-peaked function of the activation energy E with the peak E^* given by [17], [19]

$$E^* = -kT\ln\left(\tau_o\omega\right). \tag{4.32}$$

Hence, (4.31) can be approximated as

$$S_{Id}\left(f\right) = \frac{4I_d^2q^2}{2H_{fin}LC_{ox}^2\left(V_{gs}-V_T\right)^2}N_t^{'}\left(E^*\right)\int_0^\infty \frac{\tau_{th}}{1+\omega^2\tau_{th}^2}dE. \tag{4.33}$$

By making use of (4.23), the integral variable can be changed from E to τ_{th}, since dE = (kT/τ_{th})dτ_{th}, and (4.33) becomes

$$S_{Id}\left(f\right) = \frac{4I_d^2q^2}{2H_{fin}LC_{ox}^2\left(V_{gs}-V_T\right)^2}N_t^{'}\left(E^*\right)kT\int_0^\infty \frac{1}{1+\omega^2\tau_{th}^2}d\tau_{th} \tag{4.34}$$

$$\approx \frac{I_d^2q^2kTN_t^{'}\left(E^*\right)}{2H_{fin}LC_{ox}^2\left(V_{gs}-V_T\right)^2 f^\gamma}. \tag{4.35}$$

Hence, for very low drain biases, the total drain-voltage noise spectral density across the conduction channel is obtained as

$$S_{Vd}\left(f\right) = \frac{S_{Id}\left(f\right)}{g_{OUT}^2} \approx \frac{V_{ds}^2q^2kTN_t^{'}\left(E^*\right)}{2H_{fin}LC_{ox}^2\left(V_{gs}-V_T\right)^2 f^\gamma} \tag{4.36}$$

where g_{OUT} is the output channel conductance. From (4.36), $N_t'(E^*)$ can be obtained directly as in (4.37) below. For a fixed $V_{gs} - V_T$ and V_{ds} at different temperatures, $N_t'(E^*)$ is proportional to $\omega S_{Vd}/(kT)$ [17]

$$N_t^{'}\left(E^*\right) = \frac{2H_{fin}LC_{ox}^2\left(V_{gs}-V_T\right)^2}{q^2V_{ds}^2}\frac{f^\gamma S_{Vd}}{kT} \tag{4.37}$$

$$\approx \frac{2H_{fin}LC_{ox}^2\left(V_{gs}-V_T\right)^2}{q^2V_{ds}^2}\frac{fS_{Vd}}{kT} \propto \frac{\omega}{kT}S_{Vd}. \tag{4.38}$$

Using (4.32) and (4.38), and following the derivation of Dutta and Horn [17], the frequency exponent γ of the $1/f^{\gamma}$ noise spectral density is given as

$$\gamma = -\frac{\partial \ln S_{Vd}}{\partial \ln \omega} = 1 - \frac{1}{\ln(\omega \tau_o)}\left(\frac{\partial \ln S_{Vd}}{\partial \ln T} - 1\right). \tag{4.39}$$

If (4.39) is satisfied, it is a strong evidence that the number-fluctuated $1/f^{\gamma}$ noise is generated due to the thermally-activated process with a distribution of the trap activation energies.

4.3.3. Model verification and surface trap density extraction

To examine whether the measured number-fluctuated $1/f^{\gamma}$ noise can be described by the Dutta–Horn model, (4.39) is applied to calculate $\gamma(T)$ based on the S_{Vd} vs. T plot in Figure 4.7, and then the calculated $\gamma(T)$ is compared with the measured $\gamma(T)$ in the same plot as shown in Figure 4.8. For both devices, the magnitude and the overall shape of the measured $\gamma(T)$ is described reasonably well by the Dutta–Horn model [17], [98], with the largest γ discrepancy of ~0.1 found in "Device 1" between 250 and 280 K. Evidently, the number-fluctuated $1/f^{\gamma}$ noise measured in these FinFETs is well described by a random, thermally-activated process with a distribution of the trap activation energies.

The surface trap density $N_t'(E^*)$ at different temperatures can be extracted based on the S_{Vd} vs. T plot in Figure 4.7 through (4.38). This defect-temperature distribution can be parameterized as a function of the activation energy through (4.32). In Figure 4.9, $N_t'(E^*)$ at f = 10 Hz is plotted as a function of T (lower x-axis) and E^* (upper x-axis). The shape of $N_t'(E^*)$ greatly affects the values of γ because if the trap distribution around E^* increases with energy, $\gamma > 1$; while if $N_t'(E^*)$ decreases with energy, $\gamma < 1$. From this, the effect of a peak in $N_t'(E^*)$ is that γ changes from greater to

smaller than unity, while a dip in $N_t'(E^*)$ results in γ changing from smaller to greater than unity. These corresponding changes in γ and $N_t'(E^*)$ are observed in Figure 4.8 and Figure 4.9, respectively. The extracted trap density is comparable to that of the bulk-CMOS devices with the SiO_2/poly-Si gate stack [43], [96], [100] and is of the same order as that predicted in the ITRS roadmap [96], [101]. The overall magnitudes of the trap-energy distributions extracted in all the measured devices are within the same order and similar to each other, with only the positions of a few characteristic peaks/dips differing in energy. For example, in "Device 1", there are dips in the trap-energy distribution at 0.68 eV and 0.86 eV and a peak near 0.74 eV, whereas in "Device 2" there is one peak and one dip at 0.70 eV and 0.83 eV, respectively. This suggests that the devices have comparable overall defect densities, especially near the room temperature they are almost the same, however, there are likely variations in the detailed defect microstructures. For all the measured devices, the trap density decreases with energy near the room temperature, thus, γ less than unity (~0.9) is observed in the $1/f^{\gamma}$ noise data at the room temperature.

4.3.4. Applicability of the McWhorter noise model

The distinct difference of the McWhorter model from the thermal-activation model is that the channel carriers are captured by or emitted from the oxide traps through the quantum mechanical tunneling, with the tunneling time constant increasing exponentially with the distance z from the Si/SiO_2 interface as [38]

$$\tau_t = \tau_o \exp\left(\alpha_t z\right) \tag{4.40}$$

where $\alpha_t = 10^8$ cm^{-1} is the attenuation coefficient of the electron wave function in the oxide. For the equi-energy tunneling process, only the traps located within kT from the

electron quasi-Fermi level (E_{fn}) contribute to the current fluctuations. The noise spectral density of the occupancy of traps within an elemental channel length Δx in the McWhorter model is given by [38]

$$S_{\Delta N_t}(x,f)=\int_{E_V}^{E_C}\int_0^{t_{ox}}\int_0^{2H_{fin}} 4N_t\Delta x f_t(1-f_t)\cdot\frac{\tau_t}{1+\omega^2\tau_t^2}\,dydzdE \tag{4.41}$$

where $E_C - E_V$ is the silicon energy bandgap. The Fermi-Dirac trap occupancy function f_t is given by

$$f_t=\frac{1}{1+\exp\left(\dfrac{E-E_{fn}}{kT}\right)}. \tag{4.42}$$

$N_t(E, x, y, z)$ is assumed to be uniformly distributed in the gate area, and $f_t(1 - f_t)$ in (4.41) is a sharply-peaked function of the electron quasi-Fermi level E_{fn}. Thus, $N_t(E, x, y, z)$ can be approximated by $N_t(E_{fn}, z)$ and taken out of the integrals with integral variables of x, y, and E. The term $f_t(1 - f_t)$ is replaced by $-kT(df_t/dE)$, since the two expressions are the same. Hence, (4.41) can be further derived as

$$S_{\Delta N_t}(x,f)=4kT(2H_{fin})\Delta x\int_0^{t_{ox}} N_t(E_{fn},z)\frac{\tau_t}{1+\omega^2\tau_t^2}\,dz. \tag{4.43}$$

Similar to the derivation of (4.26)–(4.31), the total drain-current noise spectral density in the strong-inversion region derived based on the McWhorter model is

$$S_{Id}(f)=\frac{4kTI_d^2q^2}{2H_{fin}LC_{ox}^2(V_{gs}-V_T)^2}\int_0^{t_{ox}}\frac{N_t(E_{fn},z)\tau_t}{1+\omega^2\tau_t^2}dz. \tag{4.44}$$

The Lorentzian in (4.44) is a sharply-peaked function of the distance z from the Si/SiO_2 interface with the peak z^* given by

$$z^* = -\frac{1}{\alpha_t}\ln\left(\tau_o \omega\right). \tag{4.45}$$

Similar to the derivation of (4.31)–(4.35), the final expression of $S_{Id}(f)$ is derived approximately as

$$S_{Id}\left(f\right) \approx \frac{I_d^2 q^2 kTN_t\left(E_{fn}, z^*\right)}{2H_{fin}LC_{ox}^2\left(V_{gs}-V_T\right)^2 \alpha_t f^{\gamma}}. \tag{4.46}$$

Similar to the derivation of (4.35)–(4.38), the final expression of $N_t(E_{fn}, z^*)$ is derived approximately as

$$N_t(E_{fn}, z^*) \approx \frac{2H_{fin}LC_{ox}^2\left(V_{gs}-V_T\right)^2 \alpha_t}{q^2 V_{ds}^2}\frac{fS_{Vd}}{kT} \propto \frac{\omega}{kT}S_{Vd}. \tag{4.47}$$

Following the approach of Dutta and Horn [17], if ω and T are varied so as to keep $N_t(E_{fn}, z^*)$ unchanged, $\omega S_{Vd}/kT$ is also unchanged from (4.47), namely,

$$\frac{\partial N_t\left(E_{fn}, z^*\right)}{\partial \omega}\Delta\omega + \frac{\partial N_t\left(E_{fn}, z^*\right)}{\partial T}\Delta T = 0 \tag{4.48}$$

$$\left(\frac{\partial}{\partial \omega}\Delta\omega + \frac{\partial}{\partial T}\Delta T\right)\frac{\omega S_{Vd}}{kT} = 0. \tag{4.49}$$

(4.49) can be rearranged as

$$\Delta\omega\left(\frac{S_{Vd}}{kT} + \frac{\omega}{kT}\frac{\partial S_{Vd}}{\partial \omega}\right) + \Delta T\left(-\frac{\omega}{kT^2}S_{Vd} + \frac{\omega}{kT}\frac{\partial S_{Vd}}{\partial T}\right) = 0. \tag{4.50}$$

Combining (4.48) and (4.50), we have

$$\frac{-\left(\omega/T\right)S_{Vd} + \omega\left(\partial S_{Vd}/\partial T\right)}{S_{Vd} + \omega\left(\partial S_{Vd}/\partial \omega\right)} = \frac{\partial N_t\left(E_{fn}, z^*\right)/\partial T}{\partial N_t\left(E_{fn}, z^*\right)/\partial \omega}. \tag{4.51}$$

Since $\partial S_{Vd}/\partial\omega = (S_{Vd}/\omega)(\partial \ln S_{Vd}/\partial \ln \omega)$ and $\partial S_{Vd}/\partial T = (S_{Vd}/T)(\partial \ln S_{Vd}/\partial \ln T)$, (4.51) becomes

$$-\frac{\omega}{T}\frac{\partial N_t}{\partial \omega}S_{Vd}+\frac{\omega S_{Vd}}{T}\frac{\partial N_t}{\partial \omega}\frac{\partial \ln S_{Vd}}{\partial \ln T}=\frac{\partial N_t}{\partial T}S_{Vd}+S_{Vd}\frac{\partial N_t}{\partial T}\frac{\partial \ln S_{Vd}}{\partial \ln \omega}. \tag{4.52}$$

Then, the frequency exponent γ of the $1/f^{\gamma}$ noise spectral density is given by

$$\gamma=-\frac{\partial \ln S_{Vd}}{\partial \ln \omega}=1-\frac{\omega}{T}\frac{\partial N_t/\partial \omega}{\partial N_t/\partial T}\left(\frac{\partial \ln S_{Vd}}{\partial \ln T}-1\right). \tag{4.53}$$

From (4.45),

$$\frac{\partial z^*}{\partial \omega}=-\frac{1}{\omega \alpha_t}. \tag{4.54}$$

Substitute (4.54) into(4.53), the frequency exponent γ of the $1/f^{\gamma}$ noise spectral density based on the McWhorter model is given by

$$\gamma=-\frac{\partial \ln S_{Vd}}{\partial \ln \omega}=1+\frac{1}{T\alpha_t}\frac{\partial N_t/\partial z^*}{\partial N_t/\partial T}\left(\frac{\partial \ln S_{Vd}}{\partial \ln T}-1\right). \tag{4.55}$$

To test the applicability of the McWhorter model in explaining the measured $\gamma(T)$ in Figure 4.8, the S_{Vd} vs. T plot at f = 10 Hz in Figure 4.7 is used to fit (4.55) to the measured $\gamma(T)$ in Figure 4.8. Without *a priori* knowledge of the spatial variation of the trap density ($\partial N_t/\partial z^*$), one possible fitting is obtained with the condition

$$\frac{1}{T\alpha_t}\frac{\partial N_t/\partial z^*}{\partial N_t/\partial T}=0.036 \tag{4.56}$$

at f = 10 Hz, which corresponds to the same result by (4.39) derived from the Dutta–Horn model, with $-1/\ln(\omega\tau_0) = 0.036$.

From (4.38) and (4.47), $N_t(E_{fn}, z^*) = \alpha_t N_t'(E^*)$ can be obtained. If $N_t'(E^*)$ being independent of z is assumed to follow the temperature variation in Figure 4.9 as predicted by the Dutta–Horn model, $\partial N_t/\partial T$ can be obtained directly by multiplying the

numerical derivative of the data in Figure 4.9 by α_t, as shown in Figure 4.12(a). Then, to meet the condition in (4.56), $\partial N_t/\partial z^* = 0.036T\alpha_t(\partial N_t/\partial T)$ is required, which is plotted in Figure 4.12(b). This implies that for the McWhorter model to explain the measured noise data in Figure 4.7 and Figure 4.8, the variations of the trap density with respect to both the temperature and the trap location have to follow the patterns shown in Figure 4.12 at various temperatures. As noticed, Figure 4.12 is only for the probing frequency f = 10 Hz, which corresponds to z^* = 2.75 nm by (4.45). At a different probing frequency, one would expect a different pattern in Figure 4.12(b) due to a different temperature variation in Figure 4.12(a), which would be a very unlikely event. In addition, if we do not assume the temperature dependence of $N_t'(E^*)$ follows that in Figure 4.9, there could be arbitrary variations of $N_t(E_{fn}, z^*)$ with respect to both T and z^* in order for (4.55) to match the measured noise data, since the McWhorter model involves random variations in both the temperature (ΔE around E_{fn} due to the temperature dependence of E_{fn}) and the trap location (Δz around z^*).

Whereas for the thermal-activation model analyzed in section 4.3.2, the trapping/detrapping time constant has no dependence on z, and is only a function of the trap activation energy E as in (4.23). Hence, (4.39) is automatically fulfilled with no dependence on the detailed trap distribution with respect to the trap location z in each device, and therefore, the thermal-activation model is more convincing than the McWhorter model.

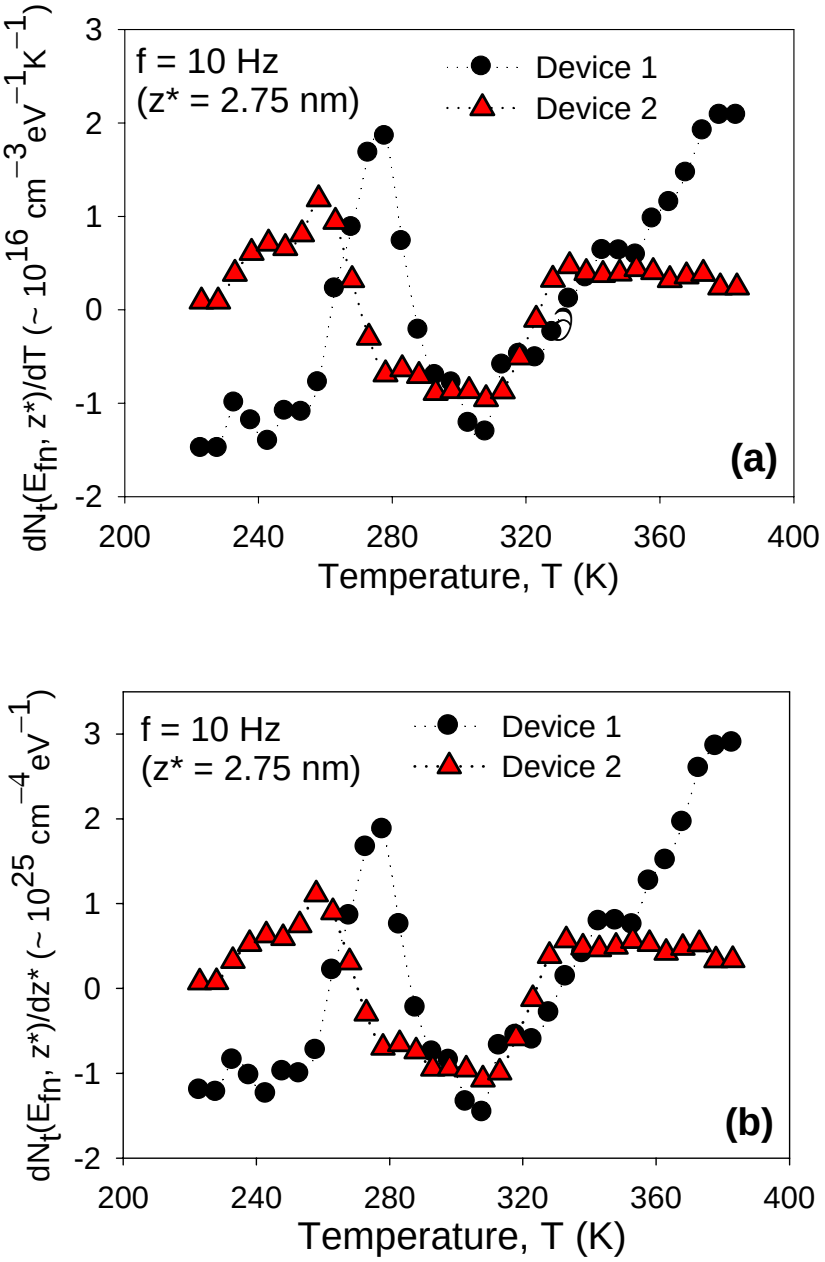

Figure 4.12: (a) Partial derivative of $N_t(E_{fn}, z^*)$ with respect to the temperature T vs. the temperature T, derived based on Figure 4.9, (4.38) and (4.47). (b) Partial derivative of $N_t(E_{fn}, z^*)$ with respect to the trap location z^* vs. the temperature T, obtained based on the data in (a) and (4.56) at f = 10 Hz, which corresponds to z^* = 2.75 nm.

4.4. Chapter 4 conclusion

In conclusion, for the investigated symmetric DG FinFETs, the current conduction in the weak-inversion subthreshold region is volume inversion with channel carriers conducting through the whole silicon body, thus, the mobility

fluctuation is the dominant $1/f$ noise generation mechanism. The extracted Hooge parameter is at the high end of the reported data range for bulk-CMOS devices with the conventional SiO_2/poly-Si gate. This may be due to less surface-roughness and impurity scatterings in the volume-inverted and ultralow-doped FinFETs. The conduction in the strong-inversion region is surface mode with the number fluctuation as the dominant mechanism. Detailed measurements and analyses of the temperature dependence of the $1/f^{\gamma}$ noise are performed as a means to examine the origin of the observed $\gamma < 1$ at room temperature. It is finally believed to be caused by a thermally-activated process with a distribution of activation energies, which can be quantitatively described by the model of Dutta and Horn. The success of this model in describing the correlated temperature and frequency dependence of the noise characteristics allows the energy distribution of the defects responsible for the noise generation to be estimated, and the extracted trap density is comparable to that in bulk-CMOS devices. Applicability of the McWhorter model for explaining the same noise data has also been examined, and it is found ambiguous due to possible random variations of the trap density with respect to both the temperature and the trap location. Due to the comparable noise characteristics to the bulk-CMOS counterpart, the FinFET device is expected to be very promising for analog and RF circuit applications.

CHAPTER 5: **Low-Frequency Noise in Gate-All-Around Silicon Nanowire Transistors**

Due to its better gate control, the gate-all-around (GAA) silicon nanowire transistor (SNWT) [102]–[105] is considered an important candidate for future CMOS scaling beyond 32-nm node. The GAA nanowire CMOS inverter logic gates and ring oscillators (RO) have been fabricated and characterized in the literature [106]–[109]. The noise margin and the inverter threshold voltage depend on the transitions between the subthreshold and the strong-inversion regions. High noise levels in the subthreshold region (close to the threshold voltage) may disturb the normal switching behaviors. SNWTs have also been widely studied as chemical and biochemical sensors [109]–[112]. The biosensing is based on the pronounced conductance changes induced by the depletion of the silicon body when the charged biomolecules are bound to the channel surface. The high noise level in the depletion (subthreshold) region may lead to the reduced signal-to-noise ratio in these sensors. Hence, the LFN in GAA SNWTs is a main concern in the subthreshold region. Different noise generation mechanisms from [9] are observed. Together with the study of the impact of channel orientations (<110> and <010> directions), it concludes that the mobility-fluctuated LFN is dominant in the subthreshold region.

On the other hand, as the SNWT has an almost intrinsic body, the normal SiO_2/poly-Si gate stack may set the wrong threshold voltage V_T. The cost-effective FUlly SIlicided (FUSI) metal-gate scheme with dual gate work functions is thus

introduced [113], [114]. The FUSI-gate work function is optimized through the silicidation-induced impurity segregation (SIIS) [115], so that the desired V_T for low-power applications of SNWTs can be achieved. Hence, in the strong-inversion region, the LFN characteristics in GAA SNWTs with the respective conventional poly-Si gate, pre-doped NiSi FUSI gate (doped-FUSI), and undoped NiSi FUSI gate (undoped-FUSI) are compared. Different gate voltage dependences of the LFN above V_T are observed, which means that different charge conditions near the gate/SiO_2 interface induced by different gate electrodes may play an important role in the low-frequency channel current fluctuations, most likely through the mobility scattering.

The multi-gate transistors also turn out to be an effective way to meet the scaling limitations of nonvolatile memory (NVM) cells. The SONOS-type NVM cells fabricated by combining a nitride trap layer with the FinFET [116] or the GAA SNWT [117] have demonstrated good memory performance. However, the Fowler–Nordheim (FN) tunneling mechanism, which has been widely used for programming and erasing NVM cells, induces the gradual degradation of the oxide properties such as the oxide-trap generation [118]. The 1/*f* noise probed in the transistor is mostly correlated with the oxide-traps existing within 3 nm from the SiO_2/Si interface [119], and should therefore be one of the accurate methods for characterizing the oxide degradation. Hence, a comparative study of the 1/*f* noise degradation caused by the FN tunneling stress in cylindrical-channel GAA SNWTs and planar-channel double-gate (DG) FinFETs under different polarities and magnitudes of the stress voltage and different stress times is performed. The impact of the device architecture is clearly observed and further studied by simulating the potential-energy distribution and the electric field in the gate oxide and around the SiO_2/Si interface.

CHAPTER 5: LFN in Gate-All-Around Silicon Nanowire Transistors

5.1. Low-frequency noise in the weak-inversion subthreshold region

5.1.1. Device and dc measurement

The details of the fabrication process were as follows [105]: The 8"-(100) silicon-on-insulator (SOI) wafer with a silicon layer (~10^{15} cm^{-3}) of thickness 200 nm on top of a buried oxide (BOX) of thickness 150 nm was used as a starting material. The active area was patterned and etched down to a 60-nm-wide Si narrow fin of different lengths by the alternating-phase-shift-mask (alt-PSM) lithography in a KrF scanner, plasma resist trimming and dry etching. The short-length fin can be achieved by using the advanced lithography tools such as ArF with immersion and/or by some kind of spacer techniques. The patterned Si was then oxidized in the dry O_2 at 875 °C for 4 hours, which resulted in two Si nanowire cores due to the stress limited oxidation and located at the bottom and top of the Si fin respectively. The top wire was etched away by dry etching and the bottom wire was released from the oxide by wet etching (6-min dip in the 1:25 DHF solution). It was followed by the gate stack deposition, which contained 4-nm thermally-grown SiO_2 and 130-nm LPCVD amorphous-Si (α-Si). After the gate stack deposition, the gate was patterned and etched. To surmount the issue of defining the gate under the silicon body and to protect the nanowire during the gate dry-etch step in case of any misalignment in the gate lithography step, the gate was defined longer than the wire length, around 70-nm oversize on each side of the wire. The implantation of the source/drain (S/D) and α-Si gate was then carried out using As with 4×10^{15} cm^{-2} dose and 30 keV energy and BF_2 with 2×10^{15} cm^{-2} dose and 35 keV energy for N- and P-FETs, respectively. A longer activation annealing (950 ºC for 15 min) was used to ensure the uniform dopant diffusion throughout the α-Si gate and S/D extensions beneath the gate. The standard metal-contact formation and

sintering processes completed the process. The schematic view of the SNWT is shown in Figure 5.1(a). The thickness of the thermally-grown SiO_2 gate dielectric is 4 nm. The Si core has a cross section of rectangular shape with the height of ~120 nm and width of ~30 nm. For the calculation purpose, the cross section of the SNWT is treated as a circle with an equivalent radius of ~40 nm. The gate lengths L of the investigated SNWTs are 90, 130, and 180 nm.

Prior to noise analyses, the dc characteristics of SNWTs were measured by an HP4156C Semiconductor Parameter Analyzer. The transfer characteristics of both n- and p-type SNWTs with the gate length of 90 nm at $|V_{ds}|$ = 50 mV and with the channel oriented in the <110> and <010> directions are shown in Figure 5.1(b). The typical electrical parameters of the measured SNWTs are the threshold voltage of 0.13 V for n-FET and –0.27 V for p-FET, and the subthreshold slope of ~60 mV/dec for n-FET and 66 mV/dec for p-FET. LFN measurements were then performed using two battery-powered SR570 Low-Noise Current Preamplifiers and one HP35670A Dynamic Signal Analyzer to obtain the frequency spectrum. The background noise at corresponding gate voltages with all other terminals grounded was also measured, and subtracted from measurements at nonzero drain biases to obtain the device LFN.

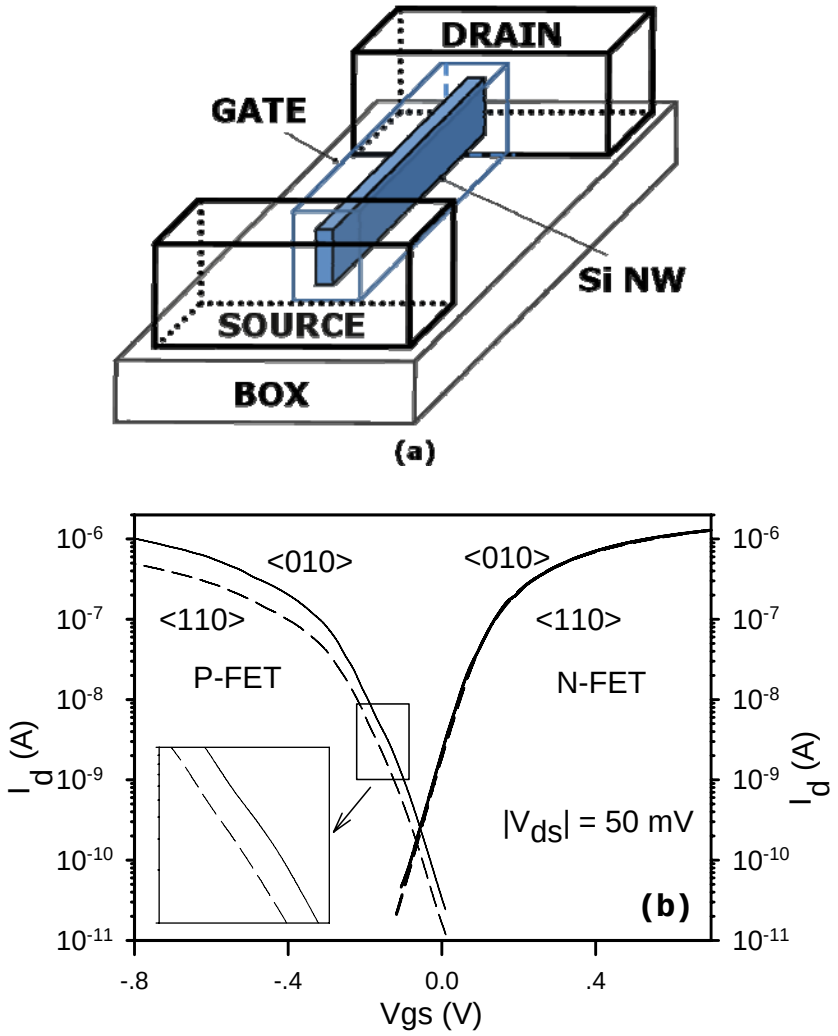

Figure 5.1: (a) Schematic view of the SNWT. (b) Transfer characteristics of both n- and p-type SNWTs with L = 90 nm at $|V_{ds}|$ = 50 mV, and with the channel oriented in the <010> and <110> directions, respectively. The Zoom-in view of the subthreshold current of the p-FET from I_d = 1×10^{-9} to 1×10^{-8} A is shown in the inset.

5.1.2. Measurement results and discussion

In the subthreshold region, the current-conduction behavior in the SNWT is very different from that in the bulk-CMOS transistor. In the subthreshold region of a lightly-doped GAA SNWT, the drain-current level is proportional to the area of the cylindrical cross section for a given bias condition, and volume inversion takes place [105], [120]. The carriers flow through the whole silicon body and, thus, can be considered as the "bulk conduction" as compared to the "surface conduction" in bulk-

CMOS transistors. The interaction between the oxide traps and the conduction channel is therefore suppressed due to the large separation of most carriers from the interface and the oxide traps. In the ultrascaled SNWTs with the gate area below 0.1 μm^2, only several traps, or a single trap, or even no trap would be active in the trapping and detrapping process near the Si/SiO_2 interface [9], [77]. Hence, the generation of the exact $1/f$ noise in a single ultrascaled SNWT through the carrier trapping and detrapping process and its correlated mobility scattering becomes less probable. However, the typical $1/f$ noise was observed in the studied SNWTs in the subthreshold region with no random telegraph signal (RTS) noise on top of it. This may be due to the fact that for the volume-inverted SNWTs in this regime, the Fermi level is not crossing the bandgap at the depletion layer as in the case of bulk-CMOS transistors and the oxide-traps are about half full and half empty and inactive in the trapping/de-trapping process. Alternatively, this no-active-trap situation may be due to the ultrascaled device dimension. Hence, the number-fluctuated noise is completely eliminated. However, the mobility-fluctuated noise still remains. This is evident from the experiments of the RTS noise in small-area devices, where the residual signal after the subtraction of the RTS noise still exhibits a $1/f$ spectrum [77].

Figure 5.2(a) shows the frequency dependence of the measured drain-current noise spectral density S_{Id} in six samples of the 90-nm p-type SNWTs with the channel oriented in the <110> direction, biased at $V_{ds} = -50$ mV and $I_d = 3.1$ nA. S_{Id} extracted at $f = 10$ Hz of each curve is shown in the inset. A typical $1/f^{\gamma}$ behavior with $\gamma = 1.03$ was obtained. The dispersion of the noise spectral density is around half decade as seen from the inset of Figure 5.2(a). It is significantly lower than that reported in [9], in which the randomly distributed oxide traps introduce up to five orders of S_{Id} dispersions. For volume-inverted SNWTs with the same subthreshold current, the

lattice quality and mobility variations of the ultrascaled SNWTs may be the main reason for S_{Id} dispersions. In order to obtain the average noise spectrum, twenty samples for each gate length were measured. The averaged results of the noise spectral density are used in the following discussion.

Figure 5.2(b) shows the average normalized drain-current noise spectral density $<S_{Id}/I_d^2>$ at f = 10 Hz as a function of the drain current I_d when sweeping the gate voltage V_{gs} while keeping $|V_{ds}|$ constant at 50 mV for both n- and p-type SNWTs with different gate lengths and different channel orientations. The log-log plot of S_{Id}/I_d^2 vs. I_d exhibits a slope close to −1, which shows that the mobility-fluctuation model is involved. If the 1/f noise is due to the carrier-number fluctuations, S_{Id}/I_d^2 is almost independent of the drain current in the subthreshold region and the proportional correlation between S_{Id}/I_d^2 and $(g_m/I_d)^2$ (g_m is the transconductance $\partial I_d/\partial V_{gs}$) should be obtained. However, as shown in the inset of Figure 5.2(b), a large slope deviation between S_{Id}/I_d^2 and $(g_m/I_d)^2$ is observed in the subthreshold region, which further confirms the mobility-fluctuation mechanism. Moreover, the normalized noise S_{Id}/I_d^2 at a fixed drain-current level is almost inversely proportional to L^2, which is a strong indication that the noise contribution from the series resistances is negligible [66].

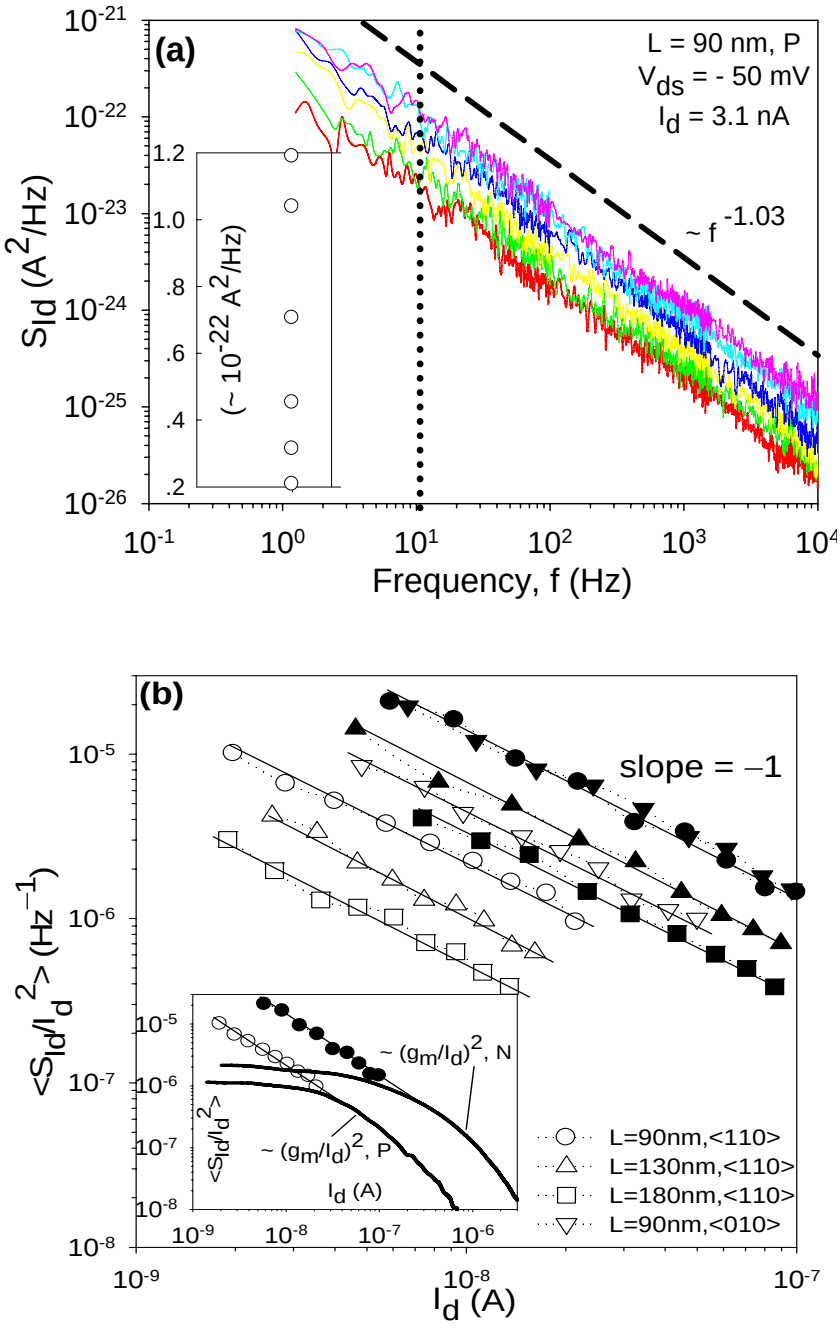

Figure 5.2: (a) Drain-current noise spectral density S_{Id} of six p-type SNWTs with L = 90 nm and the channel oriented in the <110> direction, biased at V_{ds} = -50 mV and constant I_d = 3.1 nA. Measured S_{Id} dispersions at f = 10 Hz is shown in the inset. (b) Average normalized drain-current noise spectral density at $|V_{ds}|$ = 50 mV and f = 10 Hz vs. I_d for both n- and p-type SNWTs with L = 90, 130, 180 nm, respectively. For the L = 90-nm devices, we have the channel oriented in both <010> and <110> directions. The noise data of 90-nm n- and p-type SNWTs in the <110> direction is compared with the corresponding (constant × $(g_m/I_d)^2$) in the inset. Open symbols: p-type, Solid symbols: n-type, Solid line: fitted by (5.10).

5.1.3. Model for the channel 1/*f* noise

The empirical expression of the Hooge mobility-fluctuation model [18], [95] is given as

$$\frac{S_{Id}(f)}{I_d^2} = \frac{\alpha_H}{fN} \tag{5.1}$$

with α_H the Hooge parameter and N the total number of carriers under the gate. For the studied SNWTs in the subthreshold region, N is generally smaller than 20. **This is the first time that the empirical expression (5.1) is tested for such a low *N*.**

The subthreshold current of the lightly-doped GAA SNWT can be expressed as [120]

$$I_d = \mu \frac{\pi R^2}{L} n_i kTe^{\frac{q(V_{gs}-\Delta\Phi)}{kT}} \left(1 - e^{-\frac{qV_{ds}}{kT}}\right) \tag{5.2}$$

where μ is the effective mobility, R the radius of the silicon core of the SNWT, L the channel length, n_i the intrinsic carrier concentration, and $\Delta\Phi$ the work function difference between the gate electrode and the almost-intrinsic silicon body.

From both the surface-potential expression ψ_s and Gauss's law applied at the Si/SiO_2 interface, a β-dependent expression $f(\beta)$ with β a parameter related to R and ψ_s is defined as [120]

$$f(\beta) = \frac{q}{kT}\left(V_{gs} - V_o - V(x)\right) \tag{5.3}$$

with

$$V_o = \Delta\Phi + \frac{kT}{q}\ln\left(\frac{8kT\varepsilon_{Si}}{q^2 n_i R^2}\right) \tag{5.4}$$

where $V(x)$ is the electron quasi-Fermi potential at x along the channel. In the subthreshold region, $\beta \sim 1$, $f(\beta) \sim \ln(1-\beta)$ [120], together with (5.3), $1-\beta$ can be derived as

$$1-\beta = e^{\frac{q}{kT}\left(V_{gs}-V_o-V(x)\right)}. \tag{5.5}$$

$Q_i(x)$, the carrier charge density per unit area at the channel position of x, is derived in [120] as

$$Q_i(x) = 4\frac{\varepsilon_{Si}}{R}\frac{kT}{q}\frac{1-\beta}{\beta}. \tag{5.6}$$

Since $\beta \sim 1$ in the subthreshold region, substituting (5.4) and (5.5) into (5.6), we have

$$Q_i(x) \approx 4\frac{\varepsilon_{Si}}{R}\frac{kT}{q}(1-\beta) = \frac{qn_iR}{2}e^{\frac{q}{kT}\left(V_{gs}-\Delta\Phi-V(x)\right)}. \tag{5.7}$$

Following the approach described in [49] and with the help of (5.2) and (5.7), the final expression of S_{Id}/I_d^2 for SNWTs in the subthreshold region is

$$\frac{S_{Id}(f)}{I_d^2} = \frac{\alpha_H}{fN} = \frac{\alpha_H}{f}\frac{2\mu kT}{L^2}\frac{1-e^{\frac{-qV_{ds}}{kT}}}{1+e^{\frac{-qV_{ds}}{kT}}}\frac{1}{I_d}. \tag{5.8}$$

Since the subthreshold slope of the p-type SNWT is not as ideal as that of the n-type one, two ideality factors m and m' related to the gate and drain biases, respectively, are added into (5.2) as

$$I_d = \mu\frac{\pi R^2}{L}n_i kTe^{\frac{q\left(|V_{gs}|-|\Delta\phi|\right)}{mkT}}\left(1-e^{-\frac{q|V_{ds}|}{m'kT}}\right) \tag{5.9}$$

which leads to the final mobility-fluctuation model in the subthreshold region as

$$\frac{S_{Id}(f)}{I_d^2} = \frac{\alpha_H}{fN} = m'\frac{\alpha_H}{f}\frac{2\mu kT}{L^2}\frac{1-e^{\frac{-q|V_{ds}|}{m'kT}}}{1+e^{\frac{-q|V_{ds}|}{m'kT}}}\frac{1}{I_d} \tag{5.10}$$

where m = 1, 1.1 and m' = 1, 1.03 for n- and p-type SNWTs, respectively. For SNWTs working in the Ohmic region with very low drain biases, (5.10) can be simplified as

$$\frac{S_{Id}(f)}{I_d^2} = \frac{\alpha_H}{fN} = \frac{\alpha_H}{f}\frac{q\mu}{L^2}|V_{ds}|\frac{1}{I_d}. \tag{5.11}$$

5.1.4. Model verification and Hooge parameter extraction

The effective mobility μ is approximated from the I–V data of the long-channel SNWTs and is around 150, 45, and 90 cm^2/Vs for n- and p-type SNWTs with the channel oriented in the <110> direction and p-type SNWTs in the <010> direction, respectively. From variations in Figure 5.2(b), α_H following (5.10) or (5.11) has been extracted to be $\alpha_H \approx 1.2\times10^{-4}$ and 7×10^{-5} for the n- and p-type SNWTs, respectively. α_H of p-type SNWTs is the same in the <110> and <010> directions, which means that α_H is independent of the channel orientations. The extracted Hooge parameters are within the range reported for conventional bulk-CMOS devices with the SiO_2/poly-Si gate stack and are close to the value predicted from the ITRS roadmap for 45-nm technology node [96].

S_{Id}/I_d versus V_{ds} for n- and p-type SNWTs in the subthreshold region is shown in Figure 5.3. A linear increase at low V_{ds} values is observed and a plateau is reached for high V_{ds} values ($S_{Id}/I_d = 1.88\times10^{-13}$ and 3.2×10^{-14} A/Hz for n- and p-type devices, respectively). The computed values of S_{Id}/I_d using (5.10) are also reported. Good

agreement is observed. The normalized drain-current noise S_{Id}/I_d^2 versus V_{ds} plotted in the inset of Figure 5.3 shows the similar behavior.

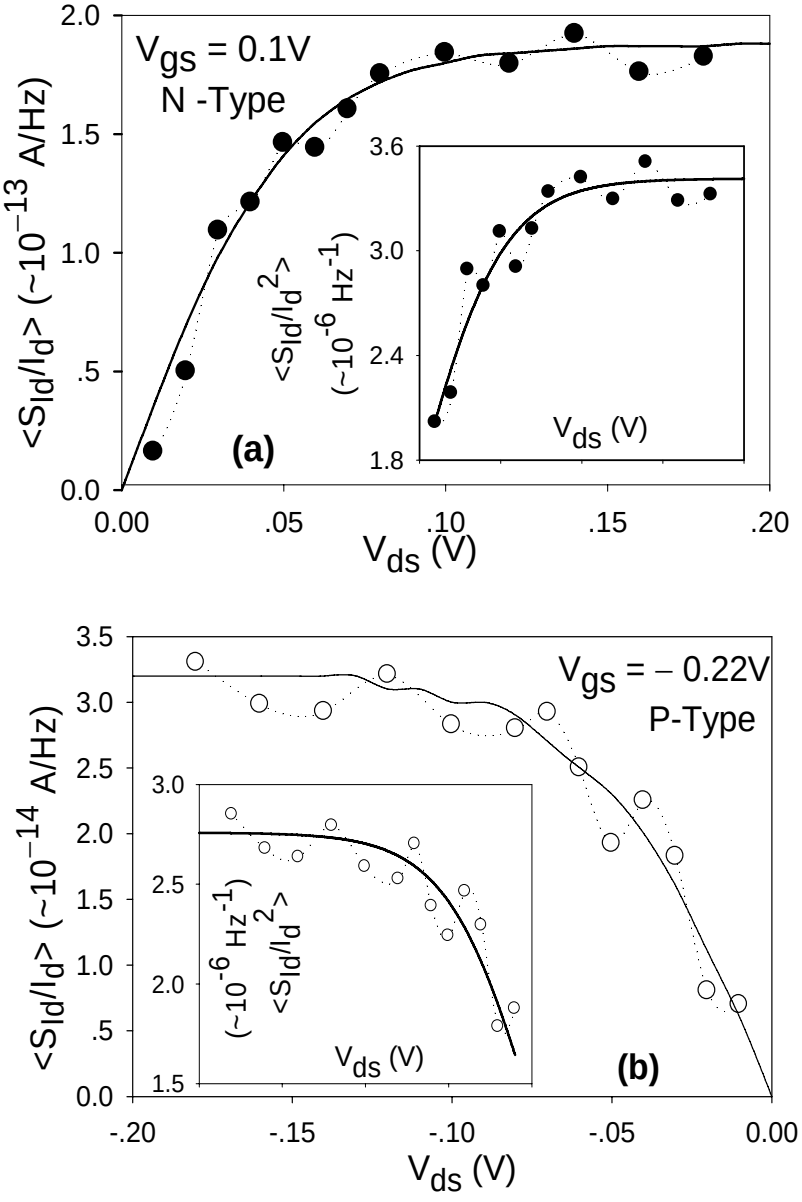

Figure 5.3: Variations of average S_{Id}/I_d at f = 10 Hz versus V_{ds} for (a) n- and (b) p-type SNWTs in the subthreshold region with L = 90 nm and the channel oriented in the <110> direction. Symbols: experimental data, Solid line: fitted by (5.10). The normalized noise $<S_{Id}/I_d^2>$ at the same bias range is shown in the inset in the respective case.

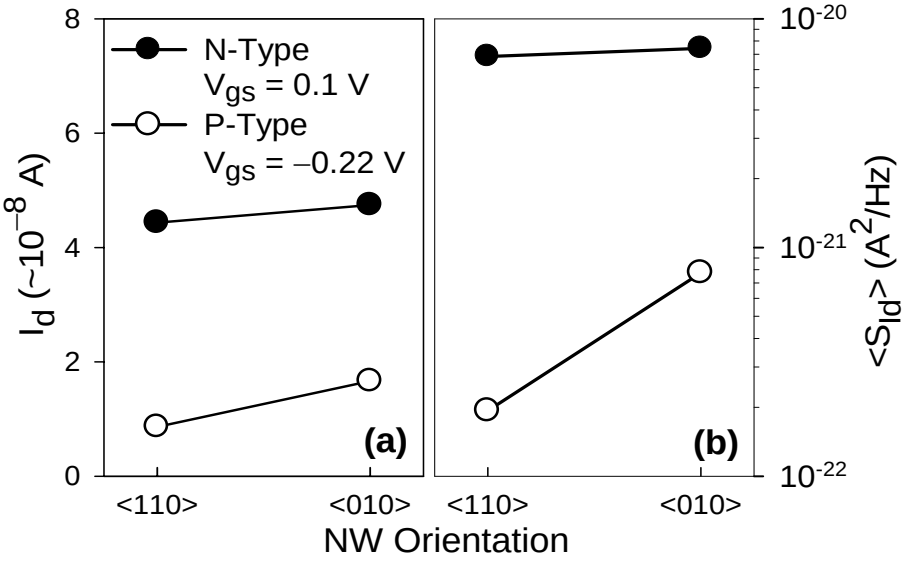

Figure 5.4: Impact of channel orientations of SNWTs on the (a) drain current I_d and (b) average drain-current noise spectral density $<S_{Id}>$ at $|V_{ds}|$ = 50 mV, f = 10 Hz and with the gate voltage fixed at 0.1 V and -0.22 V for n- and p-type SNWTs, respectively. The channel of SNWTs with L = 90 nm is oriented in the <010> or <110> direction.

5.1.5. Impact of channel orientations

The SNWTs with L = 90 nm have the channel oriented in the <110> and <010> directions, respectively. As indicated in Figure 5.1(b), for a fixed bias, there is no significant difference of the subthreshold current (or mobility) for n-type SNWTs in two different orientations. However, the subthreshold current (or mobility) for p-type devices in the <010> orientation is found to be 2.1 times that in the <110> orientation. The extrapolated I_d values at V_{gs} = 0.1 V and −0.22 V for n- and p-type SNWTs respectively are shown in Figure 5.4(a). From (5.10), it is seen that S_{Id} is proportional to μ in the channel for a given V_{ds} and I_d. Hence, as shown in Figure 5.2(b), the magnitude of S_{Id} for n-type SNWTs is almost the same in the <010> and <110> orientations, whereas the S_{Id} for p-type devices in the <010> orientation is about twice that in the <110> orientation. This actually confirms that the mobility-fluctuation mechanism is dominant in the subthreshold region, because in the number-

fluctuation model there is no dependence of S_{Id} on the mobility at a fixed drain-current level [41]. Moreover, for a given V_{ds}, if V_{gs} is fixed instead of the drain current I_d, it is expected from (5.9) and (5.10) that S_{Id} is proportional to μ^2. The measurement data shown in Figure 5.4(b) agrees with the prediction from the mobility-fluctuation model: S_{Id} of p-type SNWTs with the channel oriented in the <010> direction is almost four times that in the <110> direction. As a result, a stronger drain current and mobility enhancement observed in certain channel orientation may also cause a higher LFN level in the corresponding orientation. This would be a tradeoff for future applications of SNWTs.

5.2. Low-frequency noise in strong inversion with different gate electrodes

5.2.1. Device and dc measurement

The details of the fabrication process are similar to the ones reported in section 5.1.1 [113], [114] except that the gate FUSI step is included for cetain wafer splits. The implantation and RTA activation of the gate and source/drain (S/D) were all performed prior to the gate FUSI process. By employing a reverse gate mask, the S/D regions were blocked from the silicidation by the SiN/oxide hard mask layer. A single step NiSi FUSI process fully silicided the gate. An RTA soak anneal at 420ºC was used in order to fully silicide the GAA structure. The wafers were split into three categories after the step of α-Si gate stack deposition: only wafers designed for SNWTs with the conventional poly-Si gate or doped-FUSI gate went through the gate dopant implantation and annealing step. Then the complete gate silicidation with Ni was only done for the doped- and undoped-FUSI gate wafer splits. Figure 5.5 shows the schematics and the details on the dopant type and dose of the three wafer splits

with different gate electrodes: (a) poly-Si gate, (b) undoped-FUSI gate, and (c) doped-FUSI gate. Gate doping dose for the wafer split with the poly-Si gate was adjusted to match that with the doped-FUSI gate. The schematic of the GAA SNWT is the same as that shown in Figure 5.1(a). The thickness of the SiO_2 gate dielectric is 4 nm, the Si core has a diameter d_{nw} of ~10 nm, and the gate length L of the investigated SNWTs is 0.35 μm.

The I_d–V_{gs} transfer characteristics of both n- and p-type SNWTs at $|V_{ds}|$ = 50 mV are shown in Figure 5.6. It shows that the poly-Si and undoped-FUSI gate electrodes set the magnitude of V_T too low (n-type: 0.03 V, p-type: –0.02 V) and too high (n-type: 0.46 V, p-type: –0.65 V), respectively. The work function of the FUSI gate was tuned by using the Phosphorus (dose: 3×10^{15} cm^{-2}) and Boron (dose: 3×10^{15} cm^{-2}) pre-doping of the poly-Si for n- and p-type SNWTs, respectively; and therefore, the optimum V_T values (n-type: 0.26 V, p-type: –0.25 V) were obtained.

The 1/*f* noise measurements were then performed by using two battery-powered SR570 Low-Noise Current Preamplifiers and one HP35670A Dynamic Signal Analyzer to obtain the frequency spectrum.

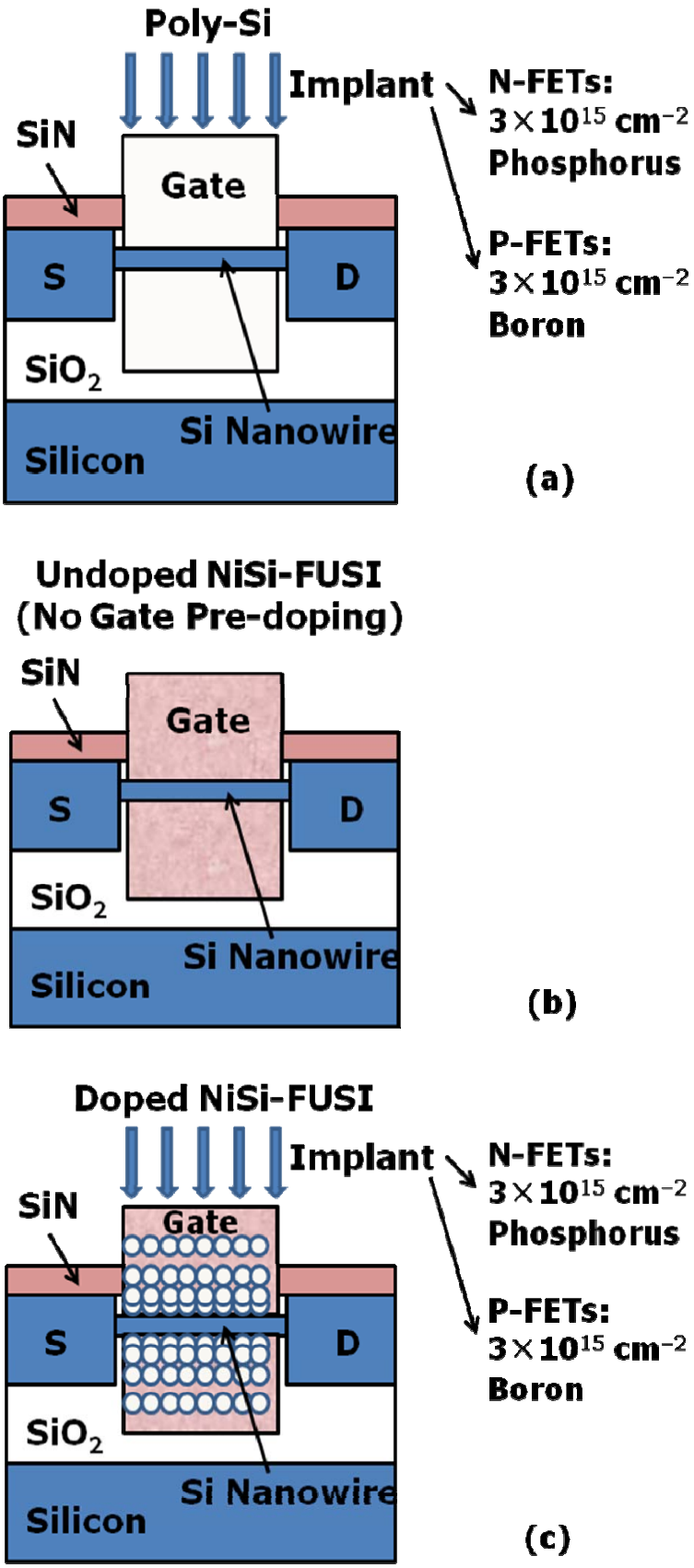

Figure 5.5: Schematic plots of three SNWT wafer splits: (a) The split has the conventional implantation-doped poly-Si gate. (b) The split has the NiSi-FUSI gate without any prior gate implantation. (c) The split has the NiSi-FUSI gate with the gate pre-doped via the implantation for the gate workfunction tuning.

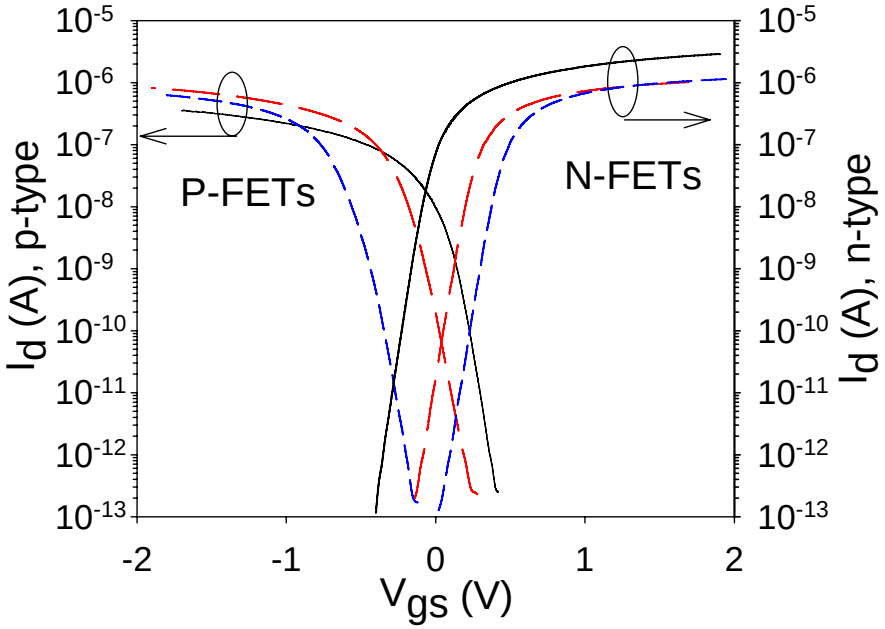

Figure 5.6: I_d vs. V_{gs} of both n- and p-type SNWTs with three different gate electrodes at $|V_{ds}| = 50$ mV. Solid line: poly-Si gate, Long dash line: doped-FUSI gate, Short dash line: undoped-FUSI gate.

5.2.2. Measurement results and discussion

Figure 5.7(a) shows the frequency dependence of the measured drain-current noise spectral density S_{Id} of seven samples of n-type SNWTs with the doped-FUSI gate, biased at $V_{ds} = 50$ mV and $I_d = 8.3\times10^{-7}$ A. The dispersion of the noise spectra is around one decade and the observed device-to-device variations are due to the statistical fluctuation of the number of oxide traps in the ultra-scaled SNWTs with the gate area on the order of 0.01 μm^2 [8], [38]. Although one or two humps are observed in certain individual noise curves, the sum of the noise spectral density of seven samples follows a $1/f^{\gamma}$ dependence with $\gamma = 1.08$, where γ is the frequency exponent. The average drain-current noise spectral density $<S_{Id}>$ vs. frequency f at $I_d = 8.3\times10^{-7}$ A for n-type SNWTs with all three different gate electrodes are shown in the inset of

Figure 5.7(a). The averaged results of the noise spectral density are used in the following discussion.

Figure 5.7(b) and (c) show the average normalized drain-current noise spectral density $<S_{Id}/I_d^2>$ at f = 10 Hz as a function of I_d at $|V_{ds}|$ = 50 mV for n- and p-type SNWTs, respectively, and the plots of $(g_m/I_d)^2$ (g_m is the transconductance $\partial I_d/\partial|V_{gs}|$) vs. I_d are shown correspondingly for comparison. For both types of SNWTs with the undoped-FUSI gate, the observed S_{Id}/I_d^2 is largely proportional to $(g_m/I_d)^2$ in the entire I_d range measured, which indicates that the $1/f$ noise of these devices is consistent with the carrier-number-fluctuation model including the correlated mobility fluctuation, and the carrier trapping/detrapping process near the Si/SiO_2 interface is the dominant noise generation mechanism with negligible correlated mobility scatterings [38], [42]. While for both types of SNWTs with the poly-Si gate or doped-FUSI gate, there are slope deviations observed between the S_{Id}/I_d^2 and $(g_m/I_d)^2$ curves, which means that the correlated mobility scattering is more significant in these two kinds of devices, especially the ones with the poly-Si gate.

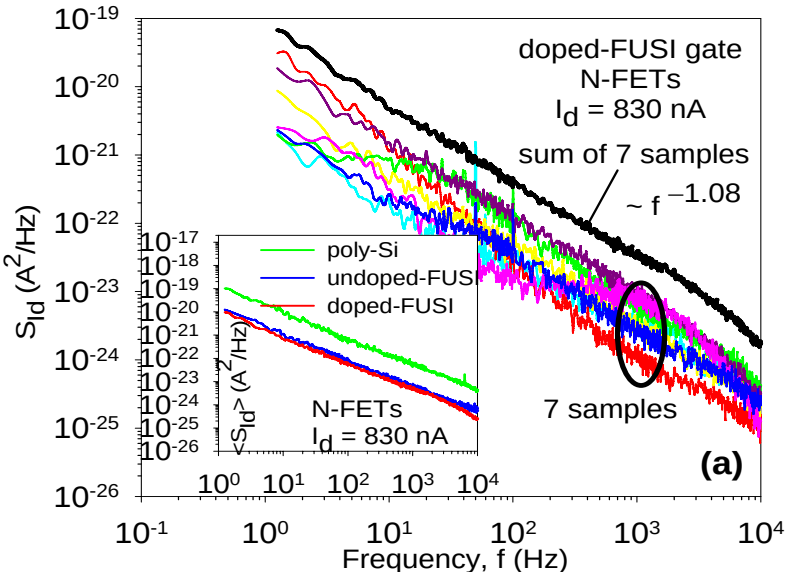

Figure 5.7: (a) S_{Id} vs. f of seven individual n-type SNWTs with the doped-FUSI gate biased at V_{ds} = 50 mV and constant $I_d = 8.3\times10^{-7}$ A, and the sum shows a typical $1/f^{\gamma}$ behavior with γ = 1.08. Average $<S_{Id}>$ vs. f at $I_d = 8.3\times10^{-7}$ A for n-type SNWTs with all three different gate electrodes are shown in the inset.

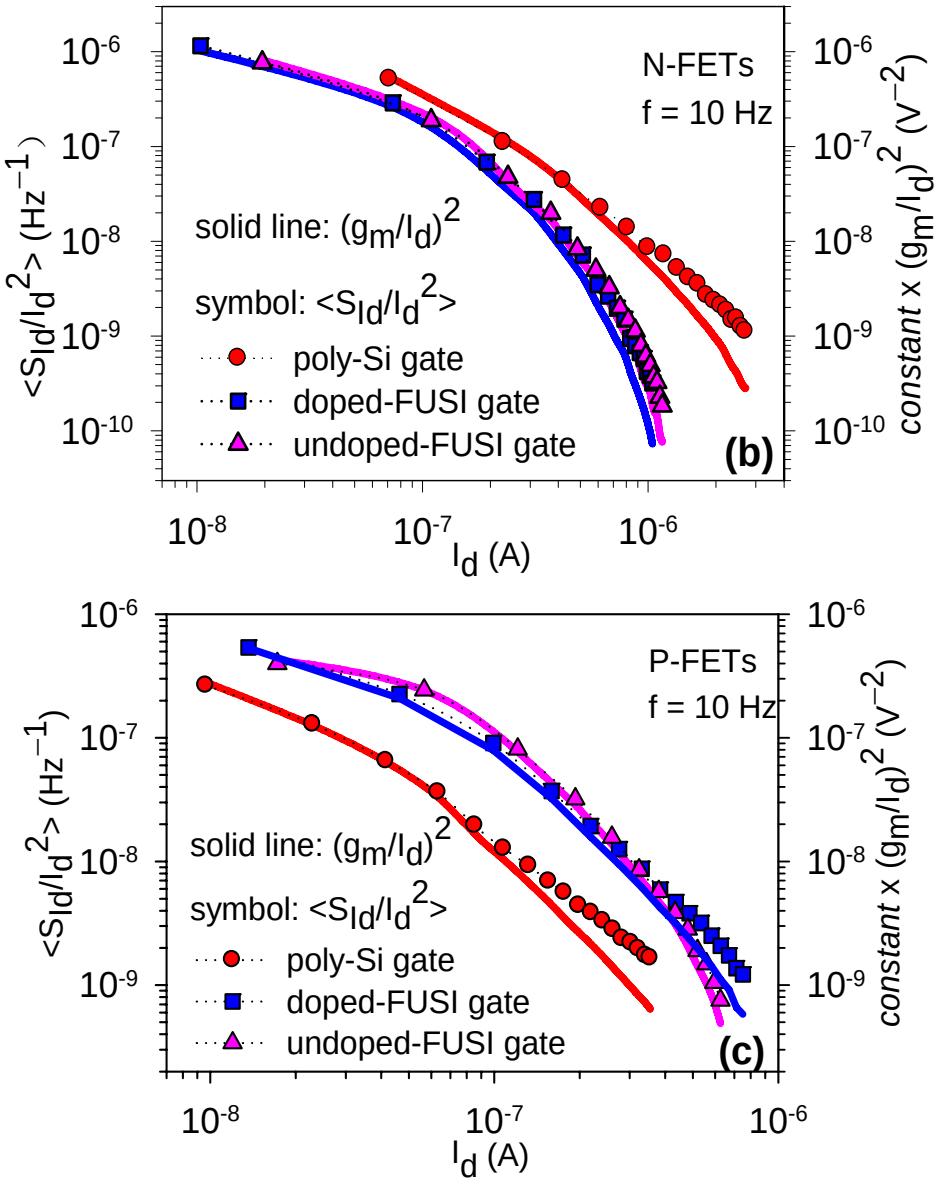

Figure 5.7 (cont.): (Symbols) $<S_{Id}/I_d^2>$ vs. I_d of (b) n-type and (c) p-type SNWTs with three different gate electrodes at $|V_{ds}|$ = 50 mV and f = 10 Hz. The noise data is compared with the corresponding plots of (*constant* × $(g_m/I_d)^2$) vs. I_d drawn by solid lines.

For the carrier-number fluctuation model including the correlated mobility fluctuation [42], [121], the gate-voltage-referred noise spectral density is given by

$$S_{V_g} = S_{V_{fb}}[1 + \alpha\mu_o C_{ox}|V_{gs} - V_T|]^2 \tag{5.12}$$

$$\sqrt{S_{V_g}} = \sqrt{S_{V_{fb}}}[1 + \alpha\mu_o C_{ox}|V_{gs} - V_T|] \tag{5.13}$$

with α the scattering coefficient, μ_o the low-field mobility, C_{ox} the gate oxide capacitance per unit area, and S_{Vfb} the flatband-voltage noise spectral density associated with the near-interface charge fluctuations, given as

$$S_{V_{fb}} = \frac{\lambda kTq^2 N_t}{f^\gamma WLC_{ox}^2} \tag{5.14}$$

where λ is the tunneling attenuation length, W the effective channel width ($W = \pi d_{nw}$ is used in the calculation), and N_t the oxide trap density ($eV^{-1}cm^{-3}$).

Figure 5.8(a) and (b) show the plots of $<S_{Vg}>^{1/2}$ measured at $f = 10$ Hz versus the gate voltage overdrive ($V_{gs} - V_T$) for n- and p-type SNWTs, respectively. A discernible slope difference is observed among the noise curves for three different gate electrodes. The SNWTs with the undoped-FUSI gate exhibit the flattest slope, indicating the insignificant correlated mobility fluctuations, whereas a pronounced linear increase of $<S_{Vg}>^{1/2}$ with respect to ($V_{gs} - V_T$) is noticed for SNWTs with the poly-Si gate. The strong gate-voltage dependences confirm that in strong inversion the noise induced by the correlated mobility scattering is most significant in SNWTs with the poly-Si gate, and then doped-FUSI gate, compared to the counterparts with the undoped-FUSI gate. Moreover, for SNWTs with $R_S(g_{mi} + 2g_{OUTi}) << 1$, where R_S is the series resistance of the source or drain side, g_{mi} and g_{OUTi} are the intrinsic transconductance and output conductance, respectively, when the effect of series resistances is significant, the trend of $(S_{Vg})^{1/2}$ being proportional to $(V_{gs} - V_T)^2$ can be observed with the SNWTs biased at constant V_{ds} [38]. This is not the case in Figure 5.8. Hence, the effect of series resistances is insignificant in the drain-current range investigated.

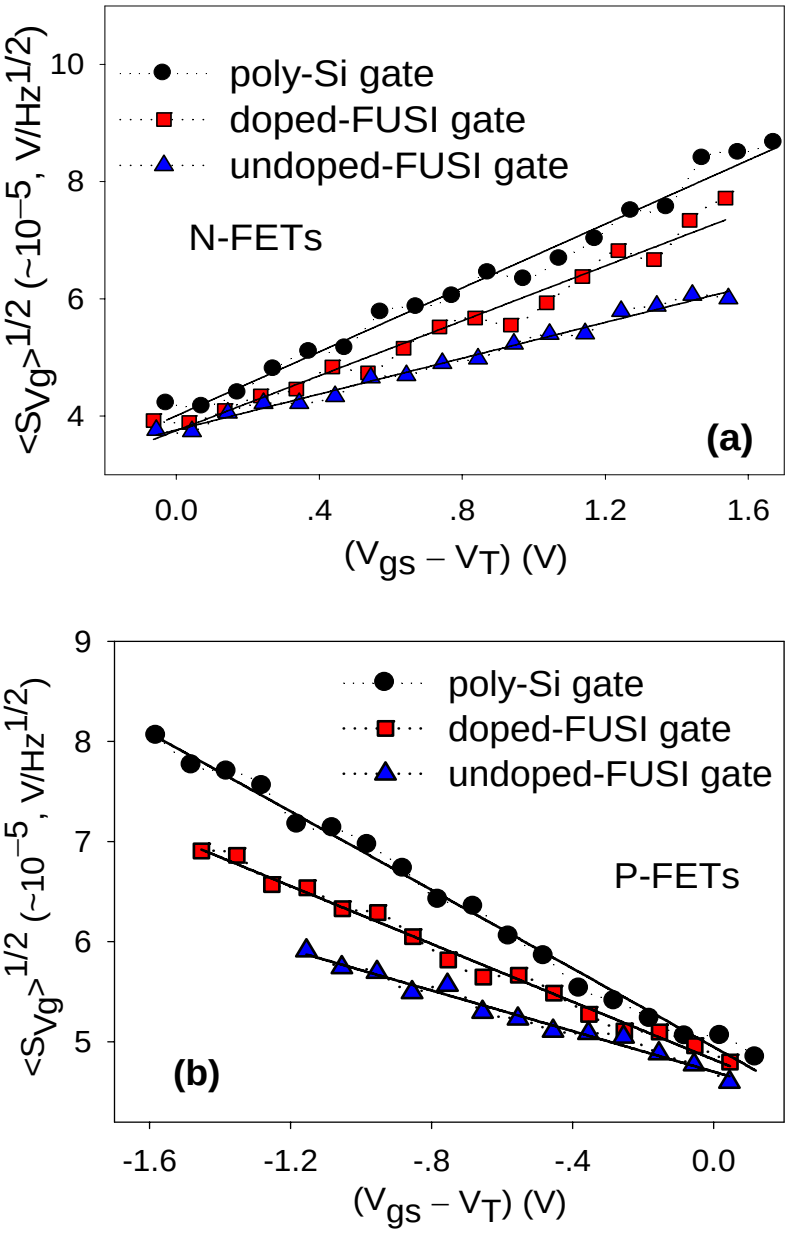

Figure 5.8: Symbols are measured $\langle S_{Vg}\rangle^{1/2}$ vs. $(V_{gs} - V_T)$ of (a) n-type and (b) p-type SNWTs with three different gate electrodes at $|V_{ds}| = 50$ mV and $f = 10$ Hz. The solid lines are fitting curves by (5.13).

5.2.3. Noise parameters extraction

With the values of $\mu_o C_{ox}$ being extracted from the I_d–V_{gs} curves and C_{ox} being calculated from the capacitance measured on the test structure of 1000 parallel

SNWTs (Table 2) and from Figure 5.8, the average values of N_t and α are extracted using (5.12)–(5.14) for the respective devices and are listed in Table 3.

Table 2: The dc parameters needed for the noise parameters extraction.

	poly-Si	doped-FUSI	undoped-FUSI
$\mu_o C_{ox}$ (F/Vs)	**N:** 2.1×10^{-4} **P:** 5.6×10^{-5}	**N:** 4.4×10^{-4} **P:** 7.0×10^{-5}	**N:** 4.3×10^{-4} **P:** 1.4×10^{-4}
C_{ox} (F/cm^2)	**N:** 1.2×10^{-6} **P:** 1.2×10^{-6}	**N:** 1.7×10^{-6} **P:** 1.4×10^{-6}	**N:** 1.7×10^{-6} **P:** 1.4×10^{-6}

Table 3: The extracted equivalent oxide-trap density and scattering coefficient of SNWTs with three different gate electrodes.

	poly-Si	doped-FUSI	undoped-FUSI
N_t (eV^{-1}cm^{-3})	**N:** 3.7×10^{17} **P:** 5.6×10^{17}	**N:** 6.8×10^{17} **P:** 7.4×10^{17}	**N:** 6.8×10^{17} **P:** 7.0×10^{17}
α (Vs/C)	**N:** 3.2×10^{3} **P:** 7.1×10^{3}	**N:** 1.4×10^{3} **P:** 4.3×10^{3}	**N:** 9.5×10^{2} **P:** 1.5×10^{3}

The extracted values of N_t are comparable to those reported for bulk-CMOS devices but are close to the high-end of the data range [96]. They are also on the same order and comparable to each other for three different gate electrodes. These results indicate that the dielectric quality is not degraded by the gate FUSI process. Moreover, the tunneling depth z at which the traps in the oxide are probed is determined by the measurement frequency f as

$$\frac{1}{2\pi f} = \tau_o \exp(z/\lambda) \tag{5.15}$$

where τ_o is the time constant at the Si/SiO_2 interface and in the range of 10^{-14} to 10^{-10} s and λ is the tunneling attenuation length (0.1 nm) predicted by the Wentzel-Kramers-Brillouin (WKB) approximation. From (5.15), for f from 1 to 10k Hz and τ_o in the range of 10^{-14} to 10^{-10} s, the depths of oxide traps probed are not beyond 3 nm. This implies that the traps located at the gate/SiO_2 interface (z = 4 nm) are not participating directly in the trapping/detrapping process with the channel.

In contrast, different values of α extracted reveal that the impact of different gate electrodes on the correlated mobility fluctuation is responsible for the observed slope difference in Figure 5.8. The use of the metal gate with a high electron concentration induces a more complete screening of both the insulator phonon modes [122], [123] and the Coulombic scattering induced by the charges trapped in the oxide and their related image charges [124]. Whereas the strongly-depleted layer of the poly-Si gate containing a very low carrier concentration is less effective in screening the phonon and Coulomic scatterings in the oxide, actually it may even anti-screen them through the long-range Coulombic scattering [125]. Hence, the negligible correlated mobility fluctuation is observed in SNWTs with the undoped-FUSI metal-gate compared to those with the poly-Si gate. However, once the FUSI gate is pre-doped, the correlated mobility fluctuation is still observable. This may be due to the existence of sub-monolayer amounts of impurities segregated at the gate/SiO_2 interface [115]. The electro-negativity difference between each segregated impurity and the oxide in the SiO_2 dielectrics induces an interface charge dipole, as shown in Figure 5.9. These high-density electric dipoles may counteract the screening efficiency of the FUSI metal-gate and, thus, the correlated mobility fluctuation is observed in SNWTs with the doped-FUSI gate.

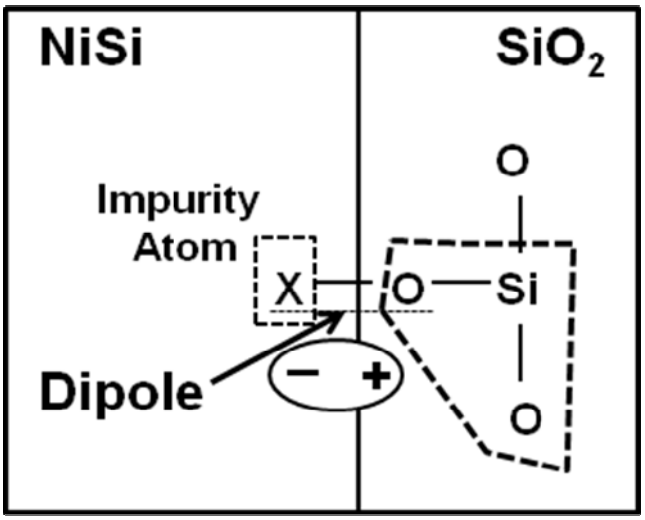

Figure 5.9: Electric dipole model at the NiSi/SiO_2 interface. *X* stands for the impurity atom that composes the impurity segregation.

It worths mentioniong that there may be trapped charges detrapping towards the gate. This may influence the measured drain-current fluctuation in two ways. In the number-fluctuation process regarding the charge interactions between the channel and oxide traps, this may be revealed as the increase of the emission time of the oxide trap seen by the channel, since the charge is emit from the oxide trap towards the gate and not returned to the channel. In the correlated-mobility process, the charges detrapped towards the gate may also influence the channel mobility as they did when they were trapped in the oxide, but the extent of the influence may be different due to different distance from the channel. More detailed design of experiments can be carried out in the future to elaborate on this point and estimate the percentage of the number and correlated mobility fluctuations that are influenced by this process of detrapping towards gate for different gate electrodes.

5.3. Low-frequency noise characterizations of the robustness of FinFETs and SNWTs to the oxide trap generation under the FN tunneling stress

5.3.1. Device and dc measurement

The details of the fabrication process of the n-channel poly-Si-gate DG FinFET and GAA SNWT are similar to the ones reported in section 4.1 and 5.1.1, respectively. The schematics of the FinFET and SNWT can be obtained from Figure 4.1(a) and Figure 5.1(a), respectively. The thickness of the SiO_2 gate dielectric t_{ox} and the gate length L for both device architectures are 4 nm and 0.35 μm, respectively. The Si core of the SNWT has a diameter d_{nw} of ~10 nm. The fin height H_{fin} and fin width t_{si} of the DG FinFET is 0.12 μm and 40 nm, respectively. The test structure in this study has 100 parallel individual SNWTs and FinFETs.

The current–voltage characterization and the FN tunneling stress of the devices were performed using an Agilent 4156C Semiconductor Parameter Analyzer. The 1/*f* noise measurements were performed using two battery-powered SR570 Low-Noise Current Preamplifiers and one HP35670A Dynamic Signal Analyzer to obtain the frequency spectrum. During the constant-voltage FN tunneling stress, the stress voltage V_G was applied to the gate electrode while keeping the source/drain grounded. In order to investigate the effect of the FN tunneling stress on the 1/*f* noise, the noise measurement and the FN tunneling stress application were alternately performed. After each FN tunneling stress cycle, both the drain current I_d and the 1/*f* noise were monitored. The evolutions of the transfer characteristics I_d–V_{gs} at the drain voltage V_{ds} = 50 mV were measured as a function of the FN tunneling stress time at V_G = 4.5 and – 4.5 V in the respective cases. The threshold voltage shift ΔV_T versus the stress time t is reported in Figure 5.10. The I_d–V_{gs} plot of the SNWT before and after the FN

tunneling stress at $V_G = -4.5$ V is shown in the inset. The negative V_T shift suggests the positive charges built up in the gate oxide.

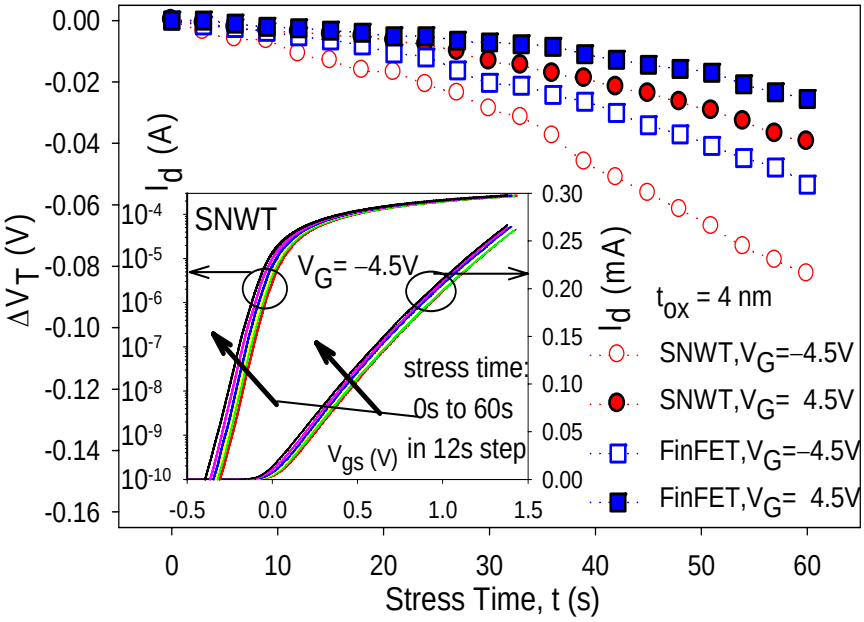

Figure 5.10: Threshold voltage shift as a function of the FN tunneling stress time. The inset shows the I_d-V_{gs} plot of the SNWT subject to the FN tunneling stress at $V_G = -4.5$ V with the stress time increasing from 0 s to 60 s in a 12-s step.

5.3.2. Measurement results and discussion

The impact of the FN tunneling stress on the 1/*f* noise is studied for both FinFETs and SNWTs. The drain-current noise spectral density S_{Id} was investigated at $V_{ds} = 50$ mV and with V_{gs} varying in the strong-inversion region, before and after the FN tunneling stress. As reported in section 5.2.2, the 1/*f* noise in this region follows the number-fluctuation model with the correlated mobility fluctuation [42], in which S_{Id} can be expressed as $S_{Id}/(g_m)^2 = S_{Vg} = S_{Vfb}[1 + \alpha\mu_o C_{ox}(V_{gs} - V_T)]^2$, with $S_{Vfb} = \lambda kTq^2 N_t/(WLC_{ox}^2 f)$, where all the symbols take their usual meanings. At $(V_{gs} - V_T) = 0$, and at fixed values of V_{ds} and f, S_{Id} is proportional to N_t. Hence, the change of the 1/*f* noise can be translated to the change of N_t. The initial near-interface oxide-trap density

$N_t(0)$ extracted for all the devices before the FN tunneling stress is on the order of 10^{17} $eV^{-1}cm^{-3}$.

The fresh devices of both FinFETs and SNWTs were stressed at different stress times t and at V_G = 4.5 and – 4.5 V in the respective cases. $\Delta N_t(t) = N_t(t) - N_t(0)$ represents the increase of the near-interface oxide-trap density after stressing for a time t. The normalized increase $\Delta N_t(t)/N_t(0)$ as a function of the stress time t is shown in Figure 5.11. The evolution of S_{Id} versus f for the SNWT before and after the FN tunneling stress at V_G = –4.5 V with the increase of the stress time is correspondingly shown in the inset. Apparently, the 1/f-type nature of the power spectral density is preserved during the stress application. The 1/f noise, which is translated to the near-interface oxide-trap density, increases only at the beginning of the stress time and tends to saturate after a short period of time around 10s. Compared to the V_T shift under the same stress condition in Figure 5.10, in which hole-traps in general keep being created as the FN tunneling stress continues. It suggests that the created oxide traps responsible for the V_T shift are not completely involved in the 1/f noise generation mechanism. The relationship between the threshold voltage V_T and the gate oxide charge density per unit volume Q_{ox} is as

$$V_T = OtherTerms - \left(\int_0^{t_{ox}} \frac{Q_{ox}}{\varepsilon_{ox}} (t_{ox} - z) dz \right) \tag{5.16}$$

where t_{ox} is the gate oxide thickness, z the direction perpendicular to the Si/SiO_2 interface with the starting point z = 0 at the Si/SiO_2 interface and end point $z = t_{ox}$ at the gate/oxide interface, and ε_{ox} the permittivity of oxide. Hence all the oxide charges within the gate oxide may contribute to the V_T shift. The oxide charges involve in the 1/f noise depending on the probing frequency f as explained by (5.15). For f from 1 to

10k Hz, the depths of oxide traps probed are not beyond 3nm. The extracted oxide-trap density from the 1/*f* noise is thus called near-interface oxide-trap density N_t. It does not mean all the oxide-traps inside the gate oxide. Hence the oxide-traps contribute to V_T shift may not be completely involved in the 1/*f* noise probed.

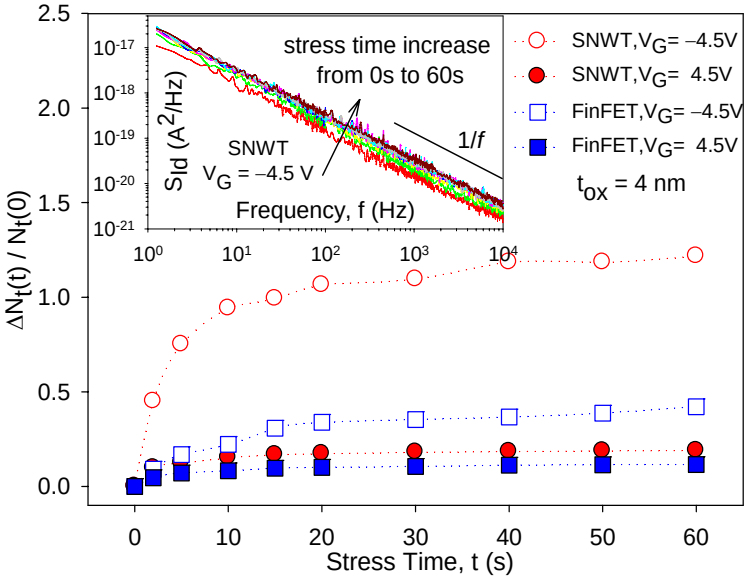

Figure 5.11: Variations of the normalized increase of the oxide-trap density ($\Delta N_t(t)/N_t(0)$) after different stress times (*t*). The corresponding evolution of S_{Id} versus *f* for the SNWT, from which the oxide-trap density is extracted, before and after the FN tunneling stress at $V_G = -4.5$ V with the increase of the stress time is shown in the inset.

The constant-voltage ($V_G > 0$ or $V_G < 0$) stress was also applied on the fresh FinFETs and SNWTs with $|V_G|$ increasing from 3 V to 6.5 V in a step of 0.5 V for studying the generation of oxide traps induced by FN tunneling. At each V_G, the device was stressed for 50s. The 1/*f* noise measurements were carried out before and after stressing at each V_G. $\Delta N_t(V_G) = N_t(V_G) - N_t(V_G - 0.5\ \text{V})$ represents the change of the near-interface oxide-trap density caused by each V_G. $|V_G| = 3$ V is used as the starting point for calculating the increase of near-interface oxide-trap density for $|V_G| = 3.5$ V,

because no increase of near-interface oxide traps is observed at $|V_G|$ = 3 V and below, as observed in Figure 5.12 that $\Delta N_t(V_G = 3\ V) = N_t(V_G = 3\ V) - N_t(V_G = 2.5\ V) = 0$. The value of V_{ox} at $|V_G|$ = 3.5 V and beyond is above 3.2 V which corresponds to the band conduction offset between Si and SiO_2 and FN tunneling occurs. For inversion, V_{ox} at V_G = 3.5 V can be approximately calculated by taking into account the flatband voltage V_{fb} and the silicon body potential $2\Phi_F$ as [127]: $V_{ox} = V_G - V_{fb} - 2\Phi_F \approx V_G - \Phi_{MS} - 2\Phi_F = 3.5 - (-0.56) - 0.575 = 3.48$ V, where Φ_F is the potential difference between the midgap position and the Fermi level in the silicon body and Φ_{MS} is the workfunction difference between the gate electrode and silicon body. For accumulation, V_{ox} at $V_G = -3.5$ V is calculated as [127]: $V_{ox} = V_G - V_{fb} - 0.55 + \Phi_F \approx -3.5 - (-0.56) - 0.55 + 0.2877 = -3.21$ V. The normalized change $\Delta N_t(V_G)/N_t(V_G - 0.5\ V)$ is plotted as a function of $|V_G|$ in Figure 5.12. The positive $\Delta N_t(V_G)$ means that the near-interface oxide-trap density increases continuously with $|V_G|$, which is most likely due to the increase of the carrier-injection probability with the gate oxide field [126]. For the FinFET and SNWT under $V_G < 0$ FN tunneling stress, $\Delta N_t(V_G)/N_t(V_G - 0.5\ V)$ increases with increasing $|V_G|$ until it reaches a maximum and then it decreases. This means that $\Delta N_t(V_G)$ may become saturated or decrease as $|V_G|$ increases. The saturation or decrease of $\Delta N_t(V_G)$ is possibly due to the factor that injected current decreases because of decrease of terminal field due to electron trapping in the gate oxide. On the other hand, the total near-interface oxide-trap density N_t increases continuously with $|V_G|$. Therefore, the plotting of $\Delta N_t(V_G)/N_t(V_G - 0.5\ V)$ will create peak structures [127].

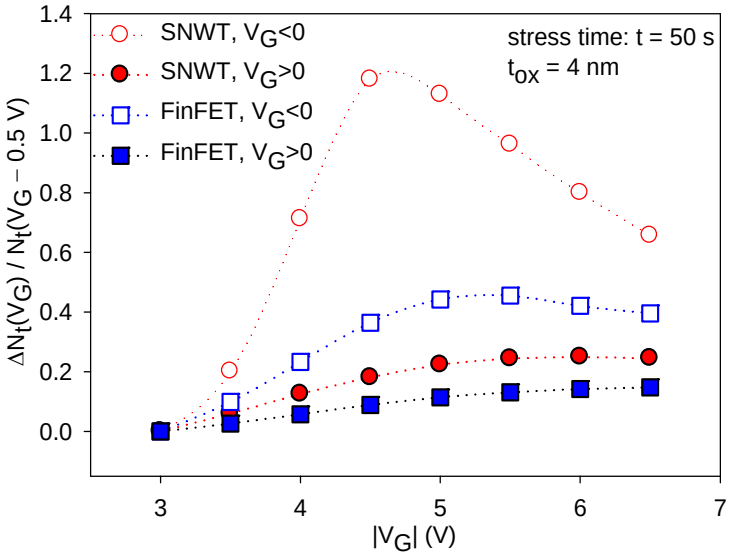

Figure 5.12: The normalized change of the oxide-trap density after stressing at each V_G ($\Delta N_t(V_G)/N_t(V_G - 0.5\ V)$) as a function of the amplitude of the stress voltage ($|V_G|$). The stress time at each V_G is 50s.

As shown in both Figure 5.11 and Figure 5.12, for a given polarity and magnitude of the stress voltage V_G and a given stress time t, the amount of the near-interface oxide traps generated in the cylindrical-channel SNWT is always much larger than that in the planar-channel FinFET. The increased efficiency of the oxide-trap generation in SNWTs is investigated through device simulations. The simulated electric fields of both the FinFET and SNWT with the gate biased at 4.5 and –4.5 V, respectively, before the FN tunneling stress, are shown in Figure 5.13. The cylindrical geometry enhances the electric field at the SiO_2/Si interface of the SNWT, which is nearly 1.6 times that of the planar-channel FinFET. The large vertical electric field at the SiO_2/Si interface enhances the carrier-injection probability, and thus, increases the efficiency of the oxide trap generation. The cylindrical-channel SNWT is therefore more vulnerable to the oxide-trap generation than the planar-channel FinFET. This observation could be more understandable through a simple calculation. Apply Gauss'

Law from the Si/SiO_2 interface to the center of Si body per unit gate area, we have $Q_i/\varepsilon_{si} = -E$, where Q_i is all the charges inside this Gauss box, ε_{si} the permittivity of silicon and E the vertical electric field at the Si/SiO_2 interface. For the charge balance of the whole device, $Q_i = -Q_G = -C_{ox}V_{ox}$, where Q_G is the gate charges per unit gate area, C_{ox} is the gate oxide capacitance per unit gate area and V_{ox} is the voltage across the gate oxide. Finally, $E = C_{ox}V_{ox}/\varepsilon_{si}$ is obtained. For FinFET, $C_{ox} = \varepsilon_{ox}/t_{ox}$, while for SNWT, $C_{ox} = \varepsilon_{ox}/(R\ln(1+t_{ox}/R))$ [128], where ε_{ox} is the permittivity of oxide, t_{ox} the gate oxide thickness and R the radius of the Si body of SNWT. For a given external bias and gate oxide thickness, E for FinFET is proportional to $1/t_{ox}$, while E for SNWT is proportional to $1/(R\ln(1+t_{ox}/R))$. In this study t_{ox} = 4nm, $R \approx$ 5nm, $1/(R\ln(1+t_{ox}/R)) \approx 0.34\ nm^{-1} > 1/t_{ox} = 0.25\ nm^{-1}$. It is obviously shown that the electric field is enhanced in the cylindrical-channel SNWT.

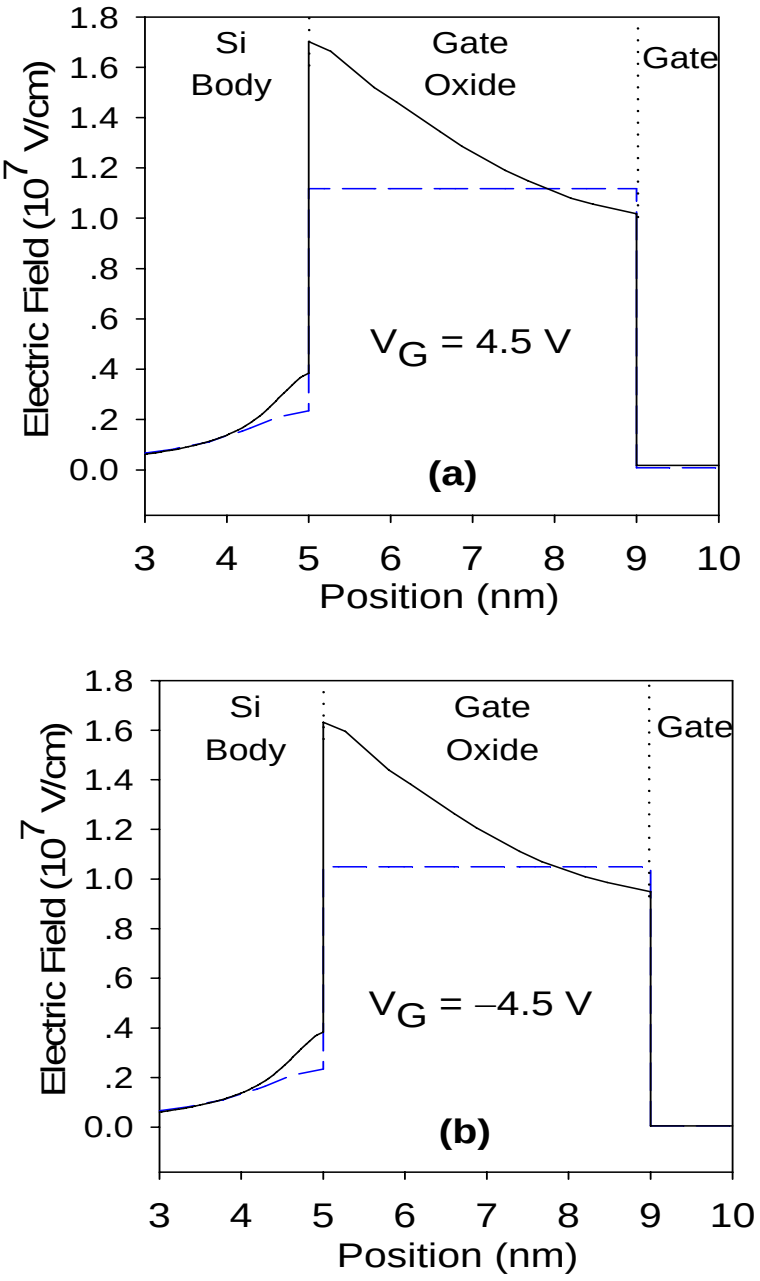

Figure 5.13: Simulated electric field distribution of the cylindrical-channel SNWT (solid line) and the planar-channel FinFET (short-dashed line) at (a) V_G = 4.5 V and (b) V_G = – 4.5 V.

It is worth mentioning that the cylindrical architecture also has an impact on the barrier width for tunneling as observed in the simulated potential-energy profiles in Figure 5.14. In the present case, the band width difference is not so significant because the terminal voltage and the barrier height determined by the band offset between SiO_2

and Si are fixed for both the FinFET and SNWT. However, once the FinFET or SNWT is built into the SONOS-type NVM cells, the barrier width of the SNWT-based cell is reduced to nearly half of that of the FinFET-based cell [117].

Another observation in Figure 5.11 and Figure 5.12 is that for both FinFETs and SNWTs, the increase of the near-interface oxide traps induced under $V_G < 0$ FN tunneling stress is much larger than that under $V_G > 0$ FN tunneling stress. This observation is well explained in the literature [129]: In the case of $V_G > 0$ FN tunneling stress, electrons are injected from the silicon body by FN tunneling, and gain energy from the oxide field. The electron-hole pairs are generated by the high-energy tail hot electrons in the heavily-doped poly-Si gate and most of them are quickly recombined [129]. While in the case of $V_G < 0$ FN tunneling stress, electrons are injected from the gate by FN tunneling through the oxide conduction band. Electrons are also accelerated by the oxide field and gain the kinetic energy. The hot electrons colliding with Si atoms at the SiO_2/Si interface produce the electron-hole pairs by the impact ionization [129]. The generated hot holes are injected back to the oxide by the gate potential, and cause the generation of the oxide traps close to the SiO_2/Si interface [130]. Hence, the generation of the oxide traps that contribute to the 1/*f* noise, namely, the near-interface oxide traps, is more severe under $V_G < 0$ FN tunneling stress than that under $V_G > 0$ FN tunneling stress. The FN tunneling processes at $V_G = 4.5$ and –4.5 V are indicated in Figure 5.14(a) and (b), respectively.

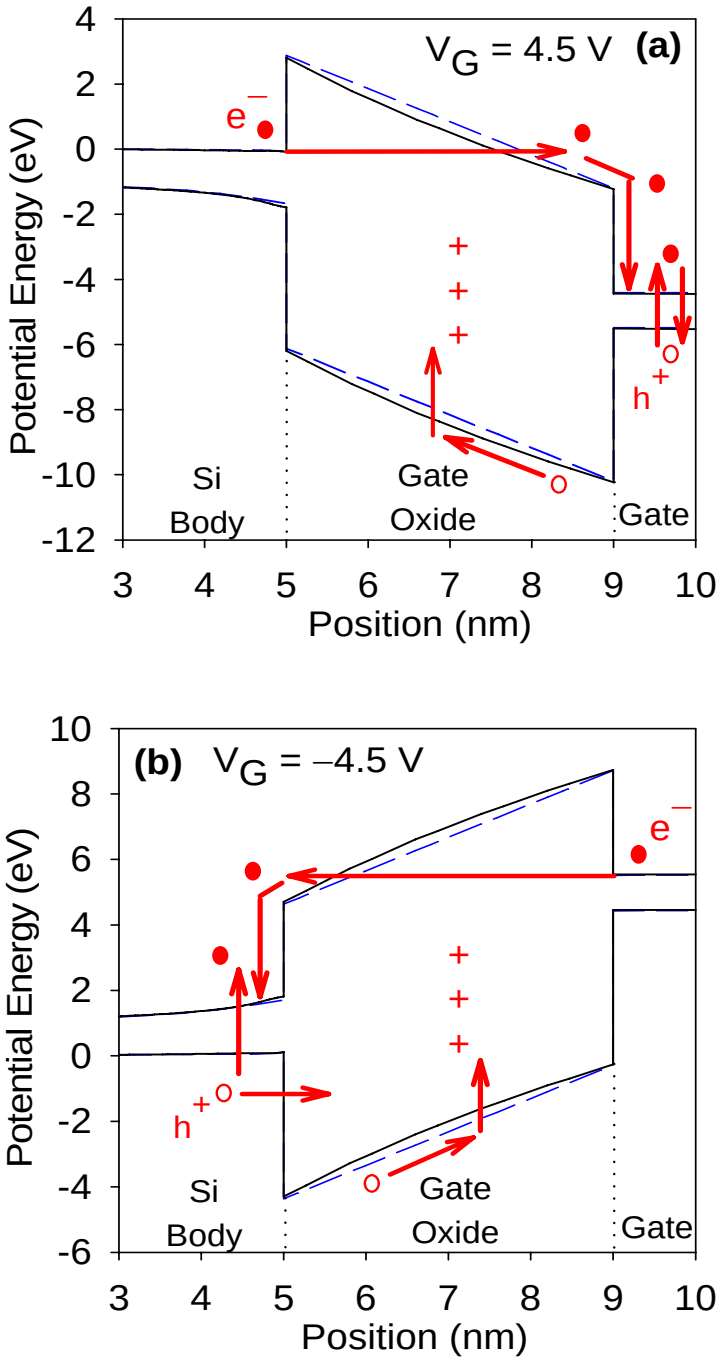

Figure 5.14: Simulated potential-energy profile of the cylindrical-channel SNWT (solid line) and the planar-channel FinFET (short-dashed line) with the FN tunneling process drawn at (a) V_G = 4.5 V and (b) V_G = – 4.5 V.

5.4. Chapter 5 conclusion

In the subthreshold region, the SNWT is volume inverted with carriers travelling through the entire silicon body; therefore, the SNWT exhibits LFN behaviours in agreement with the mobility-fluctuation model. The channel orientation may have an impact on both dc and LFN characteristics of SNWTs. In the present case, the LFN of p-type SNWTs with the channel oriented in the <010> direction is higher than that in the <110> direction, which is consistent with the observed impact of channel orientations on the drain-current level. In the strong-inversion region, the LFN of SNWTs follows the number-fluctuation model with the correlated mobility scattering. The gate electrode has a strong impact on the LFN behaviours. The limited charge carriers in the depleted layer of the poly-Si gate is less effective in screening the correlated mobility scattering, whereas it is effectively screened by the undoped-FUSI metal-gate attributed to the large electron concentration in the metal gate. For SNWTs with the doped-FUSI gate, the existence of charge dipoles at the gate/ dielectric interface may be the source of the observed mobility-scattering event.

The vulnerability of SNWTs and FinFETs to the oxide-trap generation, which is measured using the $1/f$ noise method in connection with the constant-voltage FN tunneling stress, is also studied. The device architecture has a strong influence on the oxide-trap generation. The simulation results reveal that the vertical electric field at the SiO_2/Si interface of SNWTs is increased due to the cylindrical architecture, which leads to the enhanced efficiency of the oxide-trap generation in SNWTs. Furthermore, the amount of oxide-traps generated under $V_G < 0$ FN stress is always much larger than that under $V_G > 0$ FN stress because of the back-injection of impact-ionization-generated hot holes into the SiO_2/Si interface.

CHAPTER 6: **Conclusions and Recommendations for Future Work**

6.1. Conclusions

In this work, low-frequency noise characteristics in the emerging CMOS devices such as double-gate FinFETs and gate-all-around silicon nanowire transistors have been characterized, investigated and modeled.

First of all, a floating-gate test structure for LFN characterizations in conventional CMOS devices has been presented. Instead of using various conventional designs for the input-bias stage during the LFN measurement, an alternative thinking by directly charging/discharging the channel to the desired current level before the LFN measurement has been implemented in the FG test structure. In this approach, the charges are maintained on the gate without external gate biasing during the LFN measurement, and therefore, rendering the need for elaborately designed gate-input-bias stage unnecessary. The noise introduced from the input-bias stage is thus totally excluded. The applicability of the FG test structure has been tested through measurements on the nMOS transistors fabricated by the 0.18-μm CMOS process, and its workability is demonstrated very well for both $1/f$ and RTS noise measurements.

Then, the LFN investigations on the DG FinFETs and GAA SNWTs have been carried out. For both the DG FinFETs and GAA SNWTs, the silicon channel in the weak-inversion subthreshold region is volume inverted and the current conduction is bulk conduction with channel carriers conducting through the whole silicon body.

Therefore, the mobility fluctuation is observed to be the dominant $1/f$ noise-generation mechanism. The comparative study of the channel-orientation impact on both the dc and LFN characteristics of SNWTs further confirms the mobility-fluctuation model in this region. Both the drain current and LFN in the p-type SNWT is higher for the nanowire channel oriented in the <010> direction than that in the <110> direction. The extracted Hooge parameter is at the high end of the data range reported for bulk-CMOS devices with SiO_2/poly-Si gate. This may be due to less surface-roughness and impurity scatterings in the volume-inverted and almost-intrinsic FinFETs and SNWTs.

In the strong-inversion linear region, for both the DG FinFETs and GAA SNWTs, the current conduction is surface conduction with the number fluctuation as the dominant $1/f$ noise-generation mechanism. The frequency exponent γ less than 1 is observed in the $1/f^{\gamma}$ noise characteristics of DG FinFETs. After the detailed temperature study, it is believed to be caused by a thermally-activated process with nonuniformly distributed activation energies. The model of Dutta and Horn can be used successfully in describing the correlated temperature and frequency dependence of the $1/f^{\gamma}$ noise. The energy distributions of the oxide-traps can be estimated based on this model, and the extracted trap density is found to be comparable to that in the bulk-CMOS. The applicability of the McWhorter model in explaining the same noise data has also been discussed, and found not convincing due to possible random variations of the trap density with respect to both the temperature and the trap location.

For SNWTs in strong inversion, the impact of three different gate electrodes, i.e., the poly-Si gate, doped-FUSI gate, and undoped-FUSI gate, on the LFN behaviours has been investigated. The oxide-trap density extracted based on the number-fluctuation mechanism is found to be comparable among three different gate electrodes and not degraded by the gate FUSI process. However, the gate type has a

strong impact on the correlated mobility scattering. The limited charge carriers in the depleted layer of the poly-Si gate are less effective in screening the Columbic scattering induced by the charges in the oxide traps as well as the scattering field of the insulator phonons, thus, the strongest mobility scattering is observed in SNWTs with the poly-Si gate. The correlated mobility scattering is effectively screened by the undoped-FUSI metal-gate due to the large electron concentration in the metal gate. For SNWTs with the doped-FUSI gate, the existence of charge dipoles at the gate/SiO_2 interface counteracts the screening efficiency of the metal gate, the mobility scattering is therefore observed.

The impact of device architectures on the oxide-trap generation in FinFETs and SNWTs under constant-voltage FN tunneling stress is studied by using the 1/*f* noise method. The simulation results reveal that the cylindrical architecture of the SNWT leads to the increased vertical electric field at the SiO_2/Si interface and the decreased tunneling distance when being built into the SONOS structure. Hence, the enhanced efficiency of the oxide-trap generation is observed in SNWTs. Similar to the observations in the bulk-CMOS, the amount of oxide-traps generated under $V_G < 0$ FN tunneling stress is always much larger than that generated under $V_G > 0$ FN tunneling stress because of the back-injection of impact-ionization-generated hot holes into the SiO_2/Si interface.

The DG FinFET and GAA SNWT have comparable near-interface oxide-trap density to their bulk-CMOS counterpart, but with a superior short-channel-effect immunity over the bulk-CMOS. Hence, they are expected to be very promising for analog and RF circuit applications.

6.2. Recommendations

The following works are recommended for future study.

i. The temperature study of LFN in multigate transistors biased in the subthreshold region can be performed for further understanding of the topic 'the number fluctuations vs. the mobility fluctuations'. However, an improvement of the noise measurement setup may be needed; especially the noise contribution from the temperature vibration should be taken care of.

ii. Since the area of multigate transistors is on the order of 0.01 μm^2, the number of oxide traps may be on the order of single digit. The ultrascaled dimension of multigate transistors with randomly distributed oxide traps may lead to the high dispersion of the noise spectral density. The impact of process variations on the statistical fluctuations of the noise spectral density and, in turn, on the analog/RF performance of multigate transistors can be investigated.

iii. The multigate transistor, which has the superior intrinsic RF scaling capability, may become a suitable candidate for low-power RF applications. With the properly designed RF structure and RF probe pad, the high-frequency noise characteristics of multigate transistors and their impact on the RF applications can be studied.

iv. In order to bring together the physics and device world with the circuit world, the LFN which is one of the key difficulties in RF/analog circuit designs (e.g., voltage-controlled oscillator, mixer and low-noise amplifier) is worth discussing in the RF/analog circuit domain.

v. The LFN characteristics can be investigated in the silicon-nanowire-based p^+–i–n^+ tunneling FET, which is proposed to be an excellent candidate for ultralow

power and high-density applications. Then, the comparison of noise characteristics can be done between this tunneling FET and the conventional silicon nanowire transistor.

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Journal and Letter

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