Analysis of Nonideal Effects on a Tomography-Based Switched-Capacitor Transducer

Jia Peng and P. K. Chan

***Abstract*—This paper presents a nonideal analysis of a fully-integrated switched-capacitor capacitive transducer for electrical capacitance tomography system. The investigation establishes different types of error source models as well as practical mismatch effects in the derivation of second-order analytical expressions. The analyses are conducted on the basis of heavy stray capacitances of 150 pF typically, in the context of a minimum detection capacitance ranging from 1 to 10 fF. The predicted results agree very well with the HSPICE simulation results using Level 49 BSIM3 models of AMS 0.6-μm CMOS process technology with a single 5-V supply. The conservative simulation results have shown that the capacitive transducer differential output displays a baseline dc offset of 0.083 mV at 25 °C, a change in baseline capacitance of 1 fF from 25 to 40 °C and an output temperature coefficient of 0.045 mV/°C from 25 to 100 °C at the measuring capacitance of 1 pF. Both the predicted and simulated results presented here are better than that of the reported works.**

***Index Terms*—Capacitive interface, capacitive transducer, CMOS circuit, electrical capacitance tomography (ECT), switched-capacitor circuit.**

NOMENCLATURE

A	Open-loop gain of op-amp.
C_f, R_f	Feedback capacitance and resistance of op-amps.
W, L	Channel width and length of MOS transistor switch.
$C_{\rm ox}$	Gate capacitance per unit area.
V_{t0}	Threshold voltage at $V_{\rm BS} = 0$.
K_1	First-order body effect coefficient in the BSIM3 model.
K_2	Second-order body effect coefficient in the BSIM3 model.
ϕ_s	Surface potential $\phi_s = 2(kT/q)\ln(N_{\rm ch}/n_i)$, where k is Boltzmann's constant, T is temperature in Kelvin, q is the electronic charge, $N_{\rm ch}$ is the channel doping concentration, and n_i is the intrinsic carrier density.
n_i	$n_i = 1.45 \times 10^{10}(T/300.15)^{1.5}\exp(21.5565981 - (E_g/(2kT/q)))$, where E_g is the energy gap at temperature T.
V_t	Threshold voltage of the MOS transistor switch.
$C_{\rm ov}$	Overlap capacitance of the MOS transistor switch.
V_g	Gate voltage of the MOS transistor switch.
V_B	Body bias of the MOS transistor switch.
C_x	Sensing capacitance.
C_{p1}, C_{p2}	Stray capacitances associated with the setup.
V_Q	Ideal analog ground potential.
V'_Q	Nonideal analog ground voltage source, with $V'_Q = V_Q + \delta_2$.
δ_2	Dc offset of nonideal analog ground voltage source.
$V_{\rm ref}$	Ideal reference bias voltage for detector.
$V_{\rm ref1}$	Reference voltage source 1 built using the nonideal reference driver, with $V_{\rm ref1} = V_Q + \delta_1 + V_{\rm ref}$.
δ_1	Dc offset of nonideal reference driver with respect to V_Q.
$V_{\rm ref2}$	Reference voltage source 2, with $V_{\rm ref2} = 0$.
V_e	Switch error.
ε	Gain error of op-amp from finite open-loop gain.
$V_{\rm os}$	Dc offset of op-amp.
$V_{\rm cmrr}$	Input common-mode error of op-amp.
K_ε	Gain error of detector.

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I. INTRODUCTION

ELECTRICAL capacitance tomography (ECT) is a technique used to obtain information on the distribution of the contents of closed oil pipes or vessels. It senses variations in the dielectric properties of the material inside the vessel. To measure details as fine as a small gas bubble trapped inside an oil pipe, the ECT sensing interface needs to have the ability to detect minute capacitance changes (typically ranging from 1 to 10 fF) whilst maintaining a very stable output against time and temperature. It follows then that a quality ECT transducer has to feature 1) low baseline drift against time and temperature; 2) immunity against the stray effects of the setup; 3) high sensitivity; 4) good output stability; and 5) fast data capture rate. From the literature, there are two types of ECT systems, namely the switched-capacitor (SC) ECT system [1], [2] and the ac-based ECT system [3]–[5].

The SC ECT system was the product of research done by the University of Manchester, Institute of Science and Technology (UMIST). This was the first system to successfully use a charging and discharging circuit to build a real-time ECT transducer [1], [2]. A cycle of operation consisting of a charge phase and a discharge phase, acts on the sensing capacitance C_x. A

pseudo-differential QV converter, which incorporates the filter function, is formed by two operational amplifiers (op-amps) OP1, OP2, the feedback capacitances C_{f1}, C_{f2}, and the feedback resistances R_{f1}, R_{f2}. The flow of charge is transformed into voltages that are proportional to C_x. With a baseline correction arrangement, the implementation can attain a maximum resolution of 0.3 fF. It has a linear response and demonstrates a reasonably fast rate of data capture of 100 frames per second. Integrating electrodes [2] into the SC ECT reduces the parasitic capacitance arising from the electrode wiring and allows the operating frequencies of the system to be increased. This furthers the ultimate goal of increasing the circuit sensitivity with which minute capacitances are detected. However, despite efforts to improve the UMIST SC ECT [1], [2] system, it retains the following key shortcomings.

1) External component requirements: For any given set of feedback resistor and reference voltage values, the sensitivity of the circuit depends on the presence of an accurate external clock circuitry. The maximum switching frequency of the system is indirectly governed by the op-amp bandwidth, the stray capacitances C_{p1} and C_{p2} and the on-resistance of CMOS switches. Despite the use of wide bandwidth op-amps, two large external capacitances C_{in1} and C_{in2} are also needed to ensure that the virtual ground potential is stable during high-speed charge transfer operations.
2) Large baseline drift: Although the pseudo-differential structure reduces the output offset voltage, there still exists in the discrete implementation a residual dc offset of about 20% to 30%, making up a few tens of millivolts at typical sensitivity (equivalent of typical 0.03 pF for static C_x. This offset is accounted for by the switch errors, the mismatch of discrete feedback components, the large supply operation ($+/-15$ V) that further enhances the residual dc offset through a mismatch of CMOS switches, and the intrinsic dc offsets of the op-amps. As a result, frequent calibration is required in order to compensate for the large baseline drift against the time and temperature.

Several analytical studies have been done on the ac-based ECT system in recent years [6], [7] and the signal-to-noise ratio (SNR) of the transducer [3]–[5] is reported to be 60 dB. However, a similar level of attention has not been paid to the analytical study of switched-capacitor-based ECT. This paper aims at concentrating on the analysis of the nonideal effects of a switched-capacitor correlated double-sampling (SC CDS) ECT transducer [8]. The nonideal analysis has shown not only that the proposed transducer offers improved performance with respect to the UMIST SC ECT, but that it is also suitable for fully integration. At this stage, the study will not focus on analyzing or calculating the SNR.

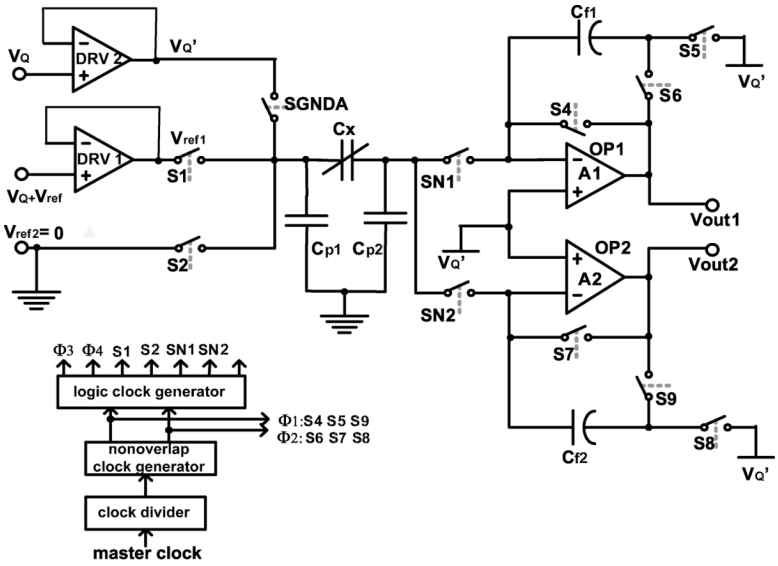
II. SC CDS ECT Front-End Transducer

A front-end transducer incorporating the CDS technique [9], [13], [14] is shown in Fig. 1(a). The use of CDS takes advantage of the cancellation of dc offsets and 1/f noise arising from the CMOS op-amps. This applies especially because the dc offsets tend to drift with time and temperature and the 1/f noise reduces the SNR dynamic range of the transducer. Fig. 1(a) consists of two capacitance detectors: Capacitance Detector 1 (CD1) and Capacitance Detector 2 (CD2) arranged in a circuit with pseudo-differential architecture. Each capacitance detector comprises one high-speed op-amp, with its positive input tied to the virtual ground V'_Q and its negative input tied to a CDS switched-capacitor network. To measure C_x, the source electrode is switched in a sequence to sources ($V_{\text{ref1}} \neq 0, V_{\text{ref2}} = 0$, and V'_Q), respectively. These sources are controlled by three MOS switches S1, S2, and SGNDA, while the detecting electrode is alternatively connected with each op-amp's virtual earth through the switch control signals SN1 and SN2. In an ideal design condition, $V_{\text{ref1}} - V'_Q = -(V_{\text{ref2}} - V'_Q) = -(0 - V'_Q)$. Due to the finite number of reference driver offsets, $V_{\text{ref1}} - V'_Q \cong -(0 - V'_Q)$. Fig. 1(b) shows the waveforms of the switch control signals. The front-end sensor consists of four operation phases derived from the nonoverlapping biphasic clock signals ϕ_1 and ϕ_2, namely the reset phase, the auto-zero phase, the charge transfer phase, and the hold phase. In the reset phase, the op-amp in the detector is configured in a unity-gain configuration while the feedback capacitor is connected to the analog ground. In the auto-zero phase, the op-amp retains the same configuration but both the sensing and feedback capacitors must be switched to analog ground to sample the op-amp offset. In the charge transfer phase, the sensing capacitance is applied with a reference voltage source (either a ground reference or alternative reference source) whilst the feedback capacitor forms the feedback loop for capacitance-to-voltage conversion. It is noted that the two reference sources are designed to be symmetrical with respect to the analog ground. When the sensing capacitance is isolated in the final hold phase, the detected voltage will be held by the feedback capacitor.

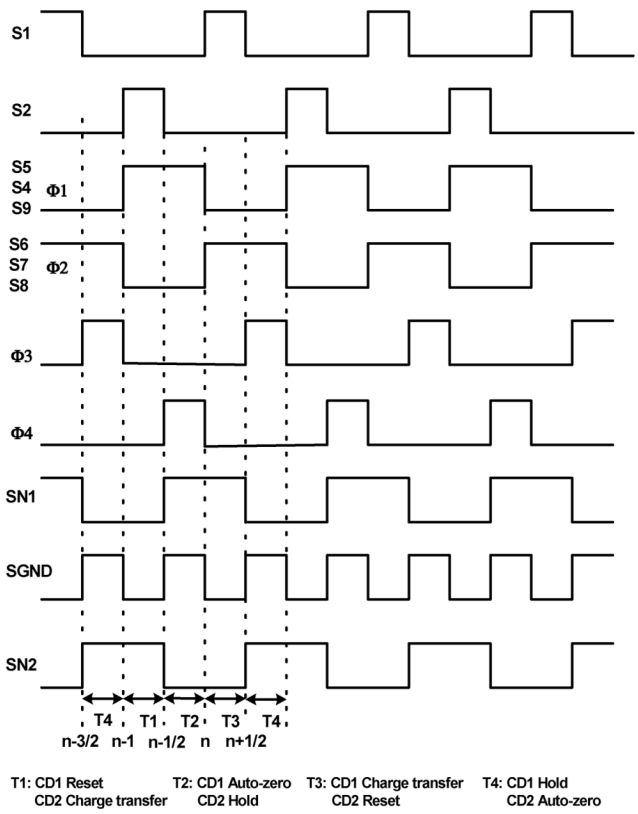
Multiple switch control clock signals S1, S2, SGNDA, SN1, and SN2 are derived by the logic clock generator together with the switch control signals S4–S9 obtained directly from ϕ_1 and ϕ_2. These signals serve to configure the circuit at each operation phase. From the analytical results summarized in Table I, it can be seen that the CDS technique removes the principal dc offsets of the op-amps in CD1 and CD2 but some residual offsets remain. The first dc offset δ_2 arises from the voltage difference between the nonideal analog ground source V'_Q and the ground whereas the second dc offset $(\delta_1 - \delta_2)$ comes from the voltage difference between the nonideal reference source V_{ref1} and the nonideal analog ground source V'_Q. The impact of these residual dc offsets together with other second-order effects will be further examined in Section III.

III. Analysis of SC CDS ECT Transducer

Although the offset and 1/f noise components of the CMOS op-amps can be canceled effectively in the design of the SC CDS ECT transducer, other second-order effects may have significant impact on the circuit's actual performance. These second-order effects are mainly accuracy, nonlinearity, minimum detectable capacitance, and drift characteristics. The nonideal SC transducer is expected to take into account the following: 1) switch errors; 2) nonideal op-amp errors; 3) error induced by heavy stray capacitances; 4) error induced by mismatched components; and 5) offsets of the reference driving sources. Such nonideal effects complicate the SC analysis



(a)



(b)

Fig. 1. Front-end SC CDS ECT transducer and its control signals: (a) transducer and (b) the switch control signals.

substantially. Following from this, one of the objectives of this paper is to investigate the influence of each effect on the respective output. This paper also aims to study the degree to which second-order effects are being suppressed by devising analytical expressions for the differential output of the SC CDS ECT transducer. Simplified BSIM3 models are applied in the analysis to match the BSIM3 models being used in the circuit simulator. Their symbols and definitions are explained in the Nomenclature of this paper and in [11] and [15]. Prior to the analysis, the design parameters for the transducer are summarized in Table II.

A list of error sources is established for the second-order analysis of a practical SC transducer. Varying degrees of inaccuracy are introduced from critical switch error sources, op-amp error sources arising from offset, finite open-loop gain, and the finite common mode rejection ratio. Based on the design parameters, the on-resistance of the switches are about 230 Ω and the off resistances are at the $G\Omega$ level. The on-resistance should meet the $R_{\rm on}C_{p2}$ time constant requirement with respect to the defined clock period. The settling error is negligible as fast settling op-amps are employed (see Fig. 2). Fig. 3(a) shows the auto-zero phase ϕ_1 of CD1, with dc offset $V_{\rm os1}(n-1/2)$ and

TABLE I
OUTPUTS AT DIFFERENT OPERATION STATUS OF CD1, CD2

Operation Phase	V_{out1} of CD1	V_{out2} of CD2
T1	$V_{out1} = V_Q' + V_{os1}$ Reset	$V_{out2} = V_Q' + (C_x/C_{f2})(V_{ref} + \delta_2)$ $V_{out2} \cong V_Q' + (C_x/C_{f2})V_{ref}$ for $V_{ref} >> \delta_2$ Charge Transfer
T2	$V_{out1} = V_Q' + V_{os1}$ Auto Zero	$V_{out2} = V_Q' + (C_x/C_{f2})(V_{ref} + \delta_2)$ $V_{out2} \cong V_Q' + (C_x/C_{f2})V_{ref}$ for $V_{ref} >> \delta_2$ Hold
T3	$V_{out1} = V_Q' - (C_x/C_{f1})(V_{ref} + \delta_1 - \delta_2)$ $V_{out1} \cong V_Q' - (C_x/C_{f1})V_{ref}$ for $V_{ref} >> \delta_1 - \delta_2$ Charge Transfer	$V_{out2} = V_Q' + V_{os2}$ Reset
T4	$V_{out1} = V_Q' - (C_x/C_{f1})(V_{ref} + \delta_1 - \delta_2)$ $V_{out1} \cong V_Q' - (C_x/C_{f1})V_{ref}$ for $V_{ref} >> \delta_1 - \delta_2$ Hold	$V_{out2} = V_Q' + V_{os2}$ Auto Zero

TABLE II
DESIGN PARAMETERS USED IN THE TRANSDUCER

Parameter	Value
Feedback capacitances, C_{f1} and C_{f2}	8 pF
Stray capacitances , C_{p1} and C_{p2}	150 pF
Non-ideal analog ground voltage, $V_Q' = V_Q + \delta_2$	1V + 2mV
Op-amp unity-gain bandwidth, GBW	43 MHz
Op-amp open-loop gains, A_1 and A_2	10000
Channel width of switch, W	10 μm
Channel length of switch, L	0.6 μm (drawn) 0.55 μm (effective)
Switching frequency of non-overlapping clocks, f_{clk}	250 kHz
Non-ideal reference voltage, $V_{ref1} = V_Q + \delta_1 + V_{ref}$	1V + 5mV + 1V
Ground reference voltage, V_{ref2}	0 V
Ideal reference bias voltage, V_{ref}	1 V
Full-scale output at maximum C_x = 2pF	250 mV

input common mode error $V_{\rm cmrr1}(n-1/2)$. Fig. 3(b) shows the charge transfer phase ϕ_2 of CD1, with dc offset $V_{\rm os1}(n)$, switch error V_{e1}, finite gain error ε_1, and input common mode error $V_{\rm cmrr1}(n)$. The CD2 in the auto-zero and transfer phases are similarly shown in Fig. 4(a) and (b), respectively. Notations pertaining to error voltage sources have similar meanings to that in Fig. 3 and so are not repeated here. Using the SC analysis method [9], [13], [14], during ϕ_1, the basic voltage equations of CD1 in Fig. 3(a) are

$$V_{\rm out1}(n-1/2) = V_{\rm os1}(n-1/2) + V_Q' + V_{\rm cmrr1}(n-1/2) \quad (1)$$
$$V_{\rm cf1}(n-1/2) = -V_{\rm os1}(n-1/2) - V_{\rm cmrr1}(n-1/2) \quad (2)$$
$$V_{\rm cx}(n-1/2) = -V_{\rm os1}(n-1/2) - V_{\rm cmrr1}(n-1/2) \quad (3)$$
$$V_{\rm cp2}(n-1/2) = -\left[V_{\rm os1}(n-1/2) + V_Q' + V_{\rm cmrr1}(n-1/2)\right]. \quad (4)$$

During ϕ_2, the basic voltage equations of CD1 in Fig. 3(b) are

$$V_{\rm cx}(n) = (V_{\rm ref} + \delta_1 - \delta_2) - [V_{\rm os1}(n) + V_{e1} + \varepsilon_1 + V_{\rm cmrr1}(n)] \quad (5)$$
$$V_{cf1}(n) = \Delta V_{\rm out}(n) - [V_{\rm os1}(n) + V_{e1} + \varepsilon_1 + V_{\rm cmrr1}(n)] \quad (6)$$

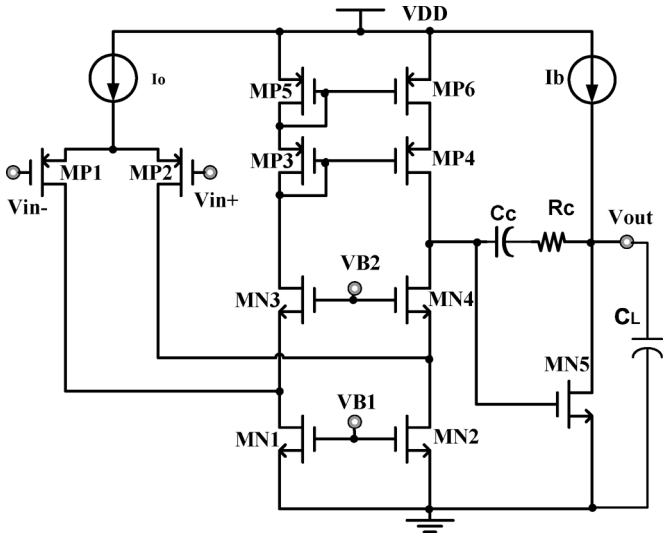


Fig. 2. High-speed op-amp for SC transducer.

$$V_{\rm cp2}(n) = -\left[V_{\rm os1}(n) + V_{e1} + \varepsilon_1 + V_Q' + V_{\rm cmrr1}(n)\right]. \quad (7)$$

The change in the charges of capacitances C_x and $C_{\rm cp2}$ are obtained as

$$\Delta Q_{\rm cx1} = C_x\left[V_{\rm cx}(n) - V_{\rm cx}(n-1/2)\right] \quad (8)$$
$$\Delta Q_{\rm cp2} = C_{\rm cp2}\left[V_{\rm cp2}(n) - V_{\rm cp2}(n-1/2)\right] \quad (9)$$

and, thus, the change in the charges of capacitance C_{f1} is

$$\begin{aligned}\Delta Q_{\rm cf1} &= \Delta Q_{\rm cx1} + \Delta Q_{\rm cp2} \\ &= C_x(V_{\rm ref} + \delta_1 - \delta_2 - V_{e1} - \varepsilon_1) - C_{\rm cp2}(V_{e1} + \varepsilon_1)\end{aligned} \quad (10)$$

where it is assumed that $V_{\rm os}(n) = V_{\rm os}(n-1/2)$ and $V_{\rm cmrr1}(n) = V_{\rm cmrr1}(n-1/2)$. The voltage developed across the feedback capacitance C_{f1} at time n is

$$V_{\rm cf1}(n) = V_{\rm cf1}(n-1/2) - \frac{\Delta Q_{\rm cf1}}{C_{f1}} \quad (11)$$

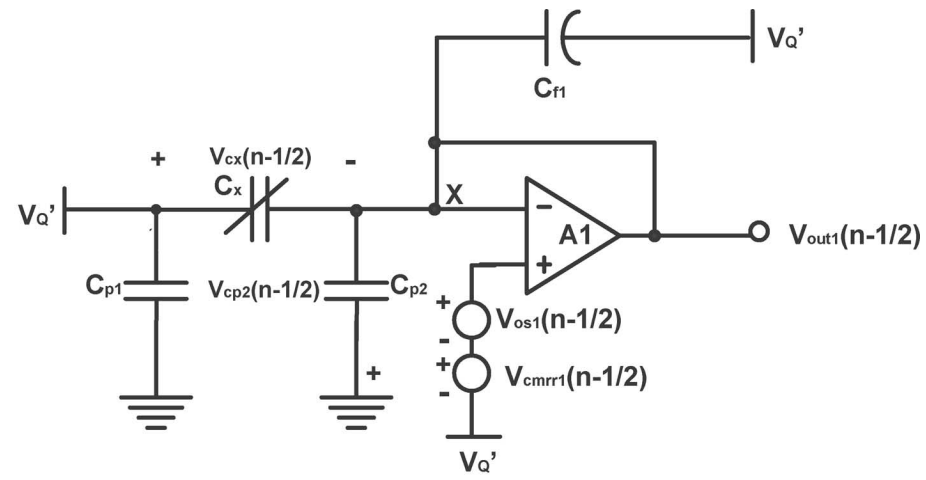
where $V_{\rm cf1}(n-1/2)$ is defined in (2). Since the output voltage of CD1 is defined by

$$V_{\rm out1}(n) = V_Q' + \Delta V_{\rm out1}(n). \quad (12)$$

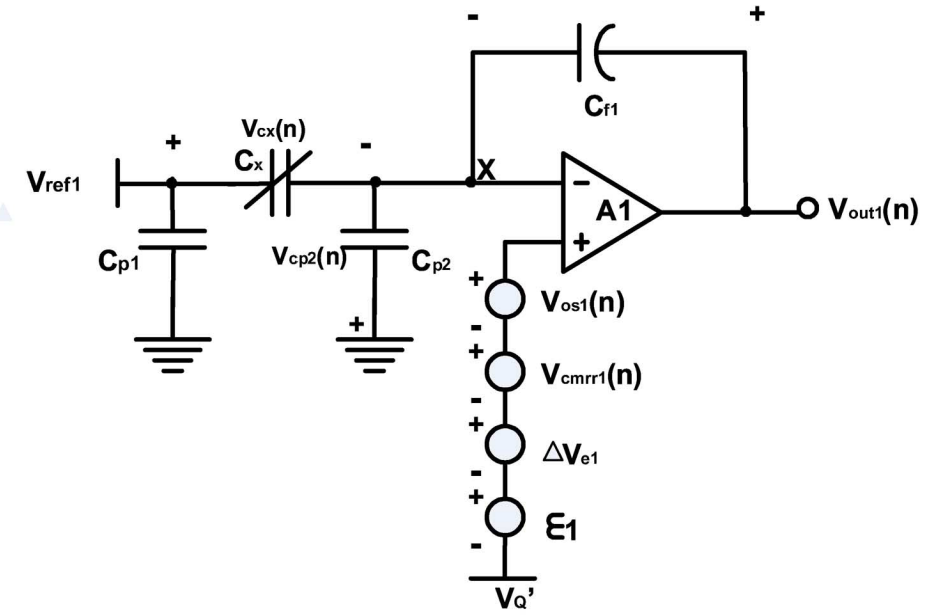
Putting (6) into (12), the output voltage of CD1 at time n is given by

$$V_{\rm out1}(n) = V_Q' + V_{\rm os1}(n) + V_{e1} + \varepsilon_1 + V_{\rm cmrr1}(n) + V_{\rm cf1}(n). \quad (13)$$

Substituting (2) and (10) into (11), the final result of the expression $V_{\rm cf1}(n)$ is further substituted into (13). One can thus relate



(a)



(b)

Fig. 3. Auto-zero and charge transfer phase of CD1 with error source models: (a) auto-zero phase $\phi 1$ of CD1 at T2 in Fig. 3(b), (b) charge transfer phase $\phi 2$ of CD1 at T3 in Fig. 4(a).

(12) and (13) and use the definition of $\varepsilon_1 = \Delta V_{\text{out1}}(n)/A_1$ to solve the incremental output as follows:

$$\Delta V_{\text{out1}}(n) = \frac{-\frac{C_x}{C_{f1}}(V_{\text{ref}}+\delta_1-\delta_2)+\left(1+\frac{C_{p2}}{C_{f1}}\right)V_{e1}}{1-\frac{1}{A_1}\left(1+\frac{C_x+C_{p2}}{C_{f1}}\right)} \cong \frac{-\frac{C_x}{C_{f1}}(V_{\text{ref}}+\delta_1-\delta_2)+\left(1+\frac{C_{p2}}{C_{f1}}\right)V_{e1}}{1-\frac{1}{A_1}\left(1+\frac{C_{p2}}{C_{f1}}\right)} \quad (14)$$

where it is assumed that $C_{p2} \gg C_x$. The output expression of CD1 is obtained as

$$V_{\text{out1}}(n) \cong V_Q' + \frac{-\frac{C_x}{C_{f1}}(V_{\text{ref}}+\delta_1-\delta_2)+\left(1+\frac{C_{p2}}{C_{f1}}\right)V_{e1}}{1-\frac{1}{A_1}\left(1+\frac{C_{p2}}{C_{f1}}\right)}. \quad (15)$$

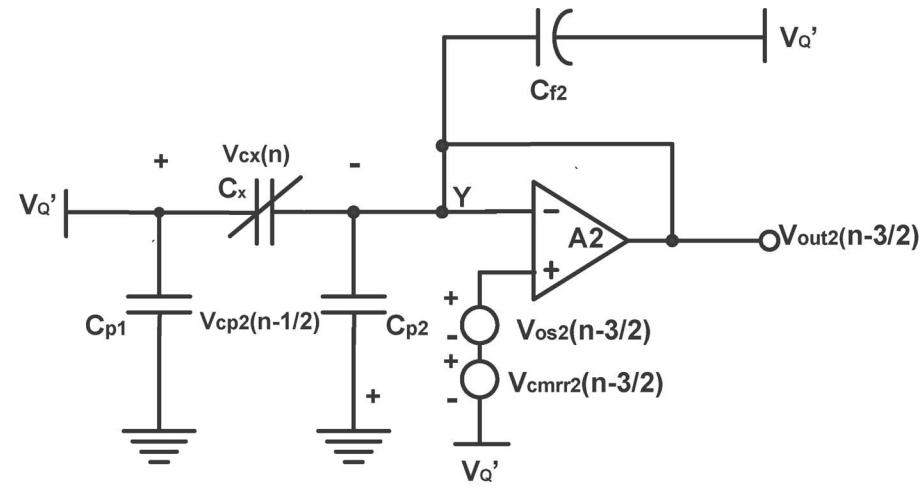
Similarly, the output expression of CD2 [see Fig. 4(a) and (b)] is obtained as follows:

$$V_{\text{out2}}(n-1) \cong V_Q' + \frac{\frac{C_x}{C_{f2}}(V_{\text{ref}}+\delta_2)+\left(1+\frac{C_{p2}}{C_{f2}}\right)V_{e2}}{1-\frac{1}{A_2}\left(1+\frac{C_{p2}}{C_{f2}}\right)} \quad (16)$$

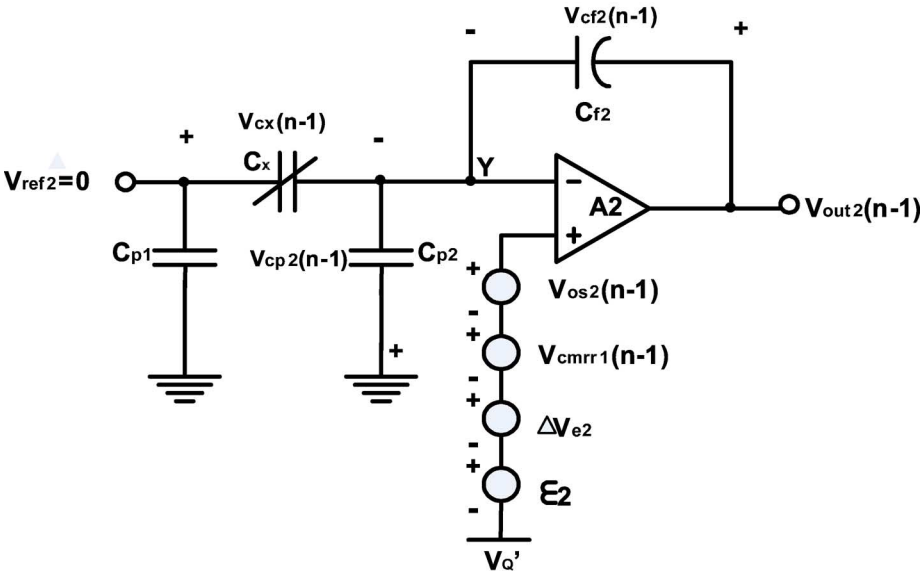
and the incremental ac voltage for CD2 output is

$$\Delta V_{\text{out2}}(n-1) \cong \frac{\frac{C_x}{C_{f2}}(V_{\text{ref}}+\delta_2)+\left(1+\frac{C_{p2}}{C_{f2}}\right)V_{e2}}{1-\frac{1}{A_2}\left(1+\frac{C_{p2}}{C_{f2}}\right)}. \quad (17)$$

From (15) and (16), it is worth noting that not only is the fundamental dc offset canceled in the CDS transducer, but that the common mode error in each single-ended output is similarly



(a)



(b)

Fig. 4. Auto-zero and charge transfer phase of CD2 with error source models: (a) auto-zero phase $\phi 2$ of CD2 at previous T4 in Fig. 3(b) and (b) charge transfer phase $\phi 1$ of CD2 at T1 in Fig. 3(a).

eliminated. This relaxes the common-mode rejection requirement for the op-amp design. Comparing (14) and (17) with the results of hold phase in Table I, additional op-amp switch error and gain error are observed in each output of detector. This error is boosted by the parasitic gain factors, $(1 + C_{p2}/C_{f1})$ and $(1 + C_{p2}/C_{f2})$, which are regarded as error multiplying factors induced by the heavy stray capacitances in the tomography operation environment.

From (14), it appears that V_{e1} is signal-dependent switch error which relates to the output according to A1(8). Thus, substituting (14) back into A1(8) again and ignoring insignificant terms, we get

$$V_{e1} \approx \frac{-W_1 L_1 C_{\rm ox}}{2C_{p2}} \times \left[V_{eff1} - \frac{\left(1+\frac{C_{p2}}{C_{f1}}\right) V_{e1} - \frac{C_x}{C_{f1}}(V_{\rm ref}+\delta_1-\delta_2)}{1-K_{\varepsilon 1}} m \right] \quad (18)$$

where $K_{\varepsilon 1} = (1 + C_{p2}/C_{f1})/A_1$ is defined as the gain error of CD1 arising from parasitic closed-loop gain of detector and finite open-loop gain of op-amp. Solving (18) for V_{e1} in CD1 gives

$$V_{e1} \approx \frac{-W_1 L_1 C_{\rm ox}\left[V_{\rm eff1}(1-K_{\varepsilon 1})C_{f1} + mC_x(V_{\rm ref}+\delta_1-\delta_2)\right]}{2C_{p2}(1-K_{\varepsilon 1})C_{f1}}. \quad (19)$$

It can be seen that the switch error V_{e1} can be approximated as a dc term as well as a C_x-dependent term. According to A1(9), the switch error V_{e2} in the CD2 output (17) is merely a dc term that is a function of bias voltages and mismatches in threshold voltage. The error terms in V_{e1} and V_{e2} can be reduced significantly through differential operation using the conversion block depicted in Fig. 5. In the figure, a switch network controlled by switching waveforms is inserted between the respective outputs of CD2 and CD1 and the respective inputs of the signal-processing stage. This processing stage consists of an ideal subtractor and an ideal fifth-order low-pass filter with

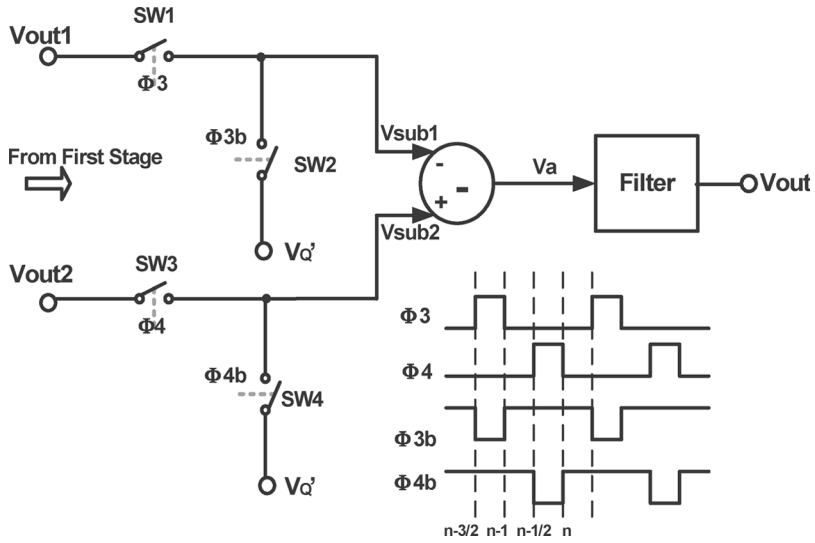


Fig. 5. Differential-to-single-ended conversion block.

a 5-kHz cutoff frequency. Since the two differential input signals from the sample-data domain are averaged over a continuous-time domain in the analog signal-processing block, the average output of the differential-to-single conversion block can be obtained as

$$V_{\text{out}} \cong \frac{V_a(n-3/2)+V_a(n-1)+V_a(n-1/2)+V_a(n)}{4} = \frac{\Delta V_{\text{out2}}(n-1/2)-\Delta V_{\text{out1}}(n-3/2)}{4}. \quad (20)$$

(19) is first substituted into (14) and A1(9) is substituted into (17). The results of this are then substituted into (20). Neglecting insignificant terms, we obtain

$$\begin{aligned} V_{\text{out}} \cong{}& \frac{V_{\text{ref}}}{2C_f}C_x+\frac{V_{\text{ref}}K_\varepsilon}{2C_f}C_x+\frac{\delta_1}{4C_f}C_x-\frac{V_{\text{ref}}}{4C_f}\left(\frac{\Delta C_f}{C_f}\right)C_x \\ &+\left(1+\frac{C_{p2}}{C_f}\right) \times\left(\frac{(WL+\Delta(WL))\,mC_{\text{ox}}(V_{\text{ref}}+\delta_1-\delta_2)/C_f}{8C_{p2}(1-K_\varepsilon)^2}\right)C_x \\ &-\left(1+\frac{C_{p2}}{C_f}\right) \times\left(\frac{WLC_{\text{ox}}\Delta V_{\text{to}}-\Delta(WL)C_{\text{ox}}V_{\text{eff1}}}{8C_{p2}(1-K_\varepsilon)}\right) \end{aligned} \quad (21)$$

where the mismatch definitions are denoted as

$$W_1L_1 = W_2L_2+\Delta(W_2L_2) = WL+\Delta(WL)$$
$$C_{f1} = C_{f2}+\Delta C_{f2} = C_f+\Delta C_f.$$

$A_1 = A_2+\Delta A_2 = A+\Delta A$. WL, C_f, and A are parameters having nominal values. $\Delta(WL)$, ΔC_f, and ΔA are the parameters representing random mismatch. Note that $1-K_{\varepsilon 1} \cong 1-K_{\varepsilon 2} = 1-K_\varepsilon = 1-(1+C_{p2}/C_f)/A$. It is apparent from (21) that the actual output comprises a fundamental term that represents the signal with measured C_x, the sensitivity error arising from the gain error of the detector, the dc offset of the reference driving source, the mismatch of the feedback capacitances, the signal-dependent charge injection error, and the static charge injection error that contributes the residual dc offset of the transducer. It is generally observed that the charge injection errors caused by switch mismatch and/or dc offsets of the driving sources are common functions of the gain error of the detectors and a parasitic bootstrapping factor.

IV. Results and Discussions

The mismatched values are applied to conservatively estimate the nonideal differential-to-single-ended output. In this case, the output (21) is made to exhibit a higher value to reflect the actual higher level of error whenever possible. This leads to practical fabrication error assumptions that $\Delta V_{\text{to}} = -5$ mV, $\Delta(WL) = +10\%$ of WL and that $\Delta C_f = -0.1\%$ of C_f. The process parameters are given that $\Phi_s = 0.81$ V, $V_{\text{to1}} = 0.848$ V, $C_{\text{ox}} = 2.72 * \text{e} - 3$ F/m^2 $K_1 = 1.057$ V$^{1/2}$ and $K_2 = -0.123$. The design parameters are given that $V_Q' = 1.002$ V for $\delta_2 = 2$ mV, $V_{\text{ref}} = 1$ V, $V_B = 0$ V, $V_g = 5$ V, $A = 10\,000$, $W = 10$ μm, $L = L_{\text{eff}} = 0.55$ μm (0.6 μm drawn length), C_f =8 pF, and $C_{p2} = 150$ pF. From these parameters, we derive that $V_{\text{eff1}} = 2.682$ V [A1(11)] and that $m = 1.27$ [A1(10)]. Assuming that $\delta_1 = 5$ mV and $\delta_1 - \delta_2 = 3$ mV, the empirical (21) becomes

$$V_{\text{out}} = (0.0625+0.000123+0.000156+0.0000313 +0.0000433)C_x + 6.62 * 10^{-5}. \quad (22)$$

The relative contribution of each individual sensitivity error term is summarized in Table III. It is important to observe that the first fundamental sensitivity term is more dominant than its other counterparts of nonideal sensitivity. However, because of the system gain calibration, these nonideal sensitivity errors are not harmful. To verify empirical (22), the realistic HSPICE transistor-level simulation was carried out using the AMS 0.6-μm CMOS process parameters together with the parasitic

TABLE III
COMPARISON OF NORMALIZED INDIVIDUAL TERM USING DESIGN AND PROCESS PARAMETERS AND PRACTICAL MISMATCHES IN SECTION IV

Fundamental term	$\frac{V_{ref}}{2C_f}C_x$	**Normalized** 1
Gain error of detector	$\frac{V_{ref}K}{2C_f}C_x$	0.0020
Offset error of reference source	$\frac{1}{4C_f}C_x$	0.0025
Mismatch error of feedback capacitances	$-\frac{V_{ref}}{4C_f}\left(\frac{\Delta C_f}{C_f}\right)C_x$	0.0005
Signal-dependent charge injection error with switch mismatch	$\left(1+\frac{C_{p2}}{C_f}\right)\left(\frac{(WL+\Delta(WL))mC_{ox}\left(V_{ref}+\delta_1-\delta_2\right)/C_f}{8C_{p2}(1-K)^2}\right)C_x$	0.0007
Dc charge injection error with switch mismatch	$-\left(1+\frac{C_{p2}}{C_f}\right)\left(\frac{WLC_{ox}\Delta V_{to}-(WL)C_{ox}V_{eff1}}{8C_{p2}(1-K)}\right)$	——

TABLE IV
COMPARISON OF IDEAL, SIMULATED, AND PREDICTED RESULTS FOR THE OUTPUT OF SC TRANSDUCER, WITH C_x RANGING FROM 0 to 2 pF

C_x (fF)	Ideal Vout(V)	Simulated Vout (V)	Predicted Vout (V)
0	0	$8.3*10^{-5}$	$6.62*10^{-5}$
1	$6.25*10^{-5}$	$1.4*10^{-4}$	$1.29*10^{-4}$
2	$1.25*10^{-4}$	$2.15*10^{-4}$	$1.93*10^{-4}$
3	$1.875*10^{-4}$	$2.75*10^{-4}$	$2.56*10^{-4}$
4	$2.5*10^{-4}$	$3.32*10^{-4}$	$3.19*10^{-4}$
5	$3.125*10^{-4}$	$4.05*10^{-4}$	$3.81*10^{-4}$
6	$3.75*10^{-4}$	$4.75*10^{-4}$	$4.44*10^{-4}$
7	$4.375*10^{-4}$	$5.40*10^{-4}$	$5.07*10^{-4}$
8	$5*10^{-4}$	$5.95*10^{-4}$	$5.7*10^{-4}$
9	$5.625*10^{-4}$	$6.7*10^{-4}$	$6.33*10^{-4}$
10	$6.25*10^{-4}$	$7.4*10^{-4}$	$6.96*10^{-4}$
11	$6.875*10^{-4}$	$8.08*10^{-4}$	$7.59*10^{-4}$
12	$7.5*10^{-4}$	$8.7*10^{-4}$	$8.21*10^{-4}$
500	$3.125*10^{-2}$	$3.163*10^{-2}$	$3.15*10^{-2}$
1000	$6.25*10^{-2}$	$6.42*10^{-2}$	$6.29*10^{-2}$
1500	$9.375*10^{-2}$	$9.78*10^{-2}$	$9.44*10^{-2}$
2000	$1.25*10^{-1}$	$1.29*10^{-1}$	$1.258*10^{-1}$

extraction from the transducer (Fig. 1) and the intentional mismatches as stated previously.

Table IV provides a comparison of the ideal, simulated, and predicted output against the detection capacitance C_x. As can be seen in the table, the predicted output values are very close to the simulated results, ranging from 0 to 2 pF for different C_x values. The final sensitivity for the entire sensor system can be scaled to the targeted value through a back-end amplifying block such as the chopper difference amplifier [8] or the chopper differential difference amplifier [12]. However, this is not a critical concern because the gain in the system will be adjusted during both low and high permittivity calibration procedures [5].

A simulated dc offset of 0.083 mV, arising from the residual charge injection error as mentioned previously, is observed at the zero value of C_x. This is close to the calculated dc offset value of 0.066 mV obtained from (22). The simulated offset

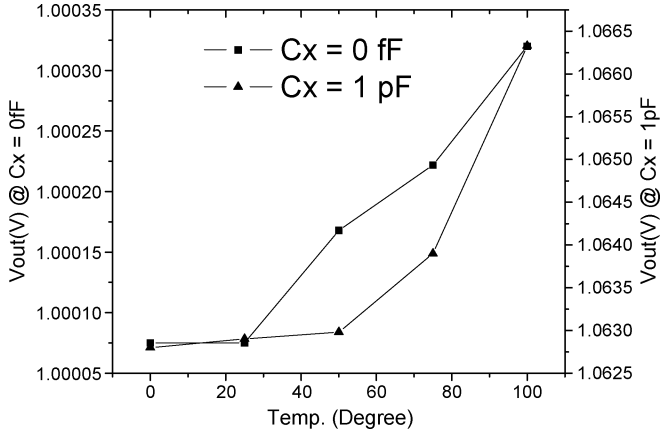


Fig. 6. Output voltage versus temperature from 0 to 100 °C with $C_x = 0$ fF and $C_x = 1$ pF.

value (equivalent to 1.33 fF) is lower than the level encountered in the prior art SC ECT transducer using discrete implementation [1], which was a few tens of millivolts (equivalent to 0.03 pF). This makes it clear that the SC CDS ECT transducer offers a significant reduction in the baseline dc offset.

The temperature drift can be studied from (21). If the parameters $V_{\rm ref}$, K_ε, δ_1, and δ_2 are very weakly temperature dependent, the transducer output becomes a function of other temperature-related parameters such as $V_{\rm eff1}$ in A1(11) and m in A1(10) which includes the surface potential $\phi_s = 2(kT/q)\ln(N_{\rm ch}/n_i)$. With an increase of temperature, the term $2(kT/q)$ increases but the other term $\ln(N_{\rm ch}/n_i)$ decreases because of the increase in the value in n_i. Fig. 6 shows the results of the output against different temperatures at zero and 1pF values of C_x. At $C_x = 0$, the output remains more or less constant and increases with temperature up to a breaking point. This observation can be explained by the fact that $\ln(N_{\rm ch}/n_i)$ counteracts $2(kT/q)$ in the temperature range 0 to 25 °C. However, $2(kT/q)$ overrides $\ln(N_{\rm ch}/n_i)$ at the breaking point, leading to the rapid increase of $V_{\rm eff1}$ in (21), and causing an increase of output with temperature. For temperatures ranging from 25 to 40 °C, the change of output is 0.065 mV, which translates to a change of 1 fF based on the

TABLE V
COMPARISON OF BASELINE AND STABILITY PERFORMANCE FOR DIFFERENT SC TRANSDUCERS

Parameter	SC ECT [1]	SC ECT [2] Integrated Electrode	SC CDS ECT This Work
Baseline dc offset at 25 °C	few tens mV	———	0.083 mV
Change of baseline capacitance with temp. at Cx = 0 (25 °C to 40 °C)	5 fF	———	1 fF
Output tempco. at Cx = 1 pF (25 °C to 100 °C)	———	−10 mV/°C	0.045 mV/°C
Stray Capacitances	150 pF	50 pF	150 pF

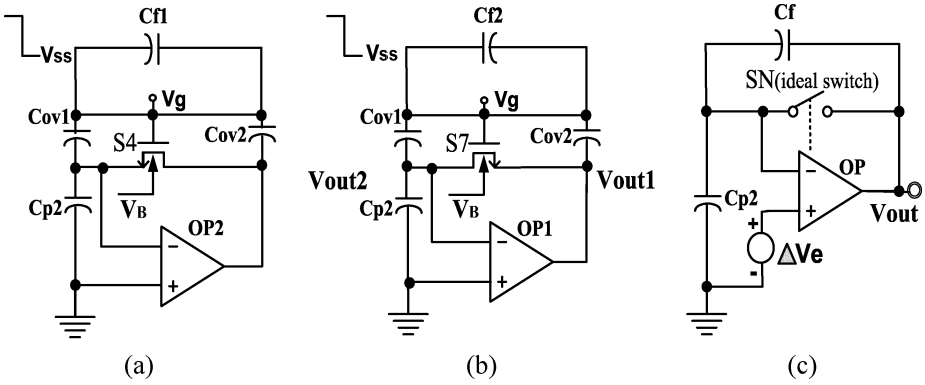


Fig. A1. Switching off nMOS switch on an op-amp during the charge transfer phase for (a) $V_{\text{out}2}$ at T1; (b) $V_{\text{out}1}$ at T3; and (c) generalized switch error source model for circuit analysis.

design sensitivity of 62.5 mV/pF. For a change of 5 fF from 25 to 40 °C, the SC CDS ECT transducer achieves considerable improvement over the results reported in [1] with regards to the baseline drift characteristic. Turning to the output stability of the detected C_x over a broad range of temperatures, we find, for example, that at $C_x = 1$ pF, the simulated result shows the output fluctuations ranging from 0 to 100 °C (see Fig. 6). At this level, the variable m in (21) contributes an additional temperature effect. Because of the term $1/\sqrt{\phi_s + V_Q' - V_B}$ in A1(10), m decreases gradually with increasing temperature. The temperature breaking point is shifted to 50 °C as a result and the temperature coefficient of the output is calculated to be 0.045 mV/°C from 25 to 100 °C. Compared to the estimated value of -10 mV/°C in the reported result of [2], the SC CDS ECT transducer offers a significantly lower operation temperature coefficient.

Table V summarizes the differences between different SC transducers. The intrinsic stability of the SC CDS ECT transducer is based on its technical merits. It brings about a reduction in the frequency at which baseline corrections need to be done, thus minimizing the amount of interruption time used in the system controller. Integrated capacitors have better matching characteristics than integrated resistors and so the component matching level is enhanced by its improved integrated design approach. With the elimination of external components and the relaxation of clock tolerance in this SC CDS ECT transducer design, it is possible to integrate the entire transducer with other building blocks such as oscillators, voltage references, ADC, DACs, and communication interfaces for each system-on-chip integrated electrodes. This allows for further miniaturization of the ECT system and holds the promise of a portable ECT system in future.

V. CONCLUSION

The influence of nonideal effects on a fully-integrated switched-capacitor CDS ECT transducer has been investigated in detail. Analytical expressions of both single-ended or differential outputs have been derived that provide insight and understanding on the heavy stray capacitances, design parameters, process parameters, nonideal components, and mismatch effects of components impacting the performance of the SC transducer in terms of sensitivity error and residual baseline dc offset. The hand-calculated results obtained are similar to that of the HSPICE simulation carried out using realistic Level 49 BSIM3 models. Not only does the differential output exhibit a dc offset of low baseline, the simulation results confirm that the SC CDS transducer provides more favorable levels of baseline dc offset drift and output thermal stability as compared to the prior art. A noise analysis of the transducer will be conducted in the future to further the work done here.

APPENDIX
SWITCH ERRORS

Refer to the identically-designed circuits Fig. A1(a) and (b). S4 and S7 are critical switches in the SC CDS ECT transducer that contribute significant levels of error. These switches are implemented using nMOS transistors and will be turned off when either CD_1 or CD_2 moves from the auto-zero to charge transfer phase. Each time a switch is turned off, charges are released into

the conducting channel. These charges move towards the MOS source and drain terminals and bring about a charge injection effect. Simultaneously, the control clock voltage, transited from supply $V_{\rm dd}$ to $V_{\rm ss}$ (0 V), is coupled to nodes via $C_{\rm ov1}$, $C_{\rm ov2}$, and the associated capacitance with reference to ground. This causes the feedthrough effect. In addition, depending on the polarity of output, there will be a modulation of threshold voltage under the body effect of the switch. It follows then that part of the charge injection exhibits a C_x-dependent property. Details of charge injection mechanism are available in [13]. Further mismatch of threshold voltages and aspect ratios in the switch pair create additional residual errors. These errors stem from the incomplete cancellation of charges in a nonideal switch pair. From the results in Table I, $V_{\rm out2}$ appears to increase while $V_{\rm out1}$ decreases in response to the incremental C_x. Because of the decrease in $V_{\rm out1}$, the source of the switch transistor S4 is now defined in the output. This provides an indication or hint that a signal-dependent charge injection will occur in S4 because the bulk-to-source voltage is no longer a constant bias. Similarly, due to the increase of $V_{\rm out2}$, the source of switch transistor S7 is located at the virtual earth node. It implies that the charge injection to this node is purely a dc offset effect. When S4 turns off in CD1 or S7 in CD2, the error voltages introduced by the charge injection and clock feedthrough effects to the virtual grounds of op-amps are

$$V_{e1} \approx \frac{Q_{\rm ch1}}{2C_{p2}} - (V_{\rm dd} - V_{\rm ss})\frac{C_{ov1}}{C_{\rm ov1} + C_{p2}} \qquad \text{A1(1)}$$

$$V_{e2} \approx \frac{Q_{\rm ch2}}{2C_{p2}} - (V_{\rm dd} - V_{\rm ss})\frac{C_{ov2}}{C_{\rm ov2} + C_{p2}} \qquad \text{A1(2)}$$

where it is assumed that half of the charge is split on each side based on fast clock transition [10], [14] and the other terms are given as

$$\begin{aligned} Q_{\rm ch1} &= -W_1L_1C_{\rm ox}(V_{\rm gs1} - V_{t1}) \\ &= -W_1L_1C_{\rm ox}\left(V_g - V'_Q - \Delta V_{\rm out1} - V_{t1}\right) \qquad \text{A1(3)} \\ Q_{\rm ch2} &= -W_2L_2C_{\rm ox}(V_{\rm gs2} - V_{t2}) \\ &= -W_2L_2C_{\rm ox}\left(V_g - V'_Q - V_{t2}\right) \qquad \text{A1(4)} \\ V_{t1} &\approx V_{t01} + K_1\left(\sqrt{\phi_s + V'_Q - V_B + \Delta V_{\rm out1}} - \sqrt{\phi_s}\right) \\ &\quad + K_2\left(V'_Q + \Delta V_{\rm out1} - V_B\right) \qquad \text{A1(5)} \\ V_{t2} &\approx V_{t02} + K_1\left(\sqrt{\phi_s + V'_Q - V_B} - \sqrt{\phi_s}\right) \\ &\quad + K_2\left(V'_Q - V_B\right). \qquad \text{A1(6)} \end{aligned}$$

Using the binomial series expansion of the square root term in A1(5), but neglecting second and higher-order terms, we have

$$V_{t1} \approx V_{t01} + K_1\left(\sqrt{\phi_s + V'_Q - V_B} - \sqrt{\phi_s}\right) + K_2\left(V'_Q - V_B\right) + \left(\frac{K_1}{2\sqrt{\phi_s + V'_Q - V_B}} + K_2\right)\Delta V_{\rm out1}. \qquad \text{A1(7)}$$

Considering the mismatch among aspect ratios and threshold voltages in the switch transistor pairs (S4 with parameters W_1 and L_1 and S7 with parameters W_2 and L_2), it can be assumed that $W_1L_1 = W_2L_2 + \Delta(W_2L_2)$ and $V_{t01} = V_{t02} + \Delta V_t$, where W_2L_2 and V_{t02} are treated as nominal references. Since $C_{p2} \gg C_{\rm ov1}, C_{\rm ov2}$, the terms $-(V_{\rm dd} - V_{\rm ss})C_{\rm ov1}/(C_{\rm ov1} + C_{p2})$, $-(V_{\rm dd} - V_{\rm ss})C_{\rm ov2}/(C_{\rm ov2} + C_{p2})$ in A1(1) and A1(2) tend to zero. Although the residual clock feedthrough occurs under a mismatch of switches, this can also be ignored because of the very large parasitic hold capacitance C_{p2}. Using a group comprising A1(7), A1(3), A1(1), and another that comprises A1(6), A1(4), and A1(2), the switch errors dominated by charge injection are now approximated as follows:

$$V_{e1} \approx \frac{-(W_2L_2 + \Delta W_2L_2)C_{\rm ox}(V_{\rm eff1} - \Delta V_{\rm out1} * m)}{2C_{p2}} \qquad \text{A1(8)}$$

$$V_{e2} \approx \frac{-W_2L_2C_{\rm ox}(V_{\rm eff2})}{2C_{p2}} = \frac{-W_2L_2C_{\rm ox}(V_{\rm eff1} + \Delta V_{t0})}{2C_{p2}} \qquad \text{A1(9)}$$

where

$$m = 1 + \frac{K_1}{2\sqrt{\phi_s + V'_Q - V_B}} + K_2 \qquad \text{A1(10)}$$

$$\begin{aligned} V_{\rm eff1} &= V_g - V'_Q - V_{t01} - K_1\left(\sqrt{\phi_s + V'_Q - V_B} - \sqrt{\phi_s}\right) \\ &\quad - K_2\left(V'_Q - V_B\right) \qquad \text{A1(11)} \\ V_{\rm eff2} &= V_g - V'_Q - V_{t02} - K_1\left(\sqrt{\phi_s + V'_Q - V_B} - \sqrt{\phi_s}\right) \\ &\quad - K_2\left(V'_Q - V_B\right). \qquad \text{A1(12)} \end{aligned}$$

Note that m is the combined coefficient from the summation of coefficients of the first-order term $\Delta V_{\rm out1}$ in A1(7) and A1(3). The switch error of identically-designed SC circuits in Fig. A1(a) and Fig. A1(b) can be represented by an ideal switch plus a switch error source V_e comprising both dominant charge and geometrical mismatch errors as shown in Fig. A1(c).

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