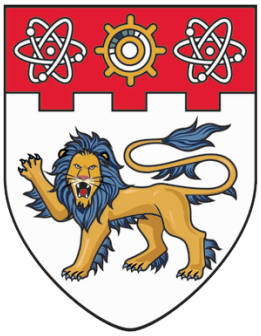

NANYANG TECHNOLOGICAL UNIVERSITY
SINGAPORE

# QUANTUM EFFICIENCY ENHANCEMENT OF GERMANIUM-ON-INSULATOR PHOTODETECTORS FOR INTEGRATED PHOTONICS ON SILICON

**LIN YIDING**

**SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING**

**2019**

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**LIN YIDING**

School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in partial fulfilment of the requirement for the degree of
Doctor of Philosophy

**2019**

# Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

2 Sept. 2019

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Date

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Lin Yiding

# Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

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Prof. Tan Chuan Seng

# Authorship Attribution Statement

This thesis contains material from one paper published in the following peer-reviewed journal where I was the first author.

Chapter 4 and 5 are published as: **Yiding Lin**, Kwang Hong Lee, Shuyu Bao, Xin Guo, Hong Wang, Jurgen Michel, and Chuan Seng Tan, “High-efficiency normal-incidence vertical *p-i-n* photodetectors on a germanium-on-insulator platform”, *Photonics Research*, **5** (6), 702-709 (2017). DOI: 10.1364/PRJ.6.000046

The contributions of the co-authors are as follows:

- I proposed the design and carried out the fabrication and characterization work of the GOI photodetectors. The devices were all fabricated in Nanyang NanoFabrication Center (N2FC), School of Electrical & Electronic Engineering, NTU. The device characterizations were performed in Silicon Technologies, Centre of Excellence (Si-COE), School of Electrical & Electronic Engineering, NTU. I also worked on the data analysis, drafted and amended the manuscript.
- Dr. Kwang Hong Lee and Dr. Shuyu Bao conducted the fabrication of the GOI at Singapore-MIT Alliance for Research and Technology.
- Ms. Xin Guo assisted in the device characterization set-up and provided guidance for collecting the characterization data of the GOI photodetectors.
- A/P Hong Wang provided technical guidance on the study and is the lead principal investigator for the entire research program in which the published work was involved.

- A/P Chuan Seng Tan provided the initial direction and technical guidance for the study. He also edited the manuscript drafts.
- Dr. Jurgen Michel provided technical guidance on the study and edited the manuscript.

2 Sept. 2019

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Date

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Lin Yiding

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It has been much more challenging than what I initially thought working towards a Ph.D. degree since 2011. Recalling the experiences over the past years, I should have set a clear goal in my mind before starting this arduous journey. Luckily, all the sadness and happiness ended up with a precious memory that is worthy to be cherished for the rest of my life.

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荣耀与恩典归于又真又活的上帝! Glory and grace to the true God!

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# Summary

Optical interconnects, enabled by electronic-photonic integrated circuits (EPICs), has been proposed as a potential solution to the latency, bandwidth and power density bottlenecks of the conventional metal interconnects in complementary metal-oxide-semiconductor (CMOS) integrated circuits. Optoelectronic components such as photodetector is one of the key building blocks, converting optical signals into electrical ones, to realize such a platform. Germanium (Ge), thanks to its CMOS-compatibility and considerable optical absorption at tele-communication wavelengths, has been widely studied for integrated photodetectors on silicon (Si).

In recent years, germanium-on-insulator (GOI) has attracted significant attention. The intermediate insulator layer can play several vital roles: 1) preventing carrier cross-talk and material inter-diffusion between Ge and the underlying Si; 2) enabling a stronger optical confinement in the top Ge for sensing and communication at mid-infrared wavelengths (3 to 14 μm); 3) enhancing electrostatic control for Ge CMOS; 4) facilitating a dense three-dimensional back-end-of-line (BEOL) electronic-photonic integration. The quality of Ge can also be generally improved compared to that from direct epitaxy, which could help reduce the dark current noise from the photodetectors. However, state-of-the-art photodetectors on GOI are reported with limited quantum efficiency (QE). This is due to their planar deployment of the contacts at the Ge surface that is inefficient in collecting the deep photon-generated carriers.

In this thesis, a method to realize a vertical *p-i-n* structure in GOI, using silicon dioxide ($SiO_2$) as the insulator layer, was developed by ion-implanting boron at one side of an epitaxial-grown Ge layer, followed by arsenic at the other side, along with a bonding and layer transfer process for the GOI fabrication. The vertical *p-i-n* structure builds a vertical electric field across the Ge layer for an efficient carrier collection. Abrupt doping profiles were verified in the transferred high-quality Ge layer. The photodetectors exhibit a dark current density of$\sim$47 mA/cm$^2$ at −1V and an optical responsivity of 0.39 A/W at 1550 nm, which are prominently improved compared to state-of-the-art GOI photodetectors. An internal quantum efficiency (IQE) of ~97% indicates an excellent carrier collection efficiency. The experimental 3-dB bandwidth of ~1 GHz agrees well with the theoretical calculation including series resistance and parasitic capacitance of the device. The bandwidth is expected to reach ~32 GHz with an optimized contact resistance as well as mesa diameter.

In addition, an improved QE was also demonstrated in uniformly tensile-strained GOI photodetectors. The tensile strain reduces the Ge bandgap and increases its band-to-band absorption coefficient, enabling an enhanced QE particularly at the tele-communication *L*-band (1,565 to 1,625 nm) and beyond. The uniform tensile strain is achieved by a patented recessed approach in placing silicon nitride ($SiN_x$) sidewall stressor. A self-aligned dry etching (SADE) method was introduced to remove the insulator ($SiO_2$) layer during the Ge waveguide-on-insulator (WGOI) patterning, followed by placing the tensile-stressed $SiN_x$ stressor at the waveguide sidewalls. A tensile strain of ~0.7% with an enhanced

uniformity was observed from the Ge WGOI with a 580 MPa-tensile $SiN_x$ stressor, using micro-Raman measurements, along the transverse direction of the waveguide. The corresponding metal-semiconductor-metal (MSM) photodetectors exhibit a ~70nm extension of the absorption coverage towards longer wavelengths and a ~2× enhancement on the QE (as well as the absorption coefficient) at 1,620 nm. An additional ~37% QE improvement was also established, compared to the detectors without employing SADE. Theoretical calculation tells that a 1.5 GPa-tensile stressor could extend the *Γ*-valley-heavy-hole and -light-hole bandgap edges towards ~1,665 and ~1,710 nm, respectively, covering the entire tele-communication bands. The results potentially facilitate a high-bandwidth and high-efficiency GOI photodetector at BEOL for integrated photonics. Suggestions have also been given to further improve the device performance. Furthermore, the concept of uniformly-straining Ge can be extended for the bandgap engineering of other semiconductor materials such as III-V and GeSn for a wide range of optoelectronic applications including light sources, electro-absorption modulators and photodetectors.

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# List of Symbols and Abbreviations

| | |
|---|---|
| 3-D | three dimensional |
| As | arsenic |
| ALD | atomic layer deposition |
| A/W | ampere per watt (the unit to measure responsivity) |
| B | boron |
| BEOL | back end of line |
| $Cl_2$ | chlorine |
| $CF_4$ | carbon tetrafluoride |
| CMOS | complementary metal-oxide-semiconductor |
| CMP | chemical mechanical polishing/planarization |
| Cu | copper |
| DWDM | dense wavelength division multiplexing |
| EA | electro-absorption |
| EPIC | electronic-photonic integrated circuit |
| EQE | external quantum efficiency |
| FEM | finite element method |
| FESEM | field emission scanning electron microscope |
| FIB | focused ion beam |
| FK | Franz-Keldysh |
| FWHM | full width at half maximum |
| Ge | germanium |
| GOI | germanium-on-insulator |
| HRXRD | high resolution X-ray diffraction/diffractometer |
| IQE | internal quantum efficiency |
| LiDAR | light detection and ranging |
| MSM | metal-semiconductor-metal |
| mT | millitorr |
| PD | photodetector |

| | |
|---|---|
| PECVD | plasma-enhanced chemical vapor deposition |
| QE | quantum efficiency |
| RIE | reactive-ion etching |
| RMG | rapid melting growth |
| RTA | rapid thermal annealing |
| SADE | self-aligned dry etching |
| sccm | standard cubic centimeters per minute |
| SEM | scanning electron microscope |
| $SF_6$ | sulfur hexafluoride |
| Si | silicon |
| $SiN_x$ | silicon nitride |
| SIMS | secondary ion mass spectrometry |
| SRH | Shockley-Reed-Hall |
| SRP | spreading resistance profiling |
| TEM | transmission electron microscope |
| TLM | transmission line method |
| TMAH | tetramethylammonium hydroxide |
| W | watt |
| WDM | wavelength division multiplexing |
| WGOI | waveguide-on-insulator |
| *W/H* | width-to-height ratio |
| *Γ*-HH | *Γ*-valley-heavy-hole |
| *Γ*-LH | *Γ*-valley-light-hole |
| $E_g^{LH}$ | Ge *Γ*-valley-light-hole bandgap |
| $E_g^{HH}$ | Ge *Γ*-valley-heavy-hole bandgap |
| $\varepsilon_{ij}$ | strain along *j*-direction induced by the stress along *i*-direction (*i*,*j* = *x*,*y*,*z*) |

# Chapter 1 Introduction

## 1.1 Background

### 1.1.1 Integrated Circuits: The Metal Interconnect Bottleneck

The advent of the first integrated circuit more than sixty years ago enabled miniaturized, powerful and economical electronic systems that are currently ubiquitous in our daily life, such as personal computers, cellular phones, wearable devices and many more. In past decades, innovation of the integrated circuits mainly focused on the down-scaling of transistors following Moore's Law [1] for reduced cost and improved performance. Thanks to this effort, an affordable and palm-sized smartphone nowadays owns a computing power far exceeding a supercomputer in the 1980s that occupied an entire room.

According to Moore's law, the number of transistors per unit area on a silicon (Si) chip doubles approximately every 18 months, which is equivalent to a scaling factor of ~0.7× on the physical dimension of the transistors. The transistor shrinkage follows well along this path till today, despite numerous technical challenges [2]. Novel semiconductor materials such as germanium (Ge) [3, 4] and III-V based semiconductors [5, 6], as well as novel structure designs such as FinFETs [7] and nanowires [8, 9], have been introduced to address the challenges and continuously enhance the transistor performance. However, there was a diminishing return found from the performance improvement of a CPU

along with the exponential growth of the transistor counts, which is called the “Moore’s Gap” (Fig. 1). For example, Intel Pentium-4 owns a ~50% more transistor count than that of Pentium-3, while only demonstrating a ~15% performance improvement [10]. One reason for this inefficiency pertains to the longer propagation delay from the metal interconnect wires that hinders the communication between the central processing unit (CPU) and memory, as shown in Fig. 2 (a). As the number of transistors per unit area increases, the gate delay from individual transistors decreases due to the reduced gate capacitance. On the other hand, the delay from the interconnect wires, especially at global level, increases drastically due to the increased wire length and density as well as its decreased cross-sectional area, in order to accommodate the wiring among the exponentially-increasing transistors. The increased wire length and shrunken cross-sectional area leads to a higher wire resistance *R*, while the increased wire density results in a higher inter-wire parasitic capacitance *C*. Both the increase prolong the *RC* time delay in data transmission and switching, hindering the performance enhancement of CPUs. Although lower-resistivity copper (Cu) metallization and low-*k* inter-metal dielectrics had alleviated this bottleneck, the projected total delay would still be a hurdle for the technology generations below 100nm.

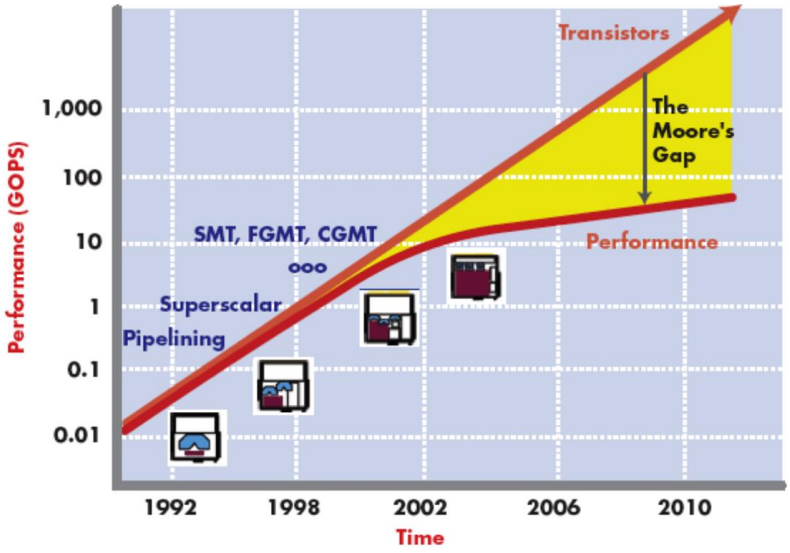


Figure 1 The Moore's gap: an increasing gap between the number of transistors and CPU performance [10].

Another reason is due to the chip heat dissipation. As seen from Fig. 2 (b), the CPU power density would have been surprisingly comparable to that of a rocket nozzle by 2010, if the conventional scaling rules had rigorously been followed. The excess heat partly comes from the aforementioned longer and thinner interconnect that increases its resistance $R$. Besides, the pursuit of a higher chip speed also makes the CPU more power-greedy, since its dynamic power dissipation ($CV^2f$, where $C$ is the gate capacitance and $V$ is the transistor supply voltage) increases with the clock frequency $f$ [11]. The resulting elevated chip temperature would accelerate the chip reliability degradation and shorten its lifetime. That is why Intel abandoned a higher clock-speed Pentium-4 design in 2004 and replaced with a dual-core architecture [12]. Although the multi-core processors could lower the chip power dissipation without compromising the CPU speed, by offering parallelism in computing, its power density would go up again when more cores are integrated, due to a more complicated wiring scheme required for inter-core

communications [13]. Therefore, the root cause for the excess power dissipation still lies on the metal interconnects.

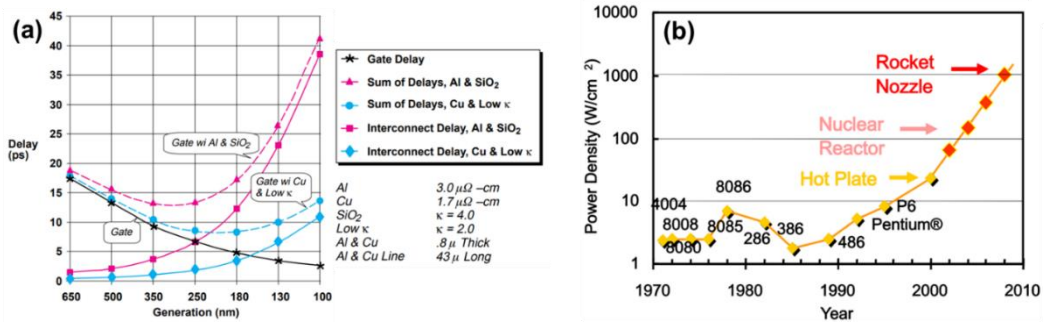


Figure 2 Two main reasons for the diminishing gain in CPU performance: (a) RC delay (courtesy of SIA: The National Technology Roadmap for Semiconductors (1997)) and (b) heat dissipation (courtesy of Intel).

In addition, the current era has witnessed a massive demand of data traffic. According to Cisco's analysis, the global Internet traffic in 1992 was only ~100 gigabytes (Gb) per day; while ten years later, in 2002, the data transmission drastically increased to ~100Gb per second and is estimated to be ~105 terabyte (Tb) per second in 2021 [14]. Although state-of-the-art fiber-optic communication at long-haul could manage to keep up with this fast-growing need, the metal interconnects mainly used at shorter (*i.e.* rack-to-rack, inter- or intra-chip) links, due to the aforementioned latency and power dissipation constraints, would definitely become one of the major obstacles. Furthermore, there are also more and more emerging applications involving bandwidth-hungry communications, such as high definition video gaming, cloud computing, Internet of Things (IOTs), autonomous driving, augmented reality and many more. Among them, IOTs are typically applied at shorter distances (i.e. inter-homes or -buildings); while autonomous driving and cloud computing also depend excessively on short-reach interactions within

data centers. These trends would make metal interconnects even more challenging to survive due to their bandwidth limitation caused by the skin effect and inter-/intra-level dielectric leakage at higher frequencies [15]. Therefore, an alternative solution is highly desired to alleviate the bottlenecks of latency, bandwidth and power dissipation at short-reach interconnects.

### 1.1.2 Optical Interconnects: A Potential Solution

Analogous to the concept of state-of-the-art long-haul fiber-optic technologies, optical communication can be further extended towards shorter-reach levels, especially at a chip scale where the metal interconnects are in charge for the data communication. The chip-level optical communication system is termed as “optical interconnects” [16]. Optical interconnects can act as a viable solution to the metal interconnect bottlenecks, since multiple advantages which fiber-optics owns would be similarly brought to the short-reach levels, including high speed, large bandwidth, reduced power dissipation and many more. First, the adoption of optical waveguides eliminates the *RC* delay problem for the electrons in metal interconnects. Second, photon propagation in the waveguide does not generate any heat, enabling a reduced power dissipation in data transmission and thus improves chip performance and reliability. Besides, unlike electrons in metal wires, photons with different wavelengths can be simultaneously transmitted in one waveguide without any interference with each other. This wavelength division multiplexing (WDM) scheme, without complexity in wiring, would enable an interconnect system with thousands of times enhancement in bandwidth. For instance, if a

wavelength interval of ~0.5nm is selected per channel, ~200 channels can be accommodated across the tele-communication *C*- and *L*- bands (1530~1625nm). Assuming a bit rate of ~10Gbit per second is introduced per channel, a total data rate of 2Tbit per second would be anticipated, which is orders of magnitude higher than that of the metal interconnects. Fig. 3 depicts the schematics of applying optical interconnects to address the multi-core wiring problem as mentioned in Chapter 1.1.1. In this all-to-all communication (ATAC) platform [17], a layer for optical interconnects is incorporated into the conventional Si complementary metal-oxide-semiconductor (CMOS) circuits (Fig. 3 (a)). Inter-core (i.e. global level) data transmission and intra-core processor-memory communication would be handled by the high-bandwidth optical interconnects, which can be extended and split to local levels closer to individual transistors where the RC delay becomes minimal. The chip power consumption thus comes only from the optical-electrical signal conversion as well as the local electrical interconnects and transistors. Fig. 3 (b) shows the top-view of the ATAC system.

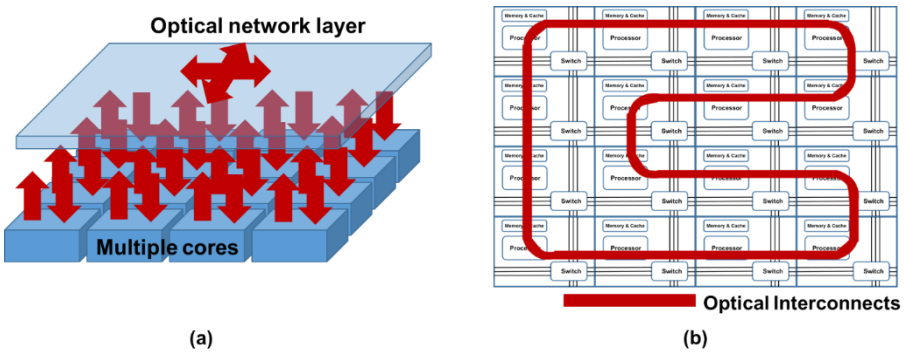


Figure 3 Schematics of an ATAC multi-core system incorporating optical interconnects from (a) 3-D view and (b) top-view [17].

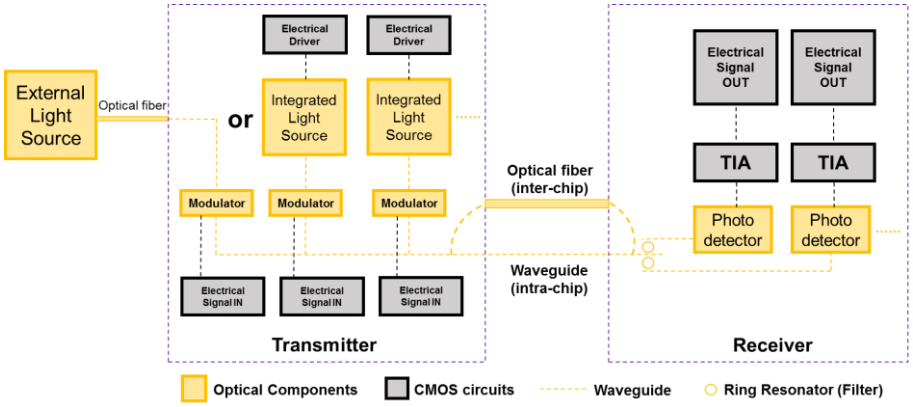


Figure 4 Schematic of an optical transceiver system with essential components.

In order to realize a fully-functional optical interconnect system, a number of components are essential: light source (laser or LED), modulator, photodetector and waveguides linking all these components. Fig. 4 shows the schematic of a common optical transceiver system for transmitting and receiving optical signals, from and towards the CMOS circuits, respectively. The light source, depending on the end application, can be either external [18, 19] or monolithically- [20, 21] and heterogeneously-integrated [22, 23]. The generated light is coupled into waveguides and sent to modulators. The modulators add “low” and “high” intensity contrast to the light which corresponds to the feeding electrical “0” and “1” signals from the CMOS circuits. The modulated light is then transmitted either via the global-level waveguides (intra-chip) or optical fibers (inter-chip) to the receivers, where the photodetectors are used to transform the optical signals back to electrical ones for the CMOS circuits to process the received data. In a WDM scheme, filters such as ring resonators can be used to de-multiplex the wavelengths to the desired photodetectors.

### 1.1.3 CMOS Compatibility for Optical Interconnects: The need for Germanium and Germanium Photodetectors

Since the optical interconnects essentially works as part of the CMOS circuitry, its comprising components are inevitable to be realized on Si (which is also the reason for the name “silicon photonics”) and thus preferred to be CMOS-compatible. A CMOS-compatible solution could facilitate a mass production with a reduced cost. Although extensive research [24-26] has been carried out by incorporating III-V based materials for optical interconnects, especially for integrated light sources, foundries are still concerned about their compatibility with CMOS. This is because the group-III and -V elements can be effective dopants into Si to affect its materials characteristics and transistor performance. Moreover, processing III-V materials are complicated and costly. In contrast, Si itself is a good material for low-loss waveguides due to its optical transparency at 1.3 and 1.55μm tele-communication wavelengths (Fig. 5) and its high refractive index contrast ($\Delta n \sim 1.9$) with respect to its native oxide $SiO_2$ [27]. High performance optical modulators on Si can also be realized utilizing the free carrier effect [28, 29] and the Pockels effect [30, 31]. However, it is also the optical transparency that limits Si for efficient photodetectors. Although the utilization of the defect state-based optical transition could enable a Si detector working at the tele-communication wavelengths [32], the corresponding quantum efficiency (QE) is insufficient and a high voltage bias (i.e. substantial power consumption) is required to obtain a

satisfactory responsivity and 3dB bandwidth. Besides, the indirect bandgap nature of Si hinders the development of an integrated light source. Hence, alternative CMOS-compatible materials are necessary as a supplement to realize the remaining parts.

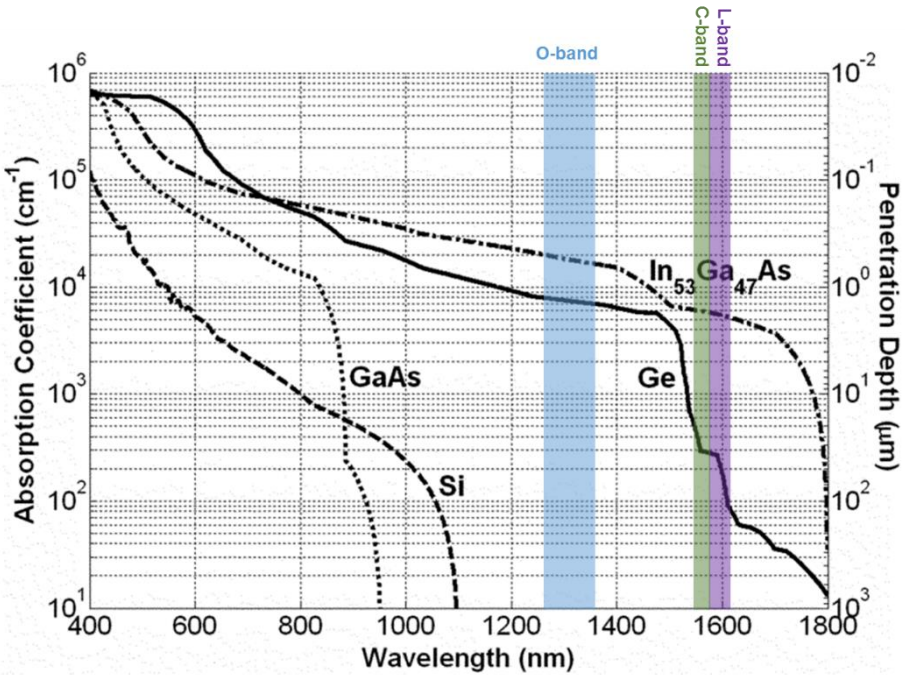


Figure 5 Absorption coefficients for various semiconductors [33]. Coverage of some key tele-communication bands are also indicated.

In recent years, with the success in high-quality Ge-on-Si epitaxy to overcome the ~4.2% lattice mismatch [34], Ge turns out to be one of the promising candidates. Over a long time in the history of CMOS development, Ge has played an important role and demonstrated a proven compatibility with CMOS process. The world's first transistor was made of Ge; Decades later, it was adopted as the transistor channel material due to its high carrier mobility, low effective mass and better compatibility with high-*k* gate dielectrics [35]. Second, as shown in Fig. 5, Ge has a direct bandgap of ~0.8eV at the *Γ*-valley, corresponding to a considerable optical absorption coverage towards the *C*- and *L*- tele-

communication bands for photodetectors [36-38]. Besides, by slightly incorporating Si, the absorption edge of Ge can be tuned to a desired wavelength up to ~1.55μm, where the Franz-Keldysh (FK) effect [39, 40] can be utilized for electro-absorption (EA) modulators [41] at the *C*-band. In such devices, the intensity of the light passing through can be modulated via the electric field-induced absorption variation, with a quicker modulation response and lower energy consumption compared to that of the Si counterparts mentioned above. More inspiringly, Ge has also demonstrated the significance as an integrated light source [42, 43], owing to its quasi-direct bandgap nature with its *L*-valley conduction band minimum only ~136meV lower than the *Γ*-valley minimum. Therefore, a fully-functional optical interconnect system could potentially be established, with the involvement of Ge. In addition, it is worthy to mention that, since Ge is lattice-matched with GaAs, it could reversely contribute to a high-quality III-V optical integration on Si as a buffer layer [25, 44].

Among these devices, Ge photodetectors have been well known for their excellent performance. Responsivities ranging from 0.2 to 1 A/W were reported, at a broad spectrum from 850 to 1550nm, for normal-incidence type detectors (Fig. 6 (a) and (b)) [45-47]. The responsivities vary depending on their Ge layer thicknesses. Typical 3dB-bandwidths for these detectors span from few GHz to ~50 GHz [48, 49]. However, there is a trade-off between the responsivity and bandwidth. A thicker Ge layer enhances the photon absorption, bringing higher responsivities; but it at the same time increases the carrier transit time to the electrodes, degrading its 3dB-bandwidth. Therefore, waveguide-integrated detectors

(Fig. 6 (c) and (d)) were developed, separating the paths for the photon absorption and carrier transition to alleviate the trade-off. Both high responsivity at ~0.8 to 1.2 A/W [50, 51] and high 3dB bandwidth over ~60 GHz [52] have thus been achieved. Meanwhile, since Si is a good material for waveguides, the waveguide-integrated design simplifies the integration for on-chip optical interconnects. Alternatively, Ge avalanche photodiodes (APD), by amplifying the absorbed carriers via avalanche multiplication, also offers a superior sensitivity and gain-bandwidth product that are useful for low-input-power and high-speed detection [53]. Thanks to these efforts, state-of-the-art Ge optical receivers have achieved ~100Gb/s data rate operation [54].

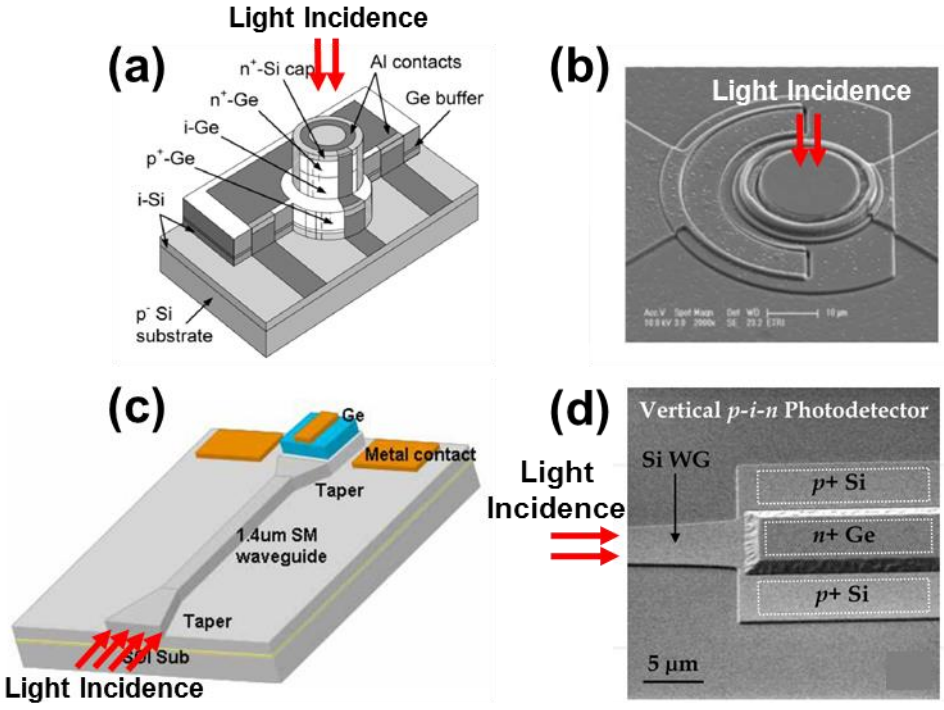


Figure 6 Schematic diagrams of a (a) normal-incidence type Ge photodetector [49] and (c) waveguide-integrated type Ge photodetector [50]. A scanning electron microscopy image of the respective type are shown in (b) [47] and (d) [55], respectively. The directions of light incidence are also indicated.

## 1.2 Motivation and Objectives of the Thesis

A photodetector with a higher QE, namely responsivity, would benefit from a higher optical-to-electrical conversion efficiency. A lower optical power would thus be detected beyond the noise level of the detector and less amplification power would be spent on the output transimpedance amplifier (TIA) circuit. Despite the excellent performance, Ge photodetectors still possess QE constraints, mainly at two aspects. First, a high QE might still be a challenge for the detectors on novel Ge platforms other than the Ge-on-Si and Ge-on-SOI. Approaches in addition to conventional epitaxy have to be involved in forming such platforms and this sometimes results in difficulties realizing detector structures that are common to Ge-on-Si and -SOI substrates. For example, germanium-on-insulator (GOI) is a novel material platform developed for high-quality Ge with electrical isolation to the Si substrate [56]. Photodetectors on GOI could reveal merits such as reduced dark current and eliminated carrier diffusion from Si below ~1.1μm where Si is absorbing [57]. In addition, GOI could serve a number of photonic applications such as mid-infrared data communication [58, 59], bio-medical sensing [60] and many more. With these capabilities, conventional bulky systems such as Fourier-transform infrared spectroscopy (FTIR), Raman spectroscopy and mechanical rotator-based light detection and ranging (LiDAR) system could be miniaturized onto a chip at an extreme low cost. However, most of the demonstrated detectors on GOI are with normal-incidence type and planar electrodes [57, 61, 62], which is limited by the methods for GOI formation. Hence, a thicker Ge layer is unable to effectively collect more

photon-generated carriers for a higher QE. This is due to the lack of feasible approach to realize a vertical *p-i-n* structure to efficiently collect the carriers. Therefore, this thesis will first attempt to address this limitation to design and fabricate a normal-incidence vertical *p-i-n* photodetector on the GOI platform to increase its effective absorption thickness.

Second, high QE is also a challenge for the Ge detectors at longer wavelengths into the *L*-band and beyond. This is due to the crossing of the incident wavelength over the Ge direct (*Γ*-valley) bandgap edge that cuts off its inter-band absorption. Although the *in-situ* ~0.2% biaxial tensile strain, resulting from the Ge-on-Si epitaxy, reduces the bandgap of Ge and enhances its absorption coefficient at the *L*-band [63, 64], the detector responsivity is still considerably low beyond ~1580nm. However, as explained in Chapter 1.1.1, with the increasing data communication traffic, an optical interconnect network with a wider bandwidth would be of great demand in the future. Consequently, a Ge detector with a wider absorption coverage would definitely benefit such network by providing a wider bandwidth under the WDM scheme. Therefore, the second part of the thesis will focus on developing a GOI detector with a further-extended absorption coverage, by inducing a uniform tensile strain in Ge. The tensile strain further reduces the bandgap of Ge, which increases its absorption coefficient at a longer wavelength and consequently facilitates a detector with a higher QE, without losing its CMOS compatibility. A method to enhance the strain uniformity was introduced by tensile-stressed silicon nitride ($SiN_x$) stressors placed at the Ge waveguide

sidewalls and recessed into the substrate layers beneath Ge. Meanwhile, the bonding and layer transfer method utilized for the GOI formation would enable a high-density back-end-of-line (BEOL) integration for the detectors via vertical stacking.

To sum up, the main objective of this thesis is to enhance the QE of the photodetectors on the GOI platform formed via the bonding and layer transfer (etch-back) approach. Two solutions are proposed and investigated, namely, to realize an abrupt vertical *p-i-n* structure along the GOI fabrication for a longer absorption path and to realize a uniformly tensile-strained Ge via the CMOS-compatible $SiN_x$ stressor for a higher absorption coefficient.

## 1.3 Major Contributions

The major contributions of this thesis are listed as follows:

- Successfully demonstrated normal-incidence vertical *p-i-n* GOI photodetectors with a dark current density of 47 mA/cm$^2$ and an optical responsivity of ~0.39 A/W, which are prominently improved compared to state-of-the-art GOI photodetectors. An internal quantum efficiency of ~97% also verifies an efficient carrier collection in the devices by using the vertical *p-i-n* structure.
- Developed a patented approach of using recessed $SiN_x$ stressor to introduce a uniform tensile strain in Ge, which is verified both theoretically and experimentally. A ~0.7% tensile strain transversely along the Ge waveguide-on-insulator was

determined, by applying the recessed $SiN_x$ stressor with its tensile stress of 580 MPa.

- A ~70 nm extension of the absorption coverage towards longer wavelengths and a ~2× enhancement on the absorption coefficient was obtained from the GOI metal-semiconductor-metal (MSM) photodetectors utilizing the 580MPa-tensile recessed $SiN_x$ stressor.

## 1.4 Organization of the Thesis

Chapter 2 gives a background study on the GOI material and its devices. The technical merits offered by GOI will first be elaborated on. The methods in realizing the GOI will then be compared to illustrate the advantages of bonding and layer transfer (via etch-back) method for BEOL integration. Lastly, a literature review on state-of-the-art GOI photodetectors will be conducted.

Chapter 3 lays the theoretical foundation of this thesis. Background knowledge on the QE of photodetectors will first be introduced, revealing the viable options for the QE enhancement. Afterwards, prior work relevant to the engineering of the absorption length and coefficient for a higher-quantum-efficiency Ge photodetector and the strain engineering for a higher-performance Ge laser will be reviewed, shaping the solutions of forming a vertical *p-i-n* structure and applying a tensile-stressed recessed $SiN_x$ sidewall stressor in this thesis. The chapter will continue with a review on the theory linking between the Ge strain and its

absorption coefficient, and finally end with a literature study on the deposition of highly-stressed $SiN_x$ stressors.

Chapter 4 focuses on the fabrication and characterization of a vertical *p-i-n* structure on a GOI platform for the high-efficiency photodetectors.

Chapter 5 discusses the development and characterization of the high-efficiency GOI photodetectors realized on the vertical *p-i-n* structure in Chapter 4.

Chapter 6 elaborates on the development of a uniformly tensile-strained Ge waveguide-mesa towards a high-efficiency GOI photodetector. Recessed $SiN_x$ stressor-strained Ge waveguide-on-insulator (WGOI) will be demonstrated with an enhanced strain magnitude and uniformity both theoretically (via finite element method calculation) and experimentally (via CMOS-process fabrication).

Chapter 7 presents the fabrication and characterization of the $SiN_x$-strained metal-semiconductor-metal (MSM) photodetectors on GOI, based on the $SiN_x$-strained Ge WGOI developed in Chapter 6. Suggestions for the process optimization of the GOI MSM photodetectors will also be proposed. Finally, the effect of $SiN_x$ stress and waveguide structural parameters on the Ge tensile strain will be studied. A theoretical limit of the recessed $SiN_x$ technology on the extension of the absorption range will also be proposed.

Chapter 8 summarizes the results in this thesis and propose the directions for future research.

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# Chapter 2 Germanium-on-insulator (GOI): Towards Advanced Electronic-photonic Integration

## 2.1 Technical Merits Offered by GOI: Materials, Devices and Integration

As discussed in Chapter 1, Ge has been demonstrated with excellent electronic and photonic properties such as superior carrier mobility and considerable optical absorption at tele-communication wavelengths for advanced transistors and photonic-integrated circuits, respectively. Inserting an insulator layer beneath the Ge, germanium-on-insulator (GOI) could further provide a number of advantages that can benefit optoelectronic applications. First, the insulator layer serves as an electrical isolation and diffusion barrier between the Ge and the bulk Si substrate. The electrical isolation benefits the electrostatic control of Ge CMOS such as suppressed short channel effects and reduced parasitic capacitance [1, 2]. Furthermore, Ge photodetectors developed on-insulator could prevent the slow carrier diffusion from the underlying Si at the wavelengths where Si is absorbing (<~1.1μm) [3, 4]. Meanwhile, Si up-diffusion is also impeded compared to that in Ge-on-Si epitaxy, which could degrade the Ge quality. Second, compared to the direct Ge epitaxy on Si, GOI could minimize the misfit dislocations generated at the Ge/Si interface for a better film quality. For example, chemical-mechanical polishing (CMP) [5] and furnace annealing [6] could be utilized to reduce

the misfit dislocations in the GOI formed by bonding and layer transfer. Aspect ratio trapping [7] could be used to locally reduce the Ge threading dislocation density by lateral over-growth. A lower dislocation density could help reduce the dark current density of the photodetectors for low-noise detection [8]. Third, the generally-lower refractive index of the insulator materials could improve the optical confinement in a Ge waveguide at the mid-infrared region and simultaneously provide a higher mode overlap with the chemical or bio-medical analytes outside the waveguide for a more sensitive sensor [9].

In addition, the selection of the insulator material can be flexible for diversified applications. For example, high-*k* dielectrics (e.g. $Al_2O_3$ and $HfO_2$) can be used to continue the transistor downscaling with a reduced gate leakage. The Ge/insulator interfacial quality could also be improved simultaneously for a better carrier transport [10, 11]; while the low-*k* dielectrics [12] could potentially facilitate a back-end-of-line (BEOL) three-dimensional (3-D) integration. For mid-infrared photonics applications, for example, cladding materials such as $SiN_x$ [9, 13], sapphire [14], chalcogenide glasses [15] and $CaF_2$ or $Y_2O_3$ [16] could offer diversified sensing spectra covering a wide range of molecules-of-interest. Therefore, all these advantages could facilitate GOI as a platform for advanced electronic-photonic integrated circuits (EPICs) across a broad spectrum ranging from the near- to the mid-infrared (Fig. 7). This potential is further verified by the recent reports of lasers [17], carrier-injection modulators [18], photodetectors [4, 19, 20] and other passive components [21] developed on the GOI platform. It is noteworthy that the etching

selectivity between the $SiO_2$ and Ge, using buffered oxide etchant, acts as an additional advantage for the GOI enabling a fully-suspended structure for the aggregation of the tensile strain for laser applications.

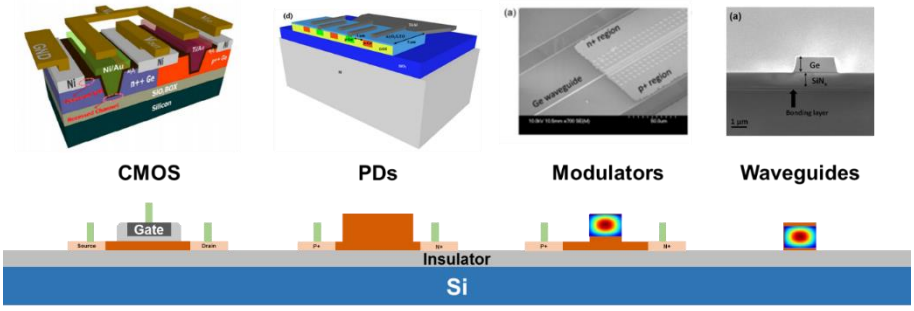


Figure 7 A schematic of a GOI platform enabling a Ge-based EPIC. Examples of a CMOS [22], photodetector [4], modulator [18] and mid-IR waveguide [9] demonstrated on GOI were included.

On the other hand, GOI enables the integration of optical interconnects by vertically stacking the Ge electronic-photonic layer on top of the Si CMOS, similar to the schematic depicted in Fig. 3 (a). This concept of 3-D integration exhibits the advantages of a smaller form factor and a flexibility in system design. Since the area occupied for photonic devices (in ~µm size) in a monolithic integration (e.g. by Ge epitaxy on Si) is much larger than that of the transistors (in ~nm size), the vertical stacking could significantly save the chip area for a denser integration. Meanwhile, the Ge-based devices can thus be flexibly designed and located with an optimal wiring configuration to the transistors, minimizing signal delay and power consumption. In order to realize the vertical stacking, the Ge layer has to be integrated at the BEOL among the inter-metal dielectric layers. This requires the GOI to be realized at a thermal budget below ~450$^{o}$C, as shown in Fig. 8. Hence, in the next section, existing methods in forming a GOI will be reviewed and compared, and

the advantages of bonding and layer transfer (etch-back) for the BEOL integration will be discussed.

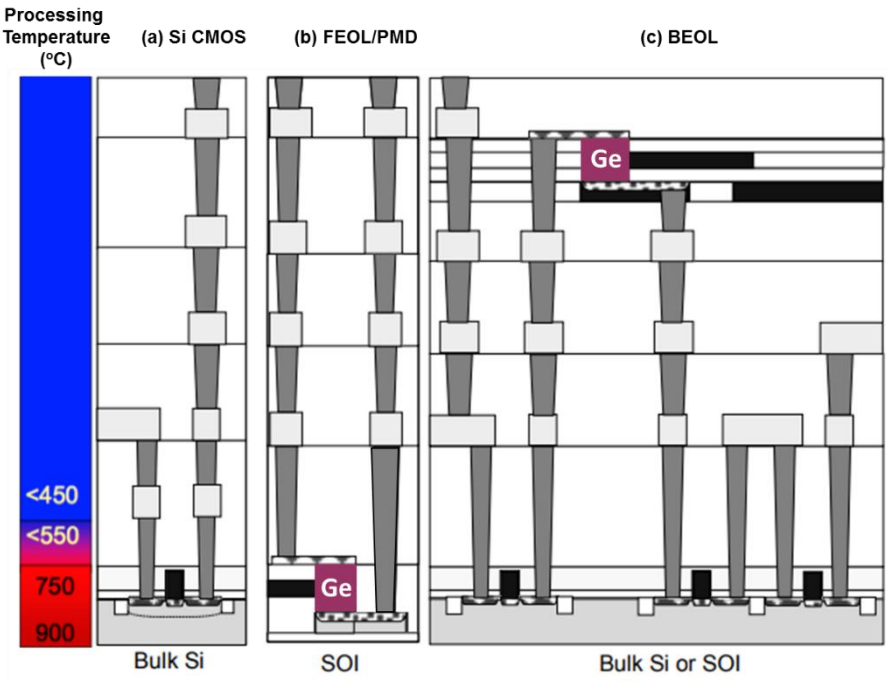


Figure 8 Cross-sectional schematics of a (b) Ge FEOL-integrated and (c) Ge BEOL-integrated EPIC. The schematic of a Si CMOS is shown in (a) as a reference. The scale bar on the left indicates the processing temperature with respect to the distance from the substrate [23].

# 2.2 Methods for GOI Fabrication

For the past few decades, numerous synthesis methods have been developed in realizing a GOI platform, including Ge condensation, rapid melting growth, Ge lateral over-growth and wafer bonding and layer transfer. In this section, these methods will be briefly reviewed and compared, to propose a practical solution that can be used for BEOL integration.

## 2.2.1 Ge Condensation

The Ge condensation technique is based on the selective dry oxidation of Si rather than Ge in the epitaxial $Si_{1-x}Ge_x$ layer on silicon-on-

insulator (SOI) substrate. Because the diffusion coefficient of Si is much faster than that of Ge, the dry oxidation keeps depleting the Si atoms to form $SiO_2$ while accumulating the Ge until a residual of ~0.03% Si [24], which consequently results in a Ge film on the thermal oxide layer. The schematic of this mechanism is shown in Fig. 9. This technique requires a high thermal budget (>900$^{o}$C) for the oxidation and the resulting Ge layer is generally thin (<100nm) [25]. Therefore it can be used for realizing high-mobility Ge channels in advanced transistors. The crystal defects generated during the condensation also pose additional challenges for the wide adoption of this technique [26].

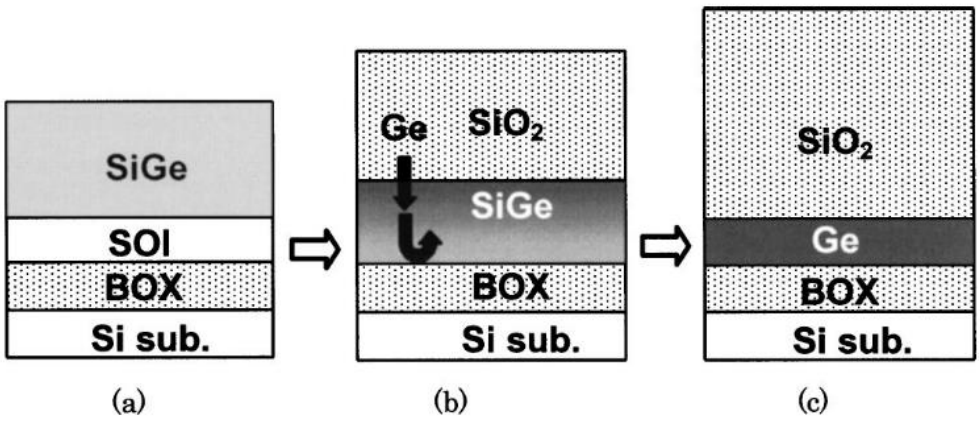


Figure 9 GOI fabrication process by the Ge condensation enabled by dry oxidation technique [24]: (a) SiGe epitaxy; (b) dry oxidation and Ge accumulation; (c) GOI formation.

## 2.2.2 Rapid Melting Growth

Rapid melting growth (RMG) [27, 28] resembles the mechanism of the conventional Czochralski crystal growth to form a high quality Ge on insulator layers. It utilizes a rapid thermal annealing (RTA) over the Ge melting point (~937$^{o}$C) to crystalize the amorphous/polycrystalline Ge deposited on the insulator. The Ge needs to be partially in contact with

the Si substrate beneath the insulator as the seed for the crystallization. An oxide cap layer was also required to fully encapsulate the Ge structure as a self-aligned micro-crucible holding and shaping the molten Ge. The corresponding cross-sectional schematic of the RMG is shown in Fig. 10. The insulator layer also serves the purpose of defect necking to prevent the propagation of the dislocations generated due to the Ge/Si lattice mismatch into the area on top of the insulator layer. Therefore, the resulting Ge film can be of high quality. A defect density lower than ~$5 \times 10^5$ $cm^{-2}$ was reported [29]. This technique is completely CMOS-compatible and can be implemented together with the well dopant activation. The crystal orientation of the grown Ge can also be controllable depending on the Si seed. However, a high crystal quality can only be obtained in a strip-shaped structure with its width smaller than 5μm [30]. Also, the thermal budget is still very high considering the BEOL integration.

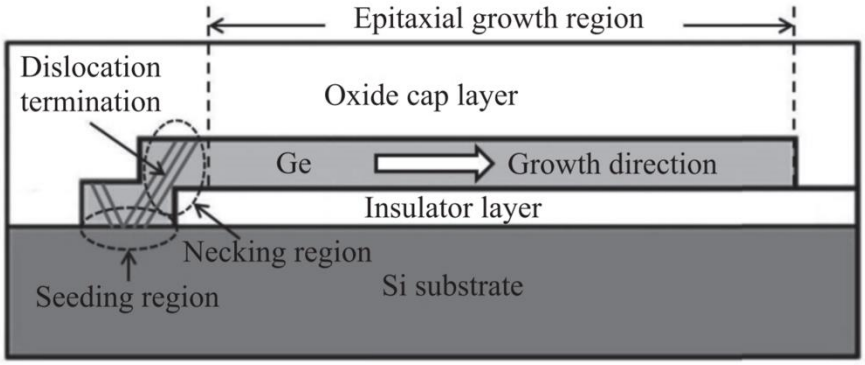


Figure 10 Cross-sectional schematic of the RMG [27].

## 2.2.3 Lateral Over-growth

Ge lateral over-growth is another monolithic integration approach for high-quality Ge-on-insulator. The insulator layer, typically $SiO_2$, was

deposited and patterned into strips to expose the Si growth windows for subsequent Ge selective epitaxy. As shown in Fig. 11, due to the selectivity between the Si and $SiO_2$, the Ge epitaxy fills the Si windows first and then starts to grow laterally on the $SiO_2$ surface until the coalescence of the growth fronts to form a complete film. Similar to the RMG, the $SiO_2$ sidewalls in the growth window trap the dislocations away from the "on-insulator" areas, where a high quality film is thus achieved. In addition, the trapped dislocations could further glide and coalesce under a post-growth hydrogen annealing (at 825°C) to further reduce the defect density (to ~1 to $4 \times 10^6$ $cm^{-2}$) and surface roughness [7]. Furthermore, unlike the RMG, this approach can produce a larger film area for a higher manufacturing throughput. However, Yu *et al.* [31] mentioned that a 600°C growth is required for a prominent lateral coalescence of the film on the insulator, following the Ge nucleation and window filling at 400°C, which indicates a trade-off between the final film quality and thermal budget. Besides, complicated optimization of the growth parameters and window orientation [32, 33] is needed to eliminate the voids formed at the coalescence position for a complete film, which might hinder its wide industrial adoption.

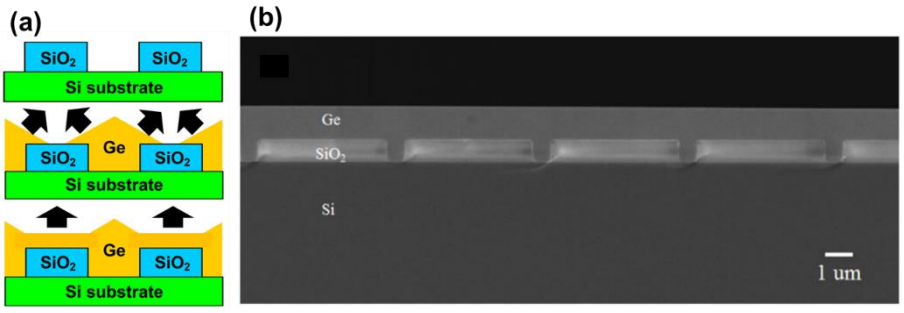


Figure 11 (a) a schematic diagram showing the Ge lateral over-growth [31]; (b) an SEM image showing the lateral-grown Ge layer on $SiO_2$ after CMP [32].

## 2.2.4 Bonding and Layer Transfer

The bonding and layer transfer technique heterogeneously integrates a Ge film, either from a bulk Ge wafer [34, 35] or an epitaxial-grown Ge layer on a Si donor wafer [36, 37], to an “on-insulator” Si handle wafer via fusion bonding. The resulting GOI is thus at wafer-level scale. The fusion bonding is one of the key enablers for 3-D integration [38] and comprises of stringent surface treatments (including surface planarization and activation, etc.) for a hydrophilic interface between the two joint wafers, where strong inter-atomic bonds, as that in the material bulk, are thus formed via post-bonding thermal treatment. The bulk Ge wafer could provide an almost dislocation-free transferred layer but could not be scaled up for a GOI wafer larger than 200mm [36]; while the epi-Ge-on-Si wafers contain a threading dislocation density of ~$10^7$ $cm^{-2}$ but can be scalable to the wafer diameter of 300mm and larger.

Main layer transfer methods include *Smart Cut*™ [39] as well as grinding and etch-back [5, 36, 37]. The former leaves a Ge film by layer splitting initiated by a hydrogen implantation, followed by thermal treatment, while the latter completely removes the substrate by wafer grinding and selective chemical etching. Fig. 12 depicts the corresponding schematic process flow. Both methods have pros and cons and can be selected based on specific applications. For example, the donor wafer can be reused after the *Smart Cut*™ splitting to save cost, while it will be completely consumed during the etch-back. The hydrogen implantation has depth limitation and cannot be applied to leave a thick Ge film, while the etch-back could easily control the final Ge thickness and surface

roughness due to the etching selectivity. In addition, the thermal treatment (400-600$^{o}$C) in the *Smart Cut*$^{TM}$ splitting may exceed the thermal budget allowed for the BEOL integration, while the etch-back was carried out close to room temperature. CMP is usually performed after the layer transfer to obtain a smooth surface on the residual Ge film, which could simultaneously remove the highly-dislocated epi-Ge close to the Ge/Si interface (now exposed at the top of the structure) and improves the ultimate film quality for a superior device performance.

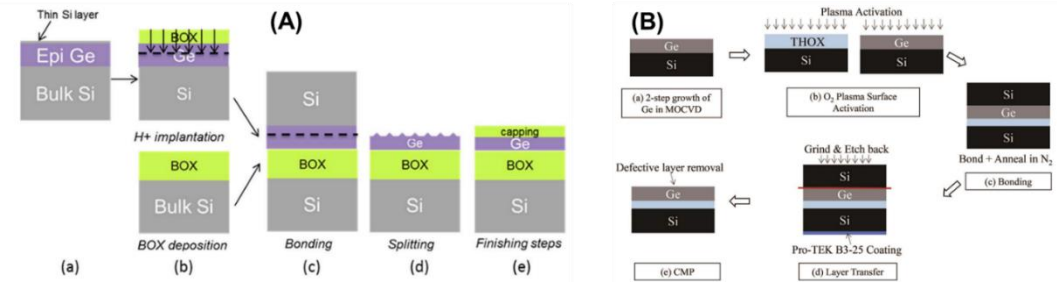


Figure 12 Schematic process flow for the wafer bonding and layer transfer of an epi-Ge layer to form a GOI involving (A) *Smart Cut*$^{TM}$ [40] and (B) grinding and etch-back [41] techniques.

## 2.2.5 Summary

To summarize, research efforts have been dedicated in developing robust and versatile methods for GOI fabrication, by which GOI with excellent Ge quality has been achieved. As mentioned, in order to facilitate the BEOL integration, thermal budget is the upmost concern. Table 1 lists the advantages and drawbacks of the respective methods reviewed above. Comparing among the methods, monolithic integration approaches including Ge condensation, RMG and lateral over-growth all requires high thermal budget for a good-quality Ge directly on the Si CMOS, while the bonding and layer transfer allows the high-temperature

Ge epitaxy being carried out on another Si, instead of the CMOS wafer, to bypass the thermal budget. Additionally, unlike the Smart Cut$^{TM}$, the etch-back can be performed at room temperature, which further saves the thermal budget. By introducing $O_2$ plasma surface activation, the post-bonding annealing temperature can be reduced from 800 to 300$^{o}$C [42], which also meets the thermal budget requirement. Apart from that, the etch-back method exhibits versatility on the final Ge thickness and can be potentially scalable to all wafer sizes for mass manufacturing. The final Ge quality is also acceptable and can be improved by CMP. The use of epi-Ge wafers saves the cost compared to that of the costly Ge wafers, which compensates the cost increase due to the unrecyclable Si removal. Therefore, the wafer bonding and layer transfer method with etch-back ends up to be an enabling technique for the Ge BEOL integration. Fig. 13 shows a corresponding schematic for the demonstration of the concept.

Table 1 Comparison among the GOI fabrication methods.

| Methods | | GOI quality | Ge thickness | Process complexity | Scale | Maximal thermal budget |
|---|---|---|---|---|---|---|
| Ge condensation | | Medium | Limited (difficult to be micron-thick) | Low (but time-consuming) | Wafer | High (>900°C) |
| RMG | | Excellent | Limited (difficult to be nanometer-thin) | High | Local (in width of microns) | High (940°C) |
| Lateral over-growth | | Excellent | Not limited | High (complicated for void-free film) | Wafer | High (600-825°C) |
| Bonding and layer transfer | Smart Cut™ | Excellent (for bulk Ge) | Limited (by $H^+$ implant depth) | Medium | Wafer (bulk Ge: ≤200mm; epi-Ge: scalable to all diameters) | Medium (400-600°C) |
| | Etch-back | Good (for epi-Ge) | Not limited | Medium | | Low (300°C) |

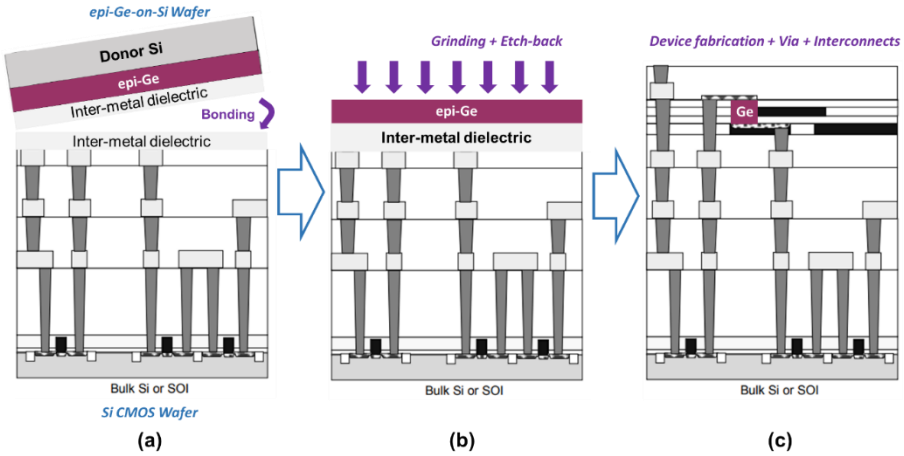


Figure 13 A schematic process flow for the use of the bonding and layer transfer technique incorporating the etch-back method for Ge BEOL integration.

## 2.3 Photodetectors on GOI

There are only a few reports on the development of a photodetector on germanium-on-insulator. For the normal-incidence detectors, Jain *et.al.* [5] reported metal-semiconductor-metal (MSM) photodetectors on a GOI fabricated by bonding and layer transfer. Only normalized photocurrent was shown, implying an indistinctive QE. Likewise, a weak responsivity of 1.56mA/W was found in the paper by Tani *et.al.* [20], for lateral normal-incidence *p-i-n* diodes on a GOI formed similarly. Lateral *p-i-n* diodes were also presented by Nam *et.al.* [4] on a lateral over-grown GOI. However, the responsivity is still limited at ~0.1 A/W at 1550nm.

Regarding the waveguide-integrated photodetectors, Assefa *et al.* [43] developed a MSM photodetector on a GOI formed by RMG, with a responsivity of 0.14A/W at 1.5μm and a 3dB bandwidth exceeding 35GHz. The relatively low responsivity was attributed to the Si-Ge inter-diffusion during the RTA. However, as mentioned, RMG needs a high thermal budget and is challenging to be used for BEOL integration. Chen

*et al.* [19] also demonstrated a MSM detector on a GOI formed by wafer bonding and layer splitting. A QE above 90% with a responsivity over 0.4A/W was reported. However, the bonding interfacial insulator layer must be kept thin for an efficient optical coupling, which tends to limit the versatility of the platform as well as the wafer-scale bonding quality since Bao *et al.* [41] recently observed GOI bonding quality degradation with thin intermediate oxide. Hence, both the devices are not suitable for the BEOL integration.

As a result, although a high quality Ge could be obtained by forming a GOI structure for a reduced dark current of the photodetectors, the reported normal-incidence detectors suffer from a low responsivity. This is due to their inter-digitated configuration of the metal contacts (Fig. 14) that are planar on the Ge surface, which could not efficiently collect the photon-generated carriers deep down in the Ge layer. Moreover, the inter-digitated contact occupied a large surface area which hinders the light incidence. Therefore, in Chapter 3, parameters influencing the detector QE will be reviewed, which provides the clues of a longer absorption depth and higher material absorption coefficient for a higher QE in GOI photodetectors. The need for a longer absorption depth gives the motivation to develop a vertical *p-i-n* structure for the photodetectors on GOI, along with its bonding and layer transfer process. The vertical *p-i-n* would build a vertical electric field across the entire Ge layer for a higher carrier collection efficiency. Details of this work will be discussed in Chapter 4 and 5. Besides, a uniform tensile strain induced by $SiN_x$ stressor will be utilized to increase the Ge absorption coefficient, for a

MSM photodetector with an enhanced QE at the *L*-band and beyond, aiming for a low-thermal-budget BEOL integration. This work will be described in Chapter 6 and 7.

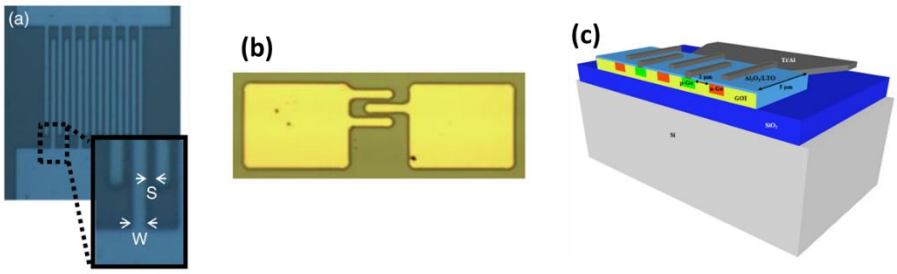


Figure 14 State-of-the-art normal-incidence GOI photodetectors by (a) Tani *et al.* [20]; (b) Jain *et al.* [5] and (c) Nam *et al.* [4].

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# Chapter 3 Quantum Efficiency (QE) Enhancement for GOI Photodetectors

## 3.1 QE of a Photodetector and Implication for Its Enhancement

Responsivity ($\Re$) is one of the key performance parameters for a photodetector. It is given as the ratio of the generated photocurrent ($I_{ph}$) from the detector to the incident optical power ($P$) and described using the following expression [1]:

$$\Re = \frac{I_{ph}}{P} = \eta q / h\nu \tag{3.1}$$

where $\eta$ is the external quantum efficiency (EQE), $q$ is the amount of charge for an electron, $h$ is the Planck's constant and $\nu$ is the photon frequency. EQE denotes the percentage of the incident photons that are successfully converted to the carriers collected by the electrodes. Apparently, a higher EQE, namely a higher responsivity, indicates the superiority of a photodetector in converting optical signal to electrical signal. This would lower the minimal detectable optical power for an enhanced sensitivity and signal-to-noise ratio of the photodetector. Consequently, a more power-efficient optical interconnect can be facilitated due to the reduced power spent on electrical amplification circuits. For normal-incidence Ge photodetectors, the EQE can be further expanded as follows [2]:

$$\eta_n = (1-r) \cdot \eta_i \cdot \left(1-exp(-\alpha_{Ge} d_{Ge})\right) \tag{3.2}$$

where $r$ denotes the surface reflectivity, $\eta_i$ the internal quantum efficiency (IQE), $\alpha_{Ge}$ the absorption coefficient of Ge and $d_{Ge}$ the thickness of the Ge layer. For vertical *p-i-n* detectors, specifically, $d_{Ge}$ refers to the thickness of the intrinsic Ge in between the *p*- and *n*-doped regions. The term $\left(1\text{-}exp(\text{-}\alpha_{Ge}d_{Ge})\right)$ indicates the amount of photons absorbed in Ge to the depth of $d_{Ge}$. It also assumes that the diffusion current for the minority carriers generated in the *p*- and *n*-region can be neglected [3]. The $\eta_i$ refers to the percentage of the photons successfully absorbed that are converted to the generated carriers collected by the electrodes. Therefore, this term could imply the material quality at the intrinsic region, since the defects such as threading dislocations could serve as non-radiative recombination centers for the generated carriers. Likewise, for waveguide-integrated Ge detectors with evanescent-coupling, the EQE can be expressed as [3]:

$$\eta_w = \eta_c \cdot \eta_i \cdot \left(1\text{-}exp(\text{-}\alpha_{Ge} \cdot L)\right) \cdot 10^{-\gamma \cdot l/10} \tag{3.3}$$

where $\eta_c$ refers to the coupling efficiency between the input waveguide and Ge, $L$ the length of the Ge along the direction of light propagation, $\gamma$ the waveguide loss in dB/cm and $l$ the length of the waveguide from the input port to the detector.

From Eq. (3.2) and (3.3), we can find out that there are a number of ways to improve the QE. For normal-incidence detectors, designing an anti-reflection coating is desired to minimize the surface reflectivity $\gamma$. Meanwhile, improving the absorption coefficient $\alpha$ of the material and

increasing the absorbing layer thickness *d* are also viable options. It can also be recommended to improve $\eta_i$ by reducing the defect density in the material to minimize the recombination of the generated carriers. While for waveguide-integrated detectors, besides similarly enhancing $\alpha$, optimizing the coupling efficiency $\eta_c$, increasing the detector absorption length $L$ and minimizing the waveguide loss $\gamma$ can be suggested.

There are a number of studies focusing on improving the epi-Ge quality for a higher QE by using SiGe buffer [4], cyclic annealing [5] and many more. Optimization of the waveguide-Ge coupling efficiency $\eta_c$ was also investigated [6, 7]. Besides, metal contact engineering away from the guided modes [8] and the Ge material itself [9, 10] are shown with significant QE enhancement due to the reduced metal/Ge coupling loss. In addition, QE enhancement by avalanche multiplication of the carriers under high electric field [11, 12] was also developed for high-sensitivity photon detection. In this chapter, specifically, prior work on absorption layer thickness (*d*) and length ($L$) optimization, as well as the engineering of the absorption coefficient $\alpha$, will be comprehensively reviewed for a higher detector QE to form the guideline of this thesis. Considering the thermal and power budget, these two approaches are practical to be applied on the GOI platform for BEOL integration.

## 3.2 Engineering Absorption Thickness and Length

As expressed in Eq. (3.2) and (3.3), it can be easily inferred that increasing the absorption thickness and length would correspondingly increase the detector responsivity and consequently the QE. Fig. 15 (a)

summarizes the responsivity of the normal-incidence Ge detectors from earlier reports in terms of their intrinsic Ge thickness [5, 13-27]. As expected, a thicker *i*-Ge leads to a higher responsivity, despite the discrepancy on the optical coupling efficiency and Ge material quality among the works. However, a thicker Ge would also adversely prolong the transit time for the photon-generated carriers to be collected by the electrodes and slow down the device speed (i.e. bandwidth), as shown in Fig. 15 (b). Therefore, there exists a trade-off between the QE and bandwidth for the normal-incidence photodetectors.

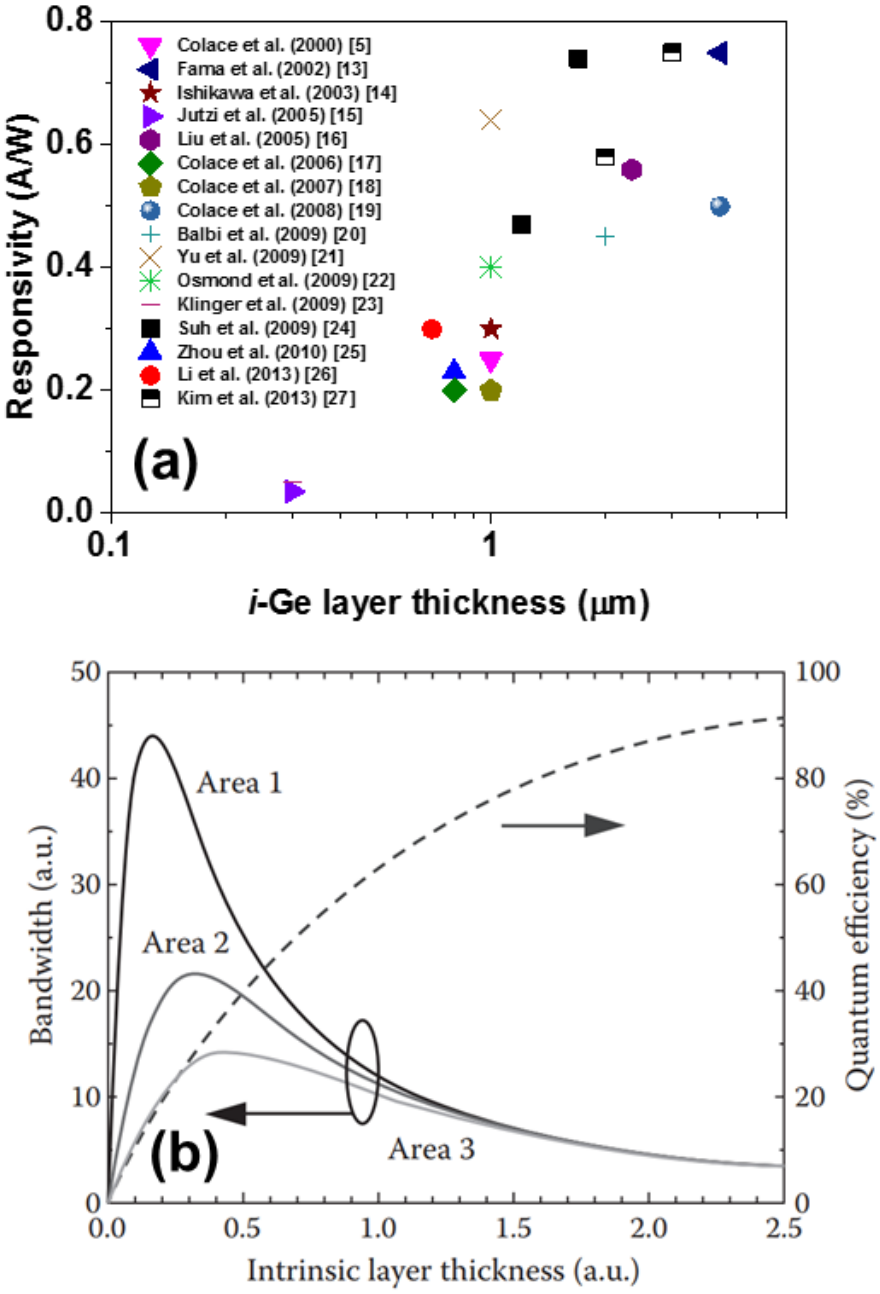


Figure 15 (a) Responsivity as a function of *i*-Ge layer thickness for the normal-incidence Ge photodetectors reported earlier. The legend indicates the first author, year and reference number for each data; (b) Bandwidth and responsivity trade-off for normal-incidence photodetectors [28]. The bandwidth firstly increases with increasing intrinsic layer thickness limited by the RC delay and decreases due to the carrier transit time. The Area 1< Area 2< Area 3.

On the contrary, waveguide-integrated Ge photodetectors brilliantly separate the paths for the carrier transition and photon absorption. The photons are butt- or evanescently-coupled (Fig. 16 (b)

and (d), respectively) and propagate longitudinally along the Ge waveguide, while the generated carriers drift either transversely or vertically across the waveguide, depending on the lateral or vertical deployment of the metal contacts (Fig. 16 (f) and (g)), respectively. Fig. 16 (a) summarizes the responsivity of waveguide-integrated Ge detectors as a function of their Ge waveguide length from earlier reports [8-10, 29-40]. A high responsivity of ~ 1A/W can generally be achieved for a waveguide length longer than 4μm and a further increase in the length does not exhibit a significant further enhancement on the responsivity. This is easy to understand if we consider a Ge absorption coefficient of $\alpha_{Ge}$~3500cm$^{-1}$ that is commonly adopted in literature [41] to estimate the amount of photon absorption via $\left(1-\exp(-\alpha_{Ge}d_{Ge})\right)$ in Eq. (3.2). A $d_{Ge}$ of 4μm could theoretically absorb ~75% of the incident power, ideally with a responsivity of ~0.93A/W at 1.55μm independent of the waveguide width and thickness. If a lateral *p-i-n* structure is adopted transversely across the waveguide with an *i*-layer thickness and a waveguide height both at 0.5μm, the corresponding device capacitance would only be ~0.4fF, which is about two orders of magnitude lower than that of a normal-incidence vertical *p-i-n* photodetector with a mesa diameter of 20μm. Therefore, a high-speed and high-efficiency photodetector could be simultaneously achieved under this scheme. This could explain the reason that a normal-incidence photodetector with a 3dB-bandwidth of ~50GHz [23] pays the cost of a limited QE, while a 3dB-bandwidth over 60GHz could easily be achieved for the waveguide-integrated detectors with an almost 100% QE [42].

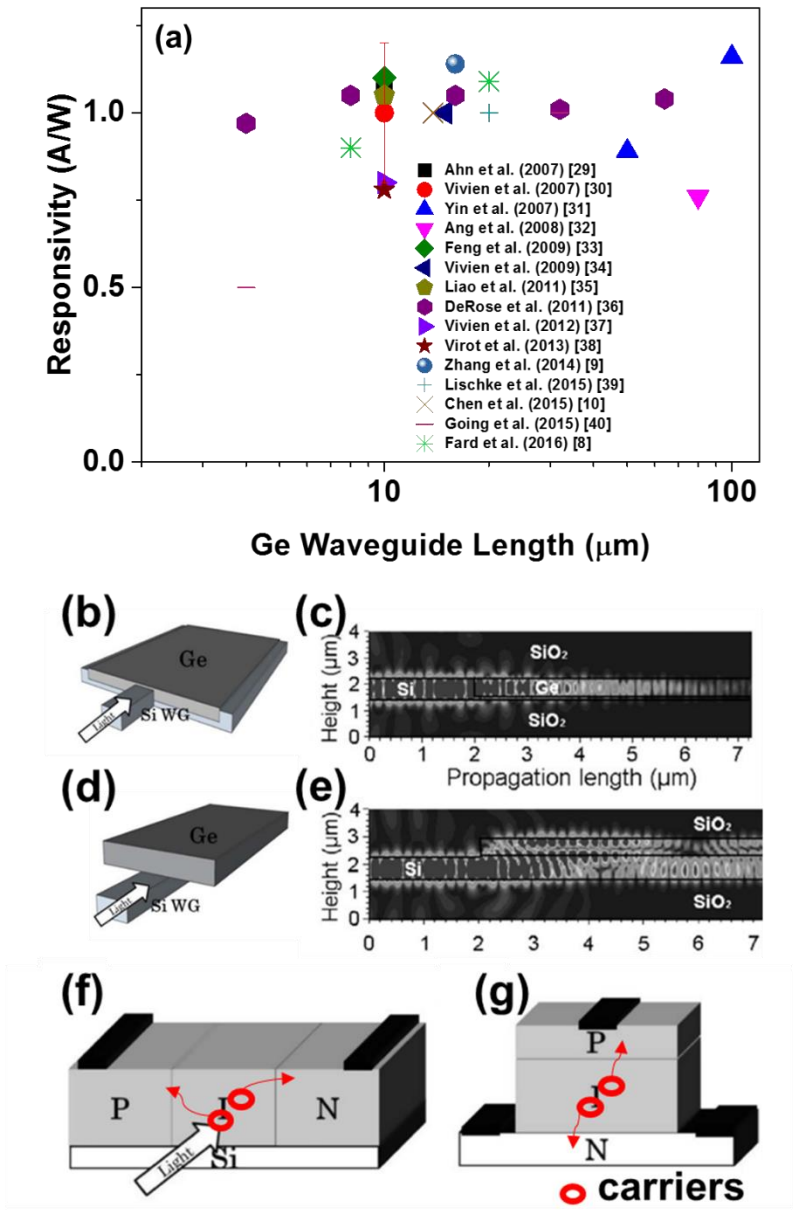


Figure 16 (a) Responsivity of waveguide-integrated photodetectors from earlier reports as a function of their Ge waveguide length; The electromagnetic field profiles of the waveguide-coupling configurations of (b) butt coupling and (d) evanescent coupling [38] are shown in (c) and (e) [43], respectively; Carrier-drift configurations (using *p-i-n* structure as an example): (d) lateral and (e) vertical [38].

In addition, novel designs were adopted for QE enhancement. As shown in Fig. 17, for normal-incidence detectors, some researchers employed resonant cavity structures sandwiching the Ge absorption layer to enable multiple photon passes in the Ge (i.e. a larger *d*) for a higher responsivity. The Ge thickness can thus be thinner for a short carrier

transit time and higher bandwidth, without a drastic compromise on the QE (for Dosunmu *et al.* [44]: 0.73A/W and 12GHz with 1.45μm Ge @ 1.55μm; for Liu *et al.* [45]: 0.25A/W and 47GHz with 0.5μm Ge @ 1.55μm). A similar concept has also been utilized in the waveguide-integrated detector design [46]. Likewise, grating [47] and micro-hole [48] structures were developed to couple the normal-incident light to lateral-propagating modes, which also increases the effective absorption thickness. However, both the grating and resonant cavity designs are limited by their narrow working wavelength range. On the contrary, the micro-hole structure can benefit a broadband detection up to ~1700nm.

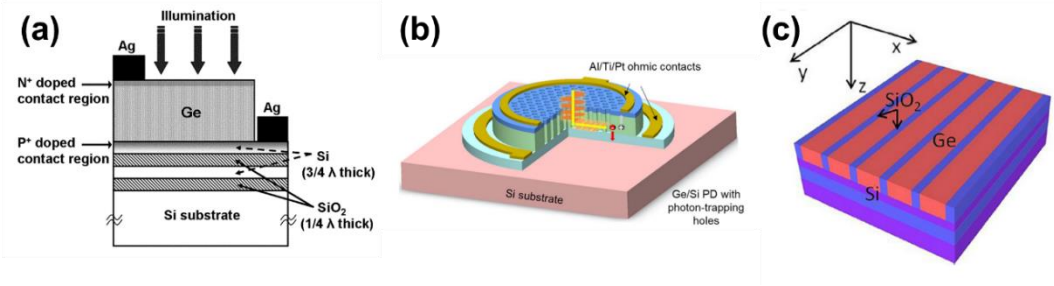


Figure 17 (a) Resonant cavity [44], (b) 2-D micro-hole [48] and (c) grating [47] structures for a higher QE of Ge photodetectors.

To summarize, literature reveals that the increase in the absorption thickness and length below ~4μm could significantly enhance the QE of Ge photodetectors, while a further increase does not exhibit further enhancement. Multiplying the photon travelling path, by forming a resonant cavity or converting the normal-incidence light into lateral-guided modes, also works but requires careful design and precise fabrication for an accurate working wavelength. Therefore, considering the planar designs for the GOI photodetectors discussed in Chapter 2.3, realizing a vertical absorption path would be the most straightforward and effective

method for a higher QE. Consequently, Chapter 4 will discuss the development of a vertical *p-i-n* structure on the GOI platform along with its bonding and layer transfer process. The vertical *p-i-n* structure could build a vertical electric field across the Ge layer to effectively collect the photon-generated carriers deeply away from the Ge surface that could not be efficiently captured by the conventional lateral contacts. The fabrication and characterization of the photodetectors will be discussed in Chapter 5.

## 3.3 Engineering Absorption Coefficient

In the previous section, we summarized the influence of absorption path on the detector QE. However, regardless of the light coupling scheme, increasing the absorption path would still inevitably increase the Ge volume and consequently the detector capacitance to slow down its speed. Therefore, to further alleviate the absorption-speed trade-off, we can alternatively improve the Ge absorption coefficient for a high-efficiency detector without compromising its compactness and device speed. Therefore, in order to achieve this motivation, earlier reports on engineering the Ge absorption coefficient were reviewed in this section.

### 3.3.1 Franz-Keldysh Effect

Franz-Keldysh (FK) effect is the shift of the optical absorption edge to lower energies under the influence of electric fields [49, 50]. It has been widely demonstrated in semiconductor materials. As shown in Fig. 18 (a), the applied electric field bends the electronic bands of the material, causing the wavefunction of electrons and holes penetrating into the

bandgap. The electron-hole pair generation is thus able to occur at an incident photon energy lower than the bandgap, which consequently enhances the material absorption coefficient at longer wavelengths. This effect has been widely used for optical modulation [51, 52]. Recently, Takeda *et al.* [53] and Liow *et al.* [54] discovered high responsivity of 1.14 and 1.30 A/W for Ge waveguide photodetectors, respectively, with reasonable 3dB bandwidths more than 20GHz at the *L*-band. They attributed the enhancement to both the FK and avalanche effects and verified the contribution from the FK effect at the *L*-band, where a ~6× enhancement was achieved under a reverse bias of 15V.

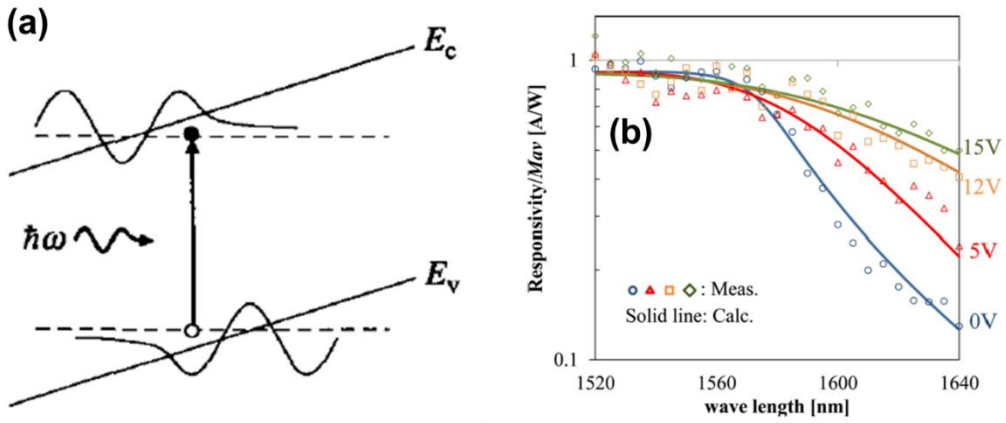


Figure 18 (a) A schematic band diagram illustrating the FK effect. The band bending induced by the electric field leads to the carrier wavefunctions penetrating into the bandgap for the photon collection below the bandgap [55]. (b) The calculated responsivity matches with the measured ones without considering the avalanche effect, demonstrating the FK effect under high reverse biases [53].

## 3.3.2 Tensile Strain

### 3.3.2.1 Tensile-strained Ge Photodetectors

It has been well known that tensile strain exerted on a semiconductor material would reduce its electronic bandgap [55]. Earlier studies have demonstrated this phenomenon on the strain engineering of

III-V based materials via epitaxy [56-58]. Following this concept, Ishikawa *et al.* [14], Cannon *et al.* [59] and Liu *et al.* [41] systematically investigated the strain resulting from the Ge-on-Si epitaxy and its effect on the Ge bandgap shrinkage. They found that the ~0.2% biaxial tensile strain in Ge resulted from the epitaxy accounts for a ~60nm red-shift of its absorption edge, enabling an enhanced QE for the photodetectors at the *L*-band. The reason for the QE enhancement is due to the increased Ge absorption coefficient that is proportional to the allowed joint density of states for the inter-band optical absorption (i.e.$\sqrt{h\nu - E_g}$ [55], where $h\nu$ is the incident photon energy and $E_g$ is the Ge bandgap energy). A shrinkage in the $E_g$ increases the joint density of states and consequently the absorption coefficient. A detailed theoretical illustration on this correlation will be discussed in Chapter 3.4. As shown in Fig. 19, according to the calculation by Liu *et al.* [41], almost an order of magnitude enhancement on the Ge absorption coefficient, across the entire L-band, was obtained with a ~0.25% biaxial tensile strain by $TiSi_2$ backside deposition.

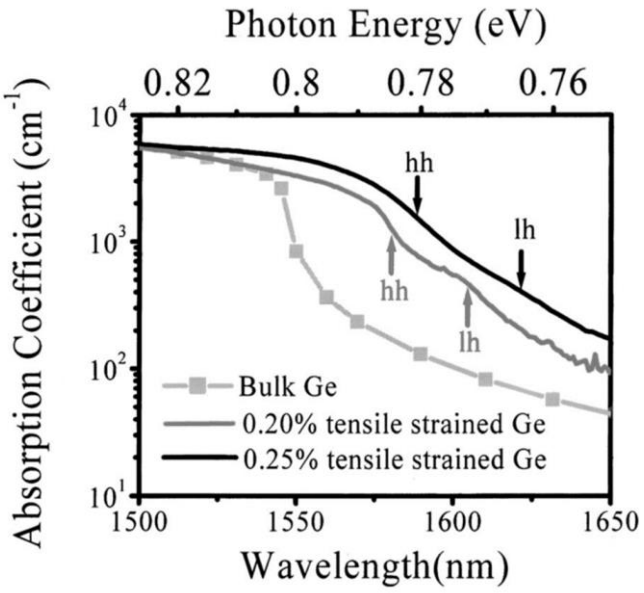


Figure 19 Absorption coefficient spectra (calculated) of 0.2% and 0.25% tensile-strained Ge, with that of bulk Ge as a reference [41].

The intrinsic ~0.2% tensile strain is insufficient for a good QE coverage across the entire *L*-band and beyond. A further increase in the tensile strain is thus necessary to facilitate a further enhancement in the detector QE. However, only few relevant publications could be found. Nam *et al.* [60] adopted a micromachining technique to remove the Si substrate and suspend the epitaxial-grown Ge film as a membrane, together with a backside tungsten stressor, for the introduction of a substantial tensile strain. More than 1% biaxial tensile strain was determined to be in the Ge membrane from micro-Raman measurements. The fabricated photodetectors exhibited a significant extension of the absorption spectra towards longer wavelengths (beyond 1800nm for ~0.76% biaxial tensile strain), as shown in Fig. 20. Ding *et al.* [61] reported tensile-strained Ge waveguide-integrated photodetectors, utilizing compressive polysilicon and tensile $SiN_x$ stressors at the Ge waveguide top and sidewalls, respectively. A constant responsivity of ~0.9A/W

across the *C*- and *L*-band was demonstrated on a 20μm-long device without roll-off. Fig. 21 (a) and (b) show the schematic of the device design and the corresponding responsivity spectra, respectively. A compressive sidewall $SiN_x$ stressor was also utilized to tune the Ge absorption edge for electro-absorption modulators [62]. Some reports [63-65] also theoretically applied the $SiN_x$ stressor on GeSn for a longer wavelength modulation and detection beyond 3μm.

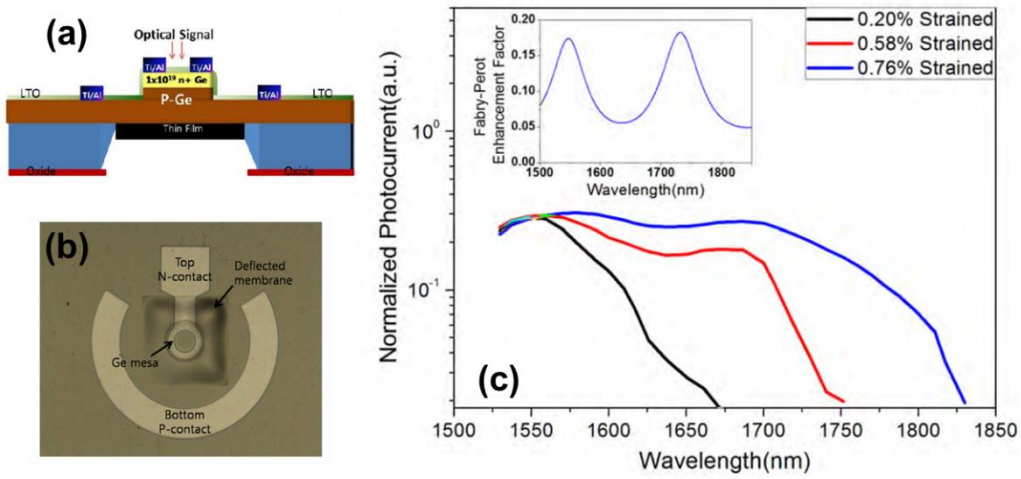


Figure 20 (a) Cross-sectional schematic [66], (b) optical image and (c) photo-response spectra [60] of the tensile-strained Ge membrane photodetector.

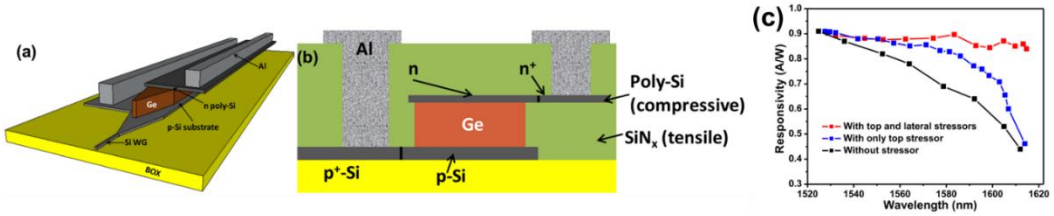


Figure 21 Schematic of (a) the Ge waveguide-integrated photodetector with localized stressors and (b) the cross-sectional view of the *p-i-n* region; (c) Responsivity spectra of the photodetectors [61].

### 3.3.2.2 Inspiration from Tensile-strained Ge Lasers

Meanwhile, there has been intensive studies on tensile-straining the Ge for a CMOS-compatible integrated light source on Si. This is because Ge is a quasi-direct bandgap material with its direct bandgap at

the *Γ*-valley only ~136meV lower than the indirect bandgap at the *L*-valley. Electronic band structure calculation reveals that tensile-straining Ge not only narrows its bandgap but also minimizes the bandgap difference at the two valleys. Theoretical calculation suggests that a biaxial tensile strain higher than ~1.9% and a uniaxial tensile strain higher than ~4.6% would hit the indirect-direct bandgap crossover point and turns Ge into a direct bandgap material [67]. Upon passing the crossover point, the free electrons would primarily fill the *Γ*-valley conduction band minimum, where the probability of population inversion and spontaneous emission would be enhanced for the light emission to occur. Therefore, various strain engineering techniques were employed to approach this crossover. For example, similar to the method adopted by Nam *et al.* mentioned earlier, suspended Ge nanowires [68, 69] and circular membranes [70, 71] were realized on Ge-on-insulator (GOI) or Ge-on-SOI platforms by patterning and selectively wet-etching the buried oxide layer underneath. By releasing the substrate constraint, the *in-situ* ~0.2% tensile strain was released and therefore magnified at the center of the structures to balance the stress. Almost 2% biaxial and more than 5% uniaxial tensile strain were achieved. Significantly red-shifted photoluminescence peaks together with their enhanced intensity indicate an improved efficiency on the direct-band spontaneous emission. On the other hand, lattice-mismatched Ge hetero-epitaxy on an $In_xGa_{1-x}As$ buffer was also studied [72-74]. The larger lattice constant in $In_xGa_{1-x}As$ induces a tensile strain in the epi-Ge layer. The compositional and elemental variation in the buffer layer also makes the strain widely-tunable upon design

requirements. Besides, silicon nitride ($SiN_x$), as an external stressor material, was extensively investigated with top [75, 76], conformal [77-79], and all-around [80, 81] configurations on Ge. A considerable tensile strain over ~1.5% could also be achieved. Theoretical calculation on the laser performance suggests a three-fold wall-plug efficiency improvement and ~50% threshold current reduction [82, 83]. A lower-threshold GeSn laser could also be similarly anticipated [84, 85], along with the Sn incorporation. Fig. 22 summarizes some of the works in tensile-straining the Ge for an integrated optoelectronic device on Si.

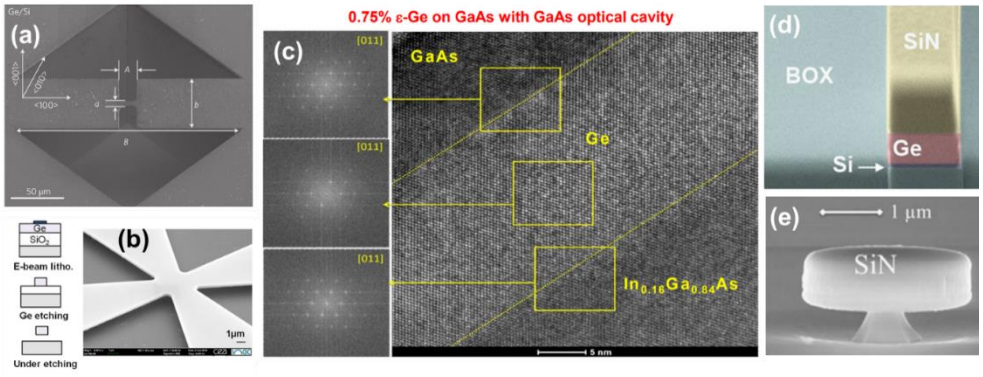


Figure 22 A summary of some Ge tensile-straining approaches for an integrated laser: Substrate undercut for (a) uniaxial-strained nanowire [68] and (b) biaxial-strained membrane [71]; (c) Ge hetero-epitaxy on InGaAs/InAlAs buffer layers [74]; $SiN_x$ stressors with (d) top [75] and (e) all-around [81] configurations.

## 3.3.3 Comparison among the Methods: The Adoption of $SiN_x$ Stressor

Comparing among these techniques, the FK effect contributes prominently to a higher detector efficiency at the *L*-band. However, this requires an excess voltage bias on the devices which hinders its wide adaptability with CMOS applications. Similarly, the suspended nature of the microstructures formed by the substrate undercut poses challenges

in thermal dissipation and CMOS integration. Although Bao *et al.* [86] released the Ge nanowire down in contact with a thermally-conductive $Al_2O_3$ layer underneath, the uniaxial strain was adversely relaxed to ~1.6%. Moreover, the challenge remains to maintain a small integration form factor, since the wet chemical undercut consumes a substantial chip area to fully release the entire structure. The $In_xGa_{1-x}As$ buffer method could not be applied to a thick Ge layer due to the critical thickness limitation. The larger lattice mismatch also generates a high density of misfit dislocations at the Ge/$In_xGa_{1-x}As$ interface that degrades its crystal quality.

The $SiN_x$ approach is particularly intriguing because $SiN_x$ has been commonly used in CMOS foundries for strained-Si technologies [87] and key passive photonic components [88]. A preliminary $SiN_x$-strained Ge photodetector was also demonstrated, as reviewed before. Therefore, in this thesis, highly-stressed $SiN_x$ was adopted as the solution to tensile-strain the Ge for a higher QE at longer wavelengths. However, the results from the literature also imply that the induced Ge tensile strain was non-uniform if one refrained from the suspended [68, 89] or pedestal [90, 91] structures, which again poses the aforementioned integration challenges. The strain non-uniformity is basically due to the direct attachment of Ge to the substrate which causes a hindered elastic deformation of the Ge near its interface to the substrate. Hence, Chapter 6 will discuss the development of a novel recessed $SiN_x$ stressor to enhance the uniformity of the tensile strain in Ge for a further improvement on the QE at longer

wavelengths. The development and characterization of the corresponding MSM detectors using this approach will be discussed in Chapter 7.

## 3.4 Theoretical Correlation between Ge Strain and Its Absorption Coefficient

It has been mentioned in Chapter 3.3.2 that a tensile strain induced in a semiconductor material would reduce its bandgap and enhance its absorption coefficient. In this section, the theory behind this phenomenon will be reviewed and served as a guide to this thesis work.

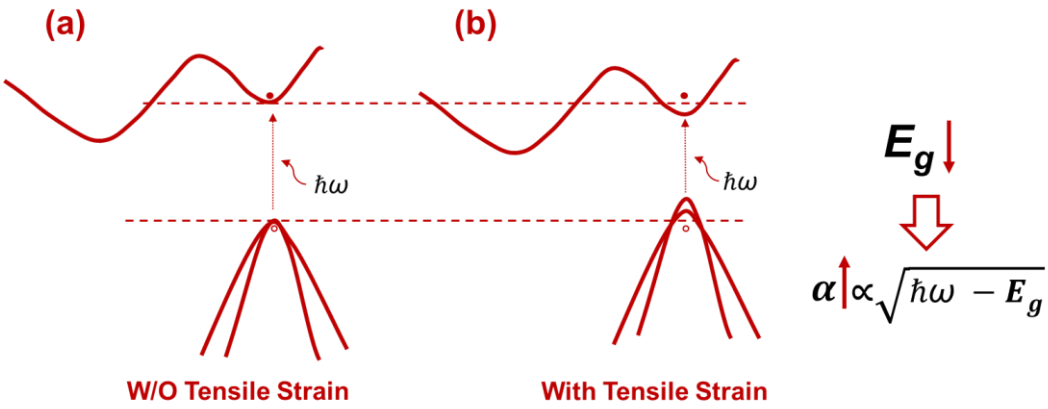


Figure 23 Electronic band structure schematics of Ge (a) without and (b) with tensile strain. The corresponding bandgap shrinkage increases the density of states accommodating the generated electron-hole pairs at an incident photon energy $\hbar\omega$, which results in an enhanced absorption coefficient.

Deformation potential theory [92] analytically describes the correlation between the bandgap of a semiconductor and its applied magnitude of strain. The strain would elastically deform the semiconductor material, causing its volumetric and lattice symmetry deformation, respectively, where the former is called hydrostatic deformation and the latter shear deformation. The hydrostatic and shear deformation energies are defined as $\delta E_{hy}$ and $\delta E_{sh}$, respectively, as shown below [55]:

$$\delta E_{hy} = -a(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) \quad (3.4)$$

$$\delta E_{sh} = -b(\varepsilon_{xx} + \varepsilon_{yy} - 2\varepsilon_{zz}) \quad (3.5)$$

where $a$ is defined as hydrostatic deformation potential and $b$ as shear deformation potential. The hydrostatic deformation potential $a = a_c - a_v$, where $a_c$ and $a_v$ are the deformation potentials for the conduction and valance band, respectively. $\varepsilon_{xx}$, $\varepsilon_{yy}$ and $\varepsilon_{zz}$ are the axial strain in the material along *x*, *y* and *z* directions induced by the stress along the same directions, respectively. Note that $(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz})$ represents the fractional change of the material volume.

Considering the coupling with the spin-orbit split-off (SO) band, the conduction-band-light-hole bandgap $E_g^{LH}$ and conduction-band-heavy-hole bandgap $E_g^{HH}$ of Ge can be expressed as follows, respectively:

$$E_g^{LH} = E_g - \delta E_{hy} - \frac{1}{4}\delta E_{sh} + \frac{1}{2}\Delta - \frac{1}{2}\sqrt{\Delta^2 + \Delta \cdot \delta E_{sh} + \frac{9}{4}\delta {E_{sh}}^2} \quad (3.6)$$

$$E_g^{HH} = E_g - \delta E_{hy} + \frac{1}{2}\delta E_{sh} \quad (3.7)$$

where $E_g$ is the original Ge bandgap without strain and Δ is the spin-orbit energy splitting between the degenerate topmost valence band and the SO valance band of Ge.

For Ge material, the $a$, $b$ and Δ employed for the calculation are -8.97, -1.88 and 0.289eV, respectively, from the experimental determination by Liu *et al.* [93] on the Ge film epitaxial-grown on Si, which is more relevant to the scenario in this work. When exerted with a tensile strain, the lattice volume would increase and the lattice symmetry would

be broken. This results in a reduced bandgap, provided the negative deformation potentials. In Chapters 5.3.2.2 and 7.1, we will utilize the theory to estimate the Ge bandgap edges with respect to the magnitude of the applied biaxial and uniaxial tensile strain, respectively.

Further on, with the understanding of the effect of strain on the material bandgap, the correlation between the material bandgap and its absorption coefficient will subsequently be discussed. If we only consider the inter-band optical absorption due to an electron-hole pair without the involvement of phonons, for a semiconductor material, we have the following expression for the absorption coefficient [55]:

$$\alpha(\hbar\omega) = C_0 \frac{2}{V} \sum_{i,f} \left| \langle f | e^{i\boldsymbol{K}_{op}\cdot\boldsymbol{r}} \hat{e} \cdot \boldsymbol{p} | i \rangle \right|^2 \delta\left(E_f - E_i - \hbar\omega\right) \left[ f(E_i) - f\left(E_f\right) \right] \quad (3.8)$$

where the constant $C_0$ can be expressed as:

$$C_0 = \frac{\pi q^2}{n_r c \varepsilon_0 m_0^2 \omega} \quad (3.9)$$

where $q$ denotes the electron charge, $n_r$ the refractive index, $c$ the speed of light, $\varepsilon_0$ the vacuum permittivity, $m_0$ the electron effective mass and $\omega$ the angular frequency. In Eq. (3.8), $\hat{e}$ is the polarization of the electric field and $\boldsymbol{p}$ the momentum operator. The term $\left| \langle f | e^{i\boldsymbol{K}_{op}\cdot\boldsymbol{r}} \hat{e} \cdot \boldsymbol{p} | i \rangle \right|^2$ denotes the interaction of the optical transition momentum matrix element between the wavefunctions at the initial state $i$ and the final state $f$ where the optical absorption occurs. Since the momentum of the absorbed photon $\boldsymbol{K}_{op} \sim {}^{2\pi}/_{\lambda} \approx 0$ is negligibly small compared to that of the electron and

holes ($\sim 2\pi/a_0$, where $a_0$ is the lattice constant), the term $\left|\langle f\left|e^{i\boldsymbol{K}_{op}\cdot\boldsymbol{r}}\hat{e}\cdot\boldsymbol{p}\right|i\rangle\right|^2$ can be simplified as:

$$\left|\langle f\left|e^{i\boldsymbol{K}_{op}\cdot\boldsymbol{r}}\hat{e}\cdot\boldsymbol{p}\right|i\rangle\right|^2 = |\hat{e}\cdot\boldsymbol{p}|^2\cdot V\cdot|\phi(0)|^2 \tag{3.10}$$

where $V$ is the lattice volume including all the quantum states inside. $\phi(\boldsymbol{R})$ is the eigenfunction for the Schrödinger equation with the lattice potential energy $V(\boldsymbol{R})=0$, indicating a free electron-hole generation without Coulomb interaction. The $\boldsymbol{R}=\boldsymbol{K}_{op}\cdot\boldsymbol{r}\approx 0$ is the differential coordinates for the electron-hole pair system. The involvement of $\hat{e}$ also explains the reason for the polarization-dependent transition efficiency between certain conduction and valance sub-bands [94]. The term $\delta\left(E_f-E_i-\hbar\omega\right)$ and $\left[f(E_i)-f\left(E_f\right)\right]$ in Eq. (3.8) are both the prerequisites for the optical absorption process, where the former illustrates that only a photon with its energy identical to the gap between the state $i$ and $f$ can be absorbed and trigger the optical transition; and the latter describes that the transition can only occur when the state $i$ is filled with an electron ($f(E_i)=1$) and the state $f$ is empty ($f\left(E_f\right)=0$). Therefore, the summation of all the possible transitions between the state $i$ and $f$ essentially implies the density of states in the material that can accommodate the incident photon energy $\hbar\omega$ and can be expressed as follows:

$$\alpha(\hbar\omega) = 2C_0|\hat{e}\cdot\boldsymbol{p}|^2\textstyle\sum_n|\phi(0)|^2\,\delta\left(E_n+E_g-\hbar\omega\right) \tag{3.11}$$

$$= 2C_0|\hat{e}\cdot\boldsymbol{p}|^2\int\frac{d^3\boldsymbol{k}}{(2\pi)^3/V}\frac{1}{V}\sigma\left(\frac{\hbar^2k^2}{2m_r^*}+E_g-\hbar\omega\right) \tag{3.12}$$

$$= \frac{C_0|\hat{e}\cdot\boldsymbol{p}|^2}{2\pi^2}\left(\frac{2m_r^*}{\hbar^2}\right)^{3/2}\sqrt{\hbar\omega-E_g} \tag{3.13}$$

where the $|\phi(0)|^2 = 1/V$ are obtained from Eq. (3.10), since the momentum matrix element is independent of the lattice volume $V$. The $E_n = \frac{\hbar^2 k^2}{2m_r^*}$ is the eigenvalue of the Schrödinger equation discussed above leading to the eigenfunction $\phi(\boldsymbol{R})$, where the $m_r^*$ is the reduced effective mass with $\frac{1}{m_r^*} = \frac{1}{m_e^*} + \frac{1}{m_h^*}$. The $m_e^*$ and $m_h^*$ are the effective mass for the electron and hole, respectively. One can find out from Eq. (3.13) that the absorption coefficient increases with increasing photon incident energy $\hbar\omega$ and decreasing bandgap energy $E_g$. Therefore, combining with the aforementioned effect of material strain on its $E_g$, it can be inferred that a tensile strain applied on a semiconductor material is capable of enhancing its absorption coefficient for a photodetector with a higher QE.

## 3.5 Realizing Highly-stressed $SiN_x$

As will be discussed in Chapter 6, based on the placement of the $SiN_x$ stressor, a highly-compressive top stressor and a tensile sidewall stressor can be used to effectively induce a tensile strain in Ge. Besides, a compressive stressor enables a broadband Ge electro-absorption modulator arrays. Therefore, in this section, we will review the prior studies on the development of a highly-stressed $SiN_x$ film as a foundation to our work.

Stress engineering in CMOS transistors has been widely adopted since the 90nm technology node for improved device characteristics [95]. Dual stress $SiN_x$ liners, as one of the stress engineering techniques, have shown effective drive current enhancement, with the highly-tensile and -

compressive liners applied on N- and P-MOSFETs, respectively [96]. To develop this technology, obtaining a highly-stressed $SiN_x$ film is well studied by various methods such as low pressure chemical vapour deposition (LPCVD) [97] and plasma-enhanced chemical vapour deposition (PECVD) [98, 99]. The $SiN_x$ deposited by PECVD has the flexibility to control the film stoichiometry, by varying the deposition parameters, compared to LPCVD. However, LPCVD involves a higher thermal budget (> 650$^o$C), which assists a higher film stress by desorbing the incorporated hydrogen in the film. Admittedly, PECVD is more appropriate in this work due to its low thermal budget below 400$^o$C for BEOL integration.

It has been a consensus that, in dual frequency PECVD, the high radio frequency (RF) mode of ~13.56 MHz helps to obtain a tensile-stressed film, while the involvement of the low RF mode of ~380 kHz benefits a compressive stress in the $SiN_x$ film [98]. The effect of some common deposition parameters on the resulting $SiN_x$ film stress is tabulated in Table 2, according to the literature. As the inter-electrode spacing [99] is an invariable and some gases such as $H_2$ [100], $N_2O$ [101] and inert gases [99] are unavailable in our PECVD system (Cello Aegis-20), their corresponding effects are not included. It has also been reported that a multilayer $SiN_x$ deposition sandwiched with surface plasma treatment and annealing at elevated temperatures (or with UV curing) could further enhance the as-deposited compressive and tensile stress, respectively, in the film [98, 99]. The former approach densifies the film and leads to a higher compressive stress, while the latter approach

desorbs the incorporated hydrogen in the film and promotes the formation of rigid Si-N bonds for a higher tensile stress. Detailed experimental development for a highly-stressed $SiN_x$ film will be discussed in Chapter 6.2.

Table 2 Effect of PECVD deposition parameters on the resulting $SiN_x$ film stress [98].

| ***Deposition parameter***<br>(assuming the parameters **increase**) | ***Effect on stress***<br>(for a **tensile** film) | ***Effect on stress***<br>(for a **compressive** film) |
|---|---|---|
| ***RF power*** | **decrease** | **increase**<br>(minor effect) |
| ***Chamber Pressure*** | **increase** | **decrease** |
| ***Deposition temperature*** | **increase** | **increase**<br>(minor effect, <400°C)<br>**decrease**<br>(>400°C) |
| ***Total $SiH_4$+$NH_3$*** | **decrease** | **decrease** |
| ***$SiH_4$/$NH_3$ ratio*** | **decrease** | **No response** |
| ***$N_2$/($N_2$+$NH_3$) ratio*** | **Not available** | **increase** |

# 3.6 Summary

In this chapter, a detailed literature review on the QE enhancement of photodetectors was performed. Two approaches, namely a longer absorption path and higher absorption coefficient, were comprehensively reviewed for a higher-efficiency GOI photodetector. Both a longer absorption path below ~4μm and a tensile strain induced by CMOS-compatible $SiN_x$ stressor were summarized that could effectively enhance the device QE. The longer absorption path was realized via a vertical *p-i-*

*n* structure, which can be easily realized on a GOI formed by bonding and layer transfer method. The tensile strain induced by the $SiN_x$ stressor could reduce the Ge bandgap for a higher absorption coefficient to improve the QE. Therefore, Chapter 3.4 discussed the theoretical background behind the correlation between the strain and the bandgap as well as the absorption coefficient and Chapter 3.5 summarized the prior work in achieving a highly-stressed $SiN_x$ film by PECVD. These information will be utilized in the subsequent chapters to develop a GOI photodetector with a higher QE.

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# Chapter 4 Realizing a Vertical *p-i-n* Structure on GOI for High-efficiency Photodetectors

As discussed in Chapter 3.2, a longer absorption path is helpful for a higher detector QE. Since the thickness of the material acts as the absorption path for the normal-incidence photodetectors, a vertical electric field across the entire Ge layer would ideally fully collect the photon-generated carriers for a maximal QE. A vertical *p-i-n* structure is thus required to build the vertical electric field. However, the vertical *p-i-n* structure is challenging to be realized on GOI using the methods such as Ge condensation, RMG and lateral over-growth, as summarized in Chapter 2.2. Therefore, in this chapter, we will introduce a method to realize a vertical *p-i-n* structure by ion-implanting $BF_2^+$ at the bottom of the epi-grown Ge-on-Si, followed by $As^+$ ions at the top of the GOI after the bonding and layer transfer process for the GOI fabrication. No additional process development is thus needed. This method would also minimize the excess diffusion of the n-type dopants if they are *in-situ* introduced during the high-temperature Ge epitaxy.

In Chapter 4.1, the corresponding detailed process flow will be introduced. Chapter 4.2 will investigate the dose and energy required for the ion implantation. Finally, Chapter 4.3 will discuss the characterization results of the fabricated GOI *p-i-n* structure. Chapter 4.4 will conclude the chapter.

# 4.1 Process Flow

Fig. 24 shows the schematic of the process flow in realizing a vertical *p-i-n* structure on GOI, along with the bonding and layer transfer process that are similar to that previously reported [1, 2]. An intrinsic Ge (*i*-Ge) layer was epitaxial-grown on a 200 mm Si (100) carrier wafer by a three-step growth approach in an Aixtron metal-organic chemical vapour deposition (MOCVD) tool. The Si wafers (*p*-type, resistivity = 1-100 Ω-cm) were cleaned using standard RCA solution followed by a dip in diluted HF solution (HF: $H_2O$ = 1:10 by volume). The cleaned wafer was then loaded into the MOCVD reactor. To initiate the growth, the wafer was baked in hydrogen at 1050$^oC$ for 10 min to desorb the thin native oxide. Afterwards, a thin Si layer was grown to condition the Si surface and bury the surface contaminants for the subsequent high quality Ge growth. The three-step growth was then introduced: (i) low temperature growth at 400$^oC$ for a smooth and continuous Ge seed layer; (ii) temperature ramping from 400 to 600$^oC$ at a rate of 6.5$^oC$/min; (iii) high temperature growth at 600$^oC$. Thermal cycling was immediately carried out thereafter, which consists of a temperature swing between 680 and 825$^oC$ followed by a 10min annealing at 825$^oC$ in $H_2$ ambient, for a repetition of 8 times. The $BF_2^+$ ion implantation was then performed after the growth to form a boron (B)-doped *p*-Ge layer at the top. Afterwards, a $SiO_2$ interfacial layer was deposited via plasma-enhanced chemical vapor deposition (PECVD) on both the Ge-on-Si carrier and another Si handle wafer. An additional ~50 nm unstrained $SiN_x$ layer was PECVD-deposited on the Ge-on-Si carrier to help with suppressing the formation of the interfacial void during the

latter bonding stage. Prior to bonding, both dielectric surfaces were treated under $O_2$ plasma for 15s, followed by deionized water rinsing and spin drying. The rinsing step was used to clean the wafer surface and populate the surface with a high density of hydroxyl (-OH) group for the interfacial Si-O-Si covalent bond formation during the subsequent annealing step. After the surface treatment, the Ge-on-Si carrier was flipped over and bonded to the Si handle wafer at room temperature followed by an annealing at 300°C for 3hrs in $N_2$ ambient to enhance the bonding strength. Grinding, tetramethylammonium hydroxide (TMAH) etching, and then chemical-mechanical polishing (CMP) were implemented to remove the Si carrier wafer and defective Ge. A Ge layer of ~1.4μm thick remained after the CMP. $As^+$ implantation was then performed to form the arsenic (As)-doped *n*-Ge layer. The dopant activation was performed at 650°C for 15s by rapid thermal annealing (RTA) to minimize the dopant diffusion.

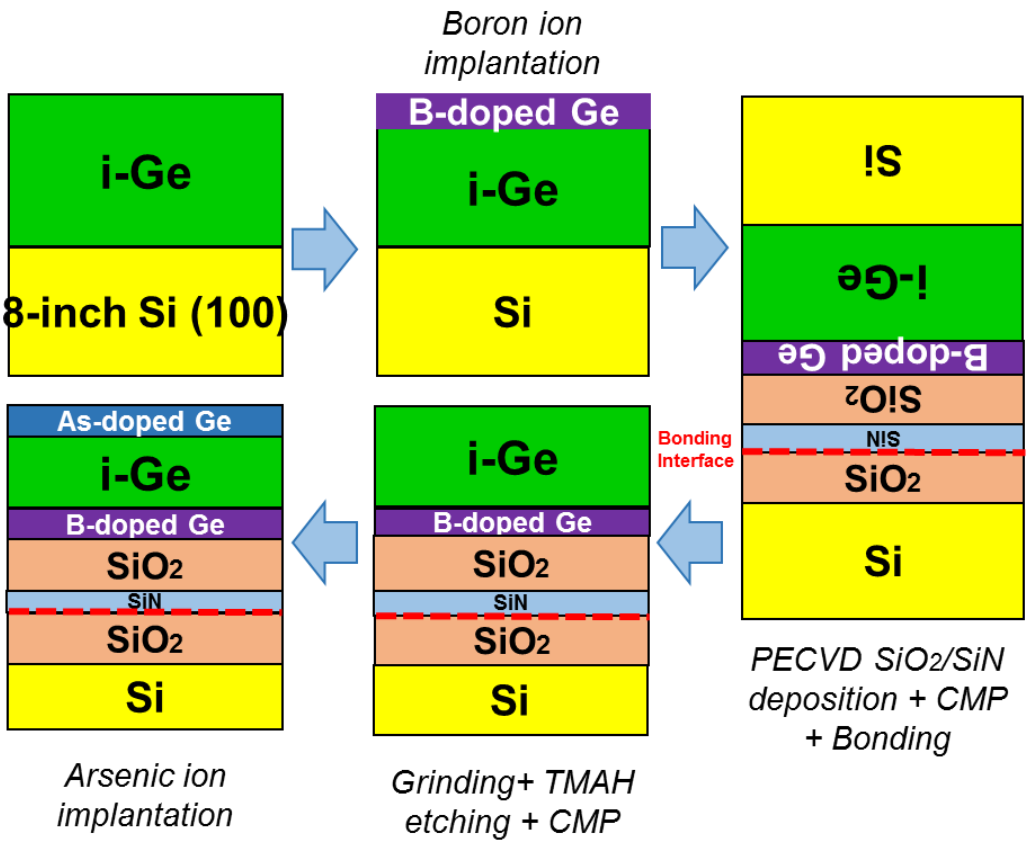


Figure 24 Schematic of the bonding and layer transfer technique for GOI vertical *p-i-n* structure fabrication.

# 4.2 Study on Implantation Parameters for As and B Doping in Ge

Prior dopant diffusion studies [3-7] reveal that *n*-type dopants such as phosphorus (P), As and antimony (Sb) are fast diffusers in Ge, while B, as a *p*-type dopant, is a slow diffuser. The diffusivity of As (~$10^{-13}$cm$^2$/s) can be more than six orders of magnitude higher than that of B (~$10^{-19}$ cm$^2$/s) at ~700°C [8]. This is also the reason why the implantation of As was lastly introduced in Fig. 24, to avoid unnecessary dopant diffusion during the post-bonding annealing. The vacancy-dominated diffusion mechanism for the *n*-type dopants results in their faster diffusivity than

that of the B, which is associated with the self-interstitials [8, 9]. For a vertical *p-i-n* structure for photodetectors, abrupt and shallow *p*- and *n*-profiles are preferred with a thick *i*-layer in the middle for a substantial photon-generated carrier collection. B is apparently advantageous in forming a shallow and abrupt *p*-type region in Ge, based on its low diffusivity; while for the *n*-type dopants, As is selected since in prior study a more abrupt dopant profile was observed [4], compared to that of the P implantation, despite its higher diffusivity. Hence, low energy implantation, with a good control of the dosage and diffusion, is necessary for a heavily-doped *n*-type shallow junction. On the other hand, since the B-doped region is ultimately located at the bottom of the Ge layer, a deep *p*-region is desired for the ease of the *n*-mesa etching depth control in the subsequent photodetector fabrication (Chapter 5.1). This requires a higher dosage with a stronger energy. Therefore, in this section, the dosage and energy optimal for the As and B ion implantation will be investigated, for a desired GOI *p-i-n* structure for photodetectors.

The Ge material used in this study was epitaxial-grown on Si (100) as described in Chapter 4.1. The sample surface was rinsed sequentially in acetone, isopropanol (IPA) and commercial buffered oxide etchant (6:1) to remove the surface organic contaminants and native oxide. Three $As^+$ dosage of $4 \times 10^{14}$, $7 \times 10^{14}$ and $1 \times 10^{15}$ $cm^{-2}$ were used for the As implantation, with the implant energy at 30 keV used in literatures for a junction depth of ~ 200 nm [3]. For the B implantation, the $BF_2^+$ dosage was fixed at $4 \times 10^{15}$ $cm^{-2}$, with the corresponding energy varied from 40 to 80 keV. Both the ion beams were tilted by 7° to the substrate surface

normal to minimize channeling. All the implantation experiments were carried out at room temperature. After the implantation, a ~ 100 nm $SiO_2$ layer was deposited on the samples by PECVD, to prevent the dopant out-diffusion during the activation by RTA at 650°C for 15 s. The chemical and electrically-active concentration profiles were then characterized by secondary ion mass spectrometry (SIMS) and spreading resistance profiling (SRP) techniques, respectively.

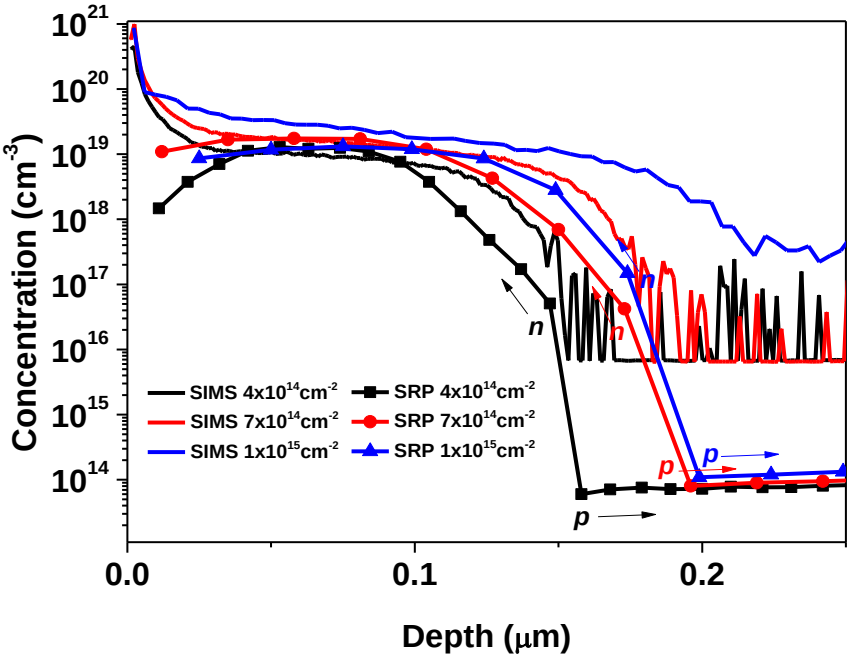


Figure 25 SIMS and SRP profiles after the dopant activation at 650°C for 15s, for the $As^+$ implantation at 30keV with respect to the dosage used.

Fig. 25 shows the SIMS and SRP profiles from the As implantation experiments. It is obvious from the SIMS results that a higher implant dosage leads to a higher chemical dopant concentration and deeper dopant profile. The noise beyond ~150nm at the dosage of $4 \times 10^{14}$ and $7 \times 10^{14}$ $cm^{-2}$ is due to the minimal detection level of the system. The "*n*"

and "*p*" labelled in the plot indicate the doping type, which reveals the profile depths of the implantation. The "*p*" regions correspond to the background concentration in the as-grown Ge. Approximately an order of magnitude lower (~$10^{18}$ $cm^{-3}$) electrically-active concentration was observed for the $4 \times 10^{14}$ $cm^{-2}$ sample close to the surface, compared to that of the other two, which is probably due to the dopant deactivation by forming inactive clusters [9]. The similar peak active dopant concentration at ~$2 \times 10^{19}$ $cm^{-3}$, irrespective of the dosage used, can be explained by the dopant solid solubility limit in Ge [5, 6]. Thus, the dosage of $7 \times 10^{14}$ $cm^{-2}$ is favored, for its maximal dopant activation rate with minimal effect from the inactive species on the Ge crystal, and the appropriate profile depth at ~ 200 nm.

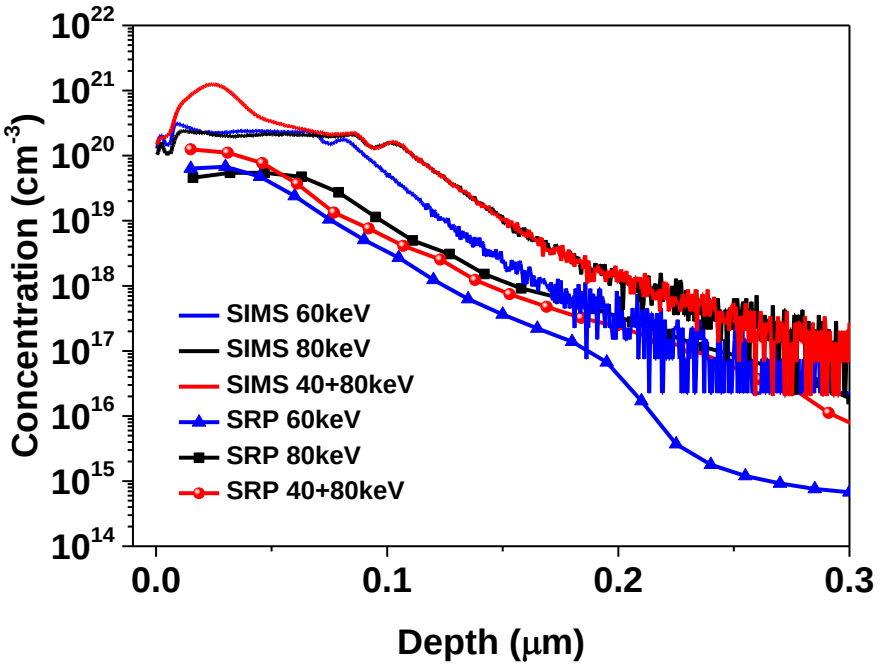


Figure 26 SIMS and SRP profiles after the dopant activation at 650°C for 15 s, for the $BF_2^+$ implantation at a fixed dose of $4 \times 10^{15}$ $cm^{-2}$ with respect to the implant energy.

The SIMS and SRP profiles for the $BF_2^+$ implantation were plotted in Fig. 26. The “40+80 keV” was performed by implanting at an energy of 40 keV followed by 80keV, both using a dose of $4 \times 10^{15}$ $cm^{-2}$. Compared to the 80 keV-only implant, the additional 40keV implant helps increasing the chemical and active concentration by about an order of magnitude and two times, respectively, at ~ 20 nm to the Ge surface. However, its active concentration beyond ~ 50 nm was adversely reduced. The reason is still not clear and might be due to the pre-amorphization of the Ge crystal in the first 40 keV implant that mitigated the crystal damage from the second 80 keV implant, which causes less dangling bonds available for an effective dopant activation. The 80keV-only implant achieves the deepest dopant profile, with an active concentration higher than $1 \times 10^{18}$ $cm^{-3}$ till the depth of ~150nm, which is sufficient for an Ohmic contact [10]. Therefore, this energy level will be used for the subsequent realization of the GOI *p-i-n* structure.

## 4.3 Characterization of the GOI Vertical *p-i-n* Structure

According to Chapter 4.2, $As^+$ implantation with the dose of $7 \times 10^{14}$ $cm^{-2}$ and energy of 30 keV, and $BF_2^+$ implantation with the dose of $4 \times 10^{15}$ $cm^{-2}$ and energy of 80 keV are preferred for the formation of the GOI vertical *p-i-n* structure. In this section, the *p-i-n* structure formed using the above implantation parameters will be characterized. Cross-sectional SEM and TEM images were captured for the respective layer information. SIMS and SRP were carried out to acquire the doping and carrier profiles

in the Ge layer, respectively. The film quality and residual strain of the transferred Ge layer were determined by both a WITec UHTS 300 confocal micro-Raman spectroscope and PANalytical X'Pert PRO high-resolution X-ray diffractometer (HRXRD).

### 4.3.1 Cross-section

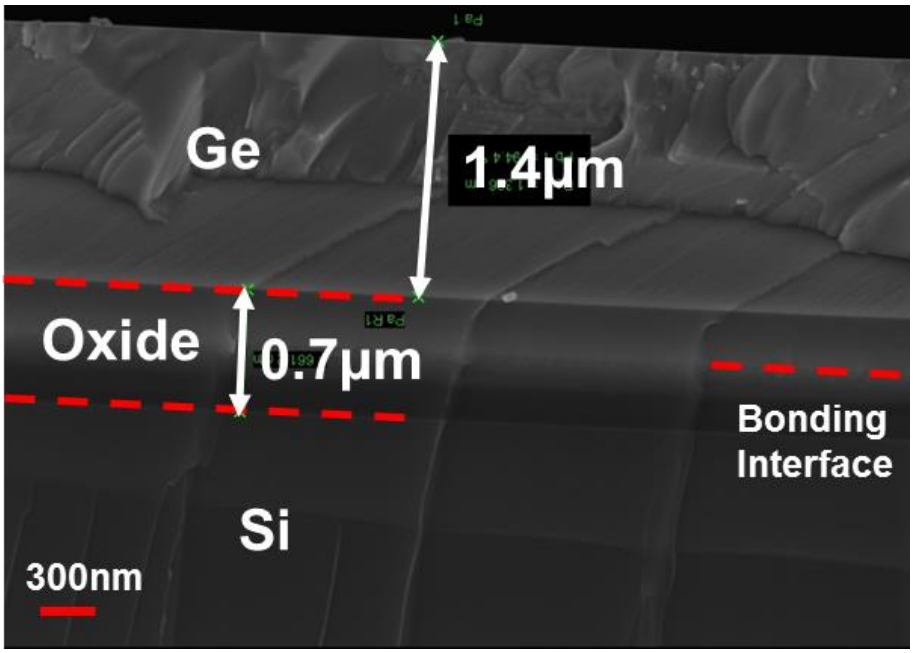


Figure 27 A cross-sectional SEM image of the GOI *p-i-n* structure.

Fig. 27 shows an SEM image of the GOI *p-i-n* structure from the cross-sectional view. A clear contrast among the respective layers is shown. A void-free and seamless bonding interface was also seen, indicating a good bonding quality. Further, from the TEM image shown in Fig. 28, the good bonding quality was verified. Besides, a high quality Ge layer was observed after the transfer without any dislocation.

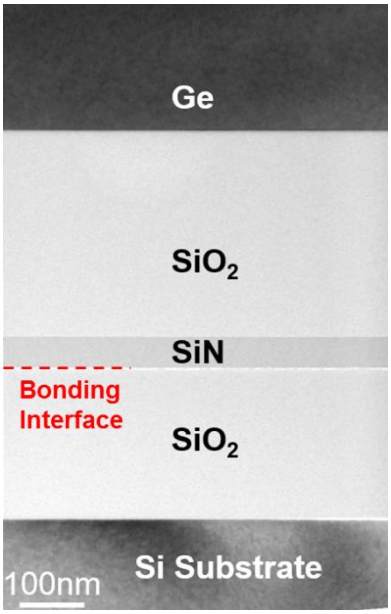


Figure 28 A cross-sectional TEM image of the GOI vertical *p-i-n* structure.

## 4.3.2 Dopant and Carrier Profiles

SIMS and SRP profiles of the *p-i-n* structure were obtained using the same approach as described in Chapter 4.2. Fig. 29 shows the doping profiles of B and As with respect to the depth in the Ge layer. Both the B and As profiles reveal abrupt concentration interfaces at ~170 and ~1100 nm depth, respectively, with low concentration below the detection limit at the middle intrinsic region. This confirms a minimal diffusion of B and As dopants in maintaining the *i*-Ge thickness for sufficient optical absorption. The SRP result shown in the inset agrees well with the SIMS profile. Due to the involvement of the layer transfer technique, the ion implantation method became viable for introducing the *p*- and *n*-type layers, each at one side of the Ge film. This eliminates the concern of excess diffusion of the *in-situ* dopants introduced during the Ge growth and cyclic annealing. Fig. 30 shows a SRP profile of a epi-Ge film grown on Si (100) with *in-situ* doped As at the top ~200nm and implanted with B after the layer transfer

(the As profile was thus switched to the bottom of the GOI). Severe As diffusion was found across the entire film due to the post-growth cyclic annealing, causing a high background concentration over $1 \times 10^{18}$cm$^{-3}$. The detector with such *p-i-n* structure would suffer from a low responsivity and slow speed due to its narrow depletion width.

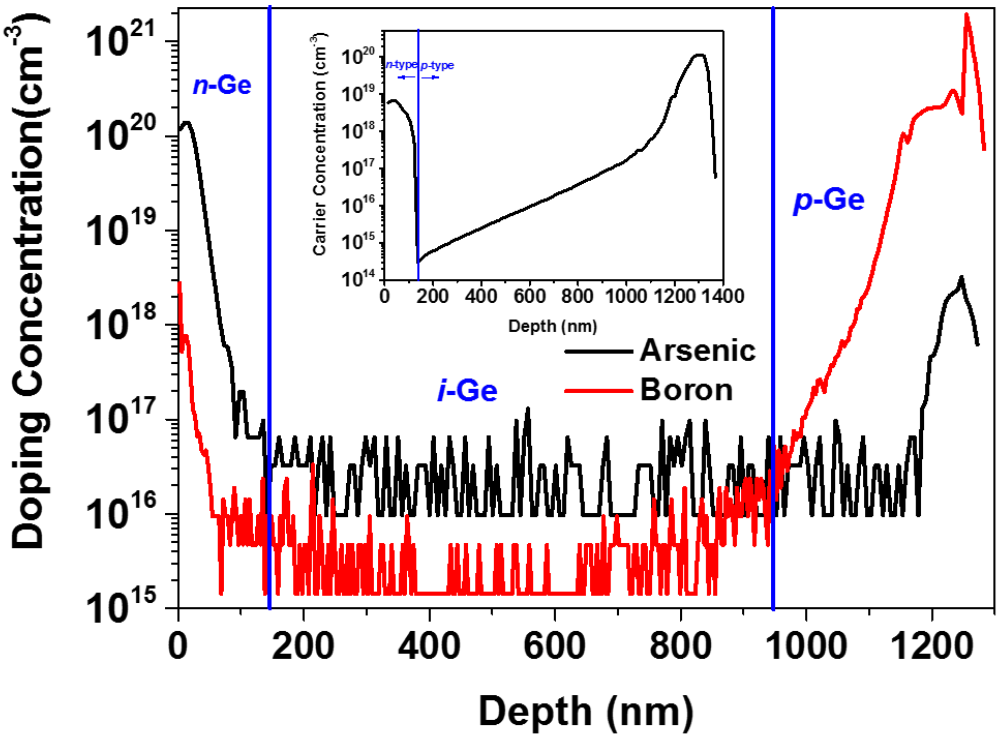


Figure 29 SIMS As and B profiles from the GOI vertical *p-i-n* structure. The inset correspondingly shows the SRP profile.

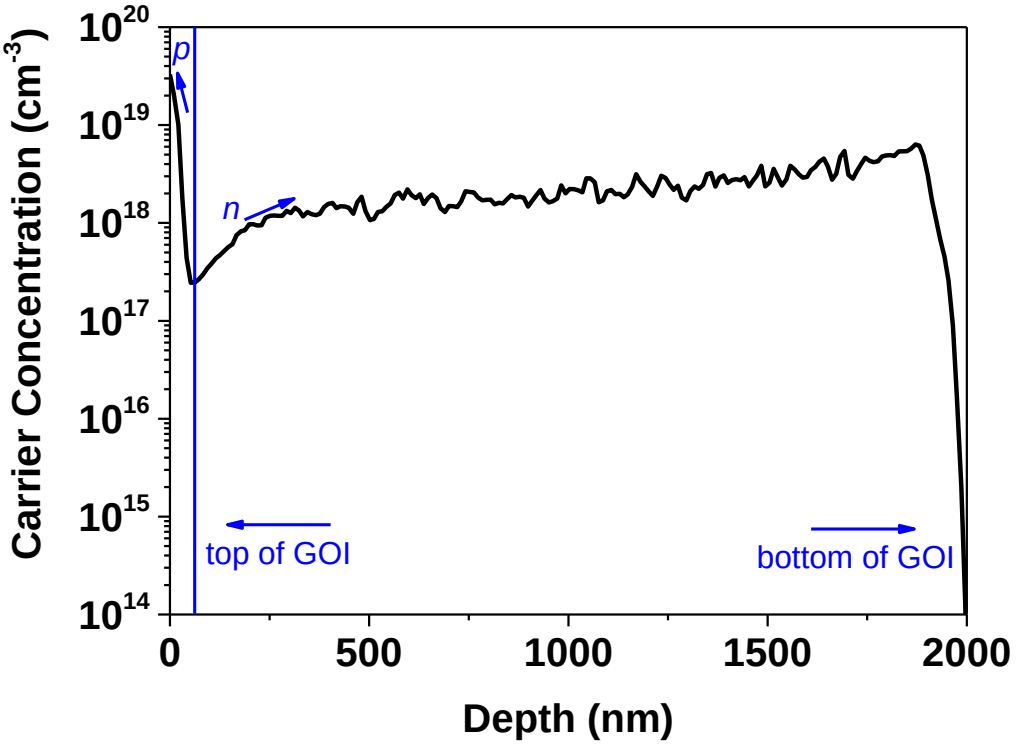


Figure 30 SRP profile for a GOI *p-i-n* structure with *in-situ* doped As at the bottom (initially at the top of the as-grown Ge film). The high thermal budget at the Ge growth (600°C) and subsequent cyclic annealing (825°C) caused a severe diffusion of the As dopants.

### 4.3.3 Film Quality and Residual Strain

Fig. 31 (a) shows a comparison of the LO-mode micro-Raman spectra of the Ge film after the layer transfer. The GOI, immediately after the grinding and TMAH etching before the Ge CMP, reveals a slight blue-shift of the Ge-Ge mode peak at ~300cm$^{-1}$, compared to the GOI after the CMP. Meanwhile, the Si-Ge mode peak at ~380cm$^{-1}$ becomes weaker after the CMP. Both of the observations verify that the CMP process removes the Si-Ge inter-diffused layer at the top of the GOI structure, which was originally at the interface between the epi-Ge and carrier Si.

To figure out the residual strain in the transferred Ge film, the Ge-Ge mode peak of the GOI after the CMP, where the peak frequency shift due to the Si incorporation was considered eliminated and only left with the strain-induced component, was compared with respect to that of the bulk Ge. The two spectra are shown in Fig. 31 (b). The residual strain is calculated as ~0.185% tensile, using the stress-induced LO phonon frequency splitting relation [11]:

$$\omega_i^2 - \omega_0^2 = [pS_{12} + q(S_{11} + S_{12})](\sigma_{11} + \sigma_{12}) \quad (4.1)$$

where $\omega_i$ = 300.06 cm$^{-1}$ and $\omega_0$ = 300.84 cm$^{-1}$ refer to the two peak frequencies of the GOI and bulk Ge, respectively. $p = -1.45\omega_0^2$ and $q = -1.95\omega_0^2$ are the phonon deformation potentials. $S_{11}$ and $S_{12}$ are the compliance tensors linking between the applied stress and the corresponding induced strain in Ge. As the strain in the film is biaxial, therefore the axial stress $\sigma_{11} = \sigma_{12}$ and can be determined as:

$$\sigma_{11} = \sigma_{12} = \frac{\omega_i^2 - \omega_0^2}{2[pS_{12} + q(S_{11} + S_{12})]} \quad (4.2)$$

As a result, the in-plane biaxial strain in the Ge film can be expressed as:

$$\varepsilon = \frac{(1-\nu)(\omega_i^2 - \omega_0^2)}{2 \cdot E \cdot [pS_{12} + q(S_{11} + S_{12})]} \quad (4.3)$$

where $\varepsilon$ is the in-plane biaxial strain in the Ge film. $\nu$ = 0.273 and $E$ = 103 GPa are the poisson's ratio and Young's modulus of Ge, respectively.

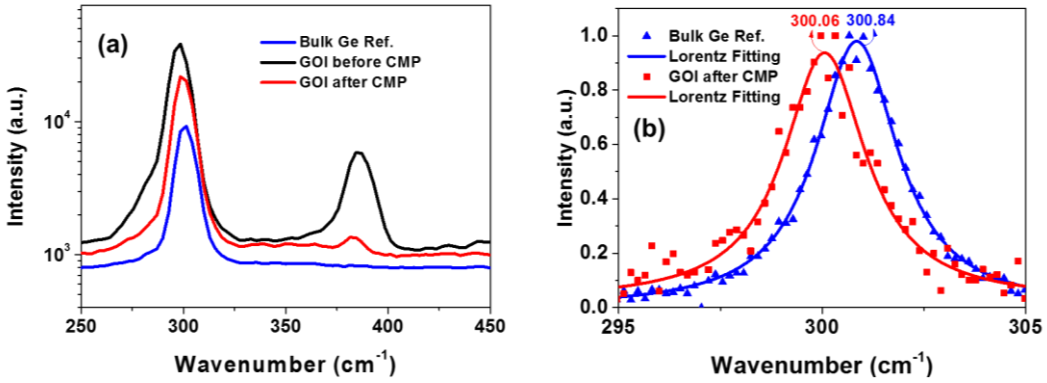


Figure 31 (a) Comparison of the LO-mode micro-Raman spectra of the transferred Ge film with respect to the bulk Ge; (b) Normalized spectra of the bulk Ge and the GOI after CMP showing the Ge-Ge phonon mode (full squares). The solid curves are the Lorentz fitting of the data points.

The HRXRD (004) 2θ − ω scan results of the as-grown Ge-on-Si and the GOI vertical *p-i-n* structure were plotted in Fig. 32, with that of the bulk Ge as a reference. It can be observed that the Ge peak intensity increases (by an order of magnitude) and the peak full-width-half-maximum (FWHM) decreases (from 227 to 48 arcsec) from the as-grown film to GOI. This indicates a significant improvement on the Ge film quality after the bonding and layer transfer, which is comparable to that of the single-crystalline bulk Ge by owing a similar FWHM value. The crystal quality enhancement is due to the removal of the highly defective Ge layer close to the Ge/Si interface during the CMP process. The same reason could be used to explain the minimized shoulder at the right-side of the GOI HRXRD peak towards a higher 2θ−ω angle, which has been correlated with the Si/Ge inter-diffusion during the Ge-on-Si growth [1]. This observation conforms well to the findings of the Ge-Ge peak shift and Si-Ge peak suppression in Fig. 31 (a).

The residual strain in the Ge film, can also be calculated based on the Ge lattice constants obtained from the HRXRD peak 2θ−ω angles of the GOI and bulk Ge, as illustrated in Ref. [1]. First, the Ge lattice constant $a^{\perp}$ out of the (001) plane can be determined from its diffraction peak angle:

$$a^{\perp} = \frac{2\lambda}{\sin(\frac{\omega_{GOI}}{2})} \tag{4.4}$$

where $\lambda$ is the incident wavelength of the X radiation (Cu $K_{\alpha 1}$ line, $\lambda =$ 1.5406 Å) and $\omega_{GOI} = 66.07^{o}$ denotes the 2θ−ω angle at the GOI (004) diffraction peak. Further, the in-plane lattice constant $a^{\parallel}$ can be calculated as:

$$a^{\parallel} = \left(\frac{1+\upsilon}{2\upsilon}\right)\left[a - a^{\perp}\left(\frac{1-\upsilon}{1+\upsilon}\right)\right] \tag{4.5}$$

where $\nu$ is the poisson's ratio as discussed before and $a =$ 5.658 Å is the strain-free Ge lattice constant obtained from Eqn. (4.4), using the 2θ − ω angle ($\omega_{Ge} = 65.99^{o}$) at the bulk Ge peak. Finally, the in-plane biaxial strain $\varepsilon$ can be determined as shown below:

$$\varepsilon = \frac{a^{\parallel} - a}{a} \tag{4.6}$$

It was found that there is ~0.15% tensile strain remaining in the Ge film, which is close to the reported values [12, 13]. This value also agrees reasonably with that determined from the Raman measurements (~0.185%). The slight discrepancy might be due to the wavelength of the laser (785nm) used in the Raman measurements could only penetrate ~89nm [14] into Ge, which only collects the strain information near the top

region of the GOI where there are still some residual inter-diffused Si incorporated (the tiny Si-Ge peak at ~380cm$^{-1}$ for the GOI after CMP, in Fig. 31 (a)). The residual Si accounts for the blue shift of the Ge-Ge phonon peak [15] and leads to a higher estimation of the tensile strain. On the contrary, the X-ray penetrates entirely through the Ge film and provides an overall strain information of the layer. Therefore, the HRXRD-determined residual tensile strain will be utilized in Chapter 5 to serve as an important guide in understanding the optical responsivity spectrum of the GOI photodetector.

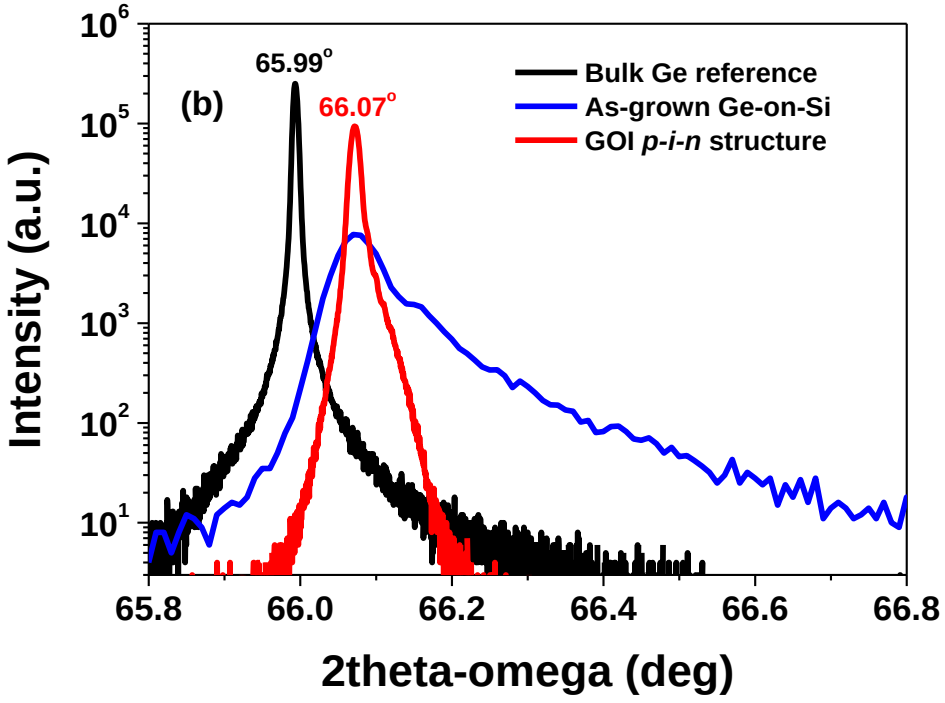


Figure 32 HRXRD (004) 2θ − ω scan of as-grown Ge-on-Si and GOI *p-i-n* structure with that of the bulk Ge as a reference. Tensile strain of ~0.15% for the Ge layer in the GOI was obtained. The values in the plot correspond to the respective peak 2θ − ω angles.

## 4.4 Conclusion

In this chapter, a Ge vertical *p-i-n* structure was successfully realized on a GOI platform, via ion-implanting $BF_2^+$ at one side of the Ge layer followed by $As^+$ at the other, along with the bonding and layer transfer process during the GOI fabrication. The dose and energy for both the implantations have been optimized. The $As^+$ implantation uses the dose of $7 \times 10^{14}$cm$^{-2}$ and energy of 30keV for a shallow and abrupt doping profile, whereas the $BF_2^+$ implantation uses the dose of $4 \times 10^{15}$cm$^{-2}$ and energy of 80keV for a deep profile for the ease of the *n*-mesa depth control (till a ~150 nm *p*-Ge remaining) in the subsequent photodetector fabrication. The fabricated GOI *p-i-n* structure has been verified with a seamless and void-free bonding interface via the cross-sectional SEM and TEM characterizations. Abrupt *p*- and *n*-doping profiles with minimal diffusion, were also confirmed via both the SIMS and SRP techniques. HRXRD scan exhibits an excellent crystal quality comparable with that of the bulk Ge for the transferred Ge layer. The residual tensile strain in the layer was determined via both the Raman and HRXRD measurements with a reasonable agreement. All the characterization results indicate that the fabricated *p-i-n* structure is suitable for the realization of a high-performance photodetector. In the next chapter, we will discuss the development and characterization of the GOI photodetectors based on the vertical *p-i-n* structure.

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# Chapter 5 Development and Characterization of Normal-incidence GOI Vertical *p-i-n* Photodetectors

In this chapter, the development and characterization of normal-incidence GOI vertical *p-i-n* photodetectors will be discussed. The chapter starts with a description of the fabrication process flow. In order to achieve a good device performance, optimization on the individual process steps will then be carried out, which will be discussed in Chapter 5.2. The characterization results on the fabricated detectors will be presented and explained in Chapter 5.3. Chapter 5.4 will conclude this chapter.

## 5.1 Fabrication Process Flow

The realized GOI vertical *p-i-n* structure, as discussed in Chapter 4, was further developed into photodetectors based on the process flow depicted in Fig. 33. First, optical lithography followed by a chlorine ($Cl_2$)-based reactive-ion etching (RIE) was performed on the GOI to form the *n*- and *p*-mesa regions. According to the doping profile of the $BF_2^+$ implantation as shown in Fig. 29, the RIE of the *n*-mesa was stopped where ~150nm Ge remained to act as the *p*-mesa. A ~400nm $SiO_2$ layer was then deposited by PECVD for device passivation. Afterwards, ring-shaped trenches were patterned on both the *n*- and *p*-mesas to define the metal/Ge contact areas, where the $SiO_2$ was removed by RIE using carbon fluoride ($CF_4$)-based gases. To ensure a complete $SiO_2$ removal without damaging the Ge surface, the etching stopped at a residual $SiO_2$

thickness of ~50nm, followed by a dip in a buffered oxide etch (6:1) solution for ~15s. The device metallization comprises of the sputtering of a Ti (bottom)/TiN/Al (top) metal stack followed by lift-off to form the device contacts. RTA was then implemented to enhance the Ohmic characteristic of the contacts.

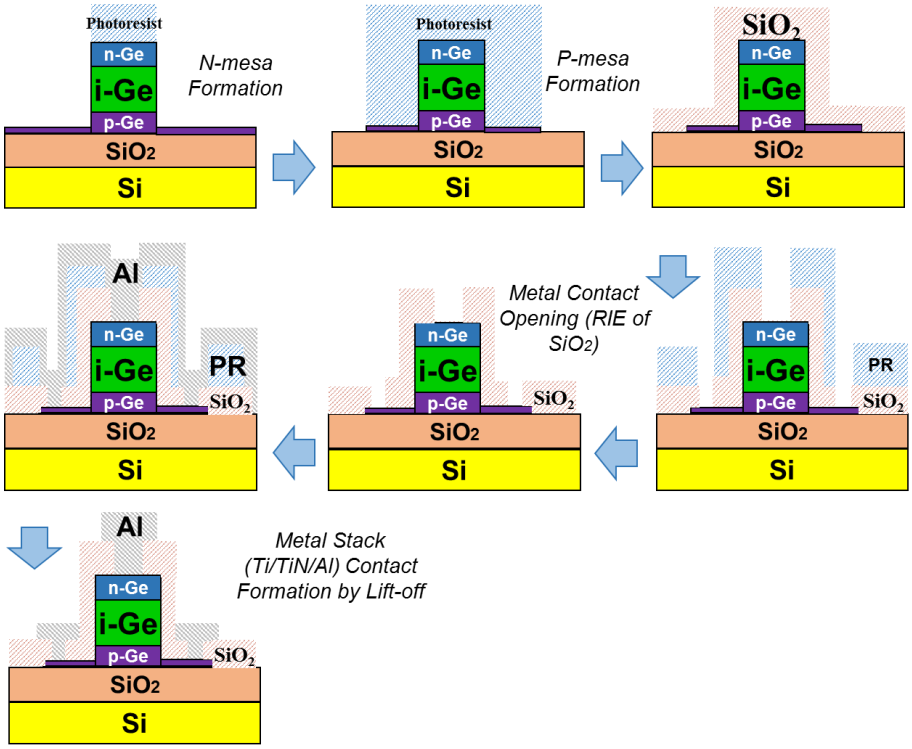


Figure 33 Schematic process flow for the fabrication of GOI vertical *p-i-n* photodetectors.

# 5.2 Development on Key Process Steps

Among the process steps discussed above, RIE and metallization are two of the key steps in achieving a high-performance photodetector. For the RIE process, a vertical sidewall is required on the Ge mesas for good device passivation and low surface leakage. In contrast, a slightly-angled (~70 to 80$^{o}$) sidewall is preferred for the $SiO_2$ RIE to prevent the step coverage during the metallization [1]. On the other hand, a low-

resistivity Ohmic contact is crucial for a photodetector with a maximal output photocurrent and reduced RC time delay. This requires a good metallization process, in which a minimal metal/Ge inter-diffusion and contact resistivity are two of the key factors influencing the contact performance.

Therefore, in this section, the work to develop these process steps will be studied and elaborated. Chapter 5.2.1 will talk about the optimization of the RIE process to achieve desired sidewall profiles for the Ge and $SiO_2$ etching. Chapter 5.2.2 will attempt to develop a low-resistivity metal/Ge contact with minimal metal/Ge inter-diffusion.

## 5.2.1 Reactive-ion Etching of Ge and $SiO_2$

The RIE studies for the Ge and $SiO_2$ etching were both performed in an Oxford Plasmalab 80 Etcher. As mentioned, $Cl_2$ gas was used for the Ge etching. Increasing the RF power and decreasing the chamber pressure could benefit a higher ion energy for the Cl-based species, which facilitates a vertical sidewall angle due to the resulting stronger physical bombardment. Meanwhile, provided a sufficient $Cl_2$ gas flow, a flat etched surface could be obtained by the timely reaction of the ion-sputtered Ge with the reactive Cl-based species, which forms a volatile $GeCl_4$ product that can be desorbed from the substrate surface. Hence, after tuning these parameters, an RF power of 200W and chamber pressure of 20mT was ultimately utilized, with the $Cl_2$ flow of 50sccm. The corresponding SEM image of an etched Ge mesa using the optimized recipe is shown in Fig. 34. A vertical sidewall can be clearly observed with a flat etched

surface acceptable for device fabrication. In addition to the $Cl_2$ gas, other gas combinations such as $SF_6$+$C_4H_8$ [2] and $SF_6$+$CHF_3$ [3] have also been reported and are capable of achieving vertical sidewalls. Besides, inductively-coupled plasma (ICP) etching could offer more flexibility over RIE for the control of the sidewall angle as well as the etched surface roughness, since the energy and the density of the reactive species could be controlled independently in the ICP chamber, alleviating the limitation of an insufficient number of reactive ions for RIE at a low chamber pressure.

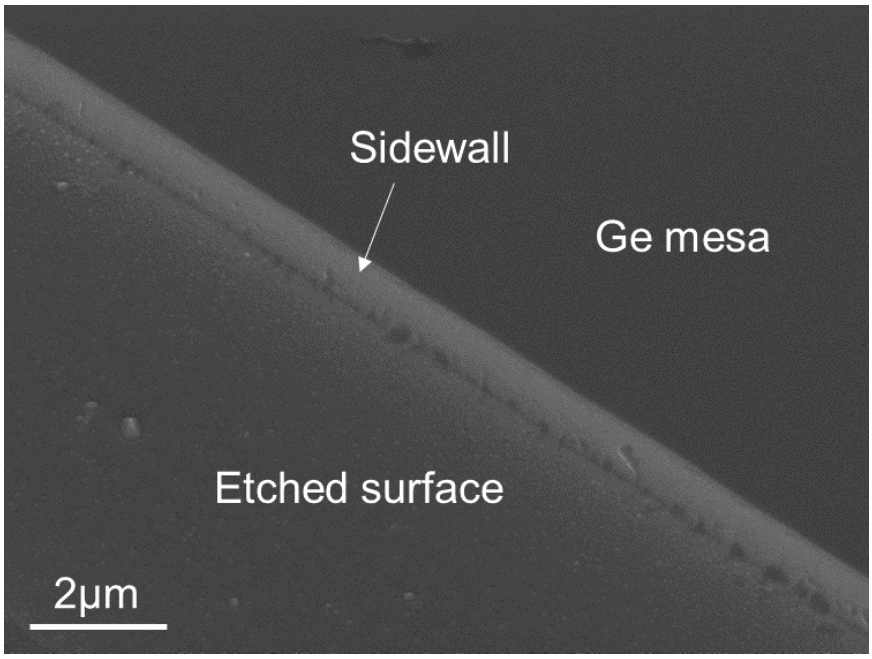


Figure 34 An SEM image of a Ge mesa etched using the optimized $Cl_2$-based RIE recipe.

The gases used for the $SiO_2$ RIE are $CF_4$ and $CHF_3$. The experiments were first carried out on dummy Si samples deposited with ~400nm $SiO_2$ by PECVD. After transferring the patterns via optical lithography, the photoresist itself acts as a hard mask for the subsequent RIE. The etched samples were then inspected at the cross-sectional view

to see the sidewall angles. Fig. 35 shows the SEM image using the recipe of 200W RF power, 150mT chamber pressure, and 30sccm each for the $CF_4$ and $CHF_3$ flow. The measured sidewall angle is ~79.2°, which is suitable for the metallization. Fig. 36 shows the ring-shaped trenches for the metal/Ge contact areas created on the $SiO_2$-passivated Ge mesas, using the same recipe.

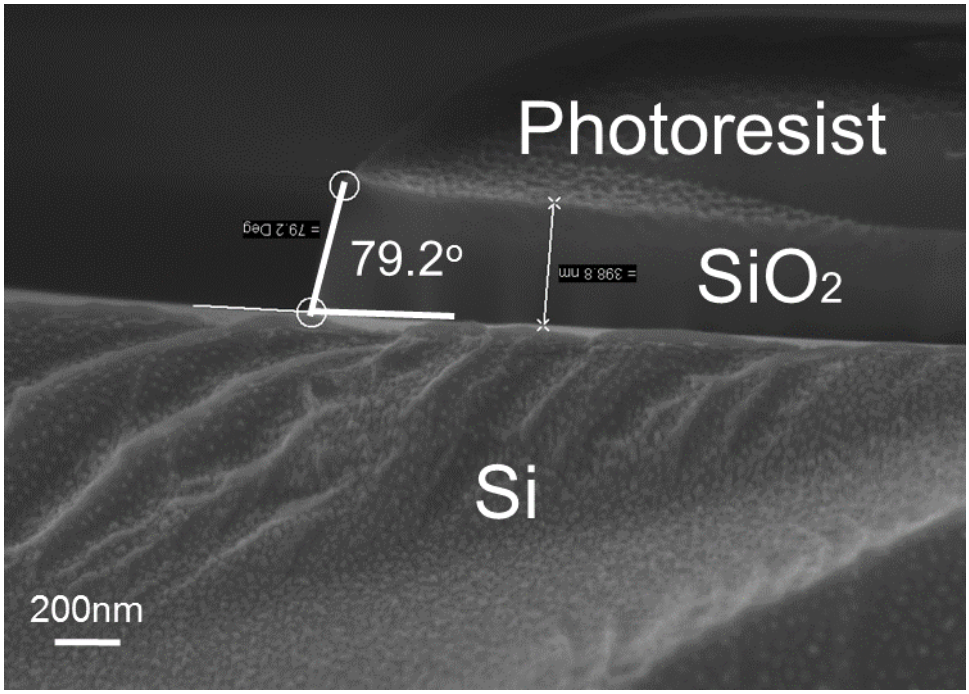


Figure 35 A cross-sectional SEM image showing the etched $SiO_2$ with a sidewall angle of 79.2°, using the optimized $CF_4$-based recipe.

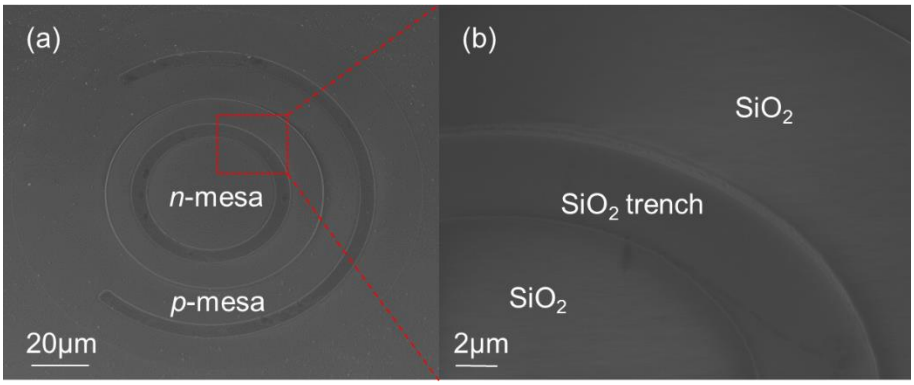


Figure 36 (a) Ring-shaped trenches created by the $SiO_2$ RIE on the Ge mesas for metal/Ge contact, using the same $CF_4$-based recipe as that used for Fig. 35. The magnified image at the region highlighted by the dashed box is shown in (b).

## 5.2.2 Metallization for Ohmic Contacts to Ge

### 5.2.2.1 Insertion of Sputtered Ti/TiN as a Diffusion Barrier

Aluminum (Al) is one of the commonly-used materials for contact metallization, especially in early-generation CMOS fabrication. Currently, it is also widely adopted in the research of Ge-based optoelectronic devices. However, depending on the temperature, Al and Ge have a significant solid solubility mutually with each other. As seen from the phase diagram in Fig. 37, the Ge could have a maximum ~2% solubility in Al and the Al could reversely have a maximum ~1.1% solubility in Ge. Such phenomenon could also be found in other CMOS-compatible metals with Ge, such as Cu and silver (Ag) [4]. Since severe spiking issue has been observed in conventional Al-Si contacts with a similar mutual solubility [5], it is expected that the Al-Ge contacts might also be similarly affected. Hence, a straightforward solution is to insert a diffusion barrier layer in between the Al and Ge.

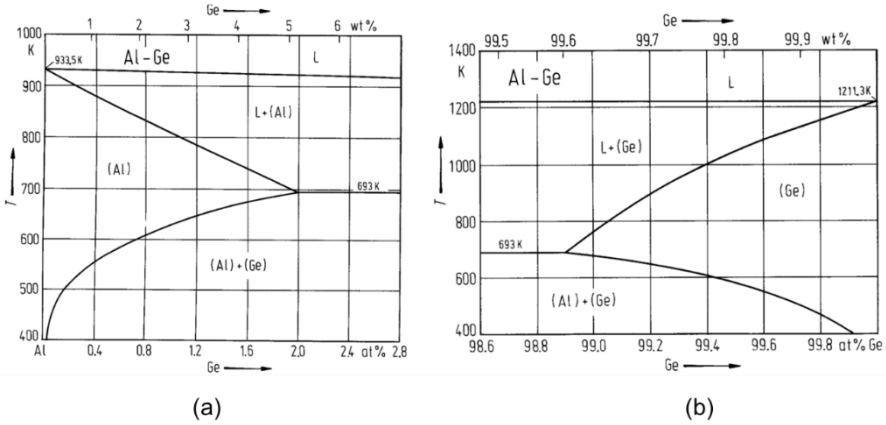


Figure 37 Al-Ge phase diagram with (a) Al-rich compositions and (b) Ge-rich compositions [4].

The initial trial started with an insertion of ~50nm Titanium (Ti) in between. The Ti layer could simultaneously provide a better adhesion to the underlying Ge, preventing its peel-off during the lift-off process. Both the Ti and the following Al (300nm) layers were deposited by Cello Ohmiker-60BL electron beam evaporator. Fig. 38 shows a cross-sectional SEM image of the Ti/Al stack on Ge after a RTA at 400$^{o}$C for 10mins. Voids can obviously be seen, which is similar to that observed at the Al-Si contact [5]. Since the metal layer is still intact on top of the voids, it is unlikely that these voids were formed due to sample dicing. To further verify the inter-diffusion between the Al and Ge, energy dispersive X-ray (EDX) mapping were carried out at the spots A and B as indicated in Fig. 38 (a). The corresponding elemental composition spectra were shown in Fig. 38 (b) and (c). A single Al peak was observed at location A while both Al and Ge peaks were found at location B, implying the occurrence of Al diffusion into Ge. Apparently, a single Ti layer by e-beam evaporation is insufficient as a diffusion barrier.

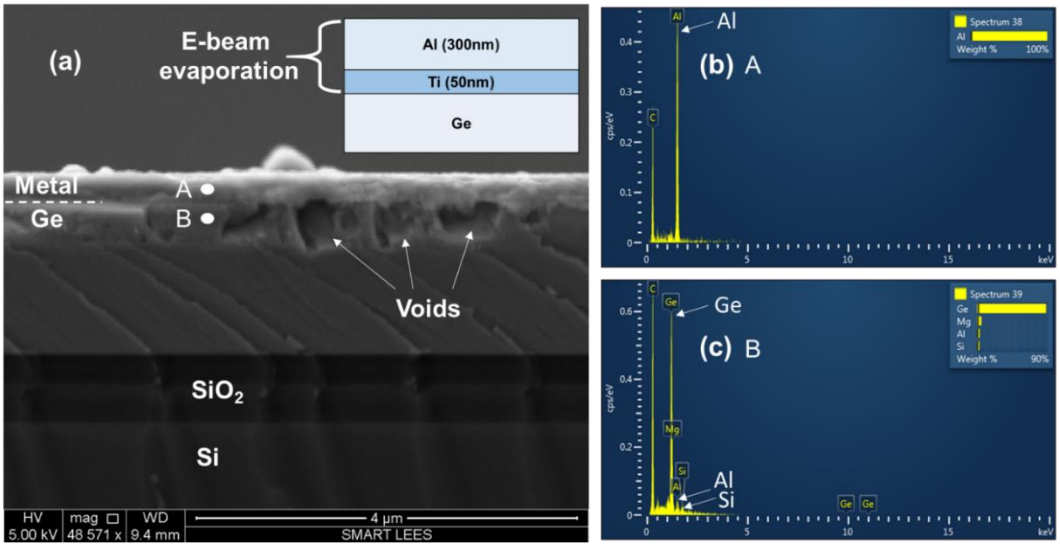


Figure 38 (a) A cross-sectional SEM image of the Ti/Al contact on Ge. Significant voids in Ge were observed. The inset indicates the schematic structure of the metal layers. The spectra of the EDX analysis performed at spots A and B in (a) are shown in (b) and (c), respectively.

Titanium nitride (TiN) has been widely adopted in CMOS industry (e.g. in Al-Si contacts [6] and Cu-filled through-silicon vias [7]) as a diffusion barrier layer. Therefore, it was also attempted to address the inter-diffusion issue in this work. Fig. 39 (b) shows the schematic structure of the metal stack employing TiN. A ~20 nm Ti and a ~50 nm TiN were sputtered sequentially in an Evatec Clusterline CLC200 system, before the e-beam evaporation of the original Ti/Al layers. Meanwhile, the post-deposition annealing time was shortened to 1min at 400$^{o}$C. The corresponding cross-sectional SEM image is shown in Fig. 39 (a). No void exists in the Ge layer. A clear contrast at the metal/Ge interface indicates a superior interface quality, compared to that without the sputtered Ti/TiN layers (Fig. 38 (a)), suggesting a suppressed inter-diffusion. EDX mapping at the circled spot (in Ge layer) in Fig. 39 (a) reveals a strong Ge peak without any detectable Al signal, indicating an insignificant Al diffusion into Ge.

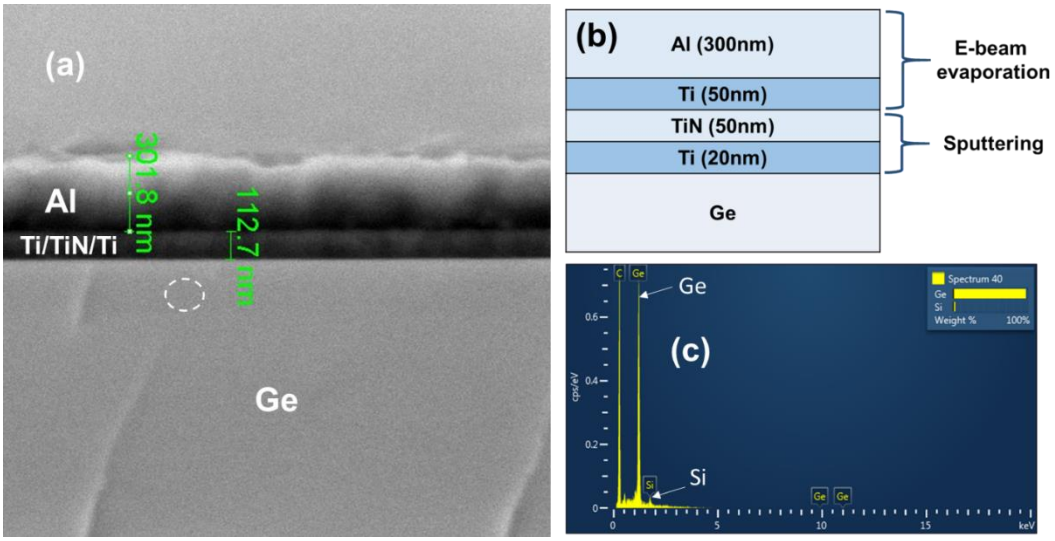


Figure 39 (a) A cross-sectional SEM image of the metal/Ge structure incorporating the sputtered Ti/TiN layers. The corresponding structure of the metal stack is shown in (b); (c) The EDX mapping spectra at the circled spot in (a).

In conclusion, the sputtered Ti/TiN layers could be well served as the diffusion barrier to minimize the Al-Ge inter-diffusion for a high-quality metal/Ge interface. To prevent the TiN oxidation, ultimately the top Al layer was also deposited in the sputtering system without breaking the vacuum. Therefore, as mentioned in Chapter 5.1, we used sputtered Ti/TiN/Al stack as the contact metal for the photodetectors.

### 5.2.2.2 Rapid Thermal Annealing for an Ohmic Contact

Due to the metal-induced gap states (MIGS) [8] at the metal/Ge interface, the Ge Fermi level is pinned at ~0.1eV above the valence band independent of the metal work function. Therefore, an Ohmic contact can be easily formed between the metal and *p*-type Ge; whereas a Schottky contact is usually formed between the metal and *n*-Ge. Apart from the Fermi-level de-pinning methods such as the insertion of intermediate thin insulator layers [9], a simple approach to realize an Ohmic contact to *n*-Ge is to ensure a heavy *n*-doping in Ge and a sufficient thermal treatment.

Both the steps could substantially reduce the metal/Ge Schottky barrier width to allow tunneling, besides thermionic emission, of the electrons through the contact, which enables an Ohmic contact behavior with a reduced resistivity. In this section, the RTA conditions will be studied, based on the *n*- and *p*-doping profiles achieved in Fig. 29, in order to obtain an Ohmic contact on both *n*- and *p*-Ge.

The transmission line method (TLM) measurements were carried out to characterize the contacts. An array of rectangular pads with width (W) and length (L) of 50 and 100μm, respectively, are patterned on the *n*- and *p*- mesa surfaces as the region for the contact. The distance (*D*) between the pads varies from 10 to 160μm. The Al-incorporated metal stack was then sputtered and lifted-off, as described in Chapter 5.2.2.1, to form the contacts. Afterwards, RTA was performed in $N_2$ ambient at a varied temperature and duration for an optimal Ohmic contact performance. An Agilent B1500A semiconductor parameter analyzer was used to trace the current-voltage (I-V) characteristics between adjacent contacts, by sweeping the voltage bias.

Fig. 40 (a) shows a microscope image of the fabricated TLM structure, with the definition of the respective dimensions indicated. Fig. 40 (b) summarizes the I-V characteristics between the contacts of *D*=10μm, at three different metal stacking and RTA conditions. The RTA at 400$^{o}$C leads to linear I-V curves, indicating an Ohmic characteristic of the contacts. However, decreasing the RTA duration to 1min and adopting sputtered Ti/TiN layers exhibit a ~64-fold increase on the drive current, under an identical voltage bias. The prominent decrease on the contact

resistance can be attributed to the alleviated Al-Ge inter-diffusion, as discussed in Chapter 5.2.2.1, resulted from both the Ti/TiN diffusion barrier and the shortened RTA time. The suppressed inter-diffusion is expected to hinder the formation of Ge voids beneath the contact and sustain a sufficient contact area for a low contact resistance. The RTA at 320°C results in a Schottky I-V characteristic, indicating an insufficient thermal budget to form the Ohmic contact. Therefore, the Ti/TiN/Al stack with RTA at 400°C for 1min will be utilized as the metallization condition for the photodetector fabrication.

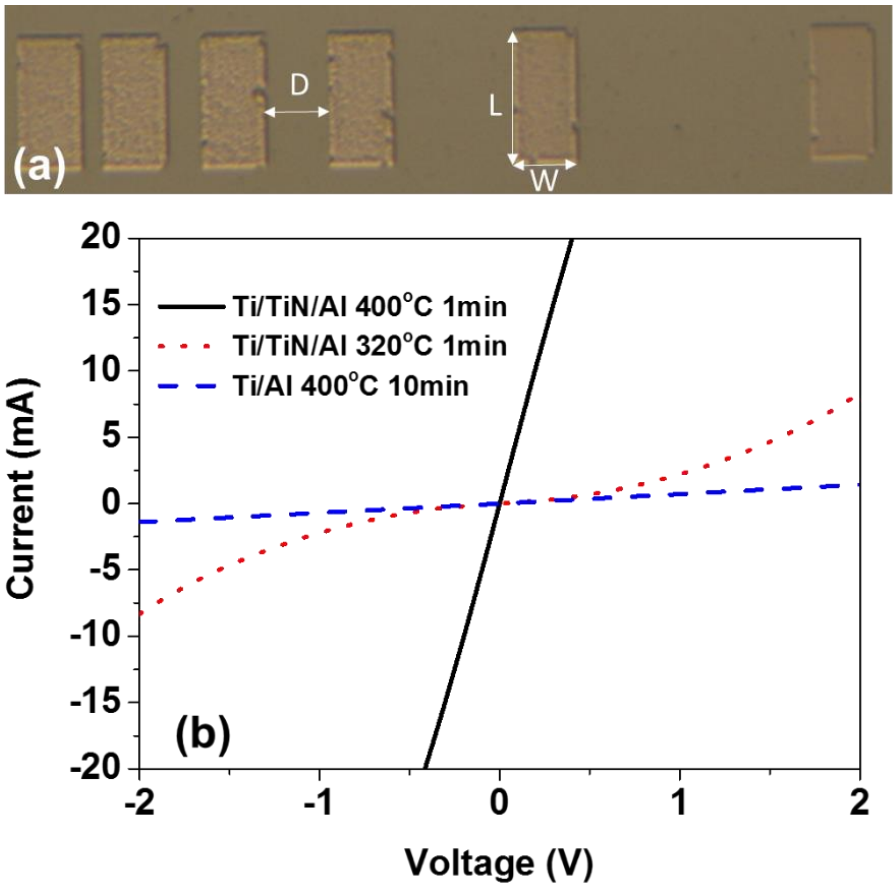


Figure 40 (a) A microscope image of the fabricated TLM structure with the respective dimensions defined; (b) I-V characteristics between the metal pads of D=10μm, at different metal stacking and RTA conditions.

To further find out the contact resistivity at the desired condition, the I-V curves from the TLM patterns on *n*- and *p*-Ge were collected and

plotted in Fig. 41 (a) and (b), respectively. All the curves are linear and revealing the characteristic of Ohmic contact. The corresponding resistance values, obtained from dividing the voltage by current, are plotted with respect to *D*, as shown in Fig. 41 (c) and (d), to extrapolate the contact resistance on *n*- and *p*-Ge, respectively. Since the measured resistance value ($R$) between any two contacts consists of the resistance of the both contacts ($R_c$) and the Ge material in between ($R_{Ge}$), which can be expressed as follows:

$$R = 2 \times R_c + R_{Ge} \tag{5.1}$$

where $R_{Ge}$ is proportional to the inter-contact distance *D*. Hence, the *y*-intercept of the linear curve-fitting on the measured data could decouple the $R_c$ from $R$, where *D*=0 and there is no $R_{Ge}$. The *y*-intercept for the *n*- and *p*-contact were thus extrapolated as 18.14 and 2.28Ω, respectively, indicating a corresponding $R_c$ of 9.07 and 1.14Ω.

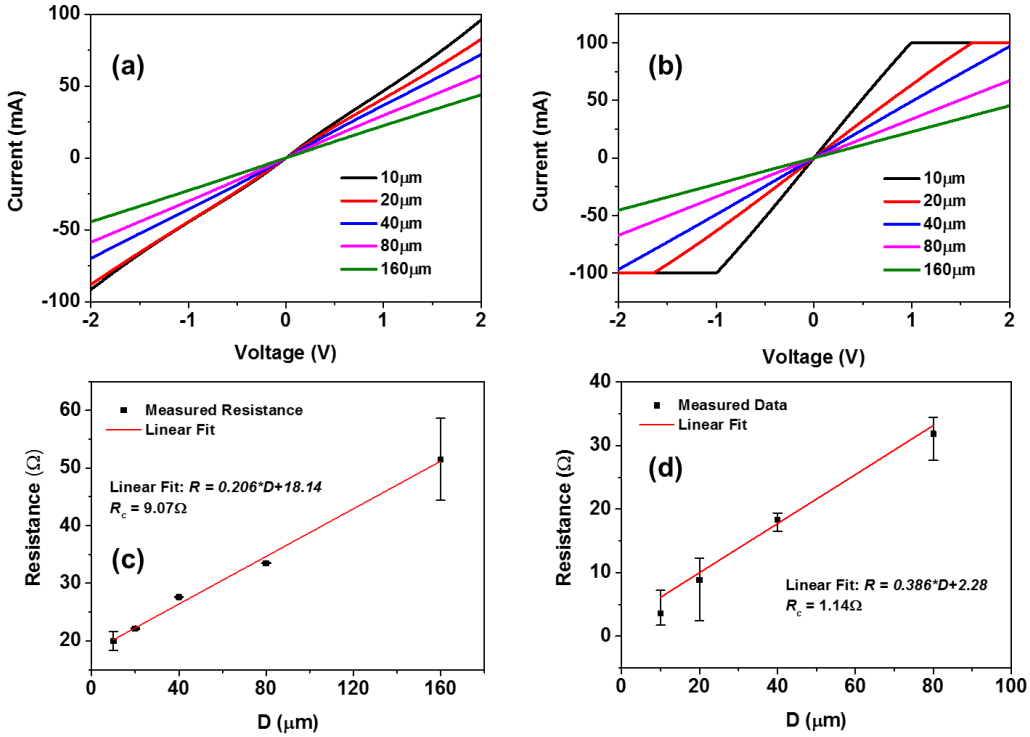


Figure 41 I-V characteristics for the Ti/TiN/Al contacts on (a) *n*- and (b) *p*-Ge, after RTA at 400°C for 1min, with respect to the inter-contact distance *D*. The corresponding contact resistance for the *n*- and *p*-contact were extrapolated in (c) and (d), respectively.

The contact resistivity $\rho$ can be further calculated as:

$$\rho = R_c W_T L \tag{5.2}$$

where $W_T$ is the transfer length denoting the average distance a carrier travels beneath the contact before it is collected by the contact. The $W_T$ can also be extrapolated from the fitted curves in Fig. 41 (c) and (d) by calculating $D = -2W_T$, where $R$=0. Therefore, the contact resistivities for the *n*- and *p*-contact are estimated as ~$4.0\times10^{-4}$ and $3.4\times10^{-6}$ Ω•cm$^2$, respectively, which are reasonable compared with the reported values [10, 11].

## 5.3 Device Characterization

Based on the process optimization discussed in Chapter 5.2, the GOI vertical *p-i-n* photodetectors were successfully fabricated, following the process flow in Chapter 5.1. Fig. 42 (a) shows an optical microscope image of a fabricated photodetector with its *n*-mesa diameter of 80μm. The image reveals clear device surface features of the mesa regions and metal pads. The field emission scanning electron microscope (FESEM) image below in (b) shows the cross-sectional structure of the detector diced from the black solid line in (a). The respective layers, together with *n*-Ge mesa and contact, can be clearly observed.

Chapter 5.3.1 will describe the characterization techniques employed to evaluate the performance of the photodetectors. Afterwards, the characterization results will be discussed in Chapter 5.3.2.

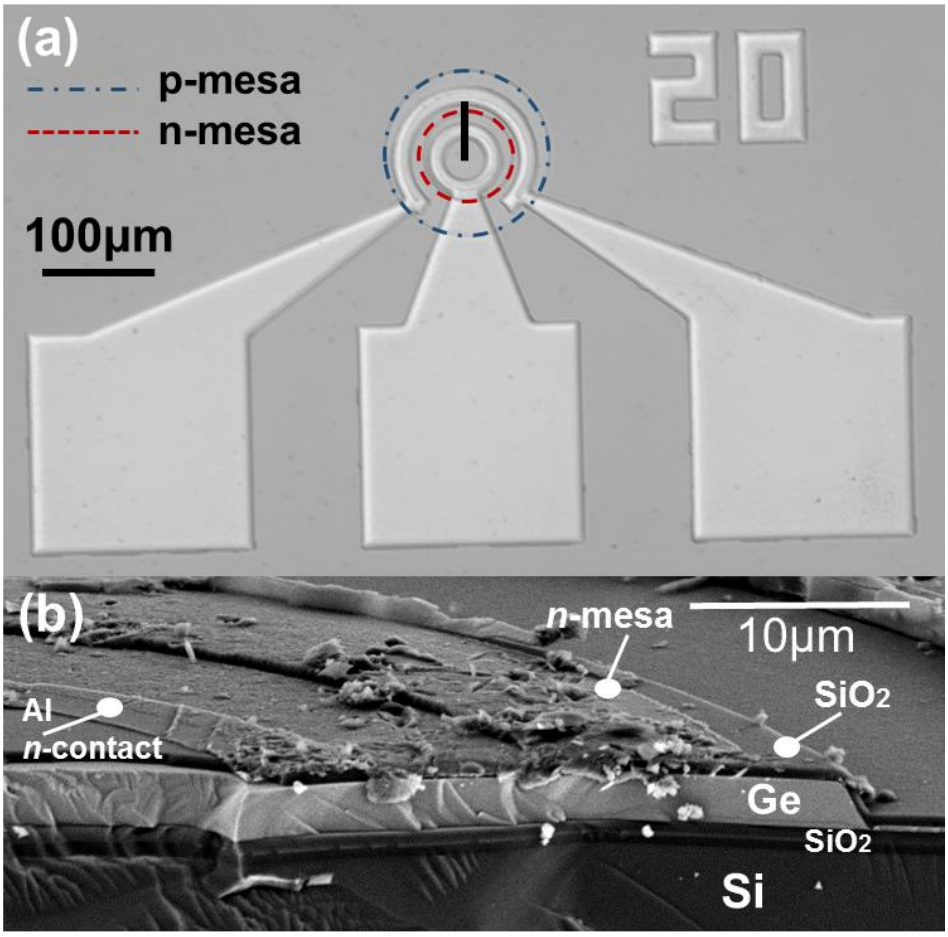


Figure 42 (a) An optical microscope image of a photodetector with its *n*-mesa diameter of 80μm; (b) a FESEM image of the fabricated photodetector diced from the black solid line highlighted in (a).

## 5.3.1 Characterization Methodology

The GOI vertical *p-i-n* photodetectors were characterized in terms of their dark current, optical responsivity, and high-frequency performance. The current-voltage (I-V) characteristic was measured by an Agilent B1500A semiconductor parameter analyzer. The I-V curves were also collected as a function of temperature ranging from 293 to 353 K to analyze the origin of the dark current. To measure the optical responsivity, a TUNICS T100S-HP/CL tunable laser covering *C*- and *L*-bands (1500 to 1630 nm) was utilized as the light source. As shown in the

inset of Fig. 43 (a), light was coupled into a Corning SMF-28 single-mode silica glass fiber to normally illuminate on the devices. Voltage bias and photocurrent were applied and collected using an Aim-TTi QL355TP power supply and a Keysight 34450A multimeter, respectively, via electrical probes placed on the *n*- and *p*-contact pads. The photocurrent was measured with respect to the applied bias at 1550nm and across the entire *C*- and *L*-band at -2V.

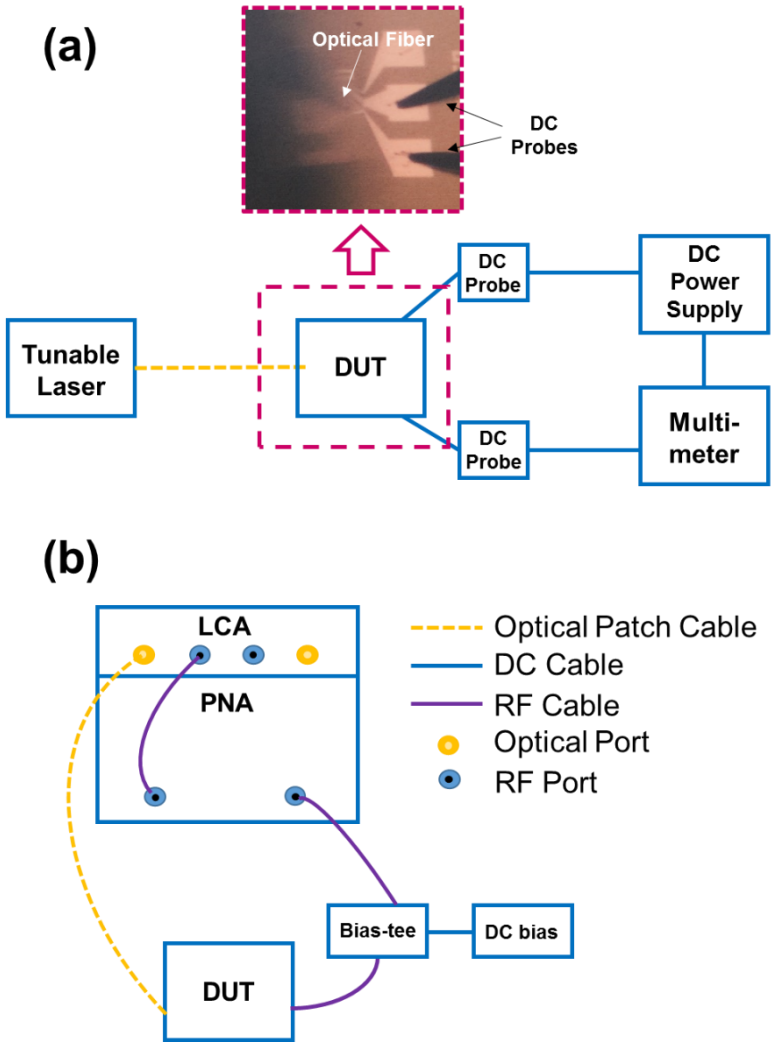


Figure 43 Schematic diagrams of the testing set-up for the (a) optical responsivity and (b) frequency response measurement. The inset in (a) shows a photo captured above the device-under-test (DUT), highlighted by the dashed box in the schematic.

The frequency response of the devices was evaluated by the scattering (S)-parameter measurement via an Agilent N5244A PNA-X network analyzer, with an Agilent N4373D lightwave component analyzer (LCA) as the modulated light source. An RF cable of 40GHz bandwidth was used. Calibration had been completed before the measurements to exclude the frequency response from the bias-tee, RF cable, and ground-signal-ground (GSG) probe. The schematics for both the measurement configurations are shown in Fig. 43. To support the analysis on the device internal QE and high-frequency performance, capacitance-voltage (C-V) measurement on the detectors was performed by probing the contact pads using a Keithley 4200-SCS semiconductor characterization system at a frequency of 100 KHz.

## 5.3.2 Results and Discussion

### 5.3.2.1 Dark Current Analysis

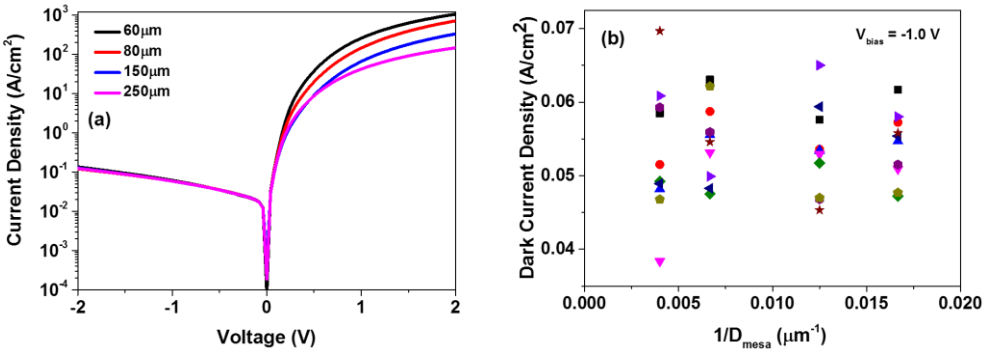


Figure 44 Dark current density-voltage characteristic of the GOI vertical *p-i-n* photodetectors at different *n*-mesa diameters; (b) summarized dark current densities for the photodetectors at -1V, as a function of the reciprocal of the *n*-mesa diameters.

Fig. 44 (a) shows the dark current density-voltage characteristic of the fabricated GOI vertical *p-i-n* photodetectors at different *n*-mesa diameters. The dark current densities are ~47mA/cm$^2$ at the reverse bias

of 1V, irrespective of the mesa diameter. The dark current mainly comprises of two components, namely bulk leakage and surface leakage current. The bulk leakage is proportional to the *n*-mesa area, whereas the surface leakage is proportional to the *n*-mesa perimeter. Therefore, the dark current density can be expressed as:

$$J_{dark} = J_{bulk} + \frac{4J_{surf}}{D_{mesa}} \tag{5.3}$$

where $J_{dark}$ is the dark current density, $J_{bulk}$ the bulk leakage current density, $J_{surf}$ the surface leakage current density and $D_{mesa}$ the *n*-mesa diameter. According to the equation, the current density independent of the mesa size indicates that there is negligible peripheral leakage current contributing to the device dark current, implying a good quality of the $SiO_2$ passivation. For a further verification, ten photodetectors were randomly selected from each mesa diameter, whose dark current density were summarized as a function of the reciprocal of the mesa diameter, as shown in Fig. 44 (b). Similarly, the dark current density is negligibly dependent on the mesa diameter, verifying a minimal contribution from the surface leakage.

To better understand the physical origin of the dark current, its activation energy was investigated, by performing the temperature-dependent I-V measurement on the device. The variation of the dark current, with respect to temperature, can manifest the dominating mechanism of its formation. The dark current $I_{dark}$ can be modelled as follows, as a function of temperature [12]:

$$I_{dark} = \mathrm{B} \cdot T^{1.5} e^{-E_a/kT} \left( e^{qV/2kT} \text{-} 1 \right) \tag{5.4}$$

where *B* is a constant, *T* is the temperature in Kelvin (K), $E_a$ is the activation energy for the dark current and *V* is the applied bias. The ideality factor *n* = 2 is used since, as will be revealed later, $I_{dark}$ is dominated by trap-assisted mechanisms. The $E_a$ can thus be extracted as the gradient of the linear fitting on the nature logarithm of $(I_{dark}/T^{1.5})$ as a function of $(1/kT)$, as shown in Fig. 45. The fitting gives a gradient of ~0.336 eV, corresponding to an activation energy $E_a$ about half of the indirect Ge bandgap (~0.66 eV). This indicates that the dark current mainly originates from the Shockley-Reed-Hall (SRH) process via the deep-level traps in the Ge bandgap [12]. This mechanism has been correlated to the carrier generation from threading dislocations in Ge at the depletion region under reverse bias [13]. Therefore the dark current is expected to be reduced further by using the oxygen-annealed GOI substrate with a suppressed Ge threading dislocation density [14].

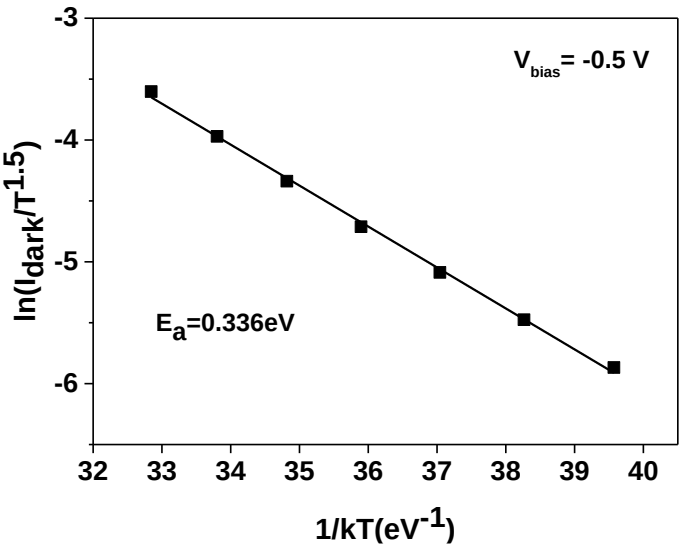


Figure 45 Activation energy extraction based on the temperature-dependent measurement on the dark current of the photodetector biased at -0.5V.

### 5.3.2.2 Optical Response

Fig. 46 shows the photocurrent of a GOI vertical *p-i-n* photodetector, with an *n*-mesa diameter of 250 μm, with respect to the applied bias. The corresponding dark I-V characteristic was appended as a reference. It could be observed that the photocurrent saturates at ~2.6 mA for a reverse bias higher than 0.3 V, exhibiting a potential for low-energy-consumption operation. The inset exhibits the measured photocurrent as a function of the incident optical power to the photodetector. The optical power values have taken into account the coupling loss of ~1.6 dB from the laser to the output end of the fiber. A good linearity was found between the optical power and photocurrent, revealing a typical behavior of a photodetector.

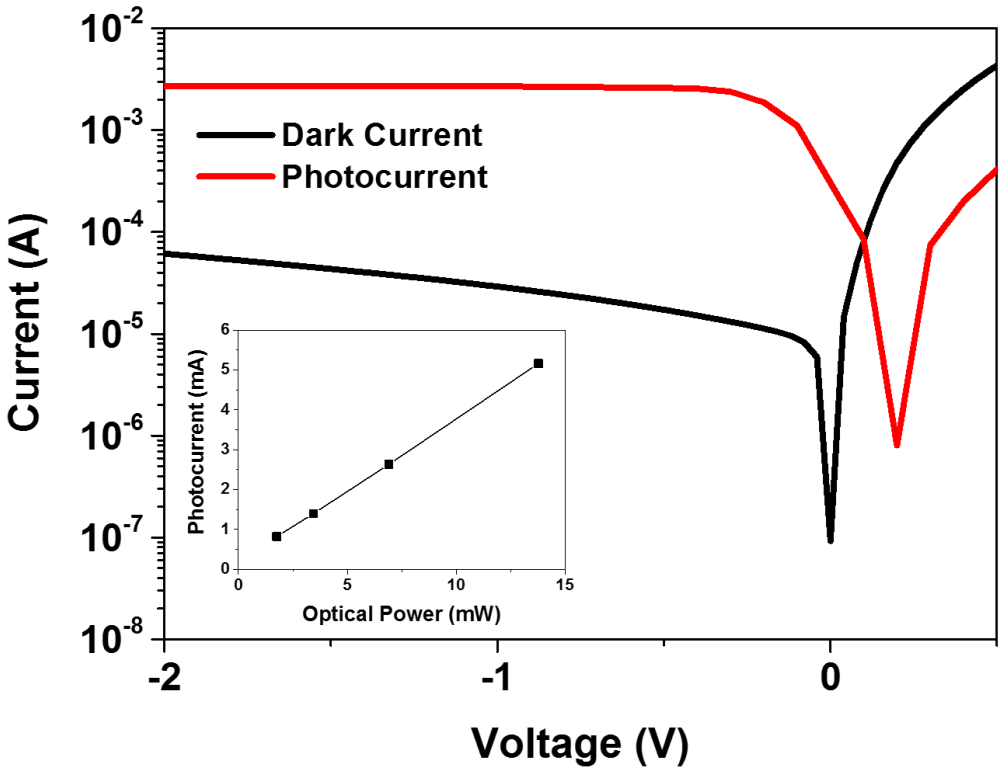


Figure 46 Photocurrent (at 1550 nm) of a GOI vertical *p-i-n* photodetector (*n*-mesa diameter of 250 μm) as a function of the applied voltage bias. Inset shows the photocurrent of the detector as a function of the incident optical power.

Given the measured ~6.9 mW illumination coming out of the fiber at 1550 nm, the device optical responsivity was determined as ~0.39 A/W. The dark current density and optical responsivity are comparable to that of the reported high performance Ge-on-Si and Ge-on-SOI photodetectors with similar *i*-Ge thicknesses [15-19], as shown in Fig. 47, implying a good material quality and device fabrication. Besides, the responsivity is higher than that of the reported GOI photodetectors [20, 21], as listed in the same figure, due to the adoption of the vertical manner for the *p-i-n* structure for a sufficient optical absorption.

It is worthy to note that surface reflection is not excluded from the responsivity calculation. To simply estimate the effect of surface reflection, the fiber was probed surface-normal to touch the $SiO_2$

passivation layer on the *n*-mesa during all photocurrent measurements. Assuming the interface between the passivation layer and the cleaved end of the fiber is lossless, the light can thus be considered propagating in silica/$SiO_2$ ambient before reaching the Ge. Therefore, the surface reflection can be calculated by the Fresnel relation:

$$r = \left|\frac{n_1 - n_2}{n_1 + n_2}\right|^2 \quad (5.5)$$

where $r$ is the surface reflectance and $n_1$ and $n_2$ are the refractive indices of $SiO_2$ (~1.44) and Ge (~4), respectively. As a result, the surface reflection could account for ~23% loss of the incident power. The responsivity could reach ~0.51 A/W by minimizing the surface reflection with proper anti-reflection coating. In addition, the optical absorption shielded by the *n*-mesa contact metal can be treated as negligible, since the diameter of the fiber core (~10 μm) is much smaller than that of the *n*-mesa.

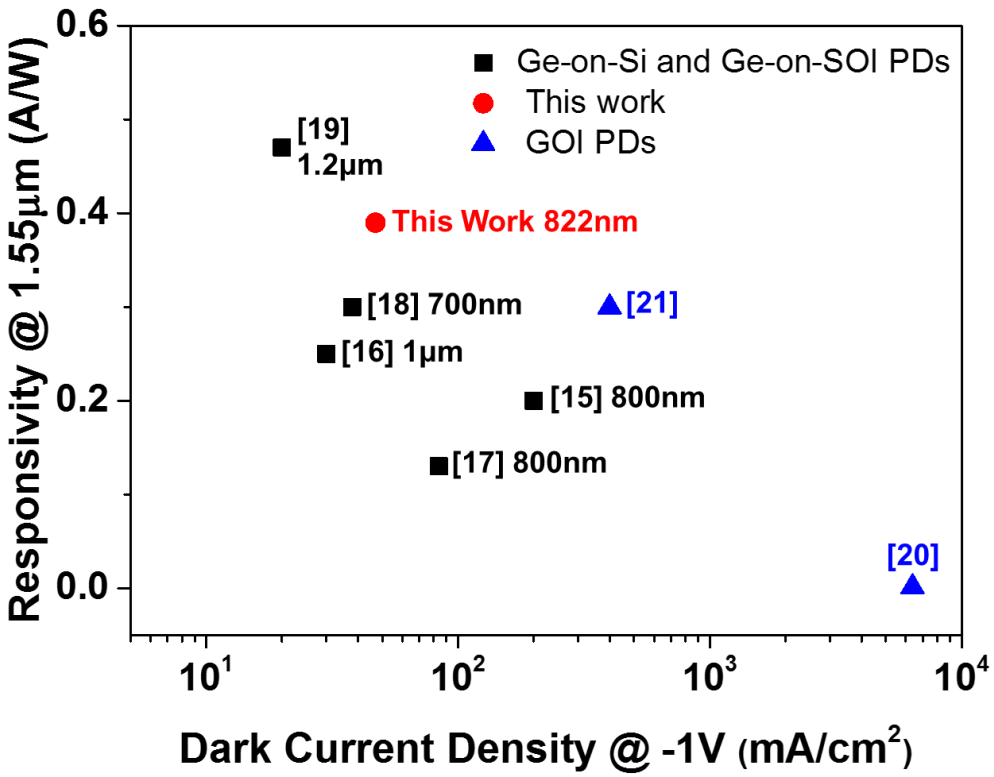


Figure 47 Performance comparison among Ge-based photodetectors. Thickness of the *i*-Ge layer for the corresponding Ge-on-Si and Ge-on-SOI devices were indicated. The numbers in square brackets are the serial numbers for the corresponding literatures in the reference list. The *i*-Ge thickness for the GOI PDs was not indicated due to their discrepant configurations (interdigitated lateral *p-i-n* [20] and waveguide-integrated [21]).

From the optical responsivity measurement, the IQE of the device could also be extracted from the following relationship [17, 18]:

$$\Re = \frac{\lambda\,(\mu m)}{1.24}(1-r)\eta_i e^{-\alpha_{Ge} d_{n-Ge}}\left(1-e^{-\alpha_{Ge} d_{i-Ge}}\right) \tag{5.6}$$

where $\Re$ is the measured device responsivity, $\lambda$ is the incident photon wavelength (1.55 μm), $r$ is the surface reflectance from Eq. (5.5) and $\eta_i$ denotes the IQE. $d_{n-Ge}$ and $d_{i-Ge}$ are the thickness for the *n*-Ge and *i*-Ge layers, respectively, while $\alpha_{Ge}$ refers to the absorption coefficient of Ge. $\alpha_{Ge}$ = 7032 cm$^{-1}$ was obtained from the ellipsometer-fitted extinction coefficient $k_{Ge}$ on the as-grown Ge-on-Si wafer before the bonding and layer transfer, via $\alpha_{Ge} = 4\pi k_{Ge}/\lambda$. $d_{n-Ge}$ was determined as ~130 nm from the SIMS characterization (Fig. 29) and $d_{i-Ge}$ was calculated as

~822 nm from the C-V measurement among the devices with different *n*-mesa areas. The junction capacitance $C_j$ can then be simply extracted from the linear interpolation on the measured capacitance data, which will be discussed in detail in Chapter 5.3.2.3 (Fig. 50 (b)). The $C_j$ extracted at -2 V was then converted using $d_{i-Ge} = \varepsilon_0 \varepsilon_r A / C_j$, where $\varepsilon_0$ is the vacuum permittivity, $\varepsilon_r$ is the Ge dielectric constant and $A$ is the *n*-mesa area. By substituting all these parameters into the equation, an IQE of ~97% was extracted, demonstrating an excellent carrier collection efficiency within the Ge *p-i-n* structure.

Fig. 48 shows the responsivity spectrum of the photodetector across the *C*- and *L*-bands. A nearly flat spectrum at ~0.4 A/W was observed until a drastic drop occurred from ~1570 nm onwards, due to a reduced density of states capable of accommodating the generated electron-hole pairs near the direct band edge of Ge. In addition, two tiny peaks at ~1570 and ~1591 nm could be identified in the spectrum where a significant sharper decrease of the responsivity started, compared to that at the lower wavelengths. These two peaks are likely to be correlated with the Ge direct bandgaps at *Γ*-valley (i.e. $E_g^{LH}$ *and* $E_g^{HH}$ mentioned in Chapter 3.4). As discussed in that sub-section, the residual biaxial tensile strain in Ge reduces its bandgap and causes the non-degeneracy at the valance band maximum, namely the splitting of the heavy-hole (HH) and light-hole (LH) sub-bands, which can be explained by the deformation potential theory (Eq. (3.4) to (3.7)). The corresponding calculated band edges are shown in the inset of Fig. 48, as a function of the biaxial tensile strain ($\varepsilon = \varepsilon_{xx} = \varepsilon_{yy}$ as in Eq. (3.4) and (3.5)). Plugging in the ~0.15%

biaxial strain value obtained from the HRXRD measurement (Chapter 4.3), the estimated cut-off wavelengths for the *Γ*-HH *and Γ*-LH band absorption are ~1569 and ~1589 nm, respectively, agreeing well with that of the two peaks from the responsivity spectrum. Therefore, similar to the epi-grown Ge photodetectors [22, 23], the residual tensile strain in the material benefits the absorption extension for the GOI photodetectors into the *L*-band.

However, the GOI detectors exhibit a higher QE than that of the as-grown Ge detectors at the *L*-band, with a responsivity of ~0.27 and ~0.13 A/W at 1600 and 1620nm, respectively. The reason still requires further investigation but it could probably be attributed to a more prominent absorption from the photons back-reflected from the bottom $SiO_2$ layer. The larger index contrast between $SiO_2$ (~ 1.44) and Ge (~ 4), compared to that between Si (~ 3.47) and Ge, might enhance the optical reflection back to the Ge layer to collect the unabsorbed photons, particularly when the Ge absorption coefficient starts to decrease. This might enable a better sensitivity performance for the GOI photodetectors at the *L*-band.

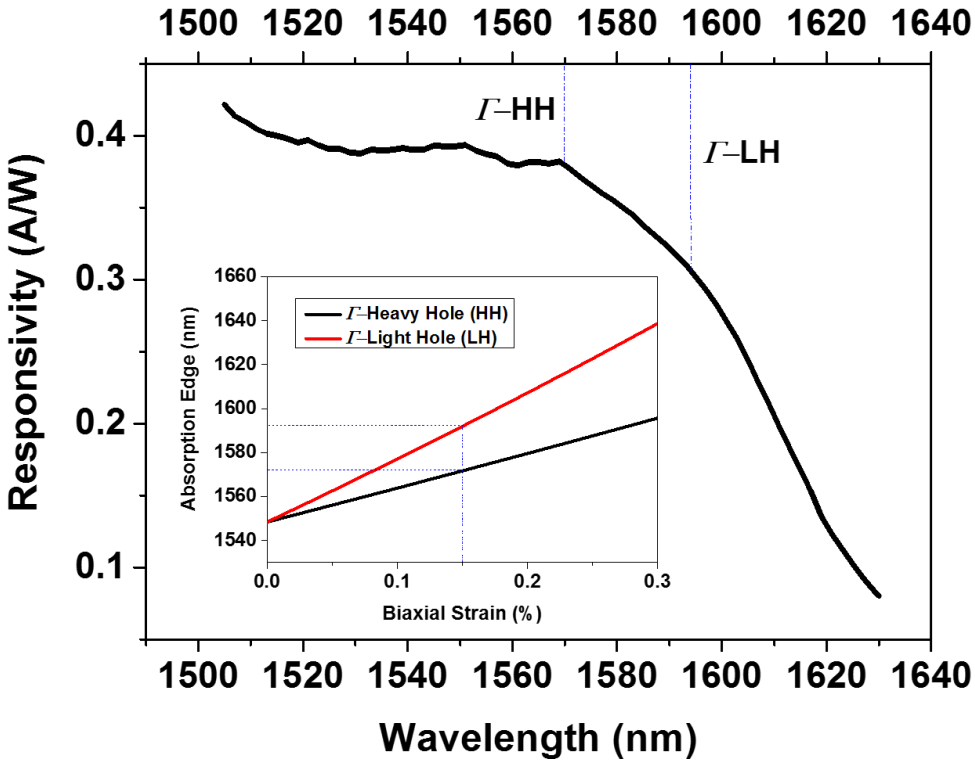


Figure 48 Optical responsivity spectrum of a GOI vertical *p-i-n* photodetector across the *C*- and *L*-bands. The two tiny peaks are likely the *Γ*-HH and *Γ*-LH band edges. Inset shows the calculated Ge direct-band edges as a function of its biaxial strain, using the deformation potential theory discussed in Chapter 3.4.

### 5.3.2.3 High-frequency Response

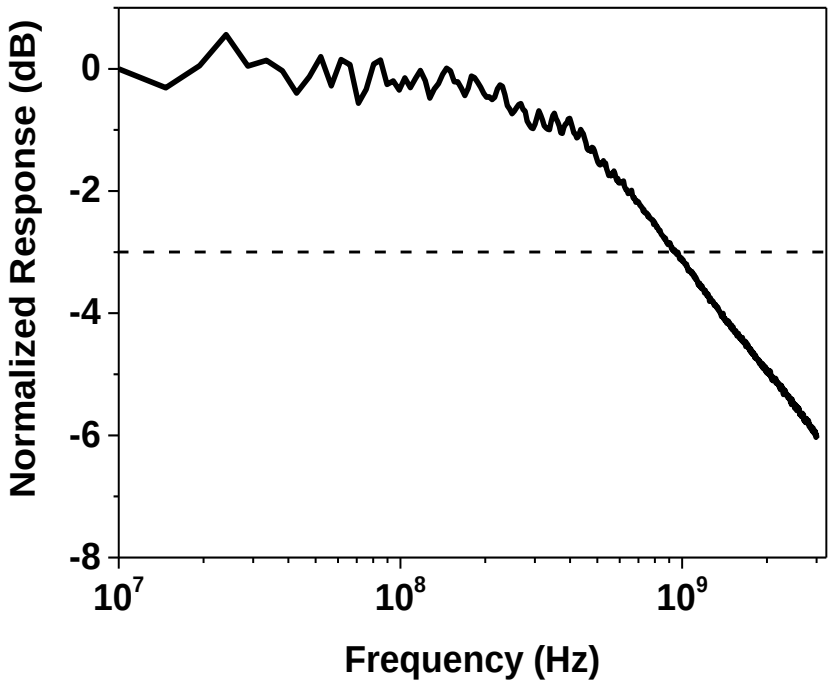


Figure 49 Frequency response of a GOI vertical *p-i-n* photodetector with its *n*-mesa diameter of 60 µm, biased at -2 V.

Fig. 49 shows the normalized frequency response of a GOI vertical *p-i-n* photodetector biased at -2 V, where an excellent carrier collection efficiency has been established. The frequency bandwidth is ~1 GHz at which a 3-dB (i.e. 50%) drop on the device electrical response occurs. The 3dB-bandwidth is theoretically determined by both the RC delay from the detector and the carrier transit time across the Ge depletion region [18], which can be expressed in Eq. (5.7) to (5.9) below:

$$f_{3-dB} = \left(1/\left({f_{transit}}^{-2} + {f_{RC}}^{-2}\right)\right)^{1/2} \quad (5.7)$$

$$f_{RC} = 1/2\pi RC \quad (5.8)$$

$$f_{transit} = 0.45 \cdot v_{sat}/d_{i-Ge} \quad (5.9)$$

where $f_{transit}$ and $f_{RC}$ refer to the 3dB-bandwidth limited by the carrier transit and RC delay, respectively. To accurately estimate the device performance, the contact series resistance $R_s$ from the device metal/semiconductor contacts was included into the total resistance $R$ in Eq. (5.8), apart from the load resistance ( $R_L$ = 50 Ω ) from the measurement apparatus. Similarly, the parasitic capacitance $C_p$ from the device contact pads was also included into the total capacitance $C$, besides the *p-i-n* junction capacitance $C_j$. The $v_{sat}$ in Eqn. (5.9) denotes the carrier saturation drift velocity in Ge (~$6 \times 10^6$ cm/s [18, 24]) and $d_{i-Ge}$ is the thickness of the *i*-Ge layer (822 nm). $R_s$ was determined from the reciprocal of the first-order derivative of the forward-biased detector I-V characteristic ($1/(dI/dV)$) at 2 V, as shown in Fig. 50 (a). To de-couple $C_j$ and $C_p$, linear interpolation was carried out on the measured device capacitance *C* at -2 V, with respect to the *n*-mesa areas. The fitted curve satisfies the following relation:

$$C = k \cdot C_{j-60\mu m} + C_p \tag{5.10}$$

where $k$ is the area ratio of the device *n*-mesas with respect to that of the smallest *n*-mesa (60μm in diameter) and $C_{j-60\mu m}$ is the junction capacitance of that smallest mesa. $C_{j-60\mu m}$ and $C_p$ could thus be extracted from the slope and *y*-intercept of the linear fit, respectively, as indicated in Fig. 50 (b). As the calculated $f_{transit}$ (~33 GHz) is much larger than $f_{RC}$ (~1.1 GHz), the detector is dominantly limited by the RC delay and therefore the measured 3dB-bandwidth reasonably matches with $f_{RC}$.

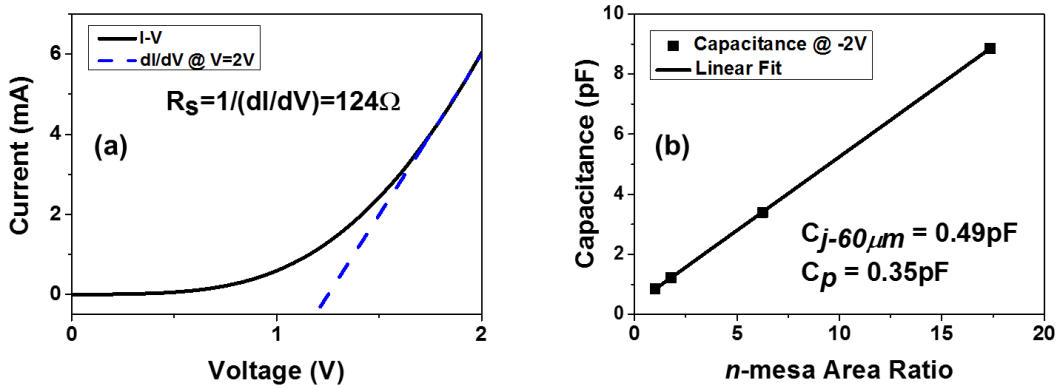


Figure 50 (a) Contact series resistance extracted from the forward-biased linear-scale I-V characteristic of the photodetector; (b) linear interpolation of the device capacitances from the C-V measurement, as a function of the *n*-mesa areas.

It is apparent that the device speed could be further improved by reducing $R_s$ and $C_j$. As shown in Fig. 51 (a), the projected $f_{3-dB}$ increases with decreasing *n*-mesa diameter due to the suppressed RC delay. As the core diameter for the single mode fiber is ~10 μm, a GOI vertical *p*-*i*-*n* detector with 10 μm *n*-mesa diameter and reasonable $R_s$ of 30 Ω [25], excluding the influence of $C_p$, is estimated to own a 3dB-bandwidth of ~32 GHz, which is close to the theoretical maximum bandwidth limited by the carrier transport across the *i*-Ge. It is also calculated, as shown in Fig. 51 (b), that the detectors with an *n*-mesa diameter of 10μm start to be carrier transit-limited with a minimal influence from the RC delay, for the *i*-Ge layer thicker than 400 nm. Therefore, although performance compromise exists between the responsivity and speed, the potential for high-speed fiber-optic communication can be fully utilized, where both a reasonable responsivity (*i*-Ge > 400 nm) and maximal speed can be projected simultaneously.

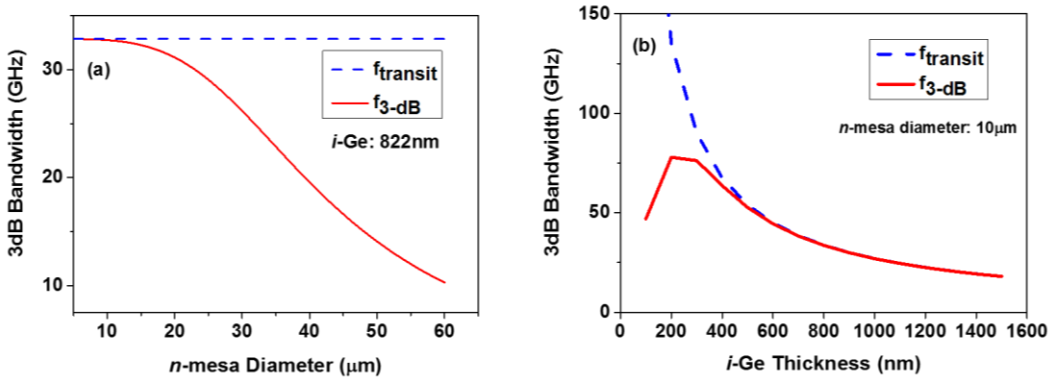


Figure 51 (a) calculated 3dB-bandwidth (red solid line) of a GOI vertical *p-i-n* photodetector ($R_S$=30 Ω) with respect to its *n*-mesa diameter. The dashed line represents the corresponding carrier transit-limited bandwidth. The *i*-Ge thickness is 822 nm; (b) calculated 3dB-bandwidth of the photodetector as a function of the *i*-Ge thickness. The *n*-mesa diameter is 10 μm.

# 5.4 Conclusion

In this chapter, normal-incidence vertical *p-i-n* photodetectors have been successfully developed on a GOI platform. First, process development on key fabrication steps was carried out. Reactive-ion etching of Ge mesas and $SiO_2$ passivation layer was optimized for desired sidewall profiles. Sputtered Ti/TiN/Al metal stack was utilized for the device contacts to prevent the Al-Ge inter-diffusion. It was verified that rapid thermal annealing at 400°C for 1 min could form good Ohmic contacts on both *n*- and *p*-Ge.

The devices reveal a dark current density of ~47 mA/cm$^2$ at a reverse bias of 1 V (i.e. -1 V), independent of their *n*-mesa diameter. This indicates a minimal device surface leakage and a good quality of the $SiO_2$ passivation. Temperature-dependent current-voltage measurement exhibits an activation energy of 0.336 eV on the dark current, implying its origin from the mid-gap states in the material. Significant photocurrent

was observed under the optical illumination via a normal-incident fiber. A responsivity of 0.39 A/W was obtained at 1550 nm. The dark current density and responsivity are superior to that of the existing GOI photodetectors, due to the adoption of the vertical *p*-*i*-*n* structure for an increased absorption thickness. The performance are also comparable with that of the reported Ge photodetectors with similar *i*-Ge thicknesses. The responsivity is expected to reach ~ 0.51 A/W by adding an anti-reflection coating, with an IQE of ~ 97%. The responsivity spectrum across the *C*- and *L*-bands reveals two tiny peaks at ~ 1570 and ~ 1590 nm, agreeing well with the *Γ*-HH and *Γ*-LH bandgap edges, respectively, estimated from the deformation potential theory. The detector (with its *n*-mesa diameter of 60 μm) owns a 3dB-bandwidth of ~ 1 GHz, which is dominated by the device RC delay. The 3dB-bandwidth is expected to reach ~ 32 GHz by minimizing the contact series resistance and *n*-mesa diameter to 30 Ω and 10 μm, respectively. This work could facilitate high-performance optical transceivers and LiDAR systems using GOI, to potentially integrate with Ge CMOS electronics and mid-infrared photonics for sensing and communication at a broad spectrum range. The device design is also compatible with other “on-insulator” platforms with different combination of semiconductor and intermediate insulator materials.

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# Chapter 6 Uniformly Tensile-strained Ge Enabled by a Recessed $SiN_x$ Stressor at Sidewalls

As discussed in Chapter 1.2 and 2.1, a wider absorption coverage for the Ge photodetectors would benefit a wider WDM bandwidth catering for the increasing demand for the short-reach data communication. On the other hand, the bonding and layer transfer method via etch-back provides an enabling solution to efficiently integrate a layer of high-quality Ge at the BEOL useful for such applications. Furthermore, in Chapter 3.3, inducing an additional tensile strain in Ge via a $SiN_x$ stressor has been discussed as a viable and CMOS-compatible approach to achieve an absorption extension towards longer wavelengths, due to the strain-induced absorption coefficient enhancement (Chapter 3.4). However, spatial non-uniformity exists in the resulting Ge strain profile, if adopting the stressor without Ge detachment from the substrate. The strain inhomogeneity would lead to a spatial variation in the electronic bandgap and consequently the absorption coefficient that could limit the QE of the photodetectors, especially at longer wavelengths close to the bandgap edge. Therefore, in this chapter, efforts will be made to realize a uniformly tensile-strained Ge waveguide-on-insulator (WGOI) by a recessed tensile-stressed $SiN_x$ stressor placed at the waveguide sidewalls. The recessed trenches were realized experimentally by a simple self-aligned dry etching (SADE) into the $SiO_2$ layer beneath Ge, together with the Ge waveguide patterning. The enhancement on the strain uniformity was both observed from the theoretical finite element method (FEM) modelling

and experimental micro-Raman measurements, compared to the $SiN_x$-strained waveguide without SADE. This work paves the way towards a higher-efficiency integrated Ge photodetector at longer wavelengths.

The chapter will start with a thermal-mechanical modelling on the strain profile in the Ge WGOI by FEM in Chapter 6.1. Comparative study will be carried out on the strain profile with respect to the placement of the $SiN_x$ stressors. The deposition of a highly-stressed $SiN_x$ film will be discussed in Chapter 6.2. Chapter 6.3 will attempt to experimentally realize the $SiN_x$-strained Ge WGOI. Characterization on the strain uniformity will be performed by micro-Raman measurements at different laser wavelengths. Chapter 6.4 will conclude the work in this chapter.

# 6.1 Strain Modelling in Ge Waveguide-on-insulator (WGOI)

## 6.1.1 Before the Placement of $SiN_x$ Stressor

COMSOL Multiphysics was utilized for the FEM modelling. The modelling started with building a GOI layer stack similar to that reported earlier [1, 2], with $SiO_2$ as the intermediate insulator. Considering the thermal and mechanical effect on the structure, the solid mechanics module was employed. The thicknesses of the Ge and $SiO_2$ are 400 and 700nm, respectively. The model followed the thermal budget during the GOI fabrication consisting of the Ge-on-Si epitaxy at 600$^oC$ and post-bonding annealing at 300$^oC$, before cooling down to room temperature. Each of the physics mechanism corresponds to a solid mechanics module

where the stress output from the previous module was imported as the initial stress for the subsequent module. Geometrical symmetry was applied penetrating the structure via the *y*-*z* and *x*-*z* planes as indicated in Fig. 52. The ultimate stress obtained in the Ge film-on-insulator was then converted to strain via below relations:

$$\varepsilon_{xx} = \frac{\sigma_{xx} - \nu \bullet (\sigma_{yy} + \sigma_{zz})}{E} \tag{6.1}$$

$$\varepsilon_{yy} = \frac{\sigma_{yy} - \nu \bullet (\sigma_{xx} + \sigma_{zz})}{E} \tag{6.2}$$

$$\varepsilon_{zz} = \frac{\sigma_{zz} - \nu \bullet (\sigma_{xx} + \sigma_{yy})}{E} \tag{6.3}$$

where $\varepsilon_{xx}$, $\varepsilon_{yy}$ and $\varepsilon_{zz}$ are the strain along the *x*-, *y*- and *z*-directions, respectively. $\sigma_{xx}$, $\sigma_{yy}$ and $\sigma_{zz}$ are the corresponding mechanical stress values. $\nu$=0.273 and $E$=103 GPa are the Poisson's ratio and Young's modulus of Ge, respectively. Since the stress is only within the *x*-*y* plane, $\sigma_{zz}$=0. Fig. 52 shows the in-plane biaxial strain profile in the Ge film-on-insulator. The tensile strain ($\varepsilon_{xx}$=$\varepsilon_{yy}$) is ~0.16%, which matches well with the HRXRD and micro-Raman results in Chapter 4.3.3, indicating the accuracy of the model.

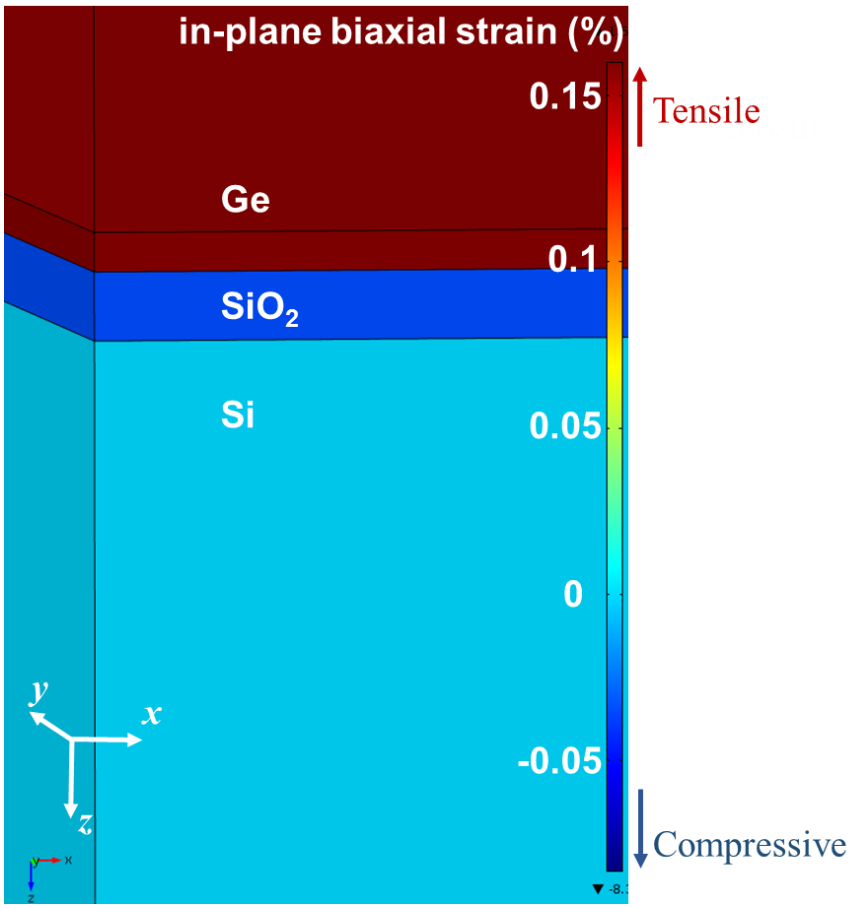


Figure 52 In-plane biaxial strain profile in the Ge film-on-insulator.

Afterwards, the Ge film was patterned into waveguides to facilitate the strain enhancement from the $SiN_x$ stressor. This arrangement is necessary because the FEM modelling for a $SiN_x$ stressor placed on the Ge film does not reveal a significant change on the Ge strain (data not shown). The waveguide was defined along <100> direction, with its longitudinal dimension (100 µm, along *y*-direction) much longer than its transverse dimension (2 µm, along *x*-direction). This was realized by adding a new solid mechanics module behind and excluding the portion of the Ge outside the waveguide, with the temperature kept constant at 300 K. The same plane symmetry applies as above, with the *y*-*z* and *x*-*z* plane longitudinally and transversely penetrating the center of the

waveguide, respectively. Fig. 53 shows the corresponding strain profiles. The longitudinal strain ($\varepsilon_{yy}$, in Fig. 53 (a)) reveals a negligible change compared to that in the Ge film-on-insulator (Fig. 52); while the transverse strain ($\varepsilon_{xx}$, in Fig. 53 (b)) exhibits a certain extent of relaxation. The strain value close to the waveguide sidewall even becomes compressive (~ -0.03%). This might be due to the shrinkage of the contact area to the on-insulator substrate along the transverse (*x*-) direction, resulting from the waveguide patterning. The reduced contact area relieved the substrate constraint on the Ge waveguide and thus relaxes its strain. This explanation also fits well for the negligible change of the $\varepsilon_{yy}$, where the Ge is still in full contact to the substrate. Therefore, the original in-plane biaxial strain changes to a uniaxial-like tensile strain exerting along the longitudinal direction. The transverse compressive strain above is thus likely to be induced, due to the Poisson effect. However, it is also the residual contact along the transverse direction that retains the slight tensile strain (~ 0.1%) close to the bottom of the waveguide.

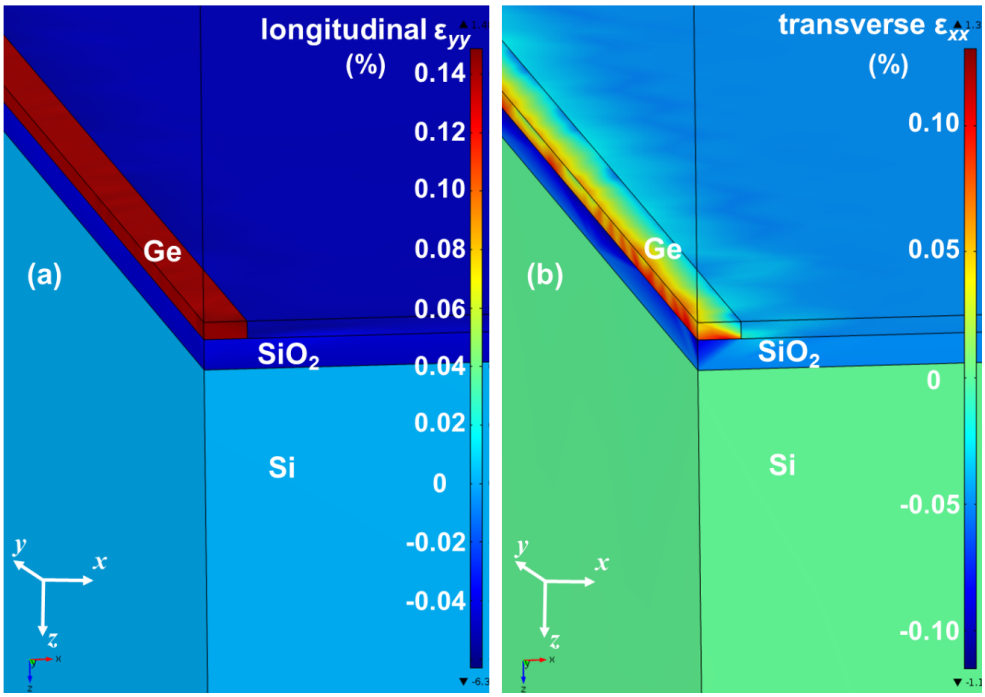


Figure 53 Strain profiles in a Ge strip WGOI along the (a) longitudinal ($\varepsilon_{yy}$) and (b) transverse ($\varepsilon_{xx}$) directions.

## 6.1.2 With $SiN_x$ Stressor

### 6.1.2.1 How to Place the $SiN_x$ Stressor for a Uniform Tensile Strain?

As discussed in Chapter 3.3.3, the use of $SiN_x$ stressor to induce the tensile strain in Ge has the advantage of CMOS-compatibility but suffers from the spatial non-uniformity in the resultant strain profile, if a suspended or pedestal Ge structure is not considered, for the feasibility of integration and packaging. This has been revealed from the strain modeling in several papers. For example, as shown in Fig. 54 (a), placing a ~2.5 GPa compressive $SiN_x$ stressor on top of a Ge waveguide generated a spatially uneven strain profile, with the bottom edge corners turning compressive, which negated the original intention for tensile strain. Extending the stressor to the waveguide sidewalls (Fig. 54 (b))

would only slightly alleviate the issue and the strain remains non-uniform near the substrate. This is due to the direct contact of Ge to the substrate layers that hinders its elastic deformation close to the substrate under the tensile strain. Therefore, the same authors in Ref. [3] alternatively attempted to strain a Ge pedestal waveguide to minimize the substrate constraint. However, this would additionally lead to integration challenges such as thermal dissipation and the inevitable use of wet chemical etching.

Therefore, in this section, we will introduce a novel and straightforward method to enhance the strain uniformity in Ge, by creating trenches into the substrate layers at both sides of the Ge waveguide together with the Ge waveguide patterning, followed by the conformal deposition of the $SiN_x$ stressor. This method could thus strain the substrate, together with the Ge waveguide, via their sidewall contact to the $SiN_x$ stressor. Meanwhile, the method does not complicate the device fabrication and integration, as the substrate trenches share the same hard mask for the Ge waveguide patterning and the Ge waveguide thus remains in full contact with the substrate.

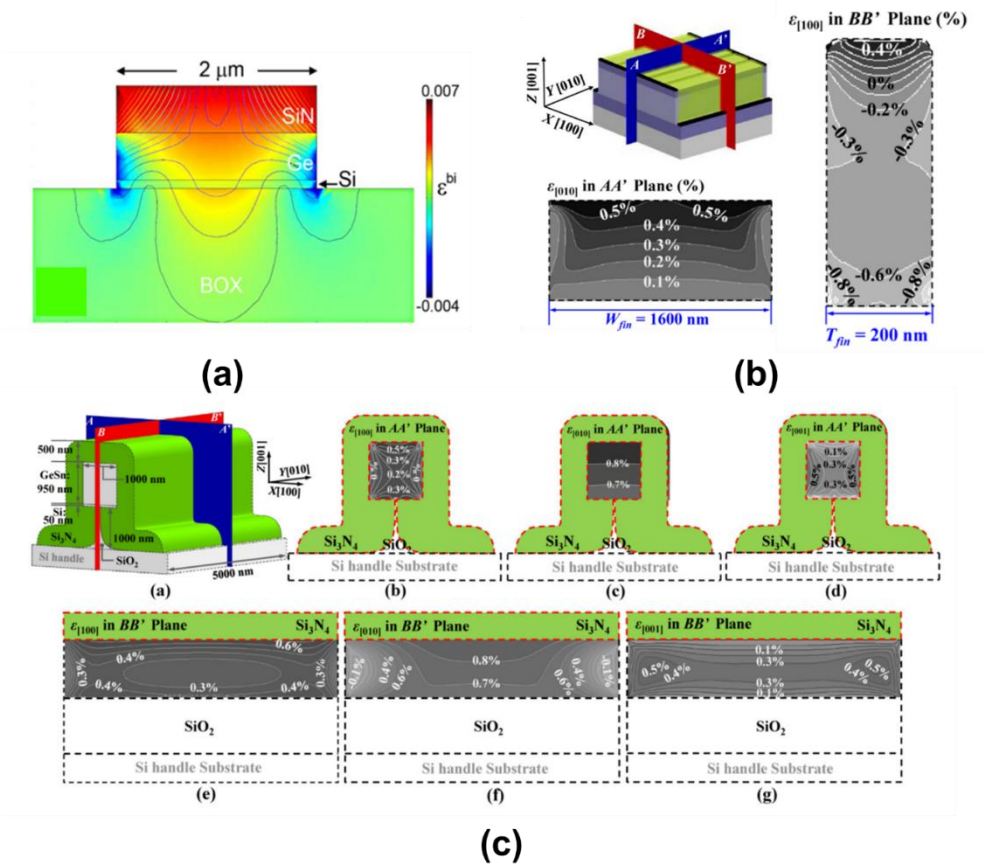


Figure 54 (a) Ge biaxial strain profile from a top compressive $SiN_x$ stressor [4]; Strain contour plots of GeSn fins with $SiN_x$ liner stressor (b) without [5, 6] and (c) with [3] the substrate undercut.

### 6.1.2.2 Strain Profile Comparison: Top, Sidewall and Recessed Sidewall $SiN_x$ Stressors

Based on the model built in Chapter 6.1.1, $SiN_x$ stressor with an intrinsic tensile stress of 1GPa was added into a new solid mechanics module following the one used for Ge waveguide patterning. The value of 1GPa has been commonly adopted in conventional strained-Si technology [7, 8]. The width and height of the Ge waveguide were reduced to 500 and 200 nm, respectively, for the demonstration of a prominent strain effect. The $SiN_x$ stressor was placed via a sidewall contact to the Ge waveguide, with its thickness identical to the waveguide height. The Young's modulus used for $SiN_x$ is 200 GPa. The temperature

was also kept constant at 300 K throughout the module, since only the initial and final temperature during the $SiN_x$ deposition are of interest for the strain calculation, which were both at room temperature. All the remaining settings in the model were identical to that described in Chapter 6.1.1. To model the substrate trenches, the Ge waveguide sidewalls were extended 200 nm deeper into the bottom $SiO_2$ layer. The trenches were similarly filled with the $SiN_x$ stressor up to the top of the Ge waveguide. In addition, a Ge WGOI tensile-strained by a top compressive $SiN_x$ stressor was also modelled for a comparison. The structural parameters remain identical to the sidewall-stressor models. The top $SiN_x$ is also ~200 nm thick and with a ~1 GPa compressive stress.

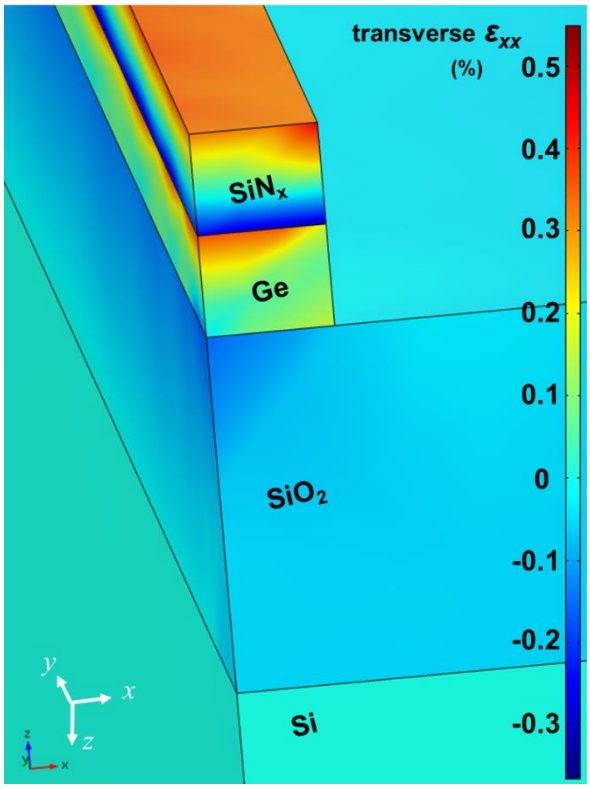


Figure 55 Transverse strain ($\varepsilon_{xx}$) profile of Ge WGOI with a top compressive $SiN_x$ stressor (1GPa).

Fig. 55 depicts the $\varepsilon_{xx}$ profile of the Ge WGOI. The top $SiN_x$ stressor is only effective on the top portion of the Ge waveguide, leaving most of the waveguide unevenly- and insufficiently-strained. As a result, depositing the $SiN_x$ at the Ge waveguide sidewalls was considered to enhance the stressor effect. Fig. 56 (a) and (b) show the structural schematics for the models employing the sidewall $SiN_x$ stressor without and with the trenches into the bottom $SiO_2$, respectively. The corresponding $\varepsilon_{xx}$ profiles in the Ge waveguide are shown in Fig. 56 (c) and (d), respectively. The use of the stressor at the waveguide sidewalls significantly increases the tensile strain as well as its uniformity in Ge, compared to that at the waveguide top. It can be further observed that the strain profile with the substrate trenches exhibits a deeper and more uniform color code, compared to that without the trenches. This implies an enhancement in both the magnitude and uniformity of the strain in the Ge waveguide. A closer observation indicates that the strain enhancement mainly occurs close to the bottom of the waveguide. This is attributed to the enhanced tensile strain in the underlying $SiO_2$ waveguide by the sidewall contact to the $SiN_x$ stressor, which can be told from its yellow-greenish color code (Fig. 56 (b)) turning from blue (Fig. 56 (a)). The sidewall stressor at both sides pulls the $SiO_2$ oppositely along the transverse *x*-direction, leading to the enhancement of $\varepsilon_{xx}$ in the top Ge waveguide close to the $SiO_2$ interface and consequently the overall strain uniformity. On the other hand, the $\varepsilon_{yy}$ reveals a negligible change (at ~ 0.17%), irrespective of the adoption of the substrate trenches, as seen

from the insets in Fig. 56 (c) and (d). This observation can also be explained by the substrate constraint as discussed earlier.

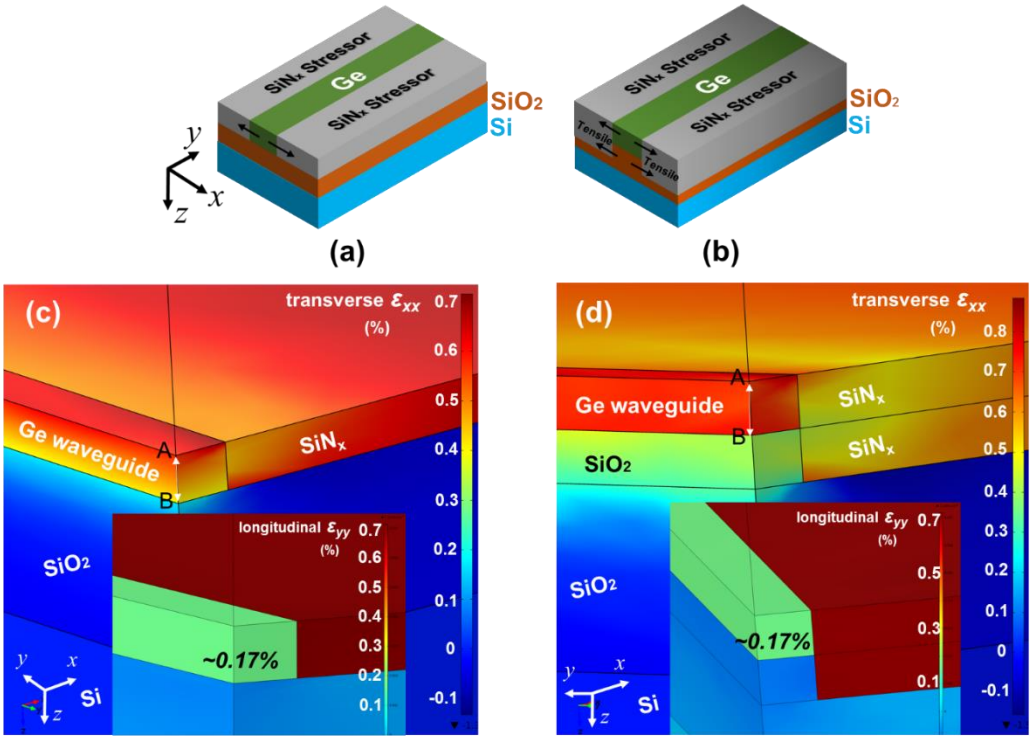


Figure 56 3-D schematic diagrams of tensile-straining a Ge waveguide-on-insulator via sidewall $SiN_x$ stressor (a) without and (b) with the trenches along the waveguide sidewalls into the bottom $SiO_2$. The corresponding transverse strain profiles ($\varepsilon_{xx}$) in the Ge waveguide were shown in (c) and (d), respectively. The insets in (c) and (d) denote the longitudinal strain profiles ($\varepsilon_{yy}$) from the respective models.

To quantitatively study the enhancement in tensile strain as well as its uniformity improvement, the $\varepsilon_{xx}$, along the point A to B as indicated in Fig. 56 (c) and (d), were extracted and plotted in Fig. 57. The plot clearly shows a significant strain enhancement throughout the Ge waveguide, with the help of the sidewall $SiN_x$ stressor straining the underlying $SiO_2$ layer via the recessed trenches. A ~ 2× increase in the Ge tensile strain was found, close to the Ge/$SiO_2$ interface. In addition, the standard deviation of the strain profile reduced from ~ 0.06 to ~ 0.02% accordingly, indicating a ~ 67% improvement in the strain uniformity.

Therefore, the modelling indicates that the sidewall $SiN_x$ stressor is superior to the top stressor in terms of its strain magnitude and uniformity. A further enhancement was also subsequently demonstrated, by adopting the recessed stressor with substrate trenches at both sides of the waveguide. This simple and CMOS-compatible method is expected to facilitate an integrated Ge photodetector with a higher efficiency at longer wavelengths. Besides, an *in-situ* tuning of the Ge strain could be realized, via the engineering of the waveguide structural parameters, without the need to change the $SiN_x$ stress. The study on the effect of these parameters will be discussed in Chapter 7.5.

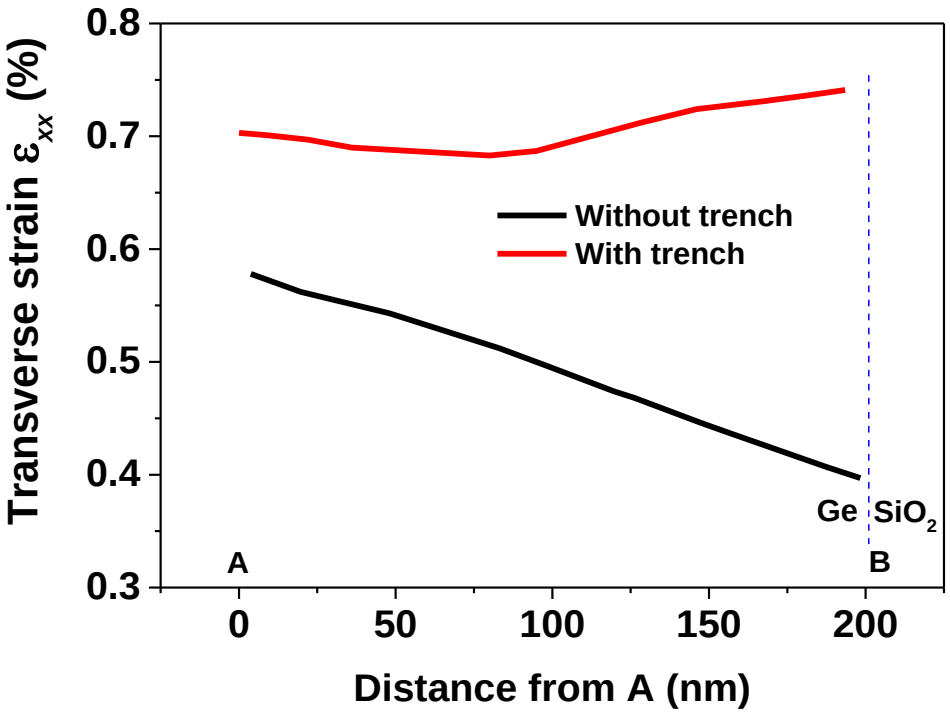


Figure 57 (a) Transverse strain ($\varepsilon_{xx}$) profiles in the Ge waveguide from A to B (in Figure 56 (c) and (d)), with respect to the use of the substrate trenches.

## 6.2 Deposition of Highly-stressed $SiN_x$

### 6.2.1 Tensile-stressed $SiN_x$ Deposition

As modelled in Chapter 6.1.2, depositing a highly tensile-stressed $SiN_x$ film is critical for a prominent tensile strain in the Ge waveguide. Following the background knowledge discussed in Chapter 3.5, a Cello Aegis-20 PECVD system was utilized for the deposition of the highly-tensile $SiN_x$, at the RF frequency of 13.56 MHz. The deposition parameters were targeted accordingly for a low RF power, high chamber pressure and low $SiH_4/NH_3$ ratio. The depositions were initially performed on 150-mm Si (111) wafers to acquire the intrinsic stress values in the $SiN_x$ film. It is assumed that an identical deposition on the Ge WGOI structure would generate the identical stress. All wafers were RCA-cleaned followed by a diluted HF (1:10) dip before the deposition. The intrinsic stress can be calculated using the Stoney's equation, as expressed below:

$$\sigma = \frac{B{t_s}^2}{6t_f}\left(\frac{1}{r_a} - \frac{1}{r_b}\right) \tag{6.4}$$

where $B = \frac{E}{1-\nu}$ is the biaxial modulus of Si. $E$ and $\nu$ are the Young's modulus (160 GPa) and Poisson's ratio (0.27) of Si, respectively. $t_s$ and $t_f$ are the thickness of the Si wafer and $SiN_x$ layer, respectively. $r_a$ and $r_b$ are the radius of curvature for the wafers before and after the $SiN_x$ deposition, respectively. The film thickness was measured by a Filmetrics F20 film thickness measurement system, while the wafer curvatures were measured both before and after the $SiN_x$ deposition, using a KLA-Tencor

FLX-2320 stress measurement system. The parameters used in three of the PECVD depositions, together with their calculated $SiN_x$ stress, are tabulated in Table 2. It can be found that the $SiN_x$ stress increases from compressive (-307 MPa) to tensile (750 MPa) by increasing the chamber pressure and decreasing the $SiH_4/NH_3$ ratio as well as the RF power, which agrees well with the trends as summarized in Table 1. However, due to the limitation of the PECVD system such as the maximum-allowable gas flow rate and chamber pressure, the resulting $SiN_x$ stress is hindered for a further increase. Therefore, alternative solutions are needed for a further enhancement of the tensile stress in the PECVD-deposited $SiN_x$.

Table 3 Deposition parameters utilized in three of the PECVD runs and their resulting $SiN_x$ stress. The negative stress value indicates a compressive stress while the positive denotes a tensile stress.

| S/N | Temperature (°C) | $SiH_4/NH_3$ Ratio | RF power (W) | Chamber Pressure (mT) | Film thickness (nm) | Stress (MPa) |
|---|---|---|---|---|---|---|
| 1 | 300 | 0.2 | 500 | 500 | 291 | -307 |
| 2 | 300 | 0.1 | 100 | 1000 | 183 | 301 |
| 3 | 300 | 0.025 | 50 | 1500 | 281 | 750 |

## 6.2.2 Stress Enhancement via Furnace Annealing

As suggested in Chapter 3.5, annealing at an elevated temperature would help desorbing the bonded hydrogen in the PECVD-deposited $SiN_x$ film and consequently increasing the film stress. Hence, the as-deposited wafers were furnace-annealed in $N_2$ ambient to study the effect of thermal annealing on the $SiN_x$ stress. Fig. 58 (a) summarizes the development of

$SiN_x$ stress as well as the furnace temperature profile as a function of the process time. The wafers were annealed at 850°C for 4 hrs. The time at 0 denotes the moment the wafers have been loaded and the annealing process started. The temperature, started from idle (425°C), was ramped up at a rate of ~ 14°C/min and cooled down naturally to room temperature after the annealing. A substantial increase by more than two times was observed on the film stress. However, inspection under optical microscope reveals that the wafer surface is heavily cracked, as shown in Fig. 58 (b). This might suggest that the desorption of the bonded hydrogen works faster than the re-configuration of the dangling Si- and N-bonds, which caused the film fracture. Therefore, a lower annealing temperature with a gentler ramping rate might be required to slow down the hydrogen desorption and result in a crack-free film.

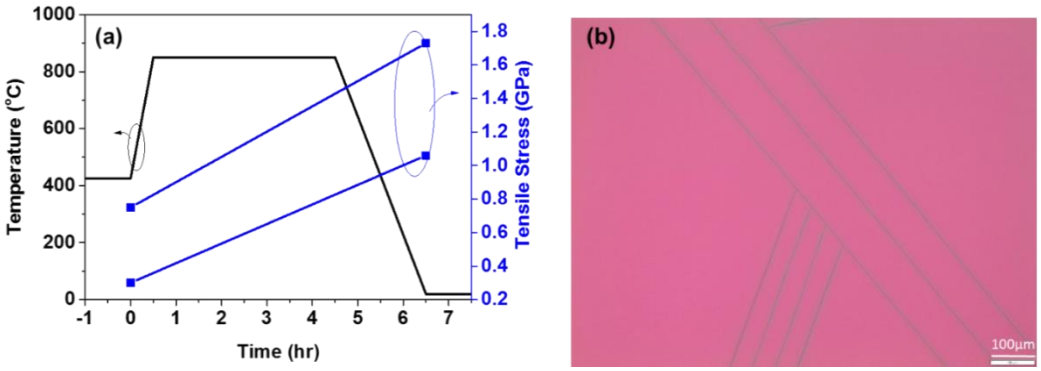


Figure 58 (a) Temperature profile (850°C for 4hrs) of the furnace annealing as a function of process time, with the $SiN_x$ stress indicated before and after the annealing; (b) an optical microscope image of the wafer surface after the annealing.

Fig. 59 (a) plots the development of the $SiN_x$ stress with a gentler temperature profile during the furnace annealing. The annealing was divided into phases, starting with an idle temperature at 300°C to match with the PECVD temperature. The maximal temperature in each phase

increased in steps, by 50°C per step till 550°C. To demonstrate the development of the $SiN_x$ stress, the wafer was unloaded intermediately after each phase, namely cooling down to room temperature, to measure its curvature. It can be found that a tensile stress of ~1 GPa can be achieved after the annealing, without any crack observed in the film (Fig. 59 (b)). This verifies that a gentler annealing profile with a lower temperature and longer annealing time contributes to the crack elimination, possibly due to the slower desorption rate of the bonded hydrogen. It can be further inferred from the study that the annealing duration is more dominant, compared to the annealing temperature, for the stress enhancement. This is because the tensile stress enhancement is insignificant after the annealing at 450°C, where a tensile stress of ~0.9 GPa has been reached. Moreover, the stress keeps increasing in the initial 3 annealing phases all at 380°C. Therefore, it can be suggested that a high-temperature annealing might not be required for a prominent $SiN_x$ stress improvement, although the maximal achievable $SiN_x$ stress is compromised, which is in accordance with the need for a low thermal budget for the BEOL application. A crack-free film can also be expected for a consecutive annealing without the intermediate cooling-down cycles.

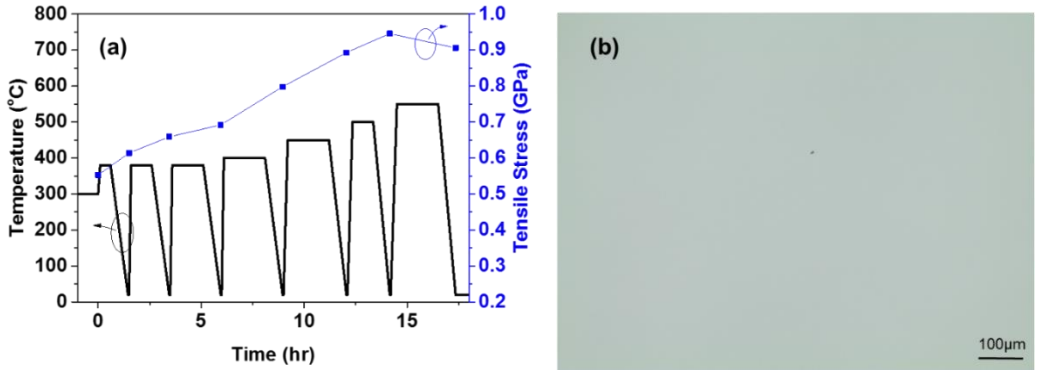


Figure 59 (a) Development of $SiN_x$ stress as a function of the process time with a gentler annealing profile; (b) a corresponding optical microscope image of the wafer surface after annealing. The particle at the center indicates that the image is focused.

## 6.2.3 Compressively-stressed $SiN_x$ Deposition

For a higher-efficiency Ge photodetector at longer wavelengths, a maximally tensile-stressed $SiN_x$ stressor at the waveguide sidewalls is more than sufficient for an extreme Ge bandgap shrinkage and consequently for a longest absorption coverage. However, for a Ge electro-absorption (EA) modulator, both the tensile- and compressively-stressed $SiN_x$ are desired to induce a considerable tensile and compressive strain in the Ge waveguide, respectively. This would facilitate a broadband tuning of the Ge absorption edge, where the Franz-Keldysh effect (Chapter 3.3.1) could take place. Therefore, in this section, deposition of highly-compressive $SiN_x$ was also developed. Together with the highly-tensile $SiN_x$ studied above, a broadband Ge EA modulator can be envisioned.

Based on the literature survey in Chapter 3.5, the RF frequency of 380 kHz was utilized, together with a high RF power, low chamber pressure and low total $SiH_4$+$NH_3$ flow. Table 3 summarizes the used

deposition parameters as well as the resulting $SiN_x$ stress in five PECVD runs aiming for a highly-compressive film.

Table 4 Deposition parameters as well as the resulting $SiN_x$ stress in PECVD runs for a highly-compressive film. The negative value indicates a compressive stress.

| S/N | Temperature (°C) | $SiH_4$ flow (sccm) | $NH_3$ flow (sccm) | RF power (W) | Chamber Pressure (mT) | Film thickness (nm) | Stress (MPa) |
|---|---|---|---|---|---|---|---|
| 1 | 300 | 55 | 145 | 200 | 300 | 343 | -216 |
| 2 | 300 | 25 | 70 | 400 | 270 | 1322 | -477 |
| 3 | 300 | 20 | 50 | 400 | 300 | 494 | -792 |
| 4 | 300 | 10 | 50 | 400 | 270 | 273 | -883 |
| 5 | 300 | 5 | 25 | 400 | 250 | 406 | -1040 |

The compressive stress increases dramatically, following well with the trends in Table 1. A ~ 1 GPa compressive stress can thus be achieved. The further enhancement of the stress is under investigation, using the recommended methods such as multi-layer deposition with surface plasma treatment among each layers (Chapter 3.5).

## 6.2.4 Conclusion

In Chapter 6.2, efforts have been made for the development towards a highly-tensile and -compressive $SiN_x$ films. A maximal ~ 750 MPa tensile stress and ~ 1 GPa compressive stress have been achieved in the as-deposited films. Furnace annealing at 850°C for 4 hrs could remarkably improve the tensile stress by ~3 times, but adversely causes the film fracture. An optimized annealing profile with a lower temperature gradient and longer annealing time could effectively eliminate the crack

formation, with the ultimate film stress close to ~ 1 GPa. The tensile $SiN_x$ itself could potentially benefit a longer-wavelength Ge photodetector, while both the tensile and compressive $SiN_x$ could facilitate a broadband Ge EA modulator. Both the devices are envisioned to widen the working bandwidth of the photonic-integrated circuits utilizing the WDM scheme, which would cater for the increasing demand of data communication.

## 6.3 Fabrication and Characterization of $SiN_x$-strained Ge WGOI

In this section, based on the structure developed in the thermal-mechanical modelling in Chapter 6.1, along with the optimized PECVD process for the highly-stressed $SiN_x$ deposition in Chapter 6.2, tensile $SiN_x$-strained Ge WGOI will be experimentally realized. Chapter 6.3.1 will discuss the fabrication of the $SiN_x$-strained Ge WGOI. The characterization of the fabricated waveguides will be discussed in Chapter 6.3.2. Chapter 6.3.3 will conclude this section.

### 6.3.1 Fabrication of $SiN_x$-strained Ge WGOI via Self-aligned Dry Etching (SADE)

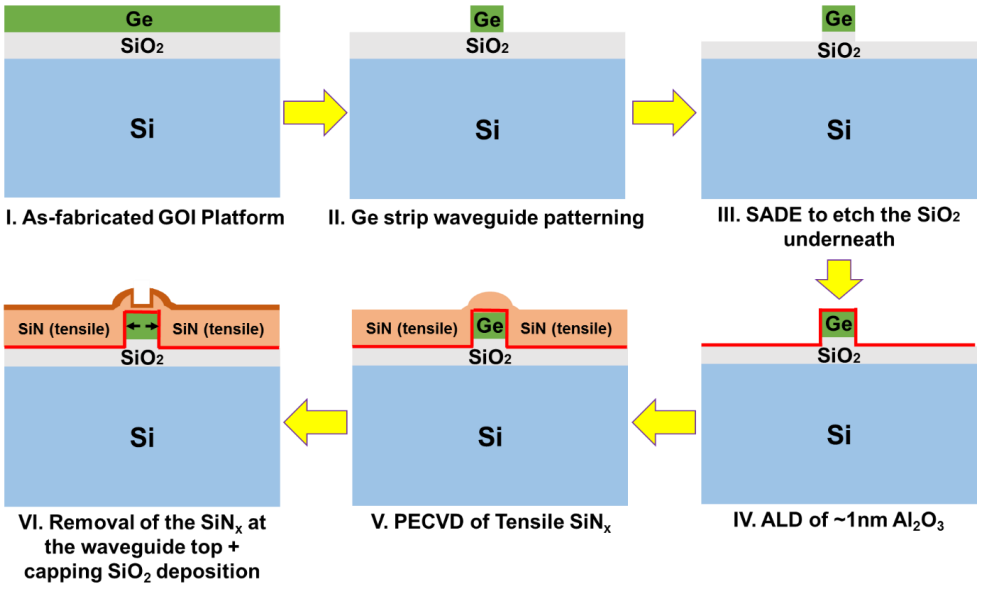


Figure 60 Schematic diagrams of the process flow for the $SiN_x$-strained Ge WGOI fabrication, employing the SADE method.

The fabrication of the $SiN_x$-strained waveguide was carried out following the schematic as shown in Fig. 60. First, the as-fabricated GOI platform (Chapter 4.1, without implantation steps) was patterned into strip waveguides, using either optical lithography (OL) or electron-beam lithography (EBL) depending on the feature size of the waveguide. A $Cl_2$-based RIE was followed subsequently to form the waveguide. By switching to carbon tetrafluoride ($CF_4$)-based gases, the RIE was continued to further etch ~500nm into the $SiO_2$ layer underneath, utilizing the same resist (AZ5214E (OL) or ZEP520A (EBL)) hard mask in patterning the Ge WGOI. This RIE step is thus self-aligned with the previous RIE for the Ge WGOI patterning and is consequently termed as the self-aligned dry etching (SADE). After the hard mask removal by $O_2$ plasma ashing, the sample was dipped in buffered oxide etchant (6:1) to remove the residual surface oxides and organics. Immediately after, a layer of ~1nm aluminium oxide ($Al_2O_3$) was deposited via atomic layer

deposition (ALD) at 250°C. The $SiN_x$ film with a tensile stress of ~ 580 MPa was then deposited by PECVD to fully bury the waveguides. The tensile stress was calculated using the Stoney's equation from the change of the wafer warpage before and after an identical deposition on a bare Si wafer, as discussed in Chapter 6.2.1. After the deposition, a second EBL patterning was performed, followed by the $CF_4$-based RIE to remove the $SiN_x$ layer at the waveguide top, since the tensile $SiN_x$ at the top would induce an undesired compressive strain to the Ge underneath (the corresponding experimental demonstration will be in Chapter 6.3.3.1). The $CF_4$-based RIE stopped when the residual $SiN_x$ was ~ 50 nm, after which a sulfur hexafluoride ($SF_6$)-based RIE was taken over to complete the $SiN_x$ removal. The etching was implemented with a low RF power and high chamber pressure to alleviate the ion-bombardment damage on the $Al_2O_3$ surface. The high etching selectivity between the $SiN_x$ and $Al_2O_3$ [9] makes the ~ 1 nm $Al_2O_3$ as an etch-stop layer to protect the Ge underneath. Alternatively, CMP could also be used to remove the top $SiN_x$. Finally, the samples were capped with a ~ 200 nm $SiO_2$ by PECVD to avoid the moisture-induced stressor delamination from the waveguide sidewalls (the detailed study will be in Chapter 6.3.3.2). As a comparison, Ge WGOIs without using SADE were also prepared, by skipping Step III as shown in Fig. 60.

Fig. 61 (a), (b) and (c) are tilted SEM images of the $SiN_x$-strained Ge WGOI at steps II, V and VI in Fig. 60, respectively. Fig. 61 (d) is an optical microscope image of the fabricated WGOI.

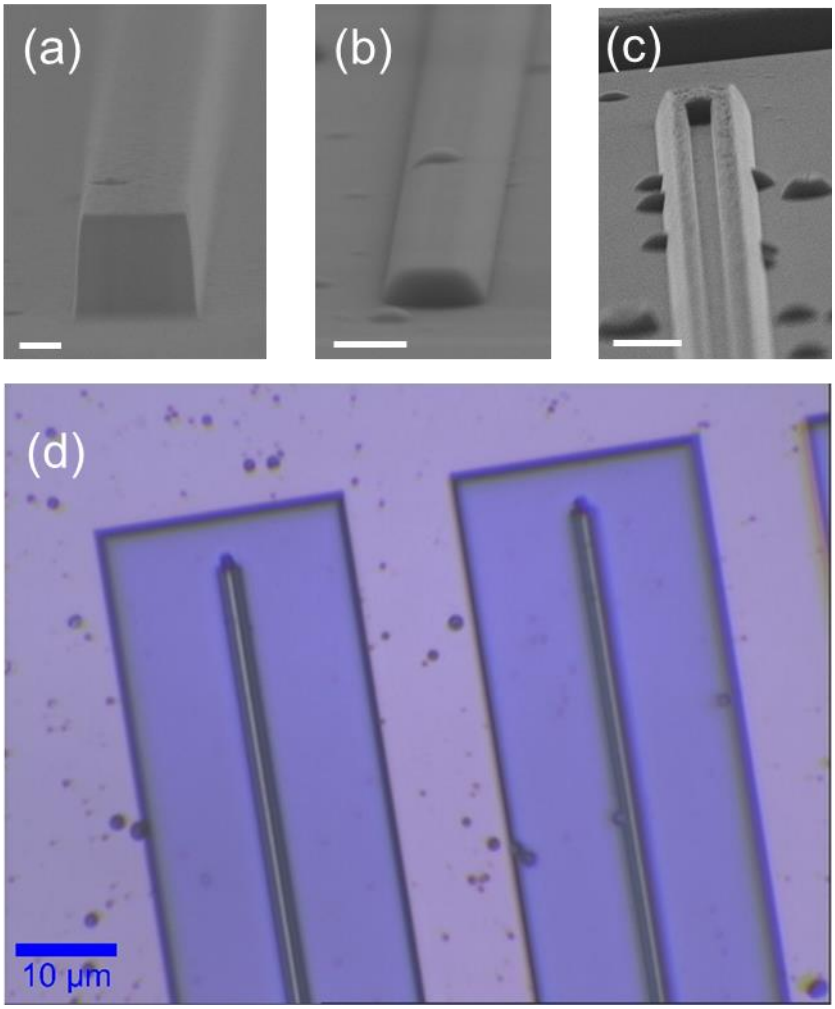


Figure 61 SEM images of the $SiN_x$-strained Ge WGOI fabrication at the steps of (a) II. Ge strip waveguide patterning, (b) V. PECVD of tensile $SiN_x$ and (c) VI. Removal of the top $SiN_x$. The scale bars are 200 nm in (a) and 1µm in (b) and (c). An optical microscope image of the fabricated waveguide is shown in (d).

## 6.3.2 Characterization of $SiN_x$-strained Ge WGOI

To characterize the fabricated waveguide, apart from the optical microscope and SEM inspections, focused ion beam (FIB) technique was utilized to reveal the cross-sectional profile at the waveguide region. In addition, micro-Raman measurement was performed to characterize the magnitude and uniformity of the tensile strain in Ge, via the shift and the full-width-at-half-maximum (FWHM) of its longitudinal optical (LO) phonon peak, respectively. The commercial micro-Raman spectroscopy is with a

confocal backscattering configuration. The backscattered laser signal from the sample went through the confocal microscope followed by a spectrometer and was finally collected by the CCD detectors to form a Raman spectrum. The numerical aperture and magnification of the confocal objective lens are 0.9 and 100×, respectively. Lasers with emitting wavelengths of 532 and 785 nm were used for the measurement. The output power of the lasers were set to have negligible effect on the Raman spectra.

### 6.3.2.1 Ge WGOI without $SiN_x$ Stressor

First, Ge WGOI without the $SiN_x$ stressor was fabricated using the optical lithography and then characterized. The waveguide dimensions (~ 2 μm in width, ~ 100 μm in length and ~ 400 nm in thickness) are identical to those modelled in Chapter 6.1.1. Micro-Raman measurement was then performed at a laser wavelength of 785 nm. Fig. 62 (a) and (b) show an optical microscope image and the corresponding micro-Raman spectrum of the fabricated waveguide, respectively. It can be clearly seen that the Raman peak of the Ge WGOI resides in between that of the bulk Ge and Ge film-on-insulator, which agrees well with the transverse strain relaxation found in the FEM modelling that would halve the blue-shift of the Raman peak. Since $\sigma_{zz}$=0, by summing the Eqn. (6.1) and (6.2), one could get the following equation:

$$\varepsilon_{xx} + \varepsilon_{yy} = \frac{(1-\nu)(\sigma_{xx}+\sigma_{yy})}{E} \tag{6.4}$$

where $\varepsilon_{xx}$ and $\varepsilon_{yy}$, as discussed previously, correspond to the transverse and longitudinal strain in the Ge waveguide, respectively. The term

$(\sigma_{xx} + \sigma_{yy})$, referring to the total in-plane stress, can be deduced from Eq. (4.1). By keeping $\varepsilon_{yy}$ as ~ 0.17% (Fig. 56 (c) and (d)), the $\varepsilon_{xx}$ can then be determined as ~ 0.04% tensile. Considering the laser spot diameter of ~ 1 µm in the micro-Raman system, the $\varepsilon_{xx}$ value reasonably matches with the modelling data (Fig. 53 (b)) near the centre of the waveguide along the transverse direction, which further verifies the accuracy of the model.

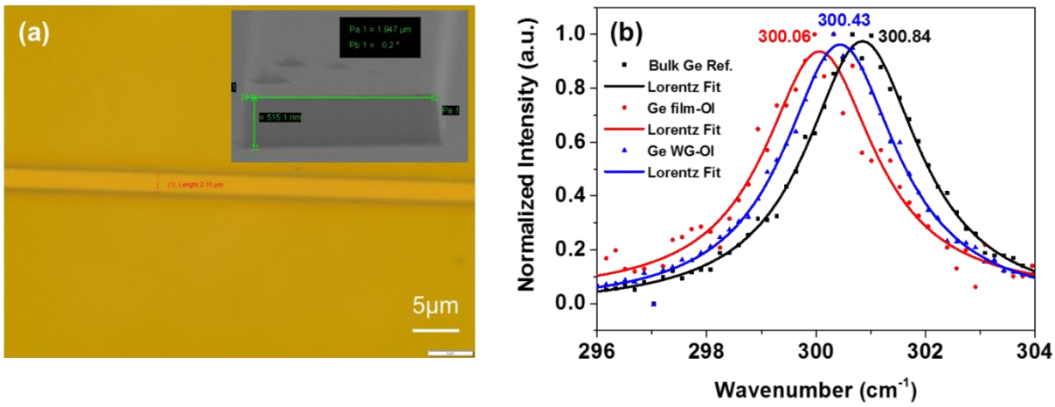


Figure 62 (a) An optical microscope image of the fabricated Ge waveguide-on-insulator, with its width measured as 2.15 µm. The inset shows a corresponding tilted SEM image with the thickness measured as 515 nm; (b) Micro-Raman spectrum of the fabricated waveguide, with the spectra of bulk Ge and Ge film-on-insulator as a reference.

### 6.3.2.2 Effect of SADE on Ge Strain

Fig. 63 (a) shows a top-view SEM image of the fabricated $SiN_x$-strained Ge WGOI with a width of 1 µm. The waveguide sidewalls were fully buried by the $SiN_x$ stressor. The two protruded lines are the residual $SiN_x$ at the waveguide top after the $SiN_x$ removal (step VI in Fig. 60). The corresponding SEM images prepared by FIB, for the waveguide without and with the use of the SADE, are shown in Fig. 63 (b) and (c), respectively. For a more legible comparison, both the images only exhibited the right-half of the waveguide from the centre. The Ge layer is ~ 100 nm thick for the ease of the subsequent micro-Raman

characterizations. The SADE-induced trench depth is ~ 460 nm into the underlying $SiO_2$ layer.

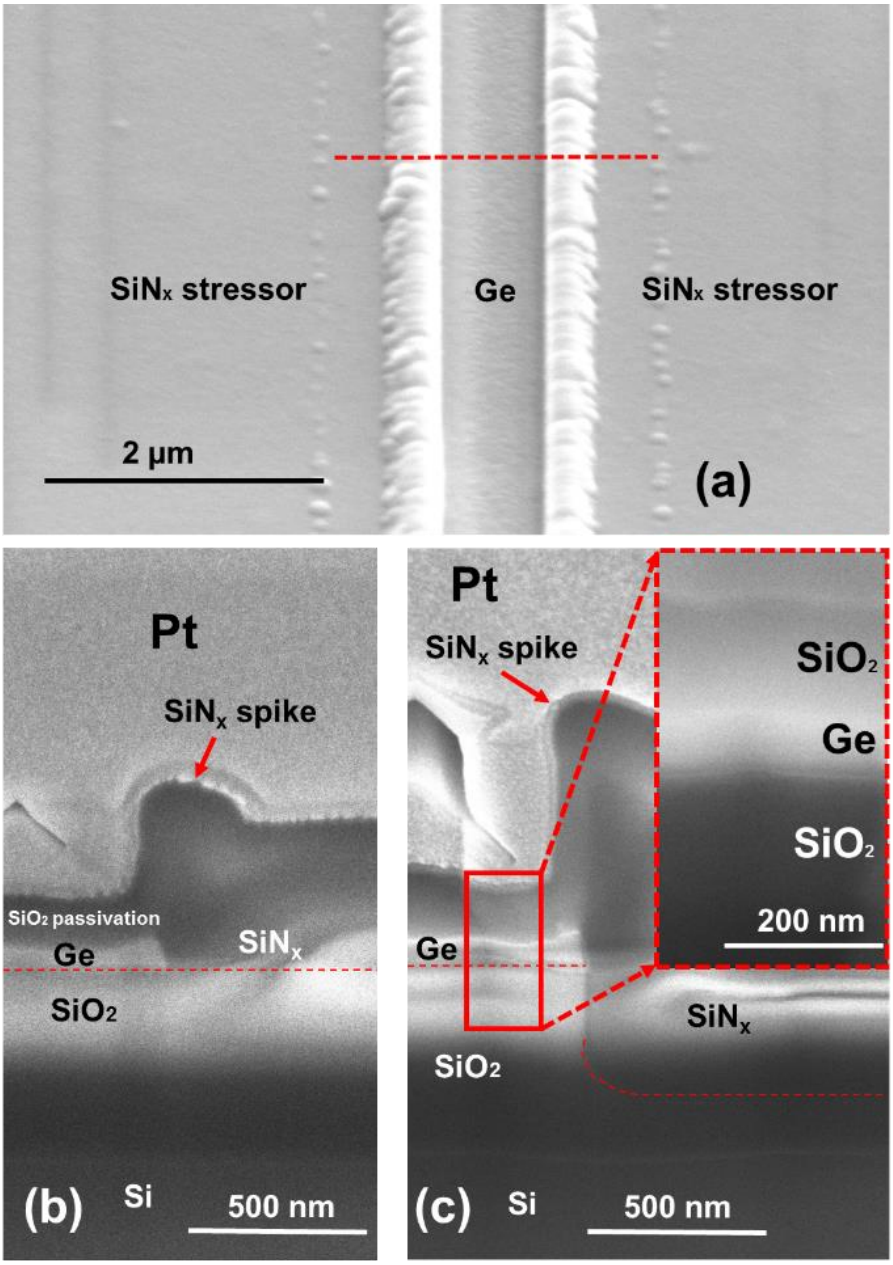


Figure 63 (a) A top-view SEM image of a fabricated $SiN_x$-strained GOI waveguide; the corresponding cross-sectional SEM images of the waveguides (b) without and (c) with the use of SE are shown, prepared by the FIB. Both the FIB cuts were perpendicular to the waveguides, outlined as the dashed line in (a). The inset in (c) is a magnified view of the area in the solid red rectangle, indicating the respective layers of materials.

Micro-Raman measurements were performed on these waveguides using both the lasers with emission wavelengths of 532 and 785 nm. The different wavelengths provide a contrast in the penetration

depth of the incident photons into Ge, therefore revealing a depth-dependent strain profile by collecting the corresponding depth-dependent inelastic-scattered photons. The wavelength of 532 nm could penetrate a half-depth of ~ 9 nm into Ge, while the 785nm could penetrate ~ 89 nm accordingly [10]. In consequence, for the ~ 100 nm-thick Ge waveguide, the 532-nm laser could manifest the strain information close to the waveguide top, whereas the 785-nm laser could collect the strain information throughout the entire waveguide. Fig. 63 shows the corresponding micro-Raman spectra at 785 nm. A bulk Ge wafer and a Ge WGOI without the $SiN_x$ stressor were also measured for stress-free (~ 300.84 $cm^{-1}$) and stressor-free (~ 300.52 $cm^{-1}$) references, respectively. Both the peak LO phonon frequencies of the $SiN_x$-strained waveguides decrease compared to that of the waveguide without the stressor, indicating a successful enhancement of the tensile strain in Ge. The slight blue shift of the peak for the waveguide without the stressor, with respect to the peak of the bulk Ge, is known to be caused by the thermal mismatch-induced tensile strain from the Ge-on-Si epitaxy (Chapter 4.3.3). In addition, the peak is significantly narrower for the waveguide with SADE applied (with a FWHM of ~8.6$cm^{-1}$), compared to that without SADE (FWHM of ~ 12.1 $cm^{-1}$). The peak FWHM is correlated with the uniformity of the strain in the Ge WGOI, since there is negligible Raman peak broadening found for the Ge structures with a remarkably higher tensile strain [11], implying that the peak broadening for the waveguides in this work is unlikely due to the strain-induced crystal quality deterioration [12]. Furthermore, the overlap of the micro-Raman spectra

for the Ge waveguide without stressor and the stressor-detached waveguide (Fig. 68 (a)) verifies that the Ge crystal quality is well maintained. Therefore, the narrower FWHM indicates a more uniform strain profile in the Ge WGOI, by applying SADE.

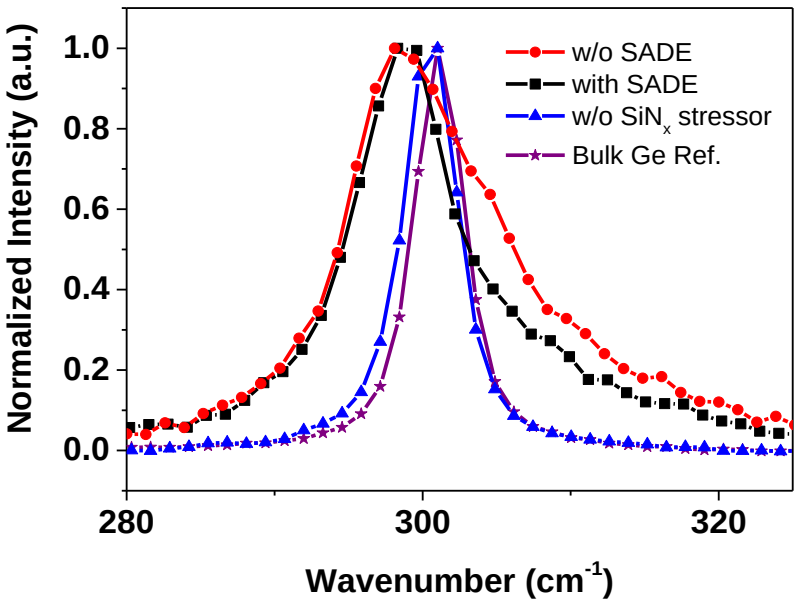


Figure 64 Micro-Raman spectra for the $SiN_x$-strained Ge WGOIs at 785 nm. The spectra of a bulk Ge wafer and a Ge WGOI without the $SiN_x$ stressor are also shown for comparison.

In addition, a shoulder at ~ 304 $cm^{-1}$ was found for the Raman spectrum without the SADE, which reveals the existence of compressive strain in the waveguide. The adoption of SADE prominently eliminates this shoulder, which corresponds to a reduction in the compressive strain and, namely, an enhancement in the overall magnitude of the tensile strain in the Ge WGOI. To further verify the effect of SADE on the strain uniformity, an additional laser emitting at 532 nm, was used, for the reason discussed before. The spectra at 532 and 785 nm were aligned based on their Si peaks (~ 520.6 $cm^{-1}$) for comparison. Fig. 64 (a) and (b) show the overlaid micro-Raman spectra at the two wavelengths for the

waveguides without and with SADE employed, respectively. The spectra completely match for the waveguide with the use of SADE, while a partial overlap below ~ 300 $cm^{-1}$ is observed for that without SADE. The partial overlap clearly manifests a strain non-uniformity in the Ge WGOI and implies the compressive strain is localized near the waveguide bottom. The complete overlap for the spectra with SADE, on the other hand, exhibits a uniform strain profile vertically across the entire waveguide. Since a complete overlap is also observed for the two peaks at 532 nm, indicating a consistent strain at the waveguide top irrespective of the use of SADE, it is believed that SADE works more efficiently on the bottom part of the GOI waveguide to compensate the compressive strain in that region. This is also a clear indication of the alleviation of the substrate constraint, agreeing well with our modelling results in Chapter 6.1.

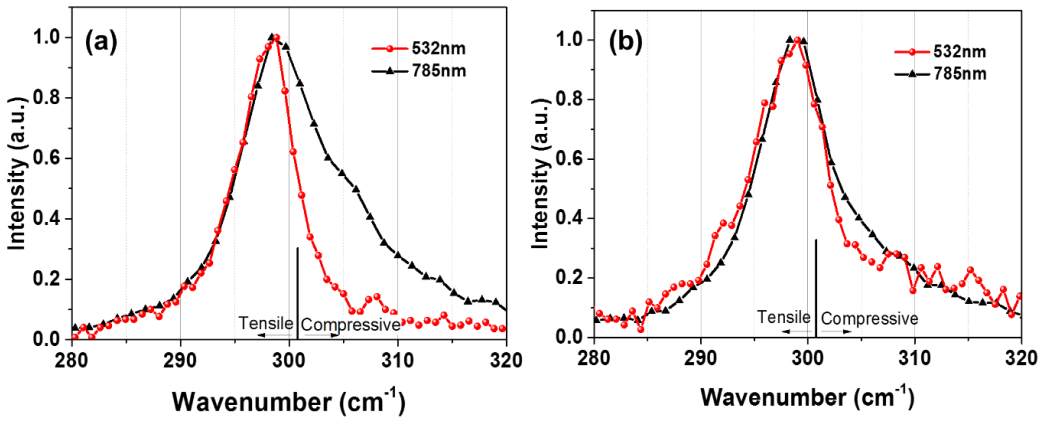


Figure 65 Micro-Raman spectra at 532 and 785nm for the Ge WGOIs (a) without and (b) with the use of SADE.

### 6.3.2.3 Preliminary Strain Magnitude Determination from Micro-Raman Spectra

To preliminarily determine the magnitude of the strain in the $SiN_x$-strained Ge WGOIs, a multiple Lorentzian peak fit was performed on the

micro-Raman spectra obtained at 785 nm. Each individual peak has a fixed FWHM (~ 2.45 $cm^{-1}$) as that of the bulk Ge (Fig. 63) to ensure it completely disassembles the broadening due to the strain non-uniformity. The result is shown in Fig. 65. A single peak centred at ~ 298.9 $cm^{-1}$ was found for the spectrum with SADE (Fig. 65 (a)), with its intensity far exceeding the remaining peaks, highlighting the major strain contribution. To correlate the Raman peak shift with the transverse strain $\varepsilon_{xx}$ in the waveguide, the stress-induced LO phonon frequency splitting relation (Eq. (4.1)) and the stress-strain relation (Eq. (6.1) and (6.2)) were utilized to form the expression below:

$$\varepsilon_{xx} = \frac{(1-v)(\omega_i^2-\omega_0^2)}{E\cdot[pS_{12}+q(S_{11}+S_{12})]} - \varepsilon_{yy} \tag{6.5}$$

where all parameters are identical to that defined in the earlier equations. An $\varepsilon_{xx}$ of ~0.70% (this and all subsequent positive values denote a tensile strain) can thus be deduced by keeping $\varepsilon_{yy}$ at ~ 0.17% (according to Fig. 56 (c) and (d)). On the contrary, no predominant strain contribution can be observed from the spectrum without SADE, due to the strain non-uniformity. Two peaks at 298.41 and 299.91 $cm^{-1}$ that are slightly superior in the intensity qualitatively represent the $\varepsilon_{xx}$ of ~ 1% and ~ 0.3%, respectively, in the waveguide. An accurate determination would be to measure the absorption edge of the corresponding photodetectors and correlate it with the magnitude of the strain via the deformation potential theory discussed in Chapter 3.4. A detailed study will be discussed in Chapter 7.

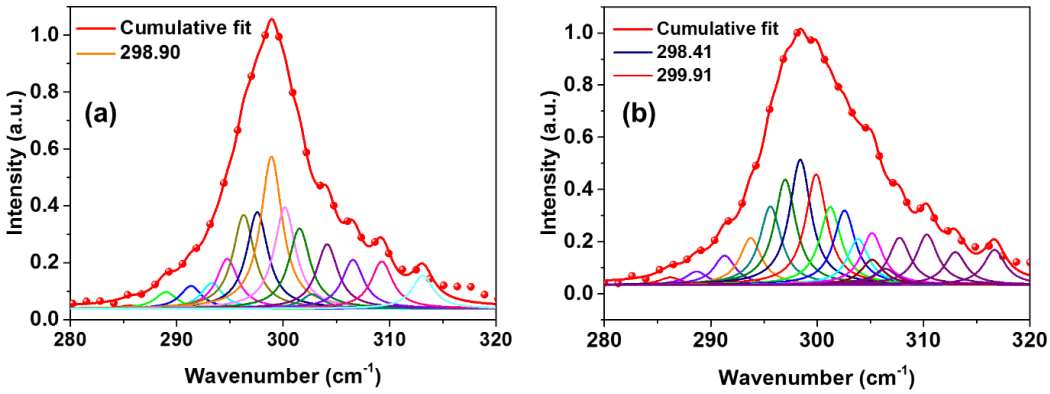


Figure 66 A multiple Lorentzian peak fit for the Raman spectra (a) with and (b) without SADE at 785 nm.

## 6.3.3 Key Process Development

In this section, key process development will be validated for a high quality and reliability $SiN_x$-strained Ge WGOI fabrication, via the micro-Raman characterization. Chapter 6.3.3.1 discusses the effect of the top $SiN_x$ removal on the strain in the Ge WGOI. Chapter 6.3.3.2 illustrates the use of the $Al_2O_3$ and $SiO_2$ capping layers on the lifetime enhancement of the tensile strain.

### 6.3.3.1 Top-$SiN_x$ Removal

Since the $SiN_x$ stressor can only be applied on the waveguide via PECVD, the tensile $SiN_x$ layer on the waveguide top will induce undesired compressive strain to the Ge underneath. Fig. 67 shows the micro-Raman spectrum of a Ge WGOI deposited with ~ 400 nm tensile $SiN_x$ (at the laser wavelength of 532 nm). The peak is red-shifted, compared to that of the bulk Ge, indicating compressive strain. In contrast, the waveguides employing the top-$SiN_x$ removal exhibit a blue-shift of the peak indicating a tensile strain (Fig. 64 and 65 above). This is because the removal could

segregate the stressors at both the sidewalls and maximize their efficiency in straining the waveguide transversely.

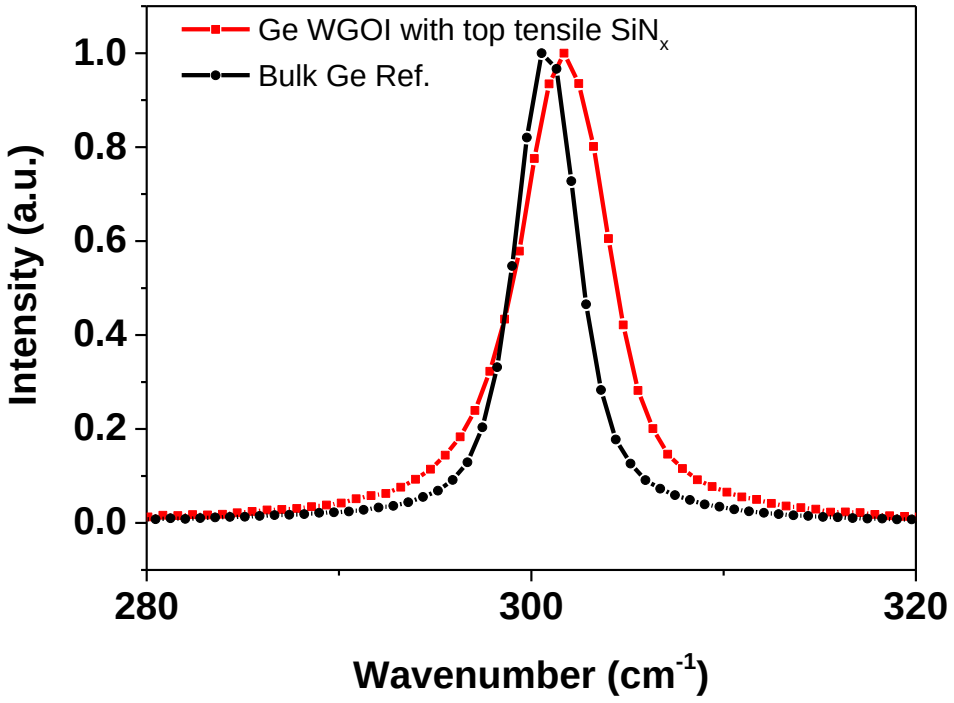


Figure 67 Micro-Raman spectrum of a Ge WGOI deposited with tensile-stressed $SiN_x$.

### 6.3.3.2 $Al_2O_3$ Interlayer and $SiO_2$ Capping

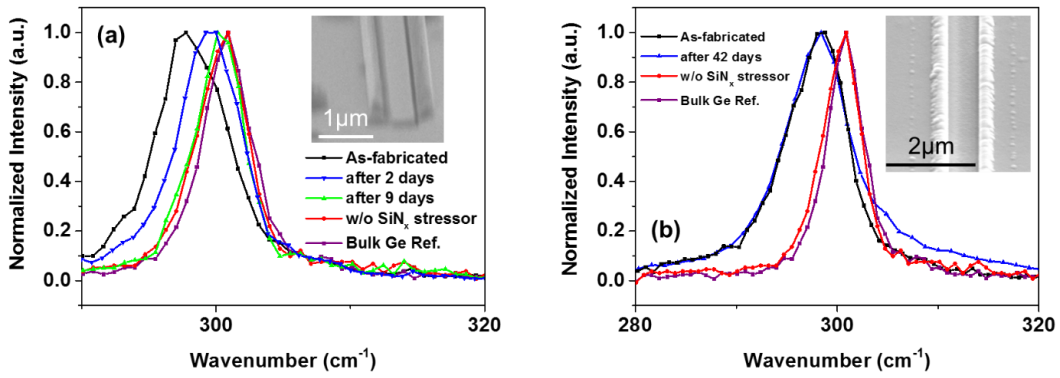


Figure 68 Micro-Raman spectra of the $SiN_x$-strained Ge WGOI (a) without capping and (b) with $SiO_2$ capping, with respect to the time since fabrication.

Fig. 68 (a) shows the red-shift of the micro-Raman peaks, with respect to time, from the initial batch of the $SiN_x$-strained waveguides, where the $SiN_x$ stressor is directly deposited on the Ge waveguide followed by the top-$SiN_x$ removal. This indicates a progressive lowering of the tensile strain in the waveguides. A SEM inspection finds that the stressors were completely detached from the waveguide sidewalls as shown in the inset, and thus the strain was lost. In view of the progressive development of the stressor delamination, it is suspected that the formation of the volatile native oxides $GeO_x$, due to the moisture attack in air, might be the reason. The volatile oxides weakened the interaction between the $SiN_x$ and Ge, which causes the detachment.

Therefore, to validate this assumption, $Al_2O_3$ and $SiO_2$ deposition were incorporated as described in the fabrication process. The $Al_2O_3$ interlayer, besides the etch-stop, can also serve as a moisture barrier [13] together with the $SiO_2$ capping at the final step. Fig. 68 (b) depicts that the tensile strain is maintained in the waveguide after 42 days without a shift in the Raman peak, suggesting a significant enhancement on the life time of the generated tensile strain. There is also no delamination of the stressor observed from the SEM image in the inset. The results support the assumption of moisture attack for the stressor failure. The strain is also expected to be maintained for an unforeseeably-long period.

In conclusion, the insertion of $Al_2O_3$ interlayer and $SiO_2$ capping successfully improves the life time of the induced tensile strain in Ge,

which is believed to be limited by the moisture diffusion into the $SiN_x$/Ge interface.

## 6.4 Conclusion

In this chapter, a tensile-strained Ge WGOI with an enhanced strain magnitude and uniformity was successfully demonstrated, both theoretically and experimentally, utilizing a recessed tensile-stressed $SiN_x$ stressor at the waveguide sidewalls. The enhancement was enabled by a sidewall contact of the stressor to the underlying $SiO_2$, together with the Ge waveguide, by creating trenches into the $SiO_2$. Therefore, the portion of the $SiO_2$ between adjacent trenches was also tensile-strained, which consequently alleviates its constraint in straining the bottom part of Ge close to the Ge/$SiO_2$ interface. This leads to a strain profile with an increased magnitude at the corresponding region, resulting in an improved overall uniformity. The FEM modelling results agree well with the concept. In preparation for the experimental demonstration of the concept, the trenches were realized by a simple and CMOS-compatible SADE method. Deposition of a highly-stressed $SiN_x$ film was also studied, by optimizing the deposition parameters, along with a post-deposition furnace annealing. Good quality films with a tensile and compressive stress of ~ 1 GPa were both achieved. The concept was further verified by the suppression of the compressive shoulder in the micro-Raman spectrum of the fabricated $SiN_x$-strained Ge WGOI, after adopting SADE, which results in an overlapped spectra at different laser wavelengths suggesting a homogenized strain profile. An $\varepsilon_{xx}$ of ~ 0.70% in the Ge

waveguide was also estimated from the micro-Raman spectra. This work facilitates an integrated Ge photodetector with an enhanced efficiency at longer wavelengths. This recessed-stressor approach could also be applied to conventional Ge-on-Si or -SOI platforms and other semiconductor materials, such as III-V and GeSn, which are also bandgap-tunable by strain, for integrated photonic applications.

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# Chapter 7 Metal-semiconductor-metal (MSM) Photodetectors on $SiN_x$-strained Ge WGOI

In this chapter, based on the $SiN_x$-strained Ge WGOI developed in Chapter 6, normal-incidence metal-semiconductor-metal (MSM) photodetectors (PDs) were fabricated. Using the MSM scheme allows for a low thermal budget during fabrication, satisfying the need for BEOL integration. In addition, MSM detectors only require simple processing and exhibit performance advantages such as high speed and gain [1].

Before device fabrication, theoretical calculation was performed to estimate the extension of the absorption coverage using deformation potential theory, which will be discussed in Chapter 7.1. The fabrication process flow for the GOI MSM PDs will then be illustrated in Chapter 7.2. The device characterization was performed in terms of DC characteristics (dark current-voltage and optical response) and high-frequency performance (3dB-bandwidth), which will be discussed in Chapter 7.3. The enhancement on the QE and the extension of the absorption coverage will also be evaluated. Chapter 7.4 will elaborate on the future process development for the $SiN_x$-strained GOI MSM PD for an improved performance. It is then demonstrated in Chapter 7.5 that the effect of the recessed sidewall $SiN_x$ stressor can be varied by tuning the structural parameters of the Ge WGOI. Hence, optimizing the waveguide

dimensions is also critical for a maximal strain in Ge, apart from maximizing the $SiN_x$ stress. Chapter 7.6 concludes the entire chapter.

# 7.1 Absorption Coverage Calculation

The extension of the Ge absorption coverage, due to the applied transverse tensile strain $\varepsilon_{xx}$, is firstly calculated using deformation potential theory as introduced in Chapter 3.4. For a specific $\varepsilon_{xx}$, since the $\varepsilon_{yy}$ is a constant at ~ 0.17% independent of the $SiN_x$ stressor, the strain along the *z*-direction ($\varepsilon_{zz}$) can be deduced from Eq. (6.3), where the $\sigma_{xx}$ and $\sigma_{yy}$ can be obtained from Eq. (6.1) and (6.2). The $\varepsilon_{xx}$, $\varepsilon_{yy}$ and $\varepsilon_{zz}$ were then plugged into Eq. (3.4) and (3.5) to acquire $E_g^{LH}$ and $E_g^{HH}$ in Eq. (3.6) and (3.7), respectively. The bandgap energies were then converted to wavelength values as the *x*-axis of the plot, as shown in Fig. 69 (a). Fig. 69 (b) and (c) show the corresponding $\varepsilon_{xx}$ profiles from the FEM modelling described in Chapter 6.1 without and with the use of SADE, respectively. The FEM models were built with identical structural parameters (1 μm in width and 400 nm in thickness) and $SiN_x$ stress (580 MPa tensile) to that in the fabricated $SiN_x$-strained Ge WGOIs. The average $\varepsilon_{xx}$ of ~ 0.40% from the model employing SADE (Fig. 69 (c)) corresponds to a *Γ*-HH and *Γ*-LH bandgap edges at ~ 1599 and ~ 1623 nm, respectively. The entire *L*-band would thus be included into the inter-band absorption coverage, facilitating a substantial QE for the GOI PDs working at longer wavelengths.

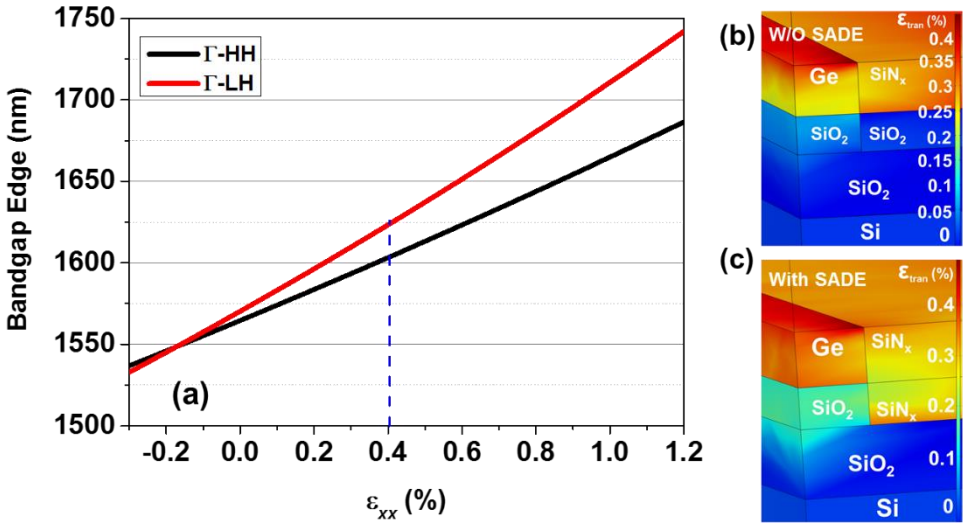


Figure 69 (a) Calculated Ge direct bandgap edges as a function of the applied transverse strain $\varepsilon_{xx}$. The $\varepsilon_{xx}$ profiles from FEM modelling without and with the use of SADE are shown in (b) and (c), respectively. The FEM models are built with identical structural parameters to that of the fabricated $SiN_x$-strained Ge WGOIs.

## 7.2 Device Fabrication

The $SiN_x$-strained Ge MSM PDs were then fabricated based on the $SiN_x$-strained Ge WGOI developed in Chapter 6. The top-view schematic of the device is shown in Fig. 70 (a), while the corresponding cross-sectional schematics with and without the use of SADE are shown in (b) and (c), respectively. The fabrication for the $SiN_x$-strained Ge WGOI is exactly identical to that described in Chapter 6.3.1, except the following variations. The Ge strip waveguide-mesas are 1 μm in width and ~ 400 nm in thickness. The $SiO_2$ trench depth is ~ 300 nm by using SADE. Apart from being an etch-stop layer, the ~ 1 nm-thick $Al_2O_3$ also unpins the Fermi level at the metal-Ge Schottky contact to suppress the device dark current [2]. After the $SiN_x$-strained Ge WGOIs were realized, contact openings were created at the waveguide top, by an additional EBL patterning followed by a $SF_6$-based RIE to expose the $Al_2O_3$-passivated

Ge. The device fabrication ended with sputtering and lift-off of a Ti/TiN/Al metal stack to form the interdigitated Schottky contacts. For comparison, control devices passivated with stress-free $SiN_x$ were also fabricated.

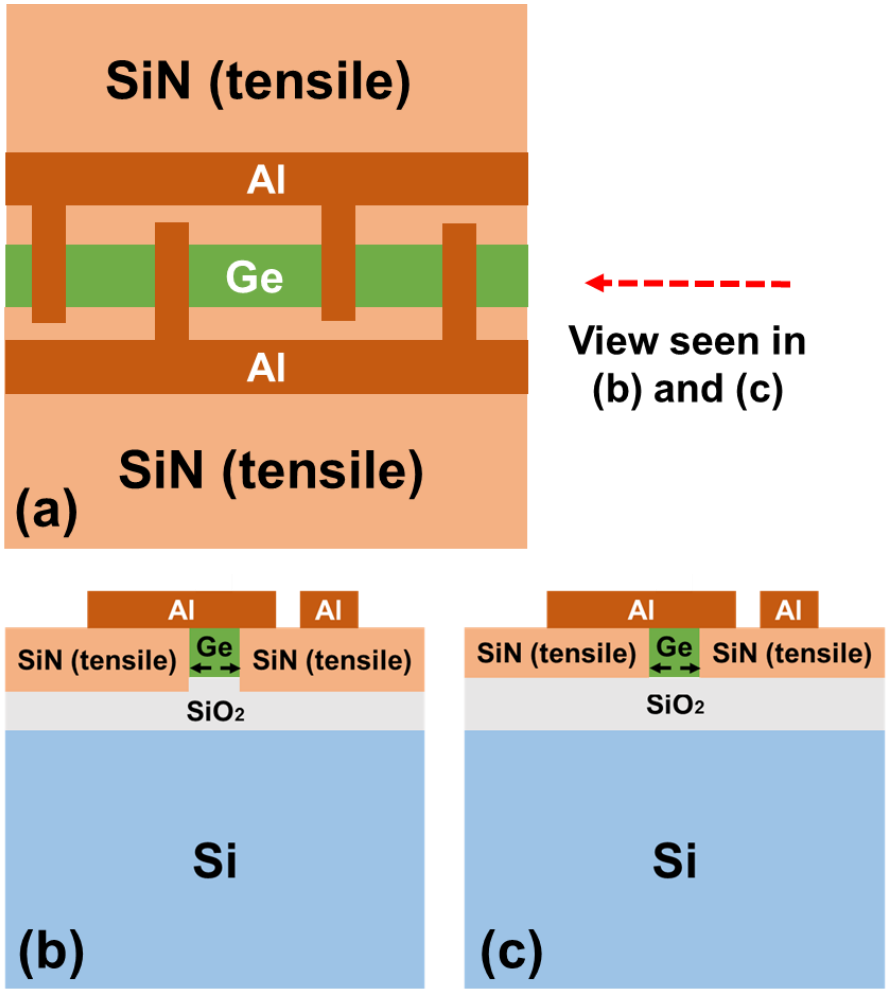


Figure 70 (a) Top-view schematic of the $SiN_x$-strained GOI MSM PD; (b) and (c) are the cross-sectional schematics of the PDs with and without the use of SADE, respectively.

## 7.3 Device Characterization

Fig. 71 (a) shows an optical microscope image of a fabricated $SiN_x$-strained GOI MSM PD. The anodes and cathodes of the interdigitated contact were extended into Ground-Signal-Ground (GSG) configuration for the high-frequency performance measurement. A top-view FESEM

image at the area highlighted in (a) is shown in (b), clearly exhibiting the active region of the device.

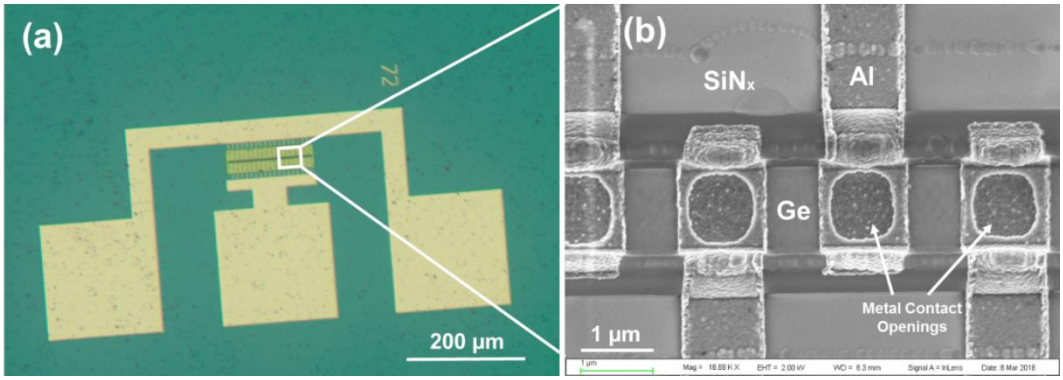


Figure 71 (a) An optical microscope image of a $SiN_x$-strained Ge MSM PD; (b) a top-view FESEM image of the device at the region highlighted in (a), exhibiting the active area with Ge waveguide mesa, $SiN_x$ stressor and interdigitated metal contacts.

FIB was used to observe the cross-sectional device features, shown as the corresponding FESEM images in Fig. 72. Fig. 72 (a) gives an overview of the device area under FIB cut. The area highlighted by a red solid box is magnified and shown in (b), with all respective layers and features indicated.

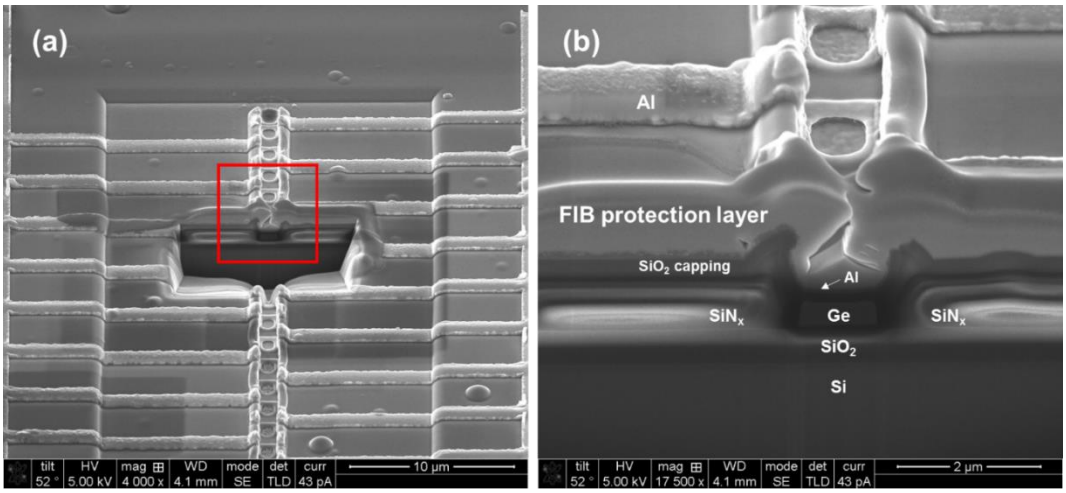


Figure 72 (a) A tilted FESEM image of $SiN_x$-strained GOI MSM PD with an opening by FIB cut; (b) A magnified image from the area highlighted by the red solid box in (a), showing the cross-sectional device features.

### 7.3.1 DC Characteristics

The dark currents and photocurrents of the Ge MSM PDs exhibit regional non-uniformity indicating process variations. Fig. 73 (a) and (b) show the dark- and photo-currents of two 36 μm-long unintentionally-strained GOI MSM PDs with respect to the applied voltage bias, at different locations in the same process run. The dark current for the device in (a) is ~147 and ~359 nA at 1 and 2 V, respectively. The dark current densities are comparable to or lower than that of the reported Ge MSM PDs with $Al_2O_3$ interlayer [1] and other interlayer materials such as $TiO_2$ [3], a-Si:H [4] and Si:C [5]. Although the Schottky barrier height is yet to be extracted from temperature-dependent dark current measurement, the Fermi level de-pinning can be considered successful in this case due to the low dark current. However, optical power of 10mW under normal illuminance, via a Corning SMF-28 single-mode silica glass fiber, gives photocurrents of ~ 11 μA and ~ 34 μA at 1 and 2 V, respectively, which are approximately two orders of magnitude higher than the dark current. Assuming a uniform distribution of the power throughout the circular fiber core (~ 9 μm in diameter) and eliminating the metal-shielded area, the responsivities can be estimated as ~ 0.03 and ~ 0.1 A/W. The low QE might be due to the residual $SiN_x$ between the metal and Ge that suppressed the tunneling of the photon-generated carriers through the Schottky barrier. This can be resulted from the insufficient RIE during the $SiN_x$ removal during the contact opening process. On the contrary, the other device in (b) shows high dark currents of ~ 264 μA and 1.07 mA at 1 and 2 V, respectively. The high dark current might be attributed to the

un-intentional thinning of the $Al_2O_3$ interlayer during the $SiN_x$ removal, which leads to an inefficient Fermi level de-pinning. The photocurrents are ~ 500 μA and ~ 1.26 mA correspondingly under the 10-mW illumination, resulting in responsivities of ~ 1.06 and ~ 2.68 A/W, respectively. The high QE indicates a substantial optical gain in the devices, agreeing with the prior report [1]. Therefore, the RIE process for the contact opening needs to be optimized for an improved etch-depth uniformity among the devices. Nevertheless, one can comparatively conclude that the device in (a) suffers from an excess interlayer thickness (residual $SiN_x$) and the optical gain can be further maximized. Consequently, there might exist an optimal interlayer thickness that can balance the gain and photocurrent for an optimal device DC performance, where some carriers could be trapped at the interface between the interlayer and Ge for the generation of additional image carriers for the optical gain, and meanwhile most of the photon-generated carriers could still be tunneled through as photocurrent. In Chapter 7.4, we will propose an improved fabrication process where the Schottky contacts are directly formed on the $Al_2O_3$-coated Ge, without the need of $SiN_x$ RIE for the contact opening, which might eliminate the issue with the etching non-uniformity.

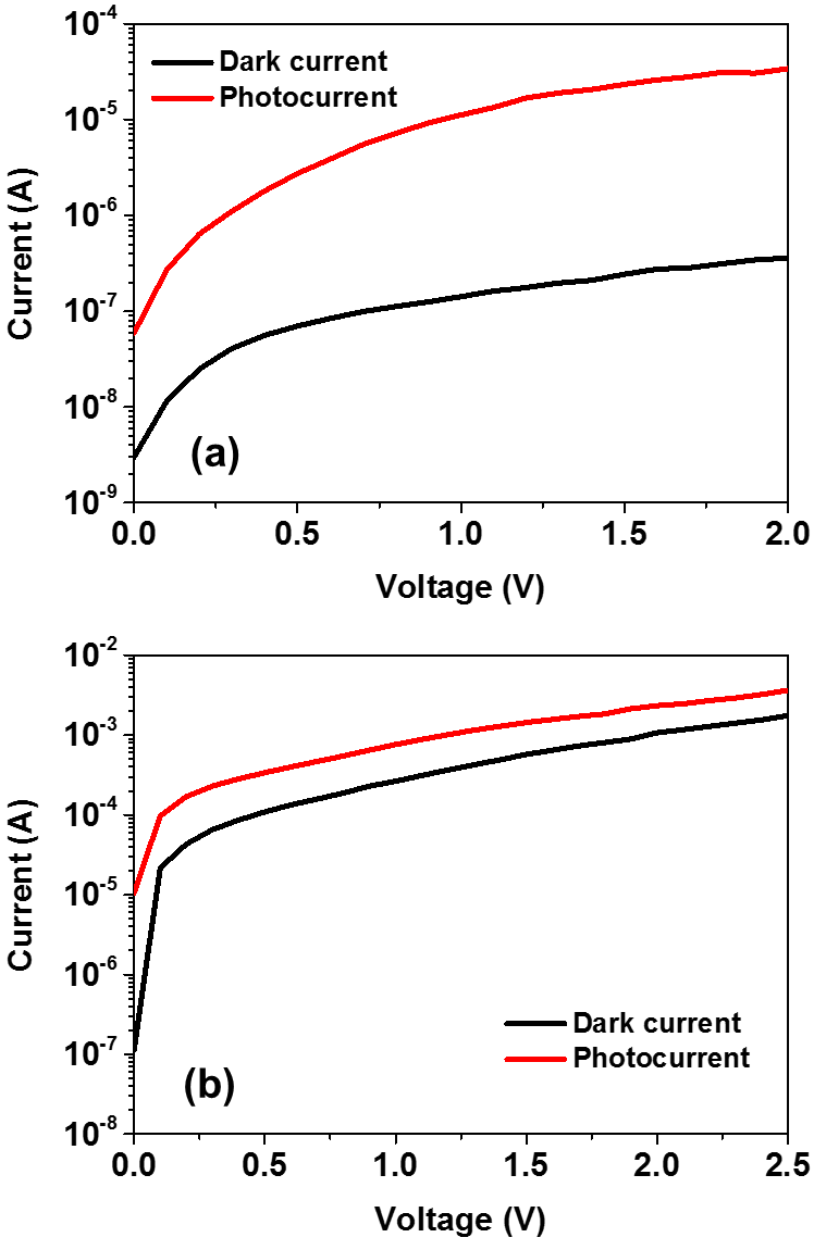


Figure 73 Dark currents and photocurrents of two unintentionally-strained GOI MSM PD.

## 7.3.2 Normalized Photocurrent Spectra

Due to the process non-uniformity mentioned above, it would be challenging to directly compare the photocurrents among the devices for their QE evaluation. Therefore, normalized photocurrents were collected as a function of the incident optical wavelength for the QE comparison.

This is because the normalized photocurrent, with respect to that at a specific wavelength, can be related to the bandgap shift and consequently the QE.

### 7.3.2.1 Absorption Coefficient Enhancement

Fig. 74 shows the normalized photocurrents of the Ge MSM PDs as a function of the incident optical wavelength spanning across the *C*- and *L*-bands (1500 to 1630 nm) using a TUNICS T100S-HP/CL tunable laser. The corresponding dark currents had been subtracted from the photocurrents, before the net photocurrents were normalized with respect to that at 1500 nm. The normalized photocurrents were found comparable within the *C*-band among all types of devices, while a significant enhancement was seen for both the $SiN_x$-strained devices beyond ~ 1560 nm. This is the demonstration of the further shrinkage of the Ge bandgap caused by the $SiN_x$-induced tensile strain in the Ge WGOI. The reduced bandgap facilitates a higher number of states close to the band extrema to accommodate more electron-hole pairs generated by photons at longer wavelengths, resulting in the higher normalized photocurrents. The enhancement was also found to increase with increasing wavelength at the *L*-band and beyond, where the photocurrents are increased by more than ~ 50% and ~ 2×, respectively, for the $SiN_x$-strained devices without and with the use of SADE and reaches ~ 2× and ~ 3× at 1630 nm. The relatively noisy spectra for the $SiN_x$-strained devices might be attributed to the additional process step of RIE for the contact opening, compared to that for the unstrained control device, which resulted in an imperfect contact interface as well as a weaker optical response. An improved

version of the fabrication process will be discussed in Chapter 7.4 to alleviate this challenge. Nevertheless, the improvement in the normalized photocurrent suggests a stronger QE for the GOI detectors, enabling a superior optical transceiver at longer wavelengths for WDM-based optical communications.

Since the fabricated devices are with identical capping and incident power, the respective photocurrents $I_{ph}$ can be considered proportional to the amount of photons absorbed and expressed as follows:

$$I_{ph} \propto (1 - e^{-\alpha d}) \tag{7.1}$$

where $\alpha$ is the Ge absorption coefficient and $d$ is the Ge thickness (~ 400 nm). As $\alpha d \ll 1$, the approximation of $1 - e^{-\alpha d} \approx \alpha d$ can be satisfied using the Maclaurin series of exponential function. Further, after the normalization, the dependency on $d$ is also eliminated. Therefore, the normalized photocurrents in this study can be directly proportional to the absorption coefficient $\alpha$. We can thus simply correlate the enhancement of the photocurrents to the $\alpha$ and conclude a more than 2× increase on the Ge absorption coefficient correspondingly at the *L*-band. One would thus anticipate a Ge photodetector with half of the absorption length for a commensurate QE and consequently facilitate half of the device capacitance for a 2× speed enhancement, provided that the device is RC-limited.

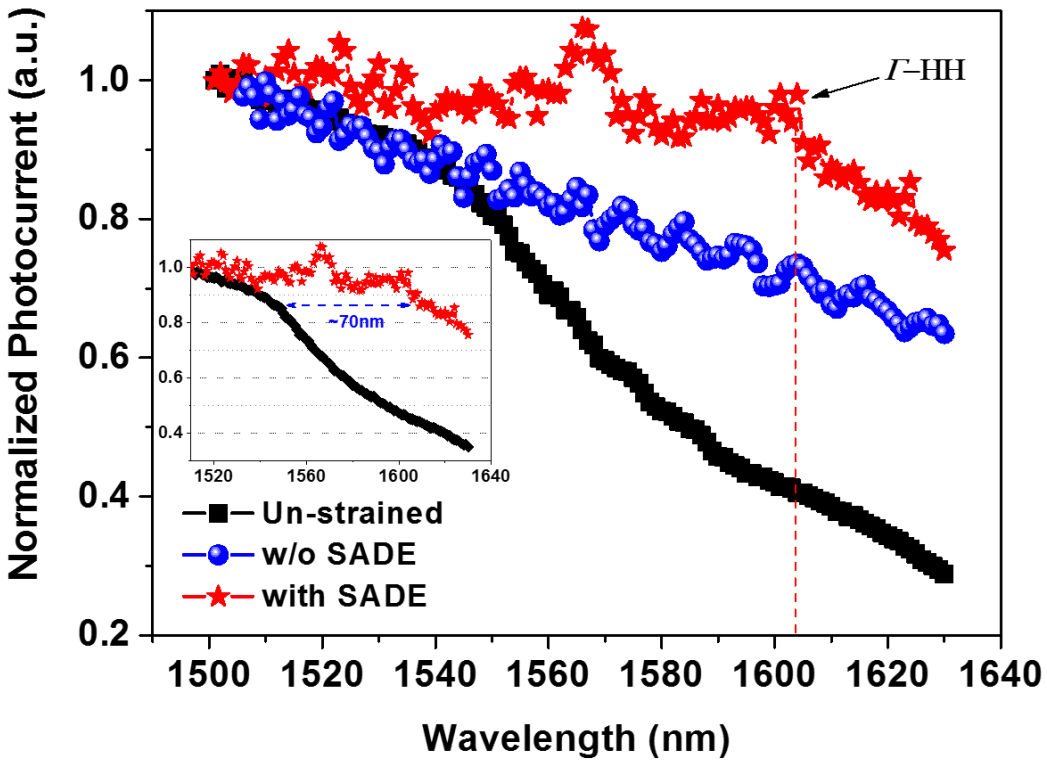


Figure 74 Normalized photocurrents of the GOI MSM PDs as a function of the incident optical wavelength. Inset is the identical plot showing a ~ 70 nm red shift of the absorption edge with the adoption of the recessed $SiN_x$ stressor using SADE.

### 7.3.2.2 Absorption Coverage Extension

With the enhancement of the absorption coefficient, the absorption coverage is simultaneously extended for the GOI MSM detectors employing the $SiN_x$ stressor. As can be seen in the inset of Fig. 74, the use of the 580 MPa-tensile $SiN_x$ stressor, together with SADE of ~ 300 nm, reveals a ~ 70 nm red shift of the Ge absorption range. The extension of the absorption coverage would facilitate a broadband dense wavelength division multiplexing (DWDM) optical communication system. Assuming a state-of-the-art DWDM scheme with a channel interval of 0.2 nm (~ 25 GHz spacing in frequency) [6], the extended absorption range could potentially accommodate an additional ~ 350 channels. A total of

14 Tbps data could thus be transmitted, if a 40 Gbps network is utilized per channel.

The normalized photocurrent spectrum in Fig. 74 for the unstrained device started to drop at ~ 1550 nm, agreeing well with its ~ 0.17% longitudinal residual strain (Chapter 6.1 and 6.3.2.1) that keeps the *Γ*-valley bandgap at ~ 0.8 eV for inter-band absorption. However, the spectrum drops linearly, without exhibiting a clear absorption edge, for the $SiN_x$-strained device without SADE. This can be explained by the non-uniform tensile strain, revealed by the $\varepsilon_{xx}$ profile from the FEM modelling (Fig. 69 (b)) with a non-uniform color code as well as the corresponding micro-Raman spectrum (Fig. 75) with a larger FWHM. This causes a spatial variation of the bandgap shrinkage as well as the extension of the inter-band absorption edge throughout the Ge WGOI. In contrast, the uniform $\varepsilon_{xx}$ profile and micro-Raman spectrum with a smaller FWHM indicate a homogenized tensile strain in the Ge WGOI adopting SADE, resulting in a spatially-uniform bandgap shrinkage to collect more photon-generated carriers and enhance the QE. This can also be supported by the extra ~ 40% photocurrent enhancement at the *L*-band, compared to the device without SADE.

In addition, the normalized photocurrent spectrum with the use of SADE presents a distinguishable drop starting at ~1603nm. The transition wavelength is consistent with the calculated *Γ*-HH bandgap edge at ~1599nm (Chapter 7.1). Considering the flat response below ~1603nm, the photocurrent drop can be attributed to the cut-off of the *Γ*-HH absorption. The calculated *Γ*-LH bandgap edge at ~ 1623 nm is difficult to

be identified from the spectrum due to the emission coverage of the tunable laser that ends at 1630 nm. A light source with a longer wavelength coverage is thus required in future work. Nevertheless, the match of the *Γ*-HH bandgap edges obtained from the modelling and photocurrent measurements gives us a confidence level for the FEM models to estimate the $\varepsilon_{xx}$ in Ge and calculate the bandgap edges. In future work, $SiN_x$-strained Ge MSM PDs with varying $SiN_x$ stress and structural parameters can be fabricated and tested for a comprehensive understanding of the correlation between the $\varepsilon_{xx}$ and the corresponding absorption coverages.

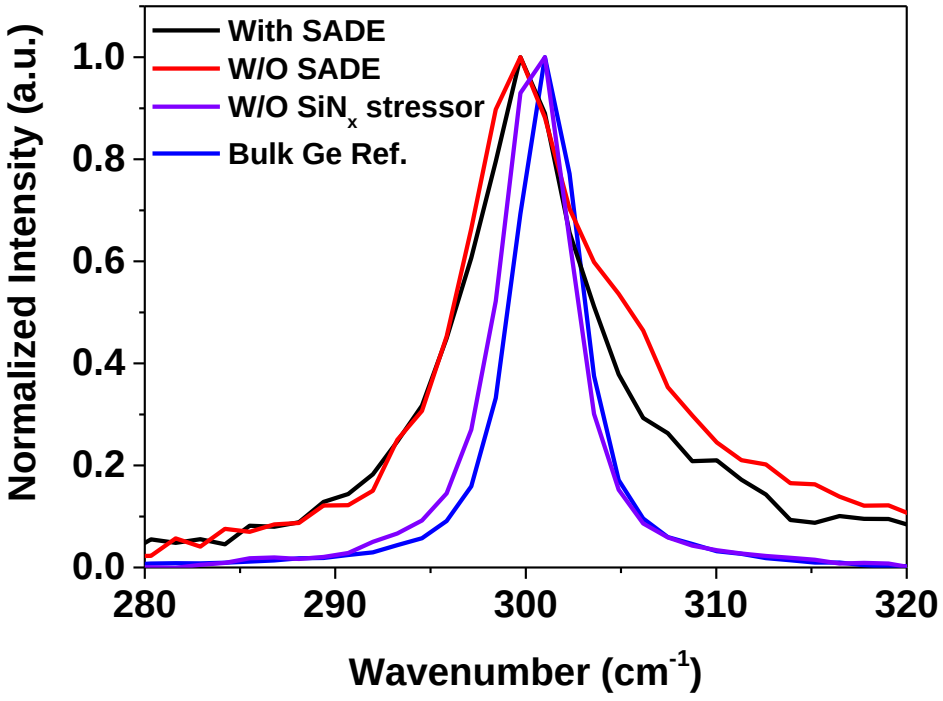


Figure 75 Micro-Raman spectra of the Ge WGOIs that forms the MSM PDs, with respect to the use of $SiN_x$ stressor and SADE.

### 7.3.3 High-frequency response

The frequency response of the device was measured by modulating an optical signal at 1550 nm with varied frequency and simultaneously recording the power output from the photocurrent, as that described in Chapter 5.3.1. The experimental set-up is identical to that described in Chapter 5.3.1. As shown in Fig. 76 (a), a 3-dB bandwidth of ~ 3.75 GHz was observed at 1V bias for a 36 µm-long unstrained Ge MSM PD. The bandwidth increases to ~ 4.5 and ~ 5.1 GHz with the voltage bias increased to 2 and 3 V, respectively. This indicates that the 3dB-bandwidth is transit time-limited. By increasing the bias voltage, the higher electric field lowers the $Al_2O_3$ barrier height and accelerates the carriers for a shorter transit time to the electrodes. Given its contact spacing of 2 µm, the bandwidth is comparable with that of the reported Ge interdigitated MSM PDs with the same contact spacing at the same bias [7]. The contact spacing can thus be further reduced for a higher 3dB-bandwidth.

Fig. 76 (b) shows the frequency response of the PDs with respect to the use of the $SiN_x$ stressor, at a bias of 1 V. The 3-dB bandwidths are ~ 2.6 and ~ 3 GHz, for the PD with and without the $SiN_x$ stressor, respectively. This implies that the tensile strain in Ge does not significantly alter the high-frequency characteristic of the PDs. The $SiN_x$-strained PDs are expected to exhibit a comparable high-speed performance, compared to that of the unstrained PDs.

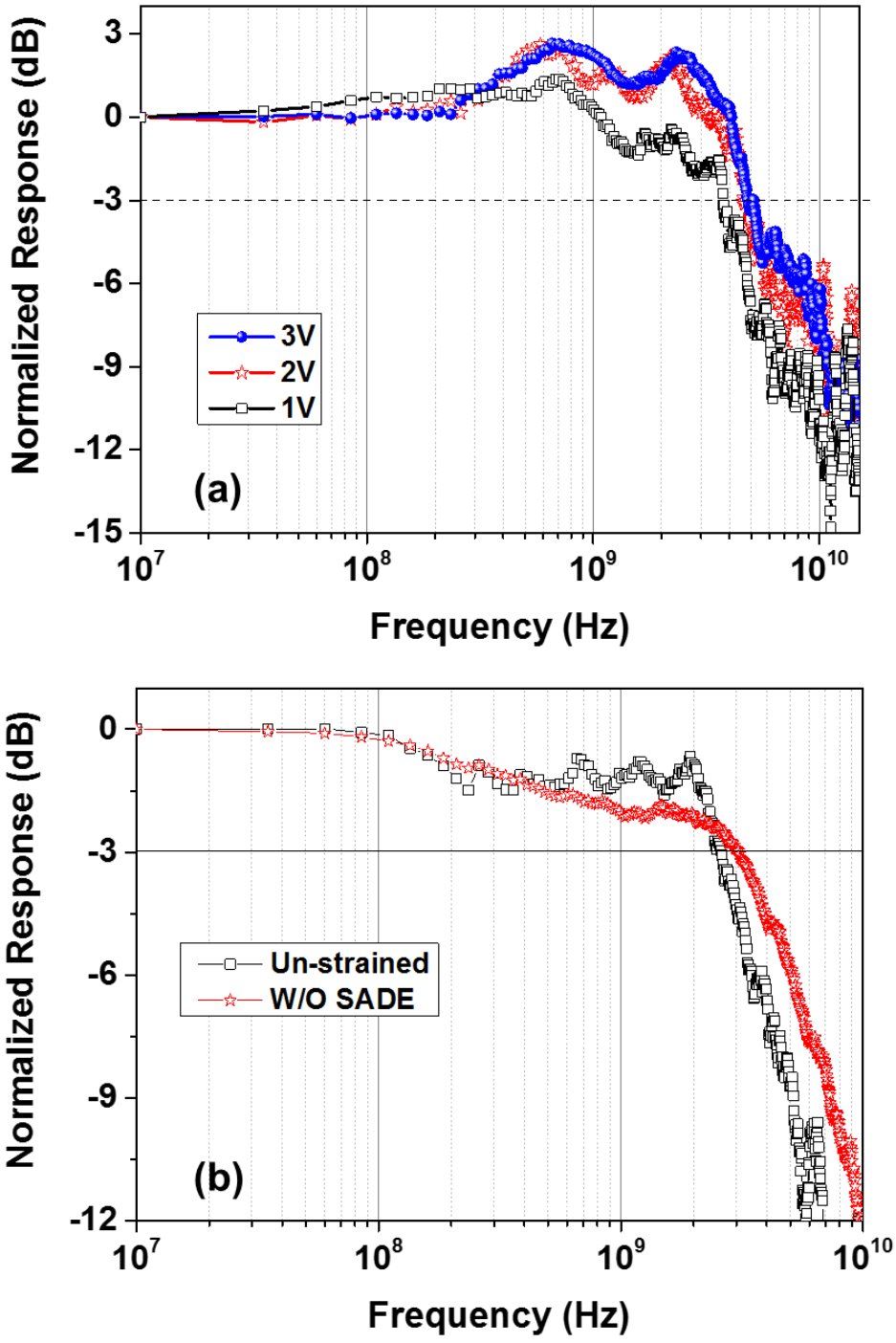


Figure 76 (a) Frequency response of an un-strained Ge MSM PDs with respect to the voltage bias; (b) frequency response of the Ge MSM PDs at 1 V with respect to the use of the $SiN_x$ stressor.

# 7.4 Future Process Optimization

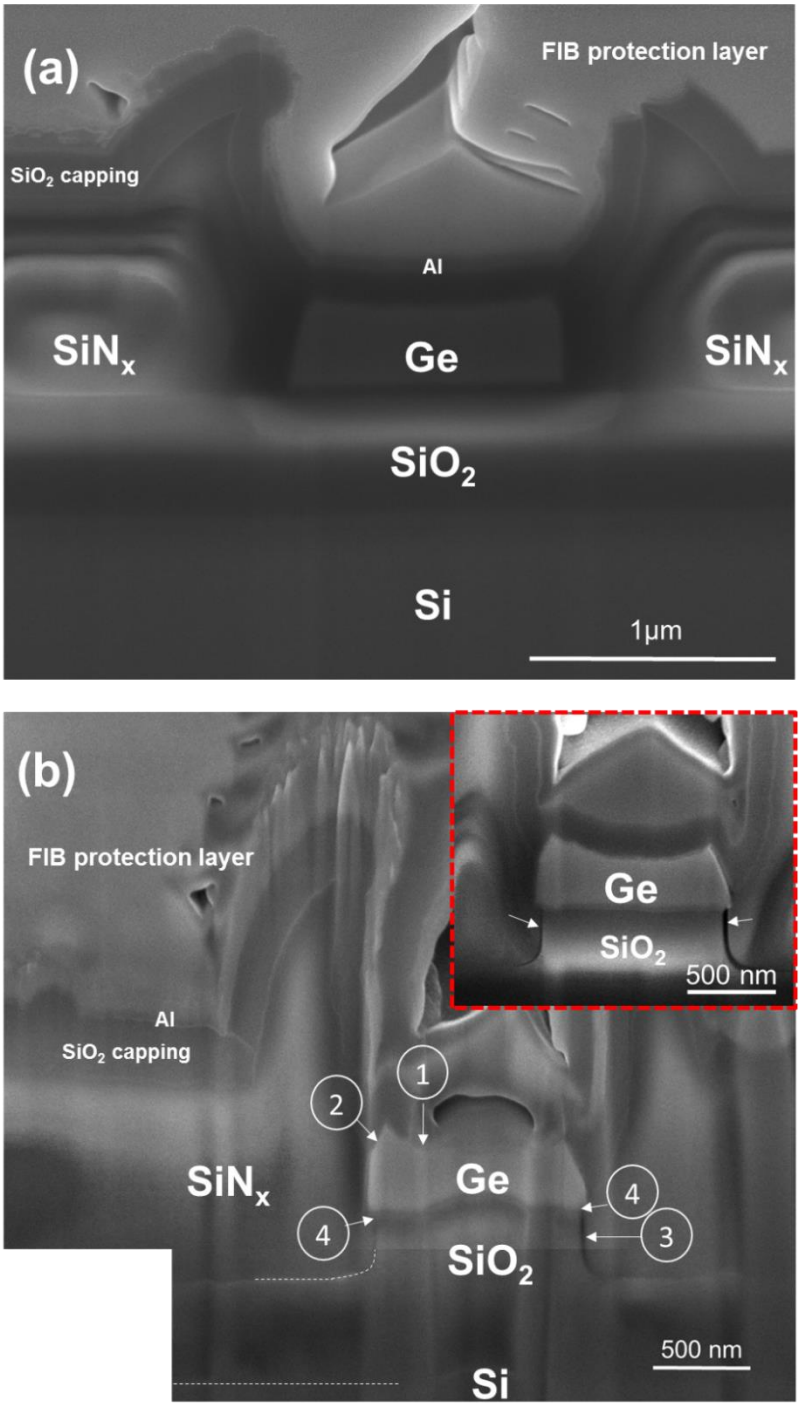


Figure 77 FIB-prepared cross-sectional SEM images of the Ge MSM PDs (a) without and (b) with the $SiN_x$ stressor recessed into the underlying $SiO_2$. The inset in (b) shows the image of the corresponding device after FIB cleaning. The substrate trench depth is ~ 300 nm.

It has been discussed in Fig. 74 that the measured photocurrent is relatively weak for the $SiN_x$-strained GOI MSM PDs using SADE. Besides, the corresponding photocurrent spectrum is also much noisier. Therefore,

it is suspected that it might be due to the fabrication process for the recessed $SiN_x$ stressor that caused the above phenomenon. Therefore, FIB technique was used to unveil the cross-sectional feature of the devices and identify the relevant root causes, with the corresponding SEM images shown in Fig. 77. The observations are summarized as follows (the serial numbers correspond to the numbers indicated in Fig. 77 (b)).

1. Apparently, the top surface of the Ge waveguide is dented, for the device adopting the recessed stressor, compared to that without the substrate trenches (Fig. 77 (a)). This might be due to over-etching of the top $SiN_x$ layer that beyond the protection of the $Al_2O_3$ etch-stop. Meanwhile, the thinner residual waveguide also explains the reason for the weaker photocurrent.
2. The Ge waveguide sidewalls are slanted. This might be caused during the SADE process by the reactive-ion bombardment, when using the Ge waveguide itself as the hard mask for the substrate trench opening.
3. Delamination was observed at the interface between the stressor and the $SiO_2$ sidewall, while the stressor/Ge interface is still kept with a seamless contact. This is probably due to two reasons. First, the slight undercut of $SiO_2$ (the arrow with number 4 in Fig. 77 (b)) resulted from the BOE dip results in the adhesion difficulty for the $SiN_x$ stressor. Second, the smaller Young's modulus of $SiO_2$ (~ 70 GPa) than that of Ge (~ 103 GPa) leads to a contrast in the induced strain that eases the crack formation.

Last but not least, during the FIB preparation, it was found that the cracks develop progressively with time. Fig. 77 (b) was captured before

the final cleaning step and the crack was not that obvious as that in the inset after the cleaning (this is also the reason waterfall features were seen in (b) due to the lack of final cleaning).

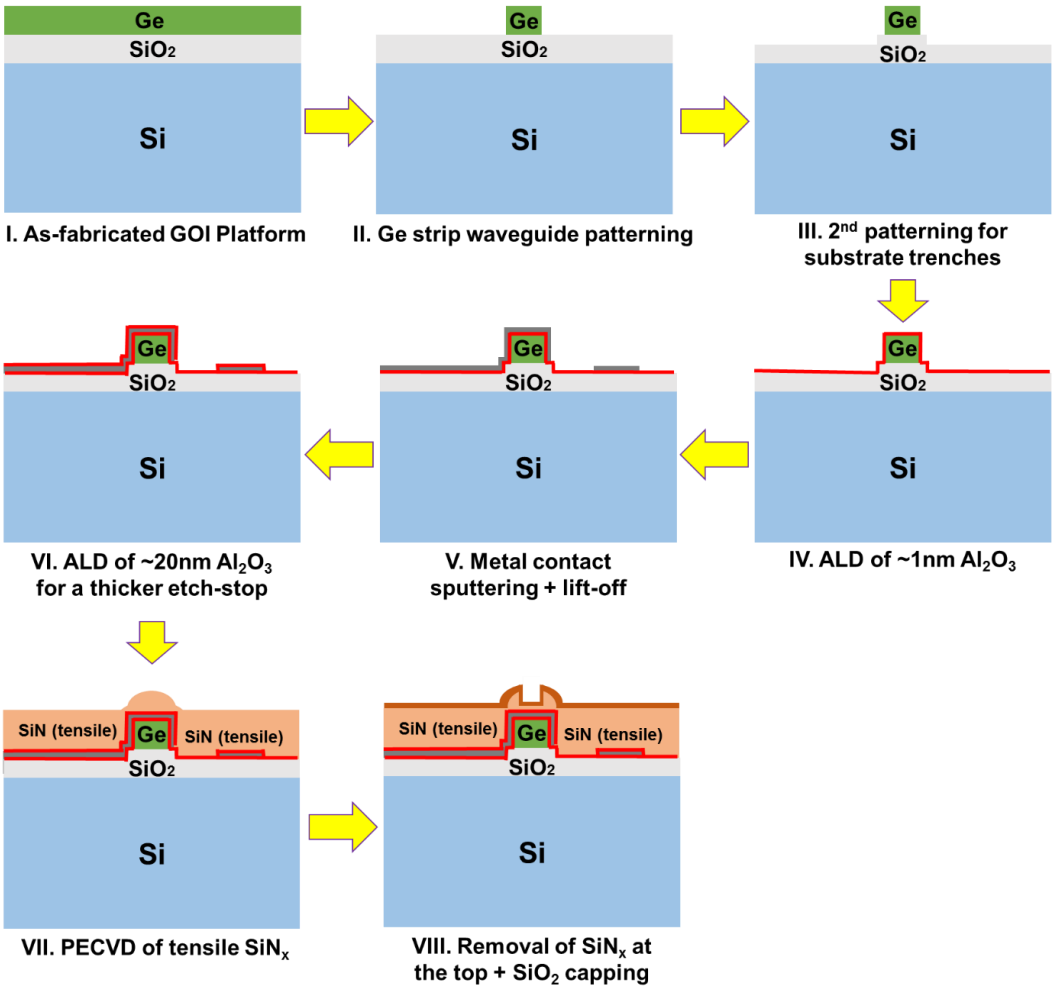


Figure 78 An improved version of the process flow for GOI MSM PD fabrication with recessed $SiN_x$ stressor.

Hence, an improved version of the device fabrication process is proposed in Fig. 78 based on the analysis above. To strengthen the stressor adhesion to the $SiO_2$ sidewall and simultaneously protect the Ge waveguide-mesa sidewall, an additional EBL patterning will be performed to fully cover the Ge waveguide with ZEP520A resist as the hard mask. The resulting $SiO_2$ waveguide will thus be wider (step III). Besides, in step

V, device metallization will be carried out in advance directly after the ALD of ~ 1 nm $Al_2O_3$, before the deposition of the sidewall $SiN_x$ stressor. This could ensure a high-quality ~ 1-nm $Al_2O_3$ interlayer at the metal/Ge interface, not affected by the top $SiN_x$ removal, for the Fermi-level depinning and consequently a stable photocurrent (in contrast to that in Fig. 73). The etch-stop layer will be realized separately by a subsequent ALD of ~ 20-nm $Al_2O_3$ after the metallization (step VI) to protect the contacts and Ge waveguide-mesa during the top $SiN_x$ removal. In this sense, the trade-off on the $Al_2O_3$ thickness will no longer be concerned, for being a thin Schottky barrier and thick etch-stop layer separately. With these modifications, the process will be much easier to control, and the device performance is expected to be improved.

## 7.5 Strain Modelling towards a Longer Absorption Coverage

The $SiN_x$-strained GOI MSM PDs realized in previous sections have demonstrated a ~ 70 nm extension of the absorption coverage and are expected to exhibit an absorption edge beyond 1630 nm including the entire *L*-band, where over ~ 2× quantum efficiency enhancement was also achieved. However, the investigation towards an extreme extension of the absorption coverage (i.e. a maximal magnitude and uniformity of the tensile strain) is of paramount interest within the capability of state-of-the-art technology. As stated before, since the optical fibre at short-reach communication does not suffer a substantial loss beyond the *C*-band as that at long-haul, a longer absorption coverage for detectors would facilitate a higher data rate under the WDM scheme for optical

transceivers in intra- or inter-data-centre communication. Therefore, in this section, we will study and propose potential options for a further enhancement of the transverse strain $\varepsilon_{xx}$ in the Ge waveguide-mesa for an extreme extension of the absorption edge. The study could serve as a guide for the design of integrated $SiN_x$-strained GOI PDs in the future.

## 7.5.1 The Effect of $SiN_x$ Stress

Fig. 79 shows the effect of intrinsic tensile stress in the sidewall $SiN_x$ stressor on the transverse strain $\varepsilon_{xx}$ in the Ge WGOI at different waveguide widths. All data were extracted from FEM modelling with the detailed information discussed in Chapter 6.1. The recessed substrate trenches were not employed in this study. The points on the lines denote the average $\varepsilon_{xx}$, which was calculated by averaging the values in the waveguides spatially across the *x*-*z* plane penetrating through the *y*-center of the waveguide (Fig. 56 (c) and (d)). The error bars indicate the $\varepsilon_{xx}$ span according to the standard deviation of the $\varepsilon_{xx}$ values, respectively. It is not surprising that the $\varepsilon_{xx}$ increases with an increasing $SiN_x$ stress for all the waveguides, due to its higher stress transferred to the Ge via the sidewall contact. Furthermore, it was also found that the $\varepsilon_{xx}$ increases faster with the waveguide width reduces, suggesting a higher $\varepsilon_{xx}$ that can be achieved in a narrower waveguide at a particular $SiN_x$ stress. This is, as discussed in Chapter 6.1.1, due to the relieved substrate constraint along the transverse direction that made the stress transfer easier. A $\varepsilon_{xx}$ of ~ 0.57 and ~ 0.85% can be induced in a 500 nm-wide waveguide, under the $SiN_x$ stress of 1 and 1.5 GPa, respectively, which are both enhanced by more than two times compared to that in a 6

μm-wide waveguide. However, the observation on the $\varepsilon_{xx}$ span finds that the strain uniformity degrades with increasing $SiN_x$ stress. At a particular $SiN_x$ stress, the uniformity also deteriorates with decreasing waveguide width. Therefore, the strain uniformity tends to be a hurdle on the way towards a higher tensile strain. This also highlights the necessity of the substrate trenches for the strain uniformity improvement.

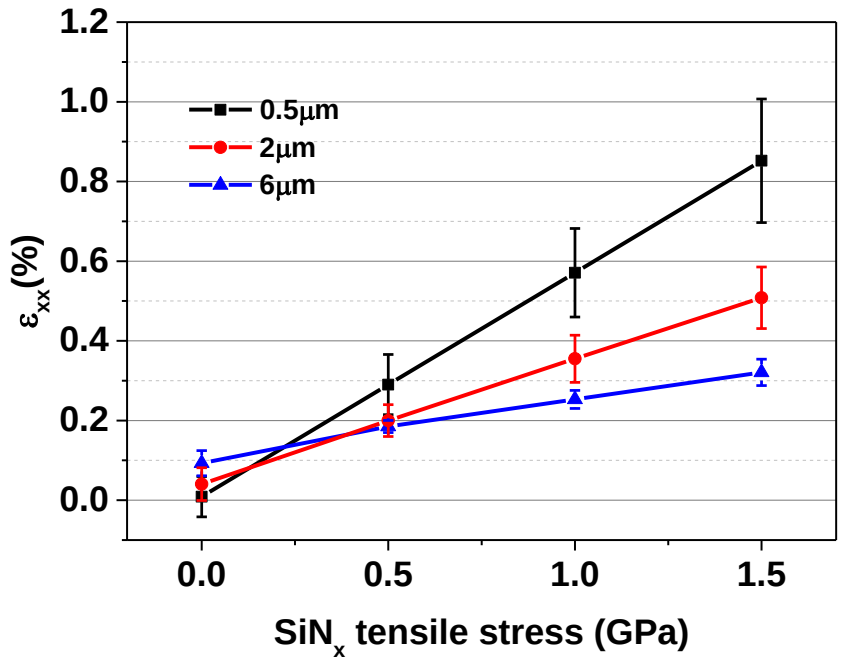


Figure 79 FEM-calculated transverse strain $\varepsilon_{xx}$ in the Ge WGOI as a function of the intrinsic tensile stress in the $SiN_x$ stressor, at different waveguide widths. The waveguide height is 400 nm. Recessed stressors are not employed.

## 7.5.2 The Effect of Ge Waveguide Width/Height Ratio

From Fig. 79, one could observe a waveguide width-dependency on $\varepsilon_{xx}$. To further reveal the effect of Ge waveguide width and recessed stressor on $\varepsilon_{xx}$, Ge WGOIs with varied widths at the $SiN_x$ tensile stress of 580 MPa, identical to that PECVD-deposited, were modelled. The waveguides were built with the same height of ~ 100 nm as that fabricated in Chapter 6.3. Another group of Ge WGOIs employing the recessed

stressor with a trench depth of 500 nm were also included as a comparison. The results are shown in Fig. 80. The average $\varepsilon_{xx}$ increases with decreasing waveguide width, irrespective of the creation of the substrate trench, agreeing with the trend shown in Fig. 79. The $\varepsilon_{xx}$ improves negligibly for the waveguides wider than 5μm, even with the substrate trenches employed. It can also be found that the recessed stressor-induced strain magnitude enhancement increases with decreasing waveguide width, which indicates that the recessed $SiN_x$ stressor works more efficiently on narrower waveguides for improving the strain magnitude. Besides, the corresponding $\varepsilon_{xx}$ span is reduced for the waveguides narrower than 5 μm, suggesting a strain uniformity improvement. However, the span shrinks unevenly among the narrower waveguides, with the 2-μm waveguide most significantly and the 0.5-μm least significantly. Therefore, there exists a trade-off between the strain magnitude and uniformity by tuning the waveguide width, although the use of the recessed $SiN_x$ stressor could be of help in alleviating the trade-off. The inset summarizes the $\varepsilon_{xx}$ determined from the micro-Raman peaks of the fabricated Ge WGOIs in Chapter 6.3, using the methods introduced in Chapter 6.3.2.3. Despite the qualitative nature of the determination method, the trend of $\varepsilon_{xx}$ revealed with respect to the waveguide width is consistent with that in the main figure.

Fig. 81 depicts the effect of Ge waveguide height on the $\varepsilon_{xx}$, with respect to the use of the recessed stressor, at the waveguide width of 1 μm. The corresponding substrate trench depth and $SiN_x$ tensile stress are 300 nm and 580 MPa, respectively. It can be found that, for the

waveguides without employing the recessed $SiN_x$ stressor, the average $\varepsilon_{xx}$ increases with increasing waveguide height. However, the $\varepsilon_{xx}$ span also increases, implying a degrading strain uniformity and similar trade-off as manifested in Fig. 80. On the contrary, with the use of the recessed stressor, the average $\varepsilon_{xx}$ slightly decreases with increasing waveguide height, whereas the $\varepsilon_{xx}$ span similarly increases as that without the recessed stressor. Comparatively, the recessed stressor works more effectively on thinner waveguides for the strain magnitude enhancement.

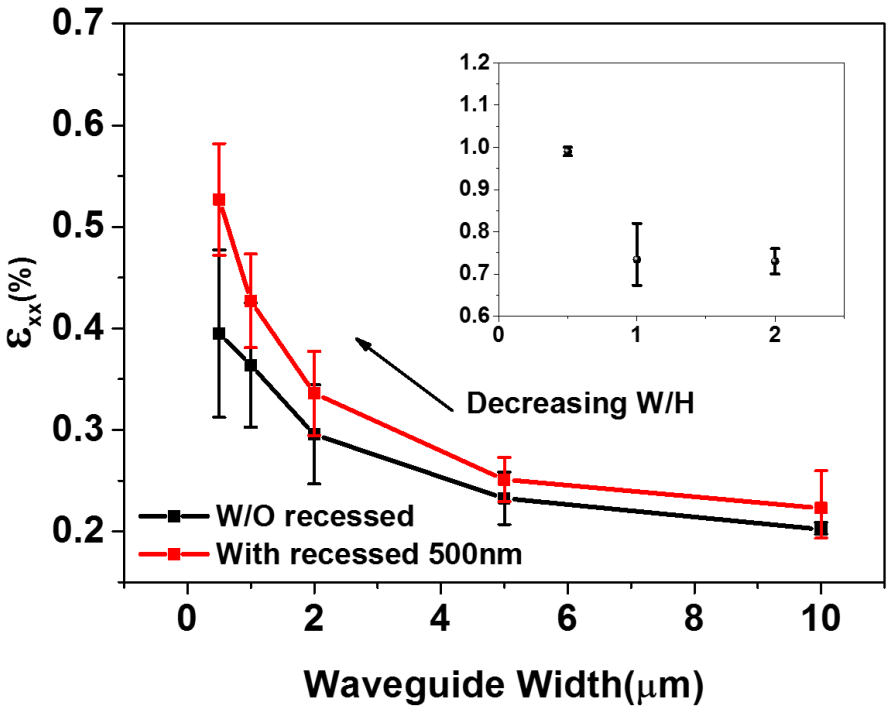


Figure 80 Transverse strain $\varepsilon_{xx}$ as a function of waveguide width, with respect to the use of the recessed $SiN_x$ stressor with a trench depth of 500 nm. Inset shows the $\varepsilon_{xx}$ calculated from the micro-Raman peaks of the fabricated Ge WGOIs with SADE in Chapter 6.3. The axis titles are identical to that of the main figure.

To concisely summarize the effect of the waveguide parameters, a new term named "width-to-height (*W/H*) ratio" is introduced by dividing the Ge waveguide width by the waveguide height. A consensus can be found that, without involving the recessed stressor, the average $\varepsilon_{xx}$ increases

with decreasing *W/H* (as denoted in the figures), while the $\varepsilon_{xx}$ uniformity degrades with decreasing *W/H*.

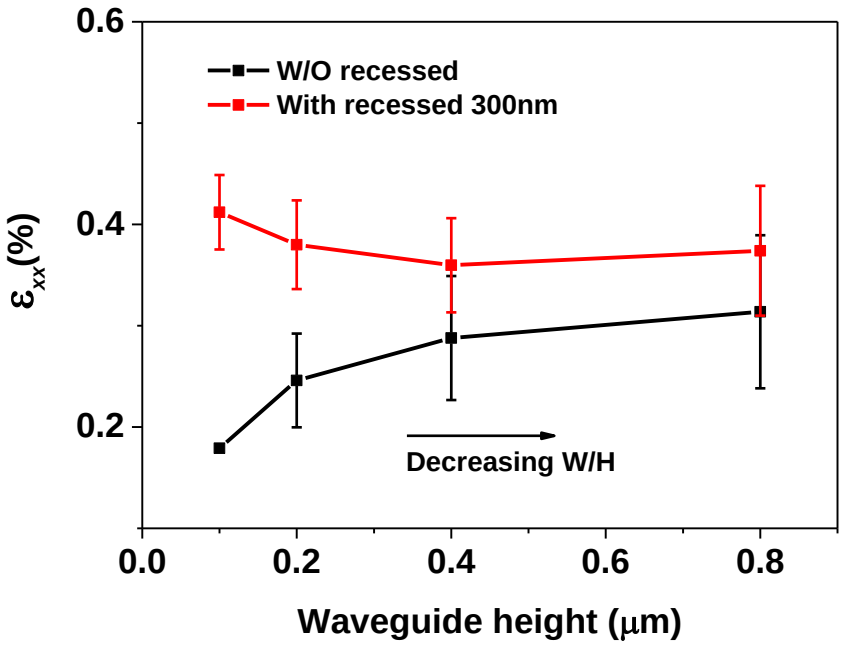


Figure 81 Transverse strain $\varepsilon_{xx}$ as a function of Ge waveguide height, with respect to the use of the recessed $SiN_x$ stressor with a trench depth of 300 nm. The waveguide width is 1 μm.

## 7.5.3 The Effect of Substrate Trench Depth

It has been observed from Fig. 80 that employing the recessed $SiN_x$ stressor could further enhance the strain magnitude and simultaneously improve the strain uniformity. Therefore, Ge WGOIs with varied substrate trench depth were modelled. The waveguides are with a width of 0.4 μm and height of 0.2 μm. The $SiN_x$ stress was kept identical at 580 MPa tensile. Fig. 82 shows the corresponding simulation result. The increase in the trench depth leads to an increase in the average $\varepsilon_{xx}$, which tends to saturate for the trench depth deeper than 300 nm. The average $\varepsilon_{xx}$ is increased by ~30% when a 100-nm trench was adopted, while the increment reduces to ~6% by further increasing the trench depth

from 300 to 500 nm. On the other hand, although decreased due to the use of the recessed stressor, the $\varepsilon_{xx}$ span exhibits no significant relevance on the trench depth shallower than 500nm, with an adverse increase further deeper at 700 nm. This indicates that a shallow trench is sufficient to achieve a substantial average $\varepsilon_{xx}$ enhancement and $\varepsilon_{xx}$ span reduction. Further increasing the trench depth does not prominently contribute to a higher magnitude and uniformity of the tensile strain in Ge.

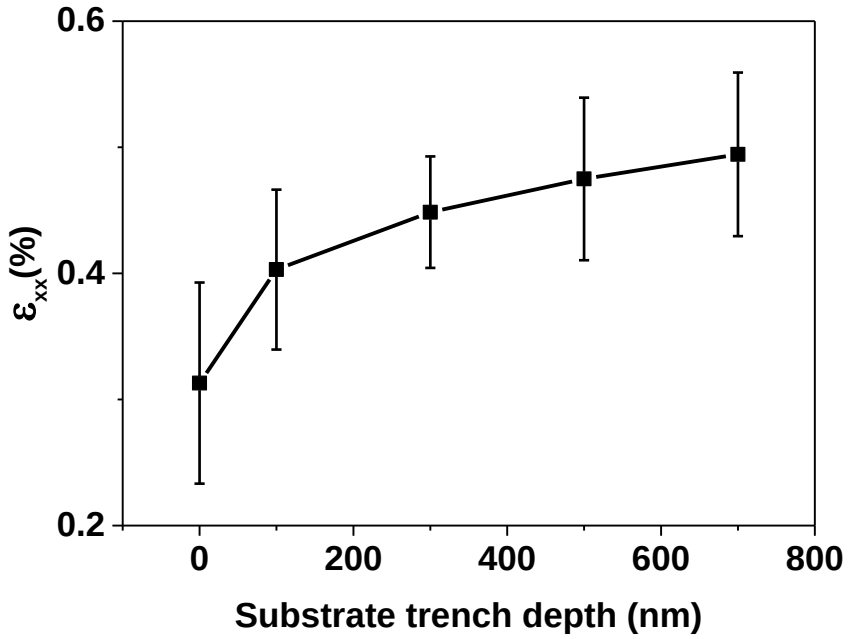


Figure 82 Transverse strain $\varepsilon_{xx}$, with the use of the recessed $SiN_x$ stressor, as a function of substrate trench depth. The waveguides are with a width of 0.4 μm and height of 0.2 μm.

## 7.5.4 Conclusion

To sum up, the effect of $SiN_x$ stress and Ge WGOI structural parameters were studied for a further-enhanced magnitude and uniformity of the transverse strain $\varepsilon_{xx}$ in Ge. It was found that the average $\varepsilon_{xx}$ increases with an increasing $SiN_x$ tensile stress and decreasing Ge waveguide *W/H*. However, both approaches suffer from a degradation on

the strain uniformity, which can be alleviated by employing the recessed $SiN_x$ stressor. The recessed stressor is more effective on a narrower and thinner waveguide for the strain magnitude enhancement. In addition, the trench depth in the recessed $SiN_x$ stressor also plays a role, with the average $\varepsilon_{xx}$ increases with an increasing trench depth. However, it is not advisable to adopt a micron-deep trench, where the improvement is insignificant compared to shallower trenches on the corresponding strain magnitude and uniformity.

Therefore, it is recommended to design the Ge waveguide with a lower *W/H* ratio (optimally at a condition of a narrow width and thinner height) for a maximal tensile $\varepsilon_{xx}$ in Ge. Meanwhile, to alleviate the strain uniformity degradation, it is necessary to adopt the recessed $SiN_x$ stressor with a shallow substrate trench depth at a maximal $SiN_x$ tensile stress. However, the photocurrent of the corresponding photodetectors would be inevitably compromised, due to its minimized Ge waveguide width and height. A further study is required to figure out this trade-off and investigate its limitation on the device design and application. Fig. 83 (a) shows an example of the $\varepsilon_{xx}$ profile of a Ge WGOI at a width and height of 0.4 μm, with the use of the recessed $SiN_x$ stressor at a substrate trench depth of 300 nm. The $SiN_x$ tensile stress is put as 1.5 GPa, a value commonly achieved in state-of-the-art foundries [8]. A ~ 1% average $\varepsilon_{xx}$ can thus be induced in Ge (Fig. 83 (b)), corresponding to an estimated *Γ*-HH and *Γ*-LH bandgap edges at ~ 1670 and ~ 1720 nm, respectively. Therefore, all telecommunication bands are expected to be covered by the corresponding photodetector, with an extension of the absorption

coverage by more than 150 nm. The structure can also support a low-loss mode profile at 1.55 μm (the inset in Fig. 83 (a)), facilitating a high QE for the photodetectors.

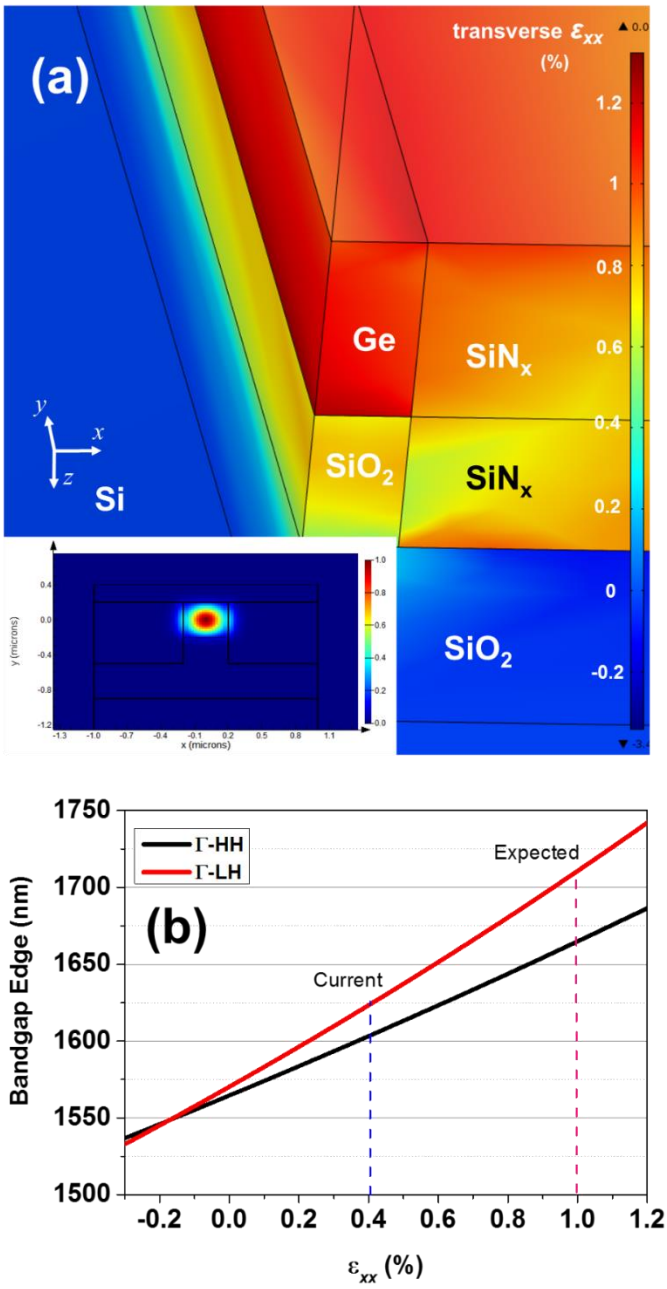


Figure 83 (a) Transverse strain $\varepsilon_{xx}$ profile of Ge WGOI (0.4 μm in width and 0.4 μm in height) with recessed $SiN_x$ stressor (substrate trench depth of 300 nm). The $SiN_x$ stress is 1.5 GPa tensile. Inset shows the mode profile of the identical structure with a propagation loss of 0.004 dB/cm; (b) replica of Fig. 69 (a), labelled with the expected bandgap edges for the Ge WGOI according to the simulated ~ 1% $\varepsilon_{xx}$ in (a).

## 7.6 Conclusion

In this chapter, $SiN_x$-strained GOI MSM PDs were successfully fabricated, potentially for high-efficiency and -bandwidth EPICs integrated at BEOL. The PDs employing a 580 MPa-tensile $SiN_x$ stressor as well as SADE exhibit a ~ 70 nm red-shift of the absorption coverage and a ~ 2× enhancement on the absorption coefficient. The 3dB-bandwidth can reach ~ 5 and ~ 3 GHz, for the PDs with and without the stressor, respectively. Suggestions on the process improvement were made for a better-performing $SiN_x$-strained GOI MSM PD. Lastly, FEM modelling further finds out that a Ge WGOI with a lower *W/H* ratio could enhance the tensile strain in the Ge without changing the sidewall $SiN_x$ stressor, for a Ge photodetector with a longer absorption coverage. The use of the substrate trenches alleviates the strain non-uniformity but it does not further improve with the increasing trench depth.

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# Chapter 8 Conclusion and Future Work

## 8.1 Conclusion

Optical interconnects has been attractive in the past two decades as one of the potential solutions to the conventional metal interconnect bottlenecks. Ge, owing to its CMOS-compatibility and considerable absorption at the tele-communication wavelengths, has been demonstrated as one of the key enablers for photodetectors in EPICs. Recently, GOI has brought researchers' attention due to its technical merits enabling a superior performance in transistors, photodetectors and mid-IR photonic devices, facilitating an advanced EPIC across a broad spectrum ranging from the near- to the mid-IR. Besides, the GOI could realize a 3-D stacking of the EPICs for a dense integration at the BEOL. By comparing among the methods in forming the GOI, the bonding and layer transfer approach via etch-back stands out, mainly because of its low thermal budget and scalability to all wafer sizes. However, the existing GOI photodetectors suffer from a poor QE due to their lateral contacts that are inefficient in collecting the photon-generated carriers deep down in the material. Therefore, this thesis focuses on the study of the GOI photodetectors towards a higher QE for the advanced EPICs.

In Chapter 3, two approaches were proposed, namely realizing a vertical *p-i-n* structure and inducing a uniform tensile strain in Ge. The vertical *p-i-n* structure could increase the absorption thickness, while the tensile strain could shrink the Ge bandgap for a higher absorption coefficient, both facilitating a higher QE. The tensile strain can be

generated by CMOS-compatible $SiN_x$ stressor for the ease of monolithic integration.

Chapter 4 attempted the first solution, namely the fabrication and characterization of the vertical *p-i-n* structure on a GOI platform, by ion-implanting $BF_2^+$ followed by $As^+$ into the Ge layer, along the bonding and layer transfer (etch-back) process in forming the GOI. Abrupt *p*- and *n*-doping profiles with minimal diffusion were confirmed. Excellent crystal quality of the transferred Ge layer, comparable with that of the bulk Ge, was also exhibited.

Chapter 5 illustrated the development and characterization of the normal-incidence photodetectors on the GOI platform, based on the vertical *p-i-n* structure. The devices reveal a dark current density of ~ 47 $mA/cm^2$ at -1V and a responsivity of 0.39 A/W at 1550 nm under -2 V. The dark current density and responsivity are prominently improved, compared to that of the existing GOI photodetectors. A high IQE of ~ 97% demonstrates the superiority of the vertical *p-i-n* structure in collecting the photon-generated carriers. The device design is also compatible with other "on-insulator" platforms with diversified semiconductor (e.g. III-V, GeSn) and intermediate insulator (e.g. $SiN_x$, $Al_2O_3$) materials.

Chapter 6 used a patented approach to induce a uniform tensile strain in the Ge WGOI, utilizing a recessed $SiN_x$ stressor, for integrated photodetectors at BEOL with an enhanced QE at longer wavelengths. The recessed stressor significantly enhances the strain magnitude and simultaneously improves the strain uniformity, from both theoretical

simulation and experimental micro-Raman measurements. A ~ 0.7% tensile strain was also determined. The recessed stressor is also applicable to other semiconductors, such as III-V and 2D materials, that are bandgap-tunable under its induced strain.

Chapter 7 demonstrated the MSM photodetectors developed on the $SiN_x$-strained Ge WGOI. Despite the imperfect fabrication, the devices employing the recessed $SiN_x$ stressor with a tensile stress of 580 MPa exhibit a ~ 70 nm red-shift of the absorption edge and a ~ 2× enhancement on the QE at the *L*-band. FEM modelling further tells that lowering the waveguide width-to-height ratio could help maximizing the tensile strain for a further extension of the absorption coverage. The devices could potentially fit for high-efficiency and -bandwidth EPICs integrated at BEOL.

To sum up, the GOI photodetectors developed by approaches of forming vertical *p-i-n* structure and recessed $SiN_x$ sidewall stressors, though not fully optimized, have demonstrated a significant QE enhancement and shown great promises for integrated optical transceivers/LiDAR systems with a higher sensitivity. A lower minimal optical input power is thus allowed, which would also save the energy spent on the electrical amplification circuits (e.g. TIA) for a commensurate electrical response. In addition, the recessed $SiN_x$ stressor approach leads to a considerable redshift of the absorption coverage, facilitating more channels for data transmission under the WDM configuration. The high-performance photodetectors can also be potentially integrated with Ge-based CMOS and mid-IR photonics for advanced EPICs on GOI

platform. The two approaches are also transferrable to other semiconductor materials and systems for diversified optoelectronic applications.

## 8.2 Future Work

Apart from the discussion in Chapter 7.4, the future work can be plenty to further improve the performance of the GOI photodetectors in this thesis. For the normal-incidence vertical *p-i-n* photodetectors, as discussed in Chapter 5.3.2.1, an oxygen annealing at 850$^{o}$C for 4 hours can be performed on the GOI to further reduce its threading dislocation density to ~1×10$^{6}$ cm$^{-2}$ [1], which is expected to decrease the SRH-generated dark current and minimize the non-radiative recombination of the photon-generated carriers. In addition, to further increase the absorption path, a waveguide-integrated photodetector can be developed on the GOI. Amorphous Si or $SiN_x$ material can be inserted as the waveguide beneath the Ge, along with the bonding and layer transfer process in forming the GOI, to facilitate an evanescent coupling. This device would be very useful for high-performance optical transceivers integrated at the BEOL.

The work of the recessed $SiN_x$ stressor can be further extended for integrated Ge EA modulator arrays. Both the highly-tensile and -compressive stressor can be applied on different Ge waveguides arranged in an array to tune their bandgap edges for a broadband optical modulation. Since EA modulators are very low in energy consumption,

this concept can be promising to meet the future demand of small-form-factor and low-energy integrated photonics.

Last but not least, the recessed stressor can also be applied on other semiconductor materials for bandgap-related applications. For example, it can be applied on direct-bandgap III-V material arrays to locally tune its emission wavelength. It can also similarly realize an array of bandgap-varied waveguides, as that discussed in the previous paragraph, for optical modulation and detection. Potential materials include II-VI and III-V compound semiconductors, group IV compounds such as GeSn and SiGeSn, 2D materials such as graphene and transitional metal dichalcogenides and many more.

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