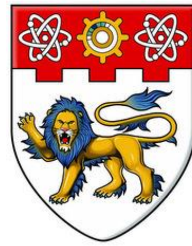

NANYANG
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DEVELOPMENT OF 3D ELECTRO-OPTICAL INTEGRATION BASED ON SILICON PHOTONIC TSV INTERPOSER

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SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

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DEVELOPMENT OF 3D ELECTRO-OPTICAL INTEGRATION BASED ON SILICON PHOTONIC TSV INTERPOSER

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Summary

Silicon photonics has been intensively researched and investigated as it provides a low-cost and power efficient solution for next generation interconnect technology based on on-chip, chip-to-chip, and long-haul optical communication. A multifunctional platform requires photonic integrated circuits (PICs) and complementary-metal-oxide-semiconductor (CMOS) circuits to be integrated in the same system. To achieve advantages of power efficiency and bandwidth densities of PIC, monolithic integration of CMOS circuits and silicon photonic functional blocks has been explored recently. However, this approach has some limitations, such as increased number of mask layers, sophisticated co-integration processing skills on the same silicon chip, huge size mismatch between CMOS and photonic functional blocks, and therefore resulted in low overall yield. In this work, the separate fabrications of silicon photonic devices and CMOS circuits are designed and experimentally demonstrated, and their integration is achieved using through-silicon-via (TSV) and flip-chip bonding technology, which is a three-dimensional (3D) integration scheme. With the scenario of interconnection along vertical dimension, the 3D integration scheme provides a shorter communication routing and lower power dissipation, and therefore has becoming one promising solution for continued scaling of tera-scale communication systems.

In this thesis, the technology options/integration strategies of electro-photonic integration based on silicon-on-insulator (SOI) photonic interposer featuring TSVs and flip-chip bonding technology are proposed and investigated. An SOI photonic TSV interposer for the purpose of inter/intra-chip optical/electrical communication

interface routing is proposed, in which TSVs are fabricated in an SOI photonics wafer. In this 3D integration scheme, high density metal lines and micro-bumps in the flip-chip bonding technology provide interconnection among guest dies, and TSVs communicate with I/O ports on the organic package (e.g., fc-BGA) and/or printing circuit board (PCB), whereas silicon photonic devices deal with huge amount of data transmitted in from and out to the external world. TSV is a key technology in the 3D integration, which provides flexible and compact electrical/physical connectivity between different chips.

The first investigation in this thesis is the TSV-induced impact on the optical performance of photonic devices. To realize compact scaling, which is one of the important benefits of 3D integration, high-density TSVs are situated close to the silicon photonic devices in the photonic interposer. One of the critical limitations in the compact 3D photonics integration is the TSV-induced stress, which affects the performance of silicon photonic devices integrated in interposer, particularly for the stress-sensitive devices, such as silicon photonic ring resonators. The impact of TSV-induced stress is analyzed, and the model of TSV-induced stress distribution in the silicon waveguide in SOI photonic interposer is built. The model of the change in effective-refractive-index caused by stress-induced changes of refractive index tensors is presented. Silicon photonic double-cascaded ring resonators integrated with TSV structures on an SOI platform are fabricated and characterized to demonstrate the impact of TSV-induced stress. The characterization results are statistically analyzed with the impact of fabrication non-uniformity eliminated. Finally, a stress aware design framework and a TSV keep-out-zone (KOZ) for the silicon photonic ring resonator are proposed. A compact scaling of SOI photonics

interposer is ultimately achieved.

The second part of design and fabrication in this thesis is a silicon photonic interposer with monolithically integrated active/passive photonic devices featuring Cu-based back-end-of-line (BEOL), including Mach-Zehnder Interferometer (MZI) optical modulators, photodetectors (PD) and thermo-optically (TO) tunable arrayed waveguide gratings (AWG). From the integration and packaging perspective, CMOS-compatible Si photonics technology is becoming one of the most promising technologies to realize very large-scale complex photonics-CMOS integration system. To take advantages of the CMOS semiconductor technology, such as high integration density, low-cost and good reliability, the progress of silicon photonics technology should further maintain standardization and adherence to the established CMOS technology methodologies. CMOS semiconductor industry has been progressing from Al-based BEOL interconnects to Cu-based at technology nodes beyond 0.18 μm. Due to Cu's higher conductivity and lower skin-effects, Cu-BEOL is also expected to enable better RF performance and higher I/O density in silicon PICs and active devices. Furthermore, Cu-BEOL based Si-photonics provides the toolboxes for the Si photonics-CMOS integration strategy based on Si photonics interposer featuring TSVs and flip-chip bonding technology.

As important active devices, MZI modulators and Ge PDs monolithically integrated in this interposer featuring radio-frequency (RF) traveling-wave electrode (TWE) via Cu-BEOL is explored with a higher speed. A latticed Cu surface pattern is designed for the Cu-BEOL. The modulator is designed with Cu-TWE for better RF performance and doping compensation for reducing the optical transmission loss

of the phase shifter caused by ion implantation. Discrete contact plugs to Ge PD are designed for reducing Cu-induced optical loss and thus improving the responsivity. The 3-dB bandwidths for both stand-alone modulators and PDs on the integrated wafer are 37 GHz and 33.7 GHz, respectively. A transmission data rate of 30 Gbps of the interposer is achieved, which is limited by the measurement setup. It is demonstrated that Cu-TWE with low resistance provides better RF performance with higher bandwidth than Al-based active devices. Cu application can further improve the integration of silicon photonic devices and CMOS circuits in the future. The Cu-BEOL based RF silicon photonic devices toolbox for high performance photonics-CMOS integration has been established.

As the key passive photonic device, AWG multiplexer/demultiplexer (MUX/DeMUX) integrated in this interposer is investigated in this thesis. The increasing demand for bandwidth in optical communications has increased the interest for dense-wavelength-division-multiplexing (DWDM) technology. This demand requires high performance wavelength MUX/DeMUX with more channels and small channel spacing. At the same time, one major issue in using a high-index contrast platform such as SOI wafer for photonic devices is its sensitivity to dimensional variations. Dimensional deviations of the devices will cause a wavelength shift in the spectral response. AWGs are larger in size and thus more vulnerable to different sources of dimensional variations, such as the variation in the silicon layer thickness, process non-uniformity, and mask error. Therefore methods for stabilizing and tuning, such as precise positioning of AWGs wavelength, or compensation for optical wavelength drift, are of great interest. By taking advantage of the thermo-optic (TO) effect in Si, thermal tuning method can

be utilized. A tunable silicon AWG based on TO effect has been demonstrated for the first time in this thesis. The thermal performance simulation shows that a uniform heating is achieved by the heater design, while the experiment results show that above 600 GHz channel tunability is achieved.

Finally, an SOI photonic TSV interposer is designed, modeled and fabricated, in which TSVs, nano-tip waveguide coupler, TO tunable silicon AWG, MZI modulator and Ge PD are monolithically integrated featuring Cu-BEOL. A 3D electro-photonic TSV integration module, including this photonic TSV interposer and electronic chip using TSVs and flip-chip bonding technology, are modeled and experimentally demonstrated and characterized. Cu transmission lines are fabricated on the electronic chip using Cu-RDL process. The fabrication process of the 3D electro-photonic TSV integration including the 100 μm-thick photonic TSV interposer and the elecronic chip using TSVs and the flip-chip bonding technology is proposed and developed. The characterization results show that 40 Gbps-data rate is achieved for the high speed photonic device, and 800 GHz channel tunability is achieved for the TO tunable silicon AWG in the 3D electro-photonic TSV integration. From modeling and experimental demonstration, this 3D electro-photonic TSV integration module provides the toolboxes for the 3D Si photonics-CMOS TSV integration strategy based on Si photonics interposer featuring TSVs and flip-chip bonding technology.

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List of Symbols

λ	wavelength
ρ	resistivity
δ	skin effect
μ	permeability
σ	conductivity
ε	permittivity (dieletric constant)
ε_{reff}	effective dieletric constant
γ	complex microwave transmission constant
η_i	quantum efficiency
c	light speed in free space
e	electron charge
f	frequency
h	Planck's constant
n_{eff}	effective refractive index
n_g	group index
n_{opt}	optical refractive index
n_{μ}	microwave refractive index
Z	characteristic impedance

LIST OF ABBREVIATIONS

2D	Two-dimensional
3D	Three-dimensional
AC	Alternating current
AWG	Arrayed waveguide grating
BCB	Benzocyclobutene
BEOL	Back-end-of-line
BOX	Buried oxide
BS	Backside
BPF	Band pass filter
CG	Concave grating
CMOS	Complementary-metal-oxide-semiconductor
CMP	Chemical mechanical polishing
CPW	Coplanar waveguide
CTE	Codfficient of thermal expansion
DC	Direct current
DCA	Digital Communications Analyzer
DRAM	Dynamic random access memory
DRIE	Deep reactive-ion etching
DUT	Device-under-test
DWDM	Dense-wavelength-division-multiplexing
ECP	Electrochemical plating
EDA	Electronic design automation

EDFA	Erbium-doped fibre amplifer
EHP	Electron-hole pair
EIC	Electronic integrated circuit
EO	Electro-optical
EPIC	Electronic-photonic integrated circuit
ER	Extinction ratio
FDTD	Finite-difference-time-domain
FEA	Finite element analysis
FS	Frontside
FSR	Free spectral range
GSG	Ground-signal-ground
I/O	Input/output
IC	Integrated circuit
ICP	Inductively coupled plasma
KOZ	Keep out zone
LA	Limiting amplifier
LCA	Lightwave Component Analyzer
LPD	Lateral photodetector
MMI	Multimode interference
MPW	Multi-project-wafer
MUX/DeMUX	Multiplexer/demultiplexer
MZI	Mach-Zehnder interferometer
NRZ	Non-return-zero
PBO	Polybenzobisoxazole

PCB	Printing circuit board
PD	Photodetector
PECVD	Plasma enhanced chemical vapor deposition
PI	Polyimide
PIC	Photonic integrated circuit
PRBS	Pseudorandom binary sequence
PVD	Physicalvapor deposition
RC	Resistance-capacitance
RDL	Redistribution layer
RF	Radio frequency
RIE	Reactive-ion etching
RLGC	Resistance-Inducance-Conductance-Capacitance
RTA	Rapid thermal anneal
SEM	Scanning electron microscope
SOI	Silicon on insulator
TCB	Thermal compression bonding
TE	Transverse-electric
TEM	Transmission electron microscope
TEOS	Tetra-Ethyl-Ortho-silicate
TIA	Transimpedance amplifier
TIR	Total internal reflection
TO	Thermo-optic
TSV	Through silicon via
TWE	Traveling-wave electrode

UBM	Under bump metal
UHVCVD	Ultra-high vacuum chemical vapor deposition
VPD	Vertical photodetector
WDM	Wavelength-division-multiplexing

Chapter 1 Introduction

1.1 Background

1.1.1 From Moore's Law to "More than Moore"

An incredible increase in the functionalities of computing systems have been seen in the past few decades, and this capability has been driven by the dimensional scaling of the semiconductor devices and the integrated circuits (IC), from millimeters to nanometers today. This scaling has enabled the transistors density on a single chip to grow at a geometric rate correspondingly, doubling every 18 months, which is referred to as Moore's Law [1]. Nowadays, some serious roadblocks exist in continuing this same trend [2]. The first one is the limitation in lithographic scaling. Moreover, the power densities will not ensure system reliability even if the lithographic scaling would continue. Hence, researchers are looking for soultions for the dimension scaling limitations beyond the 20 nm technology node. In addition, the resistance-capacitance (RC) delay and the power dissipations issues in the interconnect links is of concern when the total interconnects length becomes longer due to the increasing number of devices and the chip size.

Instead of the conventional two-dimensional (2D) geometrical scaling, the possibility in the vertical dimension has been exploited, known as the three-dimensional (3D) integration scheme, as shown in Figure 1.1. The 3D integration enables the vertical interconnects and communications in order to meet the increasing demands of functionality diversification, which is referred to as "More

than Moore" [3].

3D integration scheme and technology offer dimensional scaling and improved system performance. The main advantages of the 3D integration scheme can be summed up as follows [57]: (1) small form factor and high circuit density, (2) decreased interconnect distances between regions of a chip, decreased interconnect delay and parasitic power dissipation, (3) dramatically increasing the number of interconnects, and thus enhancing the communication bandwidth between chips, and (4) potentially allows the integration of the heterogeneous functionalities, technologies and materials. Compared with 2D integration, the difficulties in 3D integration are the development of an integration processing, avoiding the TSV-induced impact on the photonic device under compact scaling, and the co-design of different functionalities. In other words, fabrication difficulty and lack of 3D electronic design automation (EDA) tool are the main disadvantages of the 3D integration technology at present.

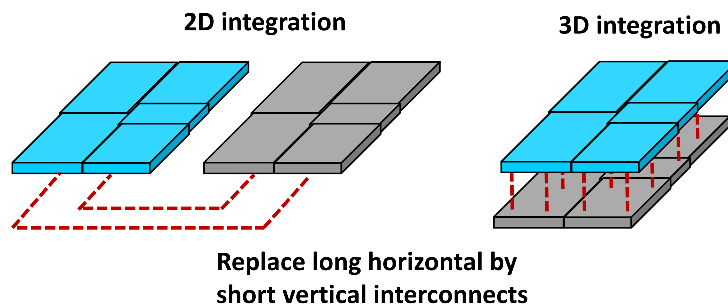


Figure 1.1 Long horizontal interconnects in the conventional 2D scheme replaced by the vertical interconnects in the 3D scheme.

1.1.2 3D Electronic-Photonic Integration

Silicon photonics has been intensively researched and developed as it provides low-

cost and power efficient solution for next generation interconnect technology based on on-chip, chip-to-chip, and long-haul optical communication [4]-[12]. A multifunctional platform requires photonic integrated circuits (PICs) and complementary-metal-oxide-semiconductor (CMOS) circuits to be integrated in a same system. To achieve advantages of power efficiency and bandwidth densities of PICs, monolithic integration of CMOS circuits and Si photonic functional blocks has been explored and demonstrated recently [13]-[23]. However, this approach requires increased number of mask layers to fabricate CMOS-integrated Si photonics chips, and it also needs sophisticated co-integration electronic design automation (EDA) tool and processing skills to integrate them together on the same silicon chip. Consequently, it is difficult to achieve high overall yield [24]-[26]. Moreover, the huge size mismatch between CMOS and photonics functional blocks is another disadvantage of the monolithic integration approach. The large footprint of Si photonics blocks can easily consume most of the die space, leaving little space for other electronics functional blocks, e.g., digital, radio frequency (RF), and high-voltage, to be placed. Some researchers [24], [25], [27] have proposed to separate the fabrication of Si photonics and CMOS electronics, and finally integrate them together using through-silicon-via (TSV), which is a 3D integration scheme. Scanning electron microscope images of monolithic integration of PIC and electronic IC (EIC), and the 3D electronic-photonic IC (EPIC) are shown in Figure 1.2 [28].

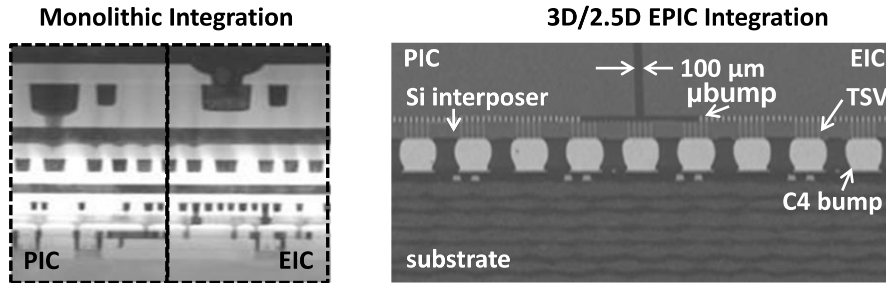


Figure 1.2 Monolithic integration and 3D/2.5D EPIC integration [28].

1.2 Motivations

1.2.1 Advantages of 3D TSV integration

- ***High circuit density and small form factor***

One crucial advantage is the increased circuit density enabled by 3D integration, without necessary 2D lithography scaling effort. Samsung Electronics has realized a 16 Gbit memory which consists of 8 vertically stacked flash dies [29], using 3D integration scheme, as shown in Figure 1.3. Each die is 50 µm-thick and with a capacity of 2 Gbit. The 8 layers stacked device is even thinner than the original wafer before grinding. The total length of the global interconnects is obviously significantly reduced due to replacing the conventional planar interconnecting wires with the vertical interconnects, which results in siginificant improvement in the performance due to the reduced resistance.

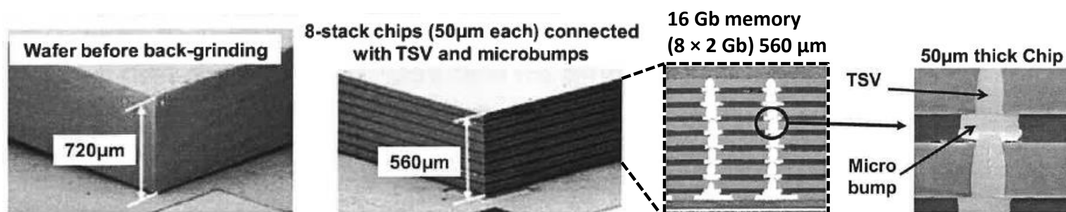


Figure 1.3 Samsung Electronics' 8 stacked flash memory using 3D integration scheme [29].

Toshiba initiated the world's first CMOS image sensor in 2008 using 3D integration scheme, in which TSVs were used for replacing the conventional wirebonding to achieve small form factor, as shown in Figure 1.4 [30]. A 36% reduced area was needed as compared to that previously required for wirebonding to the substrate.

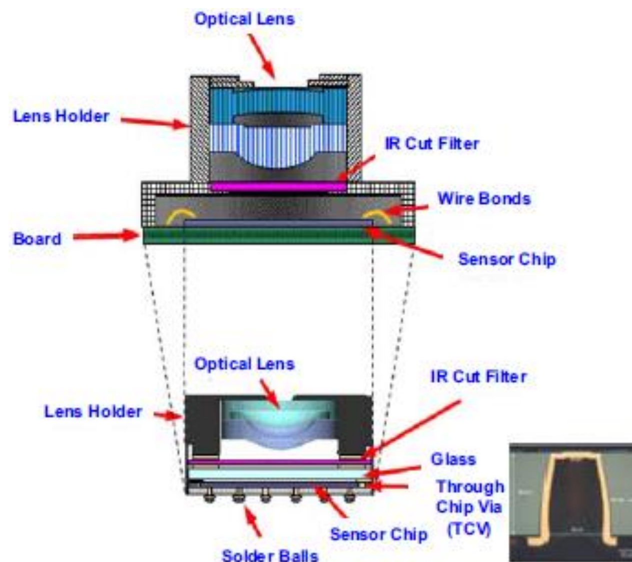


Figure 1.4 Toshiba commercial image sensor with through-chip-via (TCV) (=TSV) (2008). A 36% area reduction has been achieved [30].

- ***RC delay improvement, bandwidth enhancement with wide input/output (I/O) interfaces, and low power dissipation***

Through replacing the long horizontal interconnects by the short vertical interconnects, the decreased global interconnects leads to the decreased line resistance. Together with the low parasitic capacitance effect due to the dimensional scaling down, the RC delay and power dissipation can be improved. 3D integration implementation provides the capability to stacking the memory chips vertically and allocating the memory chips on top of the logic chip. In this case, the bandwidth

and I/O channels can be extended. Figure 1.5 illustrates a 3D integrated memory by Micron with 10 times speed improvement compared to the module using planar process [31].

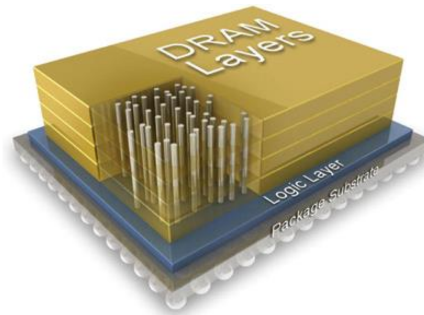


Figure 1.5 Hybrid Memory Cube, Micron. 128 Gbps compared to the 12.8 Gbps DDR3 fabricated using a planar process [31].

- ***Heterogeneous integration and adding-on more functionalities***

Since the monolithic integration requires sophisticated co-design EDA tool, the increased number of mush layers and complicated processing skill, there is a long way to go. Moreover, the mismatch between the footprints of the different functional blocks is a limitation in functionalities enhacement and the form factor improvement. 3D integration scheme provides easier separated fabrication processes, the separated design of each functional block, and therefore low cost and high overall yield, compared with the monolithic integration. Heterogeneous integration and more functionalities can be implemented in the 3D integration scheme.

1.2.2 Advantages of 3D integration based on TSV interposer over wirebonding

Compared with the 3D TSV integration, wirebonding was used in the conventional

3D integration, as shown in Figure 1.6 [32], [33]. The comparision between TSV integration and wirebonding interconnect is shown in Table 1.1. Due to hundreds times reduction in interconnects length, cross-section area, resistance, MOS capacitance and inductance compared with conventional wirebonding, TSV has the potential capabilities in improving power consumption, circuit density, bandwidth, and propagation delay. Furthermore, a cooling system can be designed around TSV to improving heat dissipation.

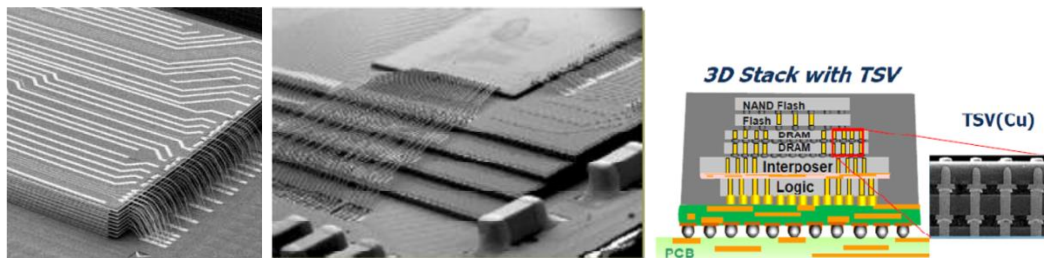


Figure 1.6 Conventional 3D integrated flash using wirebonding (Samsung), compared with 3D TSV integration (Samsung) [32], [33].

Table 1.1 Comparison between wirebonding and TSV [34], [35].

Performance	**Wirebonding**	**TSV**
Interconnects length	long (~mm)	short (~10-100 μm)
Propogation delay	significant	short
Resistance	high	reduced (500~1000 times lower than wirebonding) on the order of 1~10 mΩ/μm (skin effect at high frequency)
MOS capacitance	high	reduced (500 times lower than wirebonding) on the order of 0.1 fF/μm
Inductance	high	reduced (500 times lower than wirebonding) on the order of 0.1 pH/μm
Power consumption	high	reduced
Cross-sectional area	large (~100 μm)	small (~1 -10 μm)
density	low (~1/mm^2)	high (~10^4/mm^2)
Heat dissipation	poor	good (cool system)

1.2.3 Proposed 3D Electronic-Photonic Integration

In this thesis, the technology options/integration strategies of silicon electronic-photonic integration are investigated. Separate fabrication of the Si photonic devices and the electronic devices, and the 3D integration of them using on silicon-on-insulator (SOI) photonic interposer featuring TSVs and flip-chip bonding technology are explored and experimentally demonstrated as a 3D electronic-photonic integration scheme.

An SOI photonic TSV interposer for the purpose of inter/intra-chip optical/electrical communication interface routing is investigated and fabricated, in which TSVs are fabricated in an SOI photonics wafer. TSVs serve as high-aspect-ratio vertical interconnects which provide flexible and compact electrical/physical connectivity between different chips through the Si photonic chip [28], [36]. As shown in Figure 1.7, in this proposed 3D integration scheme, high density Cu wirings and micro-bumps in the flip-chip bonding technology provide interconnection among guest dies, and TSVs communicate with input/output (I/O) ports on the organic package (e.g., fc-BGA) and/or printing circuit board (PCB), whereas silicon photonic devices deal with huge amount of data transmitted in from and out to the external world. TSV is a key technology in the 3D integration, which provides flexible and compact electrical/physical connectivity between different chips. With the scenario of interconnection along vertical dimension, the 3D integration scheme provides shorter communication routing, lower power dissipation and small form factor, and therefore has become one promising solution for continued scaling of tera-scale communication systems.

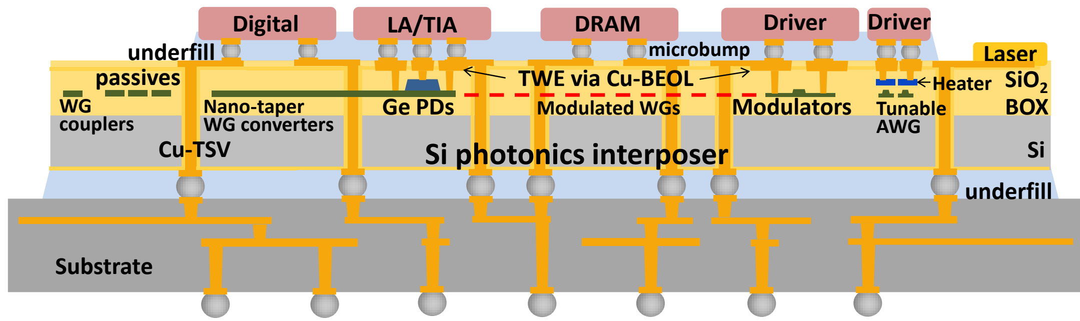


Figure 1.7 Schematic of SOI photonic TSV interposer in 3D electronic-photonic integration system (not to scale).

1.2.4 Cu Metallization/BEOL of Silicon Photonics

Silicon photonic devices have a promising future in the application of optical communications, due to their low cost, high performances and compatibility with the existing CMOS technology [37]-[40]. Silicon photonics based optical interconnects offer high bandwidth density and low power consumption compared with the traditional metal wire interconnects in high speed communication and computing system. CMOS-compatible silicon photonics technology is becoming one of the most promising candidates to realize very large-scale complex photonics-CMOS integration system. To take advantage of the CMOS technology, such as high integration density, low-cost and good reliability, the progress of Si photonics technology should further maintain standardization and adherence to the established CMOS technology methodologies. CMOS semiconductor industry has been progressing from Al-based BEOL interconnects to Cu-based at technology nodes beyond 0.18 μm. For the same reasons of Cu's higher conductivity and lower skin-effects, Cu-BEOL metallization is also expected to enable higher speed with less power consumption, and its better RF performance in Si photonic active devices

and integration helps to realize PIC with high I/O density. Furthermore, Cu-BEOL based Si-photonics provides the toolboxes also for the Si photonics-CMOS O/E IC integration strategy based on Si photonics interposer via TSVs [41] and/or flip-chip bonding.

1.2.5 Photonic devices in the SOI photonics TSV interposer

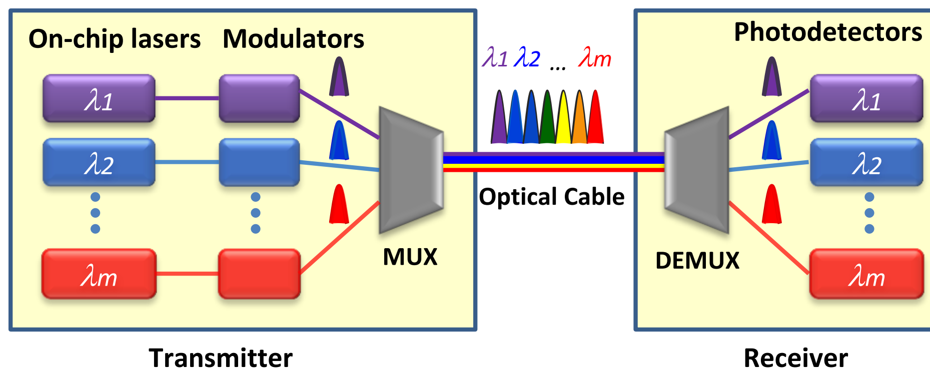


Figure 1.8 A optical wavelength-division-multiplexing (WDM) communication system [42].

The communication bandwidth is expected to be double improved every 18 months [42], [43]. The conventional electrical interconnects will impose limitations to the communications network, including large power consumption and the resulting thermal dissipation, and the inherent electrical bandwidth limits as well [42]. These limitations are related with the Cu interconnects dimensional scaling and the RC time constant. The advantages of optical interconnects includes broad bandwidth and potential low power consumption [44]-[46]. Besides the conventional fiber-optic communication systems, silicon optical communication is now becoming promising technology in the optical interconnect applications [46]-[48]. Figure 1.8 illustrates an optical interconnect system [42]. Multi-channel wavelength-division-

multiplexing (WDM) technology gives a way to increase the data communication capacity further. The key silicon components, including modulators, photodetectors (PD), arrayed waveguide grating (AWG) multiplexers/demultiplexers (MUX/DeMUX), and resonators are investigated and experimentally demonstrated in the SOI photonic TSV interposer in this thesis.

Research in the key active devices, Si modulators and Ge PDs integrated in a Si photonics platform, has made some progress. Some works have been published with 25 Gbps [49] and 30 Gbps-data rate [50]. IME nano photonics group has also reported a 40 Gbps Si PIC [51]. These works usually adopt the Al-BEOL. A 25 Gbps Si photonics platform with Cu interconnects was reported by STMicroelectronics [52]. As the key MUX/DeMUX component for multi-channel optical communications, silicon AWGs have been actively researched [53]-[55] as will be described in section 2.8 in Chapter 2.

1.2.6 Challenges

Even with the benefits sumed up above, just like any other infancy technologies, 3D silicon electronic-photonic integration also faces challenges: such as TSV fabrication in the SOI photonic wafer, impact of TSV-induced thermo-mechanical stress on the photonic devices performance, Cu metallization of the silicon photonic devices for the CMOS-compatible integration purpose, thin wafer bandling technology for the silicon photonic wafer with fiber coupling deep trenches, development of fabrication process for the 3D electronic-photonic integration, flip chip bonding alignment, and electro-optical (EO) testing of the 3D system. All these issues need to be resolved in order to bring the 3D silicon electronic-photonic

integration as a laboratory proposal to semiconductor industry.

1.3 Scope of Research and Contributions

This thesis provides a comprehensive investigation on the design, simulation, fabrication and characterization of the 3D silicon electronic-photonic integration system. The scope and objectives are listed below:

(1) TSV fabrication on SOI wafer, and the TSV keep-out-zone (KOZ) study for silicon photonic device.

(2) Design and fabrication of silicon photonic interposer featuring Cu-BEOL.

- SOI photonic interposer integrated with key components in the optical interconnect link: modulator, PD, tunable AWG MUX/DeMUX.
- Design of the silicon modulator, the Ge-on-Si PD and the tunable silicon AWG.
- Cu traveling-wave electrode (TWE) design, modeling and fabrication of high speed active photonic devices, including modulator and PD.
- Cu metallization of the photonic interposer via Cu-BEOL.

(3) Microwave modeling of the 3D silicon electronic-photonic integration based on photonic TSV interposer.

(4) Fabrication and characterization of the 3D silicon electro-photonic integration system.

- Process integration design of the 3D electronic-photonic integration system.
- Thin wafer handling of the SOI photonic wafer with fiber coupling deep trenches.

- Design and fabrication of the microwave electronic chip.
- Electronic-photonic chip-to-chip flip-chip bonding.
- EO/OE characterization of the 3D integration module.

1.4 Organizations

The organization of this thesis is listed as follows:

In chapter 2, literature review of the state-of-the-art 3D TSV integration system is presented. Basic TSV process flow and the electrical model are introduced. Fundamental principles of the microwave design of the RF TSV, RF transmission line and Cu-TWE of the active components are studied. Fundamental principles of the passive components (ring resonator and AWG) are presented.

In chapter 3, TSV fabrication process on SOI wafer is provided. TSV KOZ of the SOI photonic device are studied and characterized.

In chapter 4, SOI photonic interposer featuring RF TWE via Cu-BEOL is investigated, in which modulator, PD and tunable AWG are designed and monolithically integrated. The fabrication process are designed and experimentally demonstrated.

In chapter 5, modeling, fabrication and characterization of 3D silicon electronic-photonic integration based on silicon photonic TSV interposer are explored. Characterizations of the 3D integration module are presented.

In chapter 6, summary, conclusion and future work are presented.

Chapter 2 Literature review and device fundamental principles

2.1 The state-of-the-art 3D TSV integration

The paper entitled "Three-dimensional IC trends" published in 1986 [56] opend the era of the 3D IC integration. 3D integration was expected to provide several advantages, such as parallel processing, high-speed operation, high packing density or super large integration, and multifunctional operation. "Via-hole" was proposed to realize the vertical interconnects in the 3D integration. An image processor in a 3D integration structure was expected to be realized with video sensor on the top layer, then an analog-to-digital converter, logical unit, memory and central processing unit (CPU) in the lower layers. Nowadays, world's first CMOS image sensor initiated by Toshiba in 2008 makes this idea more realizable. A 36% integration area reduction is realized by TSV.

Industrial Technology Research Institute (ITRI) proposed a roadmap for 3D integration application and the predicted marketing time as shown in Figure 2.1 [57]. 3D IC integration based on passive TSV interposer was developed from 2010, and embedded fluidic microchannel to thermal dissipation is expected to be realized in 2018. 3D integration based on active TSV interposer was developed from 2010, and integration of memory, logic, and CPU is expected to be realized by 2018.

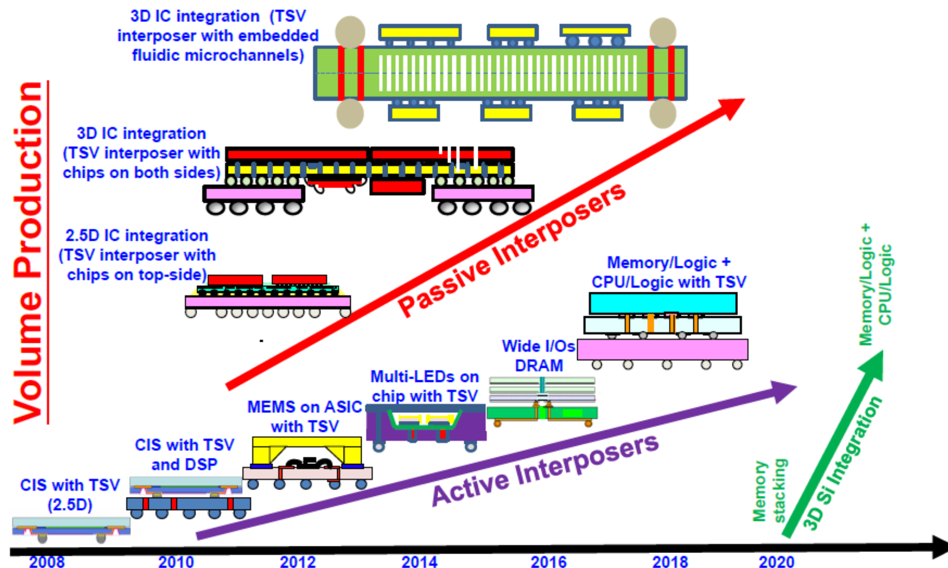


Figure 2.1 3D integration roadmap by ITRI [57].

Samsung demonstrated 3D stacking of memory and logic using TSVs and microbumps in 2006 [58], and the microscope image is shown in Figure 2.2. More I/O interfaces between the memory and logic chip are expected from TSV and a much smaller system can be obtained without wirebonding. The logic chip can be viewed as an active interposer in this 3D scheme. Samsung also reported 8 layer stacking memory with a capability of 8 × 2 Gbit as shown in Figure 1.3. Compared with the conventional 2D scheme, the package size is reduced by 35%, the power consumption is reduced by 50%, and the bandwidth is increased by 8 times.

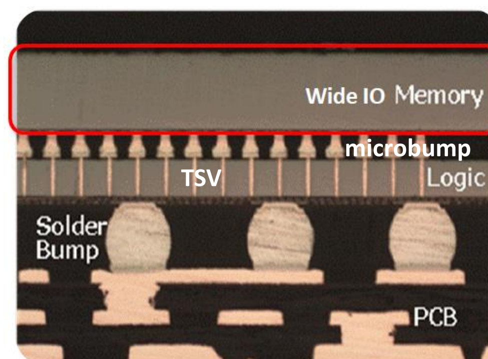


Figure 2.2 Microscope image of Samsung's 3D integrated memory [58].

TSV interposer served as carrier or substrate in the 2.5D/3D integration can enable integration of chips with fragile mechanical stability. Chips are bonded to the intermediate interposer before their final allocation in a standard package. High density interconnects interface/routing through TSV and metal wires are designed in the interposer. Figure 2.3 shows Xilinx's four field-programmable gate array (FPGAs) integrated on a Si TSV interposer [59]. Compared with the conventional 2D scheme, a 3.5 times increase in the number of logic cells is reported by using the TSV interposer. Compared to organic or ceramic substrates, silicon TSV interposer offers finer interconnect geometries (~20 times denser connection pitch) to provide device-scale interconnect hierarchy that enables more than 10,000 die-to-die connections.

Xilinx 3D IC devices utilize interposer technology, enabling high-bandwidth connectivity between multiple die and provide massive inter-die bandwidth-per-watt compared to multi-chip approaches. The devices consume lower power while enabling the integration of transceivers and on-chip resources within a single package. Interposer technology leverages proven microbump technology combined with coarse pitch TSVs on a passive (no transistors) 65 nm silicon interposer to deliver high reliability interconnect without performance degradation on one FPGA device. This breakthrough technology provides the next level of advanced system integration for applications that require high logic density and tremendous computational performance.

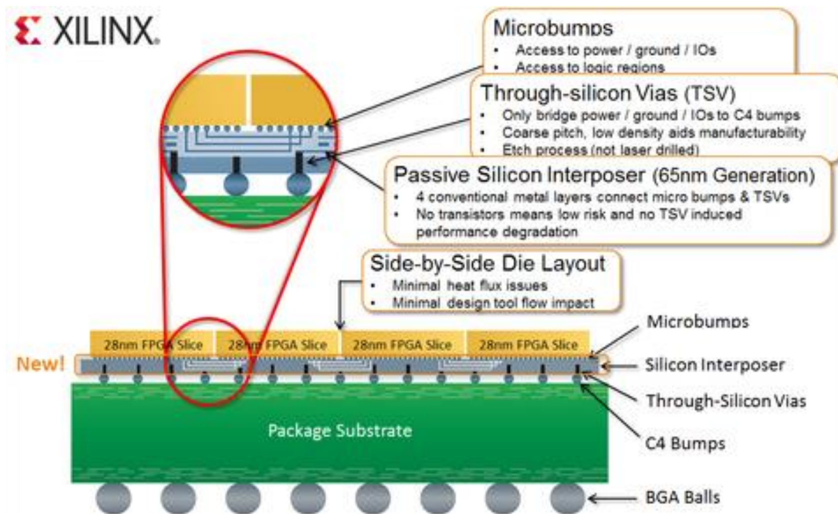


Figure 2.3 Xilinx's four field-programmable gate array (FPGAs) integrated on a Si TSV interposer [59].

2.2 Fabrication fundamentals of TSV

2.2.1 Via-first, via-middle and via last

Three main TSV processes are: "via-first", "via-middle" and "via-last", which are briefly shown in Figure 2.4 and Figure 2.5 [60], [61]. Each of them possesses its own individual advantages as well as integration problems [62], [63].

In the "via-first" process, TSV hole is etched before the CMOS transistor or other microstructure fabrication. E. M. Chow, et al. adopted the "via-first" process to etch TSV via by deep reactive-ion etching (DRIE) process, and polysilicon was selected as the conducting material [64]. M. Kawano, et al. used "via-first" process to achieve TSV in the stacked dynamic random access memory (DRAM) [65]. Polysilicon is selected as the conducting material for "via-first" process because it can bear the high temperature in the following process while metal cannot. The advantage of "via-first" is that it has less impact on the performance of photonic

device. The disadvantage is the TSV hole filling material, such as polysilicon, has higher via resistivity which leads to poor DC and RF performance. Higher via resistivity and thinning process are also challenges posed in this process.

In the “via-last” process, TSVs are fabricated after the devices fabrication and the BEOL process, and therefore the process temperature is constrained to below 450 ºC by the BEOL process. “Via-last” is etched from the wafer backside after the BEOL process and wafer thinning process. DRIE process for etching TSV hole may also induce damage in CMOS devices due to its high energy photons or electrons [66]. The advantage of “via-last” is that there are no complicated and yield sensitive backside Cu-TSV reveal issue involved in “via-first” and “via-middle”. The disadvantage is the damage to the thin wafer and the device due to the high energy in the TSV etch process and the thermal mechanical stress in ECP and annealing process.

For the “via-middle” process, it can withstand high temperature. Redolfi, et al. used Bosch process to integrate “via-middle” TSV structure with the CMOS gate [67]. Samsung has reported a 1-Gbit DRAM integrated with “via-middle” structure intended for mobile applications in 2011 [68]. Metal can be used as the hole filling material in the “via-middle” process, and the TSV fabrication-induced damage to thin wafer in the “via-last” process can be avoided. In this thesis, as DC and RF performance of the 3D integration module is the main target, therefore, “via-middle” process has been utilized.

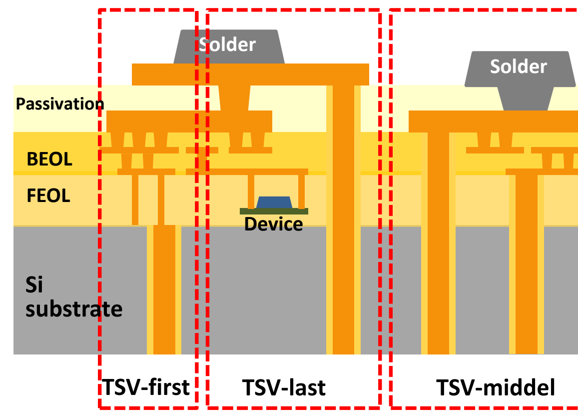


Figure 2.4 Schematic cross-sectional comparison of “via-first”, “via-middle” and “via-last” [60].

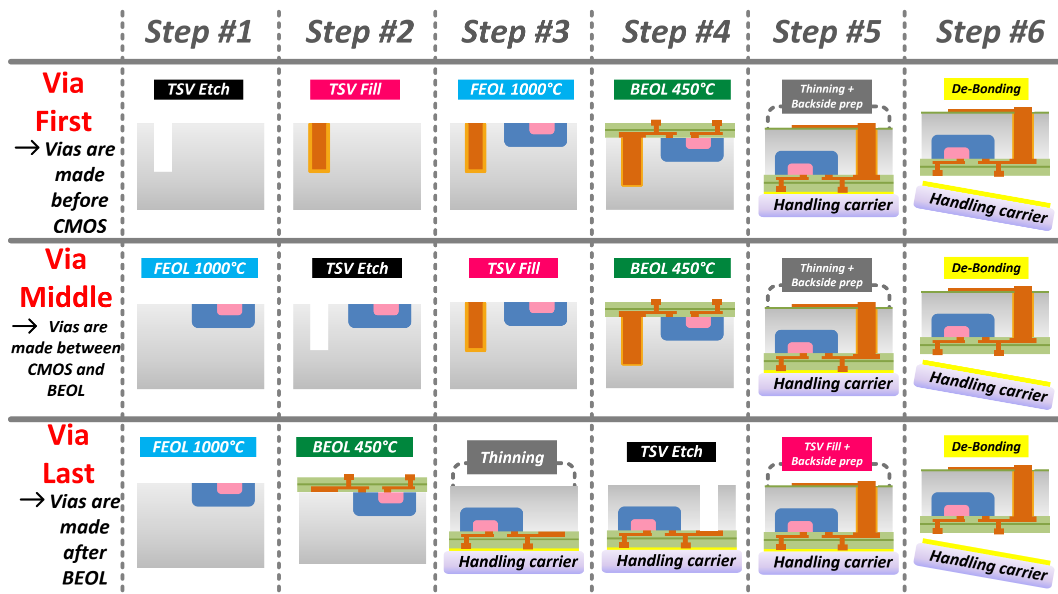


Figure 2.5: Main TSV processes for “via-first”, “via-middle” and “via-last” [61].

2.2.2 TSV fabrication process

The fabrication process of TSV mainly consists of a DRIE process for via formation, followed by a dielectric liner deposition using either plasma enhanced chemical vapor deposition (PECVD) or thermal oxidation for oxide liner, barrier and seed layer deposition by physical vapor deposition (PVD), via filling by Cu

electrochemical plating (ECP), and finally post-plating annealing and chemical mechanical polishing (CMP) process for Cu plating overburden removal [63]. Figure 2.6 shows a basic TSV process consisting of the steps listed above.

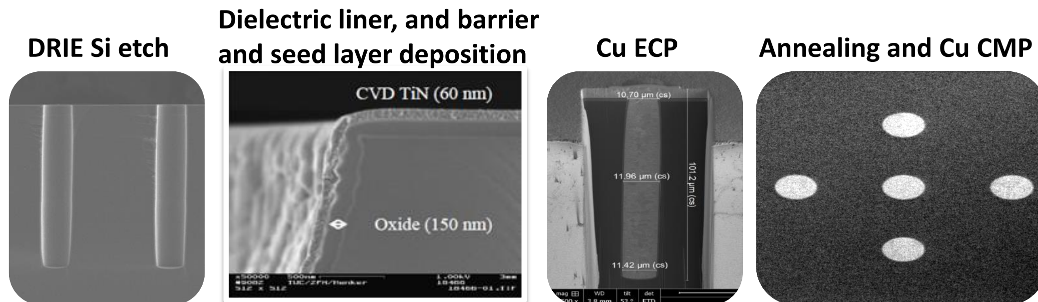


Figure 2.6: Basic process steps of TSV: DRIE silicon etch, dielectric liner deposition, barrier and seed layer deposition, Cu ECP, and post-plating annealing and Cu CMP (Source: IME, Singapore).

- ***DRIE Process (ICP Etching Process/ Bosch Process)***

For etching with larger depth, high aspect ratio and high etching rate, DRIE, namely inductively coupled plasma (ICP) etching is applicable [69]-[70]. Bosch process is the principle of the ICP etching process [71]. In Bosch process, silicon is isotropically etched by SF_6 plasma by the chemical reaction as shown in Figure 2.7. The inert molecules are dissociated into atomic fluorine radicals. Ions contained in the SF_6 plasma attack the wafer, and the fluoride radicals etch the Si. After Si etching, a passivation layer will be deposited on the sidewall. C_4F_8 gas is ionized and dissociated, and the polymerization arises from C and CF_x radicals binding under ion bombardment. The etch rate, etching and passivation time, temperature and ion energy are the process variables that need to be carefully controlled.

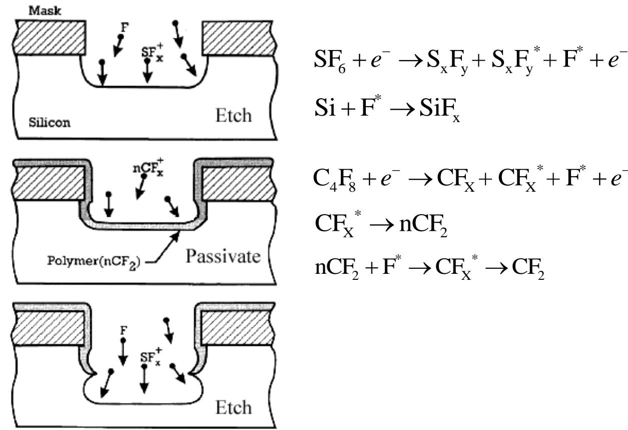


Figure 2.7 Chemical reactions of Bosch process [71].

- ***Dielectric Liner Deposition***

Silicon dioxide is commonly used as the dielectric liner in TSV to isolate the metal core of TSV from the silicon substrate. A good dielectric liner is desired for ensuring a small leakage current between the TSV and the substrate, and thus conformality is a critical consideration. O_3-TEOS (Tetra-Ethyl-Ortho-Silicate) oxide can be used to achieve a very conformal dielectric layer. The TEOS deposition provides minmum ~250 nm sidewall coverage, and the related leakage current density is less than 5×10^{-9} A/cm^2 at 2 mV/cm applied electric field [72].

- ***Barrier and seed layer deposition***

The barrier/adhesion layer and Cu seed layer can be deposited by PVD. Conformality and continuity of the deposited metal are critical for the subsequent Cu electroplating process. Prior to the PVD sputtering of the metal, a pre-cleaning process using Ar plasma to bombard the wafer surface is critical to clear the surface of any contaminants. Scanning electron microscope (SEM) images of the TEOS liner, barrier and seed layer deposition are shown in Figure 2.8 [72].

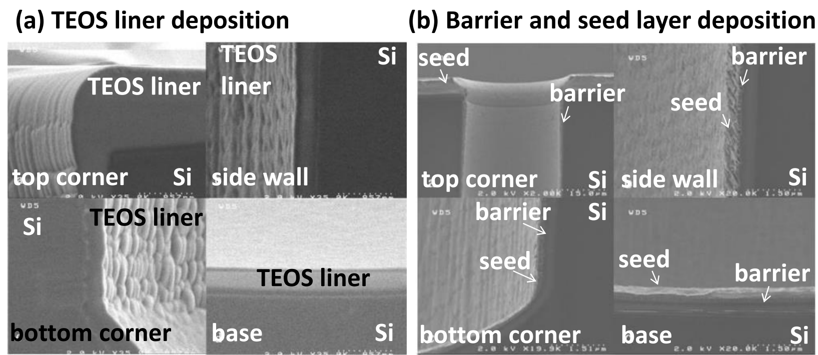


Figure 2.8 SEM images of 30 µm × 135 µm TSV after (a) TEOS liner deposition, and (b) barrier and seed deposition [72].

- ***Cu Electrochemical Plating (ECP)***

TSV copper ECP process is different from Cu-Damascene, because they have different diffusion time constants which depend on the geometries. Hence, the organic additives, the process mechanisms, and the sequences required for TSV are different from Cu-Damascene. The Cu-damascene process will be described in the Cu-BEOL fabrication section in Chapter 4. TSV ECP process is a combination of bottom-up and conformal deposition. Copper filling is determined by surface chemistry, such as additives or polymer molecules. Copper filling defects induced include bottom void, pinch off, and Copper mound. All these defects can have serious effects on TSV interconnect properties and the following processes. Voids in TSV may result in higher TSV resistance or even open interconnects, as shown in Figure 2.9.

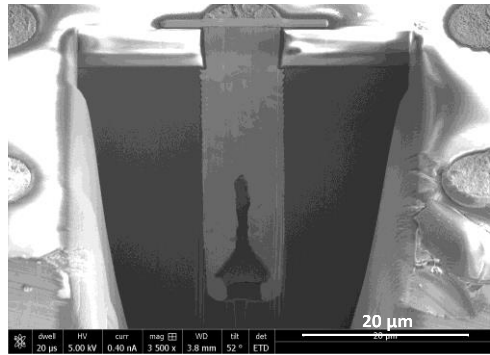


Figure 2.9 bottom void in TSV.

- ***Post-plating Annealing and Cu CMP***

Irreversible extrusion of Cu from TSV during high-temperature processing steps presents an important potential BEOL reliability issue. Commonly this reliability risk is mitigated by introducing an annealing process after Cu plating for TSV fill [73]. Annealing is also usually performed to reduce the wafer warpage [74]. The excess Cu layer on top of the TSVs from the previous Cu electroplating process is known as the Cu overburden and it is removed by CMP process, as it is difficult to delineate Cu by subtractive etch due to the limited number of volatile Cu compounds. The process uses abrasive and corrosive chemical slurry in conjunction with polishing pad.

2.3 Analytical electrical model of TSV

TSV is used for electrical connection between chips, therefore TSV resistance, inductance, and especially the parasitic capacitance should be analyzed. The equivalent electrical model presented in this section is proposed with analytical *RLGC* equations based on the lumped model [75]-[81], as shown in Figure 2.10 and Figure 2.11. The topview of TSV with radius parameters are shown in Figure 2.12.

Note that R and L represent TSV serial resistance and inductance respectively, C_{ox} is the oxide capacitance, C_{dep} is the depletion capacitance due to MOS effect, and C_{Si} and G_{Si} model the silicon dielectric losses.

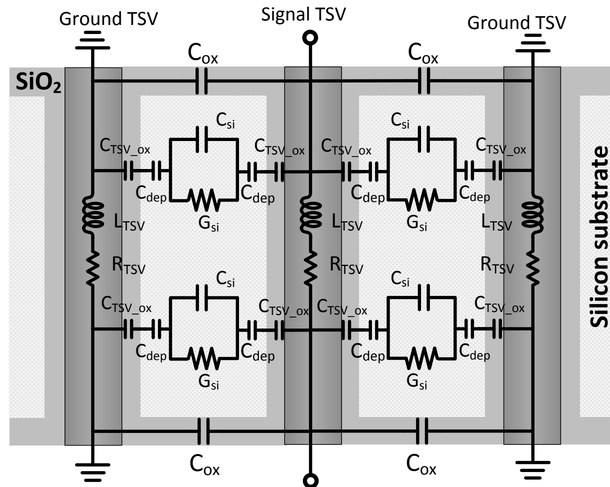


Figure 2.10 TSV equivalent electrical model.

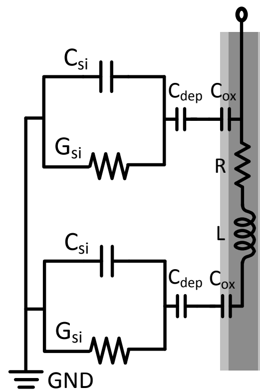


Figure 2.11 Simplified TSV equivalent model.

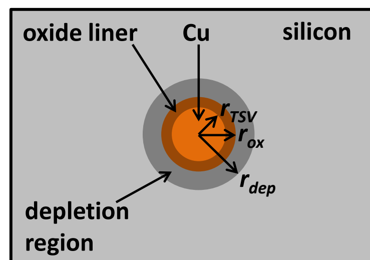


Figure 2.12 Schematic top view of a TSV, which forms a circular MOS structure.

- ***Resistance***

The series direct current (DC) resistance of a TSV is estimated through Ohm's law, as shown in Eq. (2.1), where ρ is the resistivity, and l is the TSV length.

$$R_{DC} = \frac{\rho \times l}{\pi r_{TSV}^{\ 2}} \tag{2.1}$$

As the frequency increases, skin effect reduces the TSV conductor effective cross-sectional area and therefore increases the resistance. The alternating current (AC) density near the conductor surface is larger than that at its core due to the skin effect. A TSV resistance due to the skin effect is shown in Eq. (2.2), while the total resistance is shown in Eq. (2.3),

$$R_{AC} = \frac{\rho \times L}{2\pi r_{TSV}\delta - \pi\delta^2} \tag{2.2}$$

$$R_{TSV}^{\ 2} = R_{DC}^{\ 2} + R_{AC}^{\ 2} \tag{2.3}$$

where $\delta = \sqrt{\frac{\rho}{\pi f \mu}}$ is the skin depth [82] and μ is the permeability of the TSV filling metal.

- ***Inductance***

The partial self-inductance of the TSV depends on its diameter and length and is calculated by the empirical expression in Eq. (2.4). In the case of a GS-TSV pair, the inductance is shown in Eq. (2.5), where p is the pitch between the TSVs.

$$L_{TSV} = \frac{\mu_0}{4\pi}\left[2l\ln\left(\frac{2l + \sqrt{r_{TSV}^2 + (2l)^2}}{r_{metal}}\right) + \left(r_{TSV} - \sqrt{r_{TSV}^2 + (2l)^2}\right)\right] \tag{2.4}$$

$$L = \frac{\mu l}{\pi} \cosh^{-1}\left(\frac{p}{2r_0^2}\right) \tag{2.5}$$

- ***Conductance and capacitance of the substrate***

The substrate conductance and capacitance are expressed in Eq. (2.6)-(2.7) [77],

$$G_{Si} = \frac{l\pi\sigma_{Si}}{\ln\left(\frac{p+\sqrt{p^2-4r_0^2}}{2r_0}\right)} \tag{2.6}$$

$$C_{Si} = G_{Si}\frac{\varepsilon_{Si}}{\sigma_{Si}} \tag{2.7}$$

where σ_{Si} and ε_{Si} are the conductivity and the permittivity of the Si substrate, respectively.

- ***Capacitance***

A TSV effectively forms a circular MOS structure as show in Figure 2.12, which can be analytically modeled by solving Poisson's equation in cylindrical coordinates with a full depletion approximation that assumes no mobile charge carriers in the depletion region [78]. The oxide liner capacitance and the depletion region capacitance can be calculated using Eq. (2.8)-(2.9). The total TSV capacitance is given by Eq. (2.10),

$$C_{ox} = \frac{2\pi\varepsilon_{SiO_2} l}{\ln\frac{r_{ox}}{r_{TSV}}} \tag{2.8}$$

$$C_{dep} = \frac{2\pi\varepsilon_{Si} l}{\ln \frac{r_{dep}}{r_{ox}}} \tag{2.9}$$

$$\frac{1}{C_{TSV}} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}} \tag{2.10}$$

where ε_{Si} and ε_{Sio2} are the permittivities (dielectric constants) of Si and SiO_2 respectively.

2.4 Microwave principles of TSV and transmission line

2.4.1 Classical transmission line model

In high speed circuit fabricated by deep submicrometer technology nowsdays, the ground-signal-ground (GSG) TSV needs to be treated as a transmission line [81].

Classical transmission line model is employed to obtain the characteristic parameters of the GSG TSV, the transmission line in electronic chip and the TWE in this thesis [83]. S parameter matrix describes the transmission characteristic of a two-port network as shown in Figure 2.13. The relationship between the reflected, incident power waves and *S*-parameter matrix is given by Eq. (2.11).

Figure 2.13 Incidence and reflection in a two-port network.

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{2.11}$$

The S-parameter of an unmatched transmission line is shown in Eqs. (2.12) and (2.13) [84],

$$[S] = \frac{1}{D_S} \begin{bmatrix} (Z^2 - Z_0{}^2)\sinh \gamma l & 2ZZ_0 \\ 2ZZ_0 & (Z^2 - Z_0{}^2)\sinh \gamma l \end{bmatrix} \tag{2.12}$$

$$D_S = 2ZZ_0 \cosh \gamma l + (Z^2 + Z_0{}^2)\sinh \gamma l \tag{2.13}$$

where l is the interconnects length (TSV, transmission line, TWE). Z_0 is the matching/terminal impedance equals to 50 **Ω**. Z and γ denote the characteristic impedance and the complex propagation constant, respectively. Based on the lumped-element equivalent circuit model, the characteristic impedance and the complex propagation constant are defined in Eq. (2.14) and Eq. (2.15), respectively [84],

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} = \alpha + j\beta \tag{2.14}$$

$$Z = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.15}$$

where R, L, G and C are the distributed resistance, inductance, conductance and capacitance, respectively. To derive R, L, G and C, the S-parameter are converted to *ABCD* parameters which consist of the complex propagation constant and the characteristic impedance more explicitly. The equivalent *ABCD* matrix is shown in Eq. (2.16), and the relationship between the S-parameters and the *ABCD* matrix is shown in Eqs. (2.17) and (2.18) [84].

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\gamma l) & Z\sinh(\gamma l) \\ \frac{1}{Z}\sinh(\gamma l) & \cosh(\gamma l) \end{bmatrix} \quad (2.16)$$

$$\begin{aligned} A &= (1 + S_{11} - S_{22} - \Delta S)/(2S_{21}) \\ B &= (1 + S_{11} + S_{22} + \Delta S)Z_0/(2S_{21}) \\ C &= (1 - S_{11} - S_{22} + \Delta S)/(2S_{21}Z_0) \\ D &= (1 - S_{11} + S_{22} - \Delta S)/(2S_{21}) \end{aligned} \quad (2.17)$$

$$\Delta S = S_{11}S_{22} - S_{21}S_{12} \quad (2.18)$$

Z and γ are derived by combining Eqs. (2.12), (2.13), (2.16)-(2.18):

$$Z^2 = {Z_0}^2 \frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2} \quad (2.19)$$

$$e^{\gamma l} = e^{(\alpha + j\beta)l} = \frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm \frac{\left[(1 + S_{11}^2 - S_{21}^2) - 4S_{11}^2\right]^{1/2}}{2S_{21}} \quad (2.20)$$

R, L, G, C can be derived by combining Eqs. (2.19) and (2.20) [84]:

$$R = \mathrm{Re}(\gamma Z) \quad (2.21)$$

$$L = \frac{\mathrm{Im}(\gamma Z)}{\omega} \quad (2.22)$$

$$G = \mathrm{Re}(\frac{\gamma}{Z}) \quad (2.23)$$

$$C = \frac{\mathrm{Im}(\frac{\gamma}{Z})}{\omega} \quad (2.24)$$

2.4.2 Calculation of characterization impedance and microwave effective phase index

Coplanar waveguide (CPW) includes two slots (width = *w*) with a spacing of *s* on a dielectric substrate, as shown in Figure 2.14(a) [86]. The electric and magnetic field configurations under quasi-static approximation are shown in Figure 2.14(b) [86].

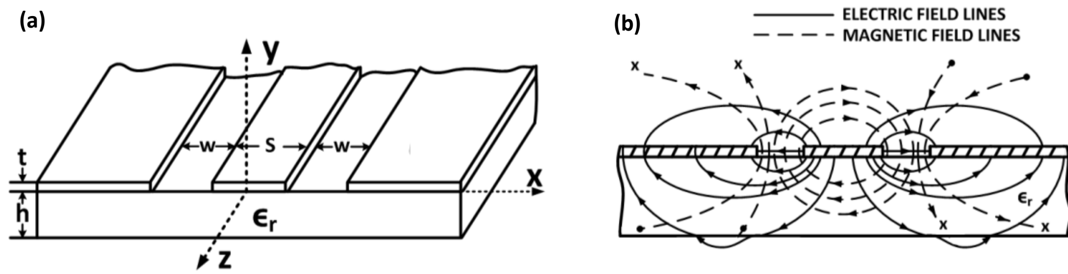


Figure 2.14 (a) CPW geometry and (b) electric and magnetic field distribution [86].

CPW characteristic impedance Z_0 and effective dielectric constant ε_{reff} of CPW are given in Eq. (2.25)-(2.30) [85], [86]. An accurate and simple approximation of $\frac{K(k)}{K^{'}(k)}$ in Eq. (2.31) has only a relative error less than 3×10^{-6} [87]. The microwave effective phase index can be estimated as the square root of the effective dielectric constant.

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_{reff}}} \frac{K^{'}(k)}{K(k)} \tag{2.25}$$

where

$$\varepsilon_{reff} = 1 + \frac{\varepsilon_r - 1}{2} \frac{K^{'}(k)K(k_1)}{K(k)K^{'}(k_1)} \tag{2.26}$$

$$k = \frac{a}{b},\ a = \frac{s}{2},\ b = \frac{s}{2} + w \tag{2.27}$$

$$k_1 = \frac{\dfrac{\sinh(\pi a)}{2h}}{\dfrac{\sinh(\pi b)}{2h}} \tag{2.28}$$

The $K(k)$ represents a complete elliptic function of the first kind and is defined in Eq. (2.29).

$$K(k) = \int_0^{\frac{\pi}{2}} \frac{d\varphi}{\sqrt{1 - k^2 \cdot \sin^2 \varphi}} \tag{2.29}$$

$K'(k)$ is the complementary function and can be calculated by Eqs. (2.30) and (2.31).

$$K(k)^2 + K'(k)^2 = 1 \tag{2.30}$$

$$\begin{aligned} &\frac{K(k)}{K'(k)} \approx \frac{\pi}{\ln\left(2 \cdot \dfrac{1+\sqrt{k'}}{1-\sqrt{k'}}\right)} \quad for \quad 0 \le k \le \frac{\sqrt{2}}{2} \\ &\frac{K(k)}{K'(k)} \approx \frac{1}{\pi} \cdot \ln\left(2 \cdot \frac{1+\sqrt{k}}{1-\sqrt{k}}\right) \quad for \quad \frac{\sqrt{2}}{2} \le k \le 1 \\ &with \ \ k^2 + k'^2 = 1 \end{aligned} \tag{2.31}$$

2.5 Principles of microring resonator

Microring resonator is one of the key silicon photonic devices for multi-channel application, which features the advantages such as wavelength flexbility and compact footprint [37]. Si microring resonator has been employed as key block to build optical MUX/DeMUX [88]-[90], interleavers [91], optical switches [92], high-speed modulators [93] and optical delay lines [94]. On the other hand, one of

the critical limitations in the compact 3D integration is the TSV-induced stress which affects the performance of silicon photonic devices integrated in interposer, especially for the stress-sensitive devices, such as silicon photonic ring resonators. Silicon photonic ring resonators are selected in this work for investigating the TSV-induced impact on the optical performance of the photonic devices integrated in the TSV interposer. Its fundamantal principles are summaried as follows.

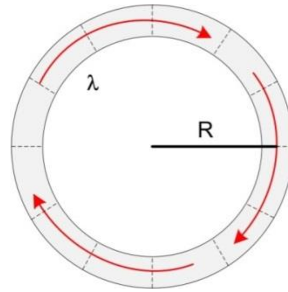


Figure 2.15 Schematic of a microring resonator. Arrows: traveling wave, λ: wavelength, R: ring radius [37].

A microring resonator is shown in Figure 2.15 schematically. The optical signal in the microring resonator is partially confined along the cavity sidewall by total internal reflection (TIR). An optical resonance is generated through the cavity field phase-matches with itself upon each round trip. The phase-matching condition of resonance is given in Eq. (2.32) [37],

$$n_{eff} L = m\lambda_m \tag{2.32}$$

where n_{eff} is the effective refractive index, L is the cavity round-trip length which approximately equals to $2\pi R$, λ_m is the mth-order resonant wavelength. The free spectral range (FSR) and group index n_g are given in Eq. (2.33) and Eq. (2.34), respectively. λ is the free-space wavelength.

$$FSR = \frac{\lambda_m^{\ 2}}{n_g L} \tag{2.33}$$

$$n_g = n_{eff} - \lambda \frac{dn_{eff}}{d\lambda} \tag{2.34}$$

2.6 Principles of Mach-Zehnder interferometer (MZI) modulator

2.6.1 MZI and multimode interference (MMI) coupler

MZI is a popular device used in optical intensity modulation employing the EO effect. The schematic of a MZI-base modulator and phase shifter cross-section are shown in Figure 2.16 [95]. The splitter/combiner can be a multimode interference (MMI) coupler, a directional coupler, or a Y-branch.

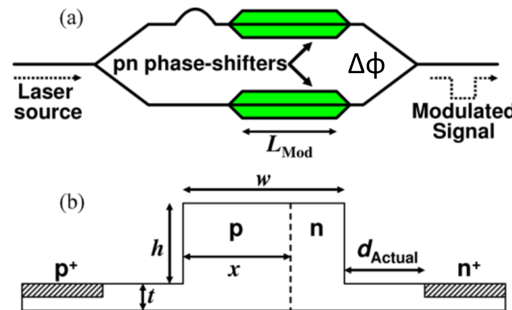


Figure 2.16 (a) Schematic of a MZI modulator. (b) Cross-sectional schematic of *p-n* junction phase shifter [95].

A phase difference $\Delta\phi$ is introduced between the two arms. When the phase shift between the two arms ($\Delta\phi$) equals $\pm\pi$, destructive interference occurs, while constructive interference occurs with no differential phase shift. The output

intensity varies with the phase difference. The output optical field amplitude is given by Eq. (2.35) [96],

$$A_{out} = \frac{\sqrt{2}}{2}\left(A_1 e^{j\phi_1} + A_2 e^{j\phi_2}\right) \tag{2.35}$$

where A_1 and A_2 denote the optical amplitudes in two arms, and ϕ_1 and ϕ_2 denote the phase delays. The input and output power are expressed as Eq. (2.36) and Eq. (2.37), respectively [96].

$$P_{in} = A_1^2 + A_2^2 \tag{2.36}$$

$$P_{out} = \left|A_{out}\right|^2 = \frac{1}{2}\left[A_1^2 + A_2^2 + 2A_1 A_2 \cos(\phi_1 - \phi_2)\right] \tag{2.37}$$

The phase difference $\phi_1 - \phi_2$ consists of the phase difference ϕ_0 at zero applied voltage and the phase difference $\Delta\phi$ arises from the bias voltage. The optical intensity transfer function is given by Eq. (2.38) [96].

$$\begin{aligned} T_{MZI} &= \frac{P_{out}}{P_{in}} = \frac{1}{2}\left[1 + b\cos(\Delta\phi - \phi_0)\right] \\ with \quad b &= \frac{2A_1 A_2}{A_1^2 + A_2^2} \end{aligned} \tag{2.38}$$

The splitter/combiner is a key component to the optical performance of the MZI modulator, which has impact on the optical insertion loss and the extinction ratio (ER). A number of structures can be used as splitter/combiner, such as directional couplers, Y-splitters, star couplers and 1×2 MMI structures. Reported Y-splitters [97], [98] and a star coupler [99] show relatively low ERs (10 dB to 16 dB). Directional couplers generally require a long coupling length for an even power

split [100], which is normally larger than 100 μm and more than ten times of the length of MMI. The coupling length is also sensitive to the fabrication tolerances in the waveguide dimensions and waveguide separation as well as the device temperature.

MMI is one of the best structures for better insertion loss and ER [101]. It has tolerance to fabrication non-uniformity and wavelength variation as well [102]. A SEM image of a MMI is shown in Figure 2.17. Large ERs are obtained using an MZI only under the balanced optical power in each arm [103], which means $A_1 = A_2$, $b = 1$ and $\phi_0 = 0$ in Eq. (2.38). Modulators utilizing MMI-splitter/combiner have demonstrated an approximately 25 dB-ER [104]-[105].

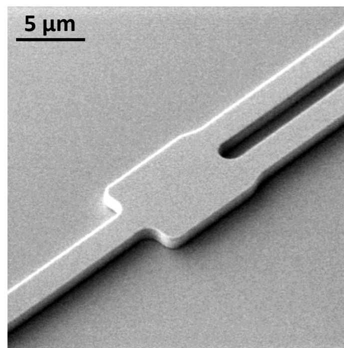


Figure 2.17 SEM image of a silicon MMI fabricated in this work.

2.6.2 Microwave design of TWE modulator

The EO effect indicates the optical refractive index change due to the applied electric field formed by an electrical modulating signal through the electrode. This refractive index change results in an optical phase change, and converted into an intensity modulation in a MZI modulator.

The TWE modulator can be regarded as a capacitive loaded transmission line [106]. The TWE itself is the unloaded transmission line, which is characterized by a series resistance R_0, an inductance L_0, a shunt impedance G_0 and a capacitance C_0 (all per unit length). The series resistance R_0 and the shunt impedance G_0 are negligible under low-loss condition. Therefore, the characteristic impedance Z_0 and microwave index n_μ of unloaded transmission line are given by Eq. (2.39) and Eq. (2.40), respectively,

$$Z_0 = \sqrt{\frac{L_0}{C_0}} \tag{2.39}$$

$$n_\mu = c \cdot \sqrt{L_0 \cdot C_0} \tag{2.40}$$

where c is the free space light speed. If the capacitive load is characterized as C_L (per unit length), the characteristic impedance Z_m and microwave index n_μ' of the loaded line are given by Eq. (2.41) and Eq. (2.42), respectively [107].

$$Z_m = \sqrt{\frac{L_0}{C_0 + C_L}} \tag{2.41}$$

$$n_\mu' = c \cdot \sqrt{L_0 \cdot (C_0 + C_L)} \tag{2.42}$$

For velocity matching, n_μ' is set to be n_{opt}. Combining Eq. (2.41) and (2.42), the inductance (per unit length) of the unloaded transmission line L_0 is given by Eq. (2.43). The capacitance of loaded line will be expressed as Eq. (2.44). The capacitance of the unloaded transmission line C_0 and the loaded capacitance C_L are expressed by Eq. (2.45) and (2.46), respectively. The relationship between Z_m, n_μ, Z_0, n_μ' is given in Eq. (2.47).

$$L_0 = \frac{n_\mu^{'} \cdot Z_m}{c} = \frac{n_{opt} \cdot Z_m}{c} \quad (2.43)$$

$$C_0 + C_L = \frac{n_\mu^{'}}{c \cdot Z_m} = \frac{n_{opt}}{c \cdot Z_m} \quad (2.44)$$

$$C_0 = \frac{n_\mu^2}{c \cdot Z_m \cdot n_{opt}} \quad (2.45)$$

$$C_L = \frac{n_{opt}^2 - n_\mu^2}{c \cdot Z_m \cdot n_{opt}} \quad (2.46)$$

$$n_\mu \cdot Z_0 = n_\mu^{'} \cdot Z_m \quad (2.47)$$

In a traveling-wave EO modulator, the electrical signal co-propagates with the optical signal. The speed limiting factors in a traveling-wave EO modulator will include impedance mismatch, microwave loss at high frequencies, and optical-electrical group velocity mismatch [108].

2.6.3 EO bandwidth

An equivalent circuit for a TWE modulator is shown in Figure 2.18, which is electrically modeled as a transmission line. The modulation depth under small signal modulation is proportional to the bias voltage, and the modulation reduction factor $r(x,\omega_m)$ is expressed as Eq. (2.48), and simplified as Eq. (2.49) [109]. The EO bandwidth is defined as the frequency, for which the optical intensity modulation depth has fallen to 70.7% of the maximum level, causing a 3 dB reduction in the received signal [107], namely $r(x,\omega_m)$ = 0.707, where ω_m is the modulation frequency.

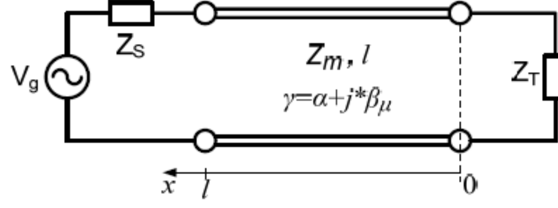


Figure 2.18 Equivalent circuit of a TWE modulator.

$$r(x,\omega_m)=\left|\frac{V(x,\omega_m)}{V(l,0)}\right| \tag{2.48}$$

$$r(x,\omega_m)=\left|\frac{V_{avg}(\omega_m)}{V_{avg}(0)}\right| \tag{2.49}$$

The modulation voltage at position x is expressed as Eq. (2.50) [110]-[111]. $V_{avg}(\omega_m)$ is the average voltage along a TWE length of l, which is given by Eq. (2.51) [110]-[111]. Therefore, $r(\omega_m)$ is calculated as Eq. (2.52), in which the microwave loss, the impedance and velocity mismatch are all taken into consideration. The symbols and expressions used in Eq. (2.50)-(2.52) are shown in Table 2.1 [106].

$$V(x,\omega_m)=\frac{V_g}{2}\cdot(1+\rho_1)\cdot e^{j\cdot\beta_{opt}\cdot l}\cdot\frac{e^{(\gamma-j\beta_{opt})\cdot x}+\rho_2\cdot e^{-(\gamma-j\beta_{opt})\cdot x}}{e^{\gamma\cdot l}+\rho_1\cdot\rho_2\cdot e^{-\gamma\cdot l}} \tag{2.50}$$

$$\begin{aligned} V_{avg}(\omega_m)&=\frac{1}{l}\cdot\int_0^l V(x,\omega_m)dx \\ &=\frac{V_g\cdot(1+\rho_1)\cdot e^{j\cdot\beta_{opt}\cdot l}}{2\cdot\left(e^{\gamma\cdot l}+\rho_1\cdot\rho_2\cdot e^{-\gamma\cdot l}\right)}\cdot\left(V_++\rho_2\cdot V_-\right) \end{aligned} \tag{2.51}$$

$$r(\omega_m)=\left|\frac{1-\rho_1\cdot\rho_2}{1+\rho_2}\cdot\frac{V_++\rho_2\cdot V_-}{e^{\gamma\cdot l}-\rho_1\cdot\rho_2\cdot e^{-\gamma\cdot l}}\right| \tag{2.52}$$

Table 2.1 Symbols and expressions used in bandwidth calculation equations [106].

Symbol	Significance	Expression or value
V_g	amplitude of the driving voltage	
ω_m	modulation frequency	
l	TWE length	
n_μ / n_{opt}	microwave / optical refractive index	
α	microwave attenuation constant	
c	velocity of light in free space	3.0×10^8 m/s
β_μ	microwave signal propagation constant in TWE	$\beta_\mu = \omega_m n_\mu / c$
β_{opt}	optical signal propagation constant in waveguide	$\beta_{opt} = \omega_m n_{opt} / c$
γ	complex microwave transmission constant	$\gamma = \alpha + j\beta_\mu$
Z_m	modulator characteristic impedance	
Z_S / Z_T	source / terminating impedance	50 Ω
ρ_1	input TWE reflection coefficient	$\rho_1 = (Z_m - Z_S) / (Z_m + Z_S)$
ρ_2	output TWE reflection coefficient	$\rho_2 = (Z_T - Z_S) / (Z_T + Z_S)$
V_+ / V_-	single pass average voltage experienced by a photon due to the forward / reverse traveling sinusoidal voltage	$V_\pm = \left(e^{\pm j \cdot \phi_\pm} \cdot \sin\phi_\pm\right) / \phi_\pm$
ϕ_+ / ϕ_-	complex phase differential between the microwave and optical signals for a forward / reverse traveling sinusoidal voltage after propagating the length of the electrode	$\phi_\pm = \left(-j \cdot \gamma \mp \beta_{opt}\right) \cdot l / 2$

- ***Perfect impedance match and microwave lossless***

In this case, $Z_m = Z_S = Z_T = 50$ Ω, $\rho_1 = \rho_2 = 0$, and $\alpha = 0$. $r(\omega_m)$ becomes Eq. (2.53). Using $r(\omega_m) = 0.707$, the EO bandwidth is calculated as Eq. (2.54), which is the mismatch between the velocity and the bandwidth under impedance match and microwave lossless condition.

$$r(\omega_m) = \left|\frac{\sin\phi_+}{\phi_+}\right| = \left|\frac{\sin\Delta}{\Delta}\right|$$
$$where,\ \Delta = \frac{\pi \cdot f_{\mathrm{m}} \cdot l \cdot (n_\mu - n_{opt})}{c} \tag{2.53}$$

$$f_{3dB_{eo}} = \frac{1.39 \cdot c}{\pi \cdot l \cdot (n_\mu - n_{opt})} \tag{2.54}$$

- ***Perfect impedance and velocity match***

In the case of velocity match, $n_{opt} = n_\mu$. $r(\omega_m)$ can be rewritten as Eq. (2.55) by using Euler's formula. Using $r(x,\omega_m) = 0.707$, Eq. (2.55) is converted to Eq. (2.56). The electrical loss under this condition is calculated by Eq. (2.57), which is −6.4 dB [106].

$$r(\omega_m) = \frac{1 - e^{-\alpha \cdot l}}{\alpha \cdot l} \tag{2.55}$$

$$\alpha \cdot l = 0.7384 \tag{2.56}$$

$$20 \cdot \log\left|e^{-\gamma \cdot l}\right| = 20 \cdot \log\left|e^{-\alpha \cdot l}\right| = 20 \cdot \log\left|e^{-0.7384}\right| = -6.4dB \tag{2.57}$$

In the case of the perfect velocity and impedance match, the EO 3 dB bandwidth can be determined by the electrical loss. Namely, the electrical 6.4 dB-bandwidth equals to the EO 3 dB-bandwidth [106].

2.7 Principles of PD

An incident photon energy greater than the bandgap energy is absorbed in the active region of the interband type semiconductor PD, resulting in an electron-hole pair (EHP) formation which contributes to a current I_p as shown in Eq. (2.58),

$$I_p = RP_{in} \tag{2.58}$$

$$R = \frac{e\eta_i}{h\nu} = \eta_i \frac{\lambda}{1.24} \tag{2.59}$$

where P_{in} is the incident power, and R is the responsivity (unit: A/W) which is defined in terms of quantum efficiency η_i, as shown in Eq. (2.59) [112]. e is the electron charge, h is the Planck's constant (6.63×10^{-34} J·s), and v is the frequency of the incident photon. η_i is defined as the ratio of the electron generation rate to the total incident photon rate, and is rewritten as the ratio of the absorbed power to the incident power. Furthermore, the quantum efficiency is given by Eq. (2.60) when photons are incident normal to a slab of width W,

$$\eta_i = \frac{P_{abs}}{P_{in}} \cong 1 - \exp(\alpha W)(1-\rho) \tag{2.60}$$

where α is the material wavelength-dependent optical absorption coefficient and ρ is the Fresnel reflection coefficent. Typical semiconductors have large values of α ($>10^4$ cm^{-1}) for photons of energy larger than the bandgap.

2.7.1 Material

The wavelengths of 1.3-1.55 μm are prevailing used for the long-distance data transition due to the minimum loss window of silica optical fiber. All users are able to connect to the servers directly without wavelength conversion, if the 1.3-1.55 μm wavelengths can be utilized in the intra/inter-chip communications. Silicon PDs have been widely used in wavelength ~ 850 nm. Its relatively large bandgap (1.12 eV) is related to an absorption cutoff wavelength of around 1.1 μm, which limits

silicon PDs' application in 1.3 -1.55 μm wavelengths [113].

III-V materials have the high absorption efficiency. However, process integration of III-V material to silicon encounters the high cost and complexities, and potential doping contaminants into the silicon devices, since III-V materials act as dopants for group IV materials as well.

Germanium, a group IV material, which avoids this contamination issue. Although Germanium is an indirect bandgap (E_g = 0.67 eV) material, its direct bandgap of 0.8 eV is only 130 meV above the dominant indirect bandgap. Therefore, Germanium provides much higher optical absorption in the range of 1.3-1.55 μm wavelength, and has become a promising PD candidate for Si photonics integration.

2.7.2 *P-I-N* Configuration

P-I-N junction is one of the most popular PD configurations. The intrinsic region *i* is depleted resulted from the built-in potential or external reverse bias, and hence the high resistivity. In this case, voltage drop and thus the high electric field generates mainly in *i* region, provides the effective collection of photo-generated EHP. In a *p-i-n* configuration, the *i* region thickness is normally many times thicker than that of the highly-doped regions, so that EHPs are generated mainly within the *i* region [114]. Another advantage of the *p-i-n* structure is that the depletion-region thickness (the *i* region) can be designed to optimize the bandwidth and the quantum efficiency [115]. Two types of *p-i-n* Ge PD structure, vertical PD (VPD) and lateral PD (LPD) are schematically shown in Figure 2.19. The VPD has a vertical *n-i-p*

junction whereas the LPD has a lateral *p-i-n* junction. The thickness of the *i* region ($t_{i\text{-}region}$) in the VPD is determined by the thickness of Ge (t_{Ge}) and the thickness of the n^+ region, which can be controlled by the Ge epitaxy condition and the doping conditions, respectively. The width of the *i* region ($w_{i\text{-}region}$) in the LPD can be controlled by the lithographically defined spacing between the p^+ and n^+ region [95].

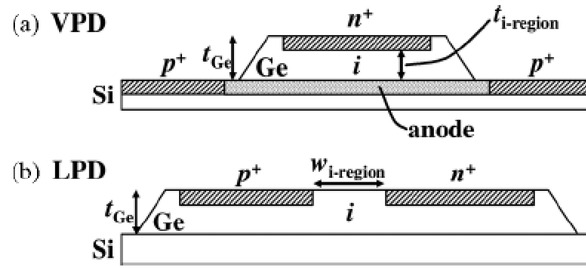


Figure 2.19 Cross-sectional schematics of the VPD and the LPD [95].

2.7.3 Bandwidth

The *p-i-n* VPD bandwidth is limited by the following two aspects [116]: (1) the carriers' diffusion from outside of the depletion layer by the carrier transport through the depletion layer, (2) the loading time of the depletion capacity. The diffusion of carriers from outside of the depletion layer was suppressed by the high doping of the contact layers. High doping reduces the lifetime of carriers by Auger recombination (lifetime ~$1/N^2$). For high frequency response, the loading time (*RC* delay) and the transit time need to be considered when diffusion is negligiable [116]. The *RC* bandwidth f_{RC} can be calculated by Eq. (2.61),

$$f_{RC} = \frac{1}{2\pi RC} = \frac{1}{2\pi \varepsilon R}\frac{d_i}{A} \tag{2.61}$$

with the intrinsic depletion capacitance $C = A\varepsilon/d_i$, where A is the junction area, ε the permittivity, and d_i the intrinsic layer thickness.

Another bandwidth limit is the time of the carriers transiting the intrinsic region. The minimum time is given by a material constant, saturation drift velocity υ_{sat} (Ge: $\upsilon_{sat} = 6\times10^6$ cm/s), and the intrinsic layer thickness d_i. The carrier transit frequency [117] f_T is calculated by Eq. (2.62).

$$f_T = \frac{\sqrt{2}}{\pi}\frac{\upsilon_{sat}}{d_i} = \frac{0.45\upsilon_{sat}}{d_i} \tag{2.62}$$

Frequencies f_{RC} and f_T together define the total 3 dB bandwidth f_{3dB} of a *p-i-n* PD and can be calculated by Eq. (2.63).

$$\frac{1}{f_{3dB}^{\;2}} = \frac{1}{f_T^{\;2}} + \frac{1}{f_{RC}^{\;2}} \tag{2.63}$$

2.8 Principles of AWG

AWG is one of the most popular MUX/DeMUX devices, which is based on the light interfering and focusing by utilizing Rowland circle [118]-[119]. The AWG has been demonstrated in various material platforms, including silica-on-silicon [120]-[122], InP [123]-[124] and SOI [53]-[55]. Silica AWGs are difficult for further large-scale integration, and InP AWGs are high-cost. Therefore silicon AWG gains research interest due to its low-cost and the photonic-CMOS integration capabilities. A 1 × N AWG is shown in Figure 2.20 schematically [125].

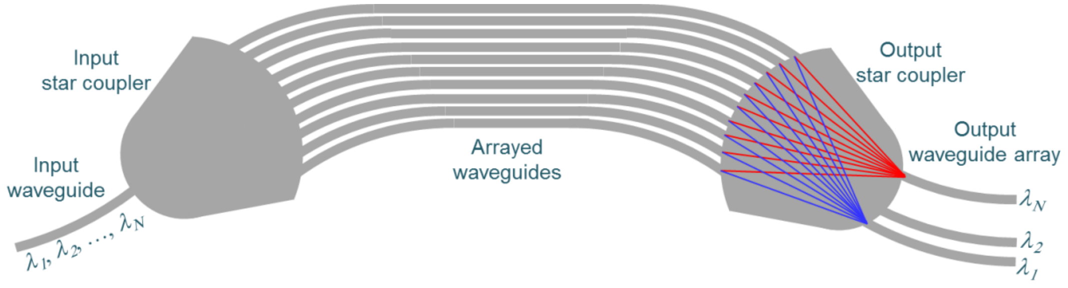


Figure 2.20 Schematic of a 1 × N AWG [125].

Multi-wavelength optical signals are incident into the input star coupler, and each optical beam will split into the arrayed waveguides with a constant path length difference (ΔL) between the neighboring waveguides. Therefore the light wave in each neighboring arrayed waveguide is delayed with a fixed differential time. Multiple light beams exiting from the arrayed waveguides at the output star coupler interfere with each other at the output waveguide interface, giving rise to constructive and destructive interference [37]. Optical signals with different wavelengths are focused on the different locations at the output facet connecting to the output waveguide arrays. Thus multiple wavelength signals are split into different output waveguides. The AWG grating equation is expressed as Eq. (2.64) [125],

$$n_s \sin\theta_i d + n_c \Delta L + n_s \sin\theta_j d = m\lambda \tag{2.64}$$

where m is the diffraction order, n_s and n_c are the effective refractive index of the star couplers and the arrayed waveguides (including the input/output waveguides), respectively. θ_i is the angle between the x-axis and the input-waveguide and θ_j is the angle between the x-axis and the output-waveguide, where i and j denote the input/output waveguide orders. ΔL is the path length difference between the

adjacent arrayed waveguides. The term $n_c\Delta L$ is the phase difference induced by the arrayed waveguides. For the center waveguides ($\theta_i = \theta_j = 0$), the grating equation is rewritten as Eq. (2.65),

$$n_c \Delta L = m\lambda_0 \tag{2.65}$$

where λ_0 is the grating center wavelength in free space. Equation (2.65) gives the arrayed waveguide length difference. For the center input/output waveguides, Eq. (2.65) can be expressed as Eq. (2.66). Subtracting the expressions in Eq. (2.66) for the mth and (m−1)th orders from each other and using the group index, FSR is calculated using Eq. (2.67).

$$\begin{cases} n_c \Delta L = m\lambda_0 \\ n_c^{'} \Delta L = (m-1)(\lambda_0 + FSR) \end{cases} \tag{2.66}$$

$$FSR = \frac{\lambda_0 n_c}{m n_{g,c}} \tag{2.67}$$

Chapter 3 TSV KOZ in Si Photonic Interposer

3.1 Introduction

TSV is a key technology in 3D integration which provides flexible and compact electrical/physical connectivity between different chips [126]. In electronics 3D integration using TSV, the impact of TSV-induced stress on transistors has been intensively investigated [127]. However, how to place TSVs in the presence of Si photonic device is an area that is missing in the literatures. To realize compact scaling, which is one of the important benefits of 3D integration, high-density TSVs are situated close to the Si photonic devices. One of the critical limitations in the compact 3D photonics integration is the TSV-induced stress which affects the performance of Si photonic devices integrated in interposer, especially for the stress-sensitive devices, such as Si photonic ring resonators. One example is the resonant wavelength shift arising from the effective-refractive-index change in the waveguide, which results from TSV-induced stress due to the different coefficients of thermal expansion (CTEs) between Cu and Si/SiO_2 of interposer. This shift results in a performance deviation from the design target.

Some works have been reported on TSV-induced stress models [126], [128]-[129]. These models are based on the 2D plane-strain solution to the classical Lamé problem in elasticity [130], namely the approximation of an infinitely long fiber (TSV) in an infinite matrix (silicon wafer). These are however, not suitable for the SOI photonics TSV interposer, which consists of buried and cladding oxide, Si

substrate and TSV with finite depth.

In this chapter, the impact of TSV-induced stress on Si photonic devices in SOI photonics interposer is analyzed. The model of TSV-induced stress distribution in the Si waveguide in SOI photonics interposer is built. The model of the effective-refractive-index change caused by the stress-induced changes of refractive index tensors is also presented. Silicon photonic double-cascaded ring resonators integrated with TSV structures have been also fabricated and characterized on an SOI platform to demonstrate the impact of TSV-induced stress, because ring resonator is one of the most stress-sensitive Si photonic devices. The characterization results are statistically analyzed with the impact of fabrication non-uniformity eliminated. Finally, this work proposes a stress aware design framework and a TSV keep-out-zone (KOZ) for Si photonic ring resonator. A compact scaling of SOI photonics interposer is ultimately achieved.

3.2 Theoretical model and simulation

Thermal stress is induced during the TSV fabrication due to the mismatch in the CTEs of the TSV material (Cu) and Si/SiO_2. The stress in the waveguide induced by TSV with different positions in interposer has been numerically analyzed by the 3D finite element analysis (FEA) method. The refractive index changes due to TSV-induced stress tensors are modeled by the stress-optic constants, and meanwhile the relationship between effective refractive index in SOI waveguide and refractive index tensors are modeled by the Mode Solver. The resonant wavelength shift of ring resonator arising from the change in the effective refractive index is simulated by the finite-difference-time-domain (FDTD) method.

3.2.1 3D FEA model and simulation of TSV-induced stress

The stress distribution in SOI photonics interposer is numerically analyzed by the 3D FEA method using the commercial software Mechanical APDL (ANSYS) 14.0. The schematic of the 3D FEA model of SOI photonic interposer is shown in Figure 3.1, which illustrates a quarter of the interposer due to the symmetry consideration. The boundary condition is set at the plane of $x = 0$, $y = 0$ and $z = 0$ to reduce the calculation load that depends on its symmetrical structure. The simulation window is set to be 50 μm × 50 μm × 50 μm to avoid the impact of boundary condition on the stress distribution in the waveguide. The thermal load is set to be annealed at 350 ℃ and cooled to room temperature of 25 ℃. The elastic mismatch between Cu and Si/SiO_2 is negligible in this 3D FEA model. A very thin TaN/Ta layer between Cu via and SiO_2 is used as a diffusion barrier in the actual experiment. As the stress caused by the TaN/Ta layer is very small, it is neglected in the simulation model. The symbol denotations, the material properties and other parameters used in simulation are listed in Table 3.1.

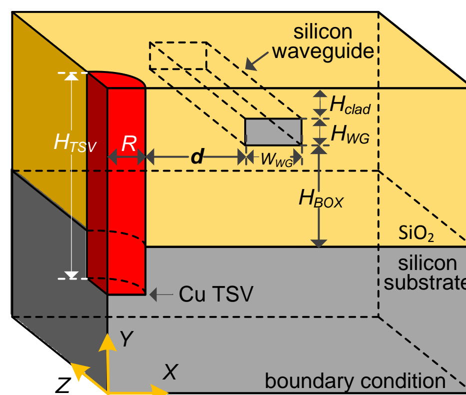


Figure 3.1 Schematic of 3D FEA model of SOI photonics TSV interposer. Due to the symmetry considerations, only a quarter of the structure is simulated. The geometries are not to scale.

Table 3.1 Symbols denotation, material properties and other parameters used in the simulation.

Symbol	**Denotation**	**Material property and other parameters**
σ_{xx} / σ_{yy} / σ_{zz}	normal stress along the *X*/*Y*/*Z* direction	
σ_{xy}	shear stress in the *XY* plane	
ΔT	thermal load	ΔT = 25ºC − 350 ºC = − 325 ºC (interposer was annealed at 350 ºC and cooled to 25 ºC)
E_f / E_m / E_o	Young's modulus of the Cu / Si / SiO_2 respectively	1.17×10^5 MPa / 1.31×10^5 MPa / 0.73×10^5 MPa
v_f / v_m / v_o	Poisson's ratio of the Cu / Si / SiO_2 respectively	0.35 / 0.28 / 0.17
α_f / α_m / α_o	CTE of the Cu / Si / SiO_2 respectively	17 ppm/ ºC / 2.8 ppm/ ºC / 0.5 ppm/ ºC
W_{WG}	width of the waveguide	0.5 µm
H_{WG}	height of the waveguide	0.22 µm
H_{BOX}	height of the buried oxide (BOX)	2 µm
H_{clad}	height of the cladding oxide	3 µm
H_{TSV}	depth of TSV	30 µm
R	radius of TSV	2.5 µm
d	the edge-to-edge distance between the TSV and the Si waveguide.	0.5 µm / 2.5 µm / 5 µm / 7.5 µm / 10 µm / 12.5 µm / 15 µm
d/R		0.2 / 1 / 2 / 3 / 4 / 5 / 6

The variables in this simulation are d/R = 0.2 / 1 / 2 / 3 / 4 / 5 / 6. Figure 3.2 shows the simulated contour plot of stress distribution in the TSV and the waveguide layer in the SOI interposer (only σ_{xx} with d/R = 0.2 is presented). It shows that the stress can reach the order of 100 MPa. The mesh volume-weighted mean stress in the waveguide in the range of $y \leq 2.5$ µm is calculated from the

contour plot, which covers the coupling region of the ring resonator in the following simulation. To extract the TSV-induced stress, the residual thermal stress distribution in the SOI photonics interposer without TSV, which is caused by the difference in the CTEs of Si and SiO_2, is also analyzed by the 3D FEA method for comparison. The simulated mesh volume-weighted mean stresses of the waveguide in the SOI interposer without TSV are: $\sigma_{xx}= -4.8$ MPa, σ_{yy}=22.7 MPa, σ_{zz}=25.9 MPa and σ_{xy} = 0.2 MPa. Positive stress represents "tension", while negative stress represents "compression". Based on the superposition principle [129], the TSV-induced weighted mean stress is calculated by deducting the weighted mean stress of interposer without TSV. The TSV-induced weighted mean stresses in the waveguide are summarized in Figure 3.3. As the waveguide is usually very long in the *Z* direction as shown in Figure 3.1, the shear stresses in this direction, namely σ_{yz} and σ_{xz}, are negligible in this work. Note that the TSV-induced weighted mean stress can reach from several MPa to hundreds MPa for $d/R < 3$.

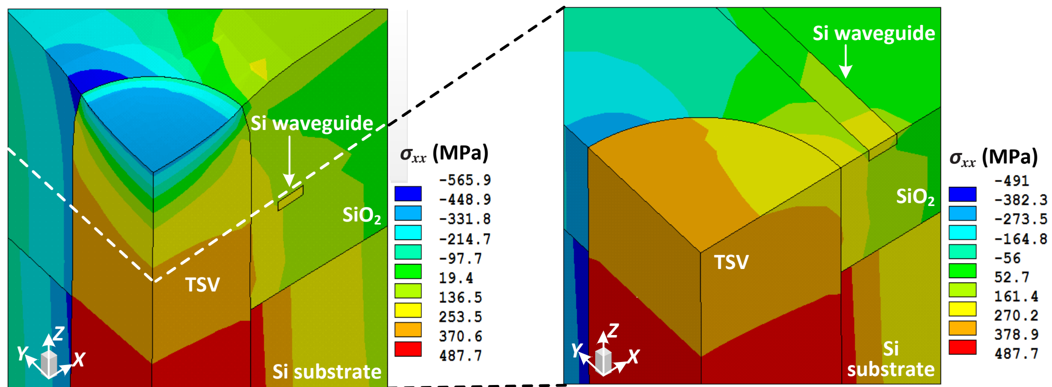


Figure 3.2 Contour plot of stress distribution in the TSV and Si waveguide (d/R = 0.2, σ_{xx}).

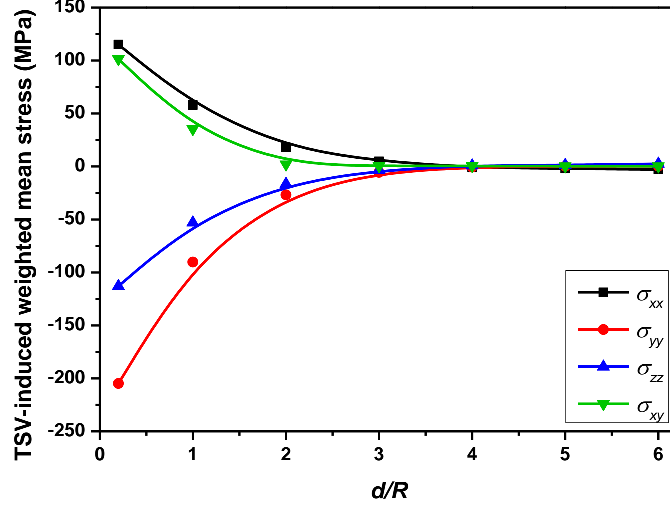


Figure 3.3 TSV-induced weighted mean stress in the waveguide in SOI interposer.

3.2.2 Change in effective-refractive-index caused by the stress-induced change in refractive index tensors

The phase of photonic devices is affected by the refractive index of the waveguide, which can be changed by stress due to the photo-elastic effect. The stress-induced change in refractive index tensors is modeled by the stress-optic constants, which are expressed in Eq. (3.1)-(3.4) [131]. Δn_{yz} and Δn_{xz} are negligible in this work because the waveguide is very long in the Z direction.

$$\Delta n_{xx} = n_{xx} - n_0 = -C_1\sigma_{xx} - C_2\left(\sigma_{yy} + \sigma_{zz}\right) \tag{3.1}$$

$$\Delta n_{yy} = n_{yy} - n_0 = -C_1\sigma_{yy} - C_2\left(\sigma_{xx} + \sigma_{zz}\right) \tag{3.2}$$

$$\Delta n_{zz} = n_{zz} - n_0 = -C_1\sigma_{zz} - C_2\left(\sigma_{xx} + \sigma_{yy}\right) \tag{3.3}$$

$$\Delta n_{xy} = n_{xy} - 0 = -C_3\sigma_{xy} \tag{3.4}$$

In the above, n_{xx}, n_{yy}, n_{zz}, and n_{xy} are refractive index tensors, and n_0 is the

refractive index without stress. $C_1=n_0^3(p_{11}-2vp_{12}) / 2E$, $C_2=n_0^3(-vp_{11}+(1+v)p_{12}) / 2E$ and $C_3 = n_0^3 p_{44} / 2G$ are the stress-optic constants related to the Young's modulus, Poisson's ratio, and the strain-optic constants (p_{11}, p_{12} and p_{44}) respectively. For isotropic crystals, $p_{44} = (p_{11}-p_{12})/2$ and $G = E/2/(1+v)$ [131]. The photo-elastic constants of Si are listed in Table 3.2 [132]. The stress-optic constants in Table 3.2 may not be accurate at 1.55 μm, because they are derived from the strain-optic constants measured at 1.15 μm. However, the dispersion is expected to be weak since the strong electronic transitions occur at the shorter wavelengths for both Si and SiO_2 [132]. The stress-optic constants of SiO_2 are ten times less than that of Si, therefore the stress-induced changes of refractive index tensors of SiO_2 are not considered in our work. The changes of refractive index tensors calculated based on the weighted mean stresses in the Si waveguide are shown in Figure 3.4. It shows that Δn_{xx}, Δn_{yy}, Δn_{zz} and Δn_{xy} decrease from the order of 10^{-3} at $d/R = 0.2$ to about zero at $d/R = 3$, and they are negligible for $d/R > 3$.

Table 3.2 Photo-elastic constants of Si [132].

material	**refractive index** [a] n_0	**strain-optic constants** [b]			**stress-optic constants**		
		p_{11}	p_{12}	p_{44}	C_1 (10^{-12}/Pa)	C_2 (10^{-12}/Pa)	C_3 (10^{-12}/Pa)
Si	3.476	−0.101	0.0094	−0.0552	−11.35	3.65	−23.72

[a] Measured at wavelength $\lambda = 1.55$ μm.

[b] Measured at wavelength $\lambda = 1.15$ μm.

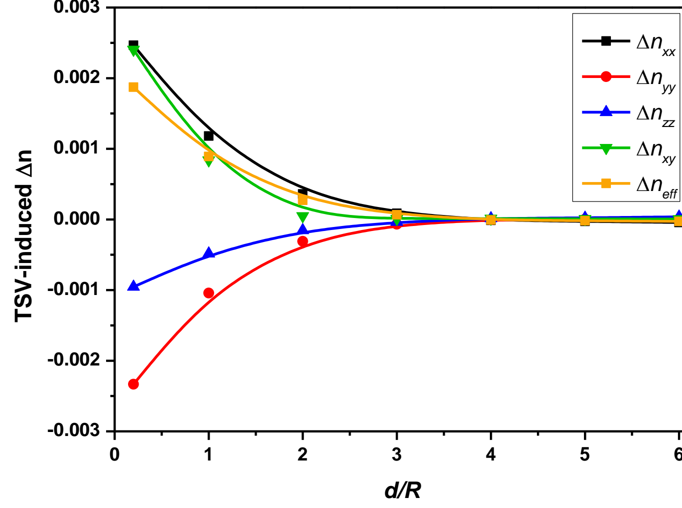


Figure 3.4 TSV-induced changes of refractive index tensors and effective refractive index.

Silicon waveguide is anisotropic under the TSV-induced stress. For anisotropic materials, the electric field (E) and the electric displacement field (D) are not parallel, and they are related by the permittivity tensor ε (a 2nd order tensor) [133]. As discussed before, the shear stresses (σ_{yz} and σ_{xz}) in the Z direction are very small and hence the refractive index tensors (n_{yz} and n_{xz}) are negligible. E_y is negligible for transverse electric (TE) mode (electric field along X axis in Figure 3.1), so the relation between E and D can be expressed as Eq. (3.5).

$$\begin{pmatrix} D_x \\ D_y \\ D_z \end{pmatrix} = \begin{pmatrix} n_{xx}^2 & n_{xy}^2 & 0 \\ n_{xy}^2 & n_{yy}^2 & 0 \\ 0 & 0 & n_{zz}^2 \end{pmatrix} \begin{pmatrix} E_x \\ 0 \\ E_z \end{pmatrix} \tag{3.5}$$

Therefore, the change in effective-refractive-index (Δn_{eff}) for TE mode is mainly caused by Δn_{xx}, Δn_{xy} and Δn_{zz}, which can be expressed as Eq. (3.6). It is in agreement with the results simulated using Mode Solver of Rsoft commercial software. The corresponding fitting results simulated using Mode Solver are

expressed as Eq. (3.7). According to Eq. (3.1), Eq. (3.3) and Eq. (3.7), the model for stress-induced Δn_{eff} can be derived as Eq. (3.8),

$$\Delta n_{eff} = \frac{\partial n_{eff}}{\partial n_{xx}} \Delta n_{xx} + \frac{\partial n_{eff}}{\partial n_{xy}} \Delta n_{xy} + \frac{\partial n_{eff}}{\partial n_{zz}} \Delta n_{zz} \tag{3.6}$$

$$\Delta n_{eff} = a_1 \cdot \Delta n_{xx} + a_2 \cdot \Delta n_{xy} + a_3 \cdot \Delta n_{zz} \tag{3.7}$$

$$\Delta n_{eff} = -\left[\left(a_1 C_1 + a_3 C_2 \right) \sigma_{xx} + \left(a_1 C_2 + a_3 C_2 \right) \sigma_{yy} + \left(a_1 C_2 + a_3 C_1 \right) \sigma_{zz} \right] \tag{3.8}$$

where a_1 = 0.843941, a_2 = 0 and a_3 = 0.218913 for TE mode. The modeling result of Δn_{eff} is also shown in Figure 3.4.

3.2.3 Simulation of TSV impact on Si photonic ring resonator

Effective-refractive-index (n_{eff}) is a critical parameter of photonic devices. According to $\Delta\lambda = \lambda \cdot \Delta n_{eff} / n_g$ [134], where λ is the wavelength and n_g is the group index, Δn_{eff} can result in a wavelength shift of the device, and hence affect the device optical performance. As discussed before, Δn_{eff} can be caused by the TSV-induced stress. A group of TSV designs with different d /R values (from 0.2 to 6) are considered in our simulation. Based on the modeling result of stress-induced Δn_{eff} in Figure 3.4, the wavelength shift of ring resonator is simulated using the FDTD method. The schematic of the Si photonic ring resonator is presented in Figure 3.5, which includes a transmission waveguide, a ring cavity and a coupling region. The parameters of the simulated ring resonator are L_c = 2 μm, r = 5 μm and the gap between ring and waveguide is 0.2 μm.

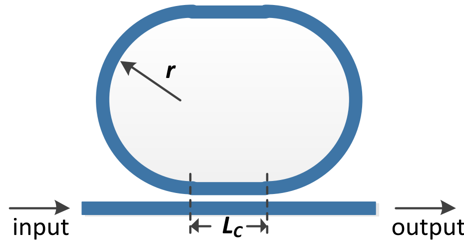


Figure 3.5 Schematic of Si photonic ring resonator. *Lc* represents the coupling length, and *r* represents the radius of the ring.

The simulated spectra are shown in Figure 3.6(a). The wavelength shift of ring resonator caused by the TSV-induced stress is presented in Figure 3.6(b). The simulated results show that the ring resonator wavelength shift decreases from the order of 0.1 nm to the order of 0.01 nm with increasing d/R. In optical communications systems, the spacing of Dense-Wavelength-Division-Multiplexing (DWDM) defined by ITU is typically 100 GHz (0.8 nm) or 50 GHz (0.4 nm) [135]-[136]. Therefore, wavelength shift in the order of 0.1 nm will result in performance deviation from the designed objective. As the wavelength shift is negligible for $d/R > 3$, the TSV KOZ of $d/R > 3$ for Si photonic ring resonator in SOI interposer is proposed, in order to keep any resonant wavelength shift one order of magnitude smaller than 0.1 nm.

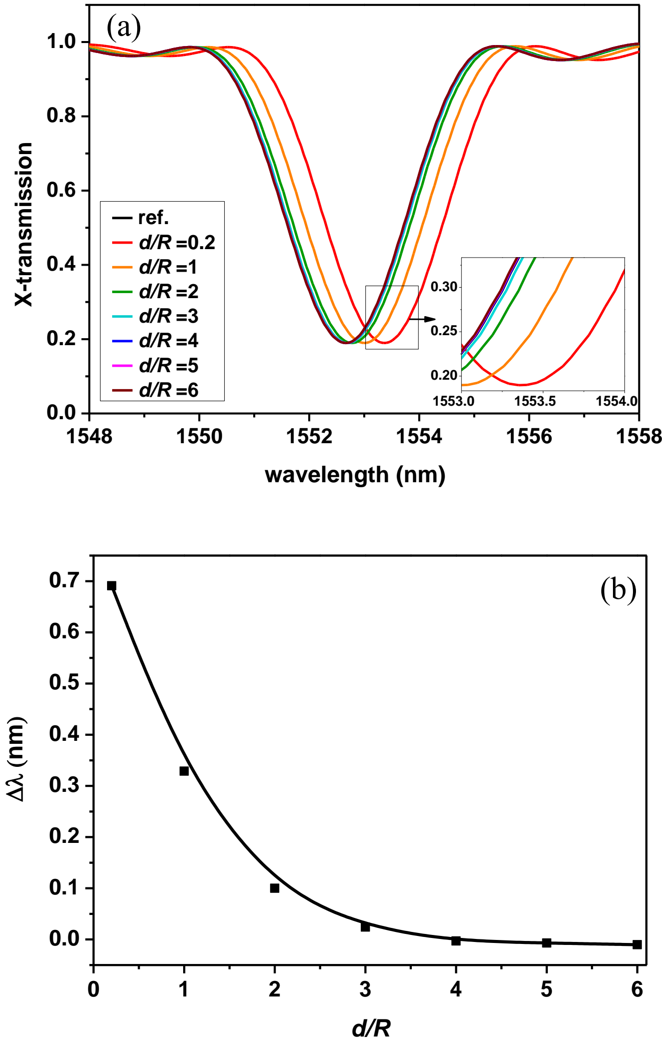


Figure 3.6 Simulated wavelength shift of a Si photonic ring resonator. (a) Ring resonator spectra and (b) ring resonator wavelength shift.

3.3 Fabrication and characterization

Si photonic double-cascaded ring resonators integrated with TSV structures on an SOI platform were fabricated and characterized to demonstrate the impact of TSV-induced stress, because ring resonator is one of the most stress-sensitive Si photonic devices. The characterization results are statistically analyzed with the impact of

fabrication non-uniformity eliminated.

3.3.1 Design of experiment and fabrication

An SOI photonics interposer integrated with Si photonic ring resonators and TSVs is designed to verify the impact of TSV-induced stress on the optical performance of Si photonic device. However, the optical performance of ring resonator is sensitive to the fabrication variation. In order to minimize the ring performance variation caused by the fabrication non-uniformity, a double-cascaded ring resonator is used, as shown in Figure 3.7. Figure 3.7 includes two double-cascaded ring-resonators, where one device is integrated with TSVs and the other is without TSVs that serves as a reference. The TSV-induced stress changes the resonated wavelength spacing of the two ring resonators. The difference of the resonated wavelength spacing between the two devices can be extracted to study the impact of TSV-induced stress. All ring resonators in the two devices are put as closely as possible to further minimize any fabrication variation. The distances between the adjacent cascaded rings, and between the top rings with TSVs and the bottom reference rings are both 150 μm. The parameters of the single ring resonator are the same as the parameters of the ring resonator simulated, namely $L_c = 2$ μm, $r = 5$ μm and the gap between ring and waveguide is 0.2 μm. A center-to-center spacing of TSVs of $6R$ ($R = 2.5$ μm) is designed, and different splits of d/R are designed, including $d/R = 0.2$, $d/R = 1$, $d/R = 2$ and $d/R = 3$.

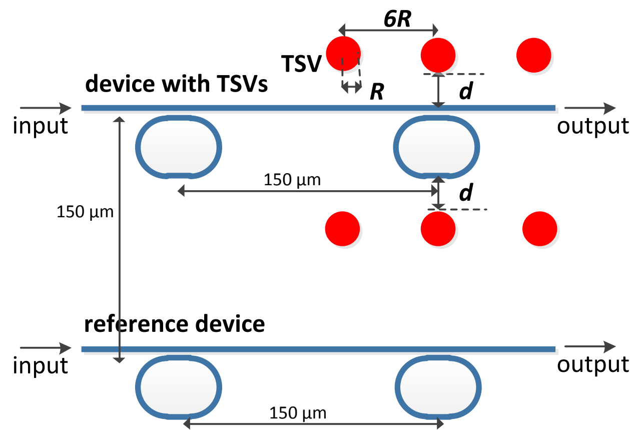


Figure 3.7 Schematic of two double-cascaded ring resonators for testing the TSV impact. The geometries are not to scale.

The devices were fabricated on an 8-inch SOI wafer with a 220 nm top Si layer and a 2 µm buried oxide (BOX). First, the Si waveguide ring resonators were formed by dry etching process. Tilted SEM images of the waveguides are shown in Figure 3.8. The tip width is about 200 nm for coupling with lensed fibers, as shown in Figure 3.8(a). Figure 3.8(b) shows the SEM image of coupling region of the ring resonator. With a 4 µm thick photo resistance pattern, 30 µm deep TSVs were etched through after the waveguide formation. The vertical and smooth sidewall of TSV in SOI interposer is shown in Figure 3.8(c). A 1 µm thick TEOS SiO_2 was deposited by the PECVD method on the sidewall of TSV for isolation. A 200 nm thick TaN/Ta layer was then deposited by PVD method as a diffusion barrier. Another 1 µm thick PVD Cu seed layer was deposited on the TaN/Ta barrier layer. Cu ECP was carried out to fully fill the TSV. Finally, the wafer was annealed at 350 ℃ followed by CMP. The microscope image of the cross-section of SOI photonics interposer integrated with copper TSVs and the SEM image are shown in Figure 3.8(d). Figure 3.8(d) shows the TSV is filled fully with copper. The inset shows the cross-section of the device with TSV.

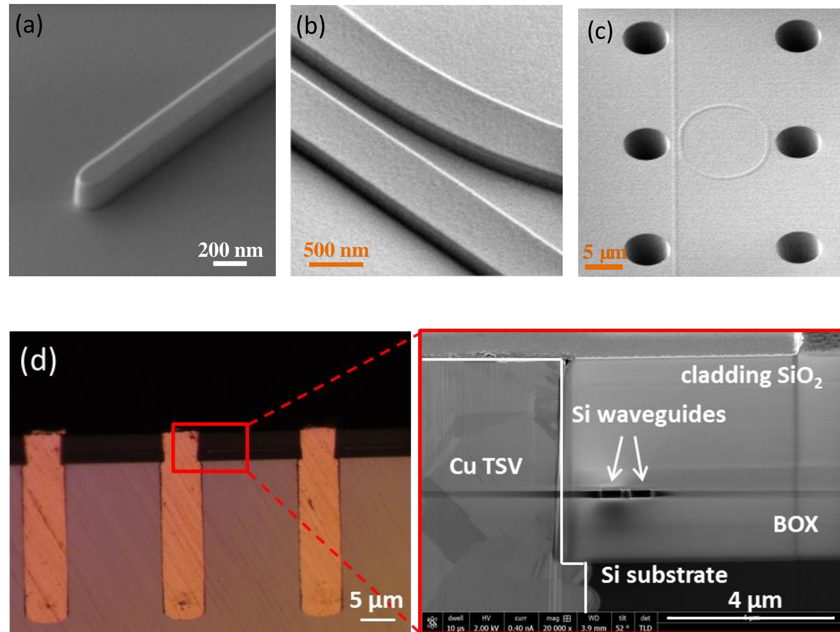


Figure 3.8 (a) SEM image of waveguide tip. (b) SEM image of coupling region of ring resonator. (c) SEM image of ring resonator integrated with etched TSV in SOI interposer. (d) Microscope image of the cross-section of SOI photonics TSV interposer (inset: SEM image of the coupling region).

3.3.2 Characterization

Agilent optical measurement system (Photonic Dispersion and Loss Analyzer) was used to characterize the optical performances of two devices with/without TSV structures at room temperature. The optical measurements were performed after selecting the TE polarization. The typical spectra of four groups of devices fabricated for testing the TSV impact are shown in Figure 3.9. Each group includes two spectra, with one belongs to the device with TSVs, and the other belongs to the reference device without TSV. Compared to the reference devices, there are changes to the wavelength spacing of each device with TSVs. The results show that the TSV-induced stress causes a wavelength shift of the ring resonators. The

differences in the resonant wavelength spacing are statistically analyzed from fifteen samples for each group. In order to consider fabrication variation in the different die locations, another four groups of two double-cascaded ring resonators without any TSVs were fabricated, and the differences in the resonant wavelength spacing are also statistically analyzed from fifteen samples of each group. The measurement results are shown in Figure 3.10, including the simulated results.

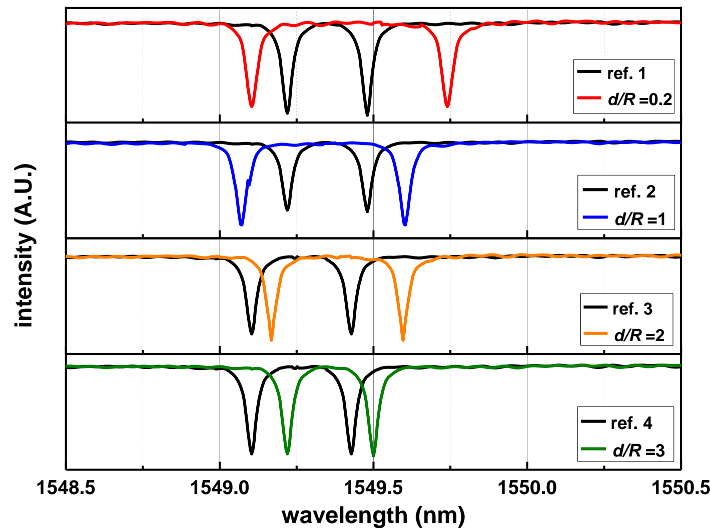


Figure 3.9 Optical spectra of double-cascaded ring resonators with/without TSV structures.

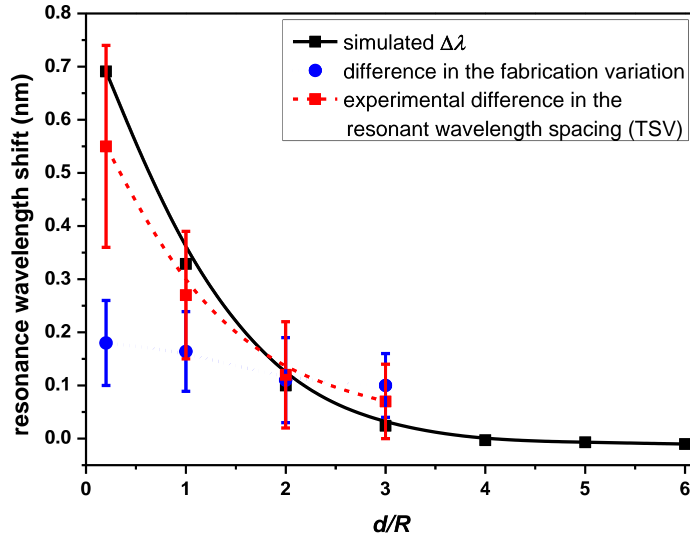


Figure 3.10 Simulated and experimental resonant wavelength shift of ring resonator.

For the four groups of devices without any TSVs, the average differences in the resonant wavelength spacing between the device and the reference is ~0.15 nm and the deviation is ~0.07 nm. The results show that in the absence of TSV-induced stress, the difference in the wavelength spacing of double-cascaded ring resonators between the device and the reference is relatively constant. For the four groups of devices with TSVs, the average differences in the resonant wavelength spacing between the devices with TSVs and the reference devices are obviously different. With increasing d/R, the average difference reduces from 0.55 nm to 0.07 nm, with a deviation that reduces from 0.19 nm to 0.07 nm. The result of wavelength spacing change shows that the TSV-induced stress impact on the optical device becomes stronger when the TSV structure is closer to the optical device. When the distance between the TSV and the waveguide is more than 7.5 μm (d/R = 3), the stress impact on the optical device is negligible. The experimental results are basically in

agreement with the analysis using the above model. In conclusion, the TSV KOZ for the Si photonic ring resonator in SOI photonics interposer has been experimentally demonstrated.

3.4 Conclusions

An SOI photonics TSV interposer has been proposed. The impact of TSV-induced stress on the optical performance of the photonic devices has been investigated theoretically as well as experimentally for the first time. The TSV-induced stress in the waveguide has been numerically analyzed by the 3D FEA method. The refractive index changes due to TSV-induced stress tensors are modeled by the stress-optic constants, and meanwhile the relationship between effective refractive index in SOI waveguide and refractive index tensors are modeled by the Mode Solver. The resonant wavelength shift of ring resonator arising from the change in the effective refractive index is simulated by the FDTD method. Experimentally, an SOI photonics interposer demo has been fabricated using a CMOS-compatible integration process. The TSV-induced resonance wavelength shift has been characterized and the experimental results are basically in agreement with the analysis in the proposed model. Finally, the TSV KOZ of $d/R > 3$ for Si photonic ring resonator in SOI interposer is proposed, in order to keep the resonant wavelength shift one order of magnitude smaller than 0.1 nm.

Chapter 4 Silicon photonic interposer featuring RF TWE via Cu-BEOL

4.1 Introduction

The concept of "interposer" is an electrical/optical/physical interface routing between one socket or connection to another. The purpose of an interposer is to spread a connection to a wider pitch or to reroute a connection to a different connection [137]. In other words, the integrated chips or devices can be electrically/optically/physically supported by the interposer vertically above and/or below. The schematic cross-section of the proposed Si photonic interposer featuring Cu-BEOL, TSVs and flip-chip bonding is shown in Figure 4.1.

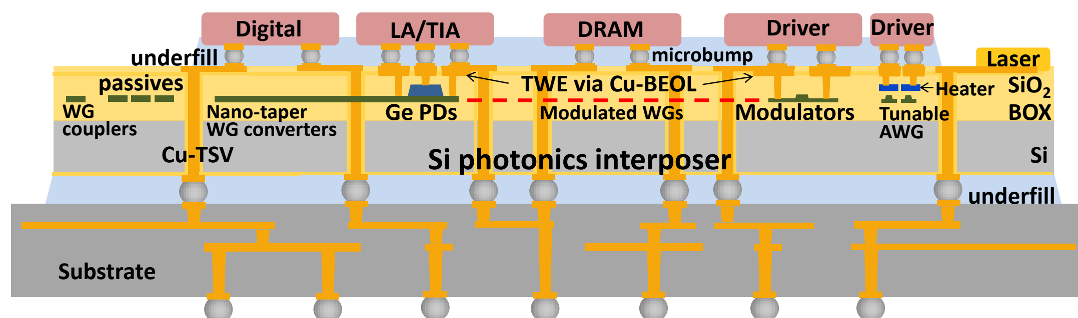


Figure 4.1 Schematic cross-section of a Si photonics interposer with Cu-BEOL in a Si photonics-CMOS O/E IC integration system (not to scale).

Besides the silicon photonic devices investigated in this chapter, the under bump metals (UBMs) or microbumps for the flip-chip bonding process were actually fabricated in this silicon photonic interposer. Here, aluminum testing pads were fabricated in place of UBMs/microbumps which were connected with the electrode

of the photonic devices. This is for the purpose of protecting the probe when testing the silicon photonic devices' performance under lab conditions. The use of UBMs and microbumps will be presented in Chapter 5 where discusses electro-photonic 3D integration based on silicon photonics TSV interposer.

In this chapter, a silicon photonic interposer featuring RF TWE via Cu-BEOL is presented. MZI optical modulators and waveguided Ge-on-Si PD is monolithically integrated within this interposer. Moreover, a TO tunable silicon AWG with Cu electrode and Ti/TiN heater is designed and monolithically integrated in this interposer. To avoid the dishing caused on Cu surface arising from the CMP process included in the Cu dual-damascene process, a latticed Cu surface pattern is designed for the Cu electrode. The modulator is designed with Cu-TWE and contact plugs for better RF performance and better efficiency, and with doping compensation [138] for reducing the optical transmission loss of the phase shifter caused by ion implantation. The measured electro-optic bandwidth at $V_{bias} = -5$ V is up to 37 GHz when it is operated at 1550 nm. At a data rate of 50 Gbps at $V_{pp} = 3.5$ V, the dynamic extinction ratio (ER) is 7.08 dB. The phase shifter is composed of a 3 mm-long reverse-biased *p-n* junction with modulation efficiency ($V_\pi \cdot L_\pi$) of ~18.5 V·mm. The Ge-on-Si PD is designed with Cu-TWE and the discrete Cu contact plugs to Ge for reducing Cu-induced optical loss and thus improving the responsivity. PDs with different Ge lengths are fabricated. The measured responsivity of 0.65 A/W at 1550 nm for 5 μm-long Ge is achieved, which is resulted from the special contact plugs design. The measured optic-electro bandwidth at $V_{bias} = -3$ V is up to 33.7 GHz when it is operated at 1550 nm. The measured eye-diagram shows that the data rate reaches 30 Gbps. A TO tunable silicon AWG with Ti/TiN heater and Cu

metallization has been investigated and demonstrated. The wide ridge-waveguide and the narrow channel-waveguide are designed for reducing the impact of the fabrication non-uniformity. The thermal distribution simulation shows that a uniform heating can be achieved by the heater design, while the experiment results reveal that above 600 GHz channel tunability has been achieved.

Finally, a process flow for monolithically integrating the RF EO devices and the TO devices into the silicon photonic interposer with Cu metallization has been established in this work, which is also a multi-project-wafer (MPW) process. Moreover, from designs and experiments, it is demonstrated that Cu TWE with low resistance provides better RF performance with higher bandwidth than Al electrode based active devices. Cu application can further improve the integration of silicon photonics devices and CMOS circuits in the future. This work has established the needed Cu-BEOL based RF-friendly Si-photonics devices toolbox for high performance implementation.

4.2 Design of modulator and PD with Cu-TWE

4.2.1 Design of Modulator and PD

The MZI modulator and vertical PD are designed on an SOI wafer with 220 nm-thick top silicon and 2 μm-thick BOX. The waveguide width is 500 nm and the slab height of the ridge waveguide is 100 nm. The waveguide tip width is about 200 nm for coupling with lensed fibers [139]-[141]. The microscope images of the modulator and the Ge-on-Si PD are shown in Figure 4.2 and Figure 4.3, respectively.

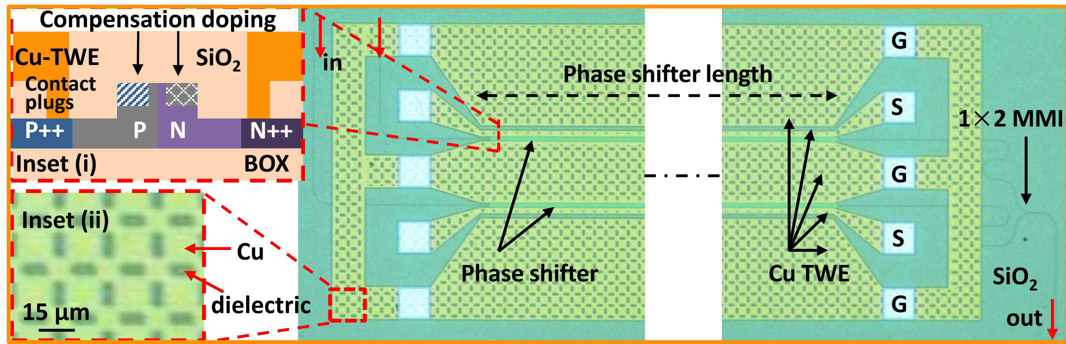


Figure 4.2 Microscope image of the MZI silicon optical modulator. Inset (i): implantation schematic diagram of the phase shifter (not to scale). Inset (ii): latticed Cu surface pattern.

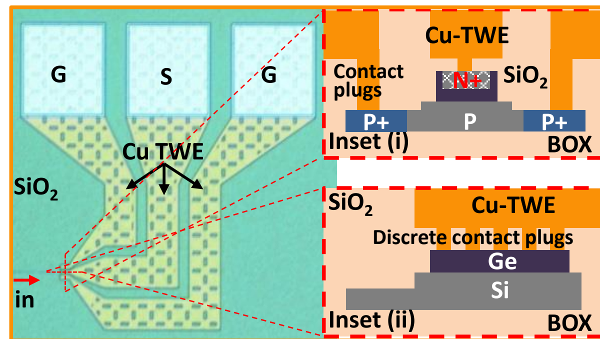


Figure 4.3 Microscope image of the Ge-on-Si PD. Inset (i): implantation schematic diagram of the Ge-on-Si (not to scale). Inset (ii): discrete contact plugs to Ge.

Among all kinds of silicon optical modulators, silicon carrier-depletion-based modulator [154]-[160] has proven itself to be the most prevailing solution for optical modulation on silicon because of its high performances, such as high speed and low power consumptions. The Si carrier-depletion-based modulator is designed with a 3 mm-long *p-n* junction phase shifter. The waveguide width is 500 nm and the slab height of the ridge waveguide of the phase shifter is 100 nm. A 1×2 MMI structure is used as the splitter and the combiner. It is an asymmetrical MZI structure and the arm length difference ΔL is 300 μm corresponding to 1.9 nm FSR,

since FSR= $\lambda^2/(n_g \cdot \Delta L)$, corresponding to a group index $n_g = 4.18$ in this design. The inset (i) of Figure 4.2 shows the pattern of implantations. The implantation compensations are designed on both areas of the ridge corners for lower implantation-induced optical loss and higher modulation speed. The implantation compensation design is similar to the modulator reported by IME [138]. The phase shifter loss is reduced through optimizing the doping level out of the depletion region while keeping the modulation efficiency and switching speed at a high level. This is realized through compensated doping in the active region with donor (acceptor) ions. The doping profile of the *PN* junction cross section is optimized with the following two considerations. First, reduce the absorption loss of the waveguide by compensated doping in the top areas of the ridge corner. Second, keep the high doping level at the bottom of the waveguide in order to avoid degrading other characteristics of the modulator such as the modulation speed [138]. The inset (ii) of Figure 4.2 shows the latticed Cu surface pattern of the Cu-TWE, which will be described in the next section 4.2.2.

In the implantation process, the introduced free carriers induce absorption loss due to free carrier's effect, which degrades the optical performance of photonic devices [138]. To reduce the optical transmission loss of phase shifter caused by ion implantation while keeping the modulation efficiency and switching speed at a high level, a doping compensation method [138] is utilized to optimize the doping level on the depletion region of the phase shift.

Figure 4.3 shows the microscope image of the Ge-on-Si PD. The inset (i) shows the implantations pattern, and the inset (ii) shows the cross-section of the discrete

contact plugs to Ge, which is designed for reducing Cu-induced optical loss the thus improving the responsivity. The Ge thickness is 500 nm, and different Ge lengths have been fabricated, including 5 μm, 10 μm and 20 μm.

4.2.2 Design and modeling of Cu-TWE

Take the electrode of modulator as an example here, in most reported modulator papers, aluminum is usually adopted as the electrodes and contact/via plugs material in silicon optical modulators [138], [142]-[149]. For example, one kind of silicon slot photonic crystal modulator with 0.54 pJ/bit power consumption was formed with Al metal electrode [142]. In 2011, one group from Fujikura achieved a silicon MZI modulator of extinction ratio beyond 10 dB at 10.0-12.5 Gbps [143]. Also, a silicon MZI modulator with low power and data rate of 12.5 Gbps was reported [144], and Bell Labs demonstrated a single-drive push-pull silicon MZI modulator with data rate up to 50 Gbps in 2012 [145]. The group in IME also presented a 50 Gbps silicon MZI modulator last year in which Al was used as the metal electrode [146]. These silicon modulators with high data rate and low power consumption based on Al electrodes have been achieved in the past few years. However, Al material has its shortcomings, such as nano-pores-induced low density and high resistivity, which impedes further improvement in high speed devices. A good alternative to be used as electrode is Cu, which can replace Al in silicon photonics devices in the future because it has lower resistivity, higher conductivity and lower activation energy than Al [150]-[152]. In principle, these advantages of Cu contribute to higher speed and lower power consumption for silicon photonics active devices and higher integration intensity for circuits. Currently, few silicon

photonics devices with Cu electrode have been reported. IMEC reported one modulator with Cu TWE and contact filling material of Tungsten (W) in 2012, which has a data rate up to 40 Gbps [153]. IBM reported a 25 Gbps microring modulator using Cu electrode [154] and a 90 nm CMOS-photonics technology node for 25 Gbps transceiver [155] in 2012. Oracle Labs reported hybrid-integration of silicon photonics using Cu electrode in 2012 [156]. Luxtera reported a 4 $\times$25 Gbps transceiver [157]. The stacked Ti/TiN/AlCu/Ti/TiN material utilized as electrodes have also been reported to reduce the RF loss [158], [159].

In this chapter, Cu-TWE of modulator is designed with Cu thickness of 2 μm. Since it is difficult to delineate Cu by subtractive etch due to the limited number of volatile Cu compounds, dual-damascene process was utilized to form the Cu TWE and the contact plugs [161]. Cu deposition and CMP process are included in dual damascene process. To avoid the dishing caused by the CMP process [162]-[164] on Cu surface, a latticed Cu surface pattern is designed for the Cu TWE of this silicon modulator. The inset (ii) of Figure 4.2 in section 4.2.1 shows the latticed Cu pattern. The size of each dielectric slot pattern is 3 μm × 8 μm. The maximum Cu unit size in the electrode is 15 μm × 15 μm, which can effectively reduce the Cu dishing [163]-[164].

HFSS, a commercial simulation software, was used to evaluate the RF loss of the latticed Cu electrode. Three kinds of metal electrodes are simulated, including the normal Al electrode, the normal Cu electrode and the latticed Cu electrode. CPW models were adopted in this simulation. All models are simulated with a Si substrate, which has permittivity of ε_r = 11.9 and resistivity of ρ = 1000 Ω·cm.

Between the Si substrate and the CPW layer, there is a 4 μm-thick oxide layer. The thickness of the CPW layer is 2 μm. To obtain a 50 Ω impedance match, the width of the central signal CPW was set to be 10 μm, and the gap between the signal and ground trace was set to be 6.4 μm. Assuming that both materials do not have any defects, the simulated result of insertion loss S21 and return loss S11 are shown in Figure 4.4. The insertion loss and the return loss of the electrical signal in the latticed Cu pattern are quite close to that in the normal Cu electrode at 40 GHz, which are both smaller than that in the normal Al electrode of different electrode lengths. These are caused by the lower resistivity of Cu (ρ_{Cu} = 1.72×10^{-6} Ω·cm) than that of Al (ρ_{Al} = 2.63×10^{-6} Ω·cm). The RF 6.4 dB-bandwidth is related to the EO 3 dB-bandwidth [165], [166]. The insertion loss of the latticed Cu electrode is less than 6.4 dB, and the return loss is less than −10 dB within 40 GHz when the electrode length is no more than 5 mm, which is longer than the length of latticed Cu electrode of our modulator. Therefore, this kind of latticed Cu electrode does not degrade the speed of our modulator within the range of 40 GHz.

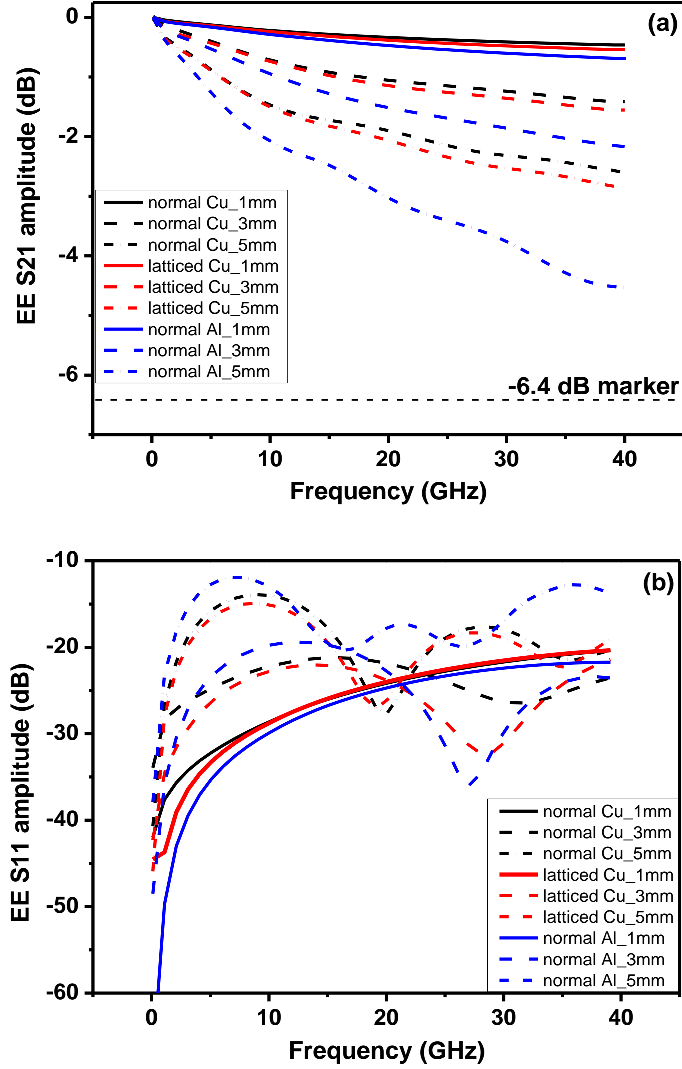


Figure 4.4 Simulated insertion loss S21 (a) and return loss S11 (b) of the normal Cu-TWE, the latticed Cu-TWE and the normal Al-TWE.

4.2.3 Modeling of unloaded/loaded Cu-TWE of modulator

In order to maximize the bandwidth of the optical modulator, the three main aspects required to be optimized are [106]-[107]: (1) microwave loss at high frequency, (2) the matching between microwave group index and the optical group index, and (3) the matching between the electrode characteristic impedance and the driver/terminator impedance. Silicon substrate of high resistivity of ρ = 1000 Ω·cm

is utilized to reduce the microwave loss. The modeling of modulator Cu-TWE with respect to the index matching and the impedance matching are described as follows.

The unloaded Cu-TWE is first analyzed. To evaluate the RF performance of the Cu-TWE varied with the signal trace width (W) and the gap (G) between the signal and the ground trace, simulations of the microwave group index and the characteristic impedance of the unloaded Cu-TWE were first performed. Coplanar waveguide (CPW) models were adopted in the simulation. All models are built on a high-resistivity silicon substrate. Between the silicon substrate and the Cu-TWE layer, there is an oxide layer of 4 μm-thick. The thickness of the Cu-TWE layer and the Cu contact plugs are both 2 μm. The silicon waveguide width is 500 nm and the slab height of the ridge waveguide is 100 nm. The main simulation parameters are shown in Table 4.1.

The simulation results of the unloaded Cu-TWE are shown in Figure 4.5. Figure 4.5(a) shows that the simulated microwave index generally increases with the increasing W and G. Larger gap would require larger trace width to obtain the same characteristic impedance as depicted in Figure 4.5(b). The simulation results are in accordance with the analytical model discussed in section 2.4.2 in Chapter 2.

Table 4.1 Simulation parameters of the Cu-TWE.

Parameter	**Symbol**	**Value**
Si permittivity	ε_r	11.9
Si substrate resistivity	ρ_{Si}	1000 Ω·cm
Cu resistivity	ρ_{Cu}	1.72×10^{-6} Ω·cm
Dielectric loss tangent of Si	$\tan\delta_{Si}$	0.015
Dielectric loss tangent of SiO_2	$\tan\delta_{SiO2}$	0.001

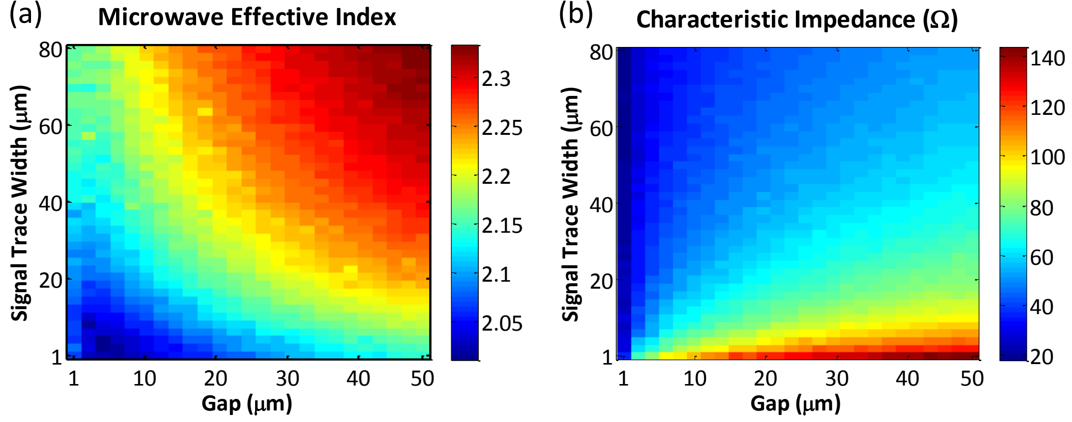


Figure 4.5 Simulated (a) microwave effective index, (b) characteristic impedance of unloaded CPW Cu-TWE model of modulator at 30 GHz frequency.

In the modulator of this thesis, the width (W) of the central signal CPW was set to be 10 μm, and the gap (G) between the signal and ground was set to be 6.4 μm to achieve a 50-Ω impedance matching.

In the actual model for modulator, the TWE is *p*-*n* junction loaded. In the *p*-*n* junction loaded Cu-TWE model, the *p*-*n* junction can be approximated by a series combination of the resistance and the depletion capacitance under the reverse bias voltage. The depletion capacitance decreases with increasing reverse bias voltage. This is caused by the carrier depletion out of the *p*-*n* junction area under a reversed bias voltage, and the effect of *p*-*n* junction on the Cu-TWE reduces with increasing bias voltage. Under high frequencies, the simultaneous matching of velocity and characteristic impedance can be calculated by the targeted *p*-*n* junction loaded characteristic impedance and index [106]-[107], as shown in Eq. (4.1) and (4.2) respectively,

$$Z_{ul} \cdot n_{ul} = Z_l \cdot n_l \tag{4.1}$$

$$n_l = n_{opt} \tag{4.2}$$

where Z_{ul} and Z_l denotes the unloaded and loaded characteristic impedances, respectively. n_{ul} and n_l denote the unloaded and loaded microwave group index, respectively. The targeted n_l equals to the optical group index n_{opt}, which is 4.18 at 1550 nm wavelength in this design. The modulator is driven by a standard 50 Ω microwave driver/terminator, and therefore Z_l = 50 Ω.

The loaded/unloaded capacitance, the unloaded inductance and the unloaded characteristic impedance can be calculated by Eq. (4.3)-(4.6), which has been discussed in section 2.6.2 of Chapter 2.

$$Z_{ul} = \sqrt{\frac{L_0}{C_0}} \tag{4.3}$$

$$L_0 = \frac{n_{opt} \cdot Z_l}{c} \tag{4.4}$$

$$C_0 = \frac{n_{ul}^2}{c \cdot Z_l \cdot n_{opt}} \tag{4.5}$$

$$C_L = \frac{n_{opt}^2 - n_{ul}^2}{c \cdot Z_l \cdot n_{opt}} \tag{4.6}$$

The calculated C_0 = 70 pF/m, L_0 = 696 nH/m, C_L = 208 pF/m, Z_{ul} = 99 Ω. From this model, a higher target unloaded characteristic impedance (or a lower loaded capacitance) would be designed for future optimization.

Finally, the simulated insertion loss S21 and return loss S11 of the loaded Cu-TWE of modulator at 0 V bias voltage are shown in Figure 4.6. The RF 6.4 dB-bandwidth is marked in Figure 4.6 as it is related to the EO 3 dB-bandwidth of the modulator [10-11]. The simulated bandwidth of the loaded 3mm-long Cu-TWE of the modulator at 0 V bias voltage is ~20 GHz due to the depletion capacitance of the *p*-*n* junction, which is in accordance with the estimated bandwidth using Eq. (2.54) in Chapter 2. The EE bandwidth of loaded Cu-TWE of the modulator will increase with increasing bias voltage. This is caused by the depletion capacitance that decreases with increasing bias voltage.

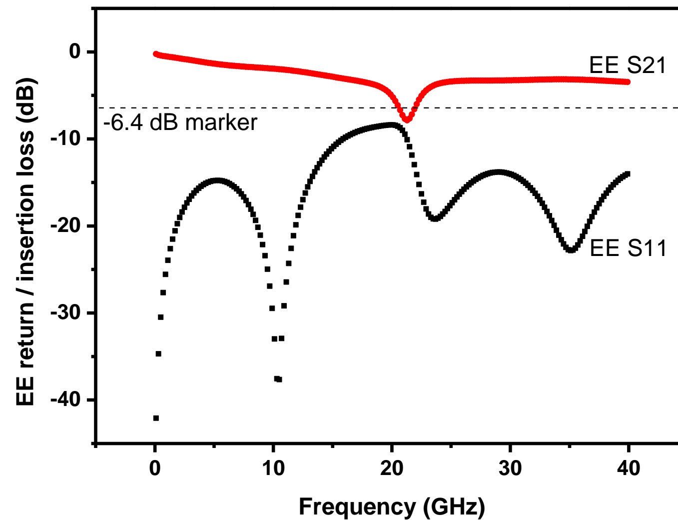


Figure 4.6 Simulated insertion loss S21 and return loss S11 of the loaded 3mm-long Cu-TWE of modulator at 0 V bias voltage.

4.3 Design of TO Tunable AWG with Cu Metallization

4.3.1 Motivation

AWG has become increasingly popular as MUX/DeMUX for WDM applications [167]-[171]. This is due to the fact that AWG-based devices have been proven to be capable of multiplexing/demultiplexing a high number of channels [168]-[171]. The increasing demand for bandwidth in optical communications has increased the interest for DWDM technology. This demand requires high performance AWG wavelength MUX/DeMUX with small channel spacing [172], [173]. The designed peak wavelength of AWGs with small channel spacing is more vulnerable to the wavelength shift/drift. Therefore, methods of stabilizing and tuning, such as precise positioning of AWGs on the ITU grid, or compensating for optical wavelength drift, are of great interest. Tunable AWGs based on silica [173], InP [174]-[178], and polymer [179]-[182] have been reported. However, tuning method for silicon AWG was not reported yet.

CMOS-compatible silicon photonics is becoming a promising technology to realize high performance photonics-CMOS integration system. Silicon AWG is a critical and extensively used optical component in the silicon optical communication networks. One of the major issues in using a high-index contrast platform such as SOI wafer for photonic devices is its sensitivity to dimensional variations. Dimensional deviations of the devices will cause a wavelength shift in the spectral response. AWGs are larger in size (few tens of micrometers), which

makes them much more vulnerable to different sources of dimensional variations, such as fabrication non-uniformity in the silicon layer thickness, and mask error. An intra-die average non-uniformity of silicon layer thickness (~0.5 nm) and its strong correlation with the peak wavelength shift (up to ~2 nm) of AWGs have been reported [183].

In this section, a tunable silicon AWG based on thermo-optic (TO) effect has been demonstrated. By taking advantage of the TO effect in silicon, thermal tuning can be utilized to compensate for non-uniformity. The wide ridge-waveguide and the narrow channel-waveguide are designed for reducing the impact of the fabrication non-uniformity. The thermal distribution simulation shows that a uniform heating can be achieved by the heater design, while the experiment results reveal that above 600 GHz channel tunability has been achieved.

4.3.2 Tunable AWG Design

An eight-channel 400 GHz silicon AWG is designed as the MUX/DeMUX. High-resistivity TiN material is used as the heater, while low-resistance Cu is used as contact plugs and electrode for the purpose of the photonics-CMOS integration [184]. The design parameters are shown in Table 4.2. Since the effective-refractive-index (n_{eff}) related optical performance of silicon AWG is ultra-sensitive to the fabrication tolerance and non-uniformity as described in introduction section, the following three designs are adopted to reduce the impact of fabrication non-uniformity, and to achieve a uniform heating and tuning.

First of all, the wide straight ridge-waveguide (0.8 μm-rib width) and the

narrow bended channel-waveguide (0.5 μm-width) are utilized. One advantage of the straight ridge-waveguide is the low optical transmission loss under TE mode. One advantage of the wide ridge-waveguide is the small impact of the waveguide thickness (rib thickness and slab thickness) on the waveguide effective-refractive-index (n_{eff}). Furthermore, wide rib dimension is used for reducing the fabrication non-uniformity impact on the waveguide n_{eff}. As shown in Figure 4.7, the slab thickness has a smaller impact on the n_{eff} of the ridge-waveguide with a wider rib, as compared to narrower rib. At the same time, a disadvantage of the ridge-waveguide is the high optical transmission loss of the bended waveguide. Bended ridge-waveguide with large radius is one solution to reduce the transmission loss, however, the large device size arising from the bended waveguide with large radius is not beneficial to the integration. Therefore, narrow channel-waveguide is used as the bended waveguide. Taper is used as the transition structure from the narrow channel-waveguide to the wide ridge-waveguide, as shown in inset i of Figure 4.12 in the Fabrication section. Besides, a wide heater (10 μm) is designed with small spacing (4 μm) to achieve a uniform heating on the silicon waveguide. The footprint of the heater is designed to cover the whole area of the arrayed waveguide to achieve a uniform heating as well. The fold line structure is designed for the heater. To reduce the heater resistance and hence the operating voltage, parallel structure of the left and right part of the heater is designed, as shown in Figure 4.12. In addition, adjacent deep trenches for for thermal insulation with other devices are designed around the heater.

Table 4.2 Design Parameters of the TO tunable silicon AWG

Parameter	**Symbol**	**Value**
Central wavelength	λ_0	1.55 µm
Channel spacing	$\Delta\lambda$	3.2 nm
Heater spacing	D_h	4 µm
Heater width	W_h	10 µm
Number of input channels	N_i	1
Number of output channels	N_o	8
Number of arrayed waveguide	N_w	23
Diffraction order	m	50
Path difference	ΔL	28 µm
Free spectral range	FSR	25 nm
Grating Pitch	d	2.8 µm

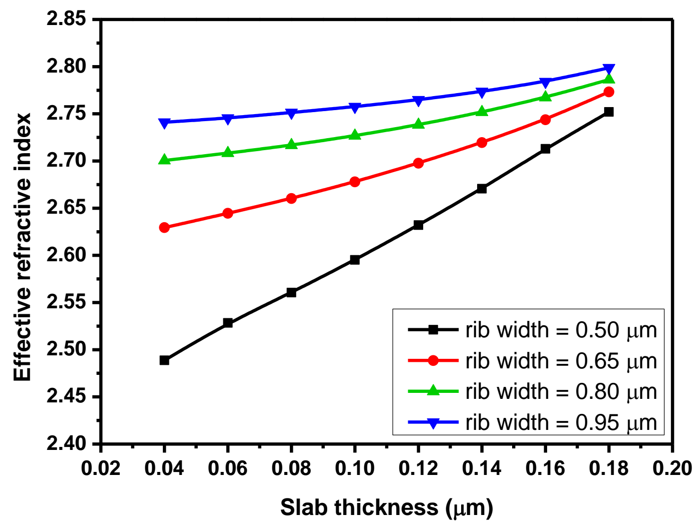


Figure 4.7 Simulated effective-refractive-index (n_{eff}) of the ridge waveguide with the different slab thicknesses and rib widths.

4.3.3 Thermal performance simulation and analysis

To optimize the heater structure for a uniform heating and investigate the thermal effect on the device, the cross-sectional thermal distributions under different bias voltages/powers on the TiN heater are simulated by COMSOL Multiphysics commercial software. The thermal conductivity of each material, which measures its ability to conduct heat, is an important parameter in the simulation. Figure 4.8(a) shows the thermal simulation structure, while Figure 4.8(b) shows the simulated result when a 40 V voltage (1.26 W power) is applied to the heater, and the silicon substrate is partially presented here. The minimum temperature shown in the scale bar is located at the bottom of the silicon substrate, which is not shown in Figure 4.8(b). The temperature of the Si waveguide is increased by ~53 K from the room temperature (298.15 K), which will lead to the thermal-induced wavelength shift ($\Delta\lambda$) of the device due to the TO effect. In addition, the simulated temperature of the Si waveguide under different bias voltages/powers with a step of 5 V on the TiN heater is shown in Figure 4.9. The result shows that the temperature of the Si waveguide is uniform with a variation of less than 1 K, which ensures the uniform tunability of the device.

The wavelength shift ($\Delta\lambda$) arising from the simulated heating temperature (ΔT) due to the TO effect can be calculated by Eq. (4.7), Eq. (4.8) and the TO coefficient of Si/SiO_2 ($(dn/dT)_{Si} = +1.84\times10^{-4}$ /K, $(dn/dT)_{SiO2} = +1.0\times10^{-5}$ /K),

$$\Delta\lambda = \frac{\Delta n_{eff}}{n_g}\lambda_0 \tag{4.7}$$

$$\Delta n_{eff} = \frac{\partial n_{eff}}{\partial n_{Si}}\Delta n_{Si} + \frac{\partial n_{eff}}{\partial n_{SiO_2}}\Delta n_{SiO_2} \tag{4.8}$$

where n_{eff} denotes the effective-refractive-index of the AWG, n_g the group index, and n_{Si} / n_{SiO2} the refractive-index of Si/SiO_2. The change in n_{eff} of the AWG (Δn_{eff}) is mainly caused by the change in refractive-index of Si (Δn_{Si}) and SiO_2 (Δn_{SiO2}), which is simulated using Mode Solver of Rsoft commercial software. The simulated $\Delta\lambda$ under different voltage/power compared with the measured $\Delta\lambda$ is shown in the Figure 4.22 in the characterization section.

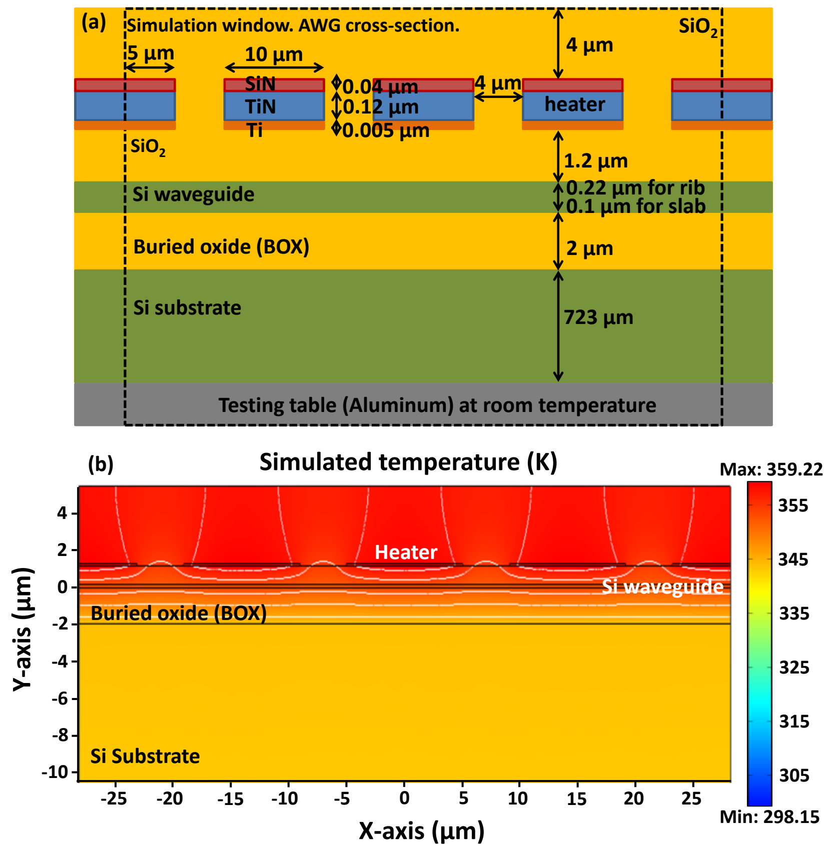


Figure 4.8 (a) Thermal simulation structure (not to scale). (b) Simulated cross-sectional thermal distribution when a 40V bias voltage (1.26 W power) is applied to the TiN heater. The temperature of the silicon waveguide is ~53K higher than the room temperature (298.15 K). The white line in the figure is the isothermal line. The silicon substrate is partially presented.

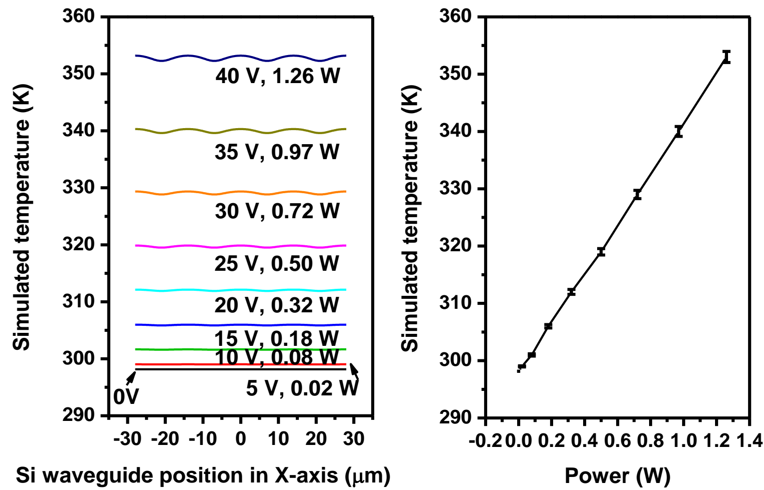


Figure 4.9 Simulated temperature distribution of the silicon waveguide under different bias voltages/powers on TiN heater. Less than 1 K temperature variation is observed from the error bar.

4.4 Fabrication Process

This silicon optical modulator, the Ge-on-Si PD and the tunable AWG were monolithically integrated on an 8-inch SOI wafer with top Si layer of 220 nm and BOX of 2 μm, using a CMOS-compatible process integration flow, in terms of both thermal budget and fabrication feasibility. After *p* and *n* compensation implantations for the modulator were done, the waveguide was formed by double anisotropic silicon dry etching processes. The fabrication process of doping compensation [138] for the optical modulator is shown in Figure 4.10. Figure 4.11 shows the scanning electron microscope (SEM) images of the silicon waveguide of the modulator and PD. The insets of Figure 4.12 show the SEM images of the silicon waveguides of the AWG. The waveguide tip width is about 200 nm for coupling with lensed fibers. The slab height of the ridge waveguide is 100 nm. The waveguide width for modulator and PD is 500 nm. The waveguides of AWG are

designed with the wide straight ridge-waveguide (0.8 μm-rib width) and the narrow bended channel-waveguide (0.5 μm-width).

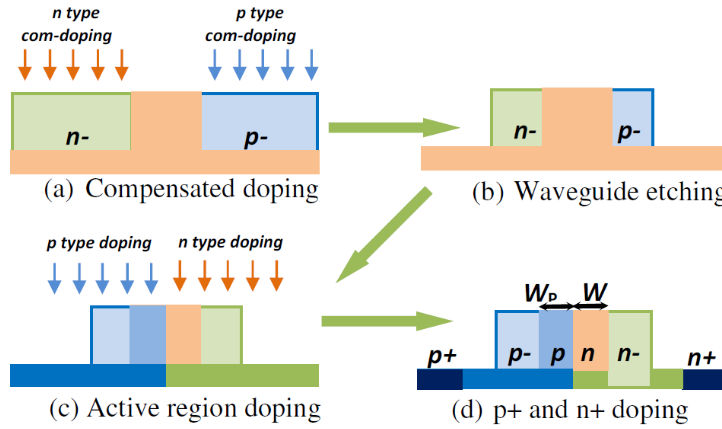


Figure 4.10 The fabrication process of the doping compensation for optical modulator [138].

Four more implantations (p^{++}, p, n, n^{++}) were performed for the formation of modulator *p-n* junction. Based on the actual implantation condition, the *p* and *n* doping levels in both compensation areas are estimated as ~ 3×10^{16} cm^{-3}, and the *p* and *n* doping levels in the modulator *p-n* junctions are estimated as ~ 4×10^{17} cm^{-3}. For the formation of the Ge vertical *n-i-p* photodetectors (VPDs), p^{+} and *p* implantations were performed. The implanted dopants in silicon were activated using a rapid thermal anneal (RTA) at 1030 ℃ for 5 seconds prior to Ge epitaxy. After depositing a 60 nm-thick oxide layer, windows were etched in the oxide using an anisotropic dry etch followed by a wet etch to ensure that the Si surface is not damaged by the reactive ion etching (RIE) process. Ge with 500 nm-thick [185], 3 μm-wide and 5 μm / 10 μm / 20 μm-lengths were then selectively grown in an ultrahigh vacuum chemical vapor deposition (UHVCVD) epitaxy reactor at 550 ℃. n^{+} implantation was then conducted on the Ge regions, and activated by RTA at 550

°C for 5 minutes. The Ge of the PD is shown in Figure 4.11(d).

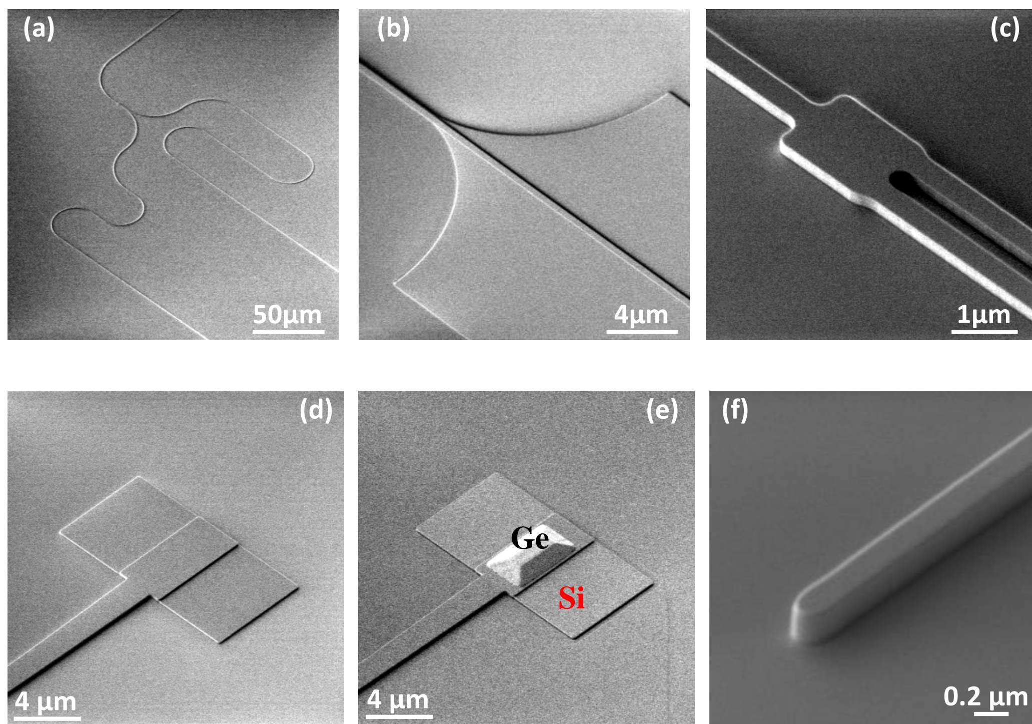


Figure 4.11 SEM images of modulator waveguide and Ge-on-Si PD. (a) Output part of the modulator. (b) Ridge waveguide of the modulator phase shifter. (c) 1 × 2 MMI combiner/splitter of the modulator. (d) Ridge waveguide of the PD. (e) Ge of the PD. (f) Waveguide nano-tip.

After the SiO_2 dielectric layer, the SiN stop layer and the SiO_2 dielectric layer were deposited in sequence and polished, and Ti/TiN was deposited and etched as heater. 0.12 μm-thick TiN is used as heater material for its high resistivity, and 5 nm-thick Ti was fabricated underlying the TiN heater for improving the material adhesion to oxide. 0.4 μm-thick SiN is deposited as via etching stop layer. The microscope image of the tunable AWG is shown in Figure 4.12. The insets of Figure 4.12 show the SEM images of the silicon waveguide, heater and Cu electrode.

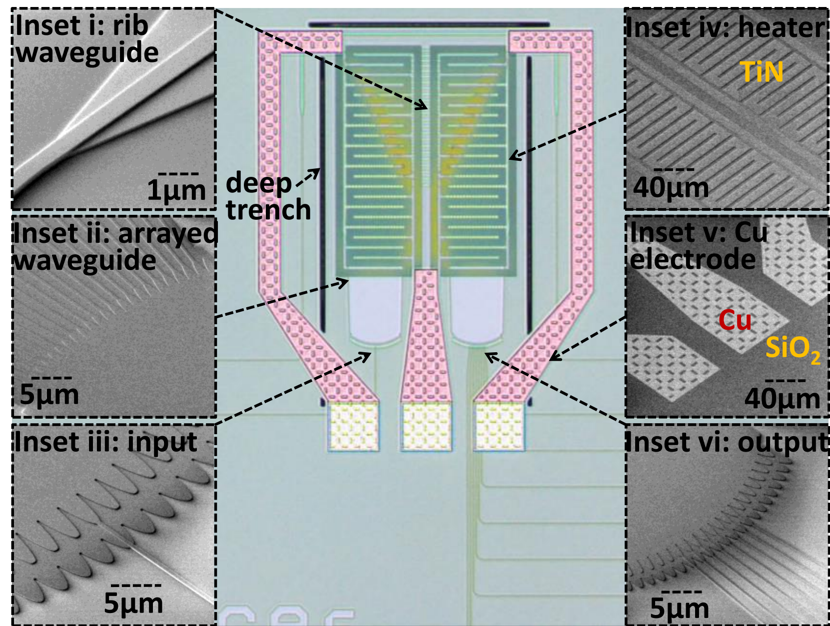


Figure 4.12 Microscope image of the tunable silicon AWG. Inset i: SEM image of the rib waveguide. Inset ii: SEM image of the arrayed waveguide. Inset iii: SEM image of the input waveguide. Inset iv: SEM image of the TiN heater. Inset v: SEM image of the Cu electrode. Inset vi: SEM image of 8 channels output.

From the photonics-CMOS integration perspective and to achieve better RF perfomance, Cu was selected as the contact plugs and the electrode material. Since it is difficult to delineate Cu by subtractive etch due to the limited number of volatile Cu compounds, dual-damascene process was utilized to form the Cu electrode and the contact plugs [161]. The process flow of Cu dual dual-damascene process is shown in Figure 4.13. Cu-TWE trench and contact plug are dry etched in sequence, and then TaN barrier layer and Cu seed layer are deposited. After Cu plating, Cu CMP and annealing are conducted. To avoid the dishing caused by CMP process on Cu surface, a latticed Cu surface pattern is designed [186], as shown in the inset v of Figure 4.12, and Figure 4.14(a) and (c).

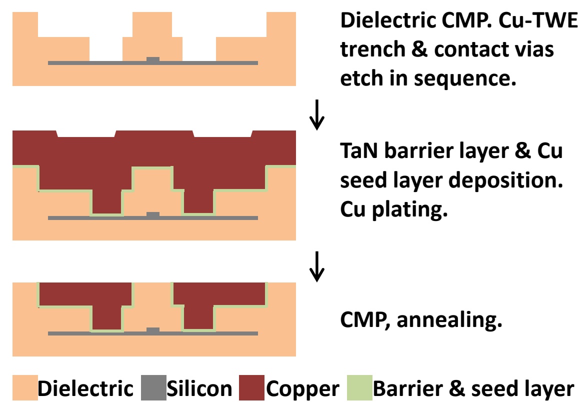


Figure 4.13 The process flow of Cu dual-damascene process.

After SiO_2 dielectric layer was deposited and polished, the trench of Cu electrode and the contact hole to Si/Ge/heater were dry etched in sequence. To avoid the diffusion of Cu into the Si/SiO_2 layer, a 250 Å-thick TaN barrier layer was deposited first. A 1500 Å-thick Cu seed layer was next deposited by PVD followed by 6 μm-thick Cu layer by ECP. After removing the excess Cu by CMP, the Cu electrode and contact plugs were finally formed after annealing. The structures of the Cu electrode are presented in Figure 4.12 and Figure 4.14, with the inset v of Figure 4.12, and the Figure 4.14(a) and (c) showing the image of the Cu electrode surface after Cu CMP. A 5000 Å-thick SiO_2 was deposited as a dielectric layer over the Cu electrode subsequently. After the opening of the bond-pad, a thin Al layer was formed on the bond-pad pattern to avoid the oxidation of Cu electrode and to protect the testing probe. The plating of the UBMs/microbumps will be shown in Chapter 5 where discusses electro-photonic 3D integration based on silicon photonic TSV interposer. Finally, more than 100 μm-deep Si trench was etched to hold optical lensed fiber for coupling with the nano-taper of Si waveguide, and also for thermal insulation around the heater, as shown in Figure 4.12.

Figure 4.14(b) shows the cross-sectional SEM image of the modulator phase shifter with Cu electrode and contact plugs. The inset shows the cross-section of the silicon ridge waveguide and the silicon slab height is ~ 100 nm. Figure 4.14(d) shows the cross-sectional transmission electron microscope (TEM) image of the Ge-on-Si PD with Cu electrode and contact plugs. Cross-sectional SEM images of the heater, the Si waveguides of the AWG, the Cu electrode and contact to heater are shown in Figure 4.15.

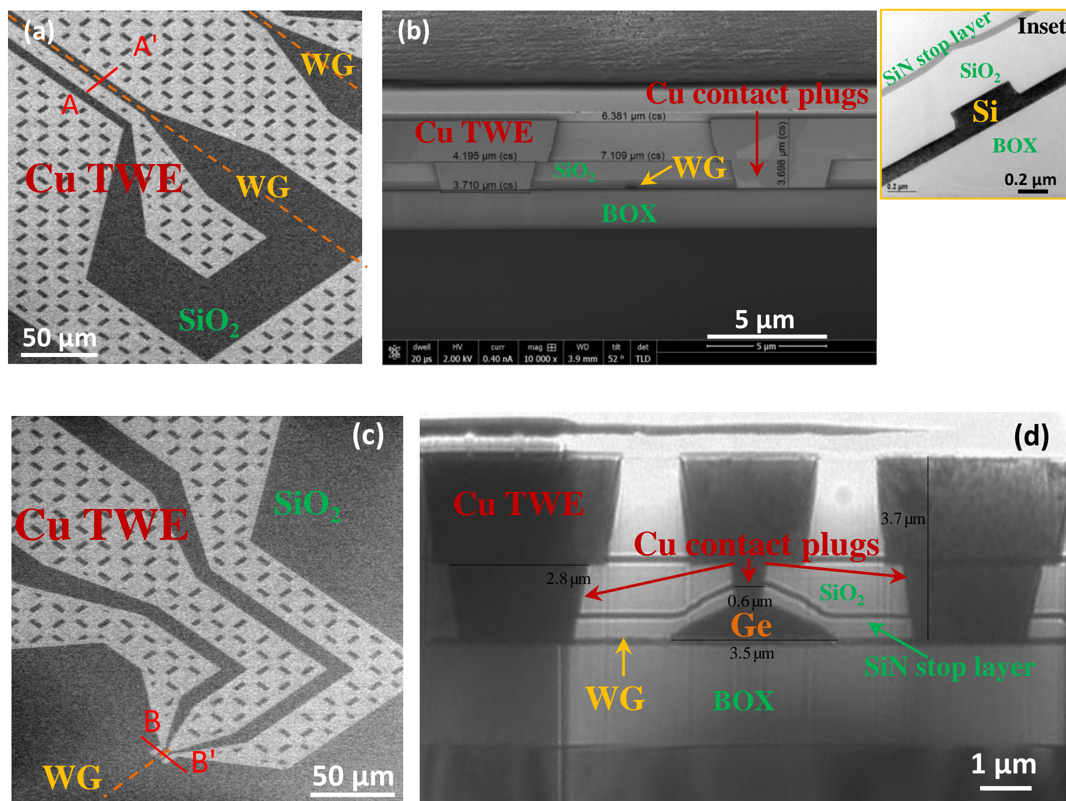


Figure 4.14 Images of the modulator and the PD with the Cu TWE. (a) SEM image of the top view of the modulator Cu TWE. (b) Cross-sectional SEM image of the modulator phase shifter at the A-A' line in (a). Inset: Cross-sectional TEM image of the silicon ridge waveguide. (c) SEM image of the top view of the PD Cu TWE. (e) Cross-sectional TEM image of the PD at the B-B' line in (c).

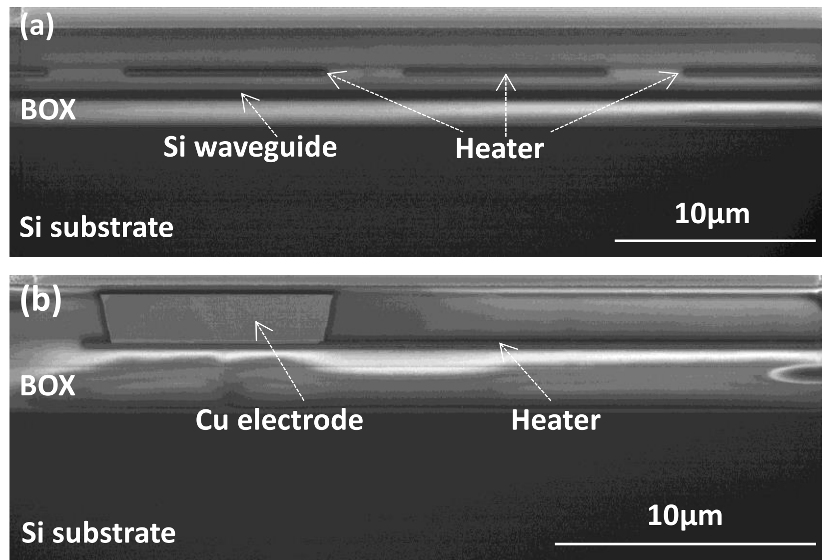


Figure 4.15 Cross-sectional SEM images of (a) the heater and the Si waveguides of the AWG. (b) The Cu electrode of the AWG and the Cu contact to heater.

4.5 Characterization

4.5.1 DC characterization of the interposer

Two lensed fibers with 2.5 μm focal-length were used to characterize the optical performance of this interposer.

- ***Cu contact***

Figure 4.16 shows the result of the Cu-induced propagation loss of the silicon waveguide. When the Cu-to-waveguide distance is more than 1.5 μm, the Cu-induced propagation loss is less than 0.1 dB/cm. Compared with the other losses, such as waveguide propagation loss and coupling loss, the Cu-induced propagation losses in the modulator, PD and AWG are negligible as their Cu-to-waveguide distance is designed to be more than 1.5 μm. The 2 μm-thick Cu sheet

resistance is shown in Table 4.3 (left). It is 18.3 ± 0.3 mΩ/square, lower than Al sheet resistance of 25.3 ± 0.4 mΩ/square. It also reveals that Cu is better than Al as the electrode and contact material of silicon photonic interposer. The Cu-to-Si contact resistivity was also measured and shown in Table 4.3 (right). Taking the optical modulator as an example, the contact size is 4 × 3000 μm^2 for both *n*- and *p*-contact. Based on the Cu-to-Si contact resistivity, the contact resistances of the modulator for both *n*- and *p*-contact are 15 mΩ and 19 mΩ, respectively.

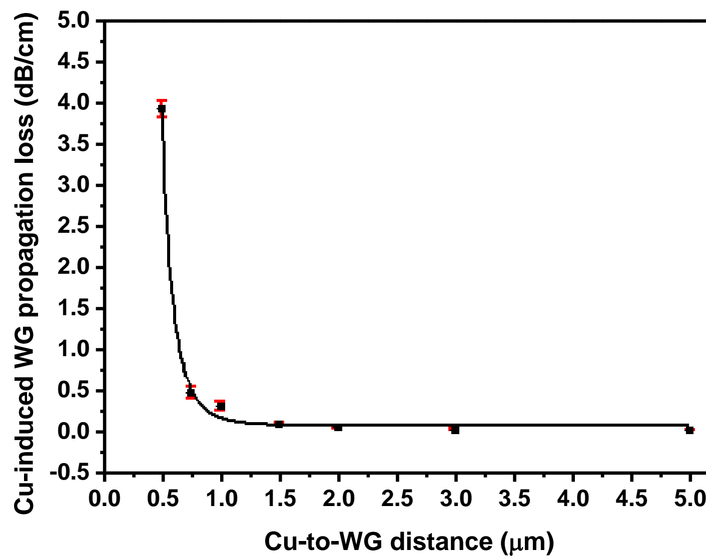


Figure 4.16 Cu-induced waveguide propagation loss.

Table 4.3 Sheet resistance of Cu and Al, and Cu-to-Si contact resistivity.

Sheet resistance (mΩ/square) with 2 μm-depth and 5 μm-width		**Cu-to-Si contact resistivity (Ω· μm²)**	
Cu	Al	*n*-contact	*p*-contact
18.3±0.3	25.3±0.4	178.4±3.3	232.9±4.5

- ***Optical MZI modulator***

The measured output spectra of the silicon optical modulator under different reversed bias voltages are shown in Figure 4.17(a). The bias is applied on one arm of the modulator. The FSR of the asymmetric MZI is 1.85 nm, which is dependent on ΔL. Without any bias, the optical extinction ratio of this modualtor is ~ 28 dB. With the reversed bias, the carrier is pumped out of the waveguide and the optical loss reduces. Thus, the optical extinction ratio decreases due to the unbalance of optical power in two modulator's arms with the increase of the reversed bias. The measured insertion loss of the modulator is ~ 9 dB as shown in Figure 4.17(a), while the dynamic loss is shown in the inset of Figure 4.17(a), which is the average measurement result. Based on the waveguide loss of 1.2 dB (undoped waveguide propagation loss ~ 0.2 dB/mm), 2 MMI loss of 0.6 dB and double fiber-to-waveguide coupling loss of 3.2 dB, the optical loss caused by implantation is 1.3 dB/mm. In Figure 4.17(b), a π-phase shift can be realized under 6.0 V reversed voltage for a 3 mm-long phase shifter, which corresponds to a modulation efficiency ($V_\pi L_\pi$) of 18.5 V·mm with a standard deviation of 0.5 V·mm. With an increase in the applied reversed voltage from −2 V to −10 V, the efficiency is reduced from 11.1 V·mm to 21.5 V·mm, which is caused by the depletion of free carriers in the *p*-*n* junction. In the deep depletion region, the modulation efficiency becomes lower because there are fewer free carriers left in the depletion region. The efficiency is improved compared with our previous Al-modulator [146] mainly due to the sheet resistance of Cu that is 28% smaller than that of Al, as shown in Table 4.3. Under the same DC bias measurement condition, the Cu-modulator *p*-*n*

junction experiences a higher DC voltage compared with the Al-modulator, therefore Cu-modulator has a larger phase shift.

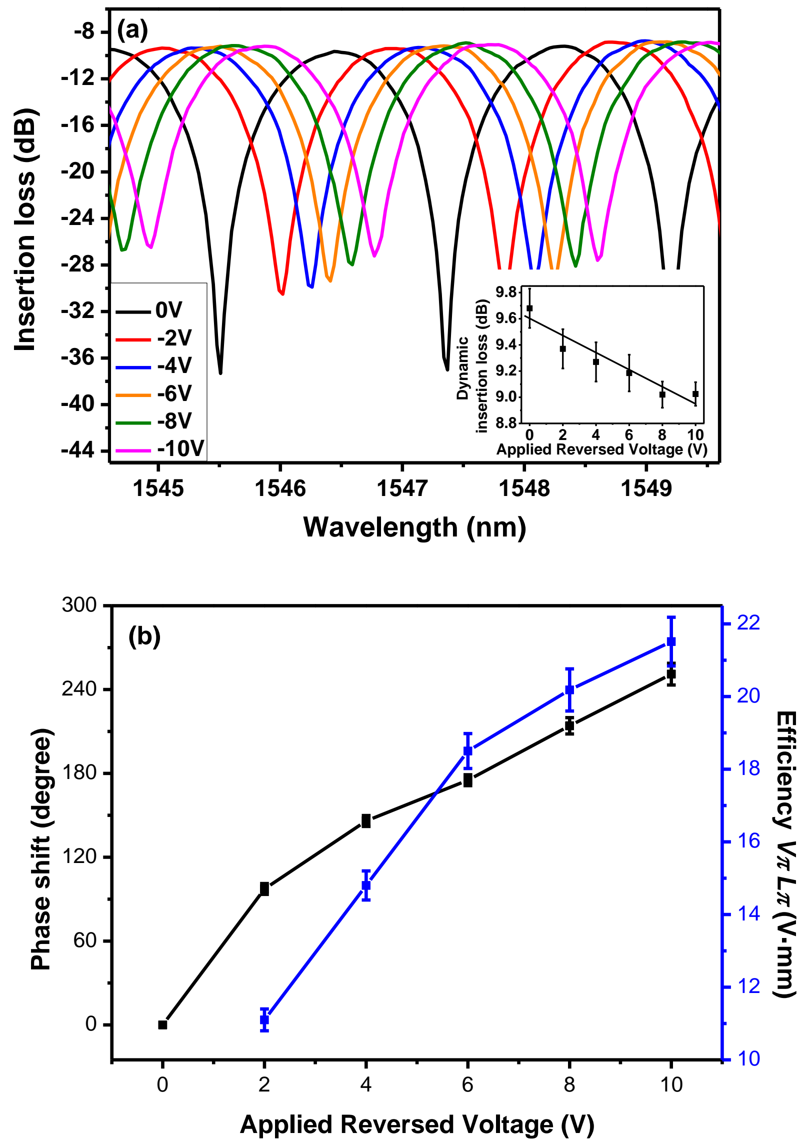


Figure 4.17 (a) Output spectra of silicon modulator with 3 mm-long phase shifter, Inset: dynamic insertion loss. (b) Phase shift and efficiency $V_{\pi}L_{\pi}$ of the phase shifter under different applied reversed voltages of the 3 mm-long phase shifter.

- ***Ge-on-Si PD***

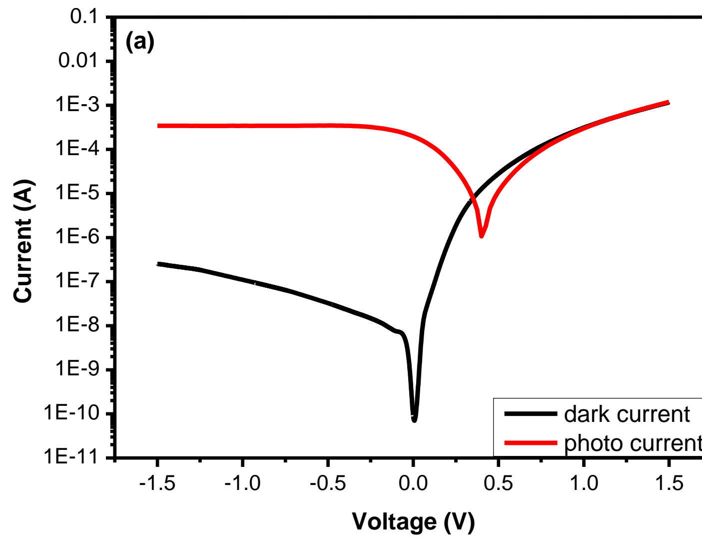


Figure 4.18 The measured dark current and photo current of the 3 µm-wide and 5 µm-long Ge-on-Si vertical PD.

The waveguide loss (undoped waveguide propagation loss) and the fiber-to-waveguide coupling loss are the same as described in the above modulator DC measurement section. The measured dark current and photo current of the 3 µm-wide and 5 µm-long PD under 1550 nm wavelength TE mode are shown in Figure 4.18. The dark current is ~100 nA under −1 V bias voltage. The responsivity of 3 µm-wide Ge PD with various Ge lengths and different tpyes of contact via for TE mode is shown in Figure 4.19, which ranges from 1.0 A/W at 1510 nm to 0.15 A/W at 1590 nm. It is noted that discrete contact plugs improve the responsivity of PD with different Ge lengths. For 5 µm-long PD, the responsivity under 1550 nm wavelength TE mode is improved from 5.8 A/W to 6.5 A/W, while the responsivity of 20 µm-long PD is improved from 7.2 A/W to 9.2 A/W. Compared with the conventional single via contact, the optical absorption of the discrete contact plugs

is reduced, since the metal contact area to Ge is reduced, and correspondingly the responsivity is improved.

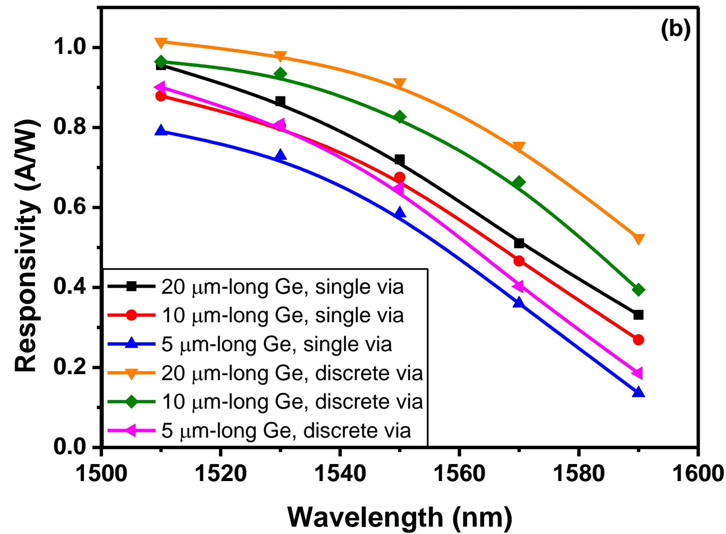


Figure 4.19 The measured responsivity of the 3 μm-wide PD with various Ge length and contact plugs type for TE mode.

- ***TO tunable AWG***

The measured output spectra of 8 channels output of the silicon AWG before heating are shown in Figure 4.20. The channel spacing is 3.2 nm and the minimum optical loss is 3.6 dB. The insertion loss consists of the waveguide loss of 1.4 dB (undoped waveguide propagation loss ~ 0.2 dB/mm) and the star couplers loss of 2.2 dB. The measured output spectra of four of the 8 channels of the silicon AWG under different bias voltages/powers are shown in Figure 4.21. The measure wavelength shifts under different bias powers are shown in Figure 4.22, which are in agreement with the simulated wavelength shifts. Above 600 GHz channel tunability is achieved. For reducing the power consumption, an optimization method can be utilized. By removing the underlying Si substrate to form a

suspended device using SiF_6 etching, the power consumption can be significantly reduced by 98% [187]. It is realized by preventing heat from leaking out of the waveguides due to the presence of the air isolation layer.

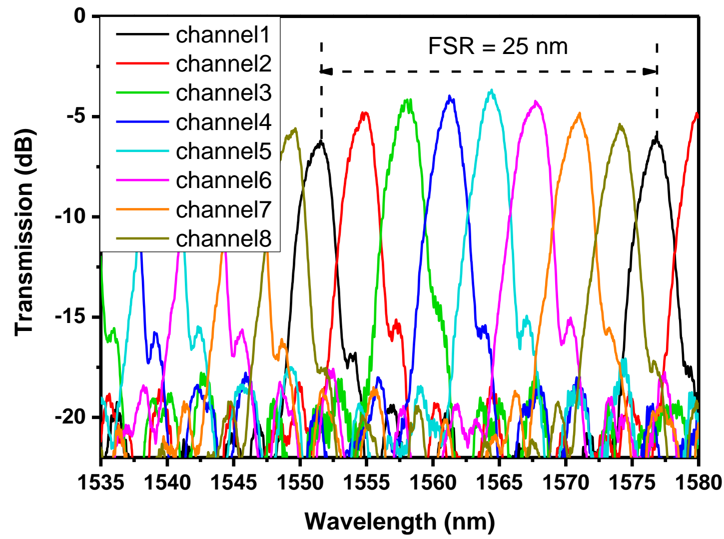


Figure 4.20 Transmission of 8 channels output before heating.

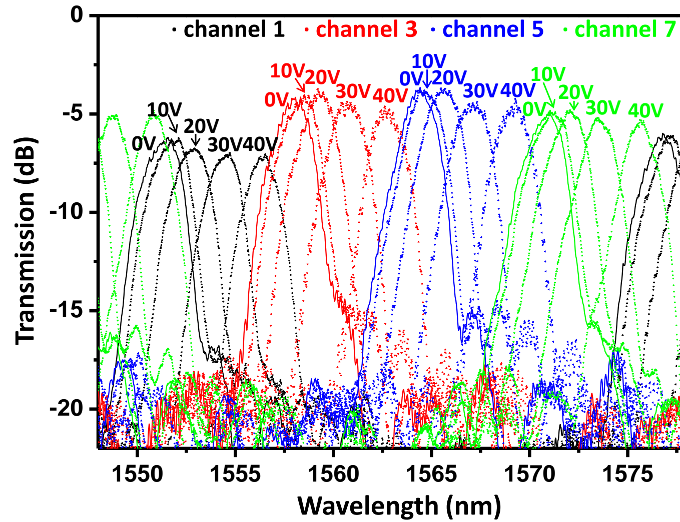


Figure 4.21 Transmission of output channel 1, 3, 5 and 7 of the AWG under 0 V (0 W), 10 V (0.08 W), 20 V (0.32 W), 30 V (0.72 W), and 40 V (1.26 W).

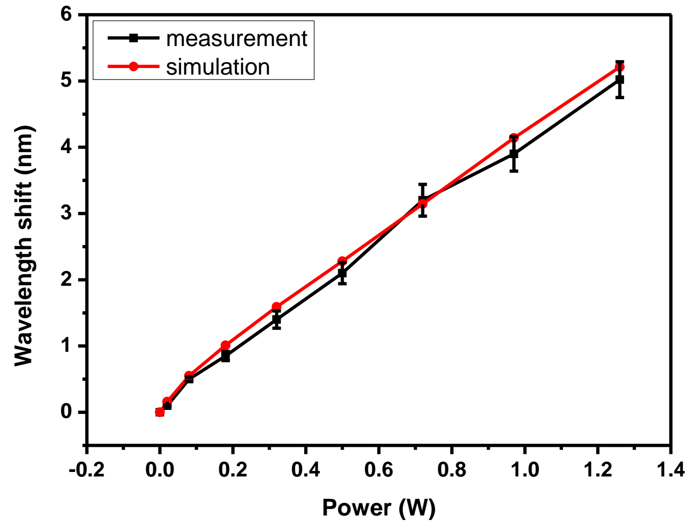


Figure 4.22 Measured and simulated wavelength shift under different bias powers.

4.5.2 AC characterization of the interposer

- ***Optical MZI Modulator***

The small signal response of the silicon optical modulator with 3 mm-long phase shifter was measured using Agilent N4373C Lightwave Component Analyzer (LCA) which has a maximum bandwidth of 40 GHz. The input signal was adopted by a probe with 67 GHz bandwidth which was pinned on one end of the Cu electrode. The 50 Ω matching impedance as a terminator was connected on the other end of Cu electrode by another probe with 67 GHz bandwidth to reduce the signal reflection. The measured EO bandwidth of silicon modulator is shown in Figure 4.24. Under a V_{bias} of −5 V, the 3 dB bandwidth of this modulator is up to 37 GHz. In order to get the eye diagram results, a high speed electrical signal coming from a 50/56-Gbps Anritsu Pattern Generator MP1822A was firstly amplified through a 67 GHz high speed driver. It was applied to the modulator device-under-

test (DUT) through a bias tee with 60 GHz bandwidth and the input probe with 67 GHz bandwidth. A continuous-wave light coming from the 1550 nm tunable laser was firstly amplified through an erbium doped fibre amplifier (EDFA) and a band pass filter (BPF), and then it was modulated by adding a non-return-zero (NRZ) pseudorandom binary sequence (PRBS) $2^{31}-1$ signal under $V_{bias} = -5.0$ V with $V_{pp} =$ 3.5 V. The output optical signal was amplified again and collected by an Agilent Digital Communications Analyzer (DCA) after the optical filter. The eye-diagram measurement setup is shown in Figure 4.23. The data rate of the eye diagram reaches 50 Gbps with a dynamic extinction ratio of 7.08 dB, as shown in Figure 4.25(a). Dynamic ER is 8.88 dB under 40 Gbps-data rate as shown in Figure 4.25(b). A performance comparison of this work with other MZI modulators is shown in Table 4.4. The efficiency and dynamic ER are better than other reported modulators. Compared with other reported modulators, the efficiency is improved from ~27-35 V·mm to 18.5 V·mm due to the lower resistivity of Cu. The dynamic ER under 50 Gbps-data rate is improved from ~3.1-5.56 dB to 7.08 dB. The dynamic ER under 40 Gbps-data rate is improved from ~3.2-6.4 dB to 8.88 dB.

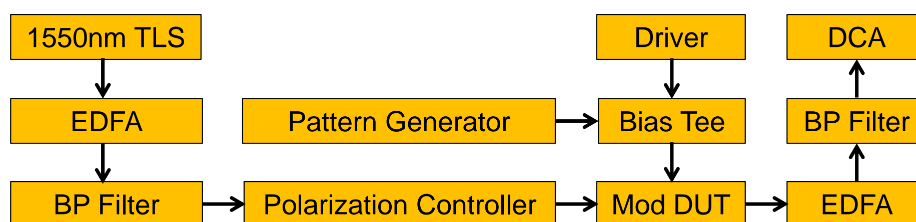


Figure 4.23 The eyediagram measurement setup of the modulator.

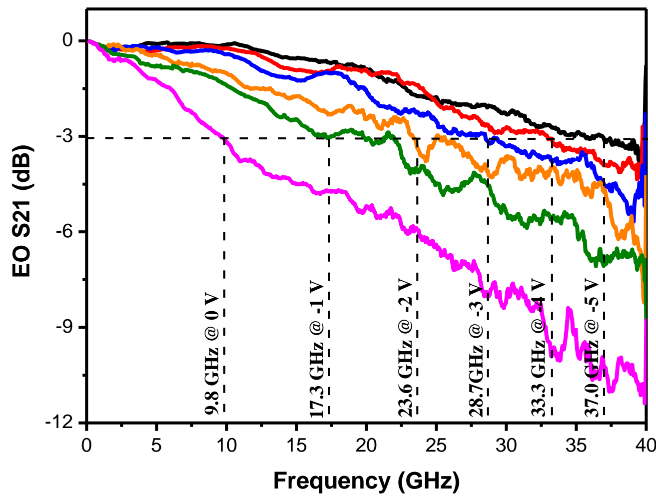


Figure 4.24 The EO bandwidth of the silicon modulator.

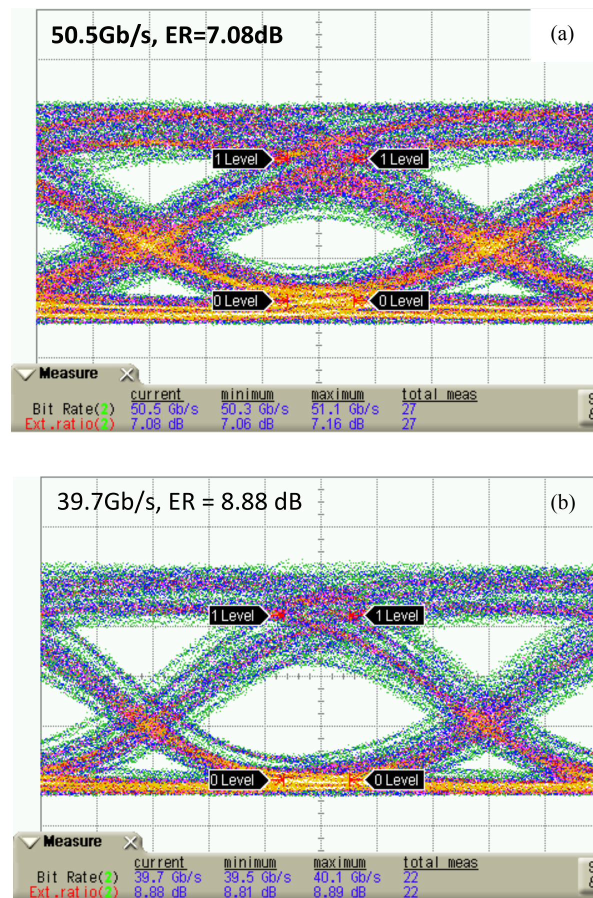


Figure 4.25 Eye-diagram at (a) 50 Gbps-data rate, and (b) 40 Gbps-data rate of the silicon modulator.

Table 4.4. Comparison with MZI modulators with TWE.

p-n junction type, wavelength	Electrode material	Phase shifter length (mm)	V_{pp}, and V_{bias} (V)	Efficiency (V·mm)	EO BW (GHz)	Data rate (Gbps)	ER (dB)
Lateral *p-n*, 1550 nm [160]	NA	1	6.5 V, −4 V	28	NA	50	3.1
Lateral *p-n*, 1550 nm [146]	Al	4	7 V, −5 V	26.7	25.6	50	5.56
Lateral *p-n*, 1529-1565 nm [147]	Al	2	6 V, −3 V	NA	NA	40	4.9-6.4
Lateral *p-n*, 1550 nm [148]	Al	1 / 2	3.5 V, −3 V	31	30 / 20	40	4.1 / 4.7
Lateral *p-n*, 1310 nm [149]	Al	3	1.5 V, 0 V	24.3 / 26.4	30	50	3.4
p-i-p-i-n diode, 1550 nm [158]	Ti/TiN/Al Cu/Ti/TiN	4.7 / 0.95	7 V, Bias NA	35	20 / 40	40	6.6 / 3.2
Lateral *p-n*, 1530 nm [159]	Ti/TiN/Al Cu/Ti/TiN	3.5 / 1	6.5 V, Bias NA	27	NA	40	10 / 3.5
This work, Lateral *p-n*, 1550 nm	Cu	3	3.5 V, −5 V	18.5	> 30	50.3-51.1 39.5-40.1	7.06-7.16 8.81-8.89

- ***Ge-on-Si vertical PD***

Small signal microwave performance was measured through Agilent N4373C

LCA which has a maximum bandwidth of 40 GHz. The measured bandwidth is 33.7 GHz under −3 V bias voltage, and is shown in Figure 4.27(a). In order to get the eye diagram results, a high speed electrical signal coming from a 50/56-Gbps Anritsu Pattern Generator MP1822A was firstly amplified through a 67 GHz high speed driver. It was applied to an external modulator through a bias tee with 60 GHz bandwidth and the input probe with 67 GHz bandwidth. A continuous-wave light coming from the 1550 nm tunable laser was modulated by adding a NRZ PRBS $2^{31}-1$ signal under $V_{bias} = -3.0$ V with $V_{pp} = 3.5$ V. The modulated optical signal is applied into the PD DUT after amplified by EDFA and BPF. The output electrical signal was collected by an Agilent DCA. The eye-diagram measurement setup for the PD is shown in Figure 4.26. The data rate of the eye-diagram reaches 30 Gbps as shown in Figure 4.27(b). The data rate of this interposer is limited by the speed of the PD. The PD testing setup in our laboratory needs to be improved to reduce the impact of the testing cable on the measured data rate of the PD. The total length of the RF cable applied is ~1.5 m and as a result the loss of a high-speed electrical signal is high. If the length of RF cable can be reduced in the future, it is possible for this integrated circuit to achieve a data rate of up to 45 Gbps.

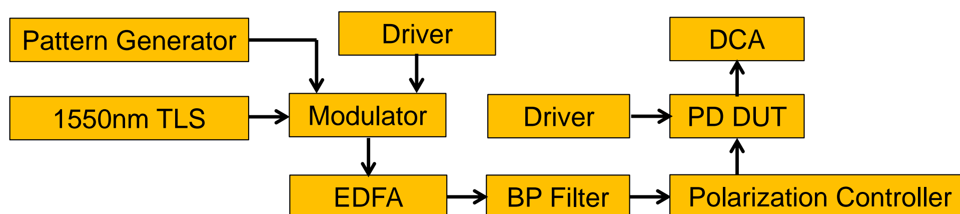
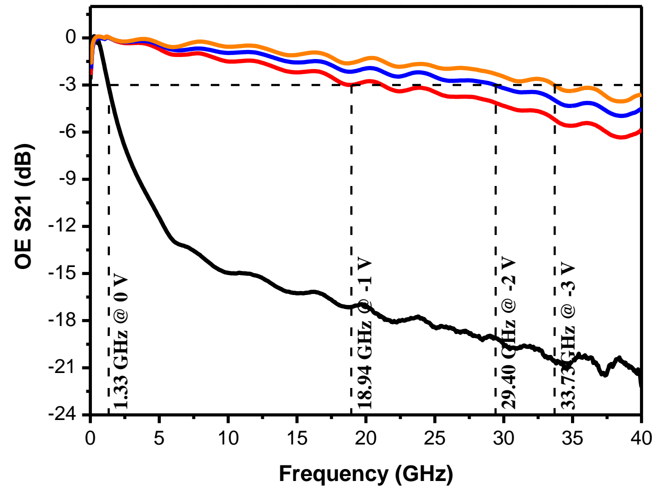


Figure 4.26 The eye diagram measurement setup of the PD.



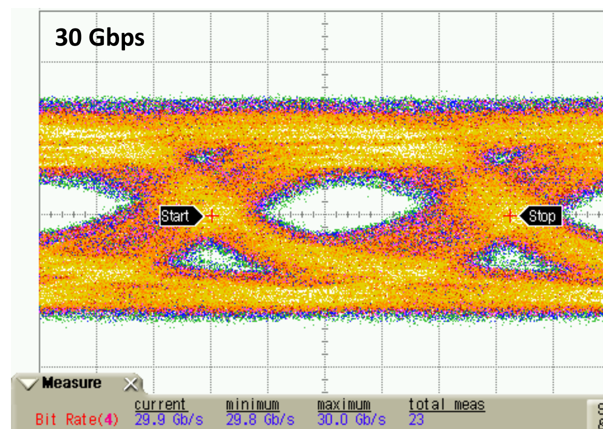


Figure 4.27 (a) The measured OE bandwith of the 3 μm-wide and 5 μm-long Ge-on-Si vertical PD. (b) The eye-diagram of the PD.

A comparison of the main performance with other reported silicon photonic interposers is shown in Table 4.5. Noted that Si photonics technology is progressing from Al-BEOL to Cu-BEOL at technology nodes beyond 0.18 μm to maintain standardization with the established CMOS technology methodologies. The main improvement achieved in this thesis is the high speed performance due to the design and fabrication of traveling-wave electrode via Cu-BEOL. Compared with the 25 Gbps-data rate of the other reported photonic interposers, the data rate in this thesis is 50.5 Gbps and 30 Gbps for the modulator and PD, respectively. Moreover, a TO

tunable Si AWG with above 600 GHz channel tunability is designed and fabricated in this interposer for the first time.

Table 4.5. Comparison with other silicon photonic interposers.

Affiliation and conference	process	devices	performances
University of Washington, Luxtera. OFC [49]	200 mm SOI wafer Al-BEOL 0.18 μm technology node	MZI/ring modulator *p-i-n* Ge PD	bandwidth: 19 GHz data rate: 25 Gbps dynamic ER: NA dark current: 433 nA @ -1V responsivity: 0.53 A/W
STMicroelectronics, Luxtera. IEDM [52]	300 mm SOI wafer Cu-BEOL 90 nm technology node	MZI modulator *p-i-n* Ge PD	bandwidth: 20 GHz data rate: 25 Gbps dynamic ER: NA dark current: 100 nA @ -1V responsivity: 0.85 A/W
IBM. IEDM [155]	300 mm SOI wafer Cu-BEOL 90 nm technology node	MZI modulator *p-i-n* Ge PD	bandwidth: 20 GHz data rate: 25 Gbps dynamic ER/dark current/responsivity: NA
This work, OFC [Author's conference paper 1]	200 mm SOI wafer Cu-BEOL 0.18 μm technology node	MZI modulator *p-i-n* Ge PD tunable Si AWG	bandwidth: 37/33.7 GHz data rate: 50.5/30 Gbps dynamic ER: 7.08 dB dark current: 100 nA @ -1V responsivity: 0.63 A/W TO tunability: > 600 GHz

4.6 Conclusion

A silicon Cu-photonics interposer is explored in this chapter, consisting of the

monolithically integrated silicon MZI optical modulator, Ge-on-Si PD and TO tunable AWG MUX/DeMUX of the integrated optical communications. Modeling of Cu TWE of modulator is conducted. Up to 37 GHz-bandwidth and 33.7 GHz-bandwidth are enabled on the stand-alone MZI modulator and Ge-on-Si PD by TWE via Cu-BEOL, respectively. A 50 Gbps data rate with 7.08 dB extinction ratio is achieved by the modulator. A 30 Gbps data rate is realized on the integrated interposer. Above 600 GHz tunability is reached for the TO tunable AWG MUX/DeMUX. From design and experiment, it is demonstrated that Cu TWE with low resistance and skin effect provides better RF performances in high speed active devices. A process flow is designed and developed for the silicon photonic interposer with monolithically integrated EO and TO devices featuring Cu-BEOL. This work has established the needed Cu-BEOL/metallization based RF silicon photonic devices toolbox for high performance photonics-CMOS integration.

Chapter 5 Electro-Photonic 3D Integration based on Si Photonic TSV Interposer

5.1 Introduction

As described in Chapter 4, a silicon photonic interposer with monolithically integrated optical modulator, PD and TO tunable AWG has been explored and experimentally demonstated, and the cross-sectional schematic of the proposed 3D silicon photonics-CMOS O/E IC integration system is shown in Figure 4.1. In this chapter, the modeling and fabrication process of the 3D EPIC integration system based on the silicon photonic TSV interposer are investigated. An electronic chip with microwave transmission line based on Cu-RDL process is presented. The flip-chip bonding of the silicon photonic TSV interposer and the electronic chip is developed. This 3D electro-photonic integration based on Si photonic TSV interposer is experimentally demonstrated and characterized for the first time.

5.2 Design and modeling

Catering to the electro-optical testing conditions in our laboratory, a demonstration-purpose 3D electro-photonic TSV integration module is designed, and the cross-sectional schematic is shown in Figure 5.1. The silicon photonic interposer in Figure 5.1 has been described in Chapter 4, while the TSVs embedded in this photonic interposer form the “silicon photonic TSV interposer”. The microwave electrical signal transmits through the transmission line fabricated in the electronic chip, and then vertically through the microbumps/UBMs and the TSVs to drive the

photonic devices. The optical signal from the testing fiber is coupled by the nano-tip waveguide coupler into the photonic devices. Silicon optical modulator and Ge-on-Si PD are integrated for experimentally evaluating the RF performance of this 3D photonic architecture. A TO tunable silicon AWG is integrated as well, for experimentally evaluating the TO performance of this 3D photonic architecture, and also acting as the MUX/DeMUX device in the optical WDM applications.

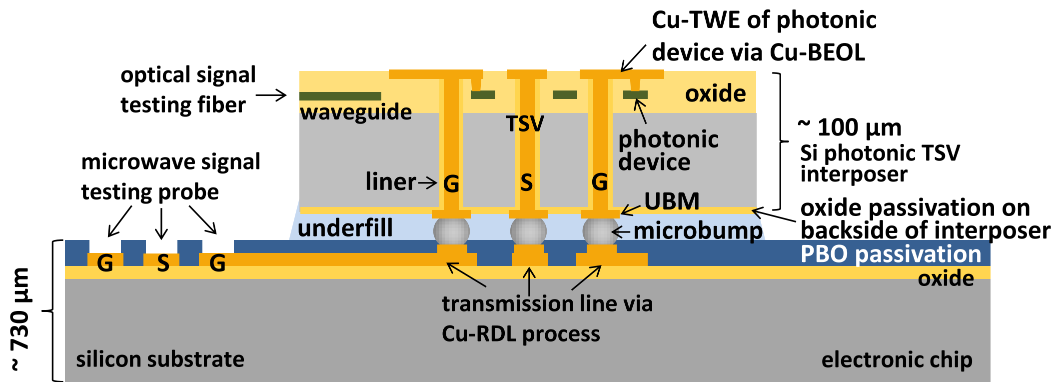


Figure 5.1 Cross-sectional schematic of the chip-level integration module.

Modeling of the Cu-TWE of the photonic device has been discussed in section 4.2.3 in Chapter 4, while modeling of the TSVs, the UBMs/microbumps, the transmission lines in the electronic chip, and the 3D electro-photonic TSV integration module are described in section 5.2.1.

Before the modeling of this 3D integration module, some design parameters limited by our present fabrication conditions need to be addressed first as follows. (1) TSV with smaller depth provides the shorter signal path and hence the smaller insertion loss, therefore the TSV depth is designed to be 100 µm, which is the smallest fabricable depth limited by our present thin wafer handling technology. (2)

At present, the highest TSV aspect ratio in 200 mm wafer can be fabricated in our lab is 5:1, which is limited by the seed layer deposition capability of our PVD equipment. Therefore the diameter of TSV can be fabricated is no less than 20 μm. (3) Due to the mismatch of CTEs between the Cu-TSV and the surrounding dielectric layer and Si substrate, the higher wafer warpage/stress arises from the higher density/smaller pitch of TSV. Risks of wafer cracking and fabrication equipment damage arise from the high wafer warpage/stress. During the fabrication recipe setup, TSV center-to-center pitch no less than 5 times of TSV diameter (no less than 20 μm in this thesis) is found to be safe for our equipment and wafer. Therefore, the center-to-center pitch of TSV can be fabricated is no less than 100 μm.

Although the TSV depth has been designed to be 100 μm, and the diameter and center-to-center pitch of TSV can be fabricated is no less than 20 μm and 100 μm, respectively, the following modeling results provide the future optimization parameters.

5.2.1 Modeling of TSV and UBM/microbump in the SOI interposer

GSG-TSV modeling is based on the CPW model as described in section 2.3 and 2.4 in Chapter 2. SOI wafer with silicon substrate of high resistivity of ρ = 1000 Ω·cm is utilized to reduce the microwave loss. The oxide liner thickness, the TSV diameter and the TSV center-to-center pitch are variables in this modeling. The simulated insertion loss S21 and the return loss S11 of the GSG-TSV with the variable liner thickness and TSV diameter are shown in Figure 5.2. In this model,

the TSV depth is fixed to be 100 μm. Noted that smaller insertion loss and return loss can be achieved with the smaller TSV diameter, while the oxide liner thickness has a minor impact on the insertion and return losses. The TSV diameter is designed to be 20 μm, which is the smallest diameter can be fabricated in our lab when the TSV depth has been designed to be 100 μm, and hence the TSV center-to-center pitch can be fabricated is no less than 100 μm.

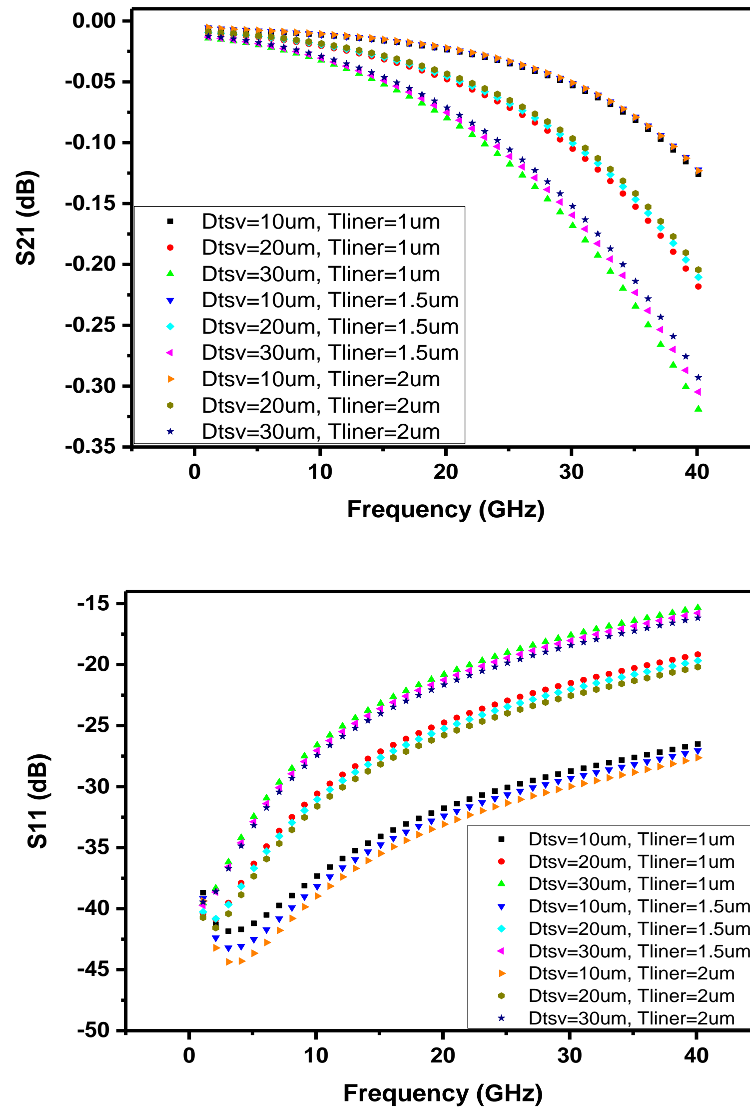


Figure 5.2 Simulated insertion loss S21 and return loss S11 of GSG-TSV with the variable liner thickness and TSV diameter.

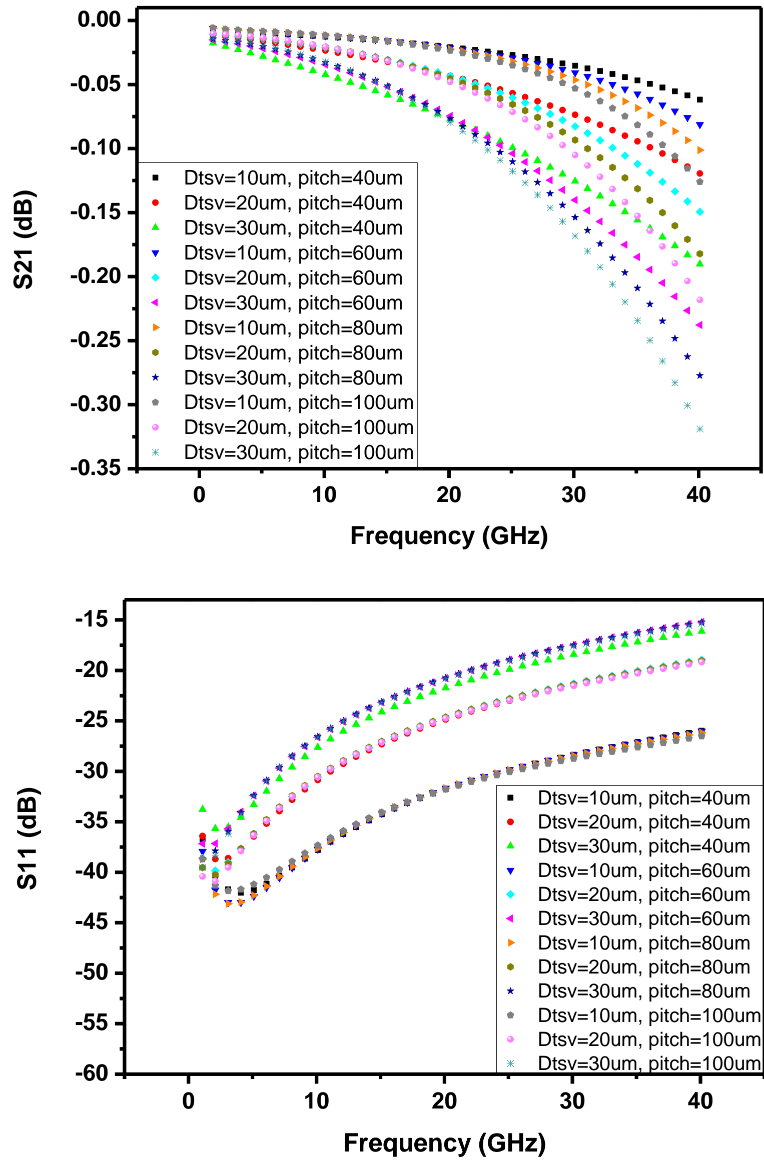


Figure 5.3 Simulated insertion loss S21 and return loss S11 of GSG-TSV with the variable TSV diameter and TSV center-to-center pitch.

The liner thickness in this thesis is set to be 1 μm. The simulated insertion loss S21 and return loss S11 of the GSG-TSV with the variable TSV diameter and TSV center-to-center pitch are shown in Figure 5.3. At low frequency, TSV transmission characteristic is dominated by capacitance, therefore smaller insertion loss and return loss can be achieved by the larger TSV pitch under a fixed TSV diameter. At high frequency, TSV transmission characteristic is dominated by inductance,

therefore smaller insertion loss and return loss can be achieved by the smaller TSV pitch under a fixed TSV diameter. For achieving a better high frequency characteristic, TSV center-to-center pitch is designed to be 100 μm, which is the smallest pitch that can be fabricated with reduced risk of wafer cracking and fabrication equipment damage arise from the high wafer warpage/stress.

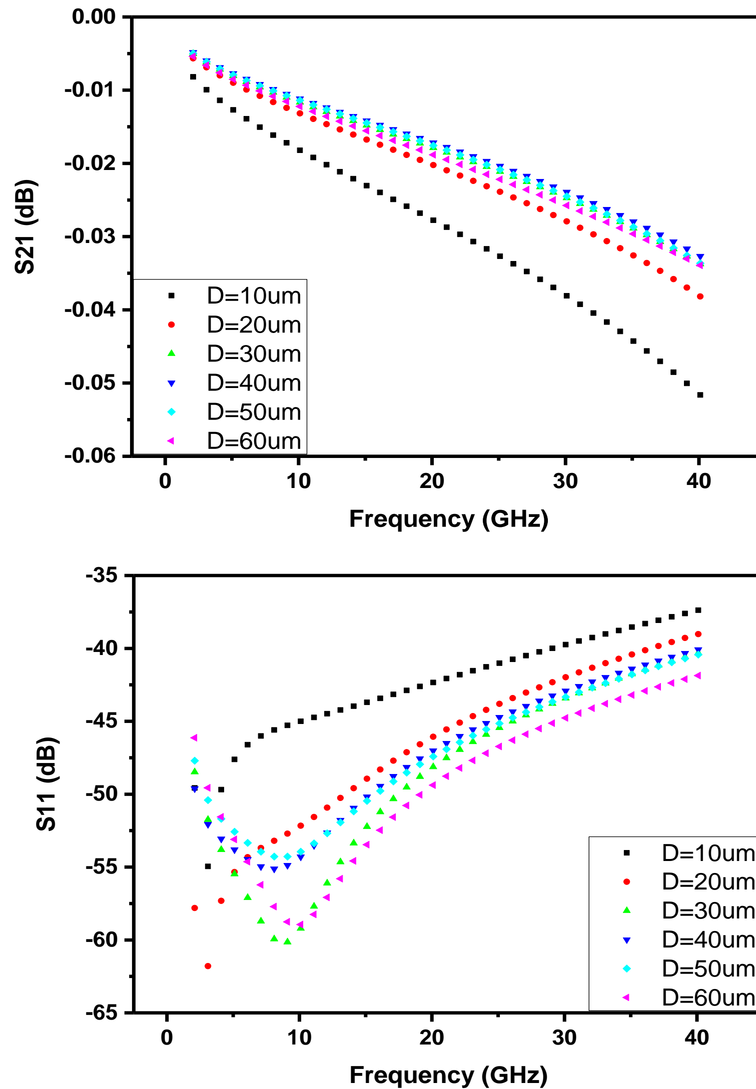


Figure 5.4 Simulated insertion loss S21 and return loss S11 of the GSG-solder (UBM/microbump) with the variable diameter.

The materials of the UBM are Cu/Ni/Au, and the materials of the microbump

are Cu/Ni/SnAg. The flip-chip underfill material U8443-14 is filled in the space around the UBMs/microbumps, for the electrical insulation and the mechanical stability purpose. The UBMs are located on the TSV backsides, and the microbumps located on the electronic chip are bonded with the UBMs, therefore the UBM/microbump center-to-center pitch is also designed as 100 μm. The UBM height is 5 μm, and the microbump height equals to its diameter. The simulated insertion loss S21 and return loss S11 of the GSG-solder (UBM/microbump) with the variable UBM/microbump diameter are shown in Figure 5.4. Noted that smaller insertion loss and return loss can be generally achieved with the larger solder diameter under 100 μm center-to-center pitch. Microbump diameter is designed to be 40 μm, since lowest insertion loss is achieved when the diameter is 40 μm, as noted from Figure 5.4.

5.2.2 Electronic chip with microwave Cu-RDL

The microwave Cu-RDL is based on the CPW model as described in section 2.4 in Chapter 2. Different from the Cu-BEOL process discussed in the modulator Cu-TWE design and fabricaton in Chapter 4, the microwave transmission line in the electronic chip is fabricated using the Cu-RDL process, which will be discussed in section 5.3 Fabrication. Latticed surface pattern is not needed since the CMP process is not introduced in the Cu-RDL process. Normal planar Cu surface can be fabricated by the Cu-RDL process. Silicon wafer with silicon substrate of high resistivity ρ = 4000 Ω·cm is utilized to reduce the microwave loss. A 3 μm-thick oxide layer underlying the Cu layer is adopted to reduce the microwave loss as well. The simulated insertion loss S21 and return loss S11 of the 3 mm-long microwave

Cu-RDL with the variable signal trace width (W) and gap (G) between the signal trace and ground trace are shown in Figure 5.5. W = 30 μm and G = 20 μm are designed for achieving the lower insertion loss and return loss. Compared with the above modeling on GSG-TSV and GSG-UBM/microbump, the long Cu-RDL (3 mm-long) caused the major microwave loss in the 3D TSV integration module.

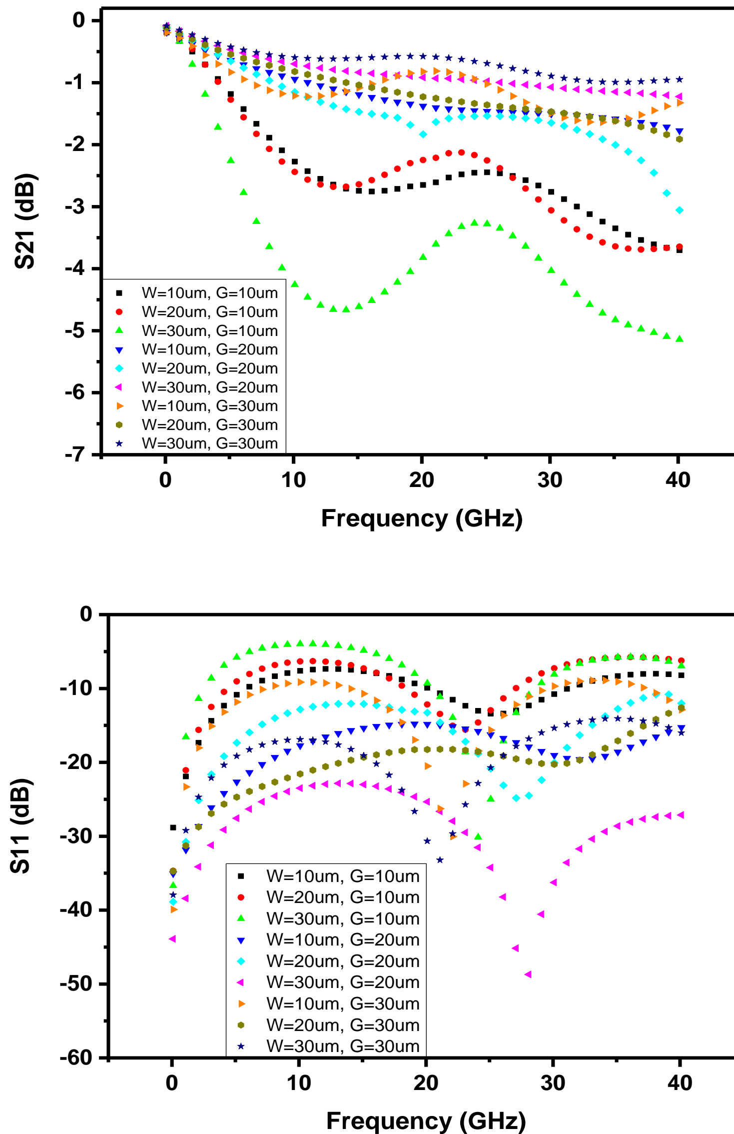


Figure 5.5 Simulated insertion loss S21 and return loss S11 of the 3 mm-long GSG-Cu-RDL with the variable signal trace width (W) and gap (G) between the signal trace and ground trace.

5.2.3 Modeling of the electro-photonic 3D TSV integration module

Based on the preceding modeling of the GSG-TSV, GSG-UBM/microbump and microwave transmission line in the electronic chip using Cu-RDL process, the model setup for the 3D electro-photonic TSV integration module in HFSS is partially shown in Figure 5.6. The main design parameters of this 3D TSV integration module are summarized in Table 5.1. The simulated EE insertion loss S21 and return loss S11 of the unloaded and the *p-n* junction loaded 3D electro-photonic TSV integration module are shown in Figure 5.7(a) and (b), respectively. The *p-n* junction doping condition is derived from the modulator design presented in Chapter 4. Noted that above 40 GHz bandwidth can be achieved for the unloaded module, while 9.35 GHz bandwidth can be achieved for the *p-n* junction loaded module at 0 V bias voltage, due to the depletion capacitance of the *p-n* junction. The EE bandwidth of this loaded 3D TSV integration model will increase with increasing bias voltage. This is caused by the depletion capacitance that decreases with increasing bias voltage. Compared with the simulated bandwidth (~20 GHz) of the loaded 3mm-long Cu-TWE of the modulator at 0 V bias voltage shown in Figure 4.6 in Chapter 4, the bandwidth in this 3D TSV integration system reduces by ~10 GHz. This is mainly caused by the microwave loss arises from the long Cu-RDL transmission line (~5 mm for the modulator) in the electronic chip.

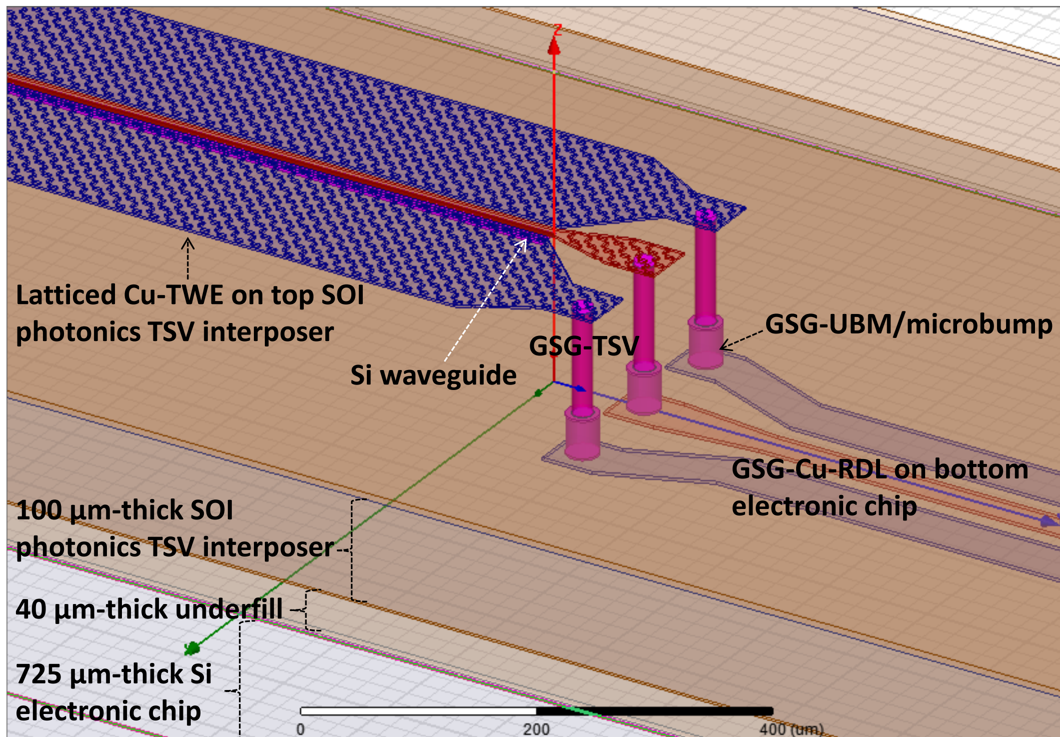


Figure 5.6 Partial model setup of the 3D electro-photonic TSV integration module in HFSS.

Table 5.1 Main design parameters of the 3D TSV integration module.

Parameter	**Value**
TSV diameter	20 µm
TSV depth	100 µm
TSV liner thickness	1 µm
UBM/microbump diameter	40 µm
TSV/UBM/microbump center-to-center pitch	100 µm
Thickness of Cu-RDL in the electronic chip	3 µm
Thickness of Cu-BEOL in the SOI photonic TSV interposer	2 µm
Thickness of the oxide layer beneath the Cu-RDL	3 µm
Si substrate resistivity of the SOI photonic TSV interposer	1000 Ω·cm
Si substrate resistivity of the Si electronic chip	4000 Ω·cm

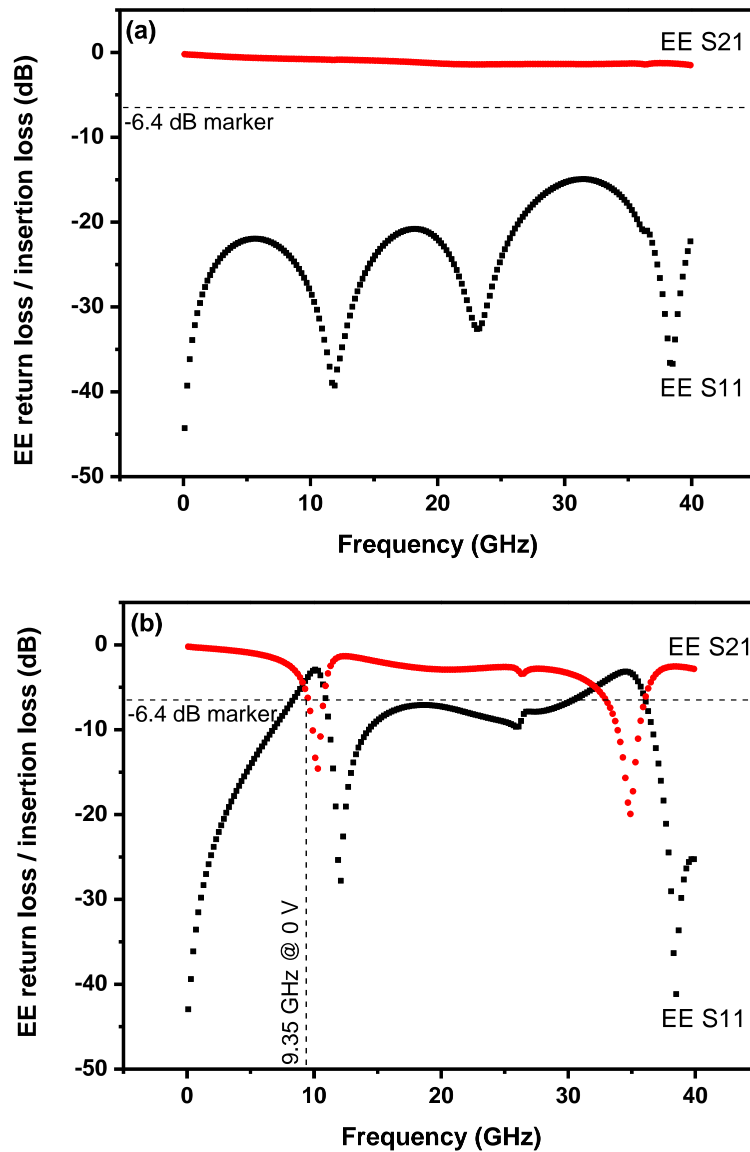


Figure 5.7 Simulated nsertion loss S21 and return loss S11 of the (a) unloaded and (b) *p*-*n* junction loaded 3D electro-photonic TSV integration module.

5.3 Fabrication

5.3.1 Silicon photonic TSV interposer

The fabrication of the photonic devices in the interposer (optical MZI modulator, Ge-on-Si PD, and TO tunable AWG using Ti heater) with Cu metallization using

Cu-BEOL process has been developed as described in section 4.4 in Chapter 4. The advantages of the TSV-middle process compared with the TSV-first and TSV-last have been discussed in section 2.2.1 in Chapter 2, and therefore TSV-middle process is utilized in the silicon photonic TSV interposer. After the fabrication of the photonic devices, the oxide dielectric layer was deposited and polished. The single-damasecene process was utilized to form the Cu contact plags: the contact holes were etched, followed by barrier layer/seed layer PVD and Cu ECP, and finally the Cu contact plugs were formed after Cu annealing and CMP. The SiN stop layer and the oxide dielectric layer were deposited, and then TSVs with 20 μm-diameter and 100 μm-depth were etched, as shown in Figure 5.8(a). After the barrier layer/seed layer PVD, Cu ECP, annealing and CMP, TSVs were finally formed as shown in Figure 5.8(b). The tilted X-ray inspection image of TSVs is shown in Figure 5.8(c), good Cu fillings without any defects can be observed. To fabricate the Cu-BEOL, and the contact vias to TSV and device contact plugs, the SiN stop layers and the oxide dielectric layers were deposited, and the Cu dual-damascene process was adopted, as described in section 4.4 in Chapter 4.

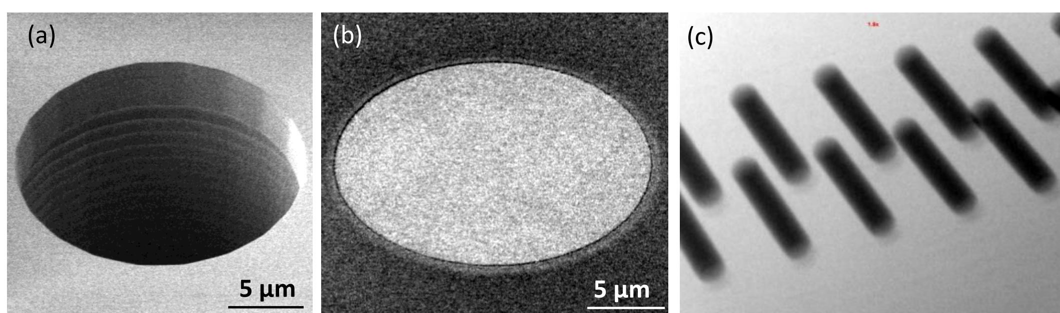


Figure 5.8 (a) SEM image of TSV hole etch. (b) SEM image of TSV after Cu CMP. (c) Tilted X-ray inspection of Cu-TSVs with 20 μm-diameter and 100 μm-depth, good Cu fillings without any defects are observed.

The cross-sectional SEM image of TSV integration with the Cu-BEOL metallization of the photonic device is shown in Figure 5.9. The TSV diameter is 20 μm, and the depth is ~100 μm. The thickness of the Cu-BEOL metallization of the photonic device is 2 μm.

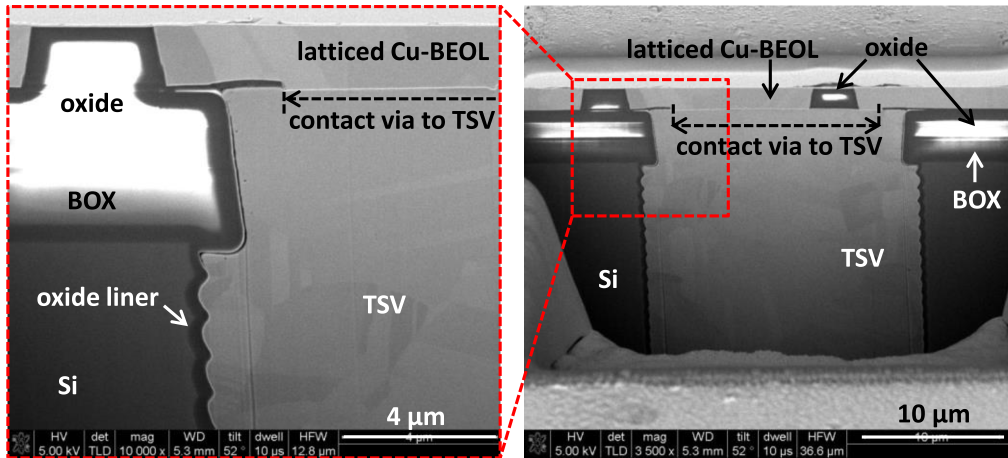


Figure 5.9 Cross-sectional SEM image of TSV integration with the Cu-BEOL metallization of the photonic device.

To reveal the backside of TSVs, temporary bonding technology using thermal plastic material is utilized for thin wafer handling. In the case of the photonic wafer, for coupling the testing fiber to the nano-tip waveguide coupler, the deep trenches with ~100 μm-depth need to be fabricated at the edge of each chip, close to the nano-tip waveguide coupler. To avoid the wafer from breaking arising from the air voids in the deep trenches during the temporary bonding and following processes in the vacumm chamber, a two-step etching of deep trench is designed, namely frontside (FS) deep trench etch before temporary bonding and backside (BS) deep trench etch after UBM/microbump plating. After the Cu-BEOL process, 8 μm-deep FS trenches were etched, followed by temporary bonding of the photonic TSV

wafer to a carrier wafer using thermal plastic material. After the TSVs' backside was revealed by backgrinding process, oxide was deposited at low temperature as the passivation layer for the electrical isolation purpose. The passivation opening to TSV was dry etched, and followed by the Ti barrier layer and Cu seed layer PVD. Cu/Ni/Au UBMs shown in Figure 5.10(a) were fabricated using the ECP process, and the barrier/seed layer is wet etched after the ECP process. A 10 μm-thick photoresist was coated for the ~90 μm-deep backside deeptrench etch of the Si substrate, and then the TSV wafer was de-bonded. The backside deep trench is shown in Figure 5.10(b).

In normal flip-chip bonding technology, microbumps are fabricated on the top wafer, while UBMs are fabricated on the bottom wafer. In this thesis, UBMs are fabricated on the top photonic TSV wafer because of the backside deep trench etch process, since it is difficult for photoresist coating to cover the spherical microbump with radius of tens of micrometers. The flip-chip bonding for this photonic interposer which is different from the traditional technology will be discussed and developed in section 5.3.3.

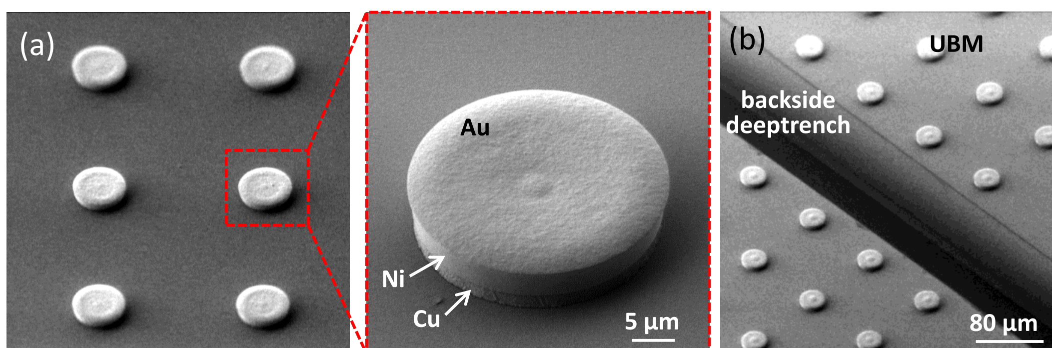


Figure 5.10 SEM images of (a) UBM and (b) backside deeptrench.

5.3.2 Electronic chip with microwave Cu-RDL and microbumps

- ***Passivation material***

For flip-chip bonding with bumping, the passivation layer has requirements in the aspects of chemical resistance, adhesion to metals, mechanical properties, thermal stability, Cu compatibility, thick film formable, smooth pattern profile, and low temperature cure (below 250 °C). Compared with other passivation materials, such as PI (polyimide), epoxy, BCB (benzocyclobutene) and fluorinated polymer, PBO (polybenzobisoxazole) is selected as the passivation material in this thesis.

HD8930 is a photo definable positive-tone aqueous PBO that can be patterned to resolve micrometer-scale patterns with controlled side-wall profiles without photoresist. This reduces the number of process steps required for coating layers, and hence improving yields and reducing overall cost. HD8930 is one of the newest materials for semiconductor stress buffer and packaging applications, which has the following major benefits: lower temperature cure (200 ºC), high chemical resistance to process and underfill chemistries, high elongation (80%), low modulus (1.8 GPa), Cu compatibility, good adhesion to eliminate cracking and delamination, good stability, smooth pattern profile, high sensitivity and high resolution.

- ***Fabrication process***

After the 3 μm oxide dielectric layer was deposited on a high resistivity Si wafer, Ti barrier layer and Cu seed layer were deposited by the PVD process. Photoresist was patterened for the Cu-RDL process, and Cu-RDL was formed by

the ECP process and the followed PR strip and barrier/seed layer seed etch. The HD8930 passivation layer was formed by lithographic pattern and curing process. Microbumps were faricated by the PVD of the Ti barrier layer and Cu seed layer, and the ECP of Cu/Ni/SnAg microbump. The SEM images of the transmission line using Cu-RDL process and the microbump are shown in Figure 5.11.

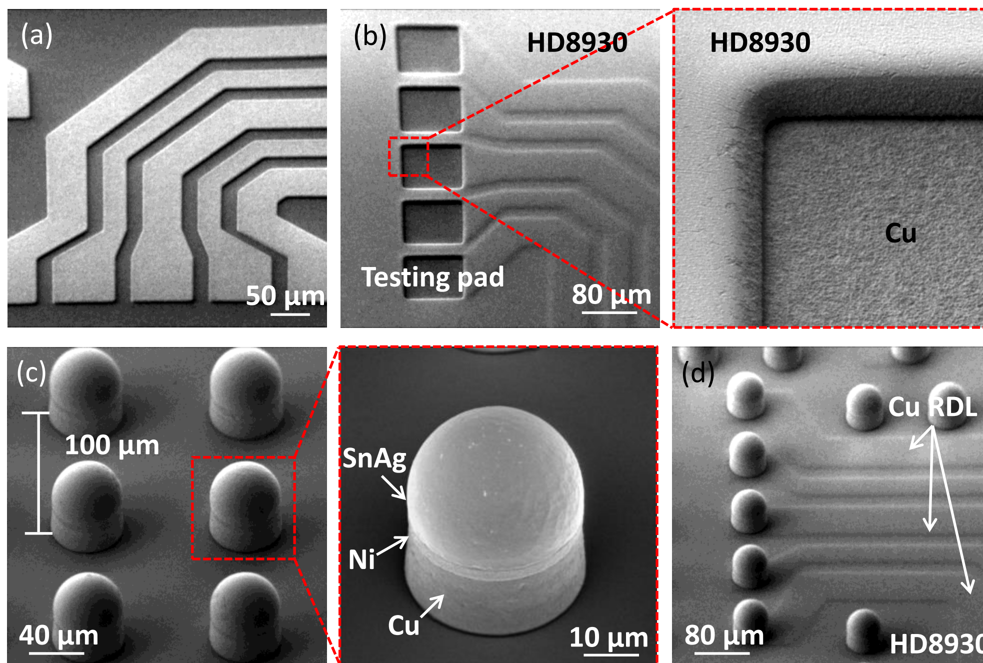


Figure 5.11 (a) SEM image of the microwave Cu-RDL. (b) Testing pads, inset: HD8930 passivation opening. (c) (d) microbump after bump reflow.

5.3.3 Flip-chip bonding of the silicon photonic TSV interposer and the electronic chip

As described in the preceding section 5.3.1, UBMs were fabricated on the top photonic TSV interposer with ~100 µm deep-trenches, while microbumps were fabricated on the bottom electronic chip. A flip-chip bonding technology for this photonic TSV interposer was developed based on the thermal compression bonding

(TCB) method [188] and vacuum reflow. The X-ray inspection and the cross-sectional microscope inspection between the developed flip-chip bonding technology for the photonic interposer, and the other traditional flip-chip bonding technologies are shown in Figure 5.12. Noted that cold joint is observed from the normal flip-chip bonding process, and squeezed UBM and microbumps are observed from the TCB process. Good bonding of the 3D module based on the photonic TSV interposer can be achieved by the developed TCB plus vacuum reflow process.

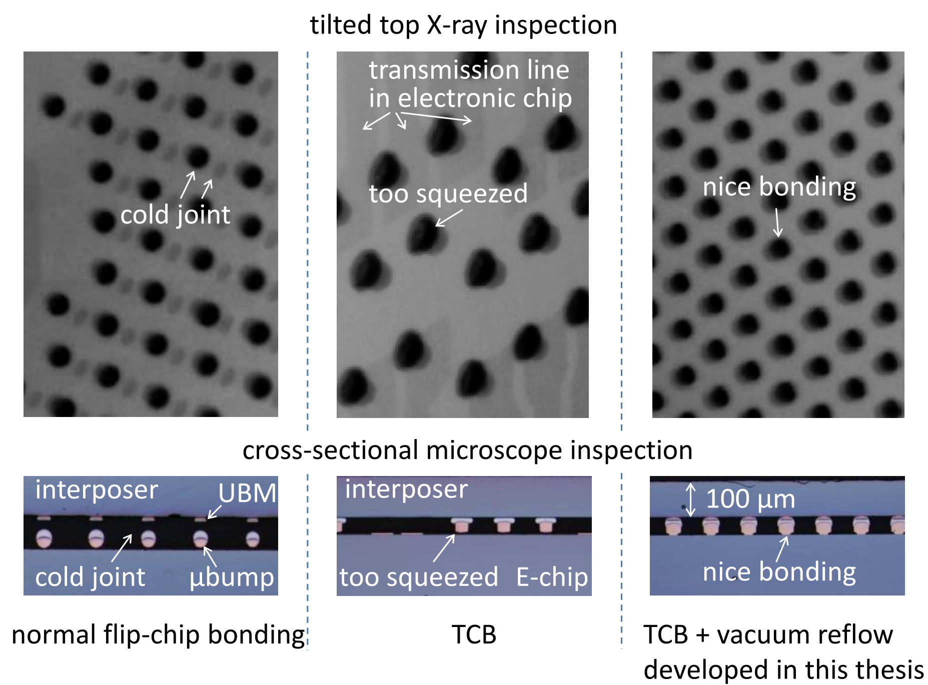


Figure 5.12 The X-ray inspection and the cross-sectional microscope inspection between the developed flip-chip bonding technology for the photonic interposer, and the other traditional flip-chip bonding technologies in the setup chips.

The 3D electro-photonic integration module based on SOI photonic TSV interposer was successfully fabricated and experimentally demonstrated for the first

time, as shown in Figure 5.13, which shows the cross-sectional microscope images and SEM images of the fabricated 3D electro-photonic integration module. A 100 μm-thick SOI photonic TSV interposer is bonded on top of the ~730 μm-thick silicon electronic chip. Inset i of Figure 5.13 shows the enlarged cross-sectional microscope image of GSG-TSVs with 20 μm-diameter and 100 μm-depth, bonded UBMs and microbumps with 40 μm-diameter, and Cu-RDL with 3 μm-thick on the bottom silicon electronic chip. The microwave electrical signal transmits through the Cu-RDL transmission line, and then vertically through the microbumps/UBMs and TSVs to drive the photonic devices. The enlarged cross-sectional image of TSV integrated with latticed Cu-BEOL on the SOI photonic interposer is shown in inset ii of Figure 5.13. The thickness of the Cu-BEOL is 2 μm. Beside the Cu-BEOL, the cross-sectional SEM image of silicon waveguide integrated in the SOI interposer is shown in inset iii of Figure 5.13. Inset iv of Figure 5.13 shows the enlarged cross-sectional microscope image of Cu-BEOL in the interposer and Cu-RDL in the Si electronic chip. Cross-sectional SEM image of the bonded UBMs/microbumps and Cu-RDL is shown in inset v of Figure 5.13, and a good bonding profile is observed. Cross-sectional SEM image of Cu-BEOL integrated with TSV is shown in inset vi of Figure 5.13, and oxide liner of TSV is observed. The computed tomography (CT) image of the 3D TSV integration is given in Figure 5.14, showing the TSV, latticed Cu-TWE of the photonic device, microbump interconnects and Cu-RDL on the bottom silicon electronic chip. A daisy chain of Cu-BEOL, TSV, UBM/microbump and microwave Cu-RDL was fabricated in the 3D integration module to test the electrical connection of the flip-chip bonding.

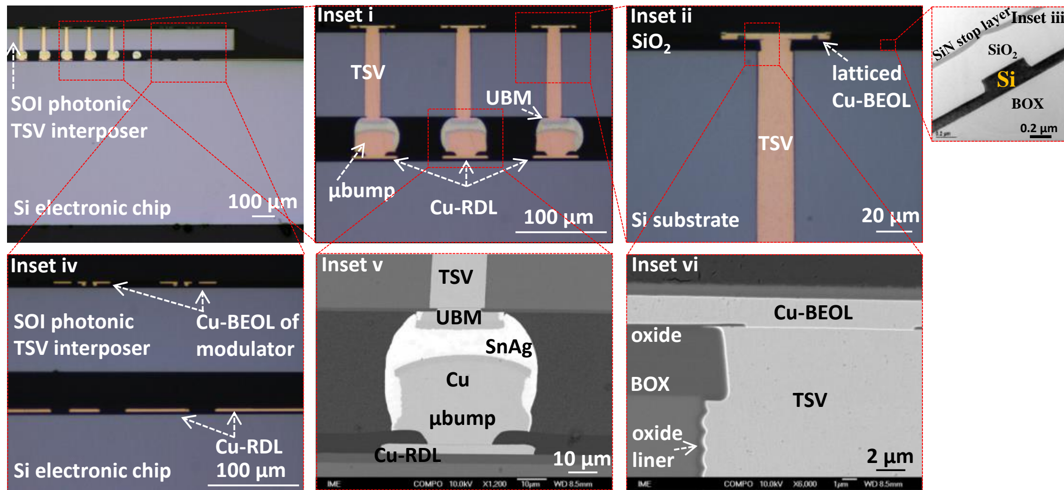


Figure 5.13 Cross-sectional microscope images and SEM images of the 3D electro-photonic integration module based on SOI photonic TSV interposer. Inset i: GSG-TSV and solder. Inset ii: TSV integrated with Cu-BEOL on the SOI photonic wafer. Inset iii: silicon waveguide in this SOI photonic TSV interposer. Inset iv: Cu-BEOL on the SOI photonic wafer and the Cu-RDL on the electronic chip. Inset v: integrated TSV, solder and Cu-RDL. Inset vi: TSV sidewall.

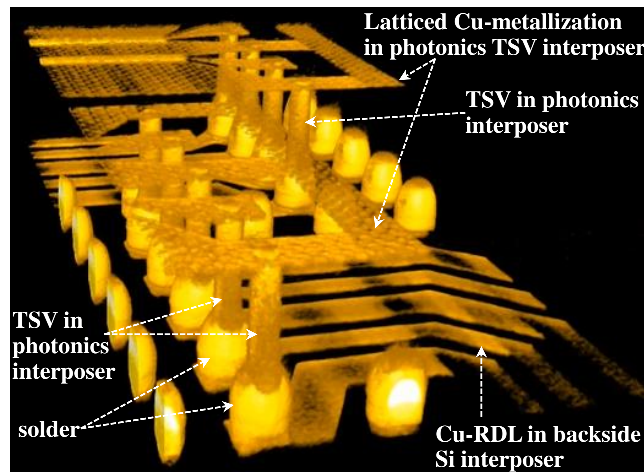


Figure 5.14 X-ray Computed Tomography (CT) image of the 3D electro-photonic integration module based on SOI photonic TSV interposer.

5.4 Characterization

As shown in Figure 5.1, the electrical signal was applied on the testing pads located on the electronic chip, while two lensed fibers with 2.5 μm focal-length were coupled to the nano-tip waveguide coupler in the photonic TSV interposer to characterize the optical performance of this 3D integration module. The electrical signal was transmitted through the microwave Cu-RDL fabricated in the electronic chip, and then vertically transmitted through the microbumps/UBMs and the TSVs to drive the photonic devices. The design and analysis of silicon photonic devices themselves is based on description in Chapter 4. However, the characterization in Chapter 4 was conducted on the normal 720 μm-thick standalone chip, while the photonic TSV interposer in this chapter is only 100 μm-thick in the 3D integration module.

5.4.1 DC characterization

- ***DC characterization of photonic devices in the 3D TSV integration system***
  - **Si optical MZI Modulator**

Figure 5.15(a) shows the output spectra of a silicon optical MZI modulator in the 3D TSV integration module with 3 mm-long phase shifter under different reversed bias voltages. The bias voltage was applied on one arm of the modulator. The FSR of the asymmetric MZI is 1.85 nm. Without any bias, the optical extinction ratio of this modualtor is ~ 22 dB. With the reversed bias, the carrier is pumped out of the waveguide and the optical loss reduces. Thus, the optical extinction ratio decreases due to the unbalance of optical power in two modulator's

arms with the increase of the reversed bias. The measured insertion loss of the modulator is ~ 9 dB, while the dynamic loss is shown in the inset of Figure 5.15(a), which is the average measurement result. The waveguide loss is 1.2 dB (undoped waveguide propagation loss ~ 0.2 dB/mm), 2 MMI loss is 0.6 dB, double fiber-to-waveguide coupling loss is 3.2 dB, and the optical loss caused by implantation is 1.3 dB/mm. These losses are the same as that in the normal interposer without TSV, since TSV KOZ has been accounted in the design phase.

In Figure 5.15(b), a π-phase shift can be realized under 6.8 V reversed bias voltage for a 3 mm-long phase shifter, which corresponds to a modulation efficiency ($V_\pi \cdot L_\pi$) of 20.4 V·mm with a standard deviation of 0.7 V·mm. With an increase in the applied reversed voltage from −2 V to −10 V, the efficiency is reduced from 12.6 V·mm to 23.1 V·mm, which is caused by the depletion of free carriers in the *p*-*n* junction. In the deep depletion region, the modulation efficiency becomes lower because there are fewer free carriers left in the depletion region. The DC performance of the modulator in the 3D TSV integration module is almost the same as the modulator in the SOI platform presented in the Chapter 4, which demonstrates the DC performance is not impacted by the TSV integration.

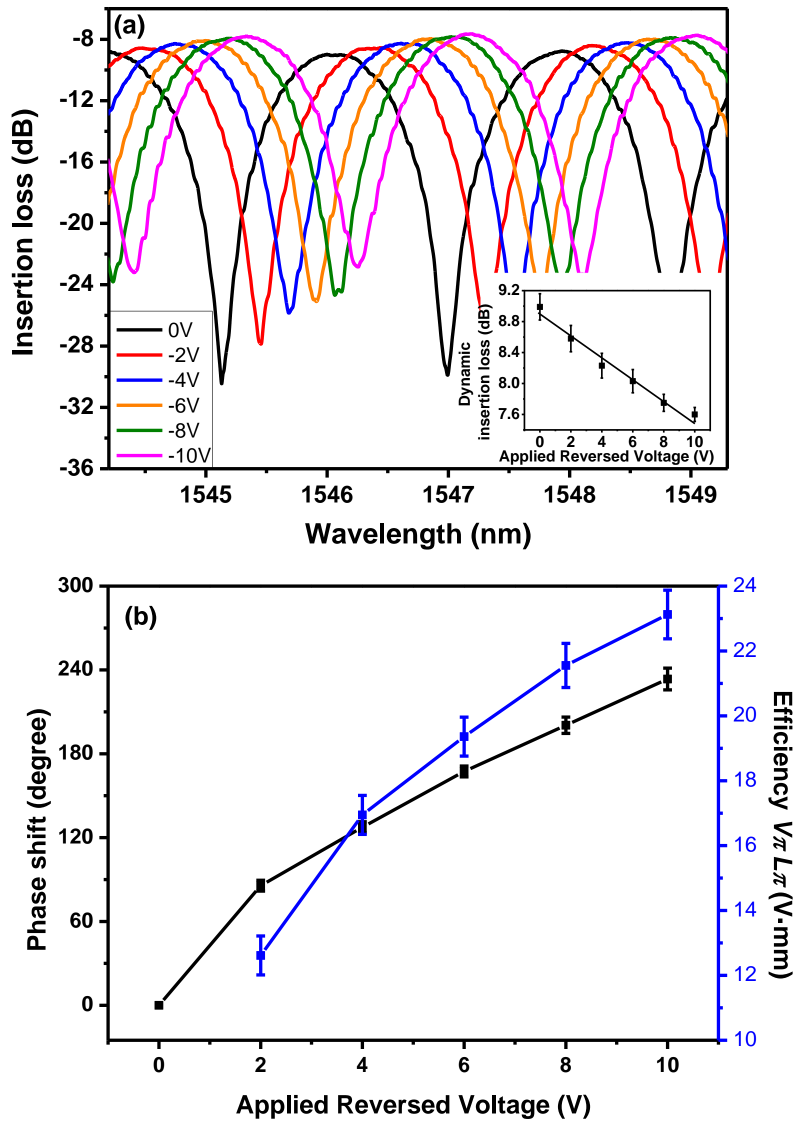


Figure 5.15 (a) Output spectra of silicon modulator in the 3D TSV integration module with 3 mm-long phase shifter, Inset: dynamic insertion loss. (b) Phase shift and efficiency $V_{\pi}L_{\pi}$ of the phase shifter under different applied reversed voltages of the 3 mm-long phase shifter.

- **Ge-on-Si vertical PD**

The waveguide loss (undoped waveguide propagation loss) and the fiber-to-waveguide coupling loss are the same as described in the above modulator DC measurement section. The measured dark current and photo current of the 3 μm-

wide and 5 μm-long Ge-on-Si vertical PD with discrete contact vias in the 3D TSV integration module under 1550 nm wavelength TE mode are shown in Figure 5.16(a). The responsivity of this PD is shown in Figure 5.16(b), which ranges from 0.78 A/W at 1510 nm to 0.18 A/W at 1590 nm. TSV KOZ has been accounted in the design phase. The DC performance of the PD in the 3D TSV integration module is close to the PD in the SOI platform presented in the Chapter 4, which demonstrates the DC performance is not impacted by the TSV integration.

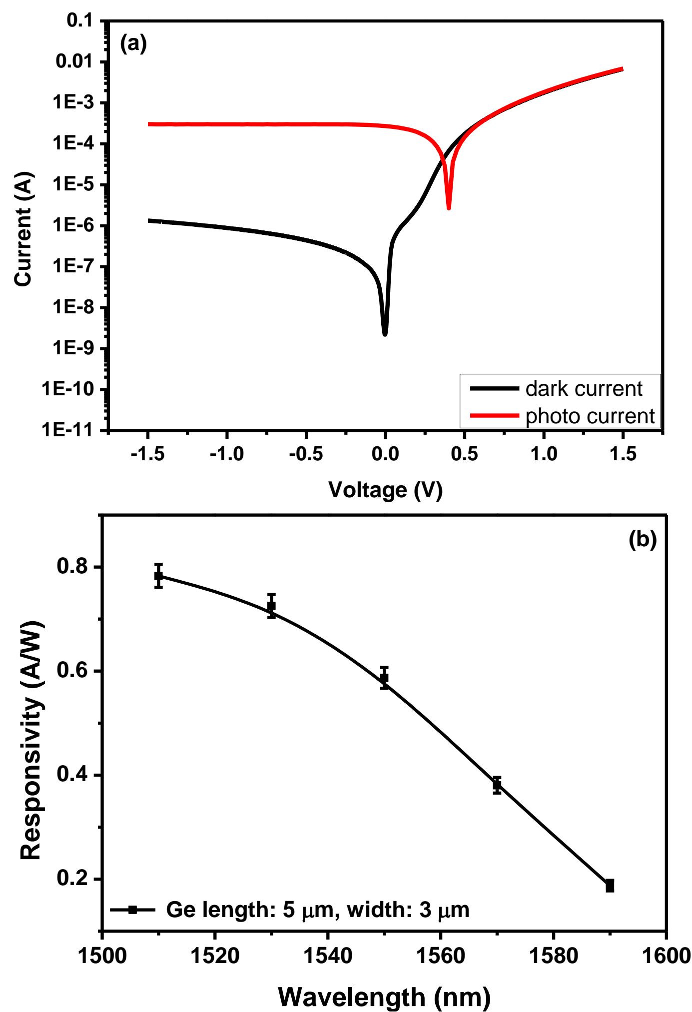


Figure 5.16 (a) The measured dark current and photo current, (b) the measured responsivity of the 3 μm-wide and 5 μm-long Ge-on-Si vertical PD in the 3D TSV integration module.

- **TO tunable silicon AWG**

The waveguide loss (undoped waveguide propagation loss) and the fiber-to-waveguide coupling loss are the same as described in the above modulator DC measurement section. The measured output spectra of 8 channels output before heating of the silicon AWG in the 3D TSV integration module are shown in Figure 5.17. The channel spacing is 3.2 nm and the minimum optical loss is 3.5 dB. The insertion loss consists of the waveguide loss of 1.4 dB (undoped waveguide propagation loss ~ 0.2 dB/mm) and the star couplers loss of 2.2 dB. The measured output spectra of four of the 8 channels of the silicon AWG under different bias voltages/powers are shown in Figure 5.18. The measured wavelength shifts under different bias powers are shown in Figure 5.19, and an 800 GHz channel tunability is achieved. The DC performance of the tunable AWG in the 3D TSV integration module is on the same order of the tunable AWG in the SOI platform presented in the Chapter 4, since thereotically the DC performance of photonic devices is not impacted by the TSV integration.

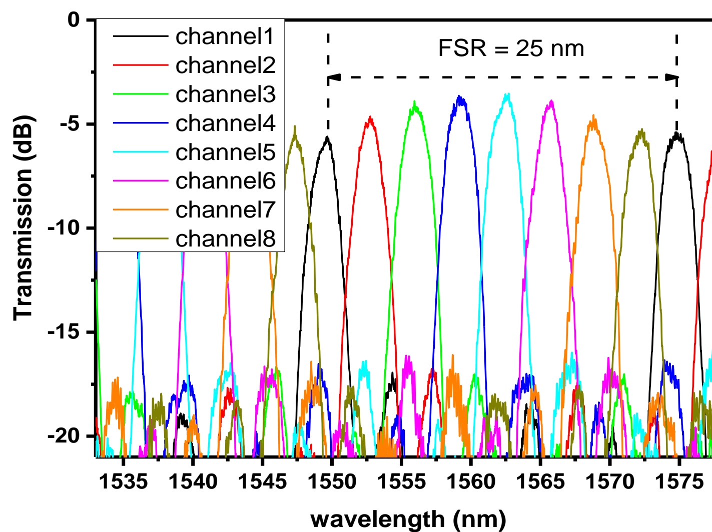


Figure 5.17 Transmission before heating of 8 channels output of the AWG in the 3D TSV integration module.

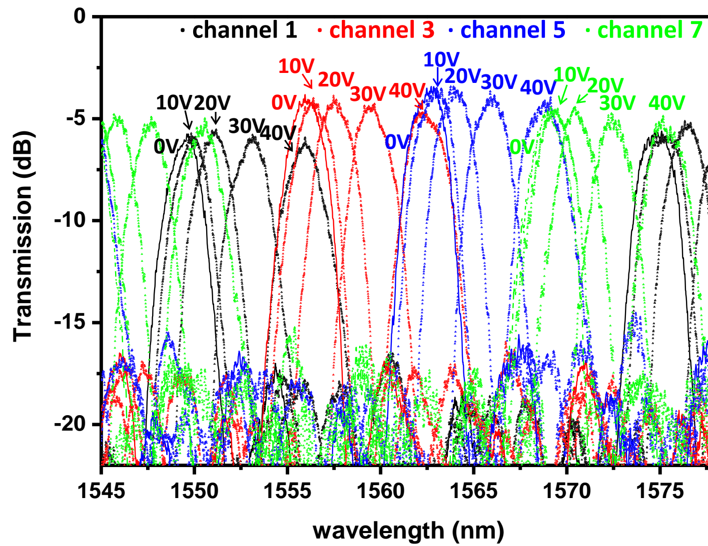


Figure 5.18 Transmission of output channel 1, 3, 5 and 7 of the AWG in the 3D TSV integration module under 0 V (0 W), 10 V (0.08 W), 20 V (0.32 W), 30 V (0.72 W), and 40 V (1.26 W).

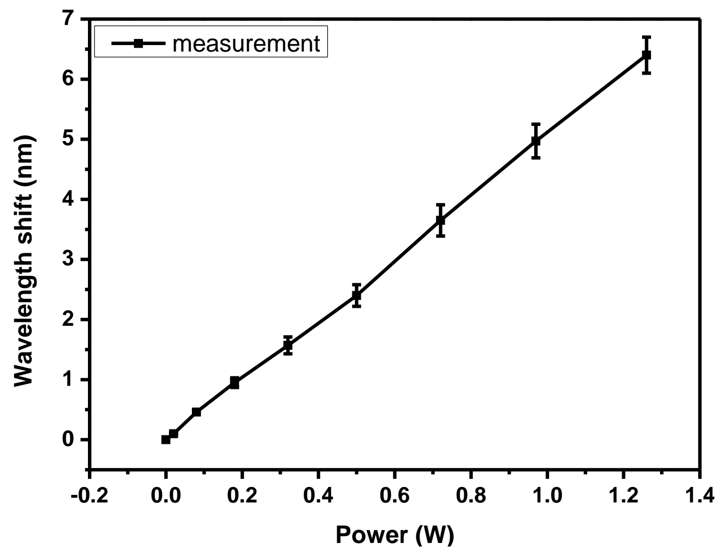


Figure 5.19 Measured wavelength shift of the AWG in the 3D TSV integration module under different bias powers.

5.4.2 AC characterization of the 3D integration system

Small signal microwave performance was measured through Agilent N4373C LCA which has a maximum bandwidth of 40 GHz. The input signal was adopted by a

probe with 67 GHz bandwidth which was pinned on one GSG-testing pad of the Cu-RDL on the electronic chip as shown in Figure 5.1. The 50 Ω matching impedance as a terminator was connected on the other testing pad on the electronic chip by another probe with 67 GHz bandwidth to reduce the signal reflection. The bandwidth and eye-diagram measurement setup is the same as shown in Chapter 4.

- ***AC characterization of Modulator and PD in the 3D TSV integration module***
  - **Si optical MZI Modulator**

For measuring the eye-diagram, a continuous-wave light from a 1550 nm tunable laser was firstly amplified through an EDFA and a BPF, and then modulated by adding a NRZ PRBS $2^{31}-1$ signal under $V_{bias} = -5.0$ V with $V_{pp} = 3.5$ V. The output optical signal was amplified again and collected by an Agilent DCA after the optical filter. The EO bandwidth is shown in Figure 5.20, and eye-diagram is shown in Figure 5.21. A 20.1 GHz-EO bandwidth and 40 Gbps-data rate have been achieved. Compared with the modulator in the SOI platform without TSV presented in the Chapter 4, the RF performance of the modulator in the 3D TSV integration module is degraded by 10 Gbps, which is due to the additional microwave loss in the long Cu-RDL transmission line in the electronic chip and in TSV. However, compared with the ultra-long interconnects in the conventional 2D E/O integration, TSV still provides the promising RF performance in the 3D integration module.

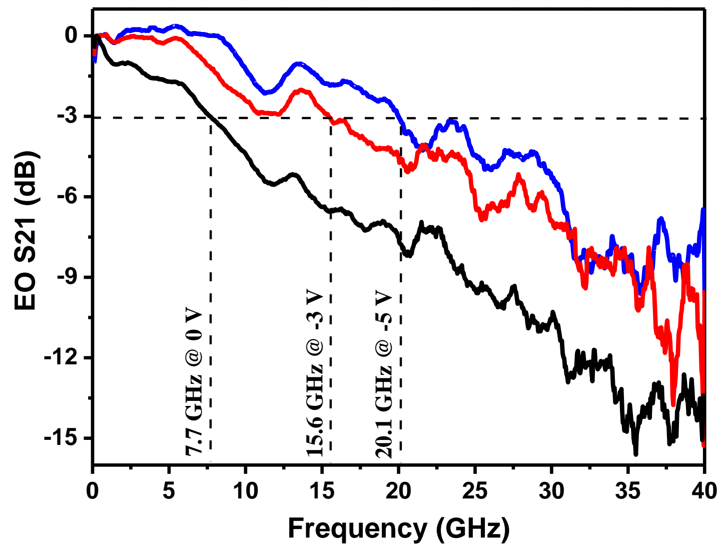


Figure 5.20 EO bandwidth of the modulator in the 3D TSV integration module under different bias voltages.

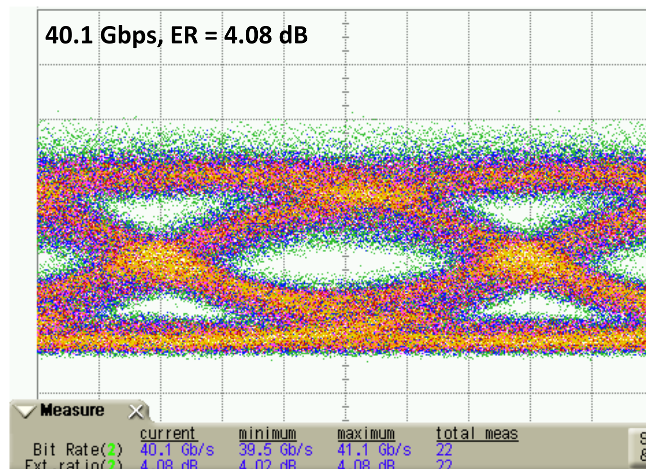
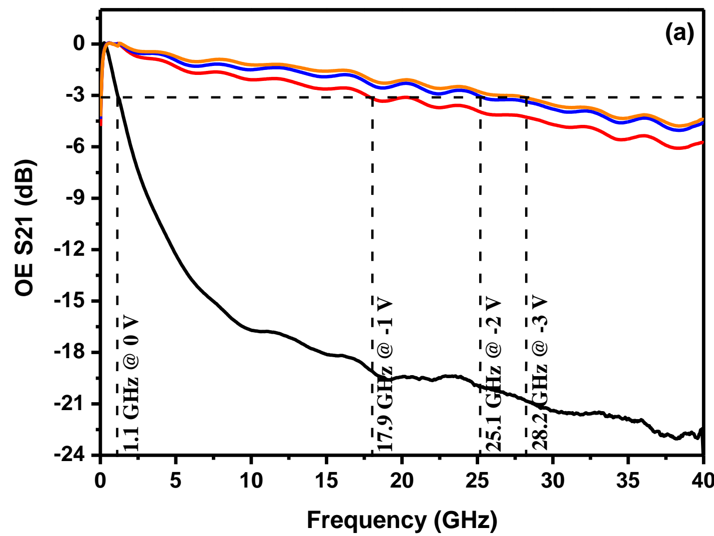


Figure 5.21 Eye-diagram of the modulator in the 3D TSV integration module.

- **Ge-on-Si vertical PD**

The measured OE bandwidth is 28.2 GHz under −3 V bias voltage, and is shown in Figure 5.22(a). In order to get the eye diagram results of PD, a high speed electrical signal coming from a 50/56-Gbps Anritsu Pattern Generator MP1822A

was firstly amplified through a 67 GHz high speed driver. It was applied to an external modulator through a bias tee with 60 GHz bandwidth and the input probe with 67 GHz bandwidth. A continuous-wave light from a 1550 nm tunable laser was modulated by adding a NRZ PRBS $2^{31}-1$ signal under $V_{bias} = -3.0$ V with $V_{pp} = 3.5$ V. The modulated optical signal was applied into the PD DUT after amplified by EDFA and BPF. The output electrical signal was collected by an Agilent DCA. The data rate of the eye-diagram reached 30 Gbps as shown in Figure 5.22(b). This data rate result is limited by the measurement condition in the laboratory. The total length of the RF cable applied is ~1.5 m and as a result the loss of a high-speed electrical signal is high. If the length of RF cable can be reduced in the future, it is possible for this integrated circuit to achieve a data rate of up to 40 Gbps. The RF performance of the PD in the 3D TSV integration module is close to the PD in the SOI platform without TSV presented in the Chapter 4. Thereotically, the bandwidth of PD is limited by the carriers' diffusion time and the loading time of the depletion capacity [116], therefore the RF performance of PD is nearly not impacted by the TSV integration.



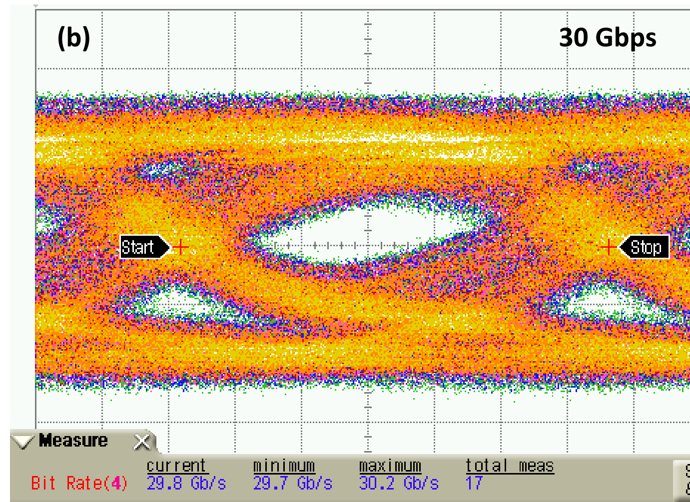


Figure 5.22 (a) The measured OE bandwith of the 3 μm-wide and 5 μm-long Ge-on-Si vertical PD in the 3D TSV integration module. (b) The eye-diagram of the PD.

5.5 Conclusions

Design, modeling, fabrication and characterization of the 3D EPIC TSV integration module based on the silicon photonic TSV interposer are explored in this chapter. A silicon photonic TSV interposer with monolithically integrated optical modulator, PD and TO tunable AWG has been explored and experimentally demonstrated, and

an electronic chip with microwave transmission line based on Cu-RDL process is presented. The flip-chip bonding of the silicon photonic TSV interposer and the electronic chip is developed. This 3D electro-photonic TSV integration is experimentally demonstrated and characterized for the first time. The characterization results show that 40 Gbps-data rate is achieved for the high speed photonic device, and 800 GHz channel tunability is achieved for the TO tunable silicon AWG in the 3D electro-photonic TSV integration.

Chapter 6 Conclusions and Future Works

6.1 Conclusions

3D electro-photonic TSV integration provides the flexible integration of the heterogeneous functionalities and technologies. Small form factor, decreased interconnect delay, high desity of circuit and interconnects and therefore enhanced inter-chip bandwidth can be achieved through the 3D TSV integration scheme. Compared with the traditional 2D electro-photonic integration, the main difficulties and challenges are the development of the integration process, avoiding the TSV-induced impact on the photonic device under compact scaling, and the co-design of different functionalities in the lack of 3D electronic design automation (EDA) tool. In this thesis, the technology options/integration strategies of electro-photonic integration based on silicon photonic interposer featuring TSVs and flip-chip bonding technology are proposed and investigated. A 3D electro-photonic TSV integration module is experimentally demonstrated for the first time. An SOI photonic TSV interposer for the purpose of inter/intra-chip optical/electrical communication interface routing is designed, in which TSVs are fabricated in an SOI photonics wafer with monolithically integrated optical modulator, Ge-on-Si PD and TO tunable Si AWG. Cu transmission lines are designed and fabricated on the electronic chip using Cu-RDL process for transmitting the microwave signal.

The first challenge solved in this thesis is investigation on the TSV-induced impact on the photonic device optical performance under compact scaling for the first time. TSV-induced stress affects the performance of silicon photonic devices

integrated in interposer, particularly for the stress-sensitive devices, such as silicon photonic ring resonators. The model of TSV-induced stress distribution in the silicon waveguide in SOI photonic interposer, and the model of TSV-induced effective-refractive-index change are built. Silicon photonic double-cascaded ring resonators integrated with TSV structures on an SOI platform are fabricated and characterized to experimentally analyze the impact of TSV-induced stress. The characterization results are statistically analyzed with the impact of fabrication non-uniformity eliminated. Finally, a stress aware design framework and a TSV KOZ of $d/R > 3$ for Si photonic ring resonator in SOI interposer are proposed, in order to keep the TSV-induced resonant wavelength shift one order of magnitude smaller than 0.1 nm under compact scaling.

The second achievement in this thesis is the design and process development of a silicon photonic interposer with monolithically integrated active/passive photonic devices featuring Cu-BEOL, including optical modulator, Ge-on-Si PD and TO tunable AWG. Integrated MZI modulator and Ge PD featuring RF TWE via Cu-BEOL are explored with better RF performance. A latticed Cu surface pattern is designed for the Cu-BEOL based on the Cu CMP process requirement. Cu-BEOL process is successfully developed for the photonic devices. The modulator is designed with doping compensation for reducing the optical transmission loss of the phase shifter caused by ion implantation. Discrete contact plugs to Ge PD are designed for reducing Cu-induced optical loss and thus improving the responsivity. The 3-dB bandwidths for both stand-alone modulators and PDs on the integrated wafer are 37 GHz and 33.7 GHz, respectively. 50.5 Gbps-data rate of modulator and a transmission data rate of 30 Gbps of the interposer is achieved, which is limited

by the measurement setup conditions. It is demonstrated that Cu-TWE with higher conductivity and lower skin-effect provides better RF performance with higher bandwidth in silicon PIC and active devices than conventional Al-BEOL. Cu application can further improve the integration of silicon photonics devices and CMOS circuits in the future. The Cu-BEOL based RF silicon photonic devices toolbox for high performance photonics-CMOS integration strategy has been established. A TO tuning method of silicon AWG integrated in this interposer is designed and experimentally demonstrated for the first time. The thermal performance simulation shows that a uniform heating is achieved by the heater design, while the experiment results show that above 600 GHz channel tunability is achieved. The precise positioning or compensation of the dimensional sensitive wavelength in the SOI DWDM technology is solved by this tuning method.

The final achievement in this thesis is the first experimentally demonstration of a 3D electro-photonic TSV integration module, which including a RF photonic TSV interposer and an electronic microwave chip. The RF photonic TSV interposer is designed by integrating TSV structure into the above discussed Cu-photonic interposer, while Cu transmission lines are designed and fabricated on the electronic chip using Cu-RDL process for transmitting the microwave signal. Based on the modeling result of this 3D integration module, higher I/O density and higher microwave performance can be achieved by TSV structure with smaller diameter, higher aspect ratio and higher density. The fabrication process of the 3D integration module is successfully developed, including the integration process of TSVs and photonic devices with Cu-BEOL, bonding technology of the 100 μm-thick interposer and elecronic chip, and so on. The characterization results show that 40

Gbps-data rate is achieved for the high speed integrated photonic device, and 800 GHz channel tunability is achieved for the TO tunable silicon AWG in the 3D electro-photonic TSV integration. From modeling and first experimental demonstration, this 3D electro-photonic TSV integration module provides the needed toolboxes for the 3D Si photonics-CMOS TSV integration strategy based on Si photonics interposer featuring TSVs and flip-chip bonding technology.

6.2 Future Works

Beyond the works presented in this thesis, the following proposed optimizations are worthy for the future works:

(a) The fabrication of TSVs with smaller diameters (less than 10 μm), higher aspect ratios (10:1) and smaller TSV center-to-center pitch (less than 3 × TSV diameter) needs to be explored for higher I/O density and higher microwave performance. As shown in the modeling results presented in section 5.2.1 in Chapter 5, smaller insertion loss and return loss can be achieved with the smaller TSV diameter and the smaller pitch. The main challenge is the improvement on the higher aspect ratio, which is limited by the condition of TSV barrier/seed layer deposition at present. In the future optimization, the barrier/seed layer materials composition, deposition method, energy and temperature, etc. needs to be optimized for higher TSV aspect ratio. Higher TSV density (smaller pitch) needs to be explored together with the stress/warpage control of the TSV wafer.

(b) The power consumption of the TO tunable AWG needs to be optimized for

practical applications, especially in the low power photonic-CMOS integration applications. In this thesis, above 600 GHz channel tunability is achieved with 1.26 W power consumption. To reduce the power consumption, the following optimization method can be pursued, by removing the adjacent SiO_2 and 120 μm of the underlying Si substrate using SiF_6 etching, while leaving a few SiO_2 beams to support the suspended device for the purpose of structural strength. Compared with the device without air isolation layer, the power consumption can be significantly reduced by 98% [187]. It is realized by preventing heat from leaking out of the waveguides due to the presence of the air isolation layer. Besides the optimization of power consumption, optimization of insertion loss can be investigated based on suppressing multimode generation and scattering near the boundary of a star coupler [189]. Transition loss, which is the major contribution to the AWG insertion loss, depends on the etch depth and the gaps between the arrayed waveguides at the star coupler boundary. The abrupt structural change at the boundary between the slab region and arrayed waveguides causes the optical field mismatching, which results in additional transition loss. More than 50% improvement of insertion loss can be achieved through optimization of the field matching in the star coupler boundary using the ultrashallow etch process [189].

(c) The PD testing setup in our laboratory needs to be improved to reduce the impact of the testing cable on the measured data rate of the PD. The total length of the RF cable applied is ~1.5 m and as a result the loss of a high-speed electrical signal is high. If the length of RF cable can be reduced in the future, it is possible for this integrated circuit to achieve a data rate of up to 45 Gbps.

(d) As shown in Figure 4.1 in Chapter 4, driver, transimpedance amplifier (TIA) and limiting amplifier (LA) will be integrated to achieve a complete 3D EPIC TSV integration system (3D silicon nanophotonics-CMOS TSV integrated transceiver). In this thesis, the microwave electrical signal transmitted from the Cu-RDL transmission line fabricated in the electronic chip is designed for demonstration purpose of the electrical signal in the complete 3D EPIC TSV integration system. In the future works, CMOS driver will be integrated in the transmitter part for driving the modulator, while CMOS TIA and LA will be integrated in the receiver part for converting the AC signal generated from the PD to the digital voltage signal. The microwave design of this complete 3D EPIC TSV integration system needs to be optimized based on the modeling presented in section 5.2 in Chapter 5 to achieve higher microwave performance.

Author's Publications

Journal Papers

1. **Yan Yang**, Xiaonan Hu, Junfeng Song, Qing Fang, Mingbin Yu, Xiaoguang Tu, Guo-Qiang Lo, and Rusli, "Thermo-optically tunable silicon AWG with above 600 GHz channel tunability," ***IEEE Photonics Technology Letters***, vol. 27, no. 22, pp. 2351-2354, 2015.

2. **Yan Yang**, Qing Fang, Mingbin Yu, Xiaoguang Tu, Rusli, and Guo-Qiang Lo, "High efficiency Si optical modulator using Cu travelling-wave electrode", ***Optics Express***, vol. 22, no. 24, pp. 29978-29985, 2014.

3. **Yan Yang**, Mingbin Yu, Rusli, Qing Fang, Junfeng Song, Liang Ding, and Guo-Qiang Lo, "Through-Si-via (TSV) keep-out-zone (KOZ) in SOI photonics interposer: a study of the impact of TSV-induced stress on Si ring resonators," ***IEEE Photonics Journal***, vol. 5, no. 6, 2700611, 2013.

4. Qing Fang, Xiaoguang Tu, Junfeng Song, Lianxi Jia, Xianshu Luo, **Yan Yang**, Mingbin Yu, and Guoqiang Lo, "PN-type carrier-induced filter with modulatable extinction ratio," ***Optics Express***, vol.22, no.24, pp.29978-29985, Nov. 2014.

Conference Papers

1. **Yan Yang**, Qing Fang, Mingbin Yu, Xiaoguang Tu, Junfeng Song, Rusli and Guoqiang Lo, "High-Performance Si Photonics Interposer Featuring RF Travelling-wave Electrode (TWE) via Cu-BEOL", in *2015 Optical Fiber*

*Communication Conference (**OFC**)*, pp. Tu2A.6, Los Angeles, California, USA, 22-26 March 2015.

2. **Yan Yang**, Mingbin Yu, Qing Fang, Junfeng Song, Xiaoguang Tu, Patrick Guo-Qiang Lo, and Rusli, “3D silicon photonics packaging based on TSV interposer for high density on-board optics module”, accepted in *2016 IEEE 66th Electronic Components and Technology Conference (**ECTC**)*, Las Vegas, Nevada, USA, 31 May-3 June, 2016.

3. Mingbin Yu,† **Yan Yang,*** Qing Fang, Xiaoguang Tu, Junfeng Song, King-Jien Chui, Rusli, and Guo-Qiang Lo, “3D electro-optical integration based on high-performance Si photonics TSV interposer,” accepted in *2016 Optical Fiber Communication Conference (**OFC**)*, Anaheim, California, USA, 20-24 March 2016. († * co-first author and co-corresponding author)

4. **Yan Yang**, Qing Fang, Mingbin Yu, Xiaoguang Tu, Junfeng Song, Rusli and Guoqiang Lo, “Modeling and fabrication of traveling-wave electrode (TWE) of Si optical modulator via Cu-BEOL”, in *2015 IEEE International Conference on Electron Devices and Solid-State Circuits (**EDSSC**)*, pp. 816-819, Singapore, 1-4 June 2015.

5. **Yan Yang**, Mingbin Yu, Qing Fang, Xiaoguang Tu, Junfeng Song, Rusli Rusli, and Guo-Qiang Lo, "Electro-Optical Integration Based on Cu-Photonics TSV Interposer," in *2015 8th International Conference on Materials for Advanced Technologies of the Materials Research Society of Singapore & 16th IUMRS-International Conference in Asia Together with 4th Photonics Global*

Conference 2015 (ICMAT2015 & IUMRS-ICA2015), Singapore, 28 Jun. to 03 Jul. 2015.

6. **Yan Yang**, Mingbin Yu, Rusli Rusli, Qing Fang, Junfeng Song, and Guo-Qiang Lo, "The impact of through-silicon via on the optical performances of silicon photonic ring resonators in SOI photonic interposer," in *2013 International Conference on Materials for Advanced Technologies (ICMAT)*, Singapore, 30 Jun. to 05 Jul. 2013.

7. Qing Fang, **Yan Yang**, Lianxi Jia, Xiaoguang Tu, Junfeng Song, Mingbin Yu, and Guo-Qiang Lo, "Arrayed waveguide grating filter integrated with cantilevered coupler on SOI platform," in *2014 6th MRS-S Conference on Advanced Materials*, Singapore, 22 – 25, Jul. 2014.

8. Weihong Li, **Yan Yang**, Mingbin Yu, Ramana Murthy, and Eugene Tan, "In-line monitoring of sidewall roughness using 3D-AFM for silicon photonic devices," in *2013 International Conference on Materials for Advanced Technologies (ICMAT)*, Singapore, 30 Jun. to 05 Jul. 2013.

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