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DC FAULT DETECTION AND CLEARANCE IN VSC-HVDC SYSTEMS

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Abstract

Today's electric grid is mostly based on alternating current (AC), as well as the loads. The advancement of voltage source converter (VSC) has paved way for the emergence of VSC-HVDC transmission systems opening up the possibility to build multi-terminal DC (MTDC) grid in future. Before we reach that mark, there are a lot of open points to be answered. One of the critical topics for such DC grid is the protection.

DC fault can be identified by the time- and frequency-domain analysis of the DC current. Thus, this thesis proposes and investigates three fault detection methods which operate in the two domains. The first frequency-domain method involves wavelet transform. Because DC fault can happen anytime and is unpredictable, the signal processing technique can work on the non-stationary fault signal and identify the presence of high frequency content caused by fault. The second method is based on time-domain, whereby the behaviour of DC-link capacitor in VSC is closely monitored. In the event of fault, the DC-link capacitor will discharge contributing to high fault current. Short-time Fourier transform (STFT) is another frequency-domain method to be considered. It will be studied how the distortion in frequency spectrum can be used to establish the indication of DC fault occurrence.

Since wavelet transform has been well-established in literature, it will be used as the benchmark to assess the performance of capacitive discharge and STFT methods. They are extensively analyzed and compared using a scaled down VSC-based DC system experimental test setup, as well as simulation model built in PSCAD/EMTDC. Results show that capacitive discharge performs better in terms of detection time and robustness, whereas STFT method consumes less computational resource, yet it can detect the fault as effective as wavelet transform. It will be shown how the noise in real fault signal affects their performances to varying degrees. Besides that, the proposed methods succeed in determining the faulted line in MTDC systems by just relying on local information.

It is also equally important to address the issue of fault clearance in DC systems. This thesis will discuss and analyse three protection schemes. Each scheme will be assessed based on how fast they clear the fault and achieve smooth recovery. For this study, it is entirely done in PSCAD/EMTDC.

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Nomenclatures

C_{dci}	DC-link capacitor at terminal i	μF
C_{sm}	MMC submodule capacitor	μF
D_f	Fault distance	km
f	System frequency	Hz
f_s	Sampling frequency	Hz
H	STFT hop size	
I_{arm}	Arm current in MMC	kA
I_{cap}	Capacitor current	kA
I_D	Diode current	kA
I_{dcij}	DC current between terminal i and j	kA
I_f	Fault current	kA
$I_{si,\alpha\beta}$	Source current in α and β axis	kA
$I_{si,dq}$	Source current in d and q axis	kA
K_{pc}, T_{ic}	PI parameter for current controller	
L_{arm}	Arm inductor in MMC	mH
L_{FCL}	Fault limiting inductor	mH
L_{si}	Source impedance	mH
m_a	Modulation index	

N	Number of submodule in MMC	
P_{ac}	AC power	MW
P_{dc}	DC power	MW
R	Correlation coefficient	
ROC	Rate of change of current	kA/s
S_n	Rated power of DC-link capacitor	MVA
T_{eq}	Equivalent time delay by current controller	s
T_a	Converter switching time	s
V_{dci}	DC voltage at termial i	kV
$V_{si,\alpha\beta}$	Source voltage in α and β axis	kV
$V_{si,dq}$	Source voltage in d and q axis	kV
$w(n)$	Window function	
φ	Phase displacement	degree
ψ(t)	Mother wavelet	
τ	Time constant	
θ_{PLL}	PLL angle	degree
θ_m	Phase margin	degree
ω	Angular frequency	rad/s

Chapter 1

Introduction

Electric power in 21^{st} century is no longer what it used to be. Apart from meeting growing demand, a strong push to produce electricity in an economically sound way, at the same time environmentally friendly without adding carbon footprint, has taken conventional power system in new direction [7]. High voltage direct current, system, or commonly known as HVDC, is one of the key technologies in this trajectory. Implementation of HVDC system is made possible by the advancement of power electronics. The converter technologies employed in present HVDC system can be broken into two types: current source converter (CSC) and voltage source converter (VSC). The inception of CSC dates back to the 1970s [8]. Then, the VSC came along in the 1990s [9]. The fact that recent years have seen increasing research interest in VSC is an evident indication of its rapid acceptance in modern HVDC system. One of the main reasons is that it allows independent control of active and reactive power, enabling integration of renewable energy into the grid. That being said, VSC is especially vulnerable to DC fault due to low inductance on its DC side. For this reason, it is of paramount importance to address the fault detection in VSC-HVDC system.

Overcurrent and undervoltage are among the indicators in the event of fault. This information is needed to quickly diagnose the underlying cause and decide the follow-up action. The ability to warrant the right tripping boils down to selectivity. If the disturbance is confirmed to be DC fault, the fault detection will dispatch tripping signal to DC circuit breaker isolating the faulted line; if it is not, the DC protection should not be activated. In real scenario, it is impossible to predict what the DC fault will be like. The severeness of DC fault can be influenced by myriad of factors, such as fault resistance and location. For this reason, a robust fault detection is desirable, ensuring that all forms of DC faults can be identified. As already mentioned, VSC-HVDC system tends to have low line inductance, which means that the lack of magnetic field diminish the impedance to the flow of fault current. As a result, the fault current can increase extremely fast. This problem demands a high-speed fault detection so that the DC protection can act fast just before the fault current reaches detrimental level. To sum up, a good fault detection in HVDC system needs to be designed with three characteristics in mind: selectivity, robustness and speed.

Fault clearance poses a huge challenge in DC domain. Before the introduction of VSC, most of the traditional HVDC systems were restricted to point-to-point connection. The only way to isolate the DC fault in this topology was disconnecting the entire DC system, which could be sufficiently served by the AC circuit breaker (CB) alone. However, for multi-terminal system, a short moment of operation shutdown is undesirable. This is where the DC CB comes into picture. It is able to extinguish the fault arc while keeping the rest of the system undisturbed. The studies on this technology thus far are only demonstrated on low voltage scale, it remains to be seen how it will actually perform in the field. Nevertheless, the understanding of system recovery when employing AC CB or DC CB in multi-terminal HVDC system is equally important. It is necessary to ensure that the recovery is smooth and fast keeping the transient to minimum.

The main focus of this thesis is to address what has been discussed above. In this work, we study and propose various novel techniques of detecting DC fault in VSC-HVDC system. A selective, robust and fast fault detection is imperative for a secure and reliable HVDC system. To that end, the methods presented in this thesis will be thoroughly evaluated to meet this expectation. In addition to fault detection, the fault clearance methods involving AC CB and DC CB are also analyzed. With all these, this thesis is completing the picture of protection in VSC-HVDC system.

This chapter introduces the DC fault detection and clearance in VSC-HVDC system. For this purpose, we present the challenges of detecting the DC fault and how we are going to approach this problem. We briefly talk about the proposed methods and present the organization of this thesis.

1.1 Objective of the Thesis

The main goals of this thesis are as follows.

1. To analyze the transient caused by DC fault in VSC-HVDC system. Abrupt change in voltage and current is an indicator and a precursor to the departure from normal operation as a result of fault. Definitive understanding of the signs can help us propose a protection logic which is able to detect the DC fault in VSC-HVDC system.

2. To build the VSC-based DC system in simulation and experiment. The simulations give us the flexibility to change parameter values and visualize different fault

scenarios. Then, we will have better idea of how much fault current to be expected when we design the experimental setup, considering the equipment ratings and necessary protective measures.

3. To develop the logics suitable for DC fault detection. We approach the fault detection by using signal processing and pattern recognition techniques, which capture the signs indicative of fault and convert this information into decision. This allows the detection to be more accurately targeted at the events in which the DC CB should trip

4. To verify the proposed fault detection methods in simulation and experiment. Their performances are assessed based on selectivity, robustness and speed.

5. To compare the protection schemes with various protective devices such as AC CB and DC CB. The difference in their operation time can influence how multi-terminal HVDC system behave during recovery. We will discuss how to strategize the recovery sequence in order to contain the transient within constraint.

1.2 Major Contributions

The major contributions are as follows:

- the development of lab-scale, two-terminal DC system experimental hardware.[10]

- the testing of fault detection method on real fault signal.[10, 11]

- the evaluation wavelet-based fault detection method using simulation and experimental model. The selections of mother wavelet, scale and decomposition level are outlined. It is demonstrated that it is able to effectively detect faulted line in multi-terminals HVDC system only relying on local information. The simulation and experimental results show the detection is resilient to influence of fault resistance and distance.[12, 13]

- the introduction of novel fault detection method based on pattern recognition, by comparing capacitive discharge and DC current. During pole-to-pole DC fault, the capacitor will discharge immediately and generate large current to the fault point through the DC lines. This phenomenon can be translated into useful information to determine the occurrence of DC fault. The presence of capacitive discharge in DC current by using correlation coefficient is traced using correlation coefficient. It is simple, fast and robust, making it a potential alternative to the existing fault detection methods in literature. Validated with simulation and experimental models, this method has robust tolerance to variation of DC fault parameters, such as resistance and location. The detection is achievable within 1 ms. The simulation results also support that it is successful in differentiating DC fault from other disturbances, such as AC fault and sudden blocking of converter.[14]

- the proposal of using short-time Fourier transform (STFT) to detect DC fault. The principal novelty is in the consideration of time-frequency resolution, whereby finer time resolution is prioritized over frequency resolution for speedy detection. As opposed to wavelet transform, the specific frequency content can be pinpointed. Additionally, the use of fast Fourier transform (FFT) algorithm reduces the computational burden. In both simulation and experiment, it is observed that the DC fault presents a consistent pattern in the frequency spectrum, which can be utilized to form fault criterion. This method is able to discriminate against load change and AC fault.[15–17]

- the comparative analysis of different protection schemes using AC CB, double-thyristor and hybrid DC CB. Each scheme is assessed in term of the time it takes to restore to normal operation. With the proposed recovery sequence, voltage spikes and current surges are under control.

The secondary contributions are as follows:

1. the development of multi-terminal HVDC system in PSCAD/EMTDC.
2. the outline of necessary steps in ensuring that the DC fault in hardware experiment is performed in safe manner.
3. the development of a framework in assessing fault detection methods in term of selectivity, robustness and speed.
4. the understanding of existing fault detection methods proposed in literature.

1.3 Organization of the Thesis

This thesis is organized in nine chapters:

- **Chapter 1:** The broad view of protection issues in VSC-HVDC system and specify the goals of this thesis is presented.
- **Chapter 2:** The state-of-the-art of HVDC protection is presented. The fault detection methods proposed in literature can be categorized into six types. Each type comes with pros and cons. Research on the protection strategy and fault behavior in HVDC system is provided.

- **Chapter 3:** The mathematical modeling and converter control of VSC-HVDC is presented. The equations explaining the fault behavior are derived and the calculation is verified with simulation.

- **Chapter 4:** The steps and components necessary for building the multi-terminal HVDC system in PSCAD/EMTDC are outlined. Two multi-terminal HVDC systems with different configurations and rating are simulated to generate diverse fault scenarios. Details regarding the design of two-level VSC experimental hardware and protection measures are presented. Using both simulation and experimental model, the results of DC fault, AC fault and load change are analyzed.

- **Chapter 5:** A comprehensive analysis of wavelet-based method detecting and locating fault in HVDC system is presented. We discuss how the mother wavelet is chosen in order to provide speedy detection. The effectiveness of this method is evaluated in simulation and experiment. Readers will have an idea of how this method performs under the influence of various fault parameters and external faults, load change and signal noise.

- **Chapter 6:** A new fault detection method based on capacitive discharge is developed. The structure of software implementation of this method is given. This method is tested against the influence of various fault parameters and AC fault, with the analysis done in simulation and experiment.

- **Chapter 7:** A new fault detection method based on STFT is introduced. It is discussed how the parameters of STFT are chosen in order to suit the application of DC fault detection. The simulation and experimental results of this method working under the influence of various fault parameters, AC fault and load change are presented with comments.

- **Chapter 8:** A comparative analysis of three protection schemes using AC CB, double-thyristor and hybrid DC CB in a multi-terminal HVDC system is presented. The working principle of each scheme is explained in detail. Sequence, such as the time of deblocking of converter and reclosing of CB, during the recovery process is discussed. From the simulation result, each scheme is assessed in term of the time they take to achieve full recovery in the event of DC fault.

- **Chapter 9:** The general discussion on the performance of proposals and conclusion of this thesis and discuss possible direction for future research are presented.

Chapter 2

Literature Review

2.1 Fault Detection Method

Despite the absence of protection standard for VSC-HVDC systems, it is generally agreed in literature that the ideal DC fault detection time is below 2 ms [18–20]. The vastly shorter detection time compared to AC system (approximately three cycles) [21] is justifiable as the lack of system inductance causes the fault current to rise at rapid rate. To respect such a stringent requirement, this chapter presents the state-of-the-art of fault detection methods that have been proposed.

2.1.1 Direct Measurement

Direct measurement [22–26] is a simple and straightforward method to determine the occurrence of DC fault. The DC current is constantly monitored on each DC line and compared with threshold. This method is fast and cheap, as it only relies on local data and does not involve intensive computation. Since there is no general consensus with the value of threshold in literatures, each author has their way of determining the threshold that satisfies their own set of protection requirements. The selection of threshold can be challenging. If the threshold is set too high, the detection of high impedance fault might be undermined; if too low, wrong detection is likely to happen.

Torres-Olguin [27] proposed a similar method which detects the fault when the current measured exceeds a threshold. He devised a protection scheme which mimics the characteristic of inverse time overcurrent relay. In other words, the detection time inversely varies with magnitude of fault current.

2.1.2 Rate of Change

The current derivative method [28–30] is based on the assumption that DC current changes sharply as a result of fault, such that $\Delta I_{dc} = I_{dc_k} - I_{dc_{k-1}}$ will yield a large value. The works cited here showed that this method can successfully select the faulted line in a DC microgrid system. Besides that, with careful calculation of threshold, it can classify the types of faults, such line and bus fault.

DC current is not the only parameter used to calculate rate of change, as Sneath [31] proposed a method based on DC voltage instead. The rate of change of voltage, or termed as ROCOV in his work, can function effectively as an indicator in determining faulted line in a HVDC multi-terminal system.

The selection of threshold is a repeat process to determine the minimum value that will differentiate the fault condition from the cases in which circuit breaker should not trip. Besides that, the threshold is very much dependent on the sampling frequency.

2.1.3 Differential Detection

Differential detection assumes the amount of current appearing at one end should be same at another on a branch during normal operation, yielding almost zero when summing them up. This method forms the backbone of protection system for most of the conventional AC systems. It was reported in Park's work [32] in which similar concept was adopted in HVDC system. Azad [33] and Irnawan [34] took rather different approach in calculating the differential current, whereby the sum of currents of all lines connected to the associated bus was considered instead; if the sum is non-zero, the fault is detected.

2.1.4 Traveling Wave

Although the traveling wave is not used particularly to detect DC fault, it is still worth mentioning here as far as the identification of faulted line in multi-terminal HVDC system is concerned.

The application of traveling wave on HVDC system was discussed in several works [35–38, 52]. Similar to how it works on AC system, the surge arrival time is recorded by detector installed at each terminal, with that the fault location can be estimated.

The complexity arises when the system is highly meshed and there are many paths the reflected wave can travel. Another downside is that the data collection requires high sampling rate. Instead of measuring the wave-front, natural frequency of the transmission line [39] is a useful criterion to locate the fault just as effectively.

2.1.5 Wavelet Transform

The wavelet transform is a type of signal processing tools suitable for non-stationary signal. The closest relative of wavelet transform is short-time Fourier transform (STFT), but the latter has fixed window size presenting difficulty to find a balance between time and frequency resolution. The working principle of both signal processing tools will be discussed in Chapter 5 and 7. For now, it is important to know that the wavelet transform is popular for its capability of capturing high frequency transient caused by short-circuit fault.

The wavelet-based method was firstly introduced to AC system [40–44]. Thereafter, researchers began to explore its application on HVDC system. The wavelet transform is applied to DC currents generating wavelet coefficient which suggests possible occurrence of fault [45]. Cheng [38] used similar methodology but on CSC-HVDC system, extracting certain characteristic harmonics with the help of wavelet transform. Some papers [46, 47] suggested using the wavelet coefficient of DC voltage as one of the fault criteria, in addition to DC current. A method based on wavelet coefficient of sheath voltage in cable was also proposed [48]. The threshold is dependent on choice of mother wavelet and system topology. Therefore, each author had their own way of selecting suitable threshold.

2.1.6 Others

For CSC-HVDC system, a fault detection based on transient harmonic was proposed by Zheng [49] whereby it took the harmonic contents and pulse as the fault criteria. This method is able to identify the internal fault and external fault notwithstanding the sensitivity to high ground impedance. The method with similar concept was also seen in

Kong's work [50]. However, as far as the detection speed is concerned, the time it takes to measure the pulse might be unsuitably long for VSC-HVDC system. The absence of DC filter also means that the boundary impeding certain harmonics from flowing into DC line is missing.

Mohammad Farshad [51] proposed a detection method by comparing the measured voltage with the already known signal and the degree of similarity was computed using Pearson correlation coefficient. In this method, only the DC voltage measurement is required. The reference signals are obtained by iterative process considering all possible fault scenarios.

2.1.7 Performance comparison

DC fault can be identified by the time- and frequency-domain analysis of the DC current. Direct measurement of current is a simple and straightforward method to determine the occurrence of DC fault in time domain. However, selective tripping cannot be achieved by merely relying on current magnitude. In this regards, rate of change method offers better discrimination in a multi-terminal system. The downside is that it is vulnerable to the noise present in the real fault signals. Although traveling wave method is accurate, it requires high sampling frequency to calculate arrival time of wavefront. Hence, it is impractical to be implemented in real time. The pattern recognition method compares the measured voltage with the already known signal. The reference signals have to be obtained through iterative trainings, considering all possible fault scenarios. As for detection in frequency domain, wavelet transform (WT) has been prominently featured in literature. This signal processing tool is able to capture high frequency content in the rapidly changing DC fault current. Most of the existing proposals of fault detection only offer theoretical analysis with focus on simulation results. It will be interesting to

Table 2.1: Comparison of fault detection methods for DC transmission system.

	Method	**Advantage**	**Disadvantage**	**Simulation validation**	**Experimental validation**
Time domain	Direct measurment	1. Computationally simple	1. Inability to discriminate faulted line in MTDC	[22–26]	×
	Rate of change	1. Offer good discrimination without communication	1. Hard threshold required 2. Vulnerable to noise	[28–30]	×
	Traveling wave	1. Highly fast and accurate	1. High sampling rate required 2. Difficult to be implemented on real time	[35–38, 52]	×
	Pattern recognition	1. Simple, accurate	1. Large training data set required	[51]	×
	Capacitor discharge	1. Versatile, independent of hard threshold 2. High tolerance towards influence of fault parameter	1. Dependent on existence of DC-link capacitor	*	*
Frequency domain	Wavelet transform	1. Accurate 2. Immune to noise	1. High computational burden 2. Filtering introduces time delay	[38, 43–47]	*
	Short time Fourier transform	1. Fast, accurate 2. Mature in embedded system domain	1. Vulnerable to noise	*	*

×=absent in literature, *=proposed in this thesis

re-evaluate their effectiveness on real fault signal, in which the noise will become part of the picture.

2.2 Fault Behavior and System Topology

The protection requirements can be subject to the grid topology, as depicted in Fig. 2.1 [53]. The radial grid is the simplest and most cost-effective, as each converter is only connected to one DC line. The ring grid connects all terminals in a circular fashion resulting in each converter connected to two DC lines. As for the meshed grid, more connections enhances reliability in the system, however it also translates to higher cost.

Each topology performs differently for a given fault scenario [54]. The meshed grid tends to result in higher fault current compared to radial and ring grid. The ring grid has the lowest transient overcurrent. Apart from that, it offers system redundancy and can maintain the power flow without much dynamic change. Therefore, it was regarded as favorable candidate for fault performance [20].

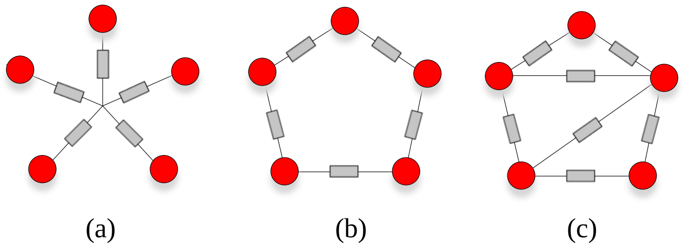


FIGURE 2.1: Nodal representation of different DC network topology. Converter terminal is represented by red node. (a) Radial, (b) ring and (c) meshed.

In addition to grid topologies, the fault response of different types of VSC configuration, depicted in Fig. 2.2, was also studied [5]. It was noted that the bipolar with metallic return is least affected by DC fault.

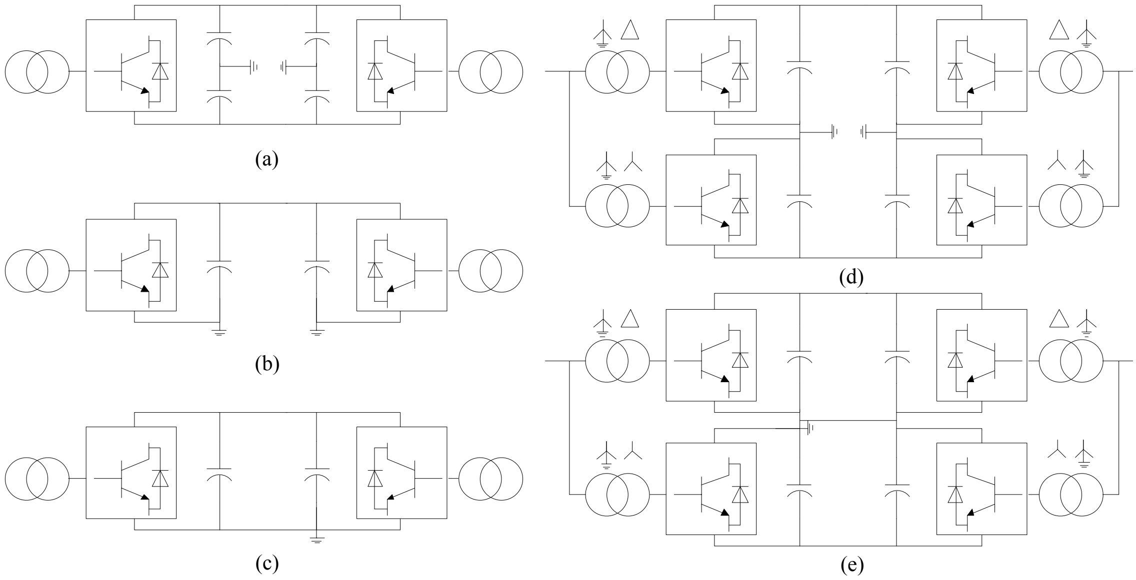


FIGURE 2.2: VSC configuration. (a) Symmetric monopole; (b) Asymmetric monopole with ground return; (c) Asymmetric monopole with metallic return; (d) Bipolar with ground return; (e) Bipolar with metallic return.

Due to different operating conditions, the fault behavior varies from topology to topology. Table 2.2 summarizes the effect of pole-to-ground (PG) and pole-to-pole (PP) fault on each of the mentioned topologies. For PG fault, the asymmetric monopole and faulted pole of bipolar configuration demonstrate identical behavior, with V_{dc} falling to 0 [6]. Even so, the healthy pole converter of bipolar configuration is not affected, hence it is able to continue normal operation. The symmetric monopole responds to PG fault

TABLE 2.2: Response of system configurations to various fault types [5, 6].

Configuration	**PG fault**		**PP fault**	
	DC voltage	**DC current**	**DC voltage**	**DC current**
Asymmetric monopole	$V_{dc} \rightarrow 0$	$I_{cap} \uparrow\uparrow$	-	
Symmetric monopole	Faulted pole: $V_{dc}/2 \rightarrow 0$ Healthy pole: $V_{dc}/2 \rightarrow V_{dc}$	Faulted pole: $I_{cap} \uparrow$ Healthy pole: temp. transient	$V_{dc} \rightarrow 0$	$I_{cap} \uparrow\uparrow$
Bipole	Faulted pole: $V_{dc} \rightarrow 0$ Healthy pole: V_{dc}	Faulted pole: $I_{cap} \uparrow\uparrow$ Healthy pole: temp. transient		

PG=pole-to-ground, PP=pole-to-pole, V_{dc}=nominal DC voltage, I_{cap}=DC-link capacitive discharge

in similar manner, but smaller voltage drop on faulted pole ($V_{dc}/2$ to 0). For this reason, the contribution of DC capacitor to fault current is relatively smaller compared to other two [5]. The power flow has to be distributed to other available path, which results in the healthy pole obtaining full V_{dc} and operating in overload mode. PP fault requires the system, whether it is symmetric monopole or bipole, to be immediately shut down by removing the faulted positive and negative poles from the grid. The DC voltage will plunge to 0. At the same time, the DC capacitors of both poles will discharge causing rapidly rising fault current. It is clear that the difference between PG and PP faults allows us to distinguish them by monitoring the changing pattern of DC voltage and current.

The recovery stage can be approached and improved by carefully designing the control strategies. The control strategy following fault clearance was firstly reported for CSC-system, in which Reeve [55] showed that it was necessary to change the current reference to provide the best recovery response. The active power reference needs to be set to zero during recovery. This is to ensure that the terminal controlling DC voltage will not have to compensate the loss of power before the DC voltage stabilizes [20, 56]. The overcurrent limitation controllers are proposed [26, 57], which effectively helps to ease the protective device requirements.

2.3 Fault Clearance

2.3.1 DC circuit breaker

The conventional AC system protection has matured over time with wide availability of standards and guidelines. With respect to that, the interest in multi-terminal HVDC system is relatively recent and the protection in this domain has a lot to catch up.

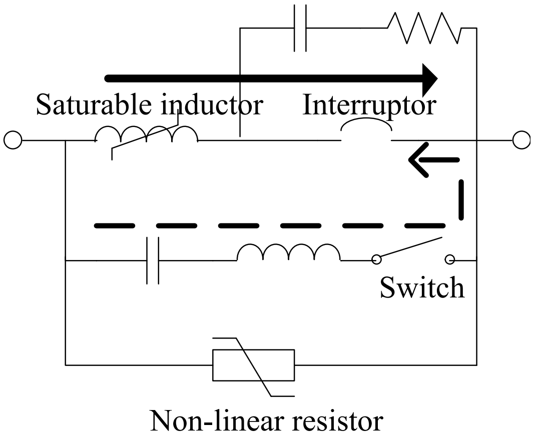
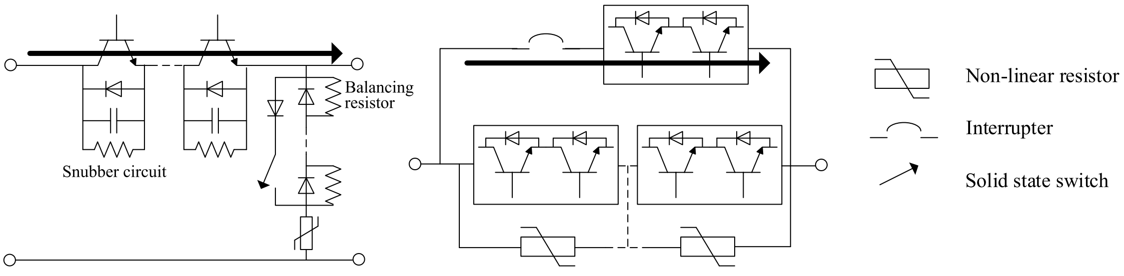


FIGURE 2.3: Circuit diagram showing the structure of DC breaker. Solid arrow line indicates flow of DC current while dash arrow line indicates flow of counter current generated by L-C.[1, 2]

One major challenge the HVDC systems need to tackle is the absence of zero crossing, which disallows the existing AC breaker to be employed on DC lines. Hence, the DC breaker has to be properly designed with the mechanism of forcing the fault current drop to zero. This can be done by pairing resonant circuit with interrupter, which is depicted in Fig. 2.3. When the fault is detected, the main interrupter on the line, which is normally closed, will be opened. At the same time, the switch in the commutation circuit will be closed. The commutation circuit is now in series with the contact opened by the interrupter. The then-charged capacitor commences to release the discharging current in a direction opposing to the fault current, in an effort to forcefully extinguish the arc across the contact. As soon as the fault current is driven to zero, the circuit breaker will have the opportunity to successfully interrupt the circuit. However, the current is still flowing; it switches path to the commutation circuit instead. The commutation stage is initiated.

Using the resonant circuit is a way of quenching the electric arc by brute force. In addition, the passive elements are normally bulky and heavy making them undesirable as far as the size of DC breaker is concerned. Hence, there has been an increasing focus recently on designing a DC breakers based on non-resonance type commutation circuit. With the power electronics becoming more and more efficient and matured, it has become widely acceptable to be incorporated as part of the working mechanism in a breaker. The use of power electronic also offers the users more freedom and flexibility to control how a breaker should work.



(a) (b)

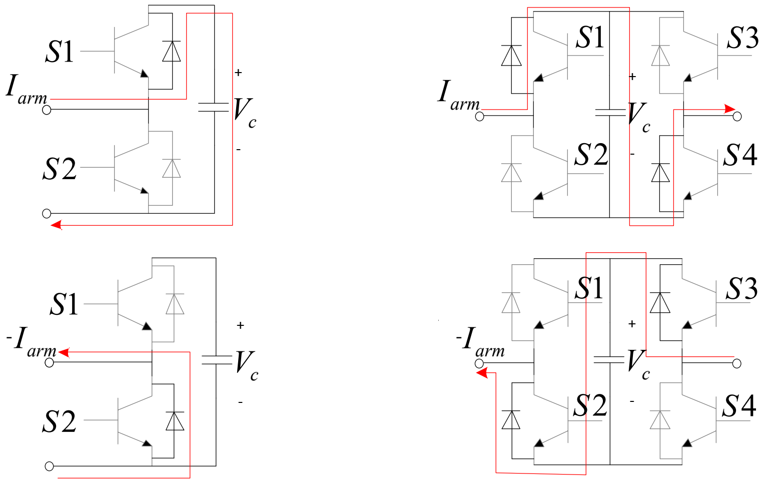
FIGURE 2.4: Non-resonant type DC breakers proposed in literatures. (a) Solid state based DC breaker [3] and (b) hybrid DC breaker [4]. Solid arrow line indicates the flow of DC current.

A circuit breaker entirely based on solid state switch has been proposed [3] and presented in Fig. 2.4(a). While the conduction loss is always the primary issue with every solid state switch, the loss reported by the authors is considerably low, around $1 - 2\%$. As the fault current is drained in the form heat due to its interaction with resistance of solid state switch, this type of circuit breaker needs to be equipped with proper cooling facility. At the expense of conduction loss, the quick fault clearance (few ms) is one of the advantages that make solid state circuit breaker a remarkable option, especially for a modern, low impedance HVDC system.

ABB integrates the state-of-the-art solid state switch breaking technology with mechanical switch, termed as hybrid HVDC breaker [4]. Using the solid state switch (see Fig. 2.4(b)), the mechanism of extinguishing electric arc has become redundant, hence substantially reducing the complexity as encountered in conventional circuit breaker. Besides that, the fault clearance is performed electrically resulting in improved speed compared with its predecessor. The Bi-mode Insulated Gate Transistor (BiGT) along with arrester in parallel forms a module which can be expanded for higher rating.

2.3.2 Protection Strategy

There are several studies proposing protection strategies using different types of protective devices. The DC breaker is able to clear the fault fast enough without interrupting the continuous operation of healthy terminals and recovery process [47, 58]. The performance of DC breaker under influence of fault parameters and breaker setting was analyzed in Martinez-Velasco's work [59]. AC breaker is another possible protection device that can be used in multi-terminal system [20, 30]. This is usually accompanied with fast DC breaker which isolates the faulted line [60]. In order to drive the current to zero, the entire system has to be temporarily de-energized. The slow operation of AC breaker, requiring at least three cycles, causes the infeed AC current to flow through the anti-parallel diodes upon the blocking of VSC. This problem can be overcome by inserting bidirectional thyristors across VSC creating a path for AC current, hence minimizing the potential damage on the diodes [61, 62].



(A) Half bridge. (B) Full bridge.

FIGURE 2.5: Operation of MMC cell topologies during blocking stage.

TABLE 2.3: Switching states of half bridge and full bridge MMC

	$S1$	$S2$	$S3$	$S4$	I_{arm}	V_c
Half bridge	0	0	x	x	>0	V_c
	0	0	x	x	<0	0
Full bridge	0	0	0	0	>0	V_c
	0	0	0	0	<0	V_c

Two level VSC and half-bridge (HB) modular multilevel converter (MMC) are vulnerable to DC fault as they are unable to entirely prevent infeed AC current from flowing into fault point when the IGBTs are blocked. As a result, the accompanied freewheeling diodes have to withstand current level beyond their capability. One can choose to use the MMC topologies [18, 57, 63, 64] that support the fault ride-through capability. Fig. 2.5 demonstrates the operation of HB and FB cells and how the latter can support voltage on DC side providing fault blocking capability. The addition of IGBT in MMC cell, however, means higher loss and cost. Qin [65] presented a comparison analysis of different MMC topologies in terms of device number and power loss.

Chapter 3

Modeling, Control and Fault Analysis of VSC-HVDC System

The application of VSC is vast, extending from motor drive to bulk power transmission. In this chapter, the background of VSC-HVDC system, including configuration, modeling and control, is introduced. VSC is particularly vulnerable to DC fault because of the presence of DC-link capacitor. The analysis of DC fault is presented here to demonstrate how the discharge current contributes to high rate of fault current.

3.1 Configuration of HVDC System

Fig. 3.1 shows the of rectifier side of VSC-HVDC system with asymmetric monopole configuration, where i and j denote the terminals. The $VSCi$ serves as the interface between AC and DC circuit. The power is transfered from one terminal to another through DC line (TL_{ij}). Other elements seen in the configuration are detailed below:

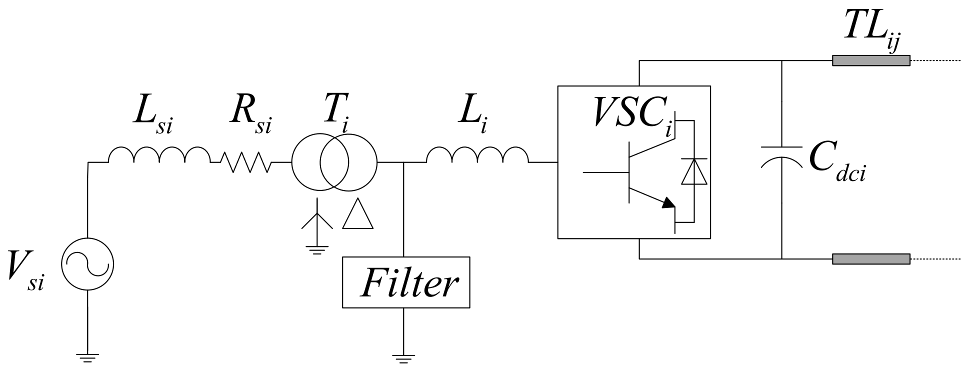


FIGURE 3.1: Typical VSC-HVDC configuration.

- AC Source

  The three-phase AC source is represented by V_{si} behind the source impedance consisting of R_{si} and L_{si} in the figure. For high voltage application, the voltage level is above $1KV_{rms}$.

- Transformer

  The grounded wye-delta transformer (T_i) is used to step up the voltage level suitable for the converter. The grounding on the neutral point of the wye connection is able to support the loop of zero-sequence current on primary winding preventing it from entering the system. The common leakage impedance of transformer is 0.1-0.2 pu [66].

- Filter

  The filter eliminates the unwanted harmonics generated by the non-linear switching action. For VSC, the pulse-width modulation (PWM) can be employed to push the harmonics to high order, hence simplifying the filter requirement.

- Phase Inductor

  The phase inductor (L_i) is provided and connected in series to maintain continuous current.

- Converter

  In contrast to traditional thyristor which can be only turned on, the insulated gated bipolar transistor (IGBT), as an example of VSC, has two degrees of freedom. The VSC can be regulated to control the amplitude modulation index (m_a) and phase displacement (φ).

- DC-link Capacitor

  To generate constant DC voltage with minimum ripple, DC-link capacitors (C_{dci}) can be installed across DC bus. Large DC capacitor, despite improving steady state performance, is likely to introduce large current during the occurrence of DC fault. Therefore, the capacitor size cannot be arbitrarily selected. One can determine the capacitor size by taking into account of steady state and dynamic response performance, based on the time constant described in (3.1). It is recommended that the optimum time constant is less than 5ms.

  $$\tau = \frac{C_{dci}V_{dc}^2}{2S_n}. \tag{3.1}$$

  where τ is time constant, C_{dci} is DC-link capacitor, V_{dc} is DC voltage and S_n is rated power.

3.2 Modeling of VSC-HVDC System

The equivalent circuit of HVDC is depicted in Fig. 3.2. The total inductance and resistance, including source, transformer impedance and phase reactor in Fig. 3.1, is now represented by R_{si} and L_{si}. The equivalent circuit is divided into two sides: AC

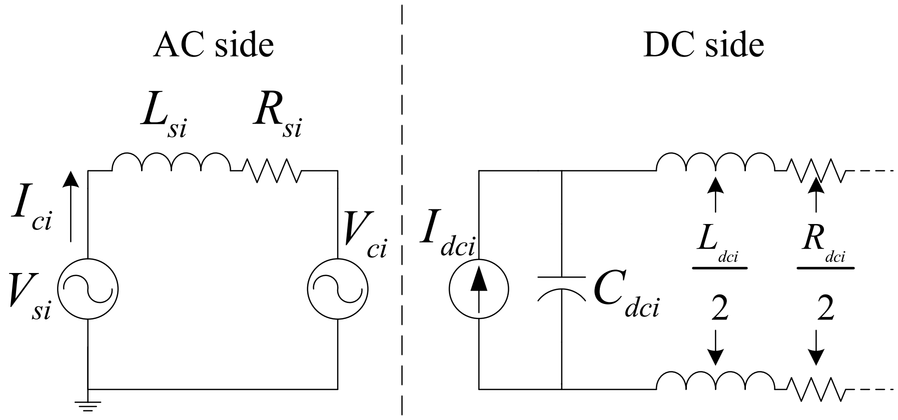


FIGURE 3.2: Equivalent HVDC circuit.

and DC. The VSC can be thought as voltage source (V_{ci}) on AC side and direct current source (I_{dci}) on DC side.

3.2.1 AC Circuit Modeling

Applying Kirchoff's Voltage law on the AC circuit:

$$V_{si} - V_{ci} = R_{si} I_{ci} + L_{si} \frac{\mathrm{d}I_{ci}}{\mathrm{d}t}. \tag{3.2}$$

To simplify the analysis of three-phase circuit, Clark transformation is employed on (3.2) resulting in following:

$$V_{si,\alpha\beta} - V_{ci,\alpha\beta} = R_{si} I_{ci,\alpha\beta} + L_{si} \frac{\mathrm{d}I_{ci,\alpha\beta}}{\mathrm{d}t}. \tag{3.3}$$

Applying Park's transformation:

$$\begin{aligned} V_{si,\alpha\beta} &= V_{si,dq}e^{j\omega t} \\ V_{ci,\alpha\beta} &= V_{ci,dq}e^{j\omega t} \\ I_{ci,\alpha\beta} &= I_{ci,dq}e^{j\omega t}. \end{aligned} \tag{3.4}$$

where $\omega = 2\pi f$

Then substituting (3.4) into (3.3):

$$V_{s,dq}e^{j\omega t} - V_{c,dq}e^{j\omega t} = R_{si}I_{c,dq}e^{j\omega t} + L_{si}\frac{\mathrm{d}(I_{ci,dq}e^{j\omega t})}{\mathrm{d}t}. \tag{3.5}$$

Dividing the equation above by $e^{j\omega t}$:

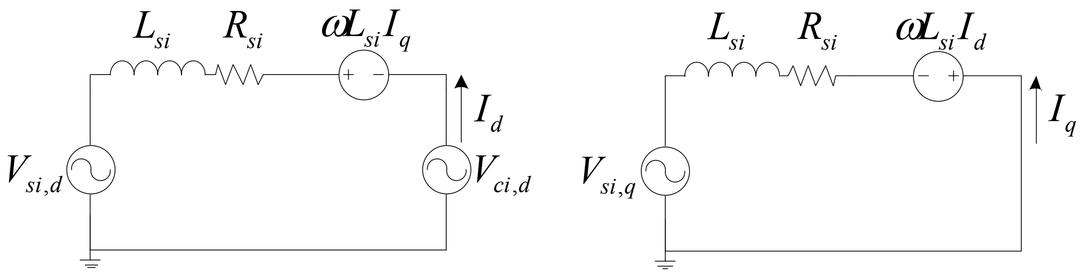
$$V_{s,dq} - V_{c,dq} = R_{si}I_{c,dq} + L_{si}\frac{\mathrm{d}I_{ci,dq}}{\mathrm{d}t} + j\omega L_{si}I_{c,dq}. \tag{3.6}$$

(3.6) can be arranged in the matrix form:

$$\begin{bmatrix} V_{s,d} \\ V_{s,q} \end{bmatrix} = R_{si}\begin{bmatrix} I_{ci,d} \\ I_{ci,q} \end{bmatrix} + \omega L_{si}\begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}\begin{bmatrix} I_{ci,d} \\ I_{ci,q} \end{bmatrix} + L_{si}\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} I_{ci,d} \\ I_{ci,q} \end{bmatrix} + \begin{bmatrix} V_{c,d} \\ V_{c,q} \end{bmatrix}. \tag{3.7}$$

where $\begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}$ is the matrix form of complex number j.

Assume the alpha-axis entirely aligning with d-axis, the voltage of q-axis will become zero (proof given in Appendix A) and the resulting equations are:



(A) d-axis circuit.

(B) q-axis circuit.

FIGURE 3.3: Equivalent AC model in $d-q$ domain.

$$\begin{aligned} V_{s,d} - V_{c,d} &= R_{si} I_{c,d} + L_{si} \frac{\mathrm{d} I_{ci,d}}{\mathrm{d}t} + \omega L_{si} I_{ci,q} \\ V_{s,q} &= R_{si} I_{c,q} + L_{si} \frac{\mathrm{d} I_{ci,q}}{\mathrm{d}t} - \omega L_{si} I_{ci,d}. \end{aligned} \tag{3.8}$$

Based on (3.8), the HVDC equivalent circuit can be represented in Fig. 3.3, as seen from AC side.

3.2.2 DC Circuit Modeling

Besides direct current source and DC capacitor as seen in Fig. 3.1, the DC circuit has to include that of the opposite terminal. The DC line model can be treated as series resistance and inductance and shunt capacitance due to the interaction between positive and negative pole lines.

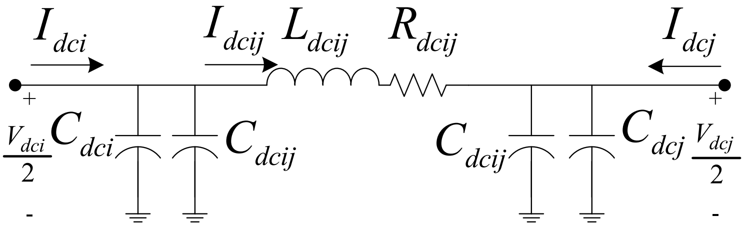


FIGURE 3.4: Equivalent circuit of DC side.

The equations that define the circuit above are as follows:

$$C_{dc}\frac{\mathrm{d}V_{dci}}{\mathrm{d}t} = I_{dci} - I_{dcij} \tag{3.9}$$

$$L_{sij}\frac{\mathrm{d}I_{dcij}}{\mathrm{d}t} + R_{sij}I_{dcij} = \frac{V_{dci}}{2} - \frac{V_{dcj}}{2}. \tag{3.10}$$

where C_{dc} is the parallel equivalent capacitance of C_{dci} and $C_{dcij}/2$.

3.2.3 Full Model

Neglecting the loss, the relationship between AC and DC circuit models is tied by power balance such that the total active power injected by the AC source is equal to the DC power, as described in (3.11-3.13).

$$\begin{aligned} S_{dq} &= \frac{3}{2}V_{si,dq}I^*_{ci,dq} \\ &= \frac{3}{2}V_{si,dq}(I_{ci,d} - jI_{ci,q}). \end{aligned} \tag{3.11}$$

$$P_{ac} \approx P_{dc}. \tag{3.12}$$

$$\begin{aligned} \frac{3}{2}V_{si,dq}I_{ci,d} &= V_{dci}I_{dci} \\ I_{dci} &= \frac{3}{2}\frac{V_{si,dq}I_{ci,d}}{V_{dci}}. \end{aligned} \tag{3.13}$$

As mentioned, the VSC is seen as direct current source from DC side and it is represented in (3.13).

3.3 Control in HVDC System

3.3.1 Feedforward Decoupled *dq* Current Control

Equation (3.8) implies the existence of mutual coupling between d and q-axis component (due to ωL_{si} term), in this case the feedback control will not be suitable because the coupling adds the complexity to the pathway in control system, significantly slowing down the performance. In order to accelerate the response, feedforward control has been suggested by the literature. The mechanism of such control is not error-based; instead it is based on the knowledge in the form of mathematical model of system, thus (3.8) has to be considered.

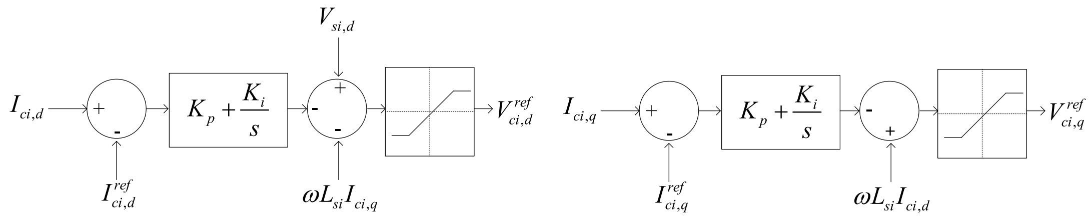
Using PI controller to track the dq-current reference, the VSC output voltage can be assumed to be:

$$\begin{aligned} V_{ci,d} &= -(K_p + \frac{K_i}{s})(I_{ci,d} - I_{ci,d}^{ref}) - \omega L_{si} I_{ci,q} + V_{si,d} \\ V_{ci,q} &= -(K_p + \frac{K_i}{s})(I_{ci,q} - I_{ci,q}^{ref}) + \omega L_{si} I_{ci,d} + V_{si,q}. \end{aligned} \tag{3.14}$$

where K_p and K_i are the proportional and integral gains. Substituting (3.14) into original equation of VSC-HVDC model (3.6) yields:

$$\begin{aligned} L_{si}\frac{\mathrm{d}I_{ci,d}}{\mathrm{d}t} + RI_{ci,d} &= (K_p + \frac{K_i}{s})(I_{ci,d} - I_{ci,d}^{ref}) \\ L_{si}\frac{\mathrm{d}I_{ci,q}}{\mathrm{d}t} + RI_{ci,q} &= (K_p + \frac{K_i}{s})(I_{ci,q} - I_{ci,q}^{ref}). \end{aligned} \tag{3.15}$$

The equations above have justified that we have decoupled stable tracking error dynamics for I_d and I_q. Fig. 3.5 shows the complete structure of feedforward decoupled current control.



(A) I_d.

(B) I_q.

FIGURE 3.5: Inner current controller.

3.3.2 Outer Controllers

The purpose of DC voltage controller is to maintain the DC voltage so that it matches the reference value. Considering the power balance at the VSC terminal:

$$\begin{aligned} P_{ac} + P_{dc} + P_{cap} &= 0, \\ \frac{3}{2} V_{si,d} I_{ci,d} + V_{dci} I_{dci} + V_{dci} I_{cap} &= 0. \end{aligned} \tag{3.16}$$

where P_{cap} and I_{cap} are the power generated by capacitor and corresponding capacitor current, respectively.

Eqn. (3.16) can be arranged by moving I_{cap} to left hand side of equation, yielding:

$$I_{cap} = -\left(\frac{3}{2} \frac{V_{si,d}}{V_{dci}} I_{ci,d} + I_{dci} \right). \tag{3.17}$$

The I_{cap} can be represented in term of capacitive value,

$$I_{cap} = C_{dci} \frac{\mathrm{d}V_{dc}}{\mathrm{d}t}. \tag{3.18}$$

Combining (3.17) and (3.18) results in:

$$\frac{\mathrm{d}V_{dc}}{\mathrm{d}t} = -\frac{3V_{si,d}}{2C_{dci}V_{dci}}\left(I_{ci,d} + \frac{2V_{dci}}{3V_{si,d}}I_{dci}\right). \tag{3.19}$$

Hence, it is clear that the DC voltage can be controlled by I_d. Eqn. (3.19) has the I_{dci} term, which can be used as the feedforward in the fixed DC voltage controller in order to avoid slow dynamic response. The block diagram is given in Fig. 3.6:

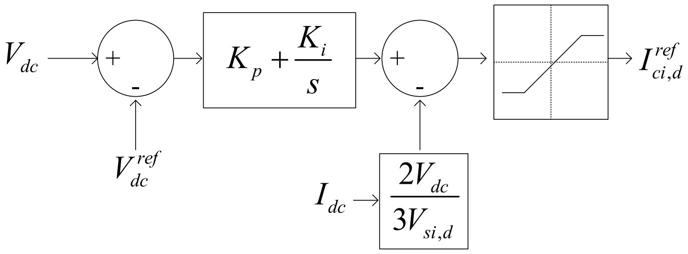


FIGURE 3.6: Fixed V_{dc} controller.

Similarly, the active power controller is used to regulate the active power transferred from AC side. Equation (3.13) suggests that active power flow can be controlled by d-axis current, with that the controller is shown in Fig. 3.7.

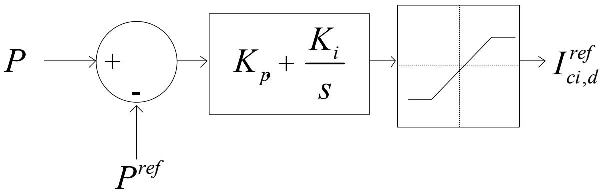


FIGURE 3.7: Fixed P_{ac} controller.

The second term in the right hand side of (3.11) implies that we can regulate the reactive power by controlling q-axis current. Hence, the reactive Power Controller is implemented as in Fig. 3.8.

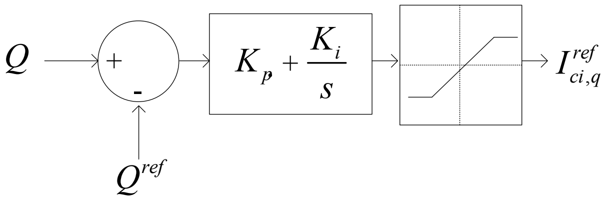


FIGURE 3.8: Fixed Q_{ac} controller.

The AC voltage can be maintained constant by reactive power compensation, hence the AC voltage controller is designed in a similar way as reactive power controller in which q-axis current is tracked. The AC voltage controller is depicted in Fig. 3.9.

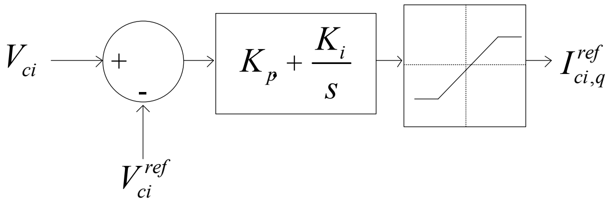


Figure 3.9: Fixed V_{ci} controller.

The complete control structure is illustrated in Fig. 3.10. There are two controllable parameters on both d and q-axes. In a two-terminal HVDC system, it is a common practice to assign one of the terminals to act as slack bus, which essentially controls the DC voltage of the system. The flow of active power is determined by the polarity of P^{ref}. For load terminal, AC voltage control is required to output desired voltage level. Even though the control strategy here is designed based on transfer function of VSC, fundamentally it is also applicable to MMC [67].

It is a common practice to adopt phase-locked loop (PLL) to generate angle reference for computation of converting abc-axis of current into dq-axis. There have been some studies that study the impact of PLL gain on the dynamic behavior and stability limit using small signal analysis. An accurate representation of the internal variable of plant, control loop and interface between terminals provides mathematical understanding of their relationship. Detailed analysis can be found in [68–70].

3.3.3 Tuning Technique of Converter Controller

The K_p and K_i in the control schemes mentioned in previous subsection can be optimally obtained by various approaches to achieve excellent loop performance. It is the easiest

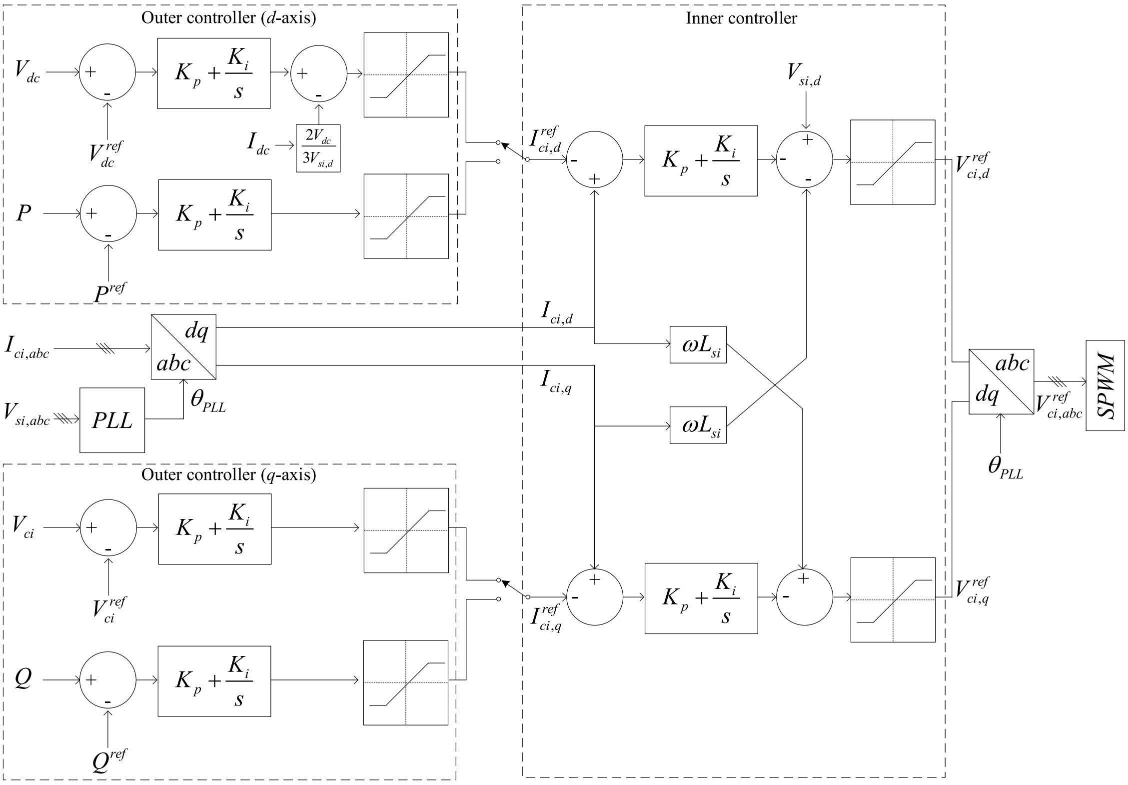


FIGURE 3.10: Control scheme of VSC-HVDC system.

way to tune the PI parameter using trial-and-error technique. The process to determine the right parameter is repetitive and tedious, but the range can be narrowed down with sufficient understanding of open loop transfer functions of the system.

Modulus optimum is widely adapted to approach the tuning of low order plant. The central idea of this method is to cancel the largest time constant in the transfer function, while ensuring the amplitude of the closed-loop frequency response is close to unity for high frequency [71].

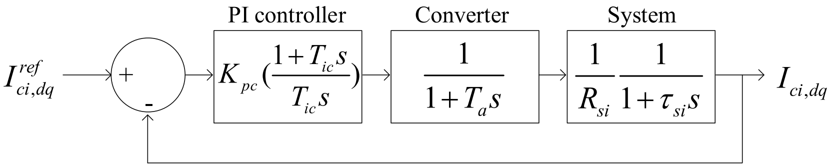


FIGURE 3.11: Transfer function of inner current controller.

The transfer function of independent I_d and I_q control loops is given in Fig. 3.11. Neglecting the feedforward term, the open loop transfer function of inner current controller can be written as:

$$G_{c,OL} = K_{pc}\left(\frac{1+T_{ic}s}{T_{ic}s}\right)\left(\frac{1}{1+T_a s}\right)\left(\frac{1}{R_{si}}\frac{1}{1+\tau_{si}s}\right). \tag{3.20}$$

where K_{pc} and T_{ic} are the PI parameters, T_a is the converter switching time and $\tau_{si}{=}L_{si}/R_{si}$.

According to modulus optimum's criteria, the pole associated with the system element has to be eliminated. Thus, the time constant of PI controller is assigned to:

$$T_{ic} = \tau_{si}. \tag{3.21}$$

Consider the cutoff frequency, ω_c, to be around $1/2T_a$. The unity gain of open loop transfer at ω_c is written as:

$$|G_{c,OL}| = \left|\left(\frac{K_{pc}}{j\tau_{si}\omega_c}\right)\left(\frac{1}{1+jT_a\omega_c}\right)\left(\frac{1}{R_{si}}\right)\right|_{s=j\omega_c} = 1. \tag{3.22}$$

Therefore, K_{pc} will take the following form:

$$K_{pc} = \frac{\tau_{si}R_{si}}{2T_a}. \tag{3.23}$$

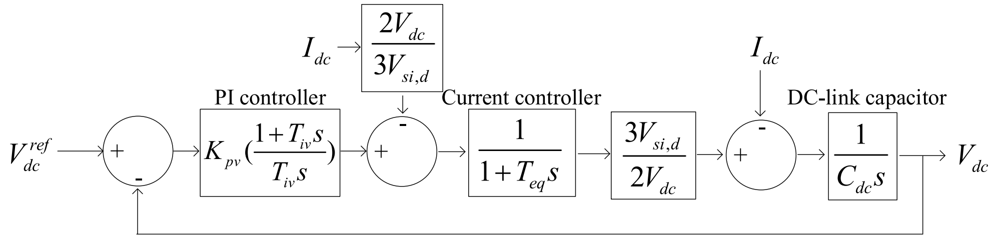


FIGURE 3.12: Transfer function of DC voltage controller.

The block diagram of DC voltage controller is depicted in Fig. 3.12. Similarly, the open loop transfer function can be derived as:

$$G_{v,OL} = K_{pv}\left(\frac{1+T_{iv}s}{T_{iv}s}\right)\left(\frac{1}{1+T_{eq}s}\right)\left(\frac{V_{si,d}}{V_{dc}}\right)\left(\frac{1}{C_{dc}s}\right). \tag{3.24}$$

where K_{pv} and T_{iv} are the PI parameters and T_{eq} is the total time delay introduced by inner current controller.

If the modulus optimum technique were to be applied in this transfer, T_{iv} would be equal to T_{eq}, canceling the third term in right hand side of (3.24). However, this setting would produce two poles at the origin and affect the stability of system. To address this issue, one can opt to use the symmetrical optimum technique instead. The basis of this technique is to maximize the phase margin. As such, the system can tolerate more delays, which is important for DC voltage controller which should have some degree of delay in order to complement the inner current controller.

Firstly, we have to determine the phase angle of $G_{v,OL}$.

$$\begin{aligned}\angle G_{v,OL} &= tan^{-1}(T_{iv}\omega) - 90^\circ - tan^{-1}(T_{eq}w) - 90^\circ \\ &= tan^{-1}(T_{iv}\omega) - tan^{-1}(T_{eq}w) - 180^\circ \\ &= \theta_m - 180^\circ.\end{aligned} \tag{3.25}$$

where phase margin θ_m=$tan^{-1}(T_{iv}\omega) - tan^{-1}(T_{eq}w)$.

The maximum phase margin can be obtained by differentiating θ_m:

$$\begin{aligned}\frac{\mathrm{d}}{\mathrm{d}\omega_c}\theta_m = \frac{\mathrm{d}}{\mathrm{d}\omega_c}\left[tan^{-1}(T_{iv}\omega_c) - tan^{-1}(T_{eq}\omega_c)\right] &= 0, \\ \frac{T_{iv}}{1+(T_{iv\omega_c})^2} - \frac{T_{eq}}{1+(T_{eq\omega_c})^2} &= 0.\end{aligned} \tag{3.26}$$

The solution of (3.26) is:

$$\omega_{c,max} = \frac{1}{\sqrt{T_{iv}T_{eq}}}. \tag{3.27}$$

Substituting $\omega_{c,max}$ back to the phase margin results in:

$$\theta_m = tan^{-1}\left(\sqrt{\frac{T_{iv}}{T_{eq}}}\right) - tan^{-1}\left(\sqrt{\frac{T_{eq}}{T_{iv}}}\right). \tag{3.28}$$

Let $tan^{-1}\left(\sqrt{\frac{T_{iv}}{T_{eq}}}\right) = \phi$, so $tan^{-1}\left(\sqrt{\frac{T_{eq}}{T_{iv}}}\right) = \phi - 90°$.

Eqn. (3.28) is rearranged to become:

$$\theta_m = 2\phi - 90°. \tag{3.29}$$

Similarly,

$$sin(\theta_m) = cos(2\phi). \tag{3.30}$$

Applying half-angle trigonometry,

$$\sqrt{\frac{T_{iv}}{T_{eq}}} = tan\phi = \sqrt{\frac{1 + sin\theta_m}{1 - sin\theta_m}}. \tag{3.31}$$

With this, T_{iv} can be obtained as follows.

$$\begin{aligned} T_{iv} &= T_{eq}\sqrt{\frac{1+sin\theta_m}{1-sin\theta_m}} \\ &= T_{eq}a^2. \end{aligned} \tag{3.32}$$

where a is the symmetrical distance between $1/T_{iv}$ to $\omega_{c,max}$.

Hence, K_{pv} can be obtained by finding the unity frequency response of $G_{v,OL}$ at $\omega_{c,max}$:

$$K_{pv} = \frac{T_c}{aKT_{eq}}. \tag{3.33}$$

where T_c=$1/\omega C_{dc}$ and K=$V_{si,d}/V_{dc}$.

3.4 Fault Analysis

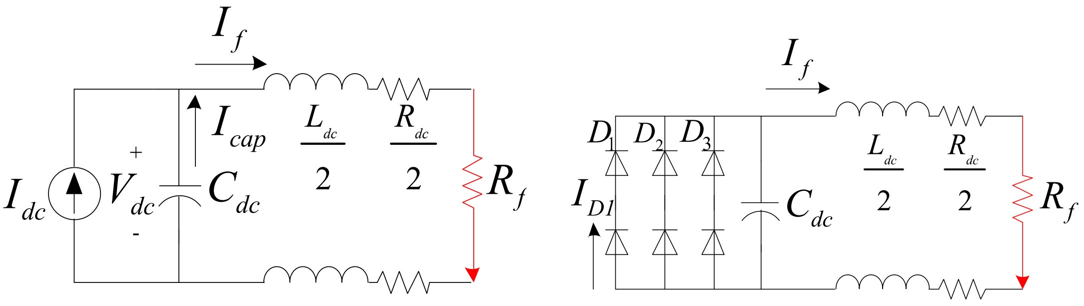
3.4.1 Introduction

The DC faults in HVDC system can classified into following types: DC bus, pole-to-ground (PG), pole-to-pole (PP).

DC cable is more prone to PG fault caused by insulation aging. The system earthing configuration determines the formation of fault current loop, thus the severity of such fault is hard to be generalized and can vary from system to system [72].

Due to direct exposure to air, the overhead line is subject to occurrence of PG and PG faults with higher degree of likelihood. While PP fault is not influenced by the system earthing, the fault current can penetrate the system extremely fast due to the discharge of DC-link capacitor. Because of the impact of PP fault, it is always treated as the most representative DC fault in literature.

The PP fault is illustrated in Fig. 3.13 [45, 62, 73, 74]. For simplicity, the cable is represented by a Π-model equivalent resistor and inductor. The PP fault can be thought as shorting the upper line to lower line via a fault resistor (R_f). L_{dc} and R_{dc} are the lumped parameters of sectional line in which the fault current loop forms. I_{dc} is the current injected from AC side.



(A) Stage 1: DC-link capacitor discharge. (B) Stage 2: Diode conducting.

FIGURE 3.13: Equivalent fault circuit.

Fig. 3.13a shows the initial stage of PP fault. The circuit can be described in the following differential equation:

$$\frac{\mathrm{d}^2 I_f}{\mathrm{d}t^2} + \frac{R_{dc} + R_f}{L_{dc}} \frac{\mathrm{d}I_f}{\mathrm{d}t} + \frac{1}{L_{dc}C_{dc}} I_f = 0. \tag{3.34}$$

The differential equation can be solved in three different ways, depending on the value of R_f. Assuming that the R_{dc} is usually small for cable, such that $R_{dc} + R_f < 2\sqrt{L_{dc}/C_{dc}}$, the solution will result in an underdamped oscillation. Using initial conditions $V_{dc}(t_0) = V_0$ and $I_f(t_0^-) = I_0$, the solution can be obtained:

$$I_f(t) = e^{-\delta_1 t}\left(I_0 cos(\omega_1 t) + \frac{V_0/L - \delta_1 I_0}{\omega_1} sin(\omega_1 t)\right), \tag{3.35}$$

$$V_{dc}(t) = e^{-\delta_1 t}\left(V_0 cos(\omega_1 t) + \frac{\delta_1 V_0 - I_0/C}{\omega_1} sin(\omega_1 t)\right), \tag{3.36}$$

where $\delta_1{=}\frac{R_{dc}+R_f}{2L_{dc}}$, $\omega_0{=}\sqrt{\frac{1}{L_{dc}C_{dc}}}$ and $\omega_1{=}\sqrt{\omega_0^2-\delta_1^2}$.

Under the condition $R_{dc}+R_f > 2\sqrt{L_{dc}/C_{dc}}$, the solution will give an overdamped response. Similarly, using the same initial conditions, the fault current is represented in (3.37).

$$I_f(t) = Ae^{m_1 t} + Be^{m_2 t}, \tag{3.37}$$

where, $m_{1,2} = -\delta_1 \pm \sqrt{\delta_1^2-\omega_0^2}$;$B = \frac{m_1 m_2}{m_1+m_2}\left(CV_0 - \frac{I_0}{m_1}\right)$;$A = I_0 - B$.

The DC voltage (V_{dc}) reaches zero when the charges of DC-link capacitor (C_{dc}) has been drained. Now, the path of fault current switches to the three phase-legs of freewheeling diodes as the corresponding IGBTs are already blocked, as depicted in Fig. 3.13b. The line inductor (L_{dc}) disallows sudden change of current, therefore the initial current for this stage is $I_f(t_1) = I'_{f0}$. Since the circuit is now reduced to RL circuit, the expression of fault current is given:

$$L_{dc}\frac{\mathrm{d}I_f}{\mathrm{d}t} + R_{dc}I_f = 0. \tag{3.38}$$

The first order differential equation is solved:

$$I'_f(t) = I'_0 e^{-\frac{R_{dc}}{L_{dc}}t}, \tag{3.39}$$

$$I_{D1}(t) = I_{D2}(t) = I_{D3}(t) = I'_f(t)/3. \tag{3.40}$$

Table 3.1: System parameters for fault analysis

Parameters	**Value**
Line inductor (L_{dc12}, L_{dc21})	1.5 mH
Line resistor (R_{dc12}, R_{dc21})	0.3 Ω
DC-link capacitor (C_{dc1}, C_{dc2})	1000 μF
DC voltage (V_{dc})	300 kV
DC current (I_{dc})	-2 kA
Fault resistor (R_f)	1 Ω
Sampling frequency (f_s)	10000 Hz

3.4.2 Verification

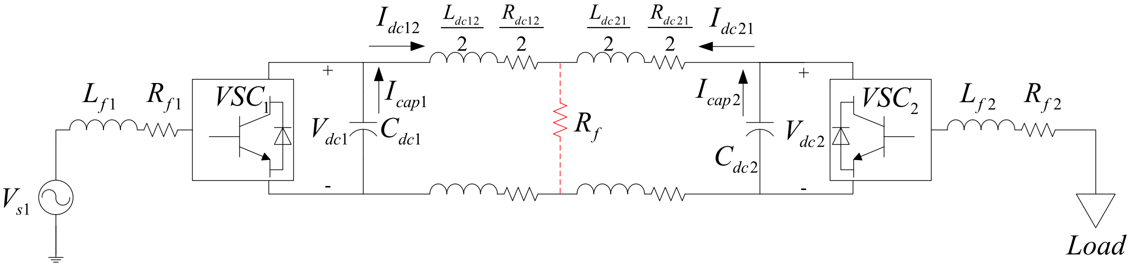


Figure 3.14: Simulated VSC-HVDC model.

A two-terminal (i, j=1,2) HVDC system, depicted in Fig. 3.14, is simulated in PSCAD/EMTDC to verify the fault analysis. The AC filter at each terminal is denoted by $L_{f(i,j)}$ and $R_{f(i,j)}$. The DC line is represented by simplified π-equivalent model consisting of L_{dcij} and R_{dcij}. The VSC ($VSCi$) has single, ungrounded DC-link capacitor ($C_{dc(i,j)}$). The PP fault is initiated in the middle of DC line. Hence, the line inductor and resistor involved in the fault loop are half of their full value. In real scenario, the VSCs will be blocked automatically when the fault current reaches 2 pu. However, the analysis here intends to illustrate how the fault event unfolds itself without any intervention. Relevant parameters are listed in Table 3.1.

Fig. 3.15 shows the analytical and simulation results at VSC_2 which is terminated with load. A good agreement between both results is achieved. During Stage 1, the capacitive discharge from C_{dc2} dominates the fault current. Stage 2 begins to take over as soon as DC voltage drops to zero, which happens at t_1=3.1 ms. Simultaneously, the fault

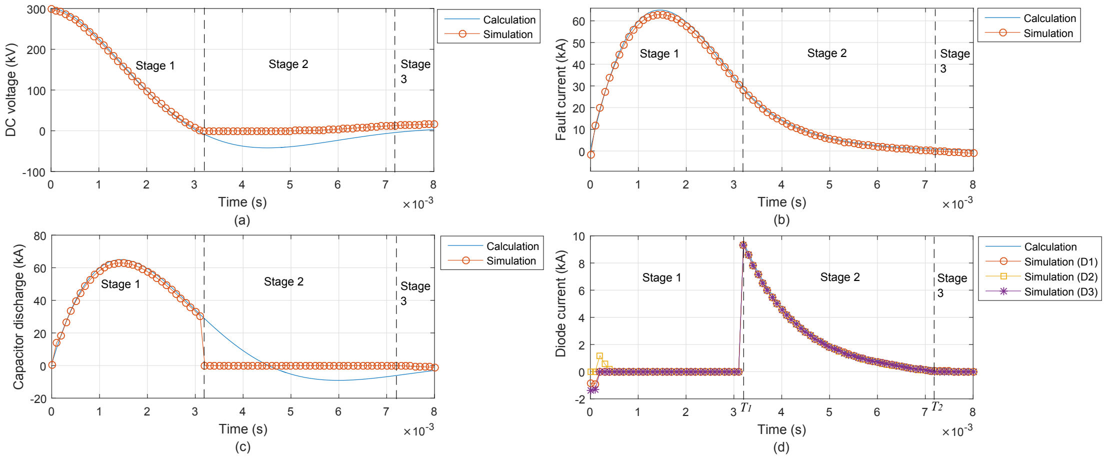


FIGURE 3.15: Analytical and simulation results for DC fault. (a) DC voltage (V_{dc2}); (b) Fault current (I_{dc21}); (c) DC-link capacitor discharge (I_{cap2}); (d) Diode current ($I_{D1,2,3}$).

current is at 30.54 kA. The upper-leg diodes ($D1, D2, D3$) have equal peak currents and the fault currents flowing through them decrease at the same rate. Due to absence of active AC source, the fault ends in Stage 3 in which the current completely becomes zero.

It is important to note that the freewheeling diodes have to tolerate very high current when Stage 2 starts. This evidently explains the vulnerability of VSC to DC fault. As the modeling of VSC is fundamentally identical with the half-bridge MMC, the same can be also said for latter case. It will be presented in Chapter 8 how the freewheeling phase can be overcome.

3.5 Summary

The modeling and control of voltage source converter (VSC) have been presented in this chapter. The derivation shows that the cross-coupling terms ($\omega L_{si} I_{ci,q}$ and $\omega L_{si} I_{ci,d}$) exist in d- and q-axis circuits, respectively. In order to achieve independent control of d- and q-axis currents (I_d and I_q), the cross-coupling terms can be compensated by using feedforward control. As a result, the I_d can be monitored to control DC voltage and active power, whereas I_q to control reactive power and AC voltage. The complete control structure is illustrated combining all the controller concerned in this chapter.

From the DC fault analysis, it is demonstrated that DC-link capacitor is the major contributor of fault current when the short circuit happens on the DC line. When the VSCs are blocked for protection purpose, the anti-parallel diodes begin to take charge of the current flow. In this stage, the current level may be so high that it results in damage of the diodes. Hence, it is evident that a fast fault detection algorithm is critical to minimize the negative impact of DC fault. The fault analysis is validated by simulation in PSCAD/EMTDC, with the result showing good agreement with analytical calculation.

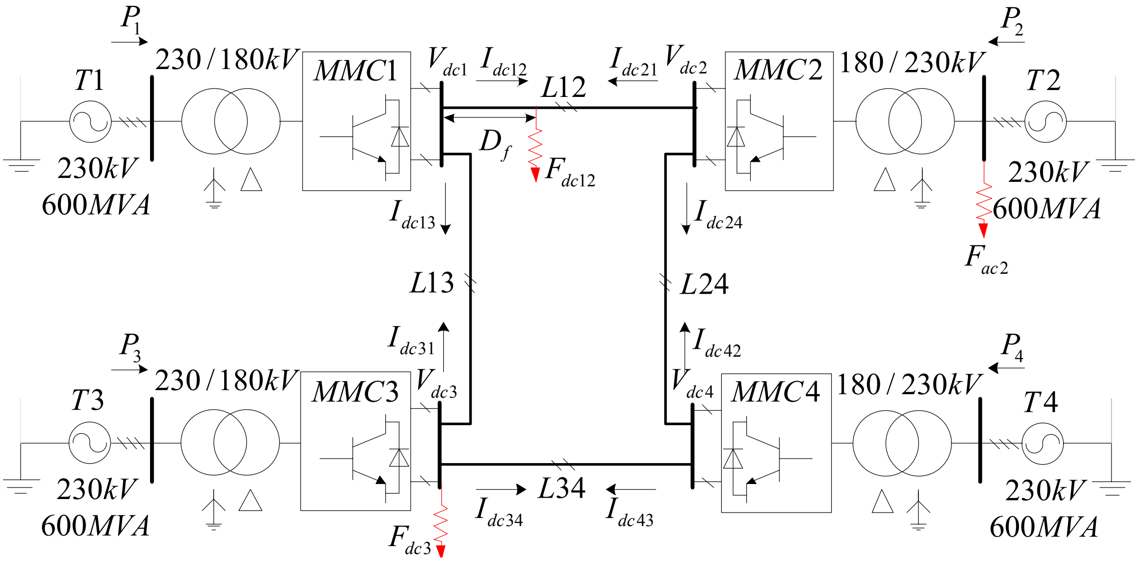
Chapter 4

Simulation and Experimental VSC-based DC Test System

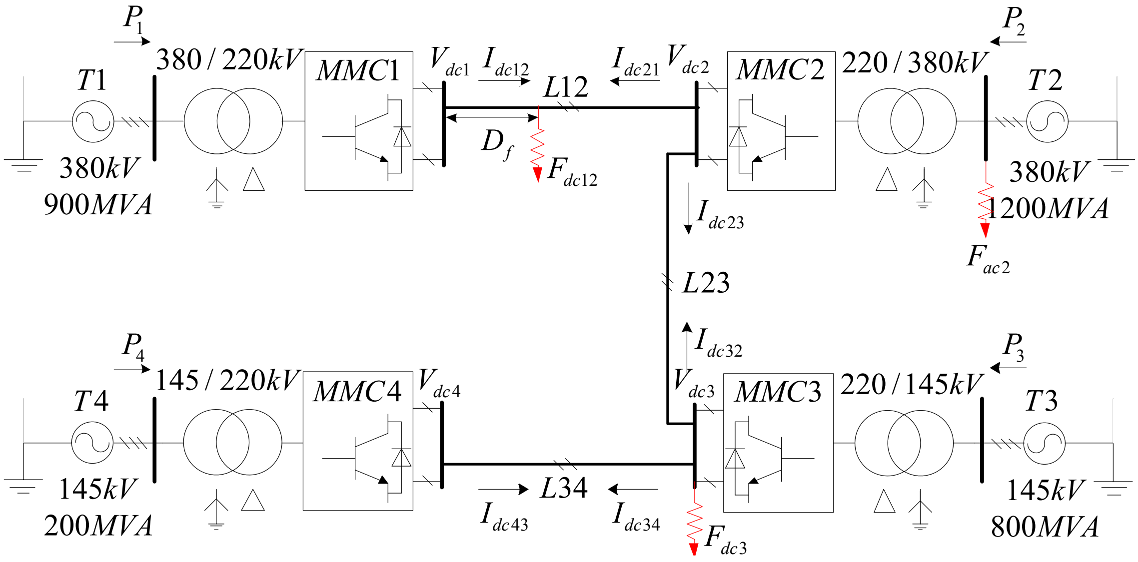
The existing research on fault detection in VSC-HVDC systems approaches performance validation mainly based on simulation-based fault signal. One of the reasons is that it is practically infeasible to create the short-circuit in real VSC-HVDC systems while it is on operation. There are some commercial laboratories with high-end equipment performing high voltage testing, KEMA for instance. However, from the standpoint of cost, it would not be justified to engage them just for research purposes. With advancement of computing technology, hardware-in-the-loop (HIL) simulation has become an increasingly popular way to design and test real-time protection algorithm. While it is a step closer to the real system, the DC fault is still performed under controlled environment.

This chapter aims to lay out the steps to create the VSC-based DC test system to validate the proposed fault detection methods. For simulation, a 4-terminal HVDC system is developed in PSCAD/EMTDC. The similar setup is difficult to be replicated in laboratory, therefore a scaled-down 2-terminal DC system is built instead. One of the important aspects of the experiment is protection as short-circuit is involved. Details regarding the converter rating and protective measure are given in this chapter.

4.1 Simulation Test Tystem



(A) Model 1.



(B) Model 2.

FIGURE 4.1: Multi-terminal HVDC systems simulated in PSCAD/EMTDC.

Table 4.1: System for simulation models

	Model 1	**Model 2**
AC frequency	60 Hz	
Number of submodules per arm, N	100	
Module capacitor	3000 μF	
Arm reactor	50 mH	
Switching frequency	180 Hz	
Line length (L12, L13, L24, L34)	100 km	200 km
DC voltage	300 kV	400 kV
Power flow	P2 = -350 MW P3 = 400 MW P4 = -300 MW	P2 = -800 MW P3 = 500 MW P4 = -99 MW

Fig. 4.1 shows the multi-terminal Modular Multilevel Converter (MMC)-based HVDC system of 4 symmetric monopole terminals modelled in PSCAD/EMTDC. Both models will be used to simulate DC and AC faults, as indicated in the same figures, for the study of this thesis.

Model 1 is symmetrical in a sense that all the AC systems are identical in terms of AC voltage and size. Model 2, on the contrary, is of structure similar to CIGRE DC Grid Test System [75] and has rather diverse AC systems, consisting of onshore ($T1$&$T2$) and offshore ($T3$&$T4$) terminals. In both models, the master-slave control is adopted, whereby $MMC1$ functions as the fixed DC voltage control and the rest as fixed active power control. More details about the system parameters are listed in Table 4.1.

4.1.1 AC System

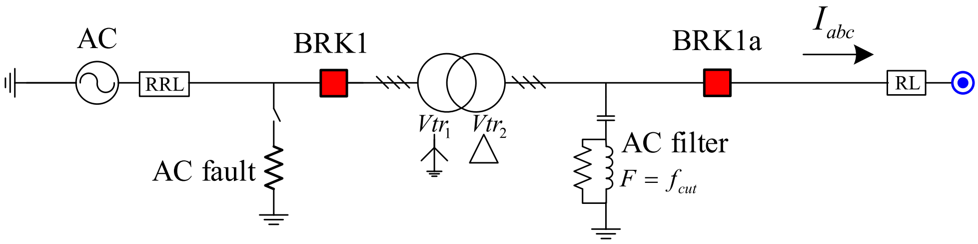


Figure 4.2: AC system modeled in PSCAD/EMTDC.

Fig. 4.2 illustrates the modeling of AC system in PSCAD/EMTDC.

TABLE 4.2: Short circuit ratio for AC systems in Model 1 and 2.

	Model 1	**Model 2**
T1	10.11	28.27
T2	10.11	21.2
T3	10.11	3.98
T4	10.11	11.64

The three-phase AC voltage source is represented by the component available in PSCAD library. The short circuit ratio (SCR), which measure the strength of AC system at the HVDC converter station, is defined in (4.1).

$$SCR = \frac{S_{ac}}{P_{dc}} = \frac{V_s^2}{P_{dc}} \frac{1}{Z_s}. \tag{4.1}$$

If V_s and P_{dc} are set as base for AC voltage and DC power, respectively, SCR can be reduced to:

$$\overline{SCR} = \frac{1}{\overline{Z_s}}, \tag{4.2}$$

where $\overline{Z_s}$ is the source impedance in per unit. The SCR for each AC system in Model 1 and 2 is given in Table 4.2. According to Gavrilovic [76], the system with SCR less than 3 is considered weak, which means it has a low short circuit capacity.

4.1.2 Converter

The MMC (see Fig. 4.3) in the simulated system adopts the detailed equivalent modeling (DEM) [77, 78]. The model not only is computationally efficient, but also offers a high degree of accuracy in reference to the detailed model. The component is readily provided in PSCAD library, depicted in Fig. 4.3. Each phase-arm is made up of $N = 100$ submodules (SM), accompanied with arm inductors denoted as $Larm$.

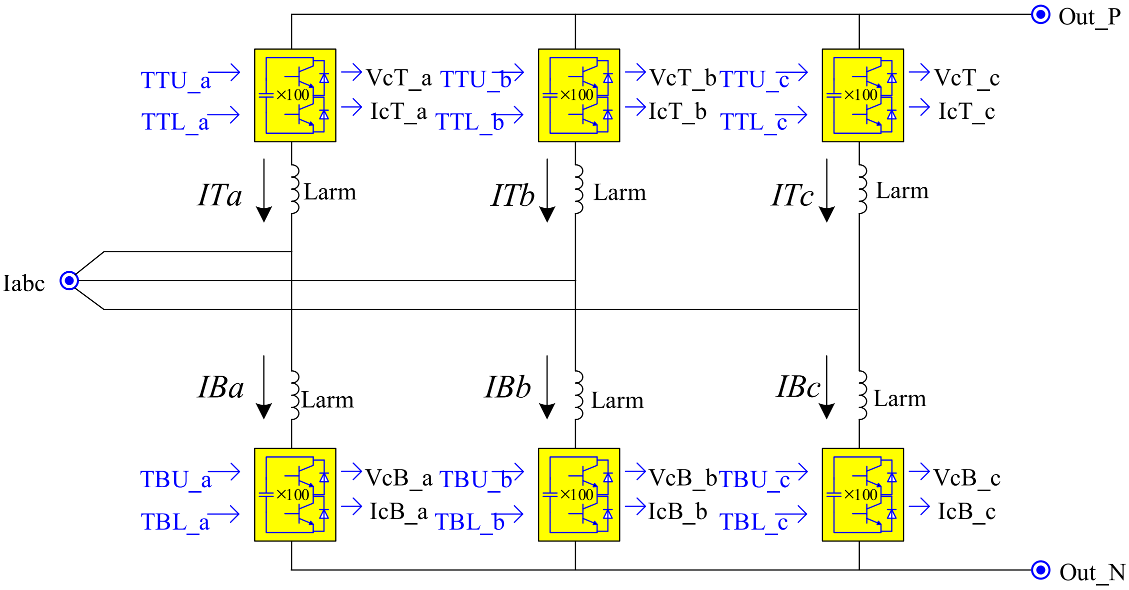


FIGURE 4.3: Three-phase MMC modeled in PSCAD/EMTDC.

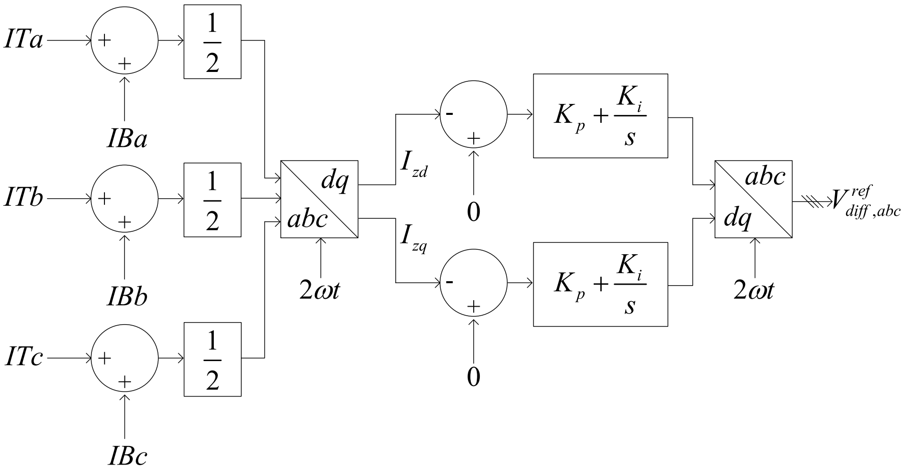


FIGURE 4.4: Control structure of circulating current suppressing controller.

The inner unbalance voltage within a phase can cause circulating current. It is shown mathematically that the current is of twice fundamental frequency and negative sequence [79]. The second harmonic effectively increases the arm current, resulting in higher converter loss. Therefore, it is important to improve the control structure by adding a controller that regulates the inner unbalance voltage, for which the Circulating Current Supressing Controller (CCSC) [80] has been proposed. As shown in Fig. 4.4, control signals $V^{ref}_{diff,abc}$ will be obtained, and they are added to the control signals generated by the inner controller for each phase before sending to SPWM.

It is also critical to ensure that the capacitor voltages at all SM are balanced throughout operation. Such commitment can be fulfilled by monitoring the SM capacitor voltage (V_c) and current (I_c). With this information, a method known as Balancing Control Algorithm (BCA) will sort the SM based on capacitor voltage at any instant [81]. For example, if the current is positive, the SM with the lowest capacitor voltages will be switched on. Consequently, the capacitors will be charged and their voltages increase. The switching signals targeted for top and bottom MMCs are TTU_i and TTB_i (i=a, b, c), respectively (see Fig. 4.3).

The DC-link capacitor is not required in most instances of MMC-HVDC systems, because the SM capacitors should suffice to maintain the voltage across DC bus. However, some literatures [82–85] use the DC-link capacitor to provide earth reference and added boost for better voltage quality. The DC-link capacitor has to be smaller than the SM capacitor in order to prevent large current contribution during DC fault.

4.1.3 Inductive fault current limiter

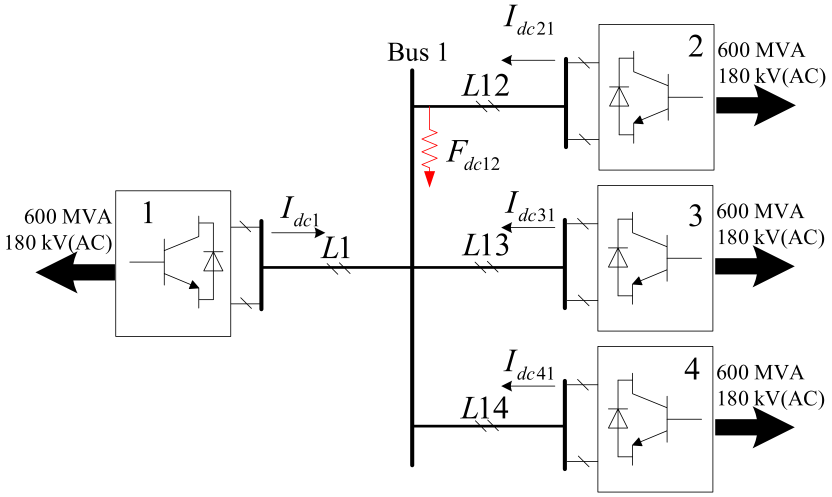


FIGURE 4.5: Radial multi-terminal HVDC system.

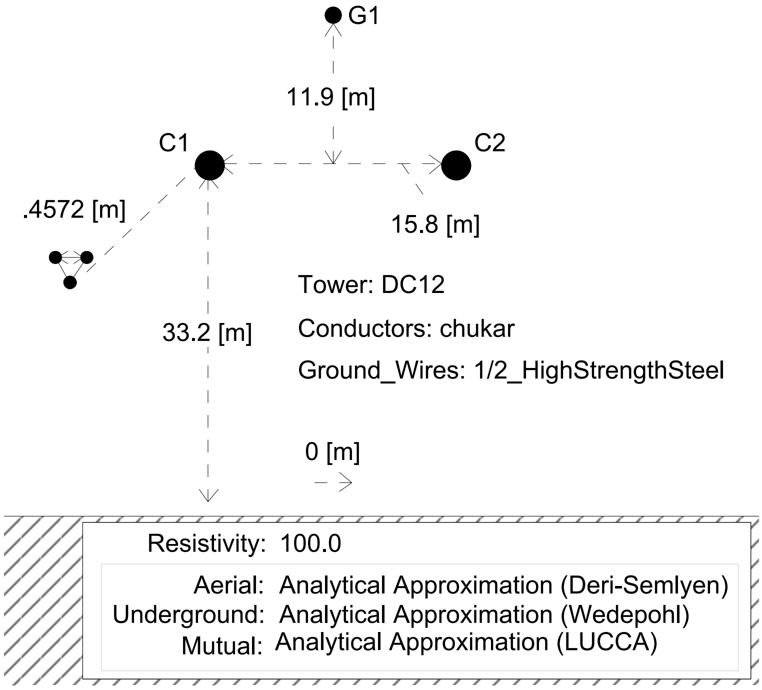
Consider a fault scenario in radial DC network as shown in Fig. 4.5, with rating similar to Model 1. DC fault F_{dc12} happens almost at the line termination of *L12*, near Bus 1. In this case, the responsibility of detecting the fault should lie on Terminal 2. However, there is no electrical difference as seen from Terminal 1, 3 and 4 (100 km away) as the fault is very close to the same bus which they are connected to. As a result, it will pose a challenge to identify the fault location merely relying on local measurement. In order to provide selectivity under this challenging condition, inductive fault current limiter (FCL) can be introduced at both ends of transmission line to impose “electrical distance”.

The size of the inductive FCL has to be selected based on the requirement of DC circuit breaker. For example, the ABB's DC circuit breaker is able to tolerate maximum current of 16 kA. Assume the operating time to be set as 2 ms, the rated current derivative is 8 kA/ms [86]. Hence, the minimum size of inductive FCL, which can be calculated as such:

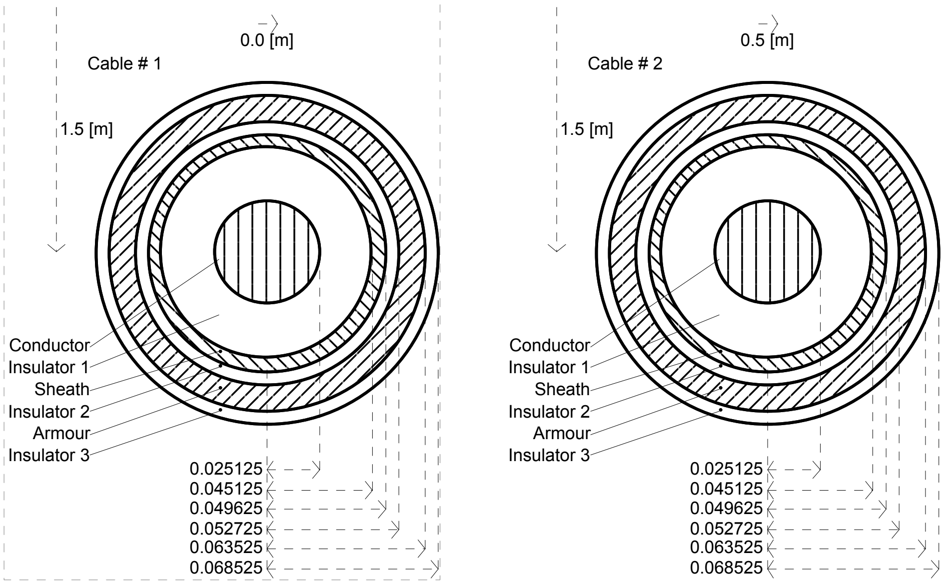
$$\begin{aligned} \frac{\mathrm{d}I_{dc}}{\mathrm{d}t} &= V_{dc}/L_{FCL}, \\ L_{FCL} &= \frac{300kV}{8kA/ms} = 37.5mH. \end{aligned} \tag{4.3}$$

4.1.4 DC Line

The DC lines in the simulated system are provided by the detailed, frequency-dependent model readily available in PSCAD library. There are two types of DC line: overhead line (OHL) and underground cable, which make up all the DC lines in Model 1 and 2, respectively. Their properties are shown in Fig. 4.6



(A) OHL model.



(B) Cable model.

Figure 4.6: Properties of DC lines used in simulation.

The line parameters of the OHL and cable can be calculated by the PSCAD Line Constant Program and are listed in Table 4.3. One can clearly notice the cable has higher capacitance. That is due to the XLPE insulation in the cable, whereas the insulation in the OHL is mostly air.

TABLE 4.3: Properties of overhead line and cable modeled in PSCAD/EMTDC.

	OHL	**Cable**
$R(\Omega/km)$	0.1061×10^{-7}	0.1109×10^{-7}
$L(\Omega/km)$	0.1761×10^{-10}	0.114×10^{-9}
$G(S/km)$	0.1×10^{-13}	0.1×10^{-11}
$C(S/km)$	0.6986×10^{-16}	0.1373×10^{-14}

4.1.5 Simulation Result

The DC and AC faults in Model 1 are simulated, and the results are presented here. The fault isolation will not be implemented just yet as the goal here is to offer readers some ideas of different signatures that appear in system parameters. However, the converter blocking mechanism will be activated by MMC terminal when the measured DC current crosses 2 per unit (p.u.) [61, 74].

It will be excessive to present all the parameters in four-terminal HVDC system. Therefore, only the critical ones are shown here: DC currents, DC voltages, and active powers, measured at each MMC terminals.

4.1.5.1 Fault on DC Line

Since the PP fault is the most severe and representative of DC fault [87], PG fault will not be discussed here.

F_{dc12} is the PP fault with 0.1 Ω occurring in the middle of $L12$. The system is started and runs until it has achieved steady state, whereby the DC voltage ramps up to 300 kV and each MMC terminals meet their respective active power demand. At 2.75 s, F_{dc12} is triggered. The MMC is blocked when the DC current rises above 4 kA, leaving

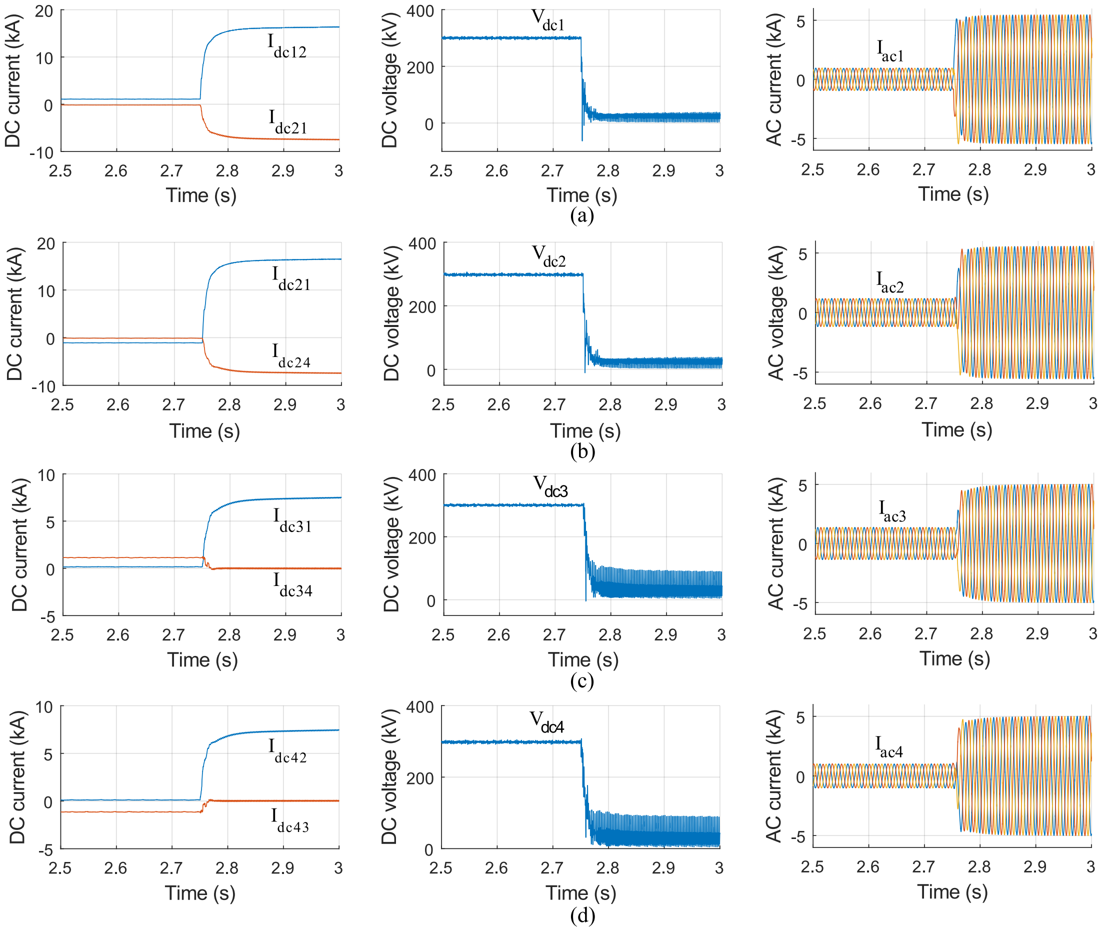


FIGURE 4.7: Simulation result for PP fault. Measurement obtained from (a) $MMC1$, (b) $MMC2$, (c) $MMC3$ and (d) $MMC4$.

the anti-parallel diodes to operate as uncontrolled rectifier. The transition from steady state to fault is shown in Fig. 4.7.

DC current: It is clear that the DC fault results in increasing DC currents in all DC lines. Most of the DC currents are continuing in the same direction, while I_{dc24} is flowing in opposite direction towards fault point. In addition, $MMC3$ and $MMC4$ deliver the currents following the shortest path, without passing through $L34$, which explains why I_{dc34} and I_{dc34} are zero after the fault.

DC voltage: The DC voltages at each MMC terminal drops to zero instantaneously as a result of DC fault. The time it takes for the DC voltage to reach zero depends on the distance between the terminal and fault point; it is seen that $MMC3$ and $MMC4$

record zero DC voltage slightly later than other terminals. Now, the charges from DC-link capacitors are depleted and the AC source begins to feed current through three-phase diode bridge into fault point. Hence, it can be seen that the DC voltage is oscillating at six times the system frequency.

AC current: The AC terminals reacts to large voltage drop after the DC voltage reaches zero by generating higher AC current, which eventually adds to the DC fault current. The vulnerability of freewheeling diode to DC fault is evident here as the AC current is now too large exceeding the thermal capability (I^2t) of diode.

4.1.5.2 Fault on AC Terminal

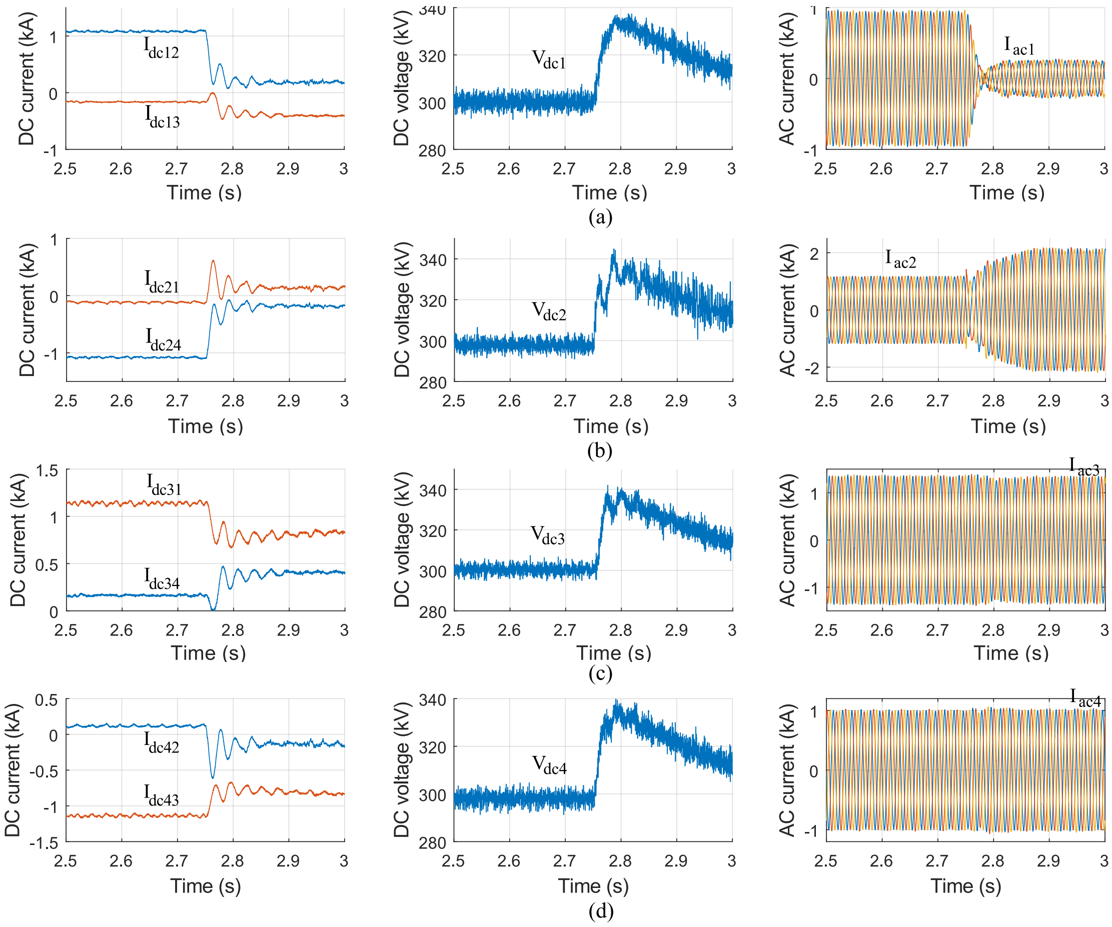


FIGURE 4.8: Simulation result for AC fault. Measurement obtained from (a) $MMC1$, (b) $MMC2$, (c) $MMC3$ and (d) $MMC4$.

In general, AC faults can be divided into four types: Single-phase-to-ground, two-phase-to-ground, three-phase-to-ground and phase-to-phase. Only three-phase-to-ground fault is studied here as it is known to be the most severe among the AC faults. F_{ac2} is created at terminal 2 at 2.75 s. The result is shown Fig. 4.8.

DC current: Fault at Terminal 2 essentially isolates the terminal from the rest of the system, hence the DC currents are flowing within the system bypassing the terminal. The transient on DC currents is caused by transition to new steady state. Due to the loss of Terminal 2, the total power demand in the system has dropped. Therefore, some DC currents appear to decrease.

DC voltage: In an effort to meet new power demand, Terminal 1, as a slack terminal, has to readjust its power output. Consequently, the DC voltage experiences some transients while moving to new steady state. The increase of DC voltage is caused by drop in total power demand; if power generation terminal, $MMC3$ for example, is lost, one will see dip of DC voltage instead.

AC current: It is clear that the I_{ac2} shows significant increase as a result of F_{ac2}. The drop of I_{ac1}, again, infers readjustment of power generation by $MMC1$ after the fault. I_{ac3} and I_{ac4} seem to be unaffected implying that their power outputs are still fulfilled.

4.2 Experimental Test System

Laboratory-scale DC grid experimental setup is developed to carry out steady-state, load change and DC fault studies. This setup aims to replicate the actual DC grid system operation at scaled-down voltage level. The test system is made up of asymmetric monopolar configuration, with its schematic block diagram shown in Fig. 4.9.

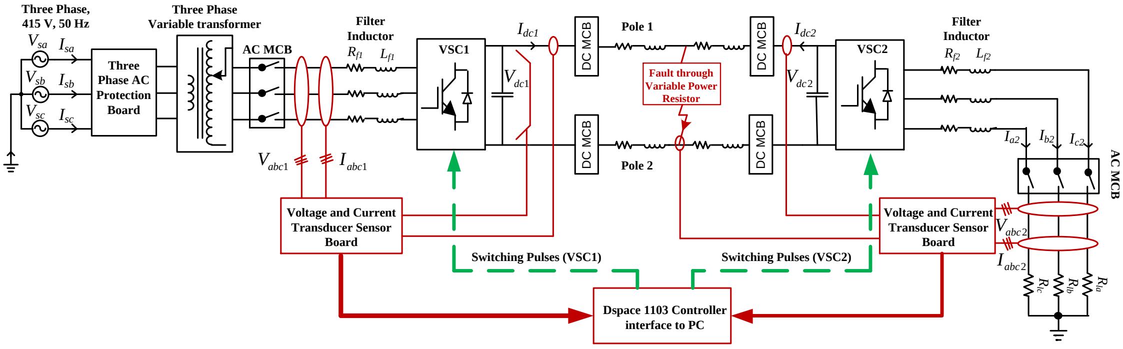


FIGURE 4.9: Schematic diagram of VSC based DC system experimental circuit.

The primary challenge of building this setup is choosing the right voltage level. As the three-phase AC source is supplied from the laboratory, it is important to ensure that the artificial short circuit in the experimental setup should be tolerated and not cause nuisance trip of upstream module case circuit breaker (MCCB). The AC source supply available in laboratory is 415 V, 50 Hz. To operate the experiment at this voltage level carries significant risk to user and high likelihood of main breaker tripping. The model is firstly simulated in MATLAB to have better understanding of the relationship between operating voltage and fault current. It is found that 85 V (line rms) is suitable for this experiment to be carried out in safe manner.

Pole-to-ground and AC faults are dangerous to be performed in this experimental setup. Both faults require direct short-circuiting to ground. It is found that the currents induced by these faults will trigger tripping of earth leakage circuit breaker (ELCB) in the laboratory. Therefore, they will be only covered in PSCAD/EMTDC simulation.

The real experimental setup is presented in Fig. 4.10. The corresponding parameters and ratings are given in Table. 4.4.

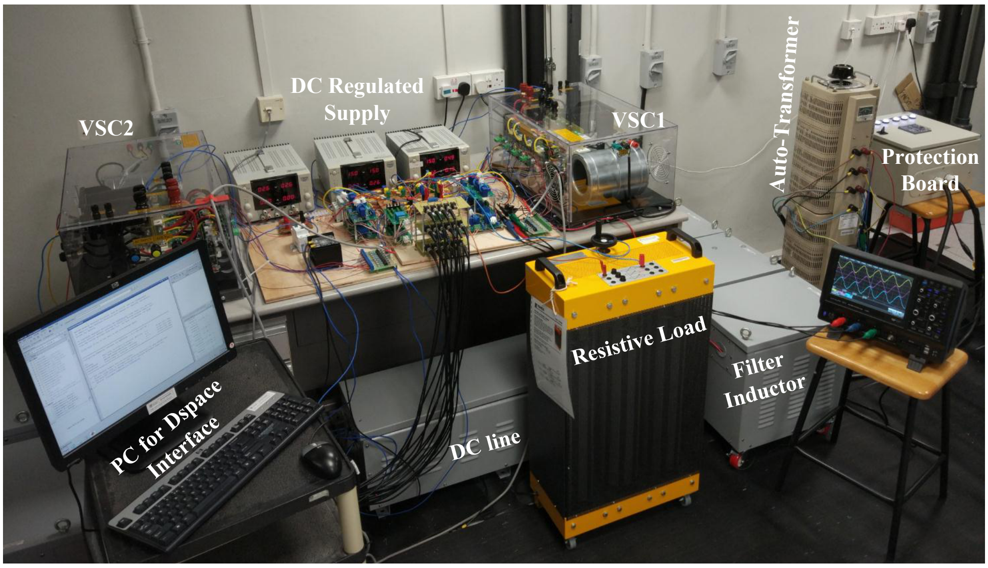


FIGURE 4.10: Laboratory experimental setup.

TABLE 4.4: Experimental setup parameters

Elements	**Values**
Supply voltage	3ϕ, 85 V Line rms , 50 Hz
3ϕ AC Protection Board	40 A, TP MCCB with Shunt trip
3ϕ Variable Transformer	30 kVA, (0-415) V
Converters (VSC1, VSC2)	30 kVA, 415 V
DC Capacitor	$C_{dc} = 2350\ \mu F$,
DC Line Paramters	$L_{dc} = 1.5\ mH$,$R_{dc} = 0.5\ \Omega$
DC MCB	C60H-DC, C 4A
Interface Filter Parameters	$R_f = 0.1\ \Omega$, $L_f = 10\ mH$
Linear Load	$R_{la} = R_{lb} = R_{lc} = 22\ \Omega$
Variable Power Resistor	5000 W, (1-16) Ω
DC Solid State Relay	D2D40, 200 V, 40 A

4.2.1 Converter

Fig. 4.11 shows the three-phase converter module ($VSC1$ and $VSC2$) used in the experimental setup. The module consists of two-level VSC, rated at 30 kVA, 415 V (3ϕ). The IGBT device allows maximum switching frequency up to 15 kHz. $VSC1$ is assigned to control the DC voltage of the system while $VSC2$ maintains the AC voltage at its terminal to ensure continuous load current. The components in the VSC are listed below:

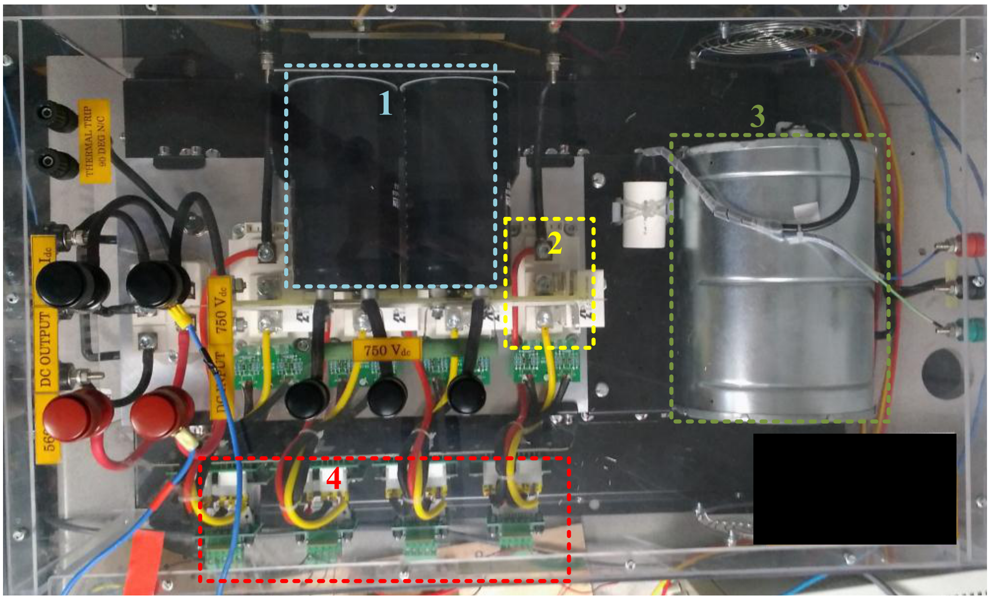


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FIGURE 4.11: Three-phase VSC module.

1. DC-link capacitor: A pair of capacitors, rated at 4700 μF, are connected in series across DC-link. Mid-point grounding is optional and a terminal is provided for that.
2. IGBT module: The solid state switch is able to support operation of 415 V(ac), 750 V(dc) and 50 A. The switching can go up to 15 kHz. There are four modules mounted on heat sink.
3. Fan: Provides added cooling to the switches during operation.
4. Gate driver: Controls the switches' dynamic behaviour and monitors short circuit protection.

4.2.2 Tuning of Controller

The inner current controller is tuned according to following parameters:

- K_{pc}=50

- T_{ic}=0.1

The frequency response of $G_{c,OL}$ is presented in Fig. 4.12, showing that this setting gives stable operation with phase margin of 65.5° and infinity gain margin.

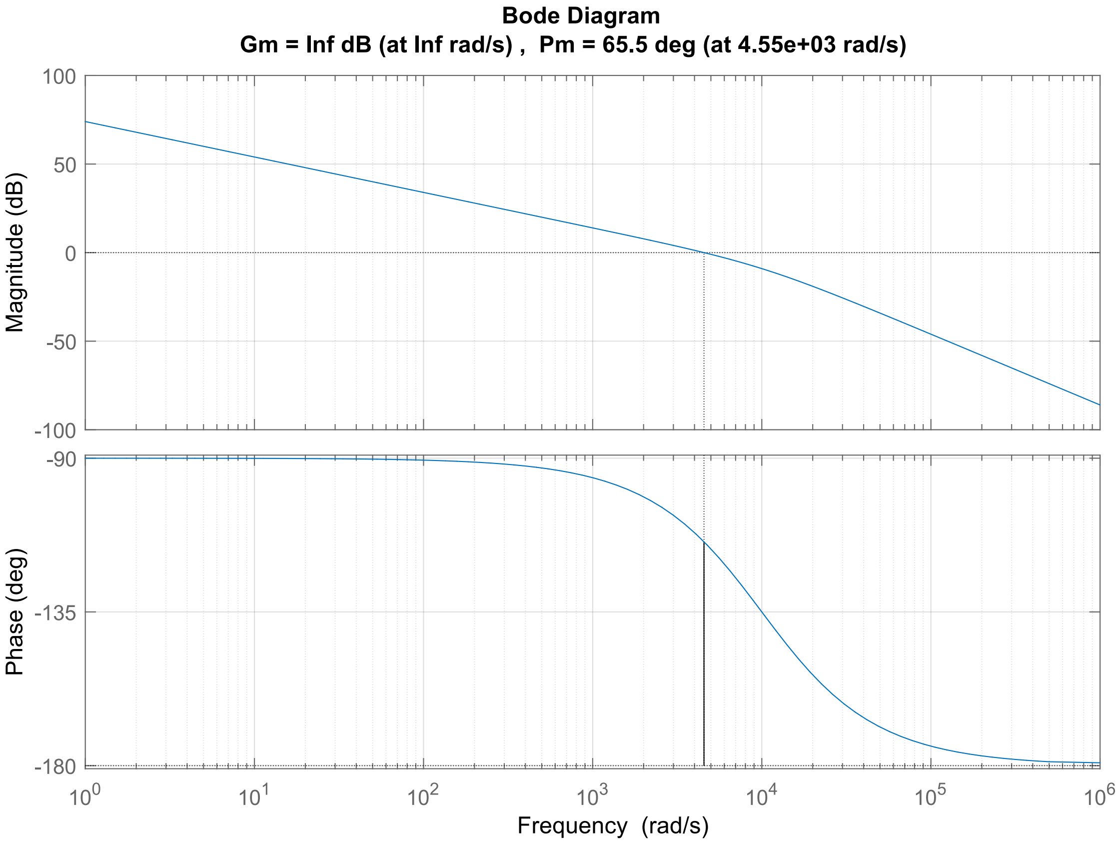


FIGURE 4.12: Open loop frequency response of inner current controller.

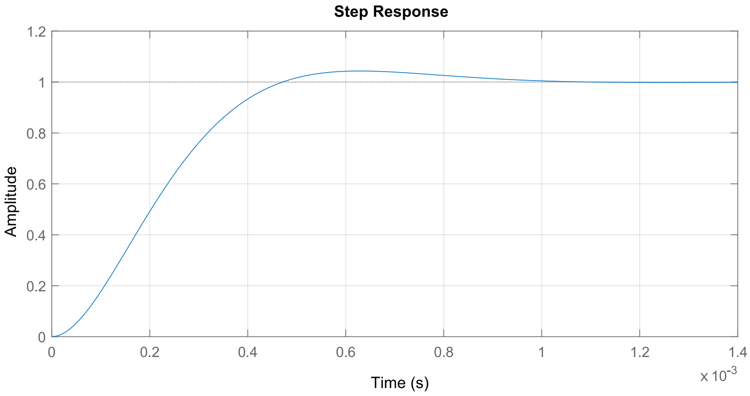


FIGURE 4.13: Step response of inner current controller.

The step response plot of inner current controller is shown in Fig. 4.13. Some characteristics about the plot can be laid out as follows.

- Rise time: 0.304 ms
- Settling time: 0.843 ms
- Overshoot: 4.3210 %
- Peak: 1.0432
- Peak time: 0.626 ms

As for DC voltage controller, the value a is chosen to be 10. The PI parameters are given as follows.

- K_{pv}=3320.3
- T_{iv}=0.0032

The frequency response of DC voltage controller shown in Fig. 4.14 indicates that the close loop dynamic is stable, with phase margin of 58.6° at 2130 rad/s (or 339 Hz).

The close loop transfer function has the step-response shown in Fig. 4.15 and following characteristics:

- Rise time: 5.709 ms
- Settling time: 0.0064 s
- Overshoot: 15.9872 %
- Peak: 1.1599
- Peak time: 0.0014 s

The calculation of PI parameters can be referred to the MATLAB code given in Appendix B.

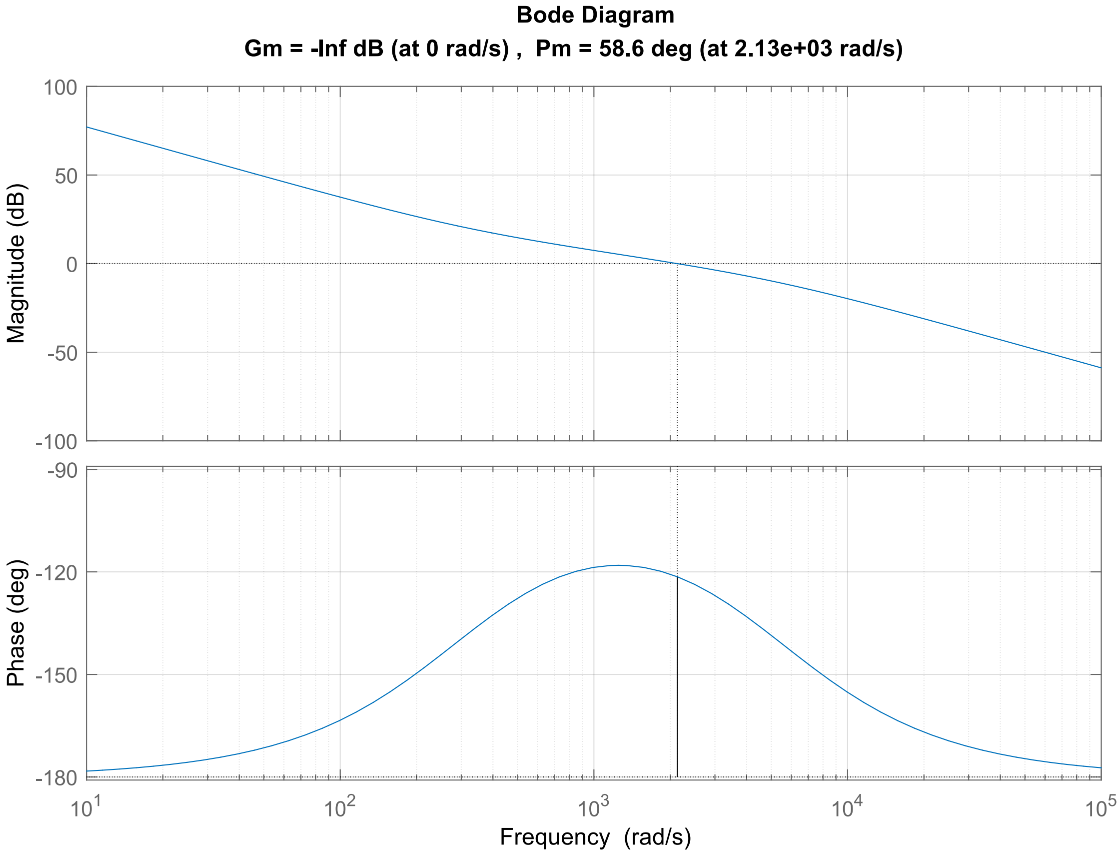


FIGURE 4.14: Open loop frequency response of DC voltage controller.

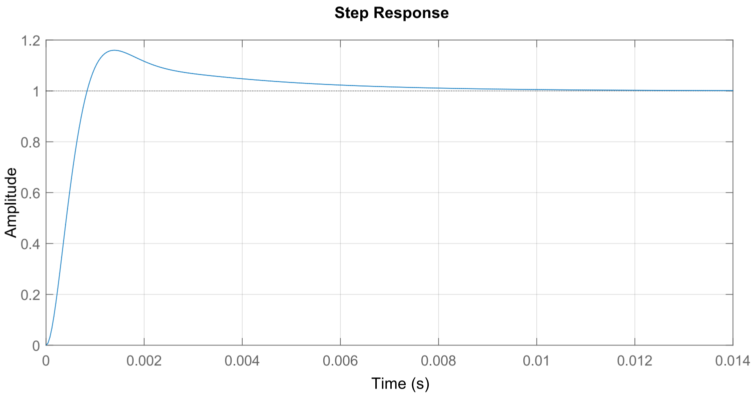


FIGURE 4.15: Step response of DC voltage controller.

4.2.3 DC Line

The DC line in the experimental setup is represented by π-equivalent model which consists of inductors and resistors (see Fig. 4.16). The inductors denoted by 1 and 2 make up the positive pole of the DC line whereas 3 and 4 for negative pole. The line

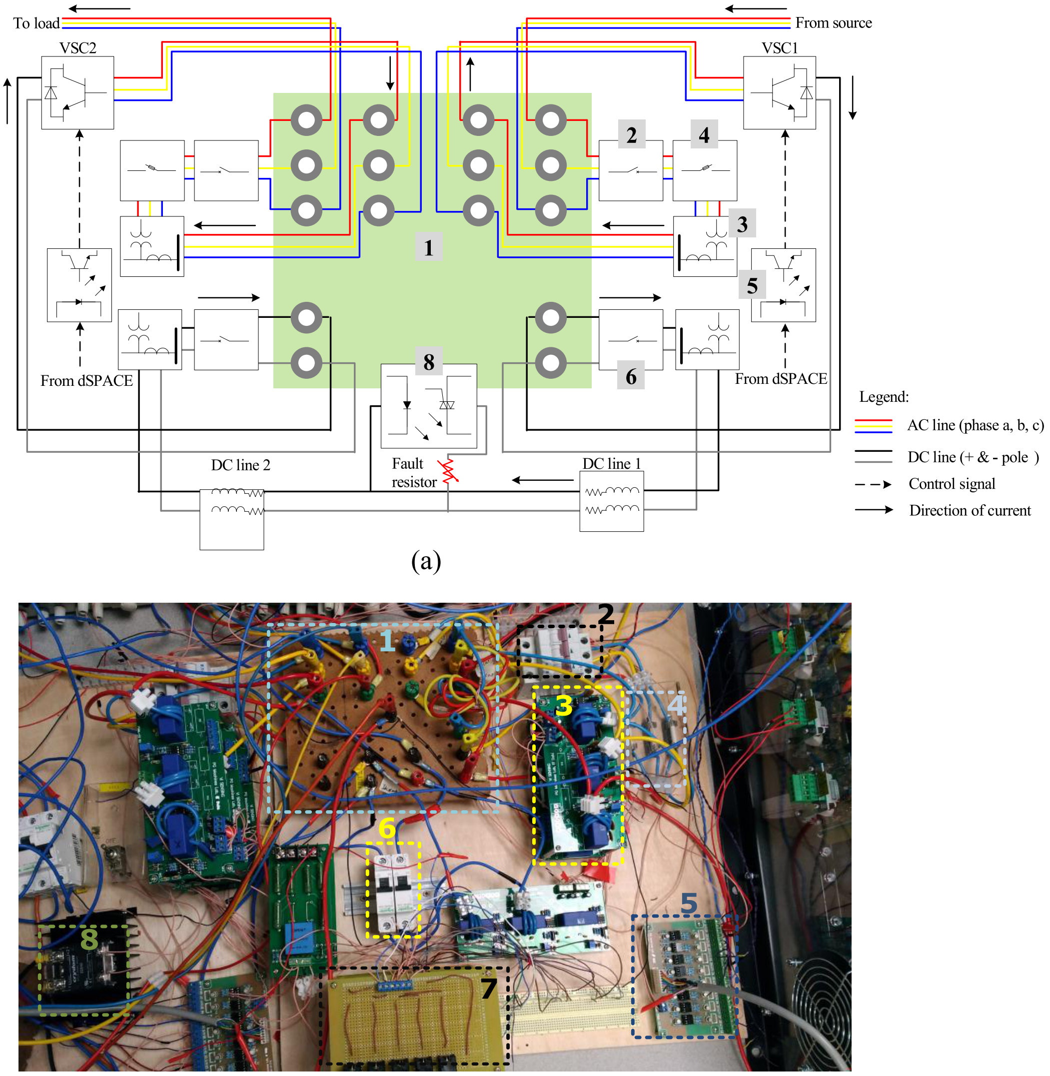
FIGURE 4.16: π-equivalent DC line.

distance can be changed by selecting one of the three inductance values available here: $1.5mH$, $2.8mH$ and $4.0mH$. With this, variation of DC fault location can be emulated.

4.2.4 Measurement and Control

The measurement and control are centralized at the same place, which is illustrated in Fig. 4.17.

1. Measurement terminus: All the connections have to terminate here before they branch out to next components. The measurements of AC voltage, AC current, DC voltage and DC currents required for control system are sourced from here.
2. AC miniature circuit breaker: Provides ease for user to isolate or connect the AC source when needed. Because the rating is intentionally chosen lower than MCCB board, it offers primary protection and faster tripping.
3. Voltage and current sensors: Measures the voltage and current from the system and converts them into signal required by control system. The schematic diagram is given in Appendix C.



(a)

(b)

Figure 4.17: Central measurement and control of VSC. (a) Schematic diagram and (b) Actual setup.

4. Fuse: Breaks the circuit instantaneously when blown by current exceeding its rating.

5. Opto-coupler gate driver circuit: Increases the voltage level of switching signal to 0/15 V before fetching it to driver circuit of converter module. The schematic diagram is given in Appendix D.

6. DC miniature circuit breaker: Schneider C60H-DC is used to protect the costly devices such as converter module and DC line inductor. It trips when the short

circuit results in current exceeding its rating (28A).

7. Signal-to-dSpace interface: Fetches the measurement signal to dSpace through TNC connector.

8. DC solid state relay: The short circuit across DC line is done by using the relay, which is operated by providing small voltage input externally. This is to prevent user from potential, direct exposure to large current caused by short circuit. The relay is able to support up to 400 V, 40 A during steady state.

4.2.5 Protection

Sufficient degree of protection is critical in order to guarantee safety of user and avoid unnecessary tripping of main breaker in laboratory. There are three levels of protection in place, as listed in Table 4.5. Primary protection is meant to take action first, followed by secondary, and lastly tertiary. To achieve this, the circuit breaker rating has to be chosen carefully so that it does not contradict next level of protection down the hierarchy.

1. Primary protection: The DC MCBs are placed at both ends of DC line. They are rated at 4 A and will trigger magnetic tripping when the current is 7 to 10 times the rating [88], with breaking time less than 10 ms. The fuses, rated at 15 A, are inserted before the filter inductor.

2. Secondary protection: The protection board consists of three-phase 40 A molded case circuit breaker (MCCB) and 40 A residual current circuit breaker (RCCB). The MCCB is required to protect the converter modules which are rated at 50 A. When the input current reaches 40 A or higher, it will trip within 30 ms. The RCCB trips against leakage current due to unbalance of three-phase currents.

TABLE 4.5: Hierarchy of protection system in experiment.

Primary protection	 DC MCB Characteristic C 250 V, 4 A	 Fuse Fast acting 15 A
Secondary protection		MCCB 40 A RCCB 40A
Tertiary protection		MCCB 100 A

3. Tertiary protection: The large MCCB is pre-installed in the laboratory and should only serve as last resort when primary and secondary protections fail. In any case, nuisance tripping of this MCCB as a result of artificial short circuit created in the experimental setup is highly undesirable.

The short circuit is created across positive and negative DC lines through a power resistor. Fig. 4.18 shows the adjustable load resistor box, rated at 5000 W, with resistance ranging 1-16 Ω. During steady state, the power resistor is disconnected. As the system is ready for short circuit, the DC solid state relay will be externally switched on providing an electrical path to the resistor load.

For safety reason, the faults involving short circuit to ground, such as AC fault and

FIGURE 4.18: Adjustable load resistor box.

pole-to-ground, are infeasible to be carried out experimentally. The current flowing into ground can be large enough to trigger the tripping of earth link circuit breaker (ELCB) installed in the laboratory and cause interruption to other lab users. Hence, both faults will be only simulated in PSCAD/EMTDC.

4.2.6 Experimental Result

4.2.6.1 Steady State

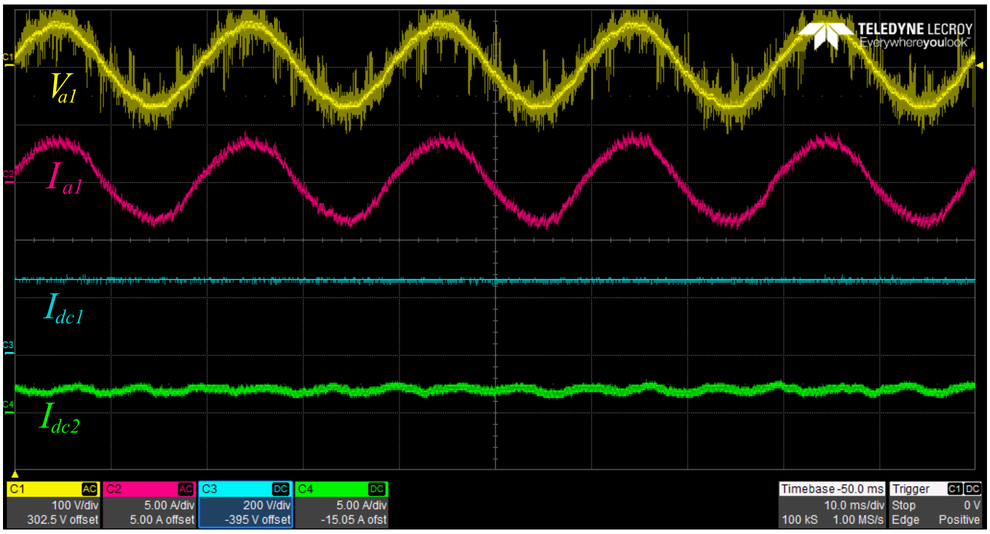


FIGURE 4.19: Experiment under steady state.

The experiment under steady state is shown in Fig. 4.19. Phase-a, V_{a1}, I_{a1}, V_{dc1} (maintained at 250 V) and I_{dc1} are shown in Fig. 4.19. Overall, the control structure is able to function normally.

4.2.6.2 Fault on DC Line

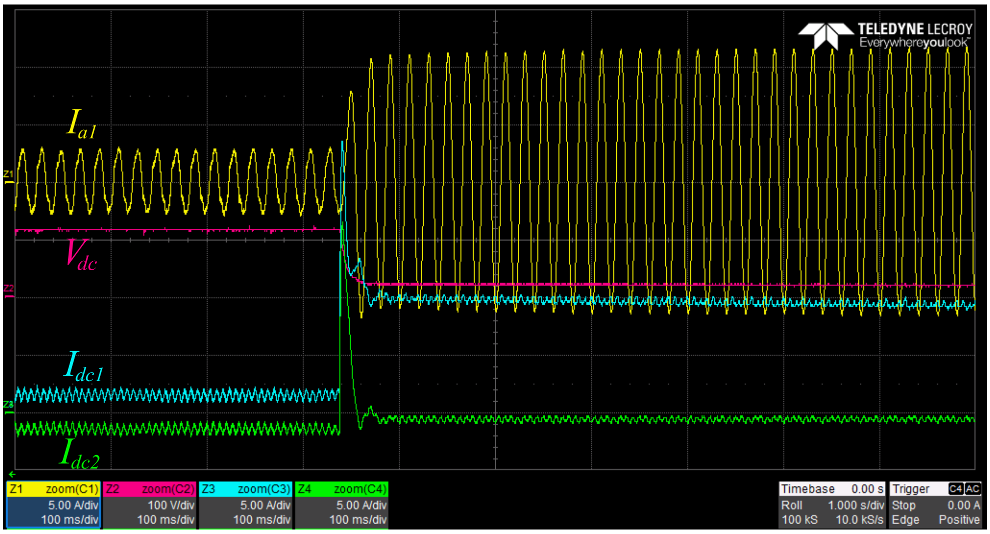


FIGURE 4.20: Experimental result for PP fault.

PP fault is created through power resistor, R_{f1} (2 Ω), with V_{a2} at 45 V and V_{dc1} maintained at 120 V. The location of the fault is in the middle of the DC line ($L_{dc1}, L_{dc2}, L_{dc3}, L_{dc4}=$ 1.5 mH, $R_{dc1}, R_{dc2}, R_{dc3}, R_{dc4}=$ 0.5 Ω). Likewise, the fault clearance is not implemented in this experiment. The results are shown in Fig. 4.20.

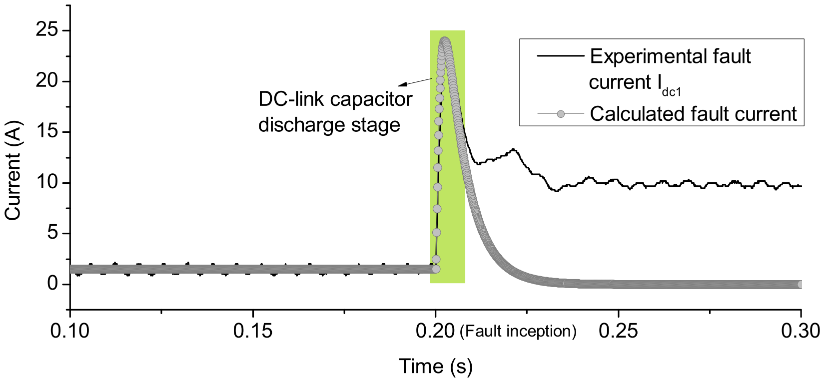


FIGURE 4.21: Comparison between experimental fault current and analytical calculation.

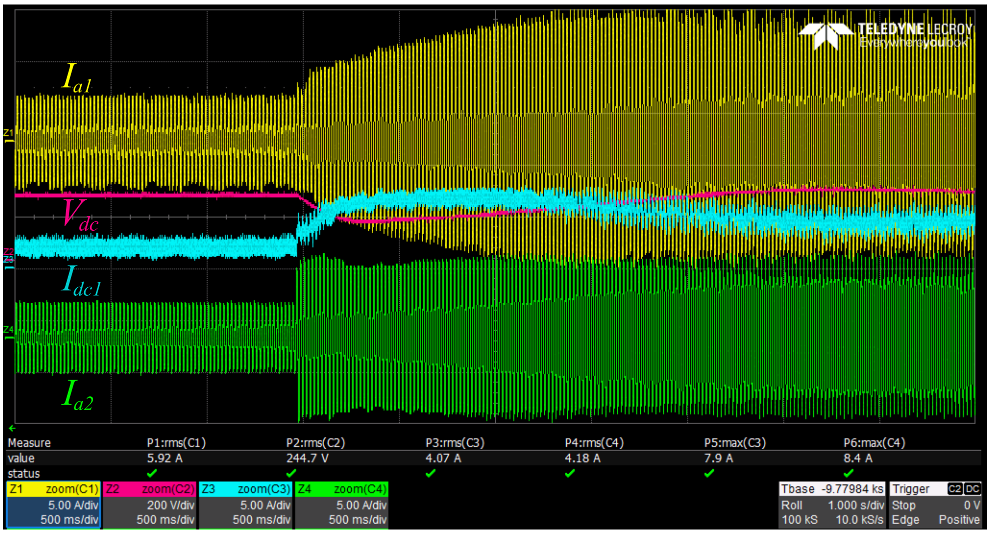
DC current: During steady state, I_{dc1} is 1.5 A, as well as I_{dc2} but negative. The PP fault causes the DC currents to increase to 23.5 A. As the VSCs are not blocked, the AC source continues to supply current into DC line. After the charges of DC-link capacitor in $VSC2$ are depleted, I_{dc2} drops to zero due to absence of AC source at $T2$.

I_{dc1} from experiment is validated with the analytical calculation from (3.37) and the result is given in Fig. 4.21. The analytical solution yields 24.01 A peak. With the good agreement between the two results, it is now evident that the DC-link capacitor discharge dominates the first few time-instants of the fault current.

DC voltage: Starting at 120 V, the DC voltage decreases sharply as a result of PP fault signifying discharging process of the DC-link capacitor.

AC current: I_{a1} begins to dominate the fault current after the DC-link capacitor is fully discharged. The AC source injects current with peak at 13 A flowing through the VSC to the fault resistor.

4.2.6.3 Load Change



Measure	P1:rms(C1)	P2:rms(C2)	P3:rms(C3)	P4:rms(C4)	P5:max(C3)	P6:max(C4)
value	5.92 A	244.7 V	4.07 A	4.18 A	7.9 A	8.4 A
status	✓	✓	✓	✓	✓	✓

Z1 zoom(C1)	Z2 zoom(C2)	Z3 zoom(C3)	Z4 zoom(C4)
5.00 A/div	200 V/div	5.00 A/div	5.00 A/div
500 ms/div	500 ms/div	500 ms/div	500 ms/div

Tbase	-9.77984 ks	Trigger	C2 DC
Roll	1.000 s/div	Stop	0 V
100 kS	10.0 kS/s	Edge	Positive

FIGURE 4.22: Experimental result for load change.

The load, R_{labc}, at $T2$ is varied from 22 Ω to 8.5 Ω and the transients experienced by I_{a1}, V_{dc1}, I_{dc1} and I_{a2} are shown in Fig. 4.22.

DC current: I_{dc1} sees a transient amounting to 7 A peak before it settles down to a new magnitude. Compared to DC fault, it is obvious that the rate of change is relatively lower. This characteristic can be exploited to differentiate the DC fault against the load change, albeit both cases have DC current increase as end result.

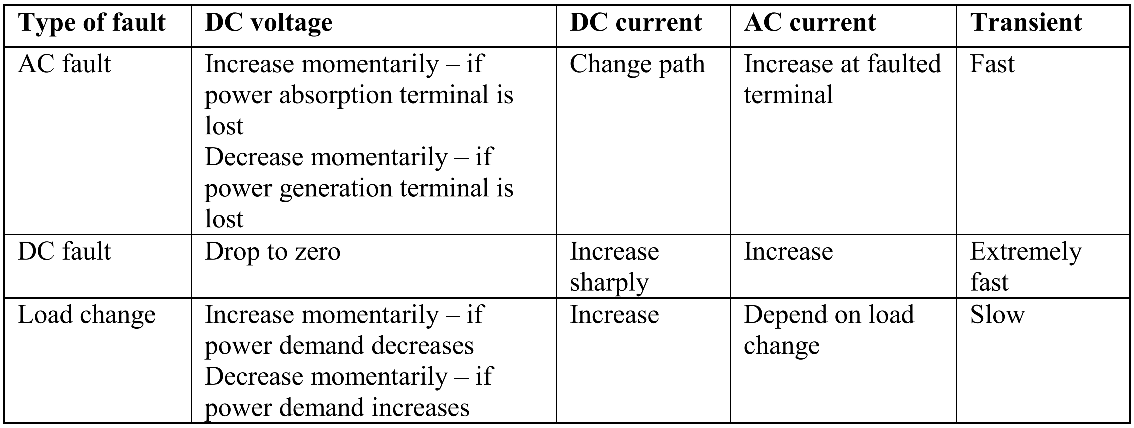
DC voltage: V_{dc1} starts to decrease at the instant of load change. The temporary drop is caused by the instantaneous need to meet new power demand and supply higher current. After few seconds, the DC voltage controller manages to bring the DC voltage back to reference value.

AC current: As expected, the AC currents at both terminals seem to increase when load resistor is changed. I_{a2} increases instantly, while I_{a1} sees a gradual increase in tandem with the DC voltage.

4.3 Summary

In this chapter, the test systems for this thesis have been presented. The fault studies will be performed in two ways: simulation and experiment. For simulation, PSCAD/EMTDC is used as a main tool to model a four-terminal MMC HVDC system. The step-by-step modeling of the system has been explained in detail. Due to the complexity of the system, it will be costly to replicate and implement it in hardware. Hence, a two level VSC, two-terminal DC system operating at scaled-down voltage level is built to conduct experimental studies. The components required for the experimental setup are described thoroughly.

Table 4.6: Summary of fault characteristic.



Type of fault	**DC voltage**	**DC current**	**AC current**	**Transient**
AC fault	Increase momentarily – if power absorption terminal is lost Decrease momentarily – if power generation terminal is lost	Change path	Increase at faulted terminal	Fast
DC fault	Drop to zero	Increase sharply	Increase	Extremely fast
Load change	Increase momentarily – if power demand decreases Decrease momentarily – if power demand increases	Increase	Depend on load change	Slow

The corresponding fault simulation is also performed. From both simulation and experiment, the behavior of the HVDC system to faults and load change can be concluded in Table. 4.6.

Chapter 5

Wavelet-based Fault Detection

5.1 Introduction

A comprehensive analysis of wavelet-based method detecting and locating fault in DC systems, built in both software and hardware, is presented in this chapter. Protection strategy is not of major focus, instead this chapter is more inclined to thoroughly study how wavelet transform can offer as a protection tool to decide right tripping signal. This chapter analyses how its performance can be affected by fault location, fault resistance and fault distance in the modular multilevel converter-based (MMC) HVDC system, which is modeled in PSCAD/EMTDC. The inter-terminal communication is preferably avoided for the reason of cost and speed, keeping in mind that this chapter assumes that the wavelet detection scheme is built to rely on local information at each terminal only. The influences of fault resistance and fault distance are also validated with the results obtained from a hardware setup of two-terminal VSC-based DC system. Readers will have an idea if the wavelet transform works on the result from experiment the same way it does on simulation result. This chapter also presents how effective the wavelet transform is in differentiating DC fault from load change, which is carried out experimentally. The improvement for the smoothened experimental result using properly designed filter will be discussed.

5.1.1 Theory

Wavelet transform is a signal processing technique that is able to analyze non-stationary signal in time and frequency domain. It differs from its counterpart, Short Time Fourier Transform (STFT), in a way that the window size in STFT is fixed. A longer time window results in good frequency resolution at the expense of time resolution, and vice versa. A convenient solution to this dilemma is wavelet transform, as it automatically changes the window size in response to the dynamic of signal. It is able to capture the high frequency abrupt change, which is specially needed in detecting the fault.

The wavelet transform breaks up a signal into the shifted and the scaled versions of the original (or mother) wavelet, allowing for simultaneous time and frequency analysis. The continuous wavelet transform (CWT) is defined as the sum over all time of the signal multiplied by the scaled and shifted versions of the wavelet function.

$$CWT(a,b)=\int_{-\infty}^{+\infty}x(t)\psi_{a,b}^{*}(t)dt \tag{5.1}$$

$$\psi_{a,b}^{*}(t)=|a|^{-1/2}\psi(\frac{t-b}{a}) \tag{5.2}$$

$\psi(t)$ is the mother wavelet, the asterisk in (5.1) denotes a complex conjugate, and $a,b\in R, a\neq 0$ (R is the real continuous number system) are the scaling and shifting parameters, respectively. The discrete wavelet transform (DWT) in (5.3) is given by choosing $a = a_0^{-}m/2$, $b = na_0^{-m/2}b_0$, $t = kT$ in (5.1) and (5.2), where $T = 1.0$, and $k, m, n \in Z$, (Z is the set of positive integers).

$$DWT(m,n) = a_0^{-m/2}(\sum x[k]\psi^*[\frac{k - na_0^{-m/2}b_0}{a_0^m}]) \tag{5.3}$$

We apply the multiresolution signal decomposition (MSD) [89, 90] technique to decompose a given signal into detailed and smoothed versions. Let $x[n]$ be a discrete-time signal, then the MSD technique decomposes the signal in the form of wavelet coefficient at scale 1 into $C_1[n]$, the smoothed (time-domain view) and $D_1[n]$, the detailed (frequency-domain view) coefficients. The decomposition process can be iterated, with successive approximations being decomposed in turn, so that the original signal is broken down into many lower resolution components. This is called the wavelet decomposition tree [89, 90], shown in 5.1. MSD technique can be realized with the cascaded quadrature mirror filter (QMF) banks [91, 92].

So, for example, using 4-scale decomposition, the original signal $x[n]$ can be represented as:

$$x[n] = C_4[n] + D_4[n] + D_3[n] + D_2[n] + D_1[n]. \tag{5.4}$$

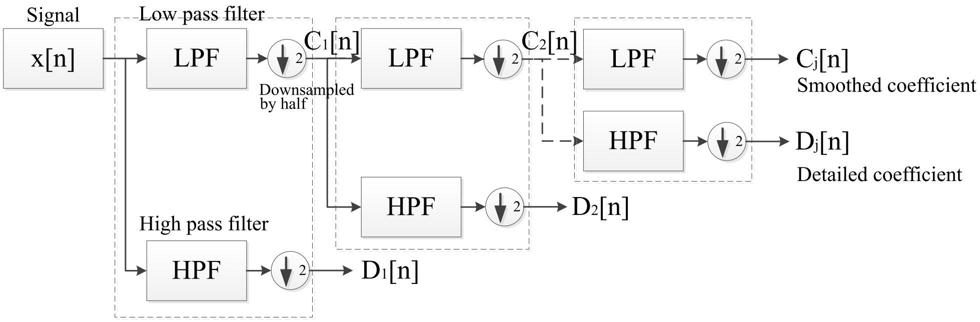


FIGURE 5.1: Multiresolution signal decomposition.

5.1.2 Selection of Mother Wavelet

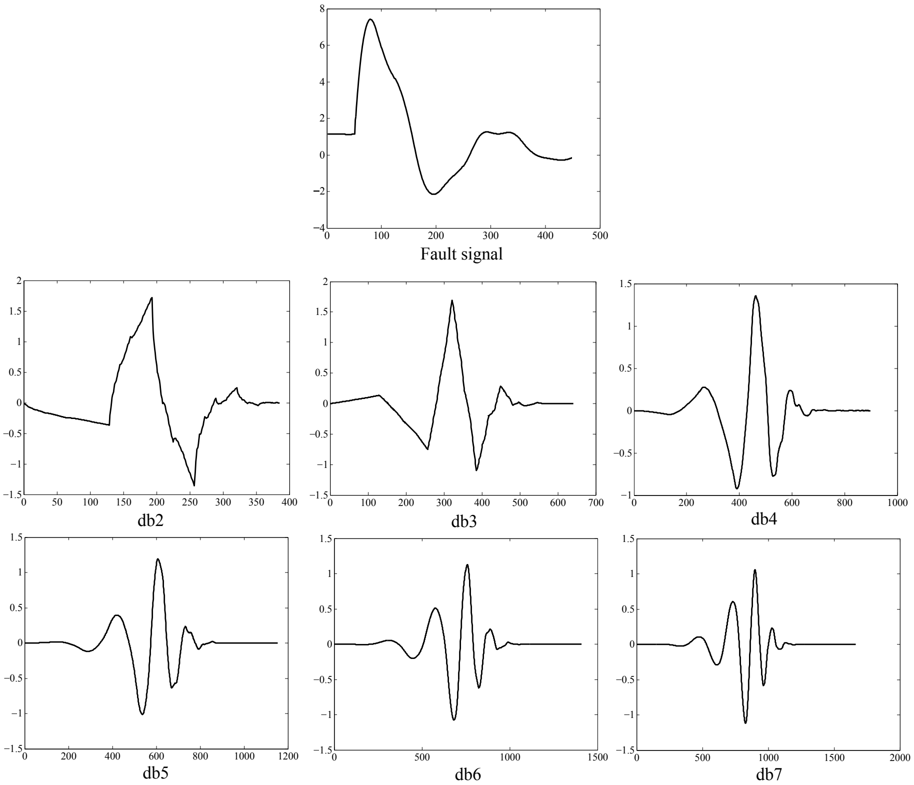


FIGURE 5.2: The cross correlation between the fault signal and Daubechies wavelet of varying orders.

The wavelet coefficient is the correlation of the signal and wavelet; the higher the wavelet coefficient, the closer the signal matches the chosen mother wavelet. Thus, a suitable wavelet should be selected such that it presents closest match to the pattern of the fault signal, so as to maximize the wavelet coefficient. Ma, Zhou and Kemp [93] worked out a method to facilitate the wavelet selection by using Pearson product-moment correlation coefficient, as represented in (5.5). The coefficient is a measure of linear similarity between two variables, with value ranging from -1 to 1. A value of 0 means that the two variables have no statistical relationship. The closer it is to 1, the stronger the association between both variables is.

$$r = \frac{\sum_{i=1}^{n}(X_i - \bar{X})(Y_i - \bar{Y})}{\sqrt{\sum_{i=1}^{n}(X_i - \bar{X})^2(Y_i - \bar{Y})^2}} \tag{5.5}$$

where X_i and Y_i are the datasets of fault signal and wavelet respectively, their corresponding averages are $\bar{X}$ and $\bar{Y}$.

Fig. 5.2 shows the fault signal obtained from simulation and the Daubechies wavelets from db2 to db7, generated by the wavelet function available in MATLAB. To compute (5.5), X_i is the fault signal while Y_i corresponds to the evaluated wavelet.

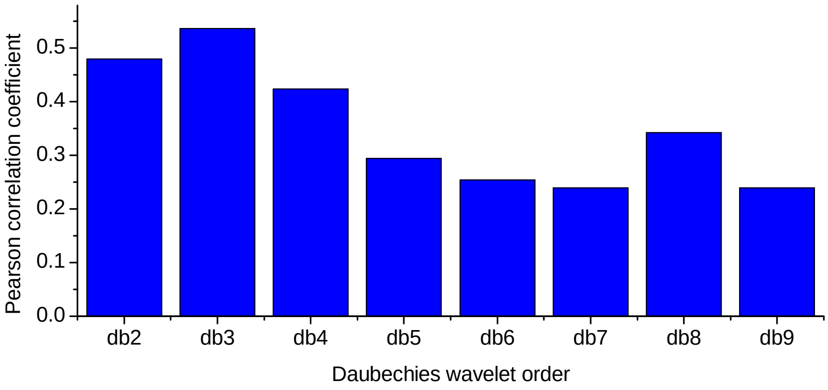


FIGURE 5.3: Correlation coefficient between fault signal and Daubechies wavelet of order 2-9.

The correlation coefficient between the fault signal and Daubechies wavelet of varying order ($db2 - db9$) is computed and depicted in Fig. 5.3. It is found that Daubechies wavelet of order 3 has the strongest association with the DC fault pattern. In other words, $db3$ is capable of generating the highest local maxima of the DC fault signal in the wavelet pattern. Also, it can best characterize the frequency content associated with fault.

5.1.3 Decomposition level

The decomposition level has to be selected such that it is able to target the frequency range generated by the fault. The frequency bands corresponding to each level of decomposition is presented in Table 5.1. It is known that the frequency content ranging [416 833] Hz is pronounced in the event of short-circuit fault [94, 95]. Therefore, for the sampling rate (f_s) of 15360 Hz, the 4th level detail coefficient will be the most suitable to localize the frequency of interest.

TABLE 5.1: Frequency band at each decomposition level

Decomposition level	**Frequency band (Hz)**	
	Approximation	**Detail**
1	0 - $f_s/4$	$f_s/4$ - $f_s/2$
2	0 - $f_s/8$	$f_s/8$ - $f_s/4$
3	0 - $f_s/16$	$f_s/16$ - $f_s/8$
4	0 - $f_s/32$	$f_s/32$ - $f_s/16$
5	0 - $f_s/64$	$f_s/64$ - $f_s/32$

5.1.4 Mother Wavelet and Time Delay

Besides having adequate sensitivity to the transient caused by the DC fault, it is equally important to choose the right mother wavelet that yields high-speed fault detection. Fig. 5.4 shows the performance of Haar, Daubechies and Coiflet wavelets on providing the maximum wavelet coefficient and corresponding time delay.

It is noticed that compact wavelets work well to localize high frequency components in the transient presenting minimum time delay. In this case, Haar and $db2-3$ stand out to be the ideal mother wavelet. s_f is the time the DC fault-induced transient begins to appear. The mother wavelets mentioned appear to produce maximum wavelet coefficients exactly at the same time. For the Daubechies wavelet family, $db5$ begins to show time delay by one sample. Coiflet wavelet is inappropriate for DC fault detection

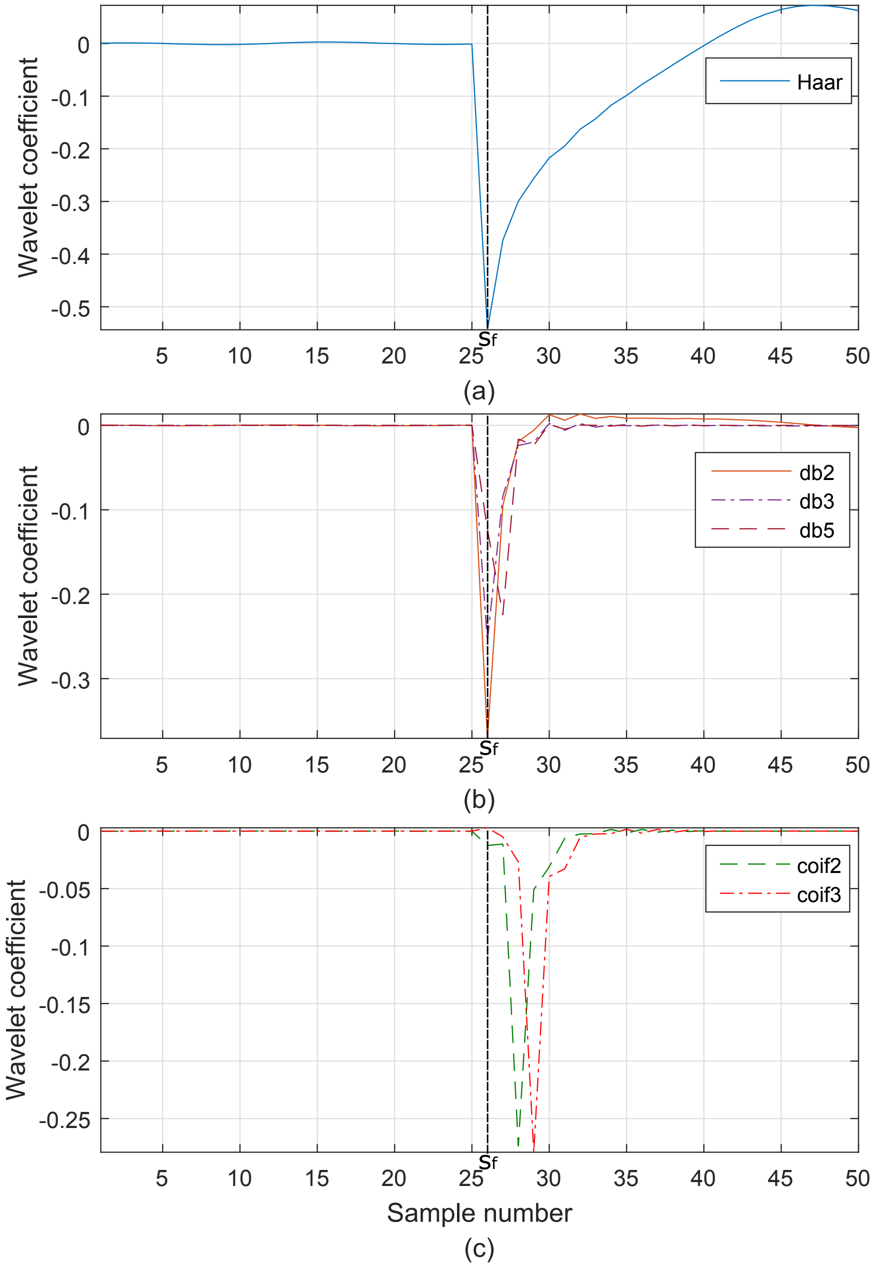


FIGURE 5.4: Time delay introduced by different mother wavelets.

as far as speed is concerned. The analysis is not too far off from the finding in Santoso's work [96] pointing out that *db*4 and *db*6 are great for fast transient in conventional AC system.

5.2 Fault Analysis on Simulation Test System

Simulation Model 1, as depicted in Fig. 4.1a, is used as the test model in this fault analysis. It consists of four strong AC systems ($Ti, i = 1, 2, 3, 4$) are connected with ring and monopole DC network. The DC lines ($L_{ij}, i, j = 1, 2, 3, 4$) with positive and negative pole are only represented as single line. $MMC1$ works as fixed DC voltage control and the remaining MMC as fixed active power control.

The DC currents ($Idc_{ij}, i, j = 1, 2, 3, 4$) are measured at each DC line. The IGBTs will not be blocked in the simulation as this chapter only intends to focus on the very first step that precedes the blocking, which is fault identification. The DC current signals are exported to MATLAB and post-processed with DWT algorithm, using the code in Appendix E, to generate the wavelet coefficients.

The fault location (D_f) is the distance from the fault to the monitoring terminal. The fault simulated here is pole-to-pole fault on DC line ($Fdc_{ij}, i, j = 1, 2, 3, 4$), represented by fault resistance R_f. The sampling rate (f_s) is selected based on the available frequency range offered by digital fault recorder [97]. The mother wavelets to be adopted is $db3$, since it has been discussed in Section 5.1.2 that the mother wavelet of this scale presents the closest similarity with fault pattern. The 4th decomposition level is considered.

The application of wavelet transform in MMC HVDC fault identification is evaluated by looking at four cases below:

- To study the influence of DC fault location: PP fault on Lij ($i, j = 1, 2, 3, 4$), occurring at 0.25 s, $R_f = 0.01\Omega$, $df = 50km$, $f_s = 15360Hz$, using $db3$.
- To study the influence of DC fault resistance: PP fault on $L12$, $0.01 < R_f < 500\Omega$, occurring at 0.25 s, $D_f = 50km$, $f_s = 15360Hz$, using $db3$.

- To study the influence of DC fault distance: PP fault on $L12$, $R_f = 0.01\Omega$, occurring at 0.25 s, $15 < D_f < 85km$, $f_s = 15360Hz$, using $db3$.
- To study the influence of sampling rate: PP fault on $L12$, $R_f = 0.01\Omega$, occurring at 0.25 s, $D_f = 85km$, $f_s = 3840, 5760, 7680, 15360Hz$, using $db3$.
- To study the function of fault current limiter: PP fault on $L12$ (radial network), $R_f = 0.1\Omega$, occurring at 0.25 s, $D_f =$ close to Bus 1, $f_s = 15360Hz$, using $db4$.

5.2.1 Influence of DC Fault Location

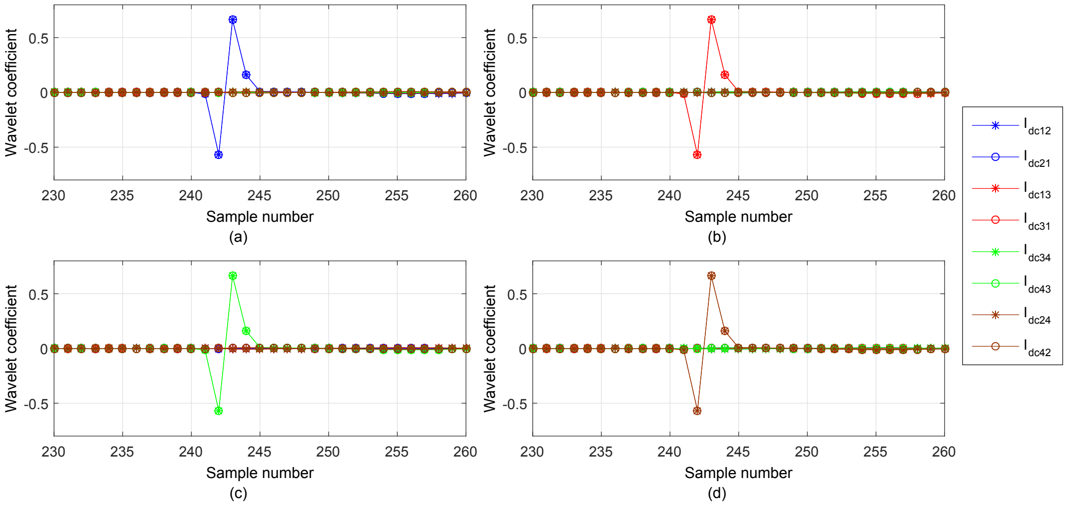


FIGURE 5.5: Detailed wavelet coefficient for each DC line current in different PP fault location. a) F_{dc12}, b) F_{dc13}, c) F_{dc34}, d) F_{dc24}.

Fig. 5.5 shows the wavelet coefficient obtained from simulating the PP fault on four DC lines in the MMC HVDC system. The PP fault is initiated by shorting the positive and negative DC lines through a fault resistance. Therefore, only the wavelet coefficient for positive pole DC current is presented here.

The steady state DC current is essentially constant, therefore the wavelet coefficient remains low, approximating to zero. The occurrence of fault on a DC line is detected when the DC currents of that line yields an increased wavelet coefficient abruptly. To illustrate, PP fault on $L13$ (see Fig. 5.5(b)) generates large overcurrent in fault current between $MMC1$ and $MMC3$, resulting in high wavelet coefficients for I_{dc13} and I_{dc31}. Similar pattern is consistently observed in other cases.

The high wavelet coefficients appear at 242nd sample. To reconstruct the decomposed signal to its original form, the fault can be said to be detected at 3841th sample (4th stage of decomposition or approximately 2^4), which is about 0.2500491 s. Taking into account the time delay introduced by 4 stages of filtering, the actual detection delay works out at 49.1 μs+(4×1/15360 Hz)=0.31 ms.

The wavelet transform also helps healthy terminals to recognize that the fault is not happening in their protection zone when the wavelet coefficients for their DC current is low throughout. The discriminative nature of wavelet transform presents a reliable method for each terminal to independently identify the fault by just monitoring their DC current.

5.2.2 Influence of DC Fault Resistance

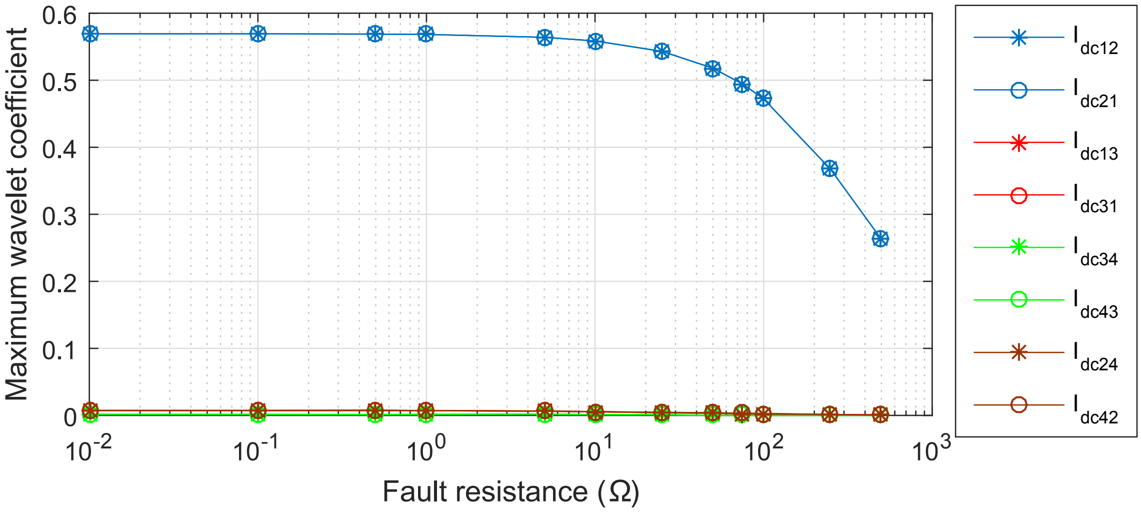


FIGURE 5.6: Effect of PP fault resistance on detailed wavelet coefficient for each DC line current.

This subsection looks into how robust the wavelet transform can detect fault with high resistance in multi-terminal HVDC system. Fig. 5.6 shows a line graph depicting the trend of detailed wavelet coefficient for each line current as the fault resistance on $L12$ is increased from 0.01 Ω to 500 Ω.

The wavelet coefficient appears to be constantly high for the PP fault resistance ranging from 0.01 Ω to 5 Ω. Beyond that, however, the value begins to show downward trend. This can be explained by the fact that fault induced transient has been dampened by large fault resistor. As a consequence, the wavelet coefficient decreases with increasing fault resistance. Despite the decreased sensitiveness to high fault resistance, the coefficients of fault current still remain vastly above that of healthy pole DC current, which revolves around 0.005, and this does not diminish the capability of wavelet transform to detect the presence of high resistance PP fault.

5.2.3 Influence of DC Fault Distance

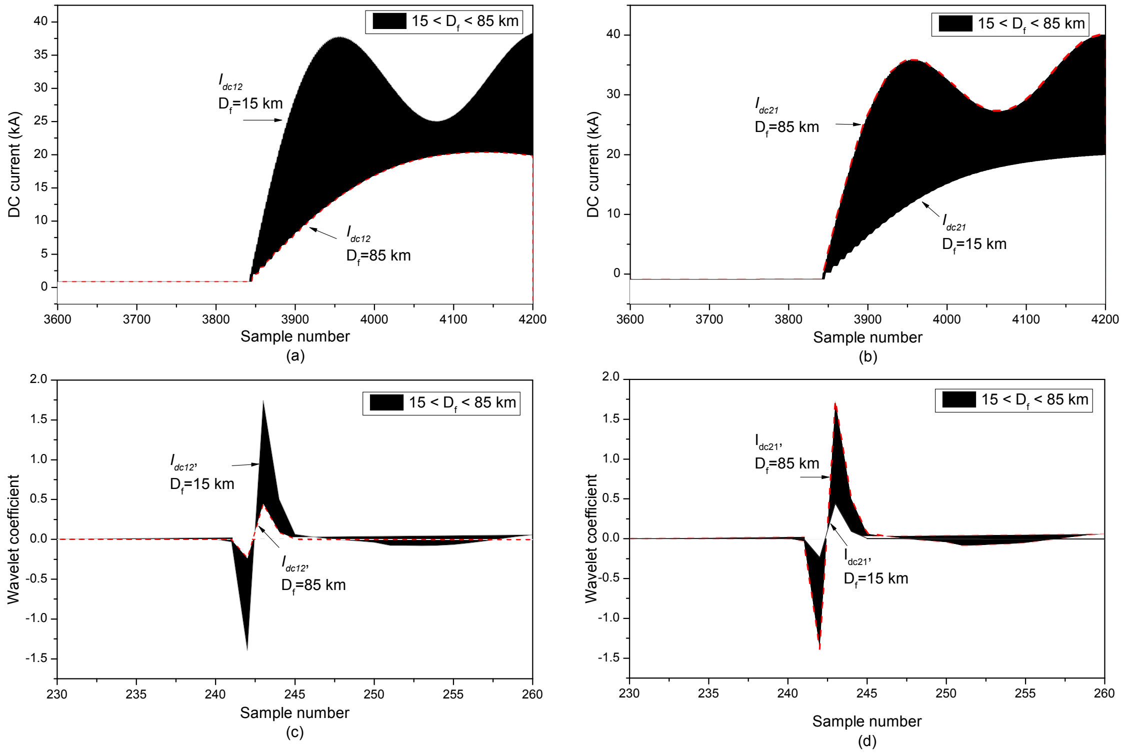


FIGURE 5.7: DC current (a) I_{dc12}, (b) I_{dc21} and their corresponding detailed wavelet coefficient (c), (d) under the influence of fault distance.

The fault-induced transients and the fault current are dependent on the location on DC lines. If a DC fault happens at a point nearer to a terminal, one can expect to see the fault current of that terminal having bigger frequency change and higher magnitude compared to its neighboring terminal sharing the same line. Fig. 5.7 shows the detailed wavelet coefficient for I_{dc12} and I_{dc21} as the location of PP fault (D_f) is adjusted from 15 km to 85 km away from $MMC1$ along $L12$.

The fault point divides the DC line into two sections such that $MMC1$ and $MMC2$ see unequal share of line resistance. The effect of fault distance is observable in Fig. 5.7(a) & (b), whereby the current magnitude decreases and the transient becomes dampened as the fault point is further away. The wavelet coefficients show sensitiveness to the fault distance. For example, the fault at $D_f = 85km$ yields the wavelet coefficient about

-0.2342 for I_{dc12} and -1.389 for I_{dc21}. At the same D_f, the highest wavelet coefficient for healthy line current is 0.019, generated by I_{dc24}. This provides a margin of 0.2152, which is considerably sufficient for the wavelet transform method to preserve reasonable selectivity. In short, all the faults evaluated in this study can be successfully detected.

5.2.4 Influence of Sampling Frquency

Keeping in mind that time is extremely critical in a protection system, the influence of sampling rate on the time delay has to be considered in designing wavelet-based fault detection method. The relationship between these two factors is summarized in Table 5.2, in which it shows how the time delay changes with the sampling rate adopted in extracting the fault signal.

Table 5.2: Effect of sampling frequency on detailed wavelet coefficient for each DC line current during PP fault on $L12$.

Line current	**Sampling frequency**							
	15360 Hz		**7680 Hz**		**5760 Hz**		**3840 Hz**	
	Wavelet coefficient	**Time (ms)**	**Wavelet coefficient**	**Time (ms)**	**Wavelet coefficient**	**Time (ms)**	**Wavelet coefficient**	**Time (ms)**
I_{dc12}	0.5693	0.065	1.116	0.11	1.388	0.12	1.973	0.26
I_{dc21}	0.5693	0.065	1.117	0.11	1.387	0.12	1.937	0.26
I_{dc13}	0.0073	2.13	0.04384	4.21	0.1221	14.72	0.1227	4.3
I_{dc31}	0.0074	2.13	0.0044	4.21	0.1219	14.72	0.1254	4.3
I_{dc34}	0.0016	27.96	0.0149	39.07	0.0425	39.03	0.0664	57.73
I_{dc43}	0.0016	27.96	0.015	39.07	0.0425	39.03	0.0669	52.73
I_{dc24}	0.0073	2.13	0.0611	14.47	0.1245	14.71	0.1659	16.41
I_{dc42}	0.0074	2.13	0.06139	14.47	0.1249	14.71	0.1673	16.41
I_{dc23}	0.005	2.13	0.0317	14.47	0.0645	14.71	0.1403	16.41
I_{dc23}	0.0031	4.2	0.0325	14.47	0.04644	14.71	0.1422	16.41

Four sets of sampling rates are assessed here: 3840, 5760, 7680, 15360 Hz. 3840 Hz, being the lowest sampling rate studied here, produces the highest coefficients for fault current I_{dc12} and I_{dc21}. This implies that, in that particular window of samples coinciding with the instant of fault, the analyzed signal has the frequency content that is close to the pseudo-frequency of wavelet at the given scale and sampling rate. The coefficient appears at 0.26 ms after the fault, which is considerably fast. Sampling frequency 15360 Hz provides the fastest fault detection despite having the lowest coefficient. The frequency content is not of particularly concern in a protection decision making. Thus, it is reasonable to say that higher sampling rate is more desirable. Nevertheless, since it is widely suggested that the optimal fault detection time should be kept within 1 ms, all the sampling rates here seem to meet this requirement.

5.2.5 Influence of decomposition level

In Section 5.1.3, it has been discussed that 4th decomposition level is the most optimum to target the frequency range associated with DC fault, considering the sampling frequency to be f_s=15360 Hz. The frequency can vary depending on fault resistance and distance. This is evidently shown in the analysis in Section 5.2.2, whereby the wavelet coefficient decreases for the high impedance fault. This can be improved by using higher decomposition level as it is more suitable to capture the reduced frequency caused by the high impedance fault. It would be interesting to understand what kind of trade-off we will face if higher decomposition level is used.

Table 5.3: Effect of decomposition level on detailed wavelet coefficient and time delay for different fault resistance. Line current evaluated is I_{dc12}.

Fault resistance	**5th decomposition level**		**6th decomposition level**	
	Wavelet coefficient	**Time (ms)**	**Wavelet coefficient**	**Time (ms)**
0.1 Ω	0.736	0.18	1.122	0.24
0.5 Ω	0.749	0.18	1.232	0.24
10 Ω	0.759	0.18	1.317	0.24
25 Ω	0.778	0.18	1.455	0.24
50 Ω	0.778	0.18	1.461	0.24
100 Ω	0.732	0.18	1.236	0.24

Table 5.3 shows the wavelet analysis of I_{dc12} for PP fault on $L12$, using 5th and 6th decomposition level. In both cases, improvement can be seen whereby the influence

of fault resistance does not compromise the wavelet coefficients at the same rate as with the case in 4th decomposition level. This suggests that the sensitiveness to high fault resistance can be improved by using higher decomposition level. However, better robustness comes at the expense of detection time. This is because cascade filtering results in time delay when computing the wavelet coefficient in subsequent level. For example, 5th decomposition level takes as much as 0.18 ms, while 6th decomposition level needs 0.24 ms. 4th decomposition level has slightly poorer robustness, but the trade-off for shorter time delay is acceptable as far as the fault detection is concerned.

5.2.6 Employment of Fault Current Limiter

The performance of wavelet transform method will be evaluated with the inductive FCL integrated into the simulated system. A challenging fault condition has been discussed in Section 4.1.3, whereby F_{dc12} will result in false tripping without FCL imposing some electrical differences. The radial multi-terminal HVDC system in Fig. 4.5 is simulated. For this study, the FCLs of 0.1 H are installed at the termination of DC lines.

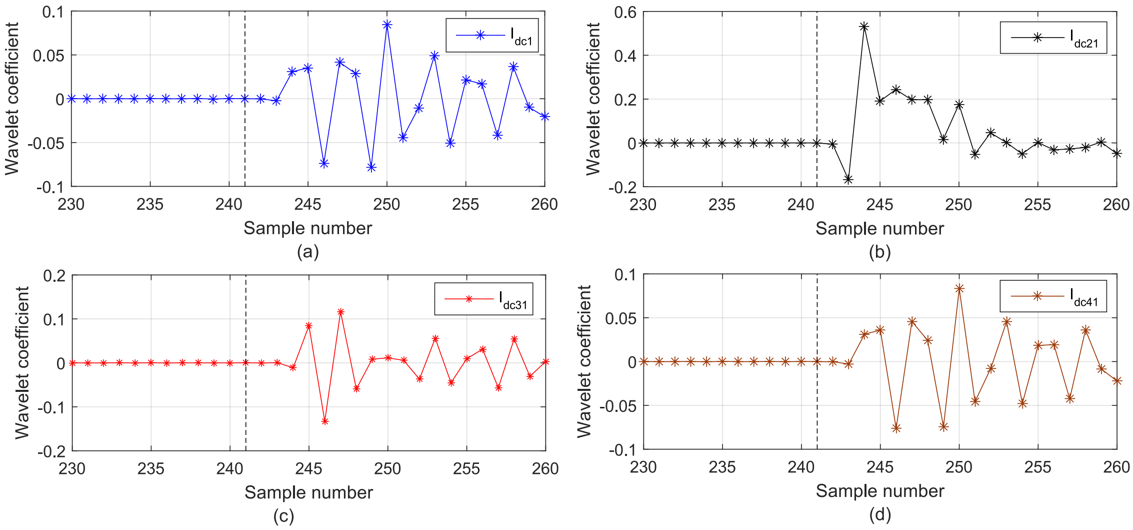


FIGURE 5.8: Detailed wavelet coefficients for DC line currents under F_{dc12} in radial multi-terminal HVDC system (including inductive FCL). (a) I_{dc1}, (b) I_{dc21}, (c) I_{dc31} and (d) I_{dc41}.

Fig. 5.8 shows the result with FCL employed in the system. The dotted line indicates the inception of fault. I_{dc21} exhibits the sign of DC fault when analyzed with wavelet transform. It yields the highest wavelet coefficient at 244th sample, slightly later than the cases without FCL. This also evidently indicates that the fault current has decreased at slower rate due to the large inductor. As for the remaining healthy lines, all their currents have low wavelet coefficients. Threshold must be set so that it is greater than the highest wavelet coefficient generated by I_{dc31} at 246th sample. Overall, the employment of FCL helps improving the selectivity of the wavelet transform method in radial network.

5.3 Fault Analysis on Experimental Test System

Experimental Model depicted in Fig. 4.9 is run to generate DC fault result.

Fig. 5.9 shows the measurements of I_{ac1}, V_{dc1}, I_{dc1} and I_{dc2}, in that order on LeCroy Wavesurfer 3024 oscilloscope, for 2 Ω DC fault. The sampling frequency used in the measurement is 10 kHz. The signals of interest here are I_{dc1} and I_{dc2} and the segment in dashed box is zoomed in to offer readers better view of the fault-induced transient. The corresponding wavelet analysis using $db3$ is presented in the same figure.

One can immediately notice that the steady state DC currents essentially do not yield zero wavelet coefficient as seen in the simulation results. The value seems to hover between $[w1,w2]$, marked by the dashed line. For now we take $[w1,w2]$ as threshold, it will be discussed in subsection later how removing the noise in the signal can reduce the steady state wavelet coefficient.

Abrupt increase of current caused by DC fault registers high wavelet coefficients for both currents. The fault inception time (3 s) is translated to 1877th sample at 4th level

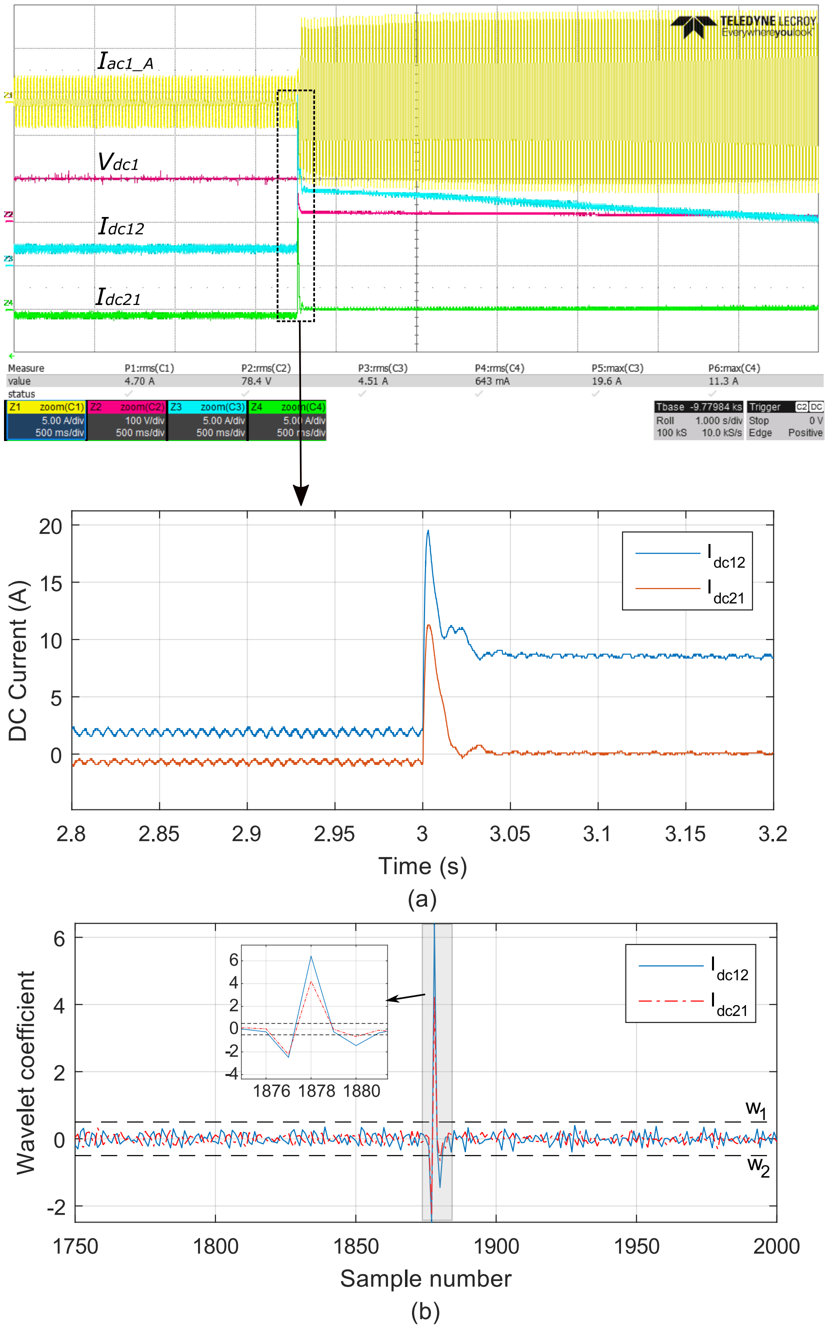


FIGURE 5.9: (a)Experimental result for 2 Ω DC fault; (b)Wavelet coefficients for I_{dc1} and I_{dc2}.

of decomposition. At that exact instant, the wavelet coefficient is seen to exceed the threshold. The highest wavelet coefficient is obtained at 1878th sample, which roughly translates to 3.001648 s. Even with the delay introduced by 4 stages of filtering (4×0.1 ms= 0.4 ms), the detection time is still reasonably short.

The algorithm of wavelet transform is written in MATLAB R2015b and computed in the Intel Core i5 CPU with 4.0 GB of RAM. The average computation time to output a sample is approximately 41.25 μs.

5.3.1 Influence of DC Fault Resistance

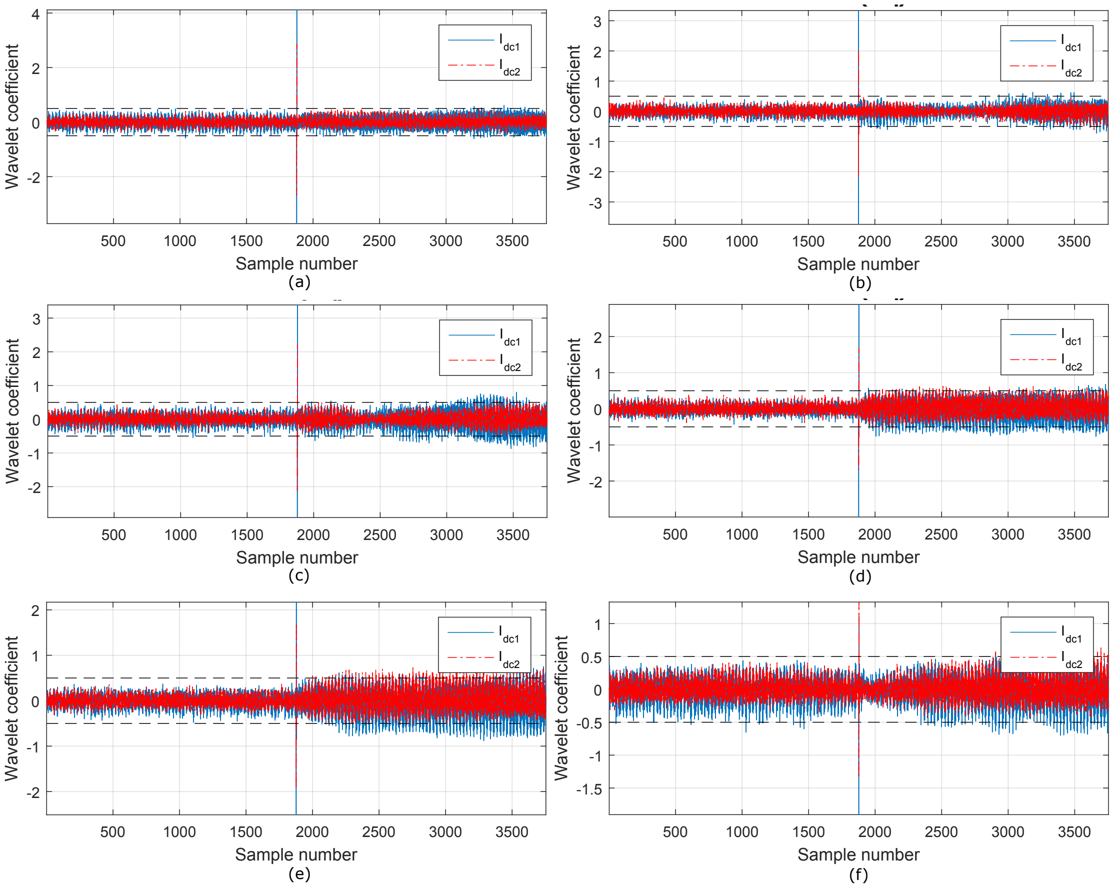


FIGURE 5.10: Wavelet coefficient for DC fault of varying fault resistance (a) 4 Ω; (b) 6 Ω; (c) 8 Ω; (d) 10 Ω; (e) 12 Ω; (f) 14 Ω.

Similar to Section 5.2.4, repeated experiments are carried out to evaluate the performance of wavelet transform on different fault resistance, ranging from 4 Ω to 14 Ω. Fig. 5.10 depicts the result of wavelet analysis on the DC currents, namely I_{dc1} and I_{dc2}.

All of the faults are detected, as can be seen that the onset of fault results in increase of wavelet coefficient. The high wavelet coefficient is observed around sample number 1877. Despite the presence of noise in the signal, the wavelet coefficients are kept within the presumed threshold, marked by the dashed line in the figures, during steady state. The wavelet coefficient shows downward trend when increasing the fault resistance. Nevertheless, a reasonably sufficient margin between threshold and the wavelet coefficient still justifies the effectiveness of wavelet transform in detecting the DC fault.

5.3.2 Influence of DC Fault Location

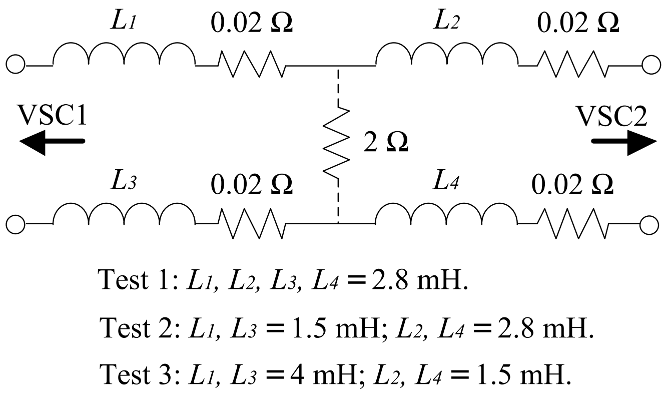
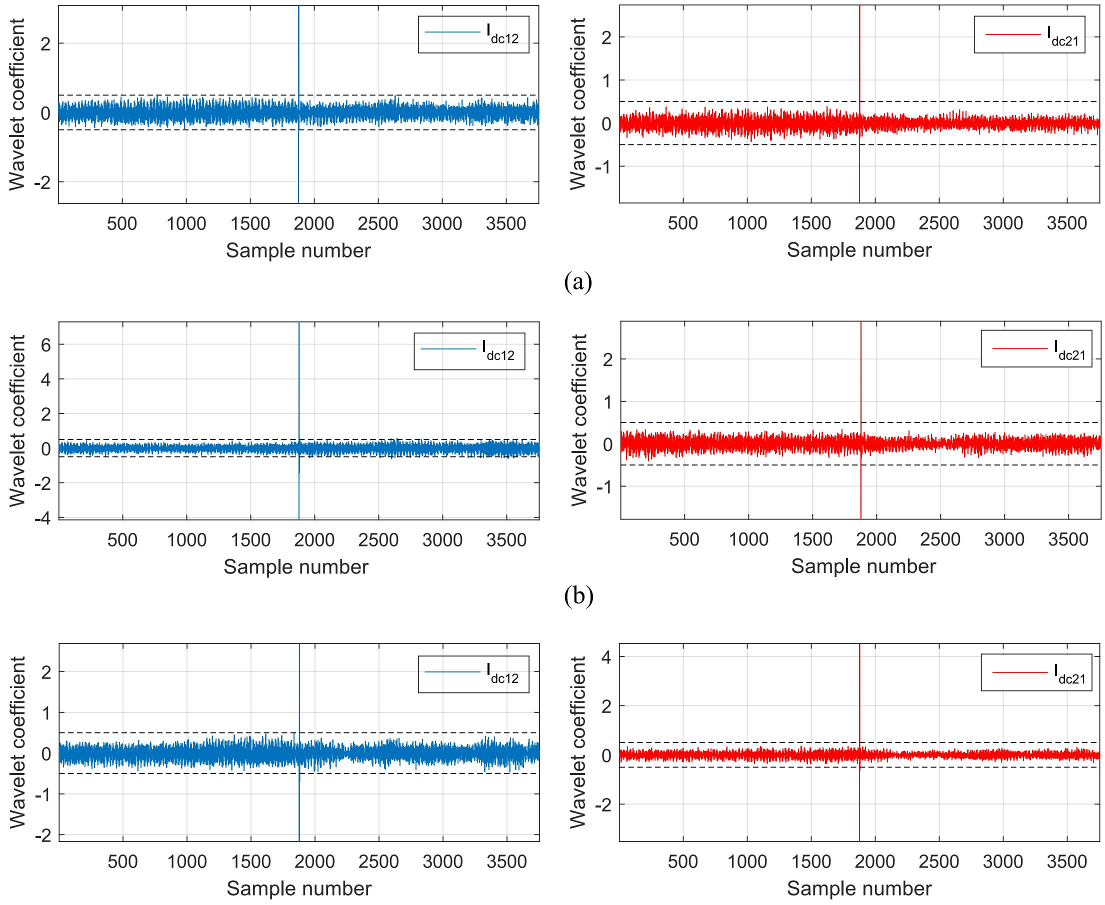


FIGURE 5.11: DC line represented by RL circuit in experiment and different line length to be investigated.

Similar to Section 5.2.4, our interest is to study the effect of fault distance on wavelet transform at experimental level. Besides the fault location on the DC line, the frequency content of transient is also a function of DC line length. Three tests with different combination of inductance representing different fault location and DC line length are carried out, as shown in Fig. 5.11. The DC currents are analyzed with wavelet transform and the result is shown in Fig. 5.12.

The wavelet transform succeeds to detect the DC fault with the wavelet coefficient exceeding threshold by large margin. One can observe that the line current of the terminal, nearer to the fault, yields the higher wavelet coefficient. For example, in Test 3, smaller L_2 and L_4 implicates the fault to be nearer to the Terminal 2, and the fault at this location results in higher wavelet coefficient for I_{dc2} compared to I_{dc1}. Even so, the



(a)

(b)

(c)

FIGURE 5.12: Wavelet coefficient for DC fault of varying fault location (a) Test 1; (b) Test 2; (c) Test 3.

two terminals are still able to recognize the occurrence of DC fault as their maximum wavelet coefficients are consistently higher than threshold in all cases.

5.3.3 Influence of Load Change

Load change in power system results in current increase that could be mistaken for DC fault. This subsection aims to study the feasibility of wavelet transform differentiating between DC fault and load change. To reproduce this phenomenon at experimental level, the resistive load at receiving end is reduced abruptly such that it will generate transient reaching the same peak as fault-induced transient. The results from experiment and the corresponding wavelet coefficients are shown in Fig. 5.13.

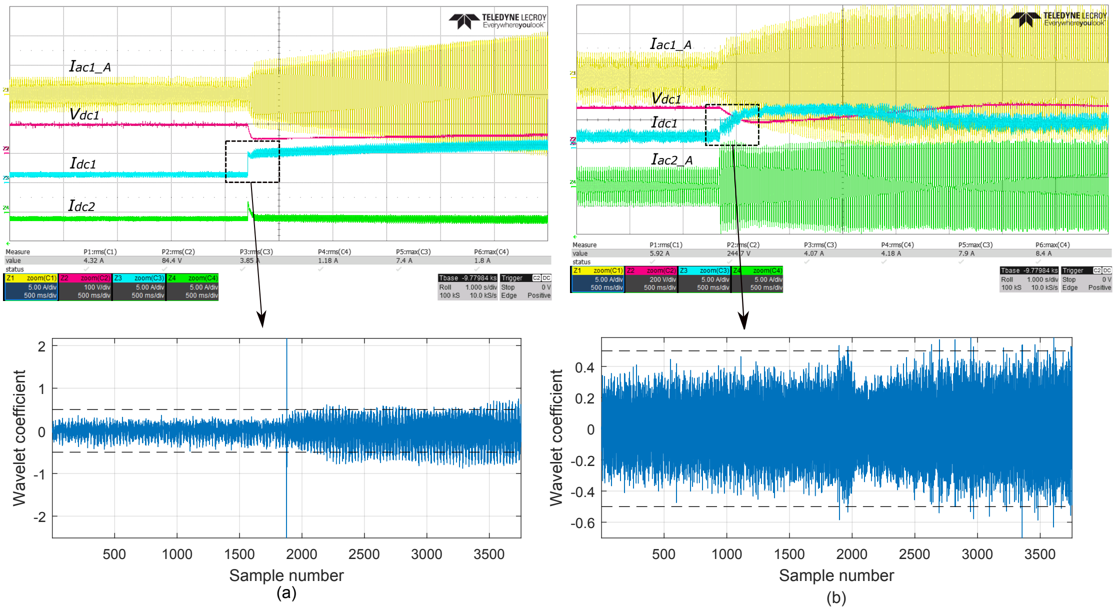


FIGURE 5.13: Experimental result and wavelet analysis for (a) DC fault; (b) Load change.

As expected, the I_{dc1} in DC fault produces high wavelet coefficient. Although the load change causes transient in the DC current, its wavelet coefficient only increases by small margin, barely crossing the presumed threshold. It is now clear that the wavelet transform presents its capability in discriminating the DC fault from load change.

5.3.4 Influence of Signal Noise

The signals measured directly from the experiment contain some noise amounting to 11.421 dB signal-to-noise ratio (SNR). Such noise, however, gives rise to non-zero wavelet coefficient during steady state. The steady state wavelet coefficients appear to stay within the presumed threshold in all the studies so far. This subsection investigates the improvement in the steady state wavelet coefficient when the noise in the signal is filtered.

The I_{dc1} for DC fault at 14 Ω is smoothened using bandstop filter (elliptic, cutoff frequencies 150Hz and 180 Hz) so as to avoid removing the fault-induced transient which

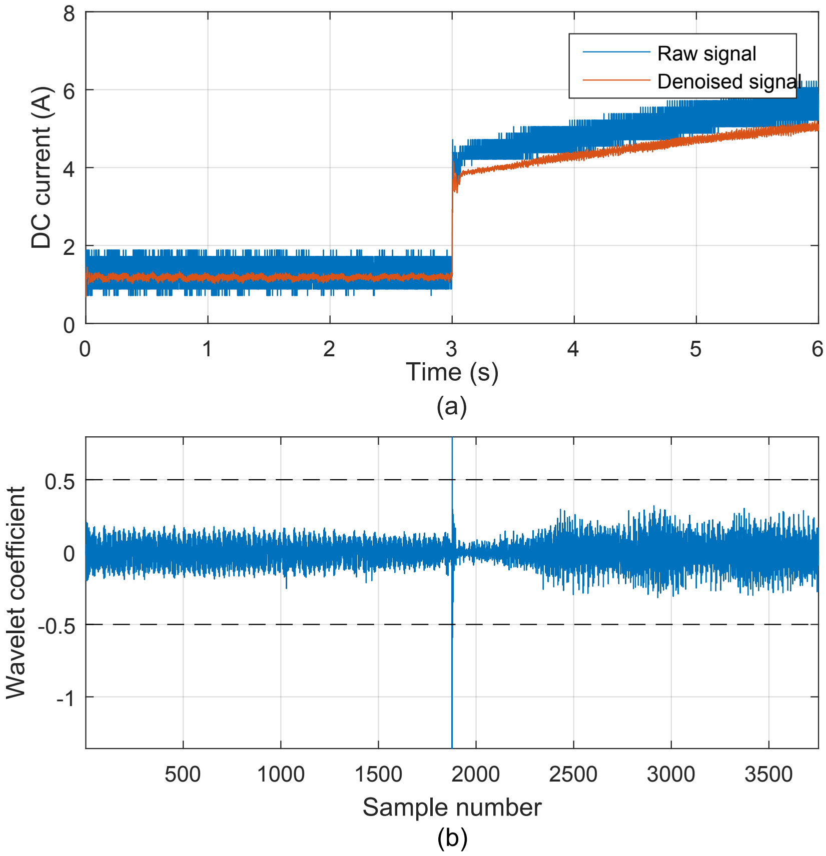


FIGURE 5.14: (a) Raw and denoised signal for DC fault at 14 Ω; (b) Wavelet coefficient for denoised signal.

is of high frequency and extremely critical for producing high wavelet coefficient. The denoised signal now has 27.658 dB SNR during steady state. Fig. 5.14 depicts the difference between raw and denoised signal. The transient in the denoised signal is not compromised. When analyzed with the wavelet transform, the steady state wavelet coefficient is seen to have decreased substantially (see Fig. 5.14(b)), compared to that in Fig. 5.10(f). In addition, the maximum wavelet coefficient does not deviate much as a result of filtering. Hence, an appropriate filtering without compromising the fault-induced transient is highly recommended if one wants to keep the steady state wavelet coefficient as low as possible.

5.4 Summary

The feasibility of wavelet transform in detecting and identifying DC fault in DC systems has been analyzed in this chapter and validated using simulation and experimental results. *db*3 is adopted in the wavelet analysis as it presents the closest match to the fault pattern and is able to detect fault with minimal delay.

The simulation result shows that the wavelet transform is able to detect the faulted line in a four-terminal HVDC system, only using the wavelet coefficient for DC line current at each terminal as criterion. The detection time shorter than 1 ms is achievable. The value of wavelet coefficient decreases as the fault resistance and the fault distance are increased, however in all cases the value is still well above the threshold by large margin. Different sampling frequencies (3840 Hz, 5760 Hz, 7680 Hz and 15360 Hz) are considered in this study. It is found that higher sampling frequency yields faster detection with decreased wavelet coefficient. The introduction of inductive fault current limiter has been analyzed; it improves the selectivity of wavelet transform method, successfully identifying the fault which is near the DC line termination.

From the experimental results, it can be inferred that the wavelet transform also presents robustness to the influence of fault resistance and distance. It is not sensitive to the transient caused by load change, allowing us to classify DC fault from other types of disturbance. The inherent noise in the experimental result yields a non-zero wavelet coefficient, thus the threshold needs to be set above that so as to avoid wrong detection. It is seen that the wavelet transform has reasonable tolerance to noise. The steady state wavelet coefficient can be vastly reduced if the signal is smoothened. The filter has to be properly designed so that only the unwanted noise is removed while the fault-induced transient, which is of high frequency, is still retained.

Chapter 6

Capacitive Discharge-based Fault Detection

6.1 Introduction

Previous chapter has studied the efficacy of wavelet transform to detect the DC fault in VSC-HVDC systems, but there is room for improvement with regards to the detection sensitivity. The fault criterion is based on hard threshold, that is, the threshold for trip setting is determined based on the margin between minimum value for faulty condition and maximum value for healthy condition. As such, one has to find different threshold when migrating from one system to another.

In this chapter, a transient analysis based on DC-link capacitive discharge is presented. This novel fault detection method attempts to use correlation coefficient as a criterion to assess the possibility of DC fault in a VSC-based DC system. As the correlation coefficient is normalized to range of 0-1, it can do away with the exhaustive process to find the threshold. During pole-to-pole DC fault, the capacitor will discharge immediately and generate large current to the fault point through the DC lines. This phenomenon can be translated into useful information to determine the occurrence of DC fault. The discharging process happens independently of the fault parameters (resistance and location), hence this method is very robust. Additionally, it does not involve complex signal processing technique, so it can be implemented with minimal computational effort.

6.1.1 Detection Based on Current Derivative

The current derivative method [28, 29] is based on the assumption that DC current surges sharply as a result of fault, such that (6.1) will yield a large value. The works cited here show that this method can successfully select the faulted line in a DC microgrid system. Besides that, with careful calculation of threshold, it can classify different fault locations, such line and bus.

$$\Delta I_{dc} = I_{dc_k} - I_{dc_{k-1}}, \tag{6.1}$$

where I_{dc_k} is the DC current signal at kth sample.

The finding of threshold is an iterative process to determine the minimum value that will differentiate the fault condition from the cases in which circuit breaker should not trip. Besides that, this method is highly sensitive to fault parameter. The time constant in the exponential term in (3.35) implies that the di/dt of fault current depends on the fault resistance (R_f) and fault distance, which can be represented by L_{dc} and R_{dc}. To illustrate the influence of fault resistance, (3.37) is calculated using parameters in Table 3.1, except that R_f is step-changed from 5 Ω to 100 Ω. The di/dt of fault current is shown in Fig. 6.1. The rate of change suffers substantial drop as the fault resistance is increased. Using the rate of change as a fault detection criterion may result in the failure to detect the DC faults with high impedance.

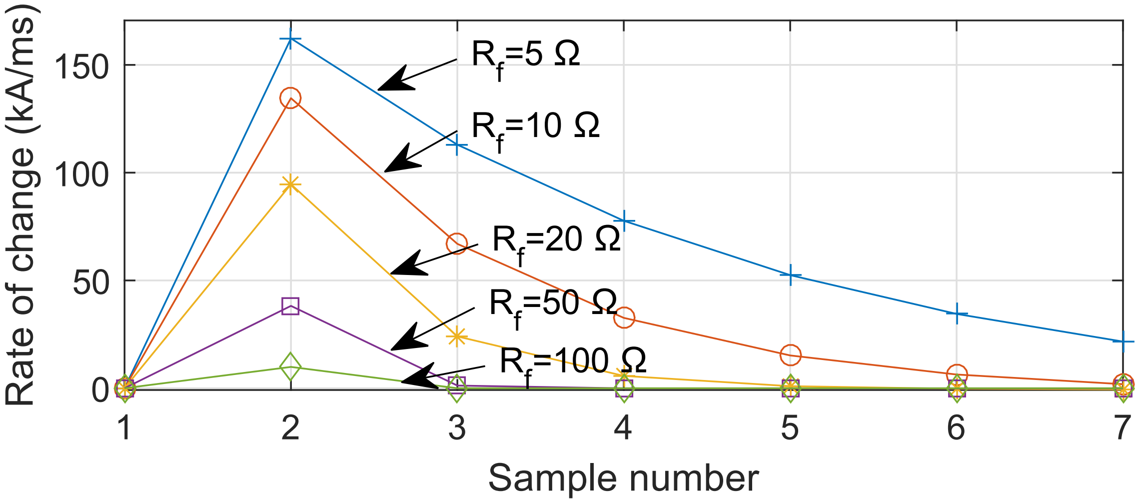


FIGURE 6.1: Rate of change of current under variation of fault resistance.

6.1.2 Detection Based on Capacitive Discharge

It has been presented in Section 3.4 that the discharging of DC-link capacitor dominates the fault current initially as a result of PP fault. This particular time frame is especially critical to make a fault decision before the fault current starts freewheeling through diodes (Stage 2). The DC-link capacitor discharge is a natural response to DC fault. Taking advantage of this phenomenon, a new fault detection method is proposed such that it monitors the behavior of DC-link capacitor; if the fault current is found to contain the current injected by the capacitor, it will be interpreted that the DC fault has occurred. To address the weakness of the method based on current derivative, a fault criterion is introduced in an effort to improve its robustness.

DC fault results in DC voltage dropping, which will invariably trigger discharging of DC-link capacitor. Such behavior of DC-link capacitor is leveraged to form a definitive fault indicator. The proposed detection method is based on the concept that, when the

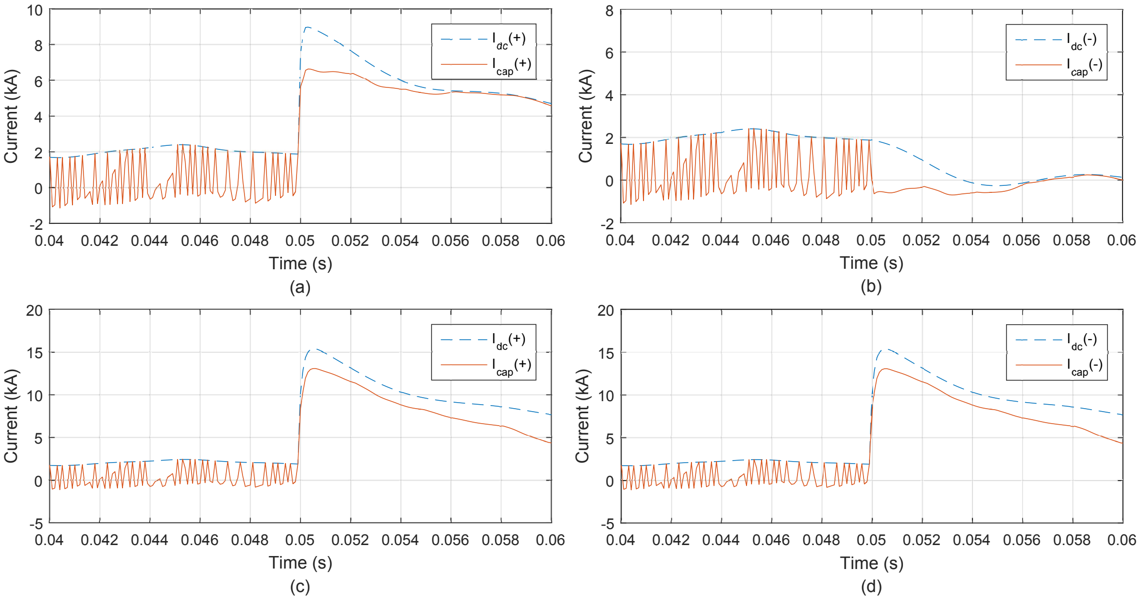


FIGURE 6.2: Fault current and discharging current of DC-link capacitor in positive and negative poles.(a) & (b) PG fault, (c) & (d) PP fault. (+) and (-) signifies positive and negative pole.

DC fault occurs, the rising pattern of the DC fault current initially will resemble that of the discharging current of DC-link capacitor.

The signals required for this fault detection method are the line currents at each VSC terminal and the discharging current of the associated DC-link capacitor. Since this method is able to work independently without relying on the information of neighboring terminals, the communication channel can be opted out. DC fault is inherently fast in penetrating VSC-HVDC system due to the lack of inductance. With the authority to make fault decision given to each terminal, the circuit breaker tripping can be executed as soon as the fault is detected within their protection zone.

The proposed method comes with the ability of classifying the faulty poles. Fig. 6.2(a-b) shows the DC line current and discharging current of DC-link capacitor during PG (positive pole short-circuited to ground) and PP faults. In the system with symmetric monopole configuration in which the DC-link capacitors are mid-grounded, PG fault may cause top and bottom capacitor to discharge at different rates. The DC-link capacitor involved in the fault loop will have its discharging current superimposed to the fault current. As a result, the fault current ($I_{dc}(+)$) and the discharging current of top capacitor ($I_{cap1}(+)$) will have a matching rising slope. On the contrary, the healthy pole (-) shows a rather opposite observation. As for the PP fault, the discharging currents of top and bottom capacitors demonstrate identical rising slope, along with their fault currents (see Fig. 6.2(c-d)). Such difference allows the proposed detection method to differentiate the type of DC fault by examining the changing pattern of DC current and discharging current of DC-link capacitor.

6.1.3 Implementation

During steady state, the DC-link capacitor goes through recurring charging and discharging due to converter switching, while the DC current is constant and non-zero. When DC fault happens, the DC current and the capacitive discharge will have identical rising patterns and equal rate of change (ROC). Their ROCs will be compared, and the similarity is quantified in term of correlation coefficient.

Fig. 6.3 presents the process of computing the correlation coefficient. The windows denoted by $1, 2, 3...9$ contain fix-sized samples from rate of change of fault current ($ROC_{dc}(n)$) and that of capacitive discharge ($ROC_{cap}(n)$). Each window calculates the correlation coefficient, as represented by $R_1, R_2, R_3...R_9$, using (6.2). The correlation coefficient can range from -1 to 1. The DC fault is detected if it returns the correlation coefficient close to 1, while 0 means there is no matching at all. For example, the 5th window has the closest matching between ROC_{dc} and ROC_{cap}, thus it will generate $R_5 \approx 1$. Wrong detection can possibly happen in the 1st window as ROC_{dc} and ROC_{cap} have fairly similar pattern, even without noticeable sign of DC fault. To solve this, a threshold (ROC_{thr}) is set. The selection of ROC_{thr} will not be as rigorous

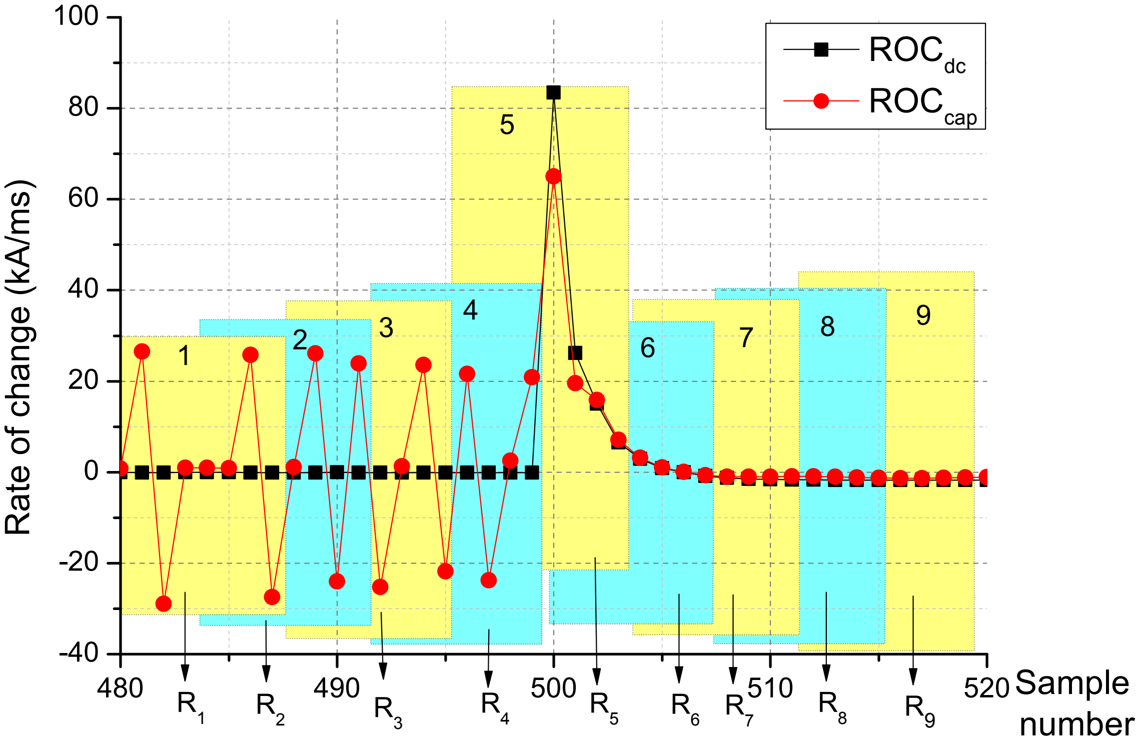


FIGURE 6.3: Computation of correlation coefficient between rate of change (ROC) of fault current and DC-link capacitive discharge.

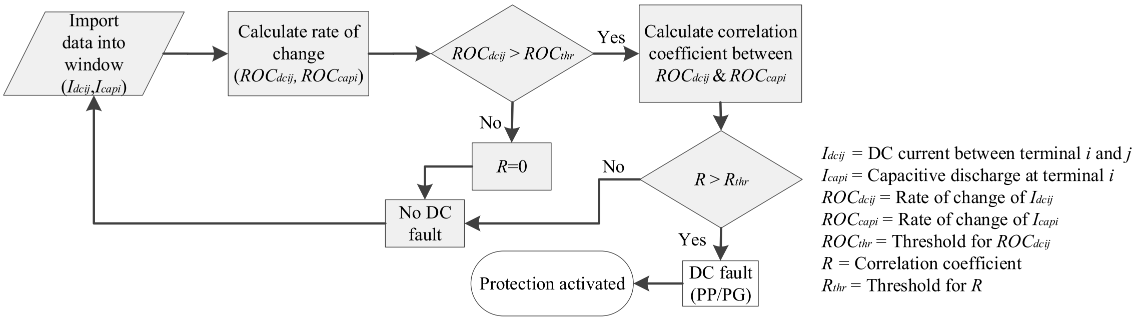
as in detection method based on current derivative. Rather, it is used to ensure that the calculation of correlation coefficient correctly captures the surge of fault current.

For an Intel® Core™ i5 CPU, the CPU time to output single sample is 41.43 μs on average. Hence, the proposed method has marginally higher CPU time than wavelet transform, which takes about 41.25 μs.

$$R = \frac{1}{N}\sum_{i=1}^{N}\left(\frac{ROC_{dc,i} - \mu_{ROC_{dc}}}{\sigma_{ROC_{dc}}}\right)\left(\frac{ROC_{cap,i} - \mu_{ROC_{cap}}}{\sigma_{ROC_{cap}}}\right) \tag{6.2}$$

where μ and σ are mean and standard deviation of the N windowed sample.

The working mechanism of the proposed method can be summarized in the flowchart shown in Fig. 6.4. The algorithm starts by loading data from the signal into window of pre-defined size. Within that window, the ROC of I_{dcij} and I_{capi} will be calculated. If the obtained ROC_{dc} is smaller than R_{thr}, the algorithm will return R=0 and interpret



I_{dcij} = DC current between terminal *i* and *j*
I_{capi} = Capacitive discharge at terminal *i*
ROC_{dcij} = Rate of change of I_{dcij}
ROC_{capi} = Rate of change of I_{capi}
ROC_{thr} = Threshold for ROC_{dcij}
R = Correlation coefficient
R_{thr} = Threshold for R

FIGURE 6.4: Flowchart of the proposed method.

it as no fault before proceeding to next window; if it is larger, there is a possibility that high ROC is caused by DC fault, the calculation of R between ROC_{dc} and ROC_{cap} will be executed thereafter. To illustrate the application of the algorithm on fault current, the signal from Fig. 6.2(a) is exported to MATLAB for calculation and the result is shown in Fig. 6.5. The algorithm registers a correlation coefficient close to 1 at the time when the $I_{dc}(+)$ and $I_{cap}(+)$ rise at the same rate, hence a DC fault is detected. This algorithm written in MATLAB takes 41.43 μs on average to generate the correlation coefficient.

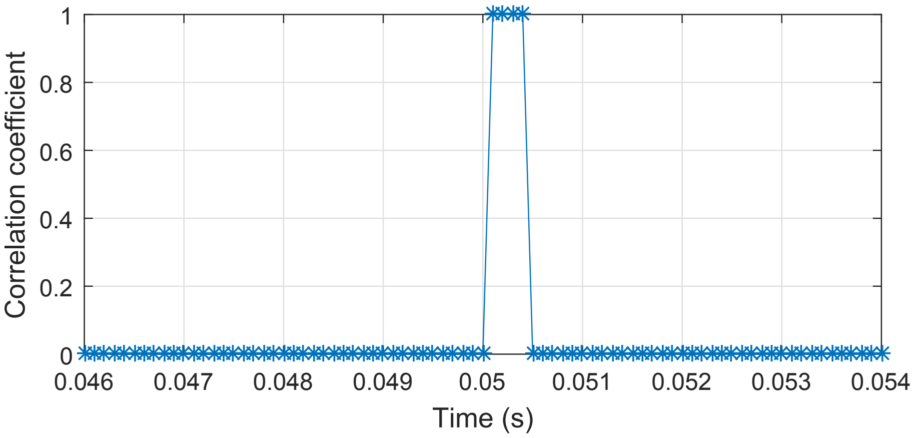


FIGURE 6.5: Computation of R for fault current during pole-to-ground fault.

In actual implementation, direct measurement of discharging current of DC-link capacitor is optional. ROC_{cap} is essentially equivalent to second derivative of voltage across DC-link capacitor, as described in (6.3). However, for the analysis in this thesis, the discharging current is directly measured.

$$\begin{aligned} ROC_{cap} &= \frac{\mathrm{d}I_{cap}}{\mathrm{d}t} \\ &= C_{dc}\frac{\mathrm{d}^2V_{cap}}{\mathrm{d}t^2}. \end{aligned} \tag{6.3}$$

6.2 Fault Analysis on Simulation Test System

The verification of proposed fault detection method starts off with a simple two-terminal VSC-based DC system simulation in PSCAD/EMTDC, as shown in Fig. 6.6. The parameters of the system model are listed in Table 6.1. The multi-terminal HVDC system, as depicted in Fig. 4.1b, will be used as the second test system providing us the results with even more diverse fault scenarios.

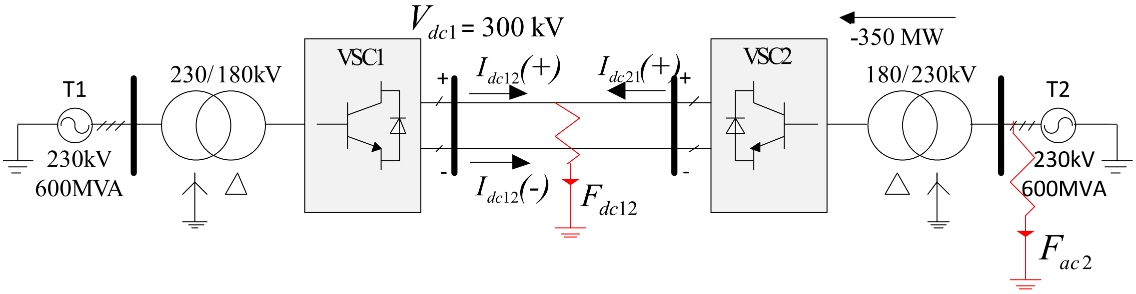


FIGURE 6.6: VSC-based DC system Simulation Model 1

TABLE 6.1: System data for VSC Simulation Model 1

System parameter	**Simulation model 1**
AC frequency	60 *Hz*
Number of terminals	2
Number of converter level	2 level VSC
DC-link capacitor	2000 μF
Switching frequency	1650 *Hz*
Sampling frequency	16.67 *kHz*
DC line	Overhead line (Detailed model) L12 = 200 km

6.2.1 VSC Simulation Model 1

The performance of the proposed fault detection method is firstly tested against the PG and AC fault at F_{dc12} and F_{ac2}. F_{dc12} is created by short circuiting the positive pole to ground, while F_{ac2} is a three-phase-to-ground fault. Assuming the DC currents from both $MMC1$ and $MMC2$ share similar fault behaviour, only the correlation coefficient of I_{dc12} is presented here.

6.2.1.1 Pole-to-ground Fault

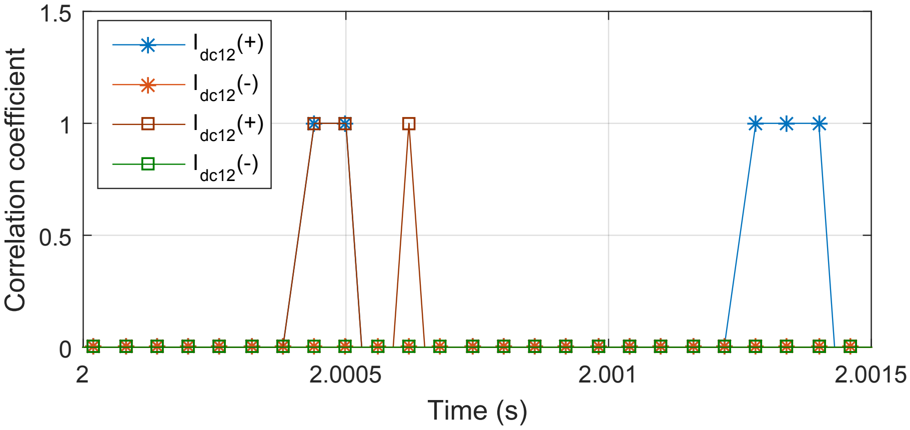


Figure 6.7: Correlation coefficient for pole-to-ground fault. * represents result for 0.1 Ω fault and □ represents 50 Ω fault.

There are two values of fault resistance used here: 0.1 Ω and 50 Ω. The result is shown in Fig. 6.7. The difference of correlation coefficient between positive and negative poles of I_{dc12} suggest that the fault is actually pole-to-ground. The first, highest correlation coefficients for both cases are obtained 0.46 ms after the fault inception. To take into account the time reflected wave needs to cause the DC current to increase, roughly 0.164 ms, the actual fault detection time can be worked out around 0.296 ms. It is important to highlight that the fault resistance has minimal influence on the sensitivity of this detection method, as the correlation coefficient remain at 1 going from 0.1 Ω to 50 Ω.

6.2.1.2 AC Fault

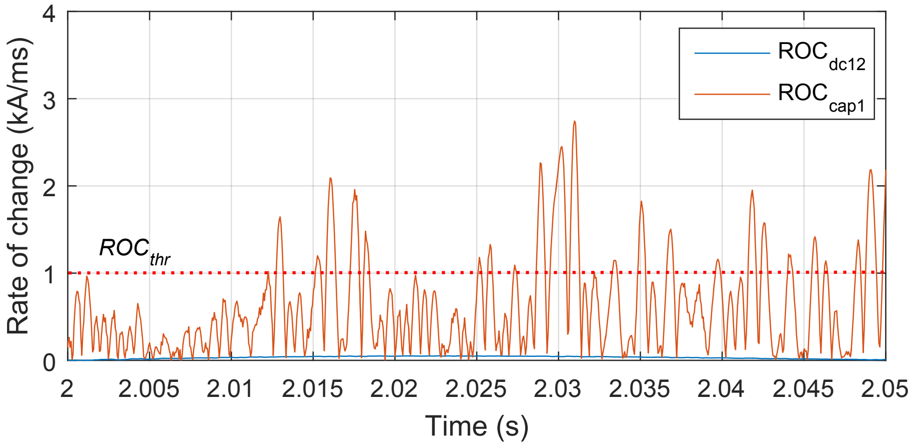


FIGURE 6.8: Rate of change of I_{dc12} and I_{cap1} during AC fault.

AC fault results in increasing DC current the same way as DC fault, except at relatively slower rate. For this reason, it is important for the capacitive discharge method to recognize this signature and discriminate in order to avoid wrong tripping.

A three-phase-to-ground fault denoted by F_{ac2} is simulated at 2.0 s. Fig. 6.8 shows the rate of change of I_{dc12} and capacitive discharge from $VSC1$. It can be seen that I_{dc12} and I_{cap1} are not behaving in identical manner. Because the threshold (ROC_{thr}) is not crossed, the detection algorithm will go back to the starting and generate the correlation coefficient at 0. (revisit Fig. 6.4). Three-phase-to-ground fault is considerably the most severe among all types of AC fault; if the capacitive discharge method is able to discriminate against three-phase-to-ground fault, it would suffice to justify that it can work for all types of AC fault as well.

6.2.1.3 Sudden blocking of gate signal

VSC2 is suddenly given a block signal amid steady state at 2.0 s. The result is shown in Fig. 6.9. As with AC fault, this event does not cause the I_{dc21} to record a ROC higher than the threshold, hence the correlation coefficient will be just equal to 0. As

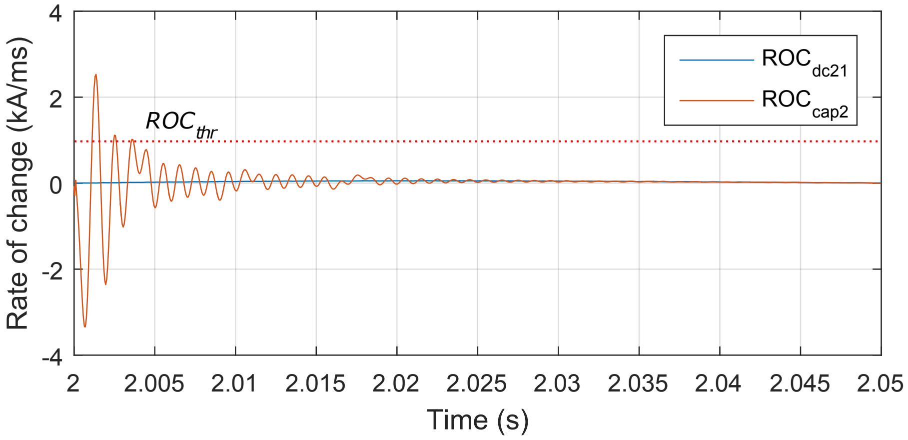


FIGURE 6.9: Rate of change of I_{dc12} and I_{cap1} when VSC2 is suddenly blocked.

the converter has stopped operation, I_{dc21} and I_{cap2} eventually come to zero, as well as ROC_{dc21} and ROC_{cap2}. It is demonstrated that the detection fidelity of the proposed method is not compromised by sudden blocking of gate signal.

6.2.2 Simulation Model 2

For MMC, the DC-link capacitor can be used to serve for filtering purpose [82–84], but it may increase the fault current if the value is too large [85]. Fig. 6.10 shows the effect of adding the DC-link capacitor of 1 μF at each MMC terminal on the DC current (I_{dc12}) during fault F_{dc12}. One can notice that the difference between the cases with and without DC-link capacitor is small, if not negligible. At the instant of fault, the capacitive contribution in the current causes the slope to be slightly steeper. Nevertheless, the capacitive discharge-based fault detection can be realized in MMC without significantly increasing the overall fault current.

The fault location (D_f) is the distance of the fault from the monitoring terminal. There are two types of power system disturbance simulated here: pole-to-pole fault and bus fault. The result is summarized in Table 6.2.

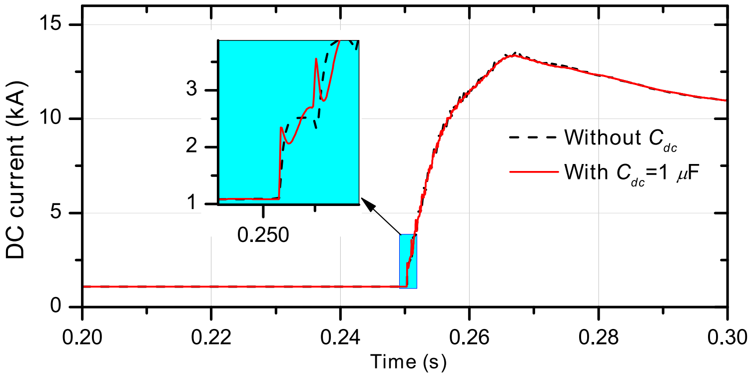


FIGURE 6.10: DC current (I_{dc12}) during fault F_{dc12} with and without DC-link capacitor of 1 μF.

TABLE 6.2: Correlation coefficient for DC fault under varying fault location and resistance.

Fault	**Location**	**Resistance (Ω)**	***R***						**Fault detected?**
			I_{dc12}	I_{dc21}	I_{dc23}	I_{dc32}	I_{dc34}	I_{dc43}	
F_{dc12}	100 km from MMC1	0.1	0.9902	0.9980	0.4396	0.3941	0	0	Yes
	100 km from MMC1	50	0.9914	0.9981	0.6682	0.3733	0	0	Yes
	100 km from MMC1	200	0.9910	0.9987	0	0.3712	0	0	Yes
F_{dc23}	25 km from MMC2	0.1	0.8262	-0.1950	0.9671	0.9661	0.8141	0.7005	Yes
	40 km from MMC2	0.1	0.7294	0.5182	0.9962	0.9755	0.3351	0.7420	Yes
	70 km from MMC2	0.1	0.7350	0.4820	0.9953	0.9883	0.3908	0.7406	Yes
	90 km from MMC2	0.1	0.6707	0.4483	0.9953	0.9755	0.6557	0.7204	Yes
	100 km from MMC2	10	0.7593	0.4401	0.9938	0.9941	0.4393	0.7515	Yes
F_{dc34}	100 km from MMC3	1.0	0	0	0.3908	0.4414	0.9982	0.9912	Yes
	100 km from MMC3	100	0	0	0.3820	0.4640	0.9981	0.9912	Yes
F_{dc3}	0 km from MMC3	0.1	0.6934	0.4292	0.9541	1.0	1.0	0.9648	Yes

6.2.2.1 Influence of Fault Resistance

The fault resistance are varied from 0.1 Ω to 200 Ω and the fault is randomly applied on different lines. F_{dc12}, F_{dc23} and F_{dc34} at $D_f = 100km$ are effectively detected, for the currents of the affected line record the R above threshold. It is also worth-noting that the detection sensitivity does not drop significantly with increasing fault resistance.

6.2.2.2 Influence of Fault Distance

The proposed fault detection method is tested for the PP fault (F_{dc23}) at different locations along $L23$ ($25 < D_f < 100km$ from $MMC2$). In this case, the two currents of interest here are I_{dc23} and I_{dc32}. Table 6.2 shows that these two currents have the correlation coefficient exceeding threshold while other currents do not show any conclusive sign of DC fault with sufficiently low correlation coefficient. The fault location does not seem to impair the sensibility of the proposed method in providing the right response.

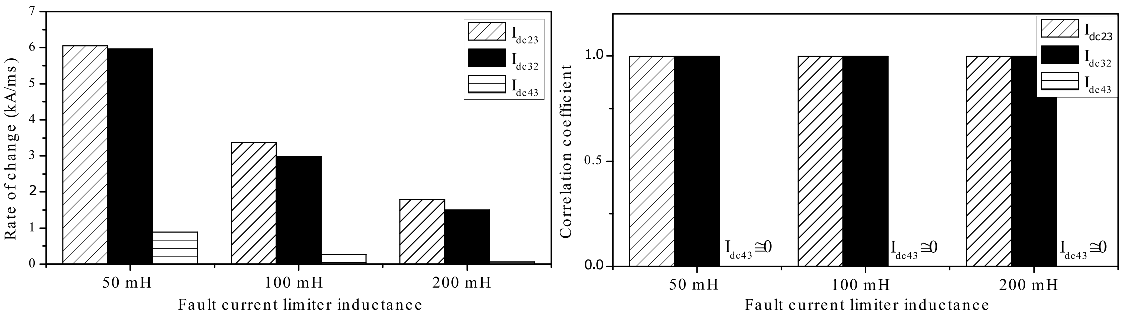
6.2.2.3 Bus Fault

From Table 6.2, it is interesting to note that both line currents of $MMC3$ record $R = 1$. This implies that the breakers at $MMC3$ will have to trip, and rightfully so. I_{dc23} and I_{dc34} see the correlation coefficient exceeding threshold, thus the corresponding circuit breakers will trip accordingly.

6.2.2.4 Employment of Fault Current Limiter

It has been demonstrated that the capacitive discharge method is able to detect almost every faulty situation. Consider the cases when F_{dc23} or F_{dc34} happen almost at the bus bar of *MMC3*, because there is no electrical distance between the two faults as perceived by *MMC2* and *MMC4*, both terminals would end up dispatching the tripping signal simultaneously like the case of F_{dc3}. In order to provide selectivity under this challenging condition, inductive fault current limiter (FCL) can be used to separate between two nearby faults as seen from the two terminals. In this subsection, the performance of capacitive discharge method will be evaluated with the inductive FCL integrated into the simulated system. In addition, the comparison between *di/dt* and capacitive discharge methods will be presented.

Fig. 6.11 shows the result of *di/dt* and capacitive discharge methods for F_{dc23} located very close to *MMC3*. Using 50 mH as the base case, the inductive FCL is varied to investigate each method's sensitiveness to DC fault. With the introduction of inductive FCL, *MMC2* and *MMC3* are now able to independently detect the fault. The rate of change of I_{dc43} is largely lower than that of I_{dc23} and I_{dc32}, making it possible for *MMC4* to recognize that the fault is outside its protection zone. While the *di/dt* method can identify the faulted line, the threshold value is dependent on the size of inductive FCL. The correlation coefficient of fault current, on the other hand, remains consistently high for all cases. Not only does the capacitive discharge method provide reliable detection, it eliminates the need of finding new threshold for different value of FCL.

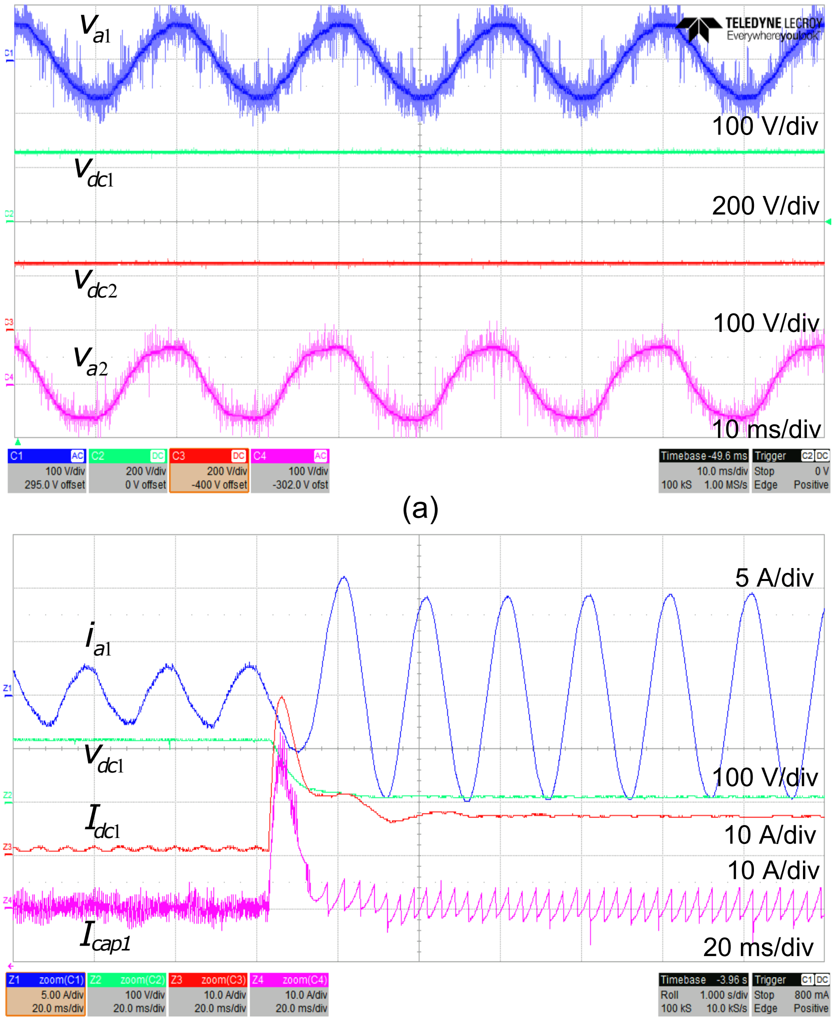


(a) (b)

FIGURE 6.11: Effect of inductive FCL size on (a) *di/dt* method and (b) capacitive discharge method.

6.3 Fault Analysis on Experimental Test System

The experimental studies are performed at an operating voltage of 85 V (line rms) and corresponding steady state result is shown in Fig. 6.12. Voltage v_{a1}, DC voltages v_{dc1}, v_{dc2} (maintained at 120 V) and v_{a2} maintained at 70 V (phase peak) are shown in the figure. DC PP fault via a fault resistance (R_f) of 2 Ω is performed and the result is shown in Fig. 6.12. Current i_{a1} increases to large value and v_{dc1} falls to almost zero after the fault. Current I_{dc1} and I_{cap1} increase simultaneously, as the DC-link capacitor releases charges through the fault path.



(a)

(b)

FIGURE 6.12: Experimental results (a) Steady state voltage v_{a1}, v_{dc1}, v_{dc2}, v_{a2}; (b) DC pole-to-pole fault with R_f=2 Ω, i_{a1}, v_{dc1}, I_{dc1}, I_{cap1}.

The power resistor acting as the short-circuit fault is connected in the middle of DC line. The fault location can be artificially varied by changing the inductance values. For each location, the resistor ranging from 2 Ω to 10 Ω will be used. The DC line inductance in 5.11 is adjusted to emulate different fault location. Some of the locations are considered as follows:

- *Location 1*: $L1, L2, L3, L4 = 1.5$ mH
- *Location 2*: $L1, L3 = 1.5$ mH; $L2, L4 = 2.8$ mH
- *Location 3*: $L1, L3 = 4.0$ mH; $L2, L4 = 1.5$ mH
- *Location 4*: $L1, L2, L3, L4 = 4.0$ mH

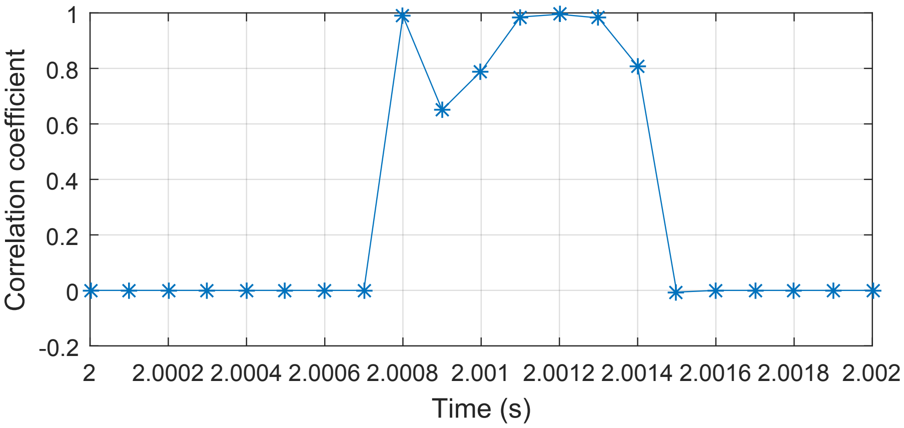


FIGURE 6.13: Correlation coefficient for experimental DC fault with R_f=2 Ω.

The DC currents and capacitive discharge are monitored and used to compute the correlation coefficient.The result for I_{dc1} and I_{cap1} is shown in Fig 6.13. The short-circuit is set to occur at 2 s. As one can clearly observe, the proposed fault detection method is able to capture the DC fault with the correlation coefficient achieving close to 1.

6.3.0.1 Influence of Fault Resistance

Fig. 6.14 shows the correlation coefficient between I_{dc1} and I_{cap1} for the DC fault with R_f=4∼10 Ω. In all cases, the correlation coefficients close to 1 are obtained within 1 ms after the fault inception, inferring that the DC fault can be detected very quickly. Even with the increasing fault resistance, the correlation coefficient consistently remain at high value. Besides that, the result shows no indication of delayed detection time

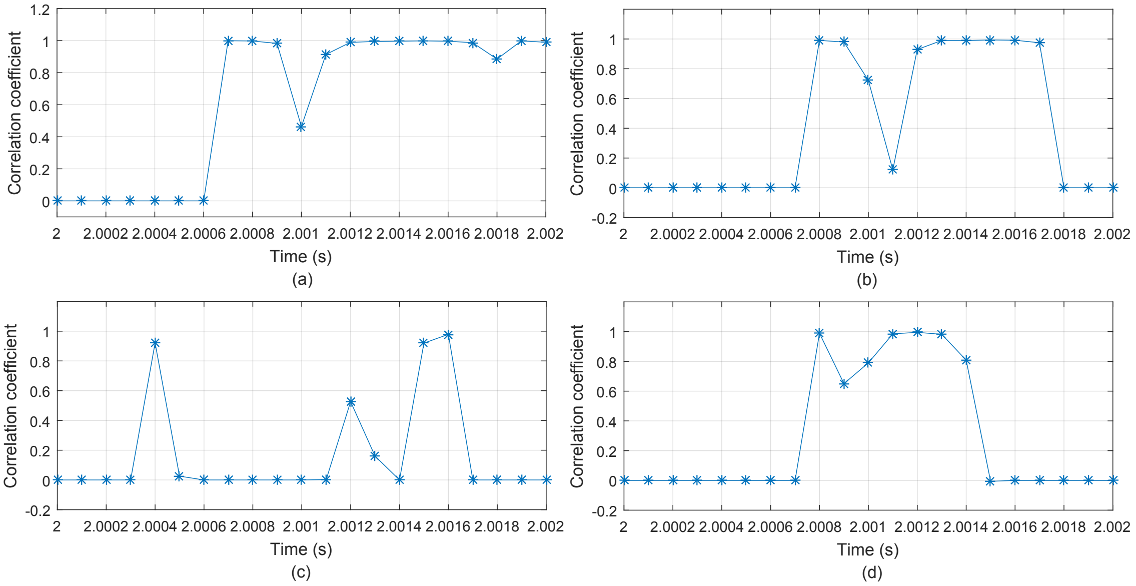


FIGURE 6.14: Correlation coefficient for experimental DC fault with various fault resistance. (a)R_f=4 Ω; (b)R_f=6 Ω; (c)R_f=8 Ω; (d)R_f=10 Ω.

due to the dampened fault-induced transient. This suggests that the influence of fault resistance does not affect the sensitiveness of the proposed fault detection method.

6.3.0.2 Influence of Fault Distance

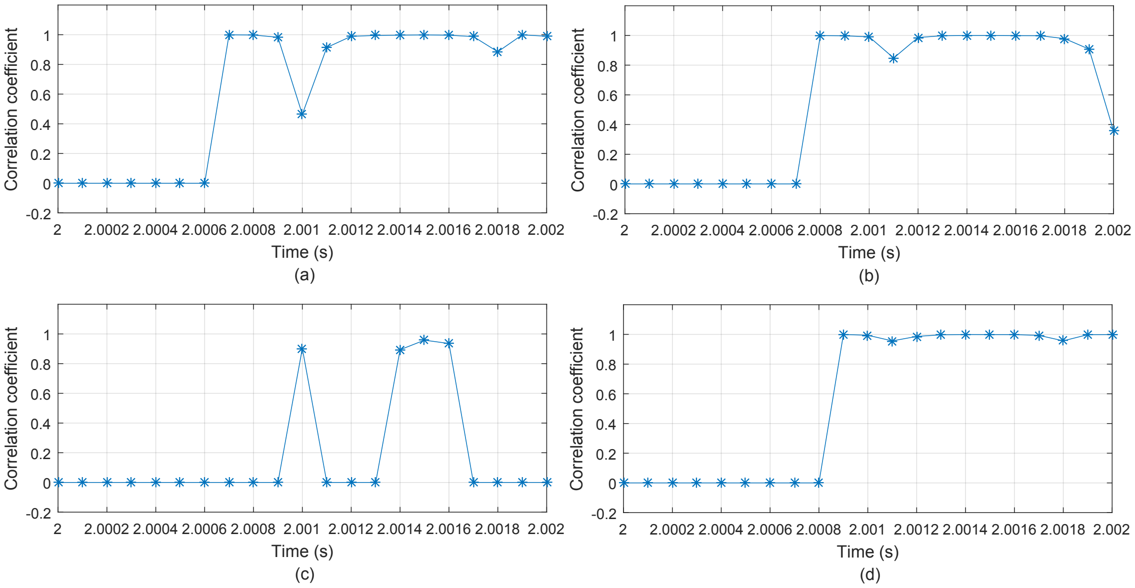


FIGURE 6.15: Correlation coefficient for experimental DC fault with various fault resistance. (a)Location 1; (b)Location 2; (c)Location 3; (d)Location 4.

The influence of fault distance on the capacitive discharge-based fault detection method is illustrated in Fig. 6.15. As expected, the DC fault yields high correlation coefficients in all locations. It is observed that high speed detection is achievable within 1 ms. Location 3 and 4 are the locations where the fault is the furthest away from $VSC1$, however the correlation coefficients do not decline substantially compared to the other cases. To that end, it is fair to say that the proposed fault detection method can make reliable fault decision without being influenced by the fault distance

6.4 Summary

The understanding of transient caused by DC-link capacitive discharge allows us to propose a novel DC fault detection method in this thesis. From the perspective of implementation, it is a simple way to detect the DC fault in a multi-terminal DC system. It makes use of the DC-link capacitor discharge, which is inherently a natural phenomenon of the DC fault, as an indicator of fault occurrence. The correlation coefficient is used to gauge the similarity between the rising patterns of DC line current and DC-link capacitive discharge. Its value ranges from -1 to 1. When DC fault happens, one should expect high correlation coefficient approaching 1, implying the possibility of DC-link capacitive discharge injecting into the DC current of faulted line.

The proposed fault detection method is validated by simulation and experiment. It is observed that the method can detect the DC fault within 1 ms on average. The fault-induced transients can change under different fault condition, however the sensitivity of this method does not drop significantly caused by the influence of fault location, resistance and distance. The correlation coefficient consistently stays above 0.90 in all cases. With the proposed method, DC bus fault can be effectively detected as well.

It is also demonstrated how DC fault can be differentiated from AC fault, such as three-phase-to-ground fault, and sudden blocking of gate signal using this method. The employment of inductive fault current limiter for the purpose of improving the selectivity of the proposed method is presented. The correlation coefficient does not need a new threshold to adapt to different operating condition, as opposed to di/dt method.

Chapter 7

STFT-based Fault Detection

7.1 Introduction

It has been widely recognized that wavelet transform is a well-established technique to analyze non-periodic and non-stationary signal, such as fault transient in voltage and current. It offers variable window size without the risk of compromising time-frequency resolution. However, the frequency-domain analysis in the wavelet transform is represented by detailed coefficients which cannot provide precise frequency content information. Short time Fourier Transform (STFT), on the other hand, operates over a fixed window length which can provide precise frequency content information for a specified window size. It is relatively not a favorable candidate due to its poor time-frequency resolution; wide window gives finer frequency resolution but bad time resolution, and vice versa. However, for the application of transient and fault signal analysis, STFT can be used, granted, certain degree of compromise is allowed. Detection speed is of utmost importance in this case, thus the time resolution should be prioritized over frequency.

In this chapter, a novel fault detection method based on STFT is proposed. As with wavelet-based method, the moving fault signal will be decomposed into chunk of predefined sample size and screened using a window function. The signal is then represented in the frequency domain to observe the spectral pattern. The advantage of this method is that it is resilient to the magnitude and rate of change of fault current, which can variably change for different fault resistance and location. Rather, it depends highly on the rising pattern of the fault current. The performance of this method will be evaluated on simulation and experimental results.

7.1.1 Theory

STFT is a variation of Fourier Transform (FT) incorporating a real and symmetric window function $w(t)$. Mathematically, the continuous STFT of a function $f(t)$ can be written in (7.1).

$$F(\tau,\omega) = \int_{-\infty}^{+\infty} f(t)w(t-\tau)e^{-j\omega t}dt. \tag{7.1}$$

where τ=time axis and ω=frequency axis.

The equation above infers that STFT performs frequency analysis (ω) in local section of signal as it changes over time (τ). In other words, it does not only tell which frequency is present in a signal but also in which time interval the frequency emerges. Because fault signal evolves in time in an unpredictable way, STFT is suitable for examining the change of frequency content as a result of fault.

To implement discrete version of STFT, the signal will be sampled with fixed sampling frequency and treated with discrete Fourier transform (DFT), which can be efficiently computed using fast Fourier transform (FFT) algorithm. Thus, (7.1) can be modified in discrete space yielding (7.2).

$$X[m,k] = \sum_{n=0}^{N-1} x[n]w[n - mH]e^{-i\frac{2\pi nk}{N}}, \tag{7.2}$$

where N=the number of FFT points, m=position of window, k=frequency index and H=hop size between successive windows.

There are several parameters that determine the property of STFT:

1. *Sampling frequency (f_s)*: High f_s means more samples available for STFT analysis, contributing to better time and frequency resolution.
2. *Number of FFT points (N)*: N is typically at the power of 2. It reflects the frequency resolution in the STFT output.
3. *Type of window function ($w(n)$)*: Different window functions have their unique frequency spectrum. For the application of fault detection, Hanning window is utilized.
4. *Window length*: Window length is proportional to the time resolution in the STFT output. As far as fault detection time is concerned, small window length is recommended. The length is typically at the power of 2.
5. *Hop size (H)*: H determines how much proportion of a window is overlapped with the successive one as it slides. Small H effectively helps to improve the time resolution. Here, H is chosen to be 2 samples.

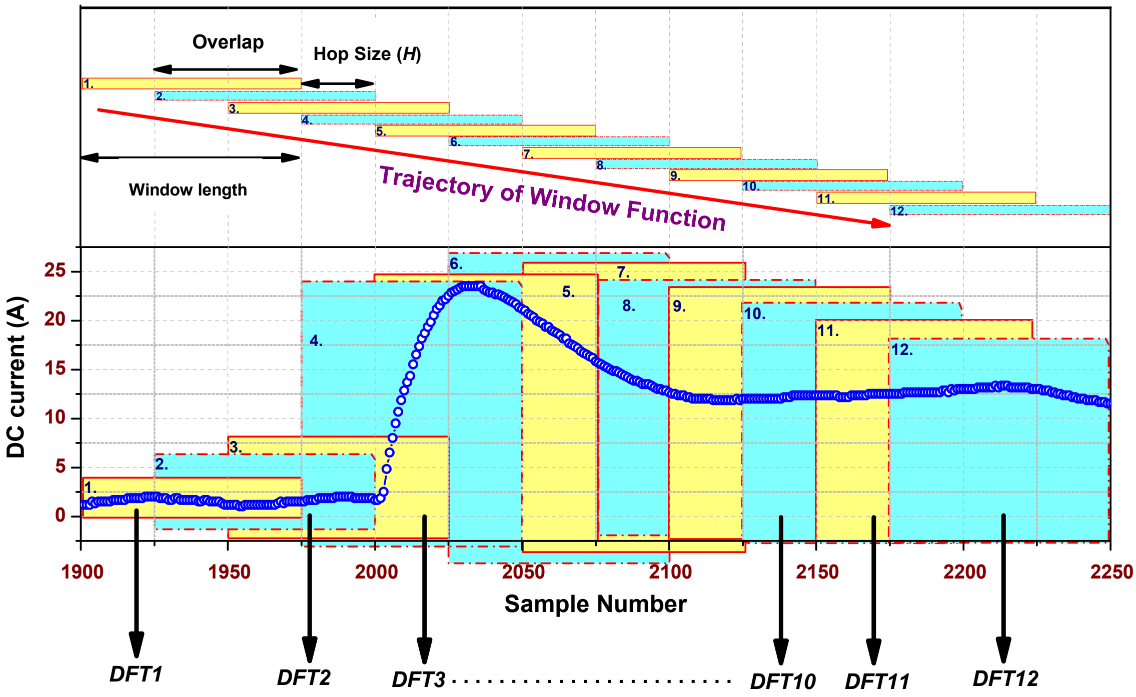


Figure 7.1: Computation of STFT on fault signal.

7.1.2 Fault Detection by STFT

Fig. 7.1 illustrates the operation of STFT on fault signal. A number of samples according to window length is captured and read into a window. In that window, the samples will be multiplied with window function (w_n), subsequently proceeding to computation of DFT. After that, the window is hoping to successive set of sample by H and DFT is computed again. The process repeats until it reaches the end of signal. The windows are denoted by $1, 2, 3...12$ and the corresponding outputs are $DFT1, DFT2, DFT3...DFT12$.

During normal operation, the DC current $i_{dc}(t)$ is presumably constant. Hence, the STFT of I_{dc} using rectangular window $(w(n) = 1)$ can be written as follows:

$$\begin{aligned} |I_{dc}(\omega)| &= \left| \int_{-\tau/2}^{\tau/2} i_{dc}(t) e^{-j\omega t} dt \right| \\ &= I_{dc} \left| \frac{sin(\omega\tau/2))}{\omega\tau/2} \right|. \end{aligned} \tag{7.3}$$

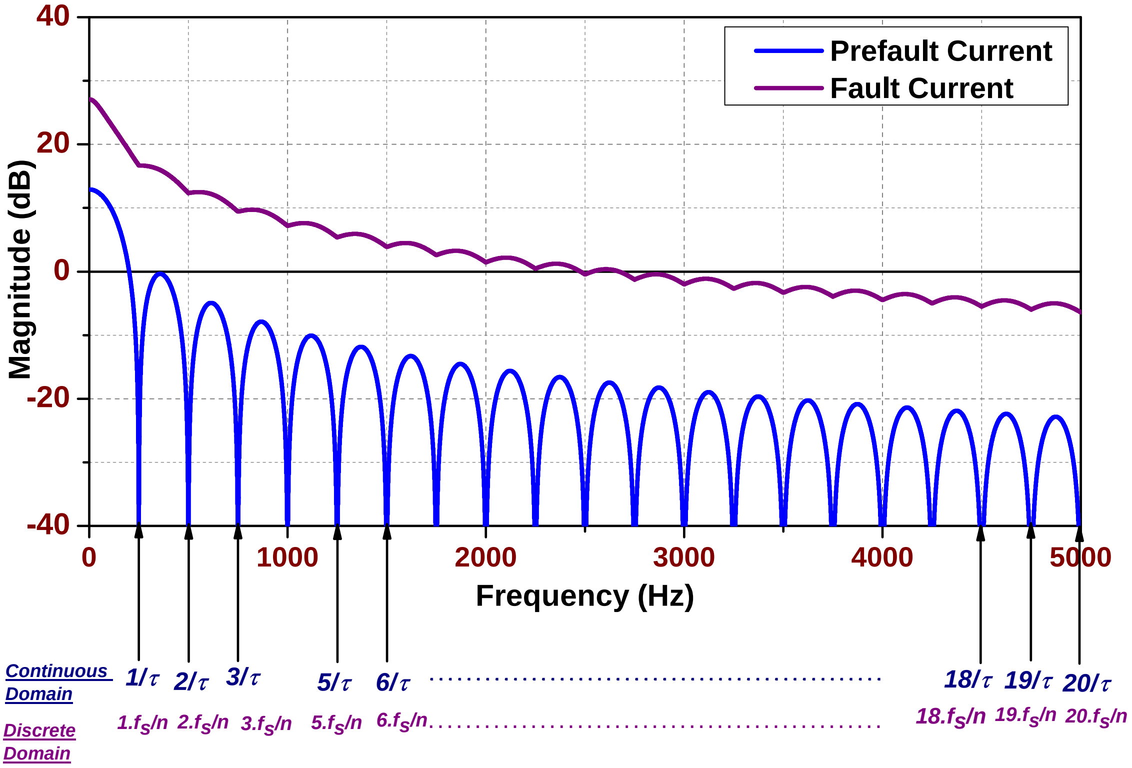


FIGURE 7.2: Frequency spectrum of pre-fault and fault signal.

It can be seen that the frequency spectrum of pre-fault current essentially resembles a *sinc* function. As shown in Fig. 7.2, it has the main-lobe with peak at a value depending on steady state DC current, and side-lobes that decrease in magnitude as it goes along with increasing frequency. The *sinc* function crosses zero periodically at frequencies denoted by $1/\tau$, $2/\tau$, $3/\tau ... 20/\tau$, or known as zero-crossing frequency bin. As for fault current, replacing $i_{dc}(t)$ in (7.3) with $I_f(t)$ from (3.37) will take the form:

$$\begin{aligned} |I_f(\omega)| &= \left| \int_0^{\tau/2} I_f(t) e^{-j\omega t} dt \right| \\ &= \left[\left(\frac{(Ae^{m_1\tau} - 1)m_1}{m_1^2 + \omega^2} + \frac{(Be^{m_2\tau} - 1)m_2}{m_2^2 + \omega^2} \right)^2 + \omega^2 \left(\frac{Ae^{m_1\tau} - 1}{m_1^2 + \omega^2} + \frac{Be^{m_2\tau} - 1}{m_2^2 + \omega^2} \right) \right]^{1/2} . \end{aligned} \tag{7.4}$$

In (7.4), one can notice that $I_f(\omega)$ is not necessarily zero at zero-crossing frequency bin. The resulting frequency spectrum is now shifted upward, indicating that the fault-induced transient has injected high frequency content into the signal. The frequency spectrum of fault current in Fig. 7.2 is obtained from DFT computation of 4th window in Fig. 7.1. The transition from pre-fault to fault demonstrates change in the frequency spectrum, one observable sign is the increased magnitude at each zero-crossing frequency bin. Using this as an indicator, we will thus be able to design a fault detection method.

7.1.3 Selection of Window Length

The analysis thus far only touches on the DC current with non-existing harmonics, which sees the frequency spectrum with signal energy focused in the main lobe near 0 Hz and the side lobes are uniformly distributed, resembling the *sinc* function. However, in the DC system based on 2-level VSC, the harmonics in DC current can no longer be neglected. For instance, 6th harmonic appears in DC current due to the conduction pattern of three-phase switches [98]. As a result, the frequency spectrum will reflect that by having increased side lobe magnitude near 360 Hz (or 300 Hz for 50 Hz AC system). Since the fault detection method proposed here assumes that the first few zero-crossing frequency bin should remain low during normal operation, it is important to choose the window length whose zero-crossing frequency bin does not coincide with the harmonics.

Table 7.1 shows how the zero-crossing frequency bin can be calculated given the window length for $f_s = 10kHz$. The first three zero-crossing frequency bins occur at $2f_s/n$, $3f_s/n$ and $4f_s/n$. It is evident that shorter window length is correlated with coarser frequency resolution.

Table 7.1: Zero-crossing frequency bins for various window length

Window length	$\mathbf{2}f_s/n$	$\mathbf{3}f_s/n$	$\mathbf{4}f_s/n$
16	1250 Hz	1875 Hz	2500 Hz
32	625 Hz	937.5 Hz	1250 Hz
64	312.5 Hz	468.75 Hz	625 Hz
128	156.25 Hz	234.375 Hz	312.5 Hz
256	78.125 Hz	117.1875 Hz	156.25 Hz
512	39.0625 Hz	58.59375 Hz	78.125 Hz

To illustrate the problem with clarity, Fig. 7.3 shows the simulation result of load change in the 2-level VSC-HVDC system. The DC current contains the ripple of 6th harmonic, with peak-to-peak about 5 A before load change and 7 A after load change. The result is post-processed with STFT to see how the frequency spectrum changes when the 6th harmonic is introduced.

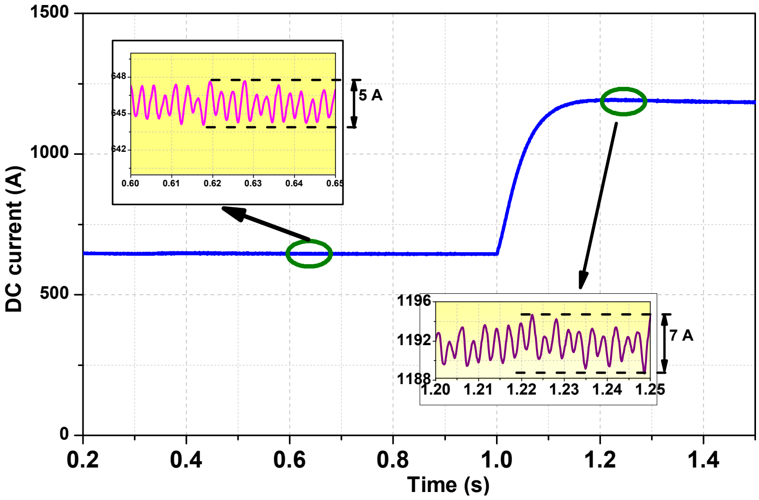


Figure 7.3: Frequency spectrum of DC current with 6th harmonic.

Fig. 7.4 shows the frequency response of the DC current using the window lengths as given in Table 7.1. In the frequency spectrum for 64 samples window length, the first zero-crossing frequency bin, which is at 312.5 Hz, exceeds 0 dB. The fault detection would result in wrong judgment if this window length were to be chosen. Other window lengths are relatively suitable, since the influence of 6th harmonic does not reach near their first zero-crossing frequency bins. However, 32-sample is the ideal window length as 625 Hz is considerably the safest frequency bin that provides enough margin away from all the possible characteristic harmonics in DC current.

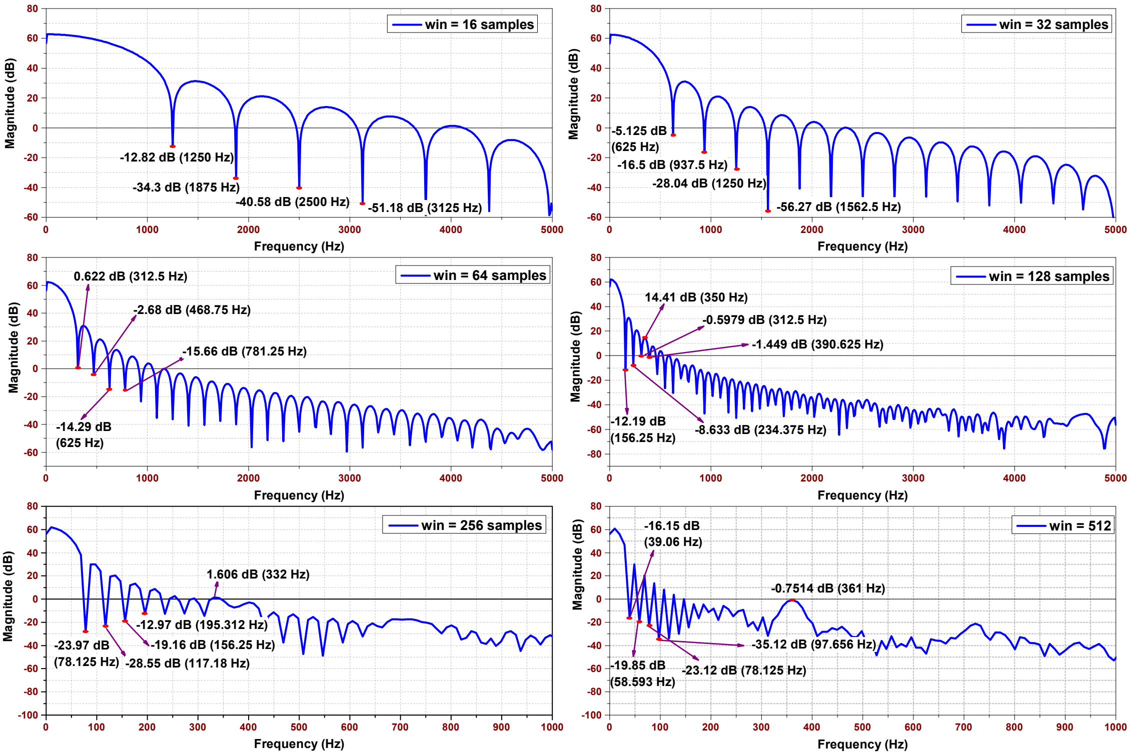
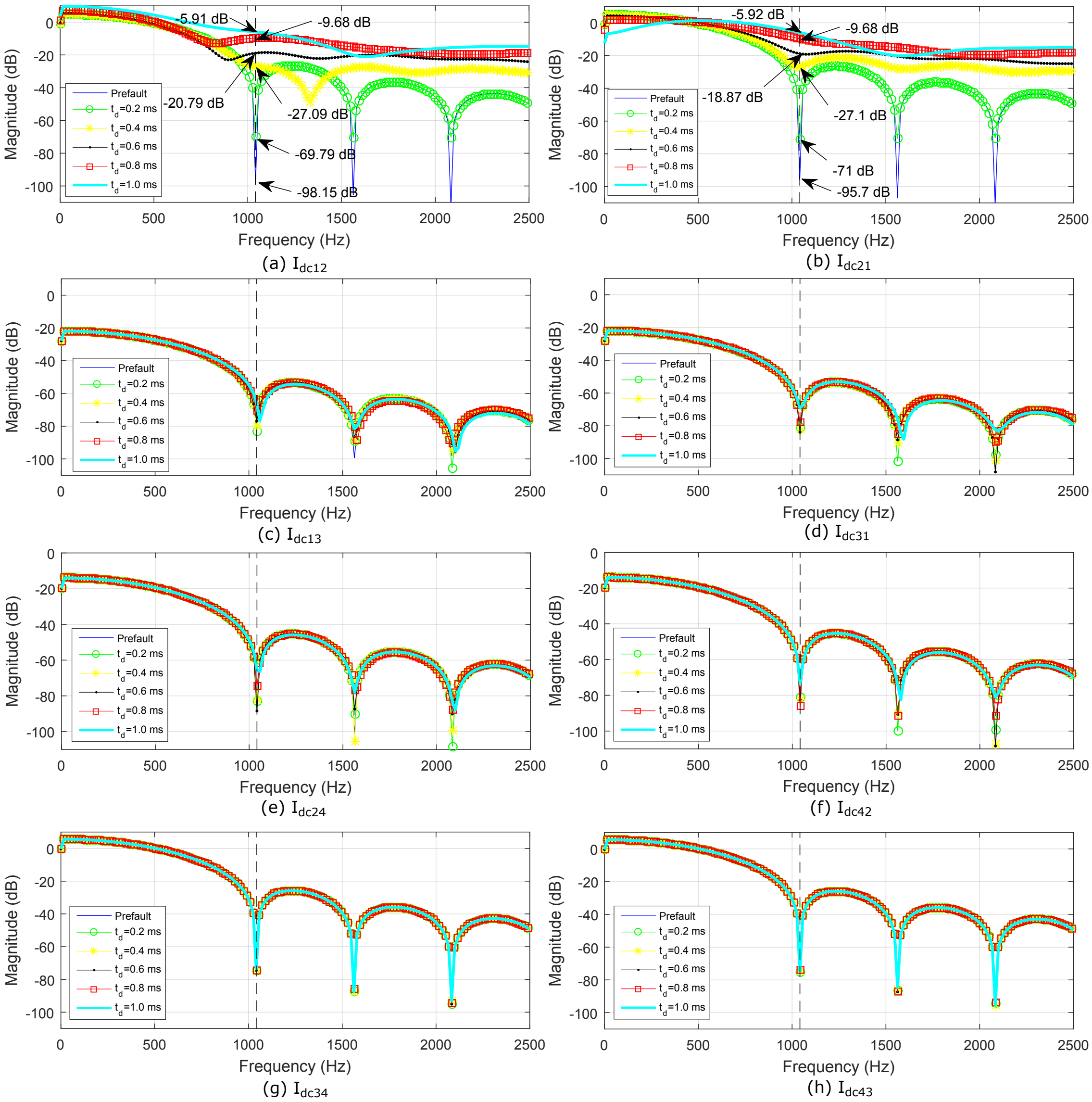


Figure 7.4: Frequency spectrum of DC current for various window length.

7.2 Fault Analysis on Simulation Test System

The STFT-based fault detection is firstly tested on Simulation Model 1 (see Fig. 4.1a). The PP fault F_{dc12} with R_f=0.1 Ω is used as the base case. The signals required are the DC currents $(Idc_{ij}, i, j = 1, 2, 3, 4)$ measured at each terminal$(MMCi)$, and they will be post-processed with the code given in Appendix F. Following the discussion in previous section, the Hanning window with length of 32 samples is chosen. The STFT will be given the parameters such as f_s=16666.67 Hz, N=1024 samples and H=2.

The result in Fig. 7.5 shows how the frequency spectrum for each DC current evolves under the influence of the DC fault. The detection time delay is denoted by t_d. For I_{dc12}



(a) I_{dc12} (b) I_{dc21}

(c) I_{dc13} (d) I_{dc31}

(e) I_{dc24} (f) I_{dc42}

(g) I_{dc34} (h) I_{dc43}

FIGURE 7.5: Frequency spectrum of DC current during DC fault on $L12$. The first zero-crossing bin is represented by dash line.

and I_{dc21}, it is observed that the first zero-crossing frequency bin (1042 Hz) only begins to experience increased magnitude after t_d=0.2 ms. The DC fault can be detected at t_d=0.8 ms when the zero-crossing frequency bin exceeds -10 dB. Other currents, which are not affected the DC fault, show a completely different trend. The shape of side lobes remain equiripple-like through 10 ms after the fault inception. In addition, the zero-crossing frequency bin appears to be undistorted showing no sign of fault on their associated DC line. With the result, it is demonstrated how the STFT-based fault detection method can identify the faulted line in a multi-terminal system and work locally at each terminal.

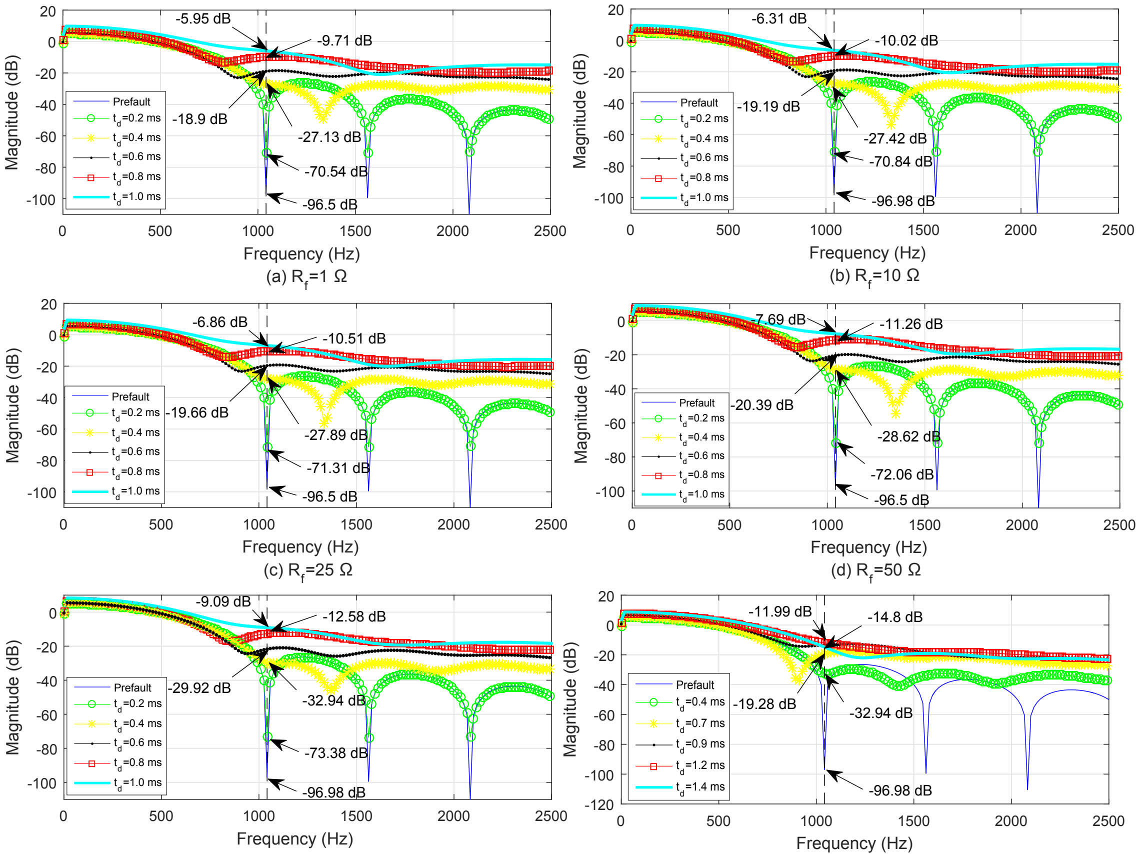
For the analysis that follows, the threshold will be benchmarked at -10 dB. If the first zero-crossing frequency bin crosses this threshold, it will be considered that the fault is successfully detected. To determine how far this threshold can be used as a valid fault criterion, the analysis will look at various fault parameters:

- To study the influence of DC fault resistance: PP fault on $L12$, $1 < R_f < 250\Omega$, $D_f = 50km$, $f_s = 16666.67Hz$.
- To study the influence of DC fault distance: PP fault on $L12$, $R_f = 0.1\Omega$, $15 < D_f < 85km$, $f_s = 16666.67Hz$.
- To study the influence of AC fault: Three-phase-to-ground on AC side of $MMC2$, $R_f = 0.1\Omega$, $f_s = 16666.67Hz$.
- To study the function of fault current limiter: PP fault on $L12$ (radial network), $R_f = 0.1\Omega$, $D_f =$ close to Bus 1, $f_s = 16666.67Hz$.

7.2.1 Influence of Fault Resistance

Fig. 7.6 presents the STFT analysis of I_{dc12} for DC fault resistance 1 Ω, 10 Ω, 25 Ω, 50 Ω, 100 Ω and 250 Ω. Similarly, we focus on the first zero-crossing frequency bin and significantly increase in its magnitude is seen in all cases.

Using the threshold -10 dB, the DC fault can be detected at t_d=1 ms except R_f=250 Ω, in which case the maximum magnitude obtained at t_d=1.2 ms is only -11.99 dB, slightly below the threshold. The decreased magnitude can be explained by the fact that the high resistance fault, for the most part, damps the rising slope of fault current,



(a) R_f=1 Ω

(b) R_f=10 Ω

(c) R_f=25 Ω

(d) R_f=50 Ω

(e) R_f=100 Ω

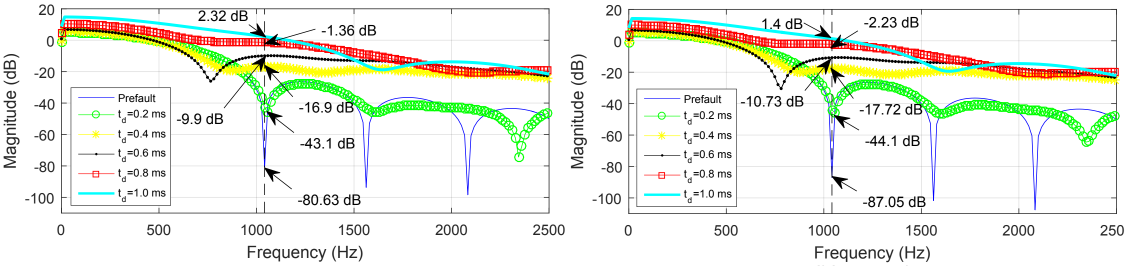
(f) R_f=250 Ω

FIGURE 7.6: Frequency spectrum of I_{dc12} for DC fault with various fault resistance.

reducing the injection of high frequency content into signal. Nevertheless, the dynamic of frequency spectrum transitioning from pre-fault to fault is still consistent with what has been observed in fault cases. The detection would succeed if we stretched the threshold to accommodate the high resistance fault.

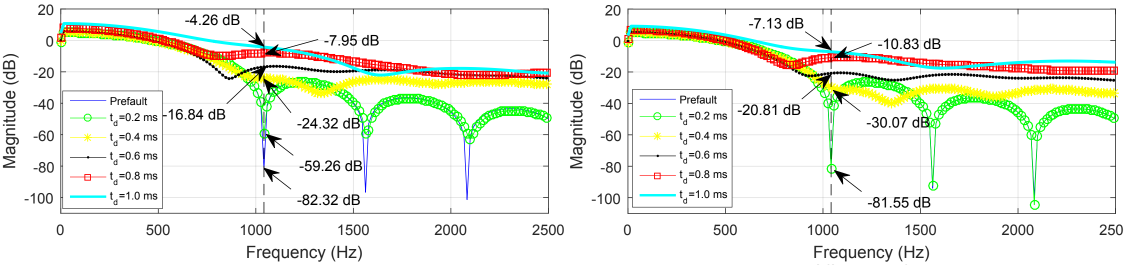
7.2.2 Influence of Fault Distance

The DC fault F_{dc12} is shifted along $L12$. The distance between the fault and $MMC1$ is represented by D_f. In this analysis, 6 cases of D_f are considered, such as 15 km, 20 km, 40 km, 60 km, 70 km and 85 km. The D_f influences the transient in fault current, thus it will be of our interest to evaluate the sensitiveness of STFT-based method to this effect.



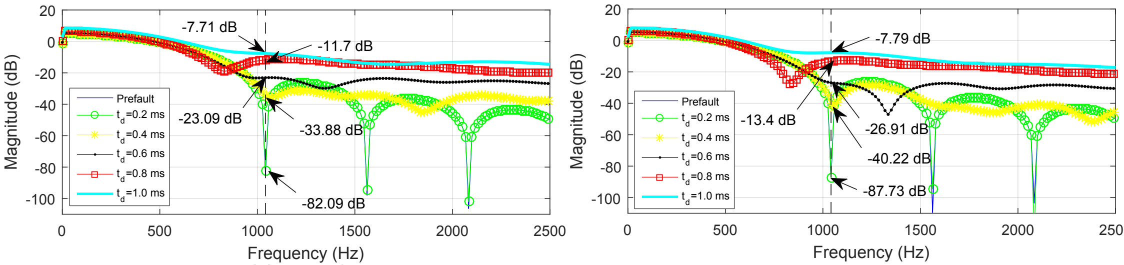
(a) Df=15 km

(b) Df=20 km



(c) Df=40 km

(d) Df=60 km



(e) Df=70 km

(f) Df=85 km

FIGURE 7.7: Frequency spectrum of I_{dc12} for DC fault with various fault distance.

The result is given in Fig. 7.7. The frequency spectrum starts showing distortion from t_d=0.4 ms onward. The first zero-crossing frequency bin exceeds the threshold at various time depending on the D_f. For the DC fault closest to $MMC1$, the fault can be identified as immediate as t_d=0.6 ms. The further away is the fault, the more time delay it takes to reach the threshold. Such trend is in line with the way traveling wave behaves, whereby the propagation time of reflected wave caused by fault is directly proportional to the fault distance. With the increase of D_f, the fault-induced transient suffers increasing attenuation, resulting in dampened high frequency content into the signal. Some adjustment can be made to the threshold in order to achieve fast detection.

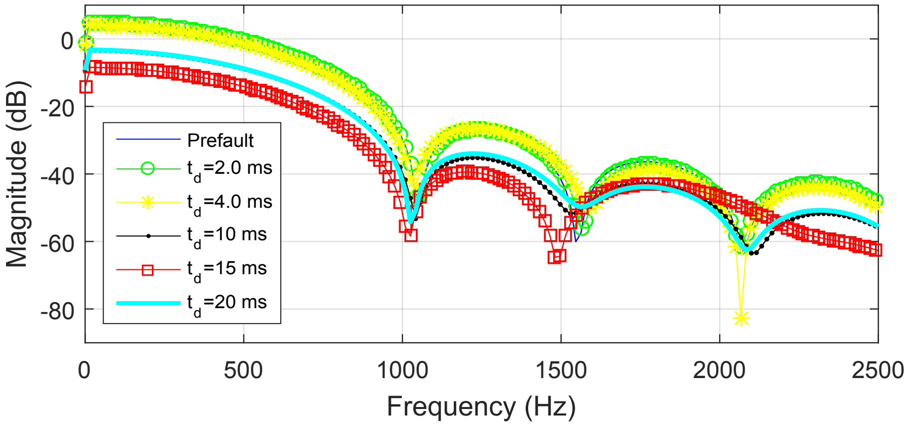


FIGURE 7.8: Frequency spectrum of I_{dc12} for AC fault.

7.2.3 Influence of AC Fault

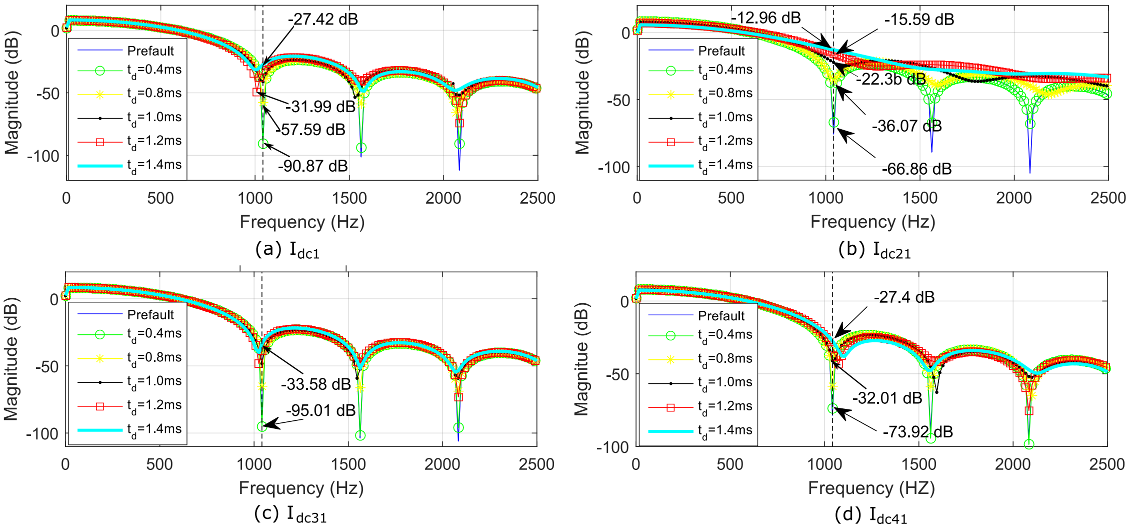
As discussed in Section 4.1.5.2, the AC fault may introduce certain degree of transient to DC current. It is important that the STFT-based fault detection method is able to recognize that and will not mistake it for DC fault.

Fig. 7.8 shows the dynamic of frequency spectrum over the course of AC fault. The AC circuit breaker usually takes about 2 cycles to trip extinguish fault current. In the lead-up to the clearance of AC fault, the side lobes maintain the shape with negligible distortion and the magnitude of the first zero-crossing frequency bin does not seem to change significantly. Therefore, the STFT will not register it as DC fault. The three-phase-to-ground fault is the most severe in the AC fault family, hence it is fair to say that the proposed detection method can discriminate against all other AC faults as well.

7.2.4 Employment of Fault Current Limiter

Having demonstrated the performance of STFT method in simulation model, it would be interesting to evaluate its effectiveness in identifying the challenging fault condition in radial HVDC system, as described in Section 4.1.3. F_{dc12} is simulated, and the inductive

FCL with value of 100 mH is placed at the end of each DC line. Similarly, the simulation uses sampling frequency of 16666.67 Hz, therefore the first zero-crossing frequency bin falls at 1042 Hz.



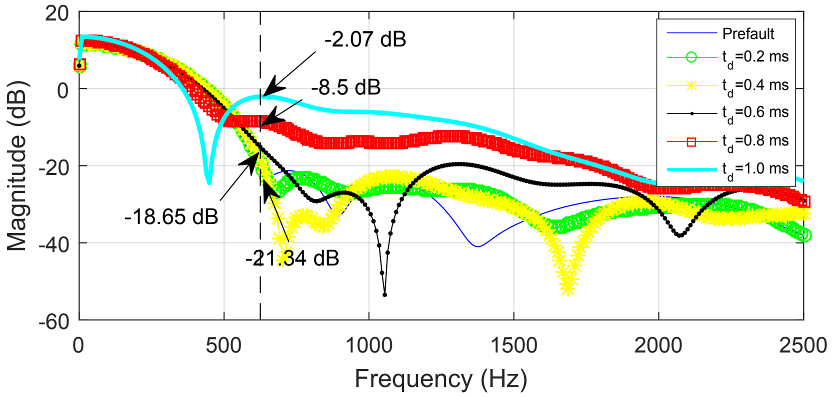
(a) I_{dc1} (b) I_{dc21} (c) I_{dc31} (d) I_{dc41}

FIGURE 7.9: Frequency spectrum of DC currents during F_{dc12} in radial HVDC system.

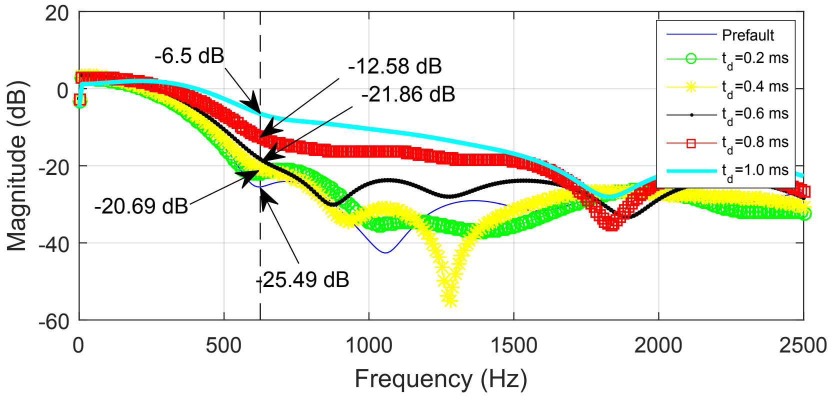
Fig. 7.9 shows the result of STFT with FCL integrated into the system. The frequency spectrum of I_{dc21} becomes distorted at t_d=1.2ms, exhibiting the sign of DC fault happening on $L12$. Notice that the presence of inductor has dampened the rate of change of fault current, which explains the prolonged detection delay. For this reason, the threshold has to be updated in this case. The other currents show no distortion in their frequency spectrum and their magnitudes of first zero-crossing frequency bin remain low. Thus, it can be said that the FCL successfully improves the selectivity by ensuring $MMC2$ to solely proceed with necessary protective action.

7.3 Fault Analysis on Experimental Test System

The STFT-based fault detection method is validated using experimental result, generated by the model depicted in Fig. 4.9. The PP fault with R_f=2 Ω is initiated in the middle of DC line, and the DC current (I_{dc1} and I_{dc2}) are measured and analyzed with STFT. For this analysis, the STFT adopts the Hanning window with length of 32 samples, using the property as such: f_s=10000 Hz, N=1024 samples and H=2. Hence, the first zero-crossing frequency bin will happen at 625 Hz.



(a) I_{dc1}



(b) I_{dc2}

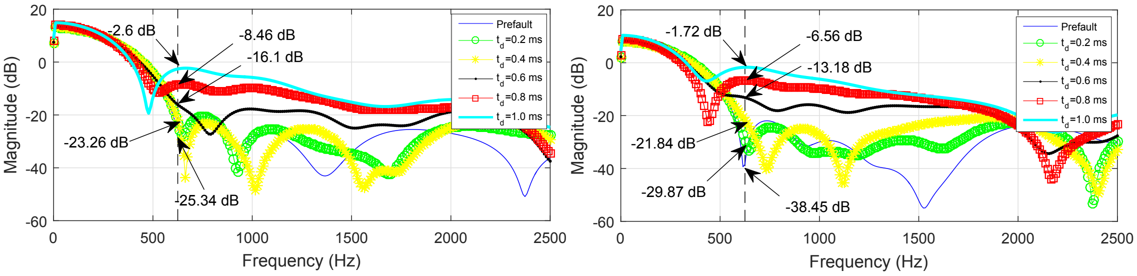
FIGURE 7.10: Frequency spectrum of DC currents for DC fault in experiment. Dash line indicates the first zero-crossing frequency bin.

Fig. 7.10 presents the frequency response for experimental fault currents. Significant distortion is visible at t_d= 0.4 ms, with the magnitude seemingly increasing all across the side lobes. The threshold as benchmarked in the simulation analysis is applicable in this case. I_{dc1} sees the first zero-crossing frequency bin exceeding -10 dB at t_d= 0.8 ms, so does I_{dc2} at 0.2 ms later.

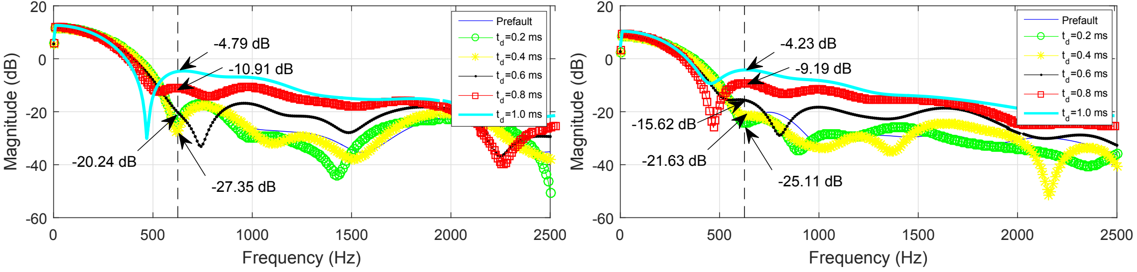
The fault parameter in the experiment is varied to study how resilient is the STFT-based method. Similar to previous analysis, -10 dB, the threshold for the first zero-crossing frequency bin, will be used as the fault criterion.

As measured by MATLAB, the average computation time for FFT algorithm is 24.27 μs.

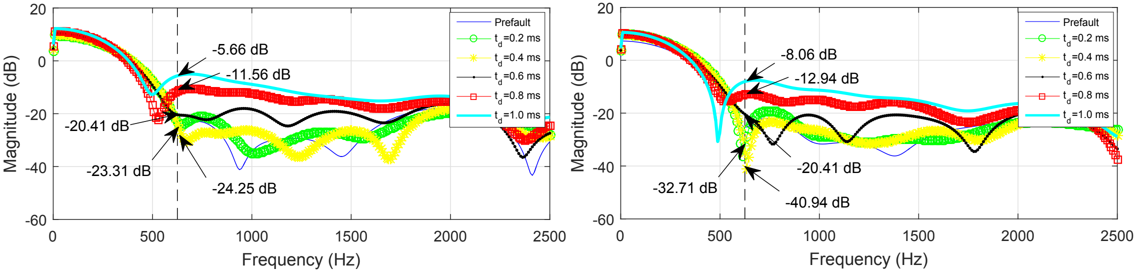
7.3.1 Influence of Fault Resistance



(a) R_f=4 Ω (b) R_f=6 Ω



(c) R_f=8 Ω (d) R_f=10 Ω



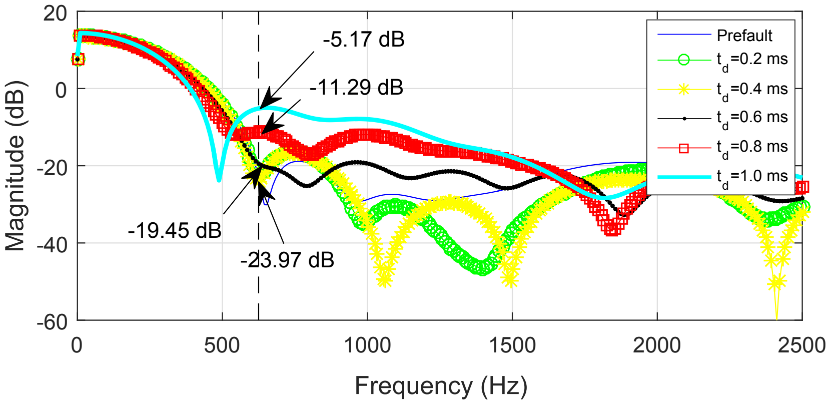
(e) R_f=12 Ω (f) R_f=14 Ω

FIGURE 7.11: Influence of fault resistance on frequency spectrum of experimental fault current I_{dc1}.

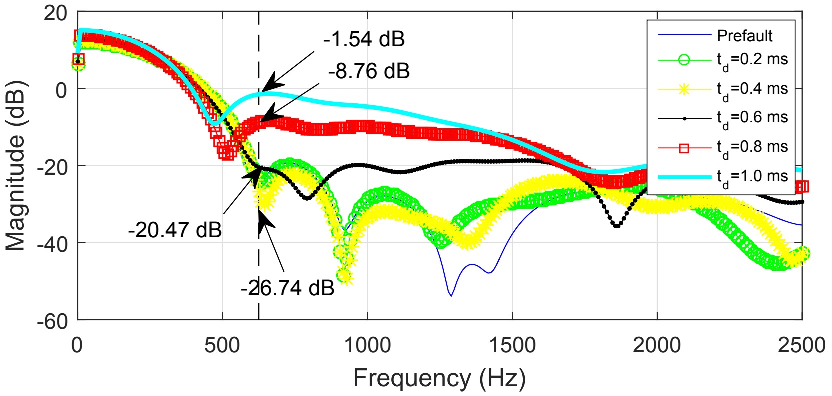
Fig. 7.11 shows the frequency spectrum of I_{dc1} for the DC fault with R_f=4∼14 Ω. All of the faults are detected, as can be seen that the first zero-crossing frequency bin escalates starting from t_d=0.6 ms. The fault detection for R_f=4 Ω, 6 Ω and 10 Ω happens at t_d=0.8 ms, while the rest at 0.2 ms later.

The trend is somewhat inconsistent with what would be expected, whereby the fault detection time is usually delayed as the R_f increases. Since the experiment runs on substantially lower capacity, a small step of R_f is equivalent to extreme attenuation in the fault-induced transient. Therefore, the maximum magnitude of first zero-crossing frequency bin appears to drop sharply as it goes from R_f=4 Ω to 14 Ω. Nevertheless, it is justified that the STFT-based fault detection method using the threshold works on the experiment, without diminishing in sensitivity under the influence of fault resistance.

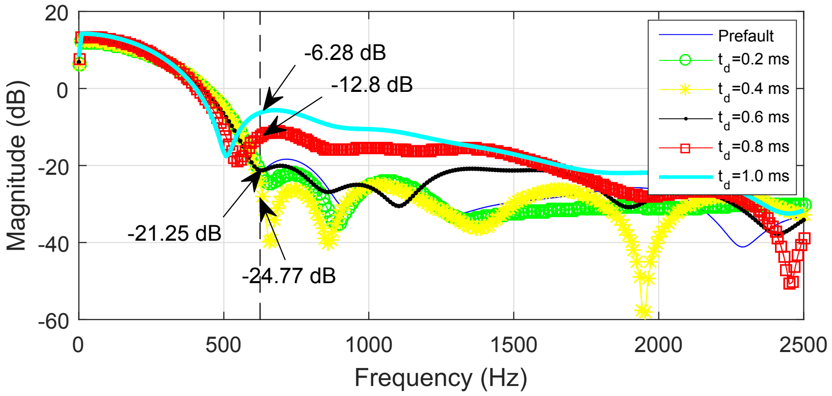
7.3.2 Influence of Fault Distance



(a) Test 1 location



(b) Test 2 location



(c) Test 3 location

FIGURE 7.12: Influence of fault distance on frequency spectrum of experimental fault current I_{dc1}.

In the experiment, the DC line inductance are adjusted according to three combinations as illustrated in Fig 5.11, this is to emulate different fault location and provide broader picture of fault-induced transient.

The result is given in Fig. 7.12. As expected, the DC fault results in distorted frequency spectrum, with the first zero-crossing frequency bin meeting the threshold 0.8 ms after the fault. At t_d=1.0 ms, among the test locations studied here, Test 2 records the highest magnitude (-1.54 dB). This is because the DC fault is much closer to $VSC1$, the diminished line resistor in the fault loop allows the fault current to rise at comparatively higher rate. Therefore, Test 2, Test 1 and Test 3, in the order of increasing fault distance, observes the drop in the magnitude of first zero-crossing frequency bin. However, the fault distance does not compromise the effectiveness of STFT in detecting the DC fault.

7.3.3 Influence of Load Change

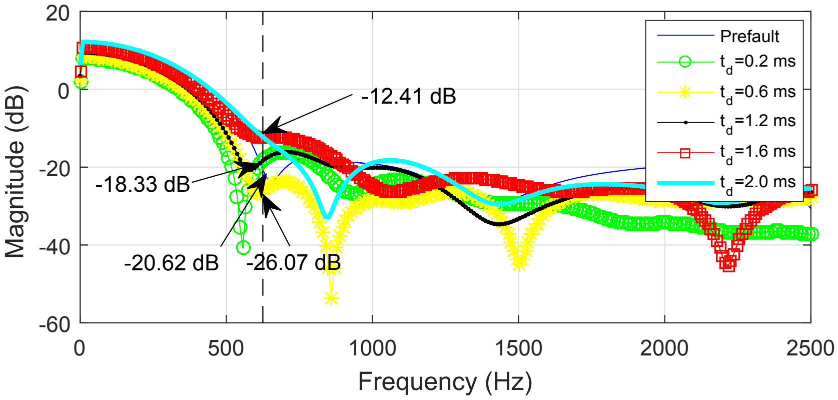


FIGURE 7.13: Frequency spectrum of fault current I_{dc1} during load change.

The STFT-based fault detection method is evaluated on load change, similar with Section 5.3.3. Likewise, it is important to ensure that the detection is selective enough to differentiate the load change from the DC fault.

Fig. 7.13 presents the dynamic of frequency spectrum due to the load change in experiment. It can be seen that the STFT is very sensitive to transient introduced by the load change, with the side lobes suffering small amount of distortion. Even so, the level of distortion is nowhere near what is observed in fault condition. The first zero-crossing frequency bin records the maximum magnitude (-12.41 dB) at t_d=1.6 ms, and it appears to decrease subsequently. Since it is below the threshold, the STFT is able to maintain its detection selectivity.

7.4 Summary

In this chapter, the application of Short Time Fourier Transform (STFT) in DC fault detection has been investigated. Because of uncertainty principle with STFT, we prioritize finer time resolution at the expense of frequency resolution, allowing us to have faster detection. The DC fault is detected by examining the frequency spectrum. Theoretically, the frequency spectrum of a constant, time invariant DC current under normal condition should look like a *sinc* function. A key signature of *sinc* function is the location of zero crossing, which happens at what is termed as zero-crossing frequency bins in this chapter. Because of the high frequency content injected by the fault-induced transient, the zero-crossing frequency bin is bound to increase in magnitude. This phenomenon is hence leveraged as a fault indicator.

The fault detection algorithm is validated using simulation and experimental DC test systems. The DC fault detection is said to be successful when the first zero-crossing frequency bin exceeds the threshold. In a multi-terminal HVDC system, the proposed method can solely rely on the local information to determine the faulted line. In addition, it demonstrates reasonable degree of robustness to the influence of fault resistance and distance. In all cases, a detection time of less than 1 ms is obtained. Most importantly, its ability to differentiate the DC fault from other types of power system disturbances, such as AC fault and load change, is substantiated by both simulation and experimental result. The improved selectivity in multi-terminal HVDC system is obtained when inductive fault current limiter is introduced.

Chapter 8

Fault Clearance and Recovery Strategy

8.1 Introduction

VSC-based DC system is especially defenseless against DC fault. Due to lack of DC-side inductance, the fault current can penetrate the system at extremely high rate. The DC fault can be divided into three stages. Stage 1, for the most part, is dominated by the discharge of DC-link capacitor. As soon as the fault is detected, the VSC will be blocked. When DC voltage drops to zero, Stage 2 starts with fault current freewheeling through diodes. This is the stage that exposes vulnerability of VSC as the diodes are likely to be damaged by overcurrent. In Stage 3, the AC supply will continue feeding current through diodes, which now form uncontrolled rectifier, into fault point. Fault detection methods have been extensively discussed in literatures [12, 34, 48, 99], it is common practice to identify DC fault within 2 ms.

The DC CB [58, 100] is known for the speediest approach to clear the DC fault. However, this kind of CB involves complicated mechanism requiring components that would contribute to large physical size and arguably high cost. Solid state-based DC CB is proposed [3, 101]. Because it operates electrically, it can cut off the faulted line very fast. Even so, it has fair share of downside - high on-state loss [59]. Recent years have seen increasing R&D focus in the protection of Modular Multilevel Converter-based (MMC). The MMC is made up of a number of independent converter units, called the submodule (SM). The flexibility of designing the SMs gives rise to variation of circuit topology [102, 103]. Full bridge SM comes with fault ride-through capability. It, however, requires twice as many semiconductor switches as half bridge SM. The AC CB is also proposed in literature as one of the protection approaches applicable in multi-terminal DC (MTDC) system [20, 30]. Its slow operation renders the anti-parallel diodes to tolerate increasing fault current during freewheeling stage. To solve this problem, one can connect thyristors in parallel with each MMC submodule. The thyristors are normally off, and can be turned on when the DC fault is detected. Several literatures [61, 62] have shown that such implementation can force the fault current to decay itself exponentially, facilitating the fault isolation. However, this scheme has only been analyzed for single HVDC converter. It would be interesting to evaluate it feasibility in a MTDC system which involves multiple DC lines.

Fig. 8.1 illustrates the schematic diagram of half bridge-based MMC, accompanied with the protection devices such as AC CB, double-thyristor, hybrid DC CB and DC switch. Each phase-arm consists n numbers of SMs, arm inductors (L_{arm}) and double-thyristors inserted in parallel with them. The DC side of MMC is connected to other similar MMC stations via underground cable or overhead line. The AC CB is placed after the AC supply while the hybrid DC CB or DC switch before the DC conductor. With the

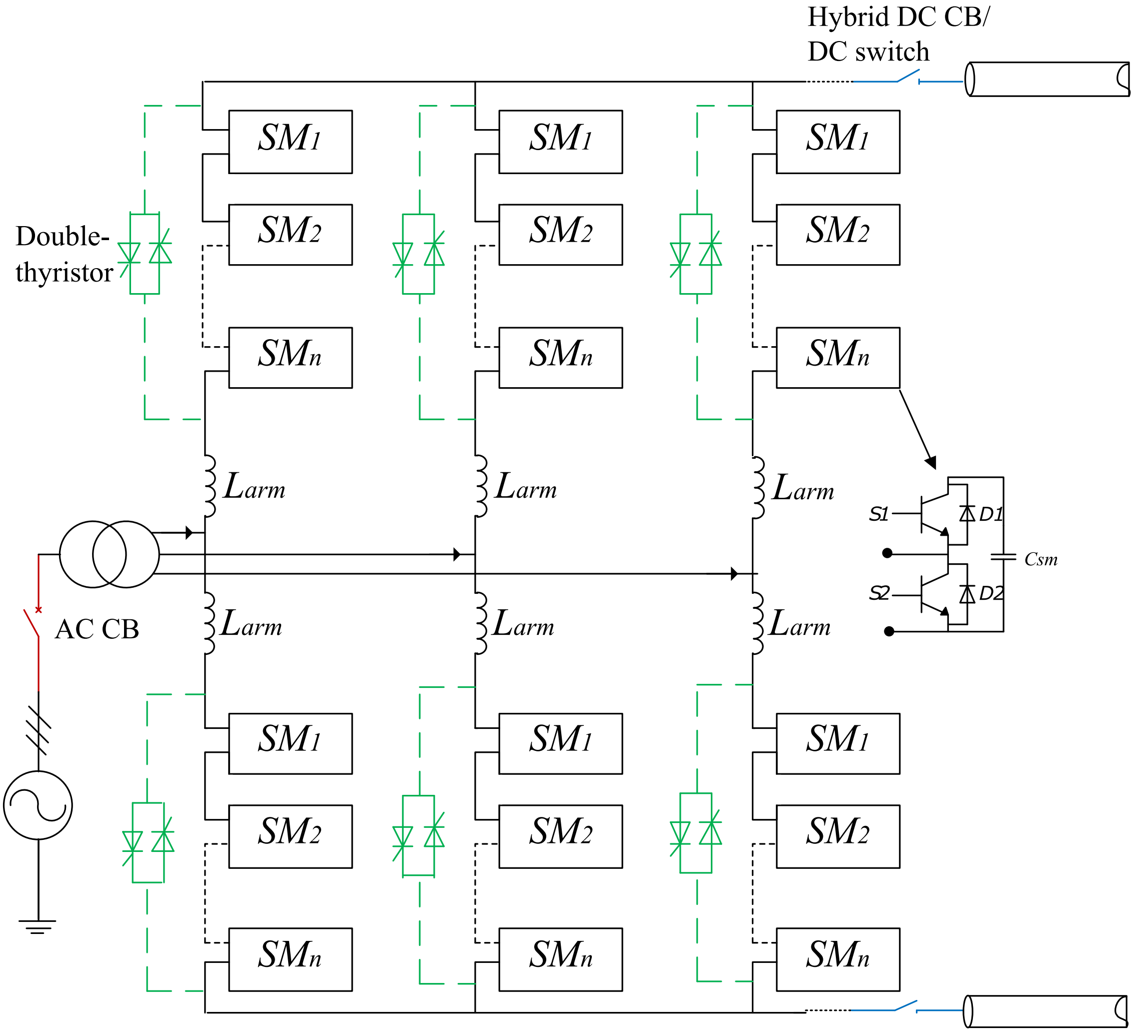


FIGURE 8.1: Fault clearance options for MMC-based DC system.

protection devices shown here, three protection schemes can be realized for this HVDC system, which are listed in Table 8.1.

TABLE 8.1: Three possible schemes for fault clearance in multi-terminal HVDC system.

Device	**Scheme 1**	**Scheme 2**	**Scheme 3**
AC CB	√	√	√
Hybrid DC CB	×	×	√
Double-thyrsitor	×	√	×
DC switch	√	√	×

The main contribution of this chapter is to perform comparative analysis of the three protection schemes proposed here, in term of the time they take to achieve full recovery in the event of DC fault. Due to unavailability of well-established standard for multi-terminal HVDC system, the chapter assumes own set of constraints that the system needs to follow during the recovery. The reader will have an idea regarding the proper sequence to restart the system for each protection scheme during post-fault, so that the transients can be kept within the constraint. A four-terminal HVDC system, built in PSCAD/EMTDC, is used as the test system.

8.2 Fault Clearance Method

8.2.1 Scheme 1

Scheme 1 is the simplest among the schemes discussed in this chapter, only involving AC CB [20, 30].

The AC CB is well-established and has been essentially adopted on the AC side of converter, therefore it is not deemed as an additional device like hybrid DC breaker. For the point-to-point HVDC system, the fault on DC line requires complete shutdown of the system before it is isolated, which can be sufficiently accomplished by AC CB. Because of its cost-effectiveness and low complexity, this scheme may be suitable in a meshed grid topology comprising protection zones that allow temporary de-energization. A fast fault detection technique is very important for this scheme to succeed. Any delay by the fault detection technique, on top of three cycles' operation of AC CB, means higher fault current the system components need to tolerate.

Upon detecting occurrence of DC fault, the blocking signal will be dispatched to all IGBTs. This is followed by opening AC CB in order to entirely cut off supply of AC current into fault point. The resulting current flow within MMC will resemble what happens in Scheme 2 (see Fig. 8.2), except now the diodes have to incur the full fault current. Following the tripping of AC CB, the fault current will decay exponentially. The DC switches on both sides of the faulted line are opened when the fault current is low enough. Wang [20] adopted a similar scheme in his work and showed that a ring-shaped grid system has to be de-energized longer than 20 ms in the event of DC fault.

8.2.2 Scheme 2

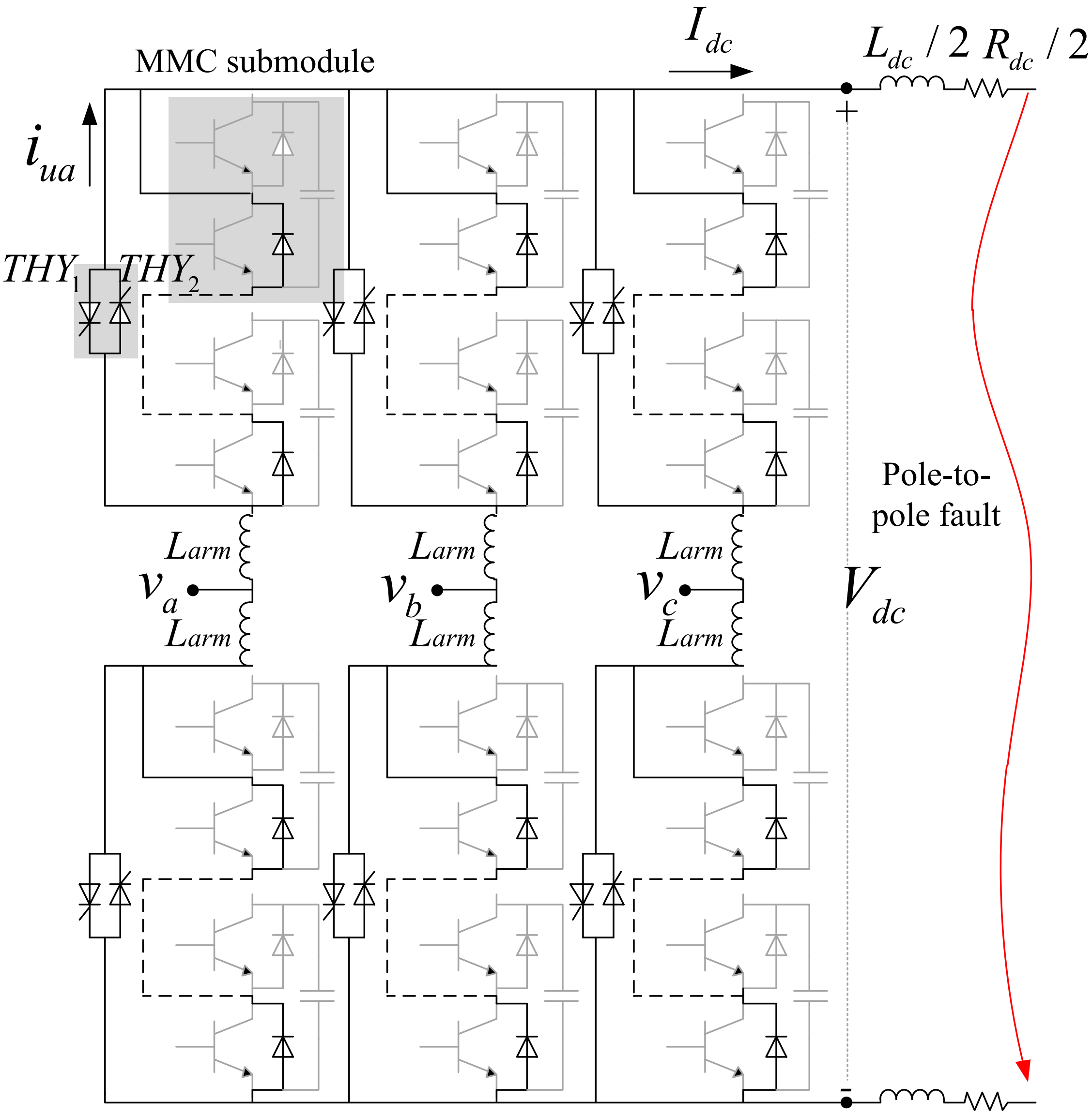


FIGURE 8.2: Current path in MMC circuit with double-thyristor scheme included during DC fault.

In this scheme, the double-thyristor inserted across upper and lower arm in each phase and AC circuit breaker (CB) are employed [61, 62].

After the fault is detected, the IGBTs in each submodules need to be blocked and the new current path is illustrated in Fig. 8.2. Following the blocking, the half-bridge submodule is no longer able to support voltage on DC side and the anti-parallel diodes continues to allow the AC current to flow like an uncontrolled rectifier bridge. The prolonged current from AC side can damage the diodes if its magnitude exceeds the diode's rating.

The post-fault behavior of the fault current can be explained mathematically. The AC side voltage of MMC can be expressed as follows:

$$v_a(t) = -v_{ua}(t) + \frac{V_{dc}(t)}{2}, \tag{8.1}$$

$$v_b(t) = -v_{ub}(t) + \frac{V_{dc}(t)}{2}, \tag{8.2}$$

$$v_c(t) = -v_{uc}(t) + \frac{V_{dc}(t)}{2}, \tag{8.3}$$

where $v_{ua}(t), v_{ub}(t), v_{uc}(t)$ are the voltage across upper phase-leg and $V_{dc}(t)$ is the DC-link voltage. $v_{ua}(t), v_{ub}(t), v_{uc}(t)$ can be written in another form:

$$v_{ua}(t) = R_s i_{ua}(t) + L_{arm}\frac{\mathrm{d}i_{ua}(t)}{\mathrm{d}t}, \tag{8.4}$$

$$v_{ub}(t) = R_s i_{ub}(t) + L_{arm}\frac{\mathrm{d}i_{ub}(t)}{\mathrm{d}t}, \tag{8.5}$$

$$v_{uc}(t) = R_s i_{uc}(t) + L_{arm}\frac{\mathrm{d}i_{uc}(t)}{\mathrm{d}t}, \tag{8.6}$$

where R_s denotes the sum of resistance of thyristor and diode in each leg, and $i_{ua}(t), i_{ub}(t), i_{uc}(t)$ are the upper arm current in each phase.

Considering that the AC voltage is balanced, the sum of the three-phase voltages will be zero, whereas the sum of the arm currents would be equal to the DC current.

$$v_a(t) + v_b(t) + v_c(t) = 0. \tag{8.7}$$

$$I_{dc}(t) = i_{ua}(t) + i_{ub}(t) + i_{uc}(t). \tag{8.8}$$

By substituting (8.1)-(8.3) and (8.8) into (8.7), we can obtain

$$\frac{3V_{dc}(t)}{2} = R_s I_{dc}(t) + L_{arm}\frac{\mathrm{d}I_{dc}(t)}{\mathrm{d}t}. \tag{8.9}$$

The DC voltage can be expressed in terms of the DC line resistors and inductors such that

$$V_{dc}(t) = R_{dc} I_{dc}(t) + L_{dc}\frac{\mathrm{d}I_{dc}(t)}{\mathrm{d}t}. \tag{8.10}$$

Combining (8.10) with (8.9) yields a complete equation describing the entire DC current behavior after the thyristors are turned on:

$$\frac{\mathrm{d}I_{dc}(t)}{\mathrm{d}t} + \left(\frac{R_s + 3/2R_{dc}}{L_{arm} + 3/2L_{dc}}\right) I_{dc}(t) = 0. \tag{8.11}$$

Taking the initial condition $I_{dc}(t_0) = I_0$, where t_0 is the time when the thyristors are turned on, (8.11) can be solved such that:

$$I_{dc}(t) = I_0 e^{-(t-t_0/\tau)}. \tag{8.12}$$

where $\tau = (R_s + 3/2R_{dc})/(L_{arm} + 3/2L_{dc})$.

Eqn. (8.12) infers that the turning on of thyristor allows the fault current to exponentially decrease to near zero, with the decay rate determined by the time constant which depends on the parameters of the DC line. Therefore, the decay rate is subject to fault location and resistance.

When the fault current freely decreases and becomes sufficiently low, the faulted line needs to be disconnected in order to resume the power flow immediately. The line disconnector can be just as simple as DC switch since it does not have to tolerate high current the same way the hybrid DC breaker does. After the fault is cleared, the thyristors and IGBTs may be turned off and on respectively.

Fig. 8.3 illustrates the current profile of thyristor and diode if this scheme is employed. Before 2.75 s, the thyristor is still off and the diode is operating under normal condition. After the fault is detected, the thyristor is turned on creating short-circuit on AC side and providing additional path for infeed AC current that would have otherwise flowed

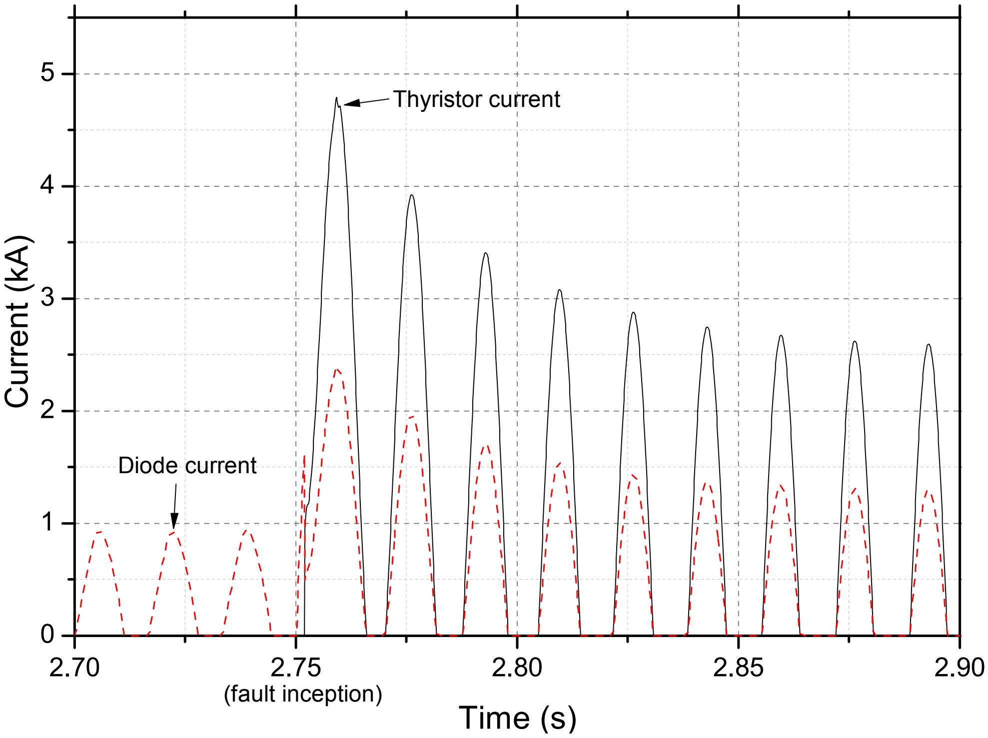


FIGURE 8.3: Current profile in thyristor and diode during freewheeling stage.

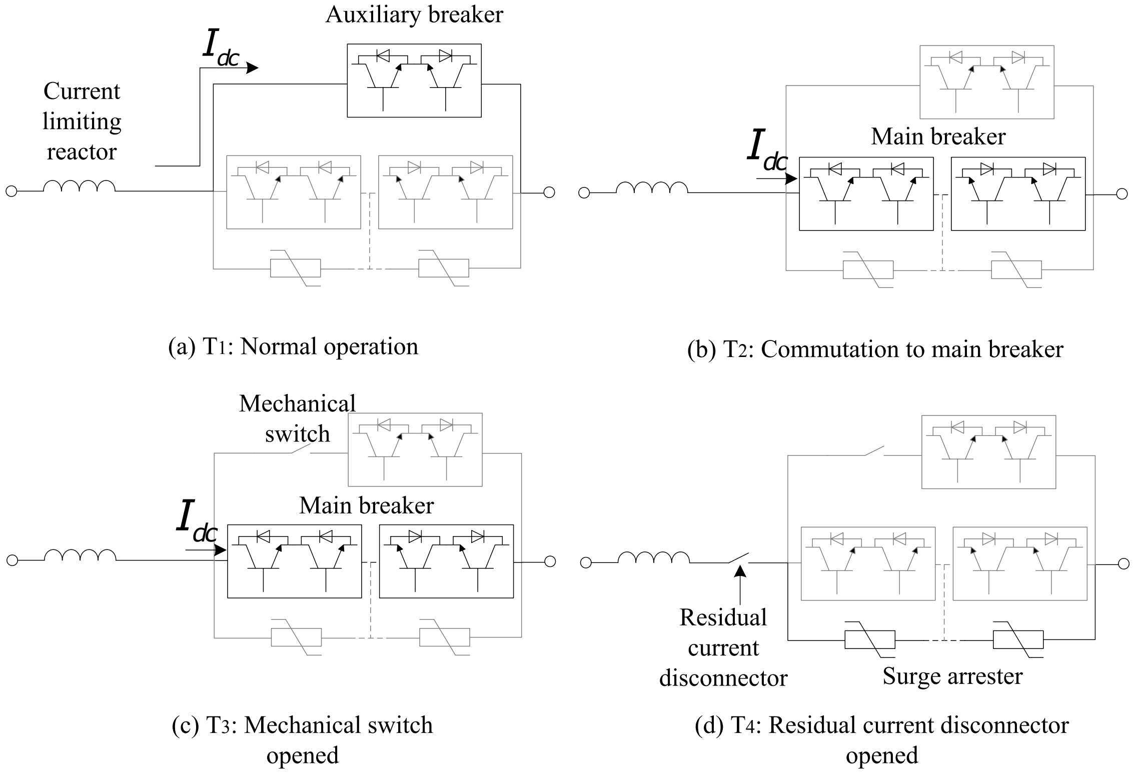
into DC side. The thyristor takes over substantial proportion of current from diode. The infeed AC current continues freewheeling within the converter until AC breaker is opened. The works on this protection scheme [61, 62] used a simple test system consisting of only one MMC terminal. Therefore, the DC current could decay fast enough without necessitating the tripping of AC CB. In this study, the performance of this scheme will be evaluated on a system that is closer to reality.

8.2.3 Scheme 3

Scheme 3 interrupts the fault current with hybrid DC breaker and AC CB [58, 100].

The hybrid DC breaker developed by ABB [4] is vastly different from the conceptual DC breakers widely known in literature [104–106]. The DC breakers usually are based on the mechanism which generates a counter current flowing against the direction of fault current in order to forcefully drive the breaker current to zero. The counter current is produced by resonant circuit comprising inductor and capacitor. The L-C is pre-charged to a voltage level depending on the current it is expected to generate. This kind of DC breaker breaks the fault reasonably fast but they can be very bulky due to the L-C component which increases in physical size with the rating.

As the 'hybrid' suggests itself, the hybrid DC breaker embodies two different types of interrupters, mechanical breaker and semiconductor-based switch, without the support of resonant circuit to create current zero. The mechanical breaker is known for low-resistive metal contacts but the operation speed is a major concern [107]; semiconductor-based switch is able to act fast but it contributes to high transfer loss. Recognizing these interrupters' strengths, the hybrid DC breaker combining the two is hence an optimum solution to make up for each other's downsides.



(a) T1: Normal operation

(b) T2: Commutation to main breaker

(c) T3: Mechanical switch opened

(d) T4: Residual current disconnector opened

FIGURE 8.4: Fault clearance sequence of hybrid DC CB.

The structure and fault clearance sequence of hybrid DC breaker is shown in Fig. 8.4. There are three paths where the current can possibly flow. During normal operation, the main breaker is still in open state, thus the current will only flow through the first path consisting of switch and auxiliary breaker. When fault occurs, the auxiliary breaker are turned off immediately while the main breaker is turned on initiating the commutation stage. The mechanical switch will take approximately 2 ms to open [31]. This is followed by blocking of semiconductor switch in the main breaker. Thereafter, the surge arrester takes over the current flow. With the current, a counter voltage is established across the surge arrester impeding the current flowing from AC supply, consequently the current is drained to zero. After the residual current disconnector is opened, the fault isolation process is completed.

The current profile in the hybrid DC breaker throughout the fault isolation process is illustrated in Fig 8.5.

T_1: The line current begins to increase as DC fault happens. At this point in time, the current is still flowing through auxiliary breaker. The main breaker remains in open state.

T_2: The DC fault is detected about 2 ms later. A block signal is dispatched to auxiliary breaker in order to commutate the current flow to main breaker.

T_3: The main breaker is turned on successfully commutating the current flow to its path. However, the current is still increasing as the mechanical switch will take 2 ms to be completely opened.

T_4: The mechanical switch has been opened. Meanwhile, the semiconductor switch in the main breaker is turned off. As seen in the figure at this time, the current increases from 0 to 5.1 kA as soon as the surge arrester picks up the current from main breaker. Along with the current, the voltage across the surge arrester appears

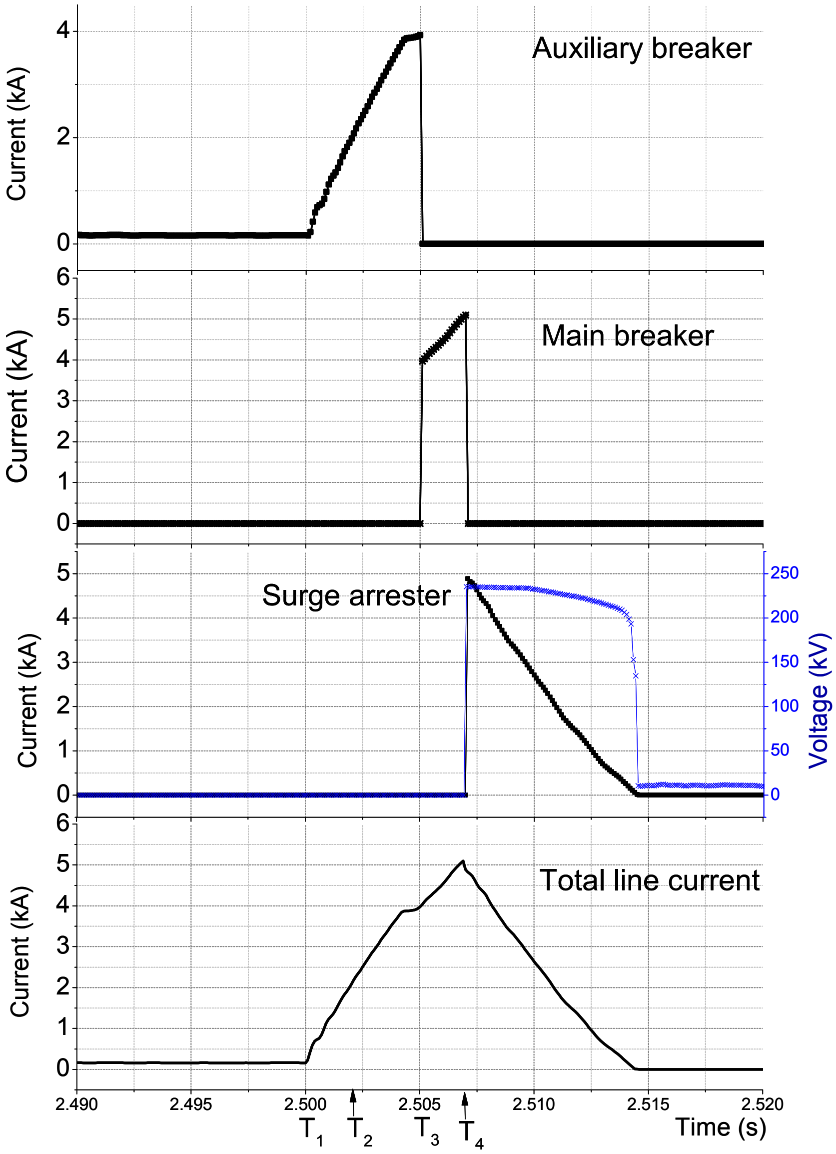


Figure 8.5: Current profile in hybrid DC CB when extinguishing fault arc.

to have increased simultaneously. Subsequently, the current is decreasing to zero. The residual current disconnector is now safe to open.

If the fault current has not reached zero after three cycles [108], the AC breaker will have to trip in order to protect the transformer from increasing AC current. The AC breaker can hence effectively serve for back-up protection in the event of DC breaker failing to trip.

8.3 Recovery Strategy

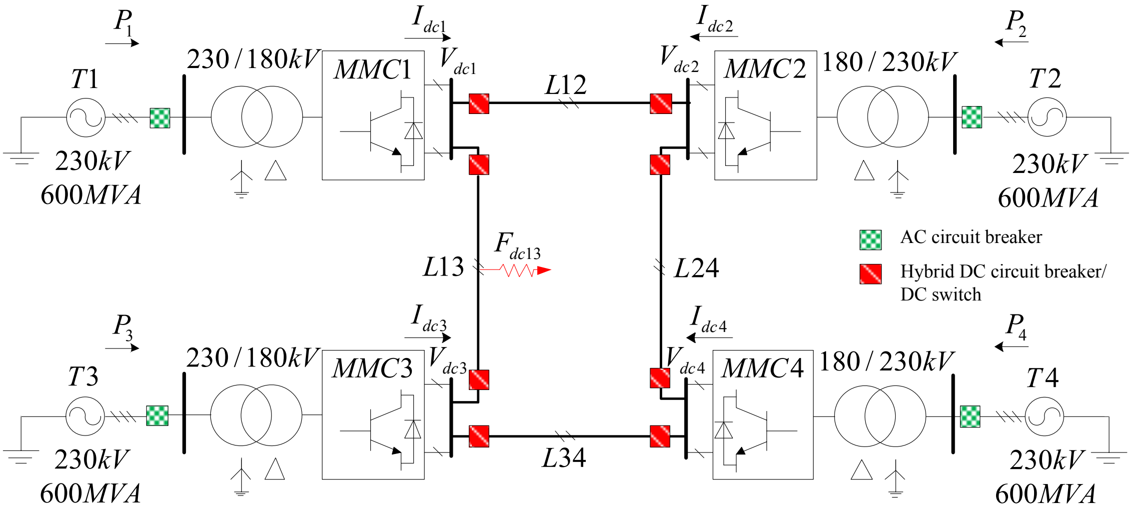


FIGURE 8.6: Multi-terminal HVDC system simulated in PSCAD/EMTDC.

Fig. 8.6 shows the multi-terminal MMC-HVDC system with the protection devices in place. Three-phase breaker model, which is already provided in library of PSCAD/EMTDC, is inserted near each AC supply. The devices required to build the model of hybrid DC CB are also available in the library. For example, the residual current disconnector and the mechanical switch are represented by single-phase breaker model, whereas the main and auxiliary breakers are made up of IGBT model. A designated control structure is built alongside with the hybrid DC CB model to time the switching sequence for different switches after the DC fault is detected. As for the DC switch, it is simply represented by a single-phase breaker model.

Fig. 8.7 shows the protection and control sequence proposed for the three schemes. The process of fault clearance can be generally broken down into three stages:

1. *Fault detection*: I_{dci} >2.0 pu is assumed as the fault criterion. Each MMC terminal ($MMC1$, $MMC2$, $MMC3$, $MMC4$) is responsible to constantly monitor the DC current (I_{dc1}, I_{dc2}, I_{dc3}, I_{dc4}), as soon as the current exceeds the threshold the

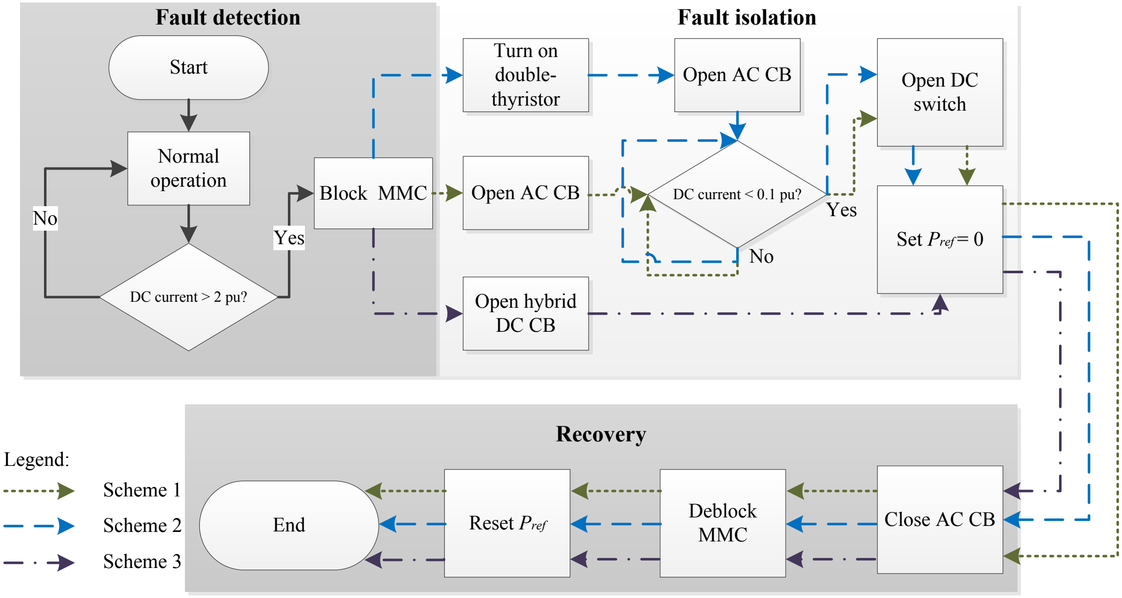


FIGURE 8.7: DC fault handling and recovery sequence.

IGBTs in that terminal will be blocked. The fault detection is expected to take about 2 ms.

2. *Fault isolation*: From this stage onward, the three schemes start to take on different paths.

   - The tripping time of AC CB is 60-100 ms [20]. However, the study here assumes 50 ms, exactly three cycles based on the system frequency used in the simulation model. After the tripping of AC CB is activated, the AC supply stops feeding the current to fault point, prompting the fault current on DC side to gradually decrease. The DC switches can trip in safe manner as the fault current is finally below 0.1 pu. Likewise, it is necessary to set P_{ref} to zero following the fault clearance.
   - The double-thyristors are deblocked at the same time the IGBTs are blocked. As a result, the AC and DC sides of MMC are successfully segregated and the DC fault current decays freely through freewheeling diodes and double-thyristors. The AC CB will have to trip amid the decaying process unless the

fault current is able to reach sufficiently low value within 3 cycles. Even so, it is more common that the fault current takes fair amount of time to drop due to large time constant of faulted line. As the fault current falls below 0.1 pu, the DC switches will open on both sides of the faulted line, with that the fault is completely isolated. Then, P_{ref} is set to zero.

- After the fault is detected, a delay of about 2 ms is introduced before the hybrid DC CB receives tripping signal. The mechanical switch requires approximately 2-3 ms [31] to commence the current commutation from auxiliary breaker path to main breaker path. This is followed by the second current commutation, now from main breaker path to surge arrester path, 2 ms later [59]. Because of fast action of hybrid DC CB, the fault current can be extinguished fast enough without having to trip the AC CB. The fault isolation can be completed less than 10 ms, significantly faster than AC CB's three cycles' operation. In the time leading up to recovery stage, P_{ref} is reduced to zero.

3. *Recovery*: This stage needs to account the time for the DC line to recover its insulation [21]. For Scheme 1 and 2 which have the AC CBs opened earlier on, an attempt will be made to reclose all the AC CBs. Now, all the schemes converge on the same process again. The MMCs are to resume operation, with the double-thyristor in Scheme 2 already in off mode. Considering the faulted line has been completely removed from the system, the DC voltage will be seen to ramp up. The DC voltage shows sign of stabilization and the power transfer is back to normal operation.

In the recovery stage, it is important to schedule the reclosing of AC CB and the deblocking of MMC such that it will not result in overvoltage and current surge [55]. The following constraints need to be respected when planning the timing in simulation:

- DC voltage: $V_{dcn} < 1.1$ pu, $n = 1, 2, 3, 4$
- DC current: $I_{dcn} < 1.2$ pu, $n = 1, 2, 3, 4$
- AC current: $I_{an} < 1.0$ pu, $n = 1, 2, 3, 4$

The ring-shaped grid, which is used in the system model, is known for its capability to offer system redundancy and good fault performance [53]. For example, if a DC fault occurring on $L13$ shown in Fig. 8.6 is removed, all the MMC terminals are still interconnected and able to trade the same amount of power through the remaining lines without sacrificing system DC voltage. This makes the recovery process less complicated. The same cannot be said for radial grid, in which removal of line means loss of corresponding terminal [20]. Thus, the recovery sequence needs to be planned on how to accommodate new system dynamic. It will be of our interest in future to investigate the recovery performance in different grid topologies.

8.4 Simulation Result

Since pole-to-pole fault is the most severe and representative of DC fault [87] for symmetrical monopole HVDC system, pole-to-ground fault will be not discussed here. In the simulation, the DC fault with resistance 0.1 Ω is triggered in the middle of line $L13$ (revisit Fig. 8.6). The three schemes will be employed to clear the fault and their corresponding recovery sequences will be evaluated based on the constraints discussed in Section 8.3.

8.4.1 Scheme 1

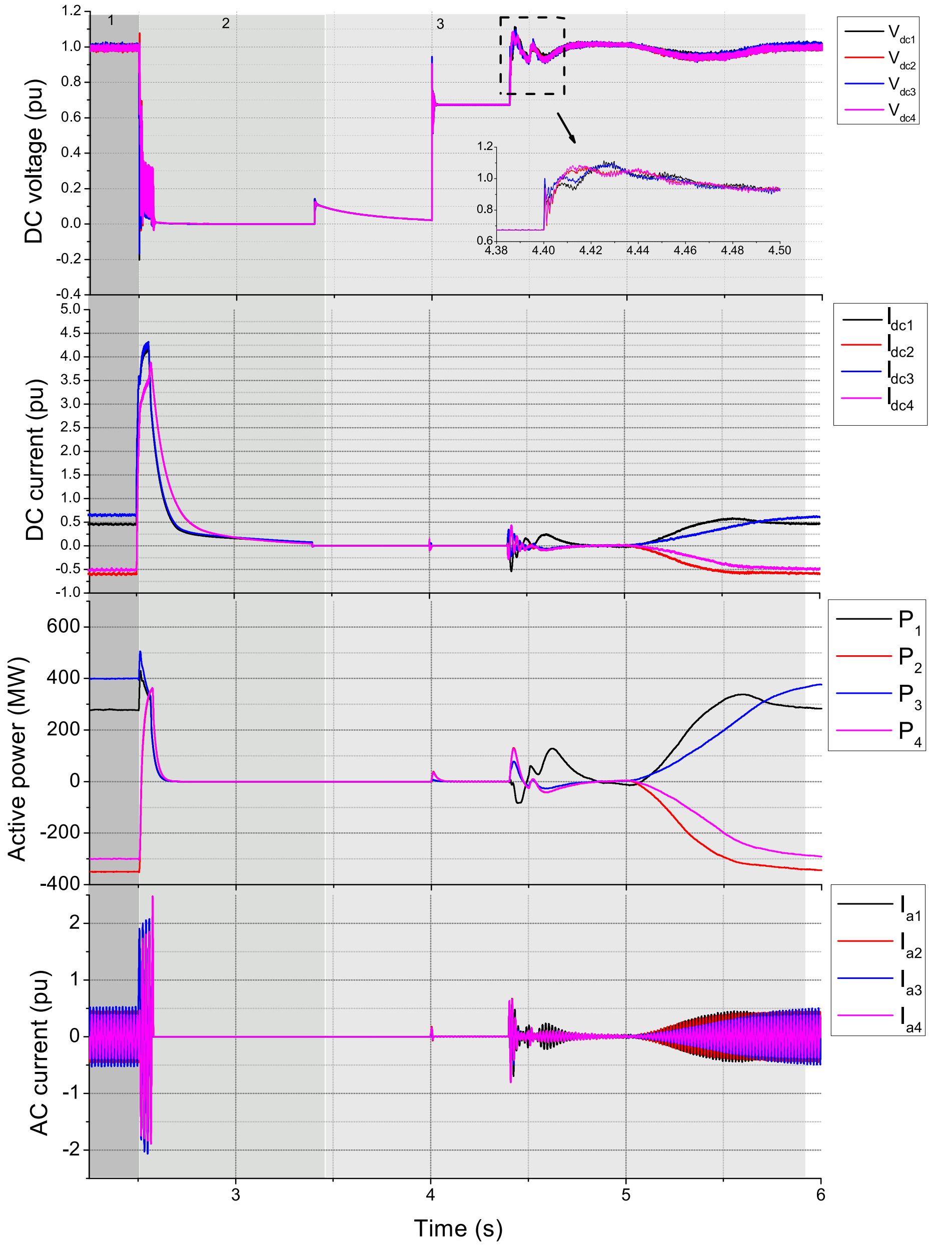


FIGURE 8.8: Simulation result for Scheme 1.

Fig. 8.8 illustrates the performance of recovery strategy for Scheme 1. The figure is segmented into three divisions represented by gray shades with different transparency, starting from normal condition and fault detection stage in 1, fault clearance stage in 2 and recovery stage in 3.

The top figure shows the dynamic of DC voltage measured at $MMC1$, $MMC2$, $MMC3$ and $MMC4$ in per unit (pu). The DC voltage starts off at 1 pu and experiences sharp drop as a result of the DC fault. Following the fault clearance, the reclosing of AC CB is executed at 4s, which sees the DC voltage to surge. The transient, which emerges 0.4 s later as the MMC is deblocked, is zoomed in and it is observed that the surge does not violate the constraint. With that, the stability of DC voltage is achieved.

In the second figure, the DC currents exceed the threshold 2 pu at 2.502 s. However, the AC CB takes three cycles to open, at which time the DC currents have increased over 3.5 pu. After the AC CBs trip, the DC currents decrease exponentially and the DC switches are allowed to trip on both sides of $L13$ at 3.4 s. The minor surge seen in Segment 3 is indicative of the attempt to reclose AC CB and deblock MMC. The DC currents remain at zero until the P_ref is reset at 5 s.

The third figure shows the active power in the system throughout the event of DC fault. The power flow is interrupted as the AC CBs at each terminal trip and restored. At 5 s, the power at each terminal begins to ramp up according to their P_ref.

The last figure shows the phase-A AC current measured at the AC side of each MMC terminal. The AC supply continues supplying the AC current to DC fault point through freewheeling diodes. Subsequently, the AC current quickly falls to zero indicating successful tripping of AC CB. The deblocking of MMC causes minor surge in the AC current. Finally, the recovery process is ended with the AC current increasing to its original value.

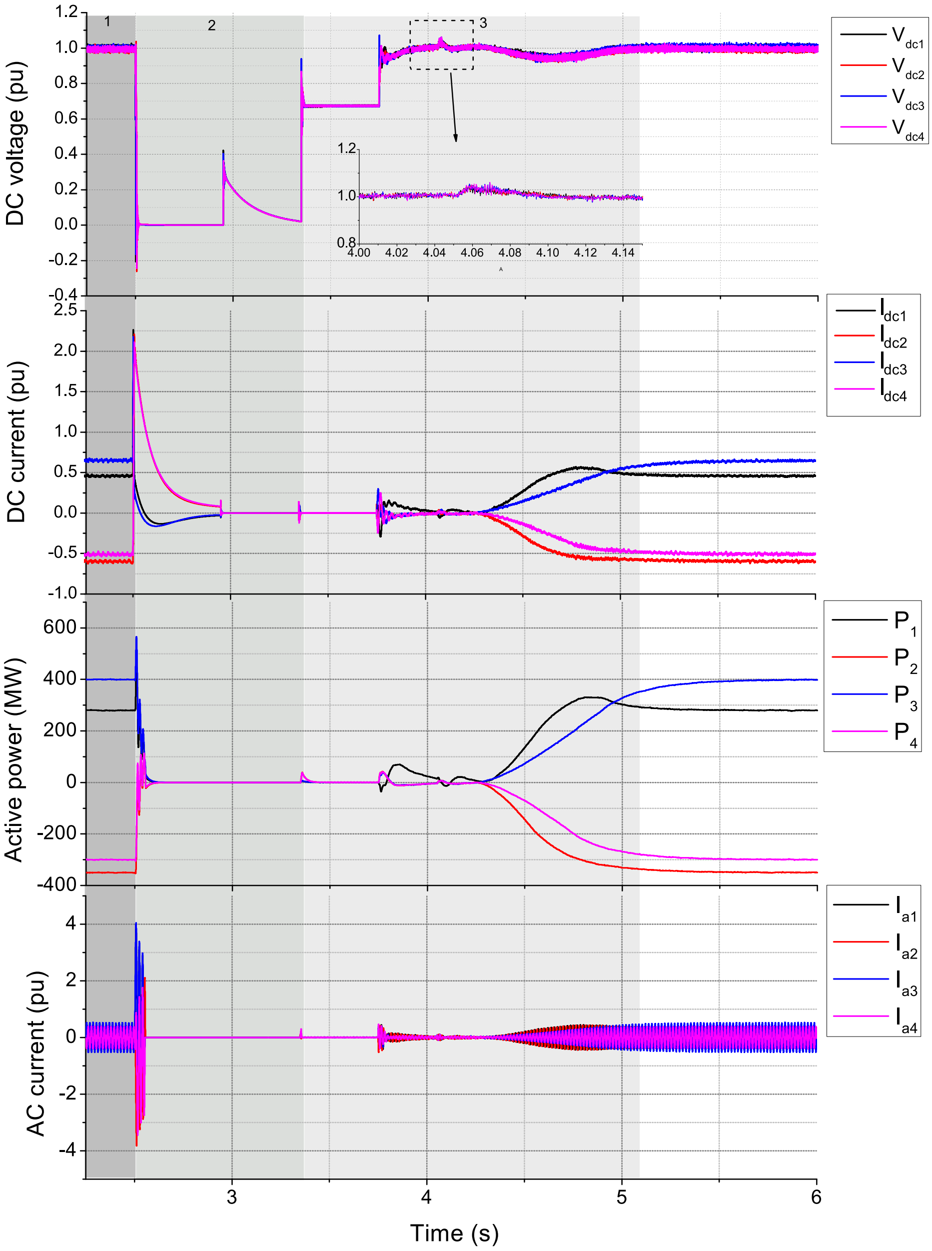


FIGURE 8.9: Simulation result for Scheme 2.

8.4.2 Scheme 2

Fig. 8.9 shows the DC voltage, DC current, active power and phase-A AC current of the multi-terminal HVDC system using Scheme 2.

The DC fault is detected upon DC currents ($I_{dc1}, I_{dc2}, I_{dc3}, I_{dc4}$) exceeding 2 pu. Shortly after that, the blocking of MMCs is activated, as well as deblocking of double-thyristor.

The DC currents can be seen decreasing gradually and reaching sufficiently low value to allow DC switches on $L13$ to open. The active powers and the AC currents are essentially zero because the AC CB at each terminal has been opened. Having the faulted line isolated, the recovery stage is initiated with reclosing AC CBs around 3.35 s. The DC voltage is established. The system operation is not resumed until MMCs are deblocked 0.5 s later, causing some spikes on the DC voltage. The recovery process is finished by resetting P_{ref} to original value, which can be seen as the DC current, active power and AC current ramp up. Overall, the simulation result shows that the multi-terminal HVDC system undergoes smooth restoration from fault with the proposed recovery strategy.

8.4.3 Scheme 3

The response of the multi-terminal HVDC system to DC fault using Scheme 3 is shown in Fig. 8.10.

Using the same fault criterion (I_{dc} > 2 pu), $MMC1$ and $MMC3$ detect the fault at slightly delayed time compared to Scheme 2. This is due to the presence of current limiting reactor in hybrid DC CB, which dampens rate of change of fault current prolonging the time it takes to reach the threshold value. After the fault is detected, both terminals execute blocking of MMC and opening of hybrid DC CB on $L13$. Because these terminals are the ones that generate power to $MMC2$ and $MMC4$, as a result the active powers at all terminals drop to zero temporarily. The fact that I_{dc2} and I_{dc4} remain well below 2 pu through the fault clearance process does not necessitate blocking of their associated MMCs. The $MMC1$ and $MMC3$ are restarted around 2.7 s. The DC voltage sees its value coming back to 1 pu at 3.06s, indicating that the recovery

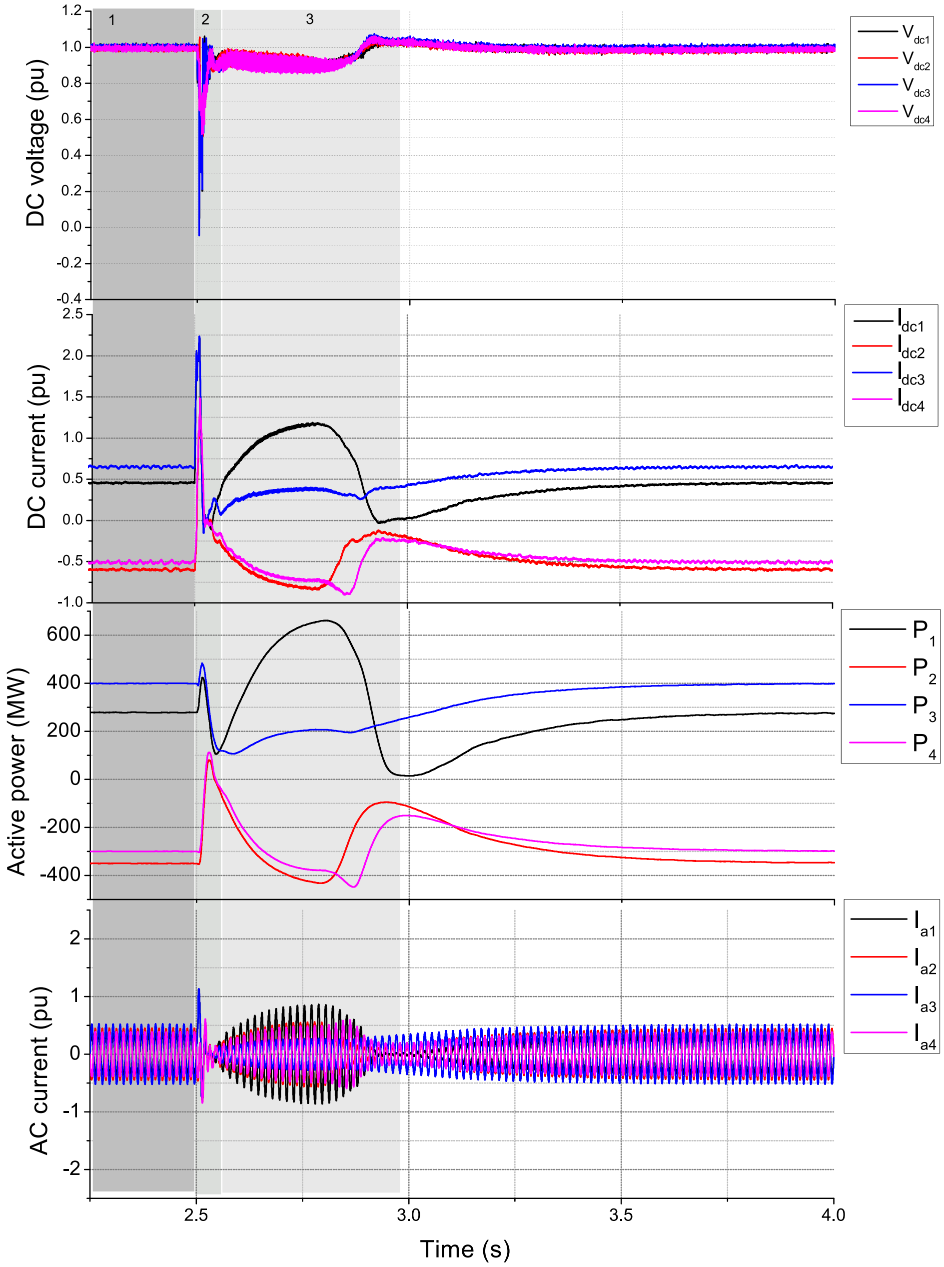


Figure 8.10: Simulation result for Scheme 3.

process is completed. It is demonstrated that the recovery strategy successfully ensures the transients experienced by all parameters within the constraint set in this study.

TABLE 8.2: Recovery performance comparison for three protection schemes.

	Scheme 1	**Scheme 2**	**Scheme 3***
Fault detected	2.5010 s	2.5010 s	2.5043 s
Block MMC	2.5014 s	2.5014 s	2.5047 s
(i) Double thyristor	×	2.5014 s	×
(ii) Hybrid DC CB	×	×	2.5070 s
(iii) AC CB	2.5600 s	2.5600 s	×
(iv) DC switch	3.4000 s	2.9500 s	×
Set P_{ref}=0	3.4000 s	2.9500 s	2.5100 s
Reclose AC CB	4.0000 s	3.3500 s	×
Deblock MMC	4.4000 s	3.7500 s	2.5297 s
Reset P_{ref}	5.0000 s	4.2500 s	2.8000 s

*only block $MMC1$ and $MMC3$.

We have analyzed different fault clearance schemes for multi-terminal HVDC system and performance of recovery strategy proposed. To summarize, the recovery strategy works reasonably well, as evidently proven by the result that the system does not experience significant voltage spike and current surge. What makes each scheme differ is how the sequence in Fig. 8.7 is timed to guarantee smooth recovery.

The sequence timing for each scheme is presented in Table 8.2. It is obvious that Scheme 3 demonstrates the most superior performance in term of the time it takes to clear the fault and restore to normal operation. The hybrid DC CB only needs about 10 ms to extinguish fault arc. Thanks to its fast action, the fault current does not continue increasing and the blocking of MMC at healthy terminals ($MMC2$ and $MMC4$) is narrowly avoided. The system is not entirely de-energized, hence this scheme is able to

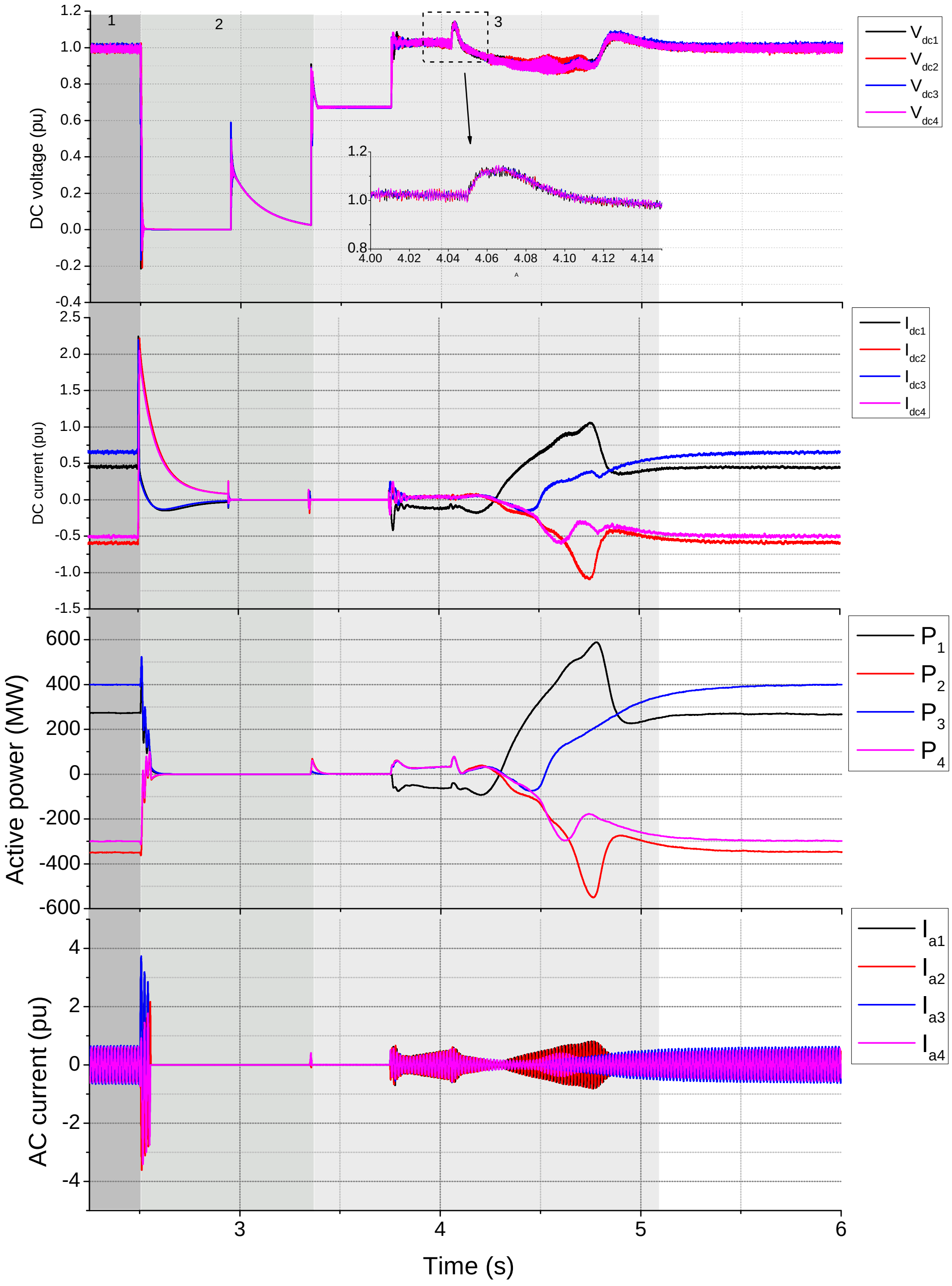


FIGURE 8.11: Simulation result for Scheme 2 with different control scheme.

achieve full recovery very quickly. On the contrary, Scheme 1 takes the longest time to resume operation in the event of DC fault. The prolonged fault clearance poses a risk to anti-parallel diodes for having to withstand large and increasing fault current. Scheme 2 can be said as the improved version of Scheme 1. The turning-on of double-thyristor not only takes current stress from diodes, it also allows the DC current to decline at higher rate, and hence faster recovery. In the case when the cost of hybrid DC CB is of great concern, Scheme 2 will be an optimum solution.

It will be interesting to investigate how the MMC working under different control scheme will behave going through the same recovery sequence. In the case with the reactive power control, the Q_{ref} is set at 0. It has been shown in the result that this control scheme is able to contain the transient within the constraint during the recovery. Fig. 8.11 shows the recovery performance for Scheme 2 with the control scheme now replaced with AC voltage control. It follows the same sequence timing as depicted in Table 8.2. After deblocking MMC, a fairly significant DC voltage surge appears around 4 s, reaching a peak of 1.145 pu. The DC voltage suffers dip and oscillation more severe in comparison to what is observed in Fig. 8.9. In addition, the I_{dc1} and I_{dc2} see slight surge amid the recovery process. Without proper control of reactive power, the transient stability becomes , but it takes about the same time as its counterpart to resume operation. This shows that proper control of reactive power has a contribution on transient stability [109].

8.5 Summary

Three protection schemes for multi-terminal HVDC system, as listed below, are investigated in this chapter:

- Scheme 1: AC CB, DC switch
- Scheme 2: AC CB, double-thyristor, DC switch
- Scheme 3: AC CB, hybrid DC CB

The performance of these schemes has been assessed in term of the time it takes to clear the DC fault and achieve restoration to normal operation. The recovery needs to be strategically executed so that the HVDC system will not experience overreaching transients, for which the sequence has been presented in this chapter. The overcurrent and overvoltage constraints are also introduced and used as the rule when deciding the time for the recovery sequence.

The results have demonstrated that the three protection schemes can achieve smooth recovery with voltage spike and current surge under control. Scheme 3 stands out to be the best protection scheme as far as the recovery time is concerned. Because hybrid DC CB can clear the fault fast enough, it does not cause total shut down of entire system, therefore the recovery can pick up reasonably quick. Scheme 1 is the most economical since no additional device is required and the AC CB is already used for the protection on AC side, however it takes the longest time to see the fault current extinguished and the system to recover. Scheme 2, with the double-thyristor, appears to substantially improve the performance of Scheme 1, by having faster recovery process.

Chapter 9

Conclusion

The DC fault transient in VSC-HVDC systems had been analytically studied, allowing us to have a better understanding of signatures associated with the DC fault. In lead-up to proposal of fault detection methods, the models of multi-terminal HVDC systems were built in the PSCAD/EMTDC environment. A DC experimental hardware based on two-level VSC was developed to obtain real fault signal in an effort to add credibility to the result. In this thesis, three fault detection methods were proposed. They were expected to meet the requirements which we highlighted right from the beginning: selectivity, robustness and speed. The performance of these methods were evaluated in simulation and experiment. The three important characteristics were assessed by testing these methods in various fault conditions. It was demonstrated that the DC fault can be effectively detected in very short time. They presented the ability to discriminate against the external faults and events in which DC CB should not trip. Furthermore, they were able to accurately capture the fault signature notwithstanding the influence of fault resistance and distance. Following the fault detection, the recovery sequence for the proposed three protection schemes in multi-terminal HVDC system was investigated.

9.1 DC Fault Detection in VSC-HVDC System

9.1.1 Wavelet-based Fault Detection

The application of wavelet transform to detect DC fault in HVDC systems had been studied. The methods of choosing the mother wavelet suited for DC fault was presented, based on time delay and its correlation to fault pattern. It was found that $db3$ was the most ideal mother wavelet. The DC fault was quantitatively detected by wavelet coefficient. Its performance was tested against the influence of fault location, resistance and distance. The investigation of relationship between sampling rate and detection speed showed that high sampling rate was preferable for fast detection. The analysis was further extended to validation using results from a scaled-down DC hardware setup. The wavelet transform was effective enough to differentiate load change from DC fault. The noise in the experimental result gave rise to non-zero wavelet coefficient during steady state. This can be improved by removing the unwanted noise using right filter while still retaining the high frequency content generated by the fault-induced transient.

9.1.2 Capacitive Discharge-based Fault Detection

The fault detection based on capacitive discharge was tested on the fault signals obtained from simulation and experiment, from which different fault types and conditions were investigated. Under certain critical fault conditions, the fault-induced transient can be quite weak for fault detection to work properly. However, we observed that this fault detection method was minimally influenced by the fault location and resistance. It was demonstrated that the DC fault could be detected within 1 ms. Another important feature of this fault detection method is the ability to distinctly recognize the bus fault and external faults, such AC fault and sudden blocking of gate signal. Without requiring complex signal processing, this method is computationally inexpensive. Besides that, it only requires the local measurement at the terminal to perform necessary calculation.

9.1.3 STFT-based Fault Detection

In Chapter 7, it was shown how the DC fault was associated with a consistently observable pattern change in the frequency spectrum of DC current. Based on this phenomenon, the STFT was used to detect the DC fault. The effectiveness of this method was strongly substantiated by both simulation and experimental results. The faulted line in multi-terminal HVDC system could be identified without the need of inter-terminal communication. Detection time as fast as 1 ms was achievable. This method was able to distinguish the DC fault from AC fault and load change. Moreover, the influences of fault resistance and distance on this method were insignificant.

9.1.4 Performance Comparison

The comparison and ranking of wavelet, capacitive discharge and STFT methods, based on the experimental validation as well as the simulation for MTDC system, are presented in Table 9.1. The following comments are cited on the proposed fault detection methods and difference in their performances:

1. The proposed capacitive discharge and STFT methods identify faulted line in MTDC by only sourcing locally accessible measurement. From the technical point of view, the elimination of communication facility cuts down the complexity of designing protection system, as well as the cost. Besides that, current sensor alone is sufficient to provide the necessary measurement, instead of voltage sensor which is arguably more expensive due to size and added insulation.

2. Time domain-based method provides faster DC fault detection than its counterpart in frequency domain. In real-time application, the signal is essentially sampled in time domain. Hence, to analyze the signal in frequency domain using FFT, or multi resolution analysis for wavelet, involves convolution and complex number resulting in time delay. In this case, the fault signature is captured the fastest by the capacitive discharge method.

3. The capacitive discharge, as a fault phenomenon itself, is unaffected by the fault parameters (resistance and distance). Therefore, the capacitive discharge method is very reliable with respect to fault detection. That being said, it can only work on the VSC-based DC system in which the DC-link capacitor is inherently available.

4. The experimental validation showcases the performance of each method in the presence of noise. The STFT method appears to be especially vulnerable to noise as it can be seen that frequency spectrum is already distorted to certain extent during normal operation, as opposed to the simulation result. To resolve this issue, one can consider to filter out the high order frequency component while preserving the one associated with fault.

5. The FFT algorithm allows the STFT method to execute the fault detection most efficiently. For wavelet method, the computational delay is caused by the cascaded filtering process. *db*3, which is used in this paper, has 6 coefficients in the filter. The algorithm to calculate the correlation coefficient in capacitive discharge method (see (6.2)) involves shifting signal along x-axis, in a fashion similar to cross correlation, resulting in high computational burden.

6. The capacitive discharge method detects the fault by comparing the patterns of DC line current and capacitive discharge based on their mutual similarity, hence

the same threshold is applicable in both experimental and simulation validations. In contrast, the wavelet and STFT methods adopt hard threshold, which means that the value tends to vary when used in different system.

Table 9.1: Performance comparison of fault detection methods.

	Wavelet transform	Capacitive discharge	STFT
No. of signals	1	2	1
Detection time (1=fastest)	3	1	2
Sensitivity to fault resistance (1=most robust)	3	1	2
Sensitivity to fault distance (1=most robust)	3	1	2
Selectivity in MTDC grid	√	√	√
Average computation time (1=fastest)	2	3	1

9.2 DC Fault Clearance in VSC-HVDC System

Three protection schemes consisting of AC CB, double-thyristor and hybrid DC CB were proposed and studied. The recovery strategy such as the sequence of re-activation of MMC operation and reclosing of CB was outlined. The recovery sequence was strategically timed so that the current surge and voltage spike adhered to the constraints introduced in this thesis. The protection schemes were tested in a multi-terminal HVDC system. The results showed that the scheme involving hybrid DC CB provided the fastest recovery. The AC CB took the longest time to clear the fault, hence its corresponding scheme had the poorest recovery performance. This could be substantially improved by employing the double-thyristor. Nevertheless, with the proposed recovery strategy, it was observed that all the protection schemes achieved good recovery with minimal transients.

9.3 Future Work

In this section, we review some of the possible future researches that can be extended from the work presented in this thesis. These are mentioned below.

9.3.1 Role of HVDC Control Strategies in Protection

In addition to detecting the fault, it is equally important to ensure that the normal operation of HVDC system is not compromised during the post-fault period. When fault happens the affected terminal is completely shut down by protection system until the fault is cleared. The change of circuit induces temporary shock to the system resulting in very high transient current, similar to the inrush current drawn by motor when first turned on. Due to the fact that the operation of HVDC system is tightly dependent on its control system, the performance of different types of control strategies during the post-fault period will be the focus area here.

9.3.2 Research on Overvoltage Protection in HVDC System

Back flashover generally occurs when lightning strikes on overhead shield wire, consequently the potential of tower rises exponentially beyond the degree insulation can withstand and the conductor is short-circuited to the tower. The analysis has been widely reported for the AC power transmission, but it is still an opening question in the domain of HVDC. Hence, this research will investigate the impact of lightning on HVDC overhead line and accordingly recommend the protection requirement.

If lightning is said to be the natural source of overvoltage, then man-made source will be the overvoltage due to switching. This phenomenon can be due to the change of circuit, for example, switching on or off inductive loads. Our research aims to address this issue, it is important given the potential of future multi-terminal HVDC grid with the renewable sources coming into picture.

9.3.3 Discussion on HVDC Protection Standard

The vision of implementing inter-regional MTDC will not be practically realized until a definitive standard governing the DC protection is established. The absence of standard in DC domain fails to form a guideline that unifies the protection design and provide interoperability between protective devices from different vendors. More efforts are necessary to fill up what has been missing in DC protection so as to match its AC counterpart, for which the well-known standard is IEC 61850. While such standard for DC system is still missing, it can borrow the existing framework from IEC 61850 [110]. In the standard, basic protocol to transfer data between the products from different vendors is defined. Clear understanding of DC fault detection is required to decide on requirement for communication speed in order to achieve substation automation. It would be interesting to link the discussion on the DC protection standard with the proposed fault detection method in this thesis.

Author's Publications

Journal Papers (listed in the order of submission time)

[1] **Y. M. Yeap** and N. Geddada and A. Ukil. Analysis and Validation of Wavelet Transform Based DC Fault Detection in HVDC System. *Applied Soft Computing*, vol 61, pp 17-29, Dec 2017. doi: 10.1016/j.asoc.2017.07.039

[2] **Y. M. Yeap** and N. Geddada and A. Ukil. Capacitive Discharge Based Transient Analysis in Multi-terminal HVDC System. *International Journal of Electric Power and Energy System*, vol 97, pp 127-137, Apr 2018. doi: 10.1016/j.ijepes.2017.10.023

[3] K. Satpathi and **Y. M. Yeap** and N. Geddada and A. Ukil. Short-time Fourier Transform Based Transient Analysis of VSC Interfaced DC Networks. *IEEE Transactions on Industrial Electronics*, vol. 65, no. 5, pp. 4080-4091, May 2018. doi: 10.1109/TIE.2017.2758745 [Yeap's contribution: proposed concept of STFT-based fault detection, constructed DC system experimental setup, analyzed experimental result using STFT.]

[4] N. Geddada and **Y. M. Yeap** and A. Ukil. Experimental Validation of Fault Identification in VSC Based DC Grid System. *IEEE Transactions on Industrial Electronics*, vol. 65, no. 6, pp. 4799-4809, June 2018. doi: 10.1109/TIE.2017.2767560 [Yeap's contribution: constructed DC system experimental setup, analyzed simulation and experimental results using wavelet transform and di=dt method.]

[5] **Y. M. Yeap** and N. Geddada and K. Satpathi and A. Ukil. Time and Frequency Domain Fault Detection in VSC Interfaced Experimental DC Test System. *IEEE Transactions on Industrial Informatics*, 2018 (in press). doi: 10.1109/TII.2018.2796068

Conference Papers (listed in the order of submission time)

[1] **Y. M. Yeap** and A. Ukil. Wavelet based fault analysis in HVDC system. In *IECON 2014-40th Annual Conference of the IEEE Industrial Electronics Society*, 2472-2478, Dallas, USA, Nov 2014.

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[Yeap's contribution: assisted Lee in building simulation model.]

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[Yeap's contribution: constructed DC system experimental setup, analyzed simulation and experimental results using wavelet transform.]

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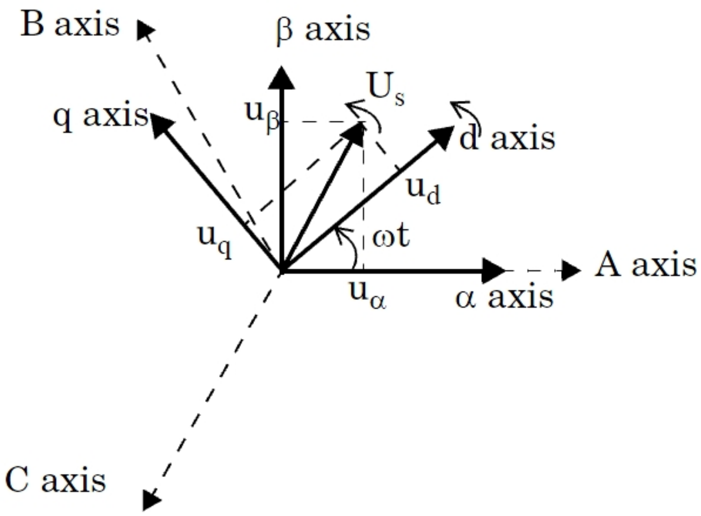
abc $\rightarrow$ dq0

Consider the three-phase voltage of a system to be following:

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} V_m sin(wt) \\ V_m sin(wt + \frac{2\pi}{3}) \\ V_m sin(wt - \frac{2\pi}{3}) \end{bmatrix} \tag{1}$$

Apply $\alpha\beta$ transformation:



$$\begin{bmatrix} V_\alpha \\ \\ V_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2}) \end{bmatrix} \begin{bmatrix} V_a \\ \\ V_b \\ \\ V_c \end{bmatrix}$$

$$= \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2}) \end{bmatrix} \begin{bmatrix} V_m sin(wt) \\ \\ V_m sin(wt + \frac{2\pi}{3}) \\ \\ V_m sin(wt - \frac{2\pi}{3}) \end{bmatrix}$$

(2)

$$= \begin{bmatrix} \frac{2V_m}{3}[sin(wt) - \frac{1}{2}sin(wt + \frac{2\pi}{3}) - \frac{1}{2}sin(wt - \frac{2\pi}{3})] \\ \\ \frac{\sqrt{3}V_m}{3}[sin(wt + \frac{2\pi}{3}) - sin(wt - \frac{2\pi}{3})] \\ \\ \frac{V_m}{3}[sin(wt) + sin(wt + \frac{2\pi}{3}) + sin(wt - \frac{2\pi}{3})]) \end{bmatrix}$$

$$= \begin{bmatrix} V_m sin(wt) \\ \\ V_m cos(wt) \\ \\ 0 \end{bmatrix}$$

Apply Park's transformation:

$$\begin{bmatrix} V_d \\ \\ V_q \end{bmatrix} = \begin{bmatrix} sin(\theta) & cos(\theta) \\ \\ cos(\theta) & -sin(\theta) \end{bmatrix} \begin{bmatrix} V_\alpha \\ \\ V_\beta \end{bmatrix} \tag{3}$$

Assume the d-axis is aligned with the voltage, so $\theta = wt$ yields:

$$\begin{bmatrix} V_d \\ \\ V_q \end{bmatrix} = \begin{bmatrix} V_m sin(wt) sin(wt) + V_m cos(wt) cos(wt) \\ \\ V_m cos(wt) sin(wt) - V_m sin(wt) cos(wt) \end{bmatrix}$$

$$= \begin{bmatrix} V_m \\ \\ 0 \end{bmatrix} \tag{4}$$

Calculation of PI Parameters

```
Vp_peak=85/1.732*1.414 %Single phase voltage peak


%AC filter

L=10e-3;

R=0.1;


C=2350e-6; %DC link capacitor


V_d=Vp_peak/(sqrt(2/3)) %d-axis voltage

V_dc=250 %DC voltage

syms s

a=4


T_sw=1/10000; %switching frequency

Ta=T_sw;

Wb=314.1592; %line frequency

Tow=L/R; %time constant of system

Ti=Tow;


%determine kp & ti of inner current controller

num_P=1;

den_P=sym2poly(R*(1+Tow*s));

P=tf(num_P,den_P);


num_D=1;

den_D=sym2poly(1+s*Ta);
```

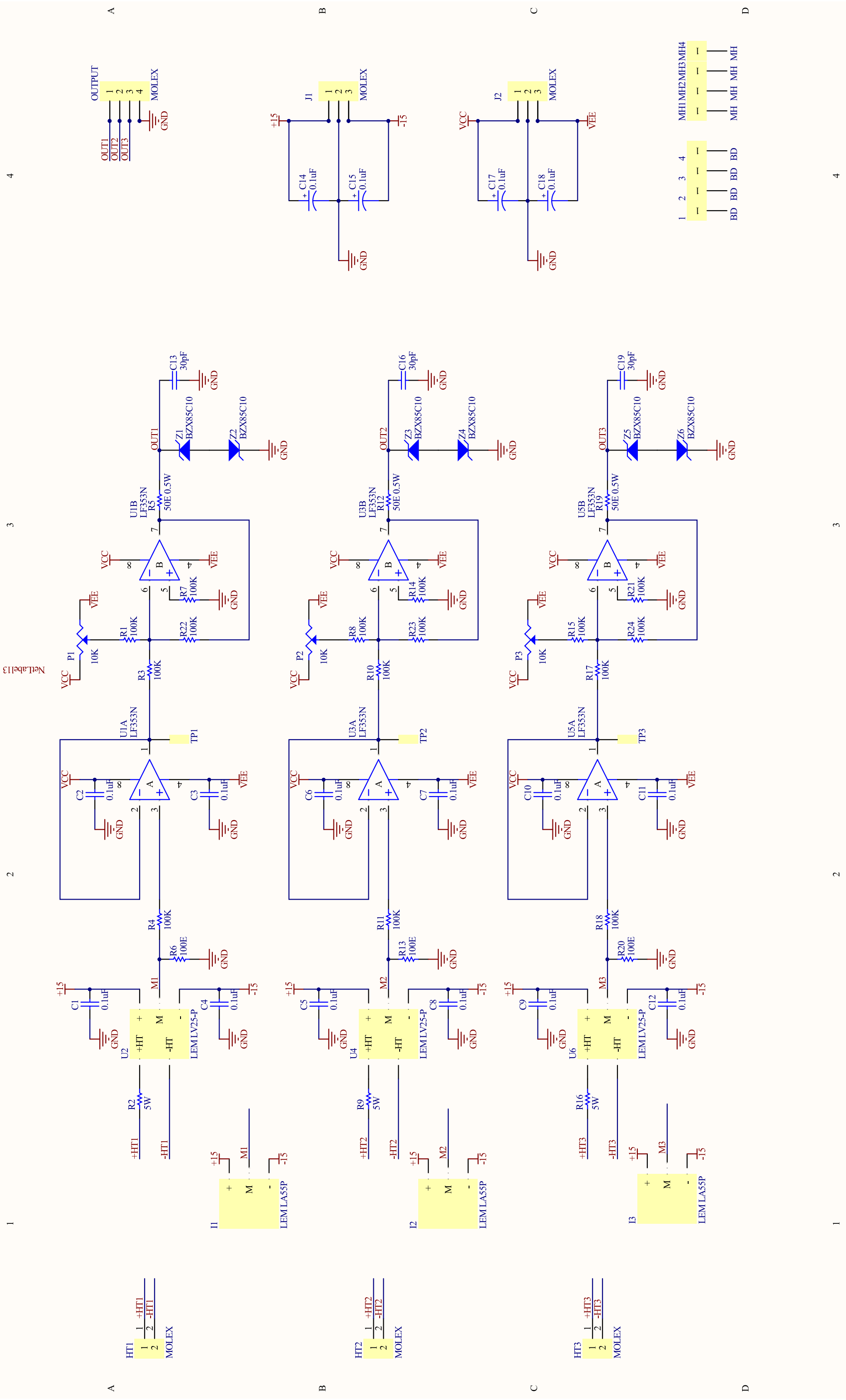
```
D=tf(num_D,den_D);


Kp_c=(L)/(2*Ta)
num_PI=sym2poly(Kp_c*(1+s*Ti));
den_PI=sym2poly(s*Ti);


PI=tf(num_PI,den_PI)


G_col=PI*D*P; %open loop tf


H=1;
G_ccl=feedback(G_col,H); %close loop tf


figure(1)
bode(G_col)
hold on
bode(G_ccl)
grid on


figure(2)
step(G_ccl)


figure(3)
rlocus(G_col)


%determine kp & ti of DC voltage controller
T_eq=2*Ta;


T_iv=a*a*T_eq;
T_c=Wb*C;


K=(3*V_d)/(2*V_dc);


num_Pdc=K;
den_Pdc=sym2poly(T_c*s);
Pdc=tf(num_Pdc,den_Pdc);
```

```
num_Ddc=1;

den_Ddc=sym2poly(1+s*T_eq);

Ddc=tf(num_Ddc,den_Ddc);


Kpv=1/(T_c*a*K*T_eq)

num_PIdc=sym2poly(Kpv*(1+s*T_iv));

den_PIdc=sym2poly(s*T_iv);

PIdc=tf(num_PIdc,den_PIdc);


Kiv=Kpv/T_iv


G_vol=PIdc*Ddc*Pdc; %open loop tf


H=1;

G_vcl=feedback(G_vol,H); %close loop tf


figure(4)

bode(G_vol)

hold on

bode(G_vcl)

grid on


figure(5)

rlocus(G_vol)


figure(6)

step(G_vcl)
```

Listing 1: Calculation of PI parameters

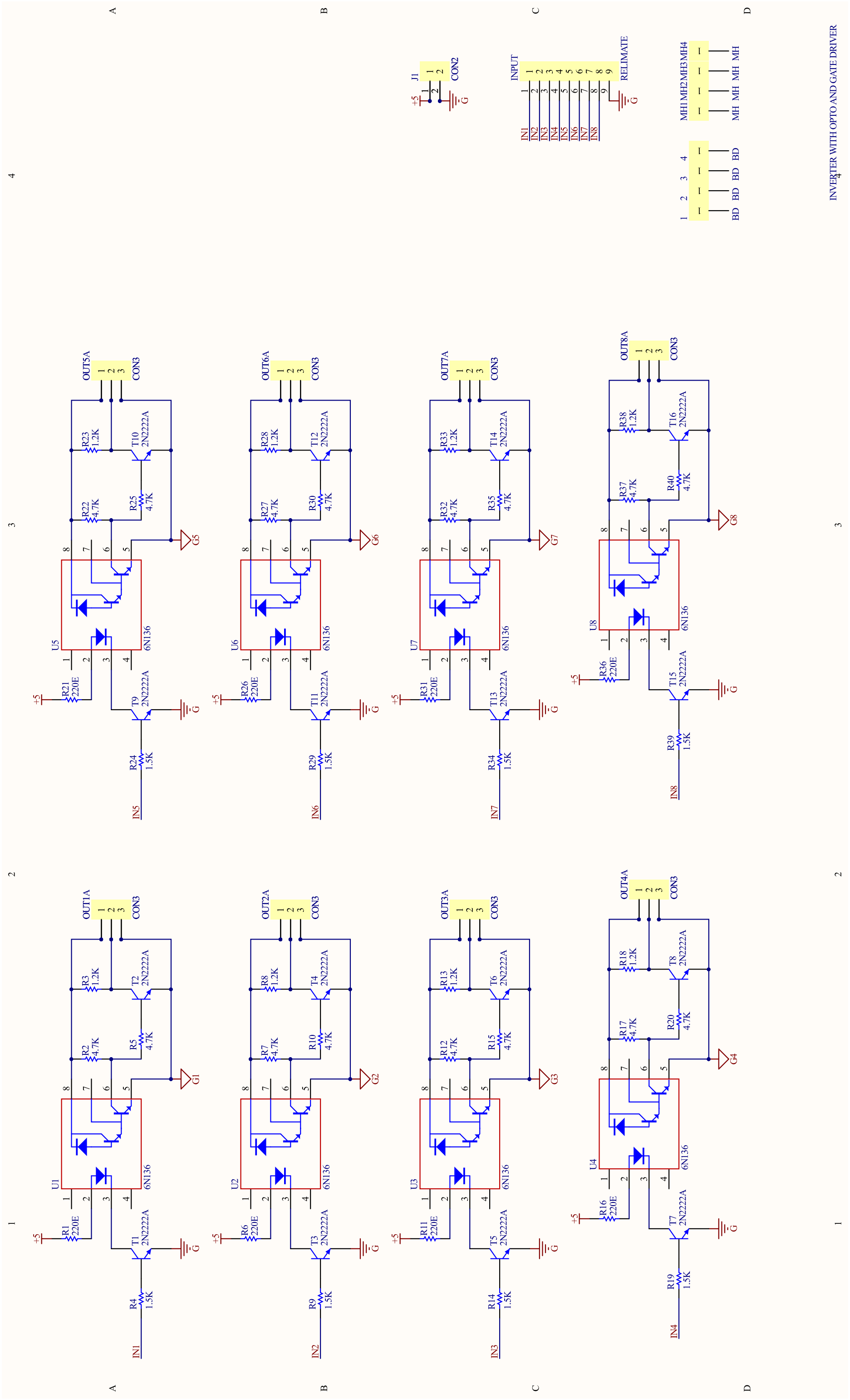
Voltage and Current Sensor Circuit

Comment	Description	Designator	Footprint	LibRef	Quantity
BD	MOUNTING HOLE	1, 2, 3, 4	BD	MH	4
0.1uF	Capacitor	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12	RAD0.2A	CAP	12
30pF	Capacitor	C13, C16, C19	RAD0.2A	CAP	3
0.1uF	Capacitor	C14, C15, C17, C18	TANC	CAPACITOR POL	4
MOLEX	Connector	HT1, HT2, HT3	MOLEX 200-2	CON2	3
LEM LA55P		I1, I2, I3	LEM LA55P	LEM LA55P	3
RELIMATE	Connector	J1, J2	100-3/2	CON3	2
MOLEX	Connector	J1A, J2A	MOLEX 200-3	CON3	2
MH	MOUNTING HOLE	MH1, MH2, MH3, MH4	MH3	MH	4
RELIMATE	Connector	OUTPUT	100-4/2	CON4	1
MOLEX	Connector	OUTPUTA	MOLEX 200-4	CON4	1
10K	Potentiometer	P1, P2, P3	POT23A	POT1	3
Res1	Resistor	R1, R3, R4, R6, R7, R8, R10, R11, R13, R14, R15, R17, R18, R20, R21, R22, R23, R24	AXIAL-0.4	Res1	18
Res1	Resistor	R2, R9, R16	AXIAL1.2	Res1	3
Res1	Resistor	R5, R12, R19	AXIAL0.5	Res1	3
	TEST POINT	TP1, TP2, TP3	TP1	TP	3
LF353N	Wide-Bandwidth Dual J-FET Operational Amplifier	U1, U3, U5	DIP8	LF353N	3
LEM LV25-P		U2, U4, U6	LEM LV25-P	LEM LV25-P	3
BZX85C10	Silicon Epitaxial Plana	Z1, Z2, Z3, Z4, Z5, Z6	DO41	BZX85C10	6


OUTPUT
MOLEX
OUT1
OUT2
OUT3
GND
J1
J2
+15
-15
VCC
VEE
C14 0.1uF
C15 0.1uF
C17 0.1uF
C18 0.1uF
MH1 MH2 MH3 MH4
MH
BD
C13 30pF
C16 30pF
C19 30pF
Z1 BZX85C10
Z2 BZX85C10
Z3 BZX85C10
Z4 BZX85C10
Z5 BZX85C10
Z6 BZX85C10
U1B LF353N
U3B LF353N
U5B LF353N
R5 50E 0.5W
R12 50E 0.5W
R19 50E 0.5W
R7 100K
R14 100K
R21 100K
R1 100K
R8 100K
R15 100K
R22 100K
R23 100K
R24 100K
P1 10K
P2 10K
P3 10K
R3 100K
R10 100K
R17 100K
NetLabel13
U1A LF353N
U3A LF353N
U5A LF353N
TP1
TP2
TP3
C2 0.1uF
C3 0.1uF
C6 0.1uF
C7 0.1uF
C10 0.1uF
C11 0.1uF
R4 100K
R11 100K
R18 100K
R6 100E
R13 100E
R20 100E
M1
M2
M3
C1 0.1uF
C4 0.1uF
C5 0.1uF
C8 0.1uF
C9 0.1uF
C12 0.1uF
U2
U4
U6
+HT
-HT
LEM LV25-P
R2 5W
R9 5W
R16 5W
+HT1
-HT1
+HT2
-HT2
+HT3
-HT3
I1
I2
I3
LEM LA55P
HT1
HT2
HT3
A
B
C
D
1
2
3
4

Opto-coupler Gate Driver Circuit

Comment	Description	Designator	Footprint	LibRef	Quantity	Value
BD	MOUNTING HOLE	1, 2, 3, 4	BD	MH	4	
RELIMATE	Connector	INPUT	100-9/2	CON9	1	
CON2	Connector	J1	MOLEX 200-2	CON2	1	
CON2	Connector	J1A	100-2/2	CON2	1	
MH	MOUNTING HOLE	MH1, MH2, MH3, MH4	MH3	MH	4	
CON3	Connector	OUT1, OUT2, OUT3, OUT4, OUT5, OUT6, OUT7, OUT8	MOLEX 200-3	CON3	8	
CON3	Connector	OUT1A, OUT2A, OUT3A, OUT4A, OUT5A, OUT6A, OUT7A, OUT8A	100-3/2	CON3	8	
Res1	Resistor	R1, R6, R11, R16, R21, R26, R31, R36	AXIAL-0.4	Res1	8	220E
Res1	Resistor	R2, R5, R7, R10, R12, R15, R17, R20, R22, R25, R27, R30, R32, R35, R37, R40	AXIAL-0.4	Res1	16	4.7K
Res1	Resistor	R3, R8, R13, R18, R23, R28, R33, R38	AXIAL-0.4	Res1	8	1.2K
Res1	Resistor	R4, R9, R14, R19, R24, R29, R34, R39	AXIAL-0.4	Res1	8	1.5K
2N2222A	High Speed Switches	T1, T2, T3, T4, T5, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16	TO-18	2N2222A	16	
6N136	High Sensitivity, High Speed OPIC Photocoupler	U1, U2, U3, U4, U5, U6, U7, U8	DIP8	6N139	8	
INVERTER WITH C	LOGO VEPL	VEPL5659-011112	VEBM	VEPLLOGO	1	


INVERTER WITH OPTO AND GATE DRIVER
U1
U2
U3
U4
U5
U6
U7
U8
6N136
T1 2N2222A
T2 2N2222A
T3 2N2222A
T4 2N2222A
T5 2N2222A
T6 2N2222A
T7 2N2222A
T8 2N2222A
T9 2N2222A
T10 2N2222A
T11 2N2222A
T12 2N2222A
T13 2N2222A
T14 2N2222A
T15 2N2222A
T16 2N2222A
R1 220E
R2 4.7K
R3 1.2K
R4 1.5K
R5 4.7K
R6 220E
R7 4.7K
R8 1.2K
R9 1.5K
R10 4.7K
R11 220E
R12 4.7K
R13 1.2K
R14 1.5K
R15 4.7K
R16 220E
R17 4.7K
R18 1.2K
R19 1.5K
R20 4.7K
R21 220E
R22 4.7K
R23 1.2K
R24 1.5K
R25 4.7K
R26 220E
R27 4.7K
R28 1.2K
R29 1.5K
R30 4.7K
R31 220E
R32 4.7K
R33 1.2K
R34 1.5K
R35 4.7K
R36 220E
R37 4.7K
R38 1.2K
R39 1.5K
R40 4.7K
IN1
IN2
IN3
IN4
IN5
IN6
IN7
IN8
G1
G2
G3
G4
G5
G6
G7
G8
OUT1A
OUT2A
OUT3A
OUT4A
OUT5A
OUT6A
OUT7A
OUT8A
CON3
+5
G
J1
CON2
INPUT
RELIMATE
MH1 MH2 MH3 MH4
MH
BD
A
B
C
D
1
2
3
4

Wavelet Transform Code

```
%Copyright: Abhisek Ukil
clear all


%---------------------------- Inputs -------------------------------
filename='fault.txt'


a=load(filename); %load signal txt file. First column is time, second column is current


signal=a(:,2);



%------------------------------------------------------------------


%---------------------------- Wavelet analysis ----------------------


mother='db3'; %db1-db10, sym1-5, coif1-4


 for scale=1:7
     [XA,XD]=waveletdecom(signal,mother,scale);


     close all
     pos1=[100 50 600 600];
     figure('Position',pos1)
     subplot(311),plot(signal,'*-'),title(num2str(scale)),grid on,
     ylabel('Fault signal'), xlabel('Sample number');axis tight
     subplot(312),plot(XD,'*-'),title('Wavelet: Detailed (freq) coefficients'),grid on,
```

```
    ylabel('Wavelet coefficient'), xlabel('Sample number');axis tight

    subplot(313),plot(XA,'*-'),title('Wavelet: Smoothed (time) coefficients'),grid on,

    ylabel('Wavelet coefficient'), xlabel('Sample number');axis tight

    pause


 end


drawnow;

pause;




function [XA,XD]=waveletdecom(data,mother,scale)


N_total=size(data,2);

XA=[]; XD=[];

for i=1:N_total

%x=data(i,:); %220 value

x=data(:,i); %220 value

S=scale;

while S>=1

[CA,CD]=dwt(x,mother);

S=S-1;

x=CA;

end

XA([1:numel(CA)],end+1)=CA; %Use smoothed version

XD([1:numel(CD)],end+1)=CD; %Use detailed version

end
```

Listing 2: Wavelet transform code

Short-time Fourier Transform Code

```
clear, clc, close all

%%%input%%%

a=load('fault.txt'); %load fault signal txt file, first column is time,
%second column is current
fs = 10000; %sampling frequency
t = 0:1/fs:3;

col=2;
vref=a(:,col);
row=size(vref,1);

%%%performing stft%%%

x = vref;
siglen = row; %size of the signal
winlen =1024; %window length
hop = winlen/16; %hop size
nfft = 1024; %number of fft points

K = sum(hann(winlen))/winlen;
```

```
[s4, f4, t4] = stftnew1(x, winlen, hop, nfft, fs);



s41 = abs(s4)/winlen/K;

%%%correction of the DC & Nyquist component%%

if rem(nfft, 2) %odd nfft excludes Nyquist point
s41(2:end, :) = s41(2:end, :).*2;
else  %even nfft includes Nyquist point
s41(2:end-1, :) = s41(2:end-1, :).*2;
end

%%%convert amplitude spectrum to dB (min = -120 dB)%%%

s41 = 20*log10(s41);

%%%plotting%%%
figure(1)
imagesc(t4, f4, s41);
set(gca,'YDir','normal')
set(gca, 'FontName', 'Times New Roman', 'FontSize', 14)
xlabel('Time, s')
ylabel('Frequency, Hz')
title('Amplitude spectrogram of the signal')
%
handl = colorbar;
set(handl, 'FontName', 'Times New Roman', 'FontSize', 14)
ylabel(handl, 'Magnitude, dB')

figure(2);
hop=surf(t4,f4,s41);
set(hop,'LineStyle','none');

figure(3);
```

```
h1=contourf(t4,f4,s41);



function [stft, f, t] = stftnew1(x, winlen, hop, nfft, fs)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Author: M.Sc. Eng. Hristo Zhivomirov       12/21/13   %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%represent x as column-vector if it is not%%

if size(x,2) > 1
x = x';
end

%%%length of the signal%%%

xlen = length(x);

%%%apply window function%%%

win = hann(winlen,'periodic'); %other window: rectwin, hamming, nuttallwin



%%%form the stft matrix%%%

rown = ceil((1+nfft)/2);  %calculate the total number of rows
coln = fix((xlen-winlen+hop)/hop); %calculate the total number of columns
stft = zeros(rown, coln); %form the stft matrix

%%%initialize the indexes%%%

indx = 0;
col = 1;

%%%perform STFT%%%
while indx + winlen <= xlen
```

```
        xw = (x(indx+1:indx+winlen).*win); %windowing

        xw1 = fliplr(xw);

        xw = [xw xw1];



        X = fft(xw, nfft); %FFT



        stft(:,col) = X(1:(rown)); %update the stft matrix


%%%update the indexes%%%


        indx = indx + hop;

        col = col + 1;


end


%%%calculate the time and frequency vectors%%%

t = (winlen:hop:winlen+(coln-1)*hop)/fs;

f = (0:rown-1)*fs/nfft;

end
```

Listing 3: Short-time Fourier transform code