Design of a Wideband Variable-Gain Amplifier with Self-Compensated Transistor for Accurate dB-Linear Characteristic in 65 nm CMOS Technology

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***Abstract*—A simple yet effective approach for variable-gain amplifier (VGA) design with accurate dB-linear characteristic is presented. In order to extend the bandwidth of the designed VGA with a minimized footprint, an inductorless-based approach is adopted. Moreover, a unique approach that exploits a self-compensated transistor to compensate dB-linear gain error is proposed. Consequently, the overall VGA has an accurate dB-linear inherent characteristic without using any additional exponential generator for gain control. To prove the concept, the designed VGA is fabricated in a standard 65 nm CMOS technology. The measured results show that the voltage gain of the designed VGA can be controlled from -19 dB to 21 dB with a gain error less than 1 dB. Meanwhile, more than 4 GHz of bandwidth can be achieved for the entire gain range. The power consumption of the VGA, excluding the output buffer, is 3.9 mW. The core circuit of this design only occupies an area of 0.012 mm^2.**

***Index Terms*—CMOS variable-gain amplifier, dB-linear, pseudo-exponential function, Taylor series.**

I. Introduction

VARIABLE-GAIN AMPLIFIER (VGA) is an indispensable building block in analog domain due to its capability to provide a tunable gain to enlarge the overall system dynamic range [1]-[3]. Tremendous efforts have been invested in the last couple of decades to address the design issue related to VGA with broad bandwidth, low power consumption and accurate dB-linear characteristic [4]-[10]. Recently, the demand for big data analytics and artificial intelligence have resulted in an exponential growth for signal processing. The data rate of several Gbps is highly expected at analogue baseband, which requires the VGA to have not only an accurate gain control with good energy efficiency, but also cover a very broad bandwidth with a compact size [11]-[14].

Although designing a VGA with above-mentioned requirments in SiGe technologies can be easily achieved with its ultra-high f_T and intrinsic exponential I-V relationship of the BJT [15], it is still preferred to implement the design in a standard CMOS technology due to reduced fabrication cost. However, as a MOSFET follows a "square-law" function, an additional exponential generator is usually required for biasing a VGA and the dB-linear accuracy is heavily reliant of the performance of the exponential generator [9], [10]. The pseudo-exponential generator is a building block, which is designed to scale the relationship between the control voltage and gain of the VGA from a linear scale to a decibel scale. Thus, optimization of the exponential generator is the enabling factor for MOSFET-based VGA design with accurate dB-linear characteristic. Several approaches have been presented in the literature with most of them having an operating frequency in sub-GHz [5]-[10]. Until recently, a breakthrough has demonstrated that the MOSFET-based design has a potential to match the performance of an HBT-based one in terms of bandwidth and dB-linear accuracy [11], [12]. However, the power consumption of such design is still relatively high. It is rather complicated to design an energy-efficient VGA operating at multi-GHz range with accurate dB-linear characteristic, due to the trade-off among bandwidth, power consumption, dB-linearity and die size. Whenever a broadband technique is employed, it either consumes a high power [13], [14] or confines the architecture from additional exponential generation circuit [16]-[18]. In [16], an innovative approach is presented for wideband VGA design with minimized power consumption in 90 nm CMOS technology. Nevertheless, the presented approach is based on a classical Cherry-Hooper amplifier structure whose gain is dependent on the feedback resistor. For designs focusing on dB-linear accuracy and low power [19], [20], they usually occupy a large die area for a better matching and only suitable for narrow bandwidth applications due to the closed-loop topology.

As the exponential function generator also consumes a considerable amount of power, for low-power design, it is desirable to design a VGA with a self-dB-linear compensation scheme, so that the additional control circuit is not needed. To further explore the principle of exponential generation as well as wideband design technique, a summary of state-of-the-art design is given in Fig. 1. As illustrated in Fig. 1(a), a combination of two transistors with different oxide thicknesses is employed as source degenerative resistors along with a

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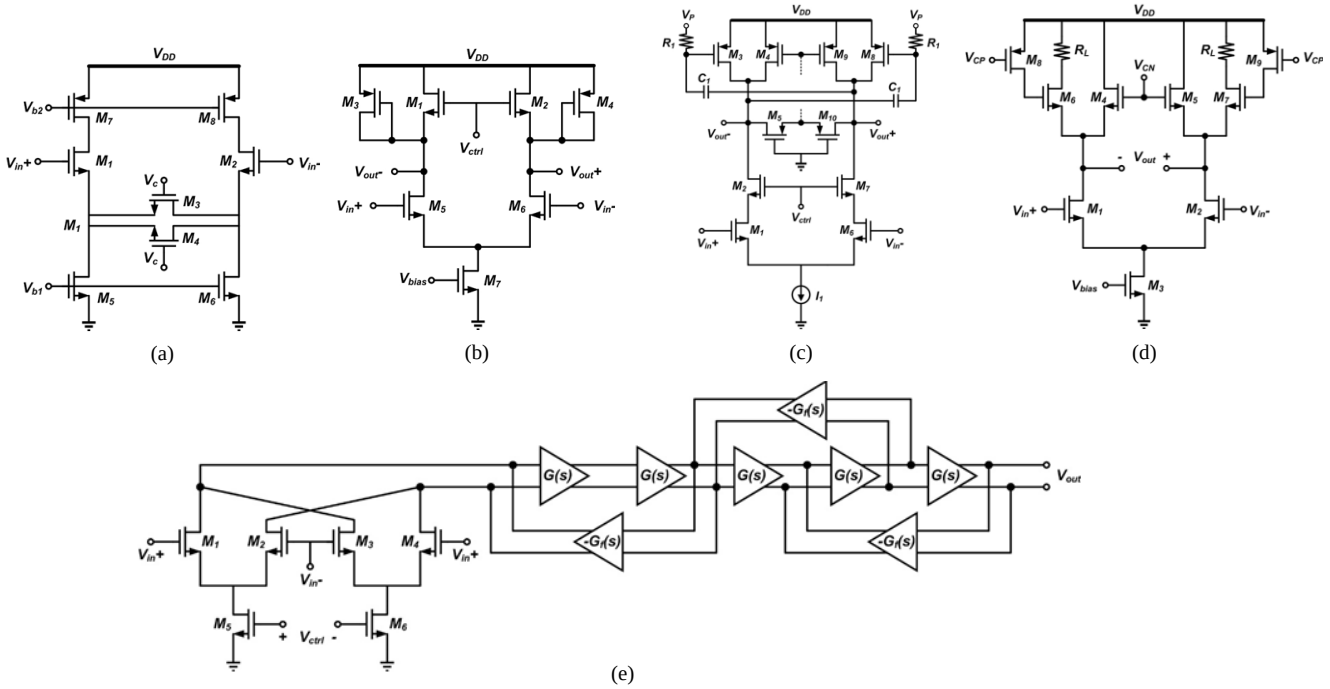


Fig.1. Various VGA topologies, (a) g_m-tuning with source degeneration, (b) current steering at load, (c) cross-coupled capacitors for gain peaking, (d) gate peaking, and (e) interleaved feedback loop.

differential amplifier to generate a linear function [21]. By cascading three of such cells, a pseudo-exponential function can be inherently observed, which is directly embedded within the VGA core. As a result, the designed VGA has a 50 dB gain range with a ±0.5 dB gain error without using any additional pseudo-exponential generator. Another design example is given in Fig. 1(b). Instead of using source-degenerated transistors at the input to control gain, adding a pair of transistors that operates at different region also works for dB-linear VGA design, as demonstrated in [22]. By carefully adjusting the bias condition of these two transistors, the current through each load transistor can be effectively controlled. In this way, a good dB-linear characteristic is achieved. The drawback of this approach is the constrained bandwidth due to parasitic capacitance accumulated at the output node, which hinders its implementation for high frequency VGAs.

In order to further increase the operation frequency, bandwidth extension techniques can be used. One of the well-known techniques is the inductive peaking, which is perhaps the most effective for energy-efficient wideband amplifier design. However, the spiral inductor is quite bulky and occupies a fairly large die area. Thus, inductor-less design attracts more attention recently. In Fig. 1(c), a pair of cross-coupled capacitors is used to generate transmission zero at higher frequency based on positive feedback, so that the overall bandwidth of the amplifier can be boosted [9]. However, the required capacitance within the feedback loop is relatively small, in the range of tens of *fF*. Such small capacitance is very sensitive and thus difficult to implement due to the existence of parasitic capacitance, which may on the contrary worsen the in-band gain flatness. In Fig. 1(d), a gate peaking technique is presented [23], which uses a similar idea with the one presented in Fig. 1(b) for dB-linear gain control, but it has a gain peaking near cut-off frequency with the assistance of transistors $M_{8,\,9}$. Since the "peaking" resistor is implemented by a MOSFET that operates in triode region, the location of transmission zero can be effectively controlled. As a result, the level of gain peaking can be well controlled by a bias voltage. Finally, a third-order interleaved feedback technique is shown in Fig. 1(e), which has also demonstrated a superior broadband performance. However, the implementation of this technique is more complicated than the previous ones. Moreover, the power consumption as well as in-band gain flatness may be of concern owing to multiple feedback loops [24], [25].

It is worth noticing that these designs can be categorized into two groups according to their gain-control principles. While topologies in Fig. 1(a), (c) and (e) adjust the overall gain by tuning their effective transconductance (g_m), the other two manipulate with the load impedance (R_{load}) of the amplifiers. Therefore, it is obvious that if both g_m and R_{load} can be tuned in the same direction, either increasing or decreasing simultaneously, an extended gain variation range could be expected.

In this paper, a four-stage inductor-less wideband VGA is designed and implemented in a 65 nm CMOS technology. The first and third stages are fixed-gain units that provide relatively high gain, while the second and fourth stages are variable gain units, which take advantage of self-compensated transistors to achieve an excellent dB-linear gain control without using any pseudo-exponential generator. The rest of this paper is organized as follows. The design of an accurate dB-linear unit cell with bandwidth extension is elaborated in Section II, followed by the overall VGA architecture presented in Section III. The measurement results of the proposed VGA are summarized in Section IV. Finally, Section V concludes the paper.

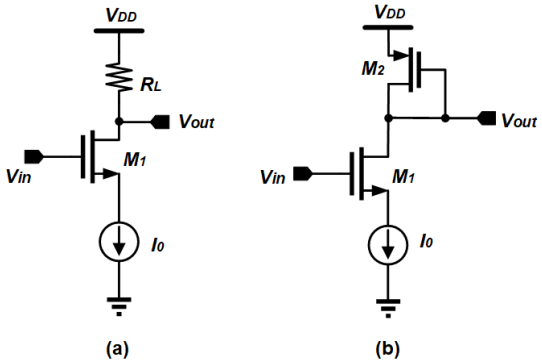


Fig. 2. Triode-based amplifiers with (a) resistor as load, and (b) diode-connected PMOS as load.

II. The Proposed Approach for VGA Design

A. Concept of Self-Compensated Transistor

The concept of self-compensated transistor is from the idea that the transconducance of a transistor as well as its output resistance can both contribute to gain tuning, and together create an exponentail function over a wide range if the transistor is biased properly. Considering the circuit shown in Fig. 2(a), a transistor, M_1, is biased in the triode region. I_0 is an ideal current source and R_L is the load resistor. The impact on transconductance of the transistor and the gain of the amplifier will be explored under different gate bias voltage as follows.

For a MOS device working in the triode region, its drain current is given by

$$I_D = K\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right] \quad (1)$$

where $K = \mu C_{ox} W/L$. μ is the charge-carrier effective mobility; C_{ox} is the gate oxide capacitance per unit area; W is the gate width; L is the gate length and V_{TH} is the threshold voltage. Since the current source is ideal, V_D is independent of the gate voltage. In order to produce the same drain current when V_G changes, V_S must change accordingly. Thus, V_S can be expressed w.r.t. V_G:

$$V_S = (V_G - V_{TH}) \pm \sqrt{(V_G - V_D - V_{TH})^2 + \frac{2I_D}{K}} \quad (2)$$

As the overdrive voltage $V_{ov} = (V_G - V_S - V_{TH}) > 0$, only the one with minus sign is applicable, obtaining

$$V_{DS} = -(V_G - V_D - V_{TH}) + \sqrt{(V_G - V_D - V_{TH})^2 + \frac{2I_D}{K}} \quad (3)$$

The transconductance, g_m, is the derivative of I_D w.r.t. V_{GS}, thus

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = KV_{DS} \quad (4)$$

By substituting (3) into (4), it becomes

$$g_m = K\left[-(V_G - V_D - V_{TH}) + \sqrt{(V_G - V_D - V_{TH})^2 + \frac{2I_D}{K}}\right] \quad (5)$$

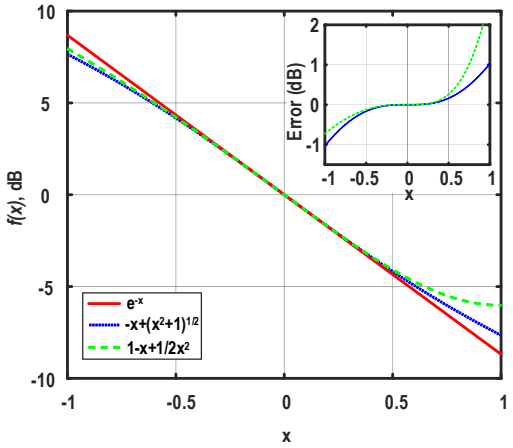


Fig. 3. Decibel scale plot of *f(x)* with comparison to Taylor series.

Thus, it can be simplified in the form of

$$g_m = K'\left(-x + \sqrt{x^2 + 1}\right) \quad (6)$$

with

$$K' = \frac{K}{\sqrt{2I_D/K}} \quad (7)$$

$$x = \frac{(V_G - V_D - V_{TH})}{\sqrt{2I_D/K}} \quad (8)$$

According to Taylor series,

$$\sqrt{x^2 + 1} \approx 1 + \frac{x^2}{2} \quad (9)$$

Hence,

$$g_m \approx K'e^{-x} \quad (10)$$

The comparison between Taylor series approximation and the new approximation function, $f(x) = -x + \sqrt{x^2 + 1}$, is illustrated in Fig. 3, showing that the new equation has a wider approximating range and smaller gain error, especially when x increases to 1. For a gain error of less than 0.5 dB, the x range is from -0.75 to 0.75, which corresponds to a gain range of 13 dB.

Meanwhile, the output resistance of the triode-biasing transistor is another issue of concern. It is different from the transistor working in the saturation region, whose output resistance is large and nearly constant. The output resistance of a triode-biasing transistor is comparable to the load resistor and varies while the biasing condition changes. The drain-to-source output conductance of the transistor operating at triode region is calculated from (1), i.e.

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = K(V_{GS} - V_{TH} - V_{DS}) = \sqrt{2I_D K} \cdot x \quad (11)$$

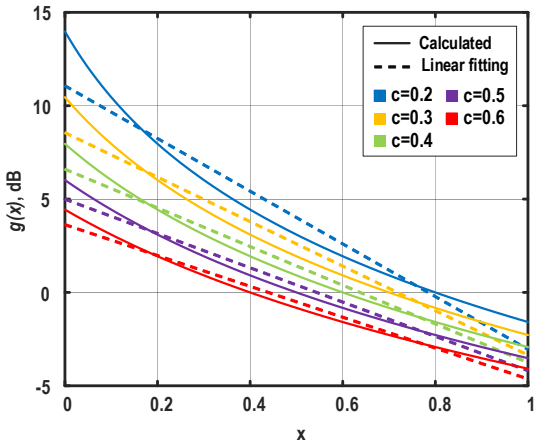


Fig. 4. The effect of c on $g(x)$ in logarithm scale.

If the load is replaced by a diode connected transistor as shown in Fig. 2(b), the output resistance can be written as

$$R_{total} = \frac{1}{g_{ds1} + g_{m2}} = \frac{1}{\sqrt{2I_D K_1} \cdot (c + x)} \tag{12}$$

with

$$c = \sqrt{K_2/K_1} \tag{13}$$

Although g_{ds1} is linearly proportional to the variable x, after paralleled with another transistor, the resultant output resistance exhibits a much smaller difference from the exponential funtion e^{-x}, if certain value of c is chosen. To illustrate this point, the function, $g(x) = 1/(c + x)$, is plotted in Fig. 4 with different values of c. It can be seen that within the same variable range as $f(x)$, $0 \le x \le 1$, a larger value of c results in a smaller change in $g(x)$ and a better dB-linearity. Therefore, by adjusting the sizing ratio of PMOS and NMOS transistor, it is promising to obtain a variable load resistance with little dB-linear error.

Recall that the overall gain of the amplifier depends on both transconductance and output resistance. By converting to dB scale, the following is obtained:

$$Gain\ range(dB) = change\ in\ gm\ (dB) + change\ in\ R_{total}\ (dB)$$

Therefore, we can exploit the feature of triode transistor, whose transconductance and output resistance changes simutaneouly in the VGA design to obtain an extended gain variation range. With careful optimization of the bias conditions, a wider gain variation range above 20 dB is feasible without sacrificing its dB-linear accuracy.

B. Proposed dB-Linear Variable Gain Amplifier Unit

The circuit schematic of the proposed wideband gain unit is shown in Fig. 5, which adopts a source coupled differential pair operating in the triode region and active inductors as load to extend its bandwidth.

1) Gain Error Compensation

The red curve in Fig. 6 depicts the operating algorithm of the input differential pair. As the control voltage increases, the overdrive voltage tends to increase, while the voltage at the output node is invariant due to the consistent operating

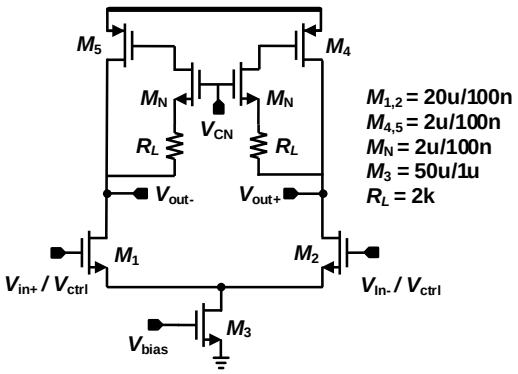


Fig. 5. Schematic of proposed variable gain unit.

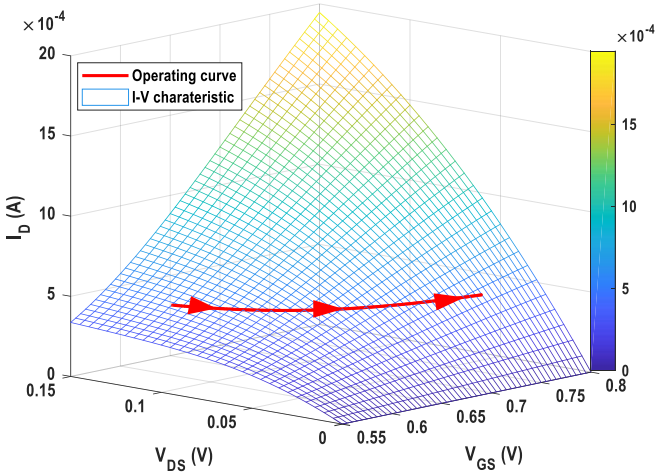


Fig. 6. I-V characteristic of the input transistor and its operating curve.

condition of load transistor. However, the current flows through the input transistors must be constant. It forces the source voltage of the input pair to be elevated, such that the drain-source voltage across the transistor is decreased. Together with the increased overdrive voltage, the input pair operates from moderate triode region to deep triode region and the resultant current remains constant.

The above mathematical analysis in Section *A* is based on the traditional characteristic equation, where all second-order effects and nonidealities are neglected. In order to have a more accurate analytical result which is consistent with the simulation result, these factors must be considered and included properly in the modified equation. With the continuous scaling of device dimensions to sub-micrometre, short-channel effects, such as threshold voltage variation, mobility degradation with vertical field, velocity saturation, etc., should not be neglected [23]. Examining on the proposed circuit, mobility degradation manifests itself strongly because the overdrive voltage is substantially high. This phenomenon can also be revealed from the I-V characteristic of the simulation result plotted in Fig. 6. Therefore, a more accurate equation to model the short channel device is given by

$$I_D = \frac{\alpha K[(V_{GS} - V_{TH})V_{DS}]}{1 + \theta(V_{GS} - V_{TH})} \tag{14}$$

where θ is a fitting parameter to describe the effect of mobility degradation with vertical field, and α is another fitting parameter to fit the calculated results with simulation results better. From the simulation, it is found that θ and α are 0.54 and 0.75, respectively. Thereafter, the transconductance is expressed as

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\alpha K V_{DS}}{[1+\theta(V_{GS}-V_{TH})]^2} \tag{15}$$

Realizing that I_D is always equal to half of the tail current and V_D is fixed due to invariant bias condition for the load transistor, we can solve V_S from the new current-voltage equation (14)

$$V_S = \frac{1}{2}\left[\left(V_G - V_{TH} + V_D - \frac{\theta I_D}{\alpha K}\right)\right] - \sqrt{\left(V_G - V_D - V_{TH} + \frac{\theta I_D}{\alpha K}\right)^2 + \frac{4I_D}{\alpha K}} \tag{16}$$

Therefore, its drain-source voltage and overdrive voltage are given by

$$V_{DS} = \frac{1}{2}\left[-(V_G - V_{TH} - V_D) + \frac{\theta I_D}{\alpha K} + \sqrt{\left(V_G - V_D - V_{TH} + \frac{\theta I_D}{\alpha K}\right)^2 + \frac{4I_D}{\alpha K}}\right] \tag{17}$$

$$V_{OV} = \frac{1}{2}\left[(V_G - V_{TH} - V_D) + \frac{\theta I_D}{\alpha K} + \sqrt{\left(V_G - V_D - V_{TH} + \frac{\theta I_D}{\alpha K}\right)^2 + \frac{4I_D}{\alpha K}}\right] \tag{18}$$

Thus, its transconductance can be expressed as equation (19) at the bottom of the page. With the active inductor as load, its load resistance is equivalent to a diode-connected transistor at low frequency. With a required gain range and dB-linear error given, the size of M_4 and M_5 can be determined. The simulation results of the input transconductance and overall output resistance are plotted in Fig. 7. Taking the value of g_m and R_{total} into logrithm scale, the variation range of g_m is from -46.6 to -55.6 dB, providing a change of 9 dB, while R_{total} is designed to vary from 36 to 48 dB, providing a change of 12 dB. As a result, a total of 21 dB can be expected from a single gain unit.

Interestingly, the changes of transconductance and output resistance in dB scale present a concave and a convex curve respectively, making them complementary to each other. The dB-linear error of g_m is positive when the error of R_{total} is negative as shown in Fig. 7, and vice versa. Overall, a reduced gain error can be expected from the simutaneous tuning of both the transconductance and output resistance.

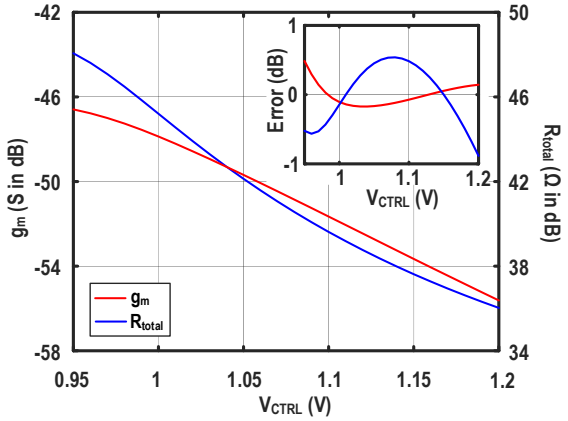


Fig. 7. Simulation results of g_m and R_{total} versus V_{CTRL} and their approximation error in dB-scale.

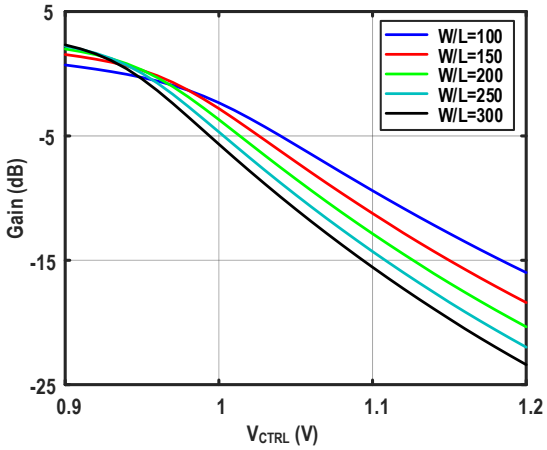


Fig. 8. Gain characteristic with different size of input transistors while L=100 nm.

To determine the best size of the transistors for the proposed design, simulation results of gain characteristic are compared as shown in Fig. 8. The length of the input transistor is fixed at 100 nm, in consideration of the threshold voltage, while its width is varied from 10 to 30 μm by a step size of 5 μm. It is observed that when a smaller transistor size is used, the transistors will enter into the triode region with a higher gate voltage, since higher overdrive voltage and drain-to-source voltage are required to attain the same current. Meanwhile, the slope of gain variation is gradual, leading to a lower gain range within a limited control voltage range, i.e. below the supply voltage of 1.2 V. As the aspect ratio of the input transistors increases, triode operation occurs at a lower control voltage while the slope becomes steeper. Therefore, the gain variation range is extended, but with a larger gain error. To have a balance in the trade-off between the gain range and gain error, W/L = 200 is selected in our design.

$$g_m = \left(\frac{\alpha K}{2} - \theta^2 i_D\right)\sqrt{\left(v_G - v_D - V_{TH} + \frac{\theta i_D}{\alpha K}\right)^2 + \frac{4i_D}{\alpha K}} - \left(\frac{\alpha K}{2} + \theta^2 i_D\right)(v_G - V_{TH} - v_D) - \frac{3\theta i_D}{2} - \frac{\theta^3 {i_D}^2}{\alpha K} \tag{19}$$

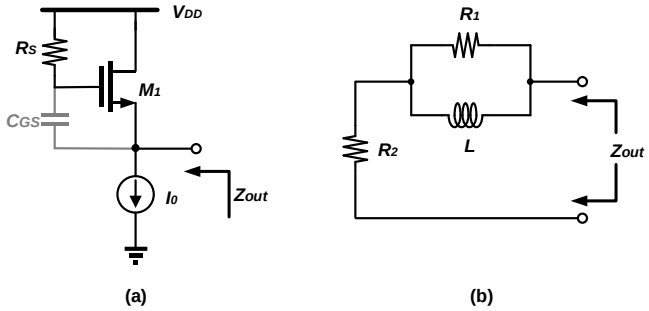


Fig. 9. (a) Inductive output provided by a source follower, and (b) equivalent network of (a).

2) Bandwidth Extension with Active Inductor

The upper cut-off frequency of the amplifier is usually limited by the parasitic capacitance associated with the output node. As previsouly mentioned, on-chip inductors can be added in series with the load resistor, thus resonating with the parasitic capacitance and extending the bandwidth. However, passive inductors occupy large die area. To solve this problem, active inductors are employed to fulfil both the die area limitation and bandwidth requirement.

Fig. 9(a) depicts a simple active inductor realized by the source follower, where the gate of transistor M_1 is connected to a series resistor R_s. Taking its gate-source parasitic capacitance into consideration, the output impedance seen from the source node can be written as [26]

$$Z_{out} = \frac{R_s C_{GS} s + 1}{g_m + C_{GS} s} \tag{20}$$

The output impedance is equivalent to a diode-connected transistor when $s = 0$, while $Z_{out} = R_s$ when s goes into infinity. If $R_s \gg 1/g_m$, an inductive behavior is expected from the circuit. The output impedance can be modeled as a lossy inductor in series with a resistor, as shown in Fig. 9(b), where

$$R_1 = R_s - \frac{1}{g_m} \tag{21}$$

$$R_2 = \frac{1}{g_m} \tag{22}$$

$$L = \frac{C_{GS}}{g_m}\left(R_s - \frac{1}{g_m}\right) \tag{23}$$

A major disadvantage of active inductor is the large voltage headroom it consumes, which restrains itself for low supply voltage applications. However, the input transistors in our design are biased in triode region instead of conventional saturation region. Therefore, such disadvantage becomes an advantage in our design. Moreover, to incorporate a flexibility of peaking magnitude, a MOS resistor is added in series with the passive resistor, arriving the final design in Fig. 5. By tuning the gate voltage M_N, the series gate resistance is changed, and thus the inductance provided by the active load.

The frequency response under different gain settings is shown in Fig. 10(a). With the help of active inductor, bandwidth is extended, and the peaking is controlled within 3 dB. The peaking is designed to appear at a relatively high frequency, in order to compensate the loss in other unit, which will be explained in detail later. From this figure, it is obvious that the peaking under different gain setting affects the frequency response in different ways. To study whether the peaking will affect the dB-linearity, simulations of gain characteristic at various frequencies are conducted. As depicted in Fig. 10(b), the chosen frequencies are 100 MHz, 2 GHz, 4 GHz, and 6 GHz, respectively. Although the magnitude of gain varies slightly, the overall dB-linearity maintains, presenting a ±0.5 dB error with V_{CTRL} varying from 0.94 to 1.2 V regardless frequency.

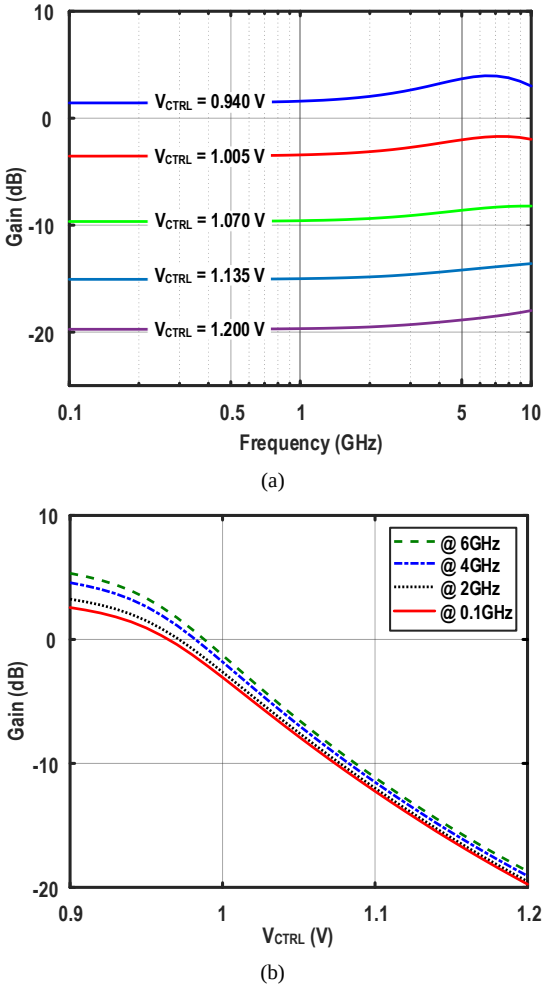
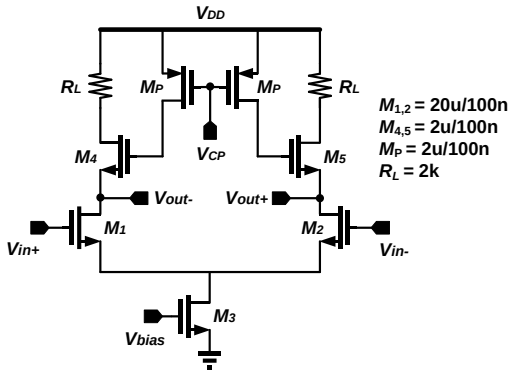


Fig. 10. (a) Frequency responses of variable gain unit under different gain settings, and (b) gain characteristic at different frequencies.

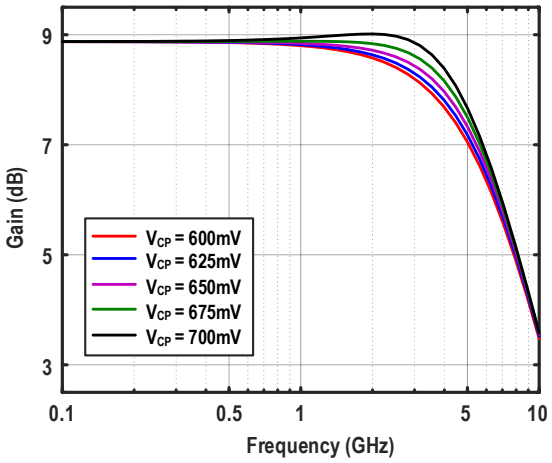
C. Fixed Gain Unit

As the variable gain unit possesses a broadband feature and exploits the triode-region operating transistors, the absolute gain of a single unit is low, where most part of its gain range is negative. Therefore, a fixed gain unit to boost the overall gain is required. A similar topology to the variable gain unit is used, except that the input differential pairs are biased in their saturation regions, as shown in Fig. 11(a).

The major function of this unit is to provide an adequate gain, such that the overall VGA can present a reasonable gain range. Therefore, passive resistor, R_L, is added in series with diode connected load, to increase the low frequency gain [16]. Active inductors are implemented again to alleviate the effect of parasitic capacitance, where PMOS transistor in triode region is



(a)



(b)

Fig. 11. (a) Schematic of fixed gain unit. (b) Frequency response of the fixed gain unit with adjustable peaking.

employed as the peaking resistor and the amount of peaking can be controlled by tuning the gate voltage of PMOS transistor.

Fig. 11(b) plots the simulation results of the fixed gain unit. The low frequency gain is nearly 9 dB, and bandwidth is extended with acceptable peaking. The active inductor is responsive to the control voltage of the series resistor, V_{CP}, such that the circuit is adjustable under PVT variations.

III. Overall VGA Architecture

To obtain a practical gain variation range, two variable gain units and two fixed gain units are needed to achieve a 42 dB gain variation from -20 dB to 22 dB. The overall configuration is given in Fig. 12, where one variable gain unit is connected to one fixed gain unit to form a single stage, followed by another identical stage. A wideband buffer is added for testing purpose.

A. Variable-Gain Amplifier Stage design

Considering a single stage, which includes one fixed gain unit and one variable gain unit, since the input DC voltage of variable gain unit is used to control the overall gain, the units must be ac coupled with capacitors, occupying large area but solving the DC offset problem in return. By comparing between the variable gain unit and fixed gain unit, the noise performance of fixed gain unit is better resulting from its higher gain, while variable gain unit offers a better linearity as it can adapt for different input power by tuning gain settings. Since the overall system noise depends on much more on the preceding stage,

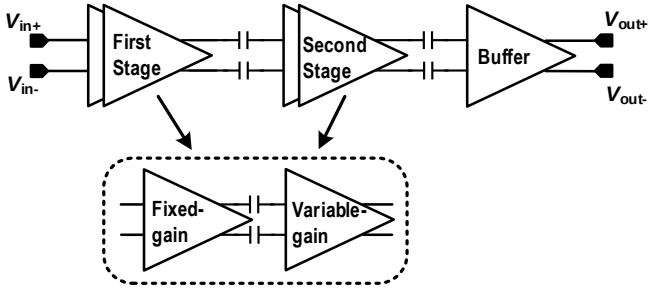
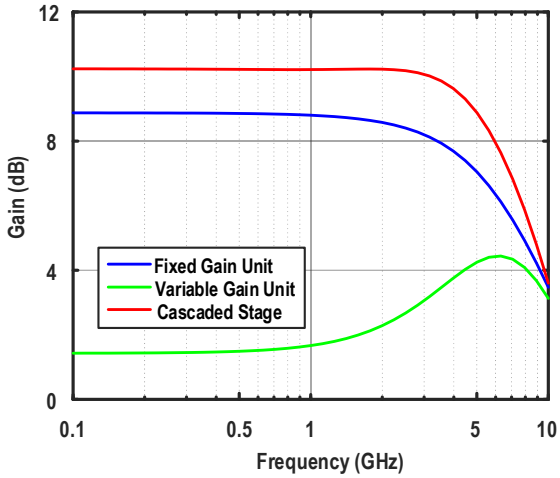
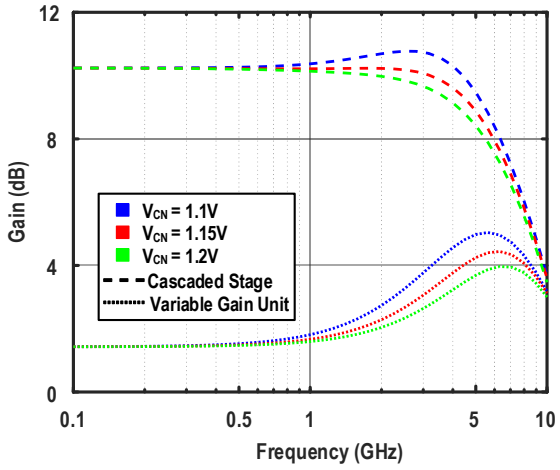


Fig. 12. Architecture of the overall VGA.



(a)



(b)

Fig. 13. (a) Frequency responses of one stage compared with separate units. (b) Adjustable peaking in one stage.

while its linearity relys on the last stage, fixed gain unit is placed in front of the variable gain unit to achieve a better NF as well as linearity.

Fig. 13(a) plots the frequency response of a single-stage VGA, in comparison with that of a fixed gain unit and variable gain unit. The high-frequency peaking in the variable gain unit compensates the early drop-off in the fixed gain unit. As a result, the overall frequency response is flat and extends beyond that of the fixed gain unit. In addition, the overall peaking can still be adjusted by either NMOS gate voltage in the variable gain

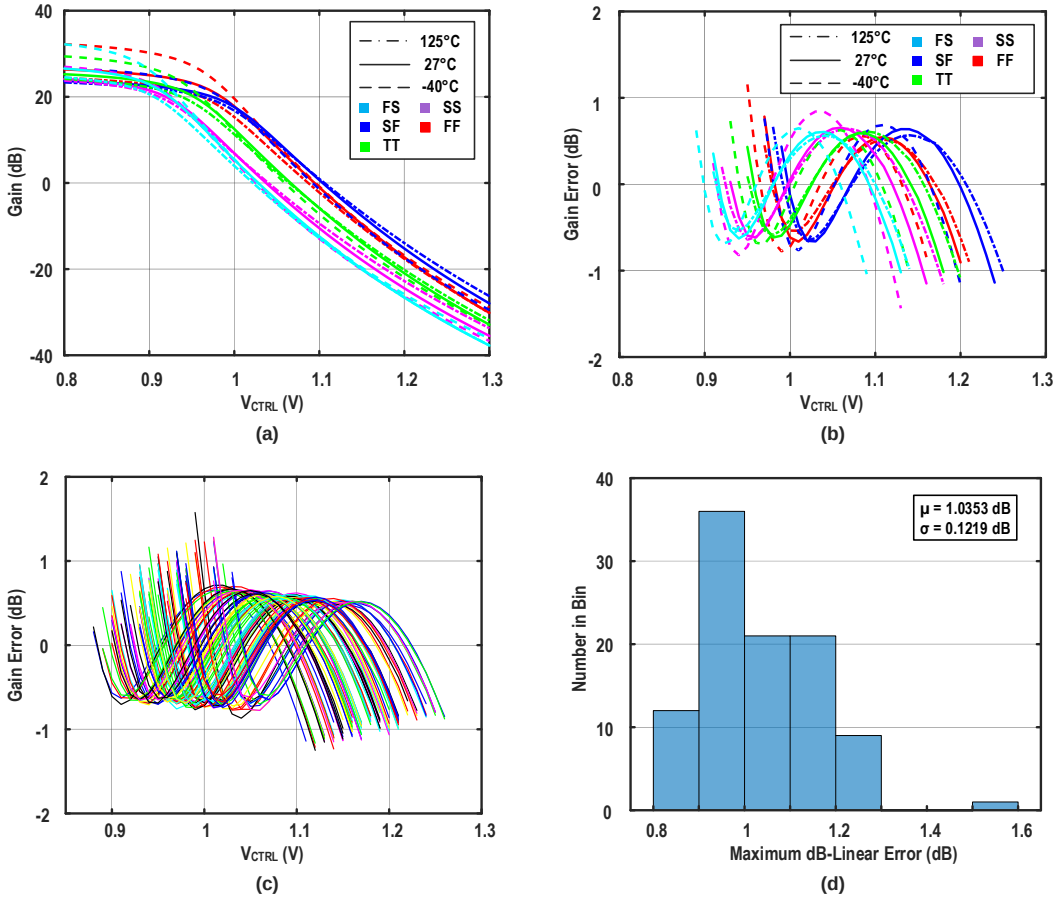


Fig. 14. (a). Gain characteristic under different corners and temperatures. (b) Gain error under different corners and temperatures. (c) Gain error curves from Monte Carlo simulations (100 runs). (d) Maximum dB-linear error histogram.

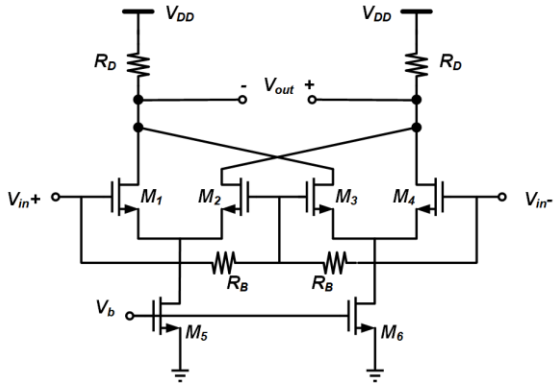


Fig. 15. f_T doubler output buffer.

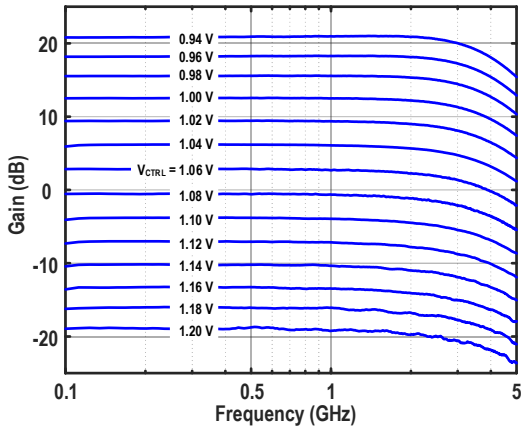
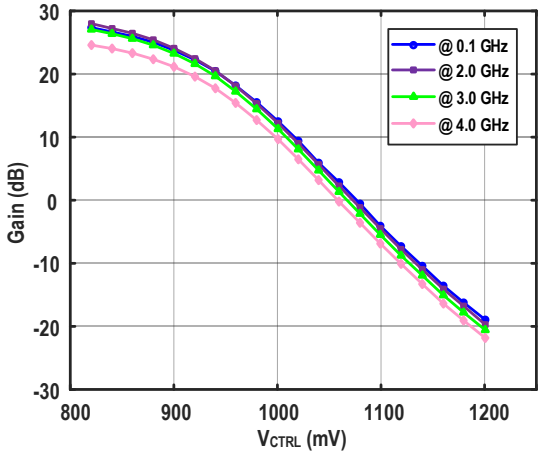


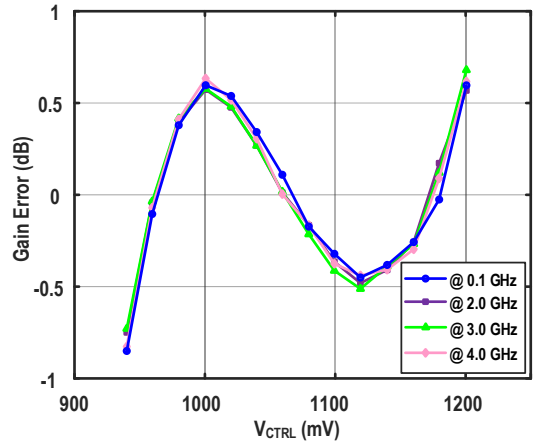
Fig. 16. Measured frequency response with various gain control voltage from 0.94 to 1.20 V.

unit (V_{CN}) or PMOS gate voltage in the fixed gain unit (V_{CP}). Taking the peaking control in the variable gain unit as an example, simulation results are plotted in Fig. 13(b). With V_{CN} decreased from 1.2 to 1.1 V, the overall peaking is increased from 0 to 0.5 dB, while the bandwidth is increased from 5.8 to 6.4 GHz.

Finally, after two identical stages are cascaded, the gain characteristic under different temperatures with various corners are simulated. With a proper PTAT current biasing circuit, the combination of corner and temperature variation only leads to a shift in the gain characteristic curve, as shown in Fig. 14(a). The dB-linear feature and the absolute gain range are well maintained, while the correspoding gain control range may shift upper or lower. By comparing a gain range of 40 dB, the gain error is given in Fig. 14(b), which shows that the dB-linear error is less than ±1 for most cases and the worst case scenario offers an acceptable maximum gain error less than 1.5 dB. The Monte-Carlo simulation is carried out to further verify the effects of process variation and mismatch. The result for 100 runs are shown in Fig. 14(c) and (d), which presents the dB-linear gain



(a)



(b)

Fig. 17. (a) Measured gain characteristic at different frequencies and (b) their corresponding gain errors for dB-linear control range.

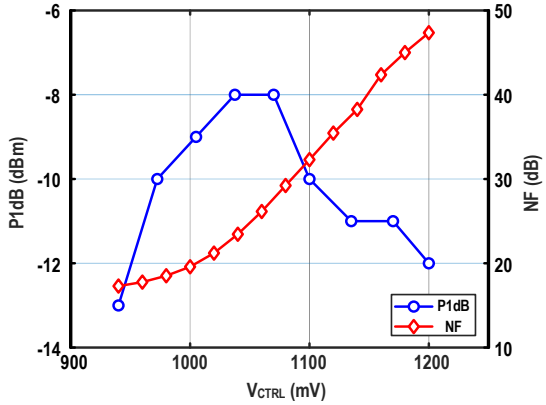
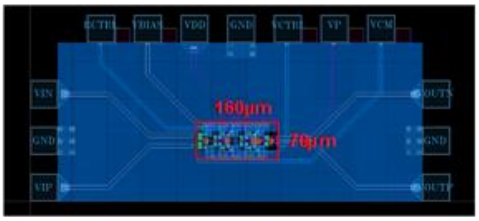
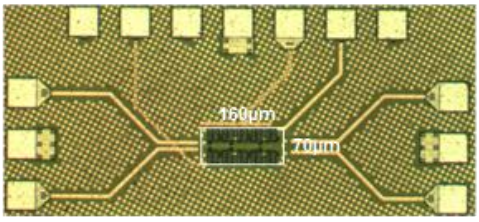


Fig. 18. Measured NF and P1dB versus gain control voltage.



(a)



(b)

Fig. 19. (a) Layout and (b) die photo of the fabricated VGA.

error curves and maximum dB-linear gain errors distribution, respectively. The mean value of the maximum gain error is found to be 1.0353 dB with a standard deviation of 0.1219 dB.

B. Output Buffer

Since the testing equipment for high frequency measurement usually adopts a standard input impedance of 50 Ω, an output buffer is required to perform output matching and avoid large capacitance loading. Generally, the output buffer is designed with no gain, such that the bandwidth is wide enough not to degrade the overall upper cut-off frequency. Meanwhile, the input capacitance of the buffer shall be small enough that it will not exceed the driving ability of the preceding stage.

The f_T doubler as shown in Fig. 15 provides the same voltage gain as simple differential stage. However, its input capacitance is roughly reduced to half. This is because the output of previous stage sees a parallel of two identical transistors, M_1 and M_2 for example, leading to a resultant capacitance equal to half of the gate-source capacitance. Therefore, this topology is widely used as an output butter, which is also adopted in our design.

IV. Measurement Results

The circuit was fabricated with Global Foundries 65 nm CMOS process and had been measured on the probe station. Frequency response under different gain settings are measured by the Keysight Network Analyzer (N5247A) and given in Fig. 16. Over a control voltage from 0.94 to 1.20 V, the VGA achieves a dB-linear gain variation range of 40 dB from -19 to 21 dB, and a upper cut-off frequency of 4 GHz.

The measured gain characteristic of the amplifier at various frequencies and its corresponding gain errors are plotted in Fig. 17(a) and (b), respectively. The amplifier can provide a maximum voltage gain of 28 dB if the control voltage is lowered to below 0.94 V, where the input transistors work in the saturation region. The dB-linear characteristic at different frequencies are well behaved, and the gain error is calculated to be less than 1 dB.

Fig. 18 depicts the noise figure and input P_{1dB} of the designed VGA under various gain settings. The noise figure increases from 17 to 47 dB with decreasing gain, while input P_{1dB} increases first and decreases for the second half control range. This is because P_{1dB} corresponds to the power where the signal amplitude saturates at either the input or output node. Under the highest gain setting, the swing at output is much larger than the

TABLE I
PERFORMANCE COMPARISON WITH OTHER STATE-OF-THE-ART DESIGNS

	TMTT'13 [15]	TCASI'12 [16]	TMTT'16 [23]	***This work***
Control method	Digital	Analog	Analog	**Analog**
dB-linear	Yes	No	Yes	**Yes**
Gain range (dB)	18 (-10 ~ 8)	60 (-10 ~ 50)	22 (2 ~ 24)	**40 (-19 ~ 21)**
Gain error (dB)	-	-	±0. 3	**±1**
BW (GHz)	1.9	2.2	2.2	**4**
IP_{1dB} (dBm)	-12.5	-13 to -55	-2 to -22	**-8 to -13**
Noise	NF = 20 to 27 dB	NF = 17 to 30 dB	NF = 24 to 29 dB	**NF = 17 to 47 dB**
Power (mW)	12.2	2.5	3.48	**3.5**
Size (mm^2)	0.048	0.014	0.01	**0.012**
Technology	0.18 μm BiCMOS	90 nm CMOS	65 nm CMOS	**65 nm CMOS**
FOM	58.4	-	1390.8	**3809.5**

input swing. Consequently, the maximum allowable swing at output will be attained first, limiting the P_{1dB}. As the overall gain decreases, the amplifier reduces its amplifying effect on the input signal. Thus, to produce the same output swing, larger input signal is needed, which leads to an increasing P_{1dB}. However, when the input power reaches a certain level, the input node will be saturated before the output node. Lastly, the layout and the die photo are given in Fig. 19(a) and (b), respectively, showing an active area of only 0.012 mm^2.

Table I presents the comparison between this work and other state-of-the-art works in multi-GHz range. Compared to other wideband VGAs published in recent years, the bandwidth of the proposed design is further extended. The chip area is not increased as contrasted to other wideband designs. This is owing to the incorporation of active inductors and frequency compensation. Although the gain error is not as good as [23], a much larger gain variation range is achieved. Last but not least, the power consumption of the designed VGA is small, which results from the simple method to generate the exponential characteristic. Based on [16], a modified figure of merit (FOM) which takes dB-linearity feature of VGA into consideration is given by

$$FOM = \frac{BW\ (GHz) * dB\text{-}Linear\ Gain\ Range\ (dB)}{Power\ (mW) * Active\ Area (mm^2)}$$

As listed in the last row of Table I, the designed VGA outperforms other state-of-the-art works.

V. CONCLUSIONS

The design of a wideband VGA with an accurate dB-linear characteristic is presented in this paper. An inductor-less-based approach is used to broaden the bandwidth of the amplifier up to 4 GHz, and non-saturated transistors are adopted to extend the variable gain range over 40 dB, while compensating dB-linear gain error and simplifying the design. In order to prove the concept, the designed VGA is fabricated in a standard 65 nm CMOS technology and measured using on-wafer probing. There is a good agreement between the simulated and measured results. Therefore, it can be concluded that the presented approach is simple and effective for VGA designs targeted for high-speed analogue signal processing.

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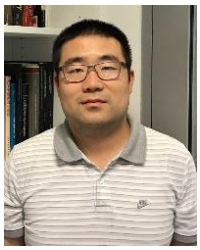

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