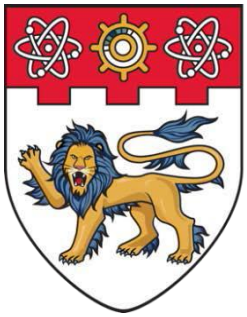

NANYANG TECHNOLOGICAL UNIVERSITY
SINGAPORE

WIDEBAND DB-LINEAR VGA FOR HIGH-SPEED COMMUNICATIONS

KONG LINGSHAN

SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

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WIDEBAND DB-LINEAR VGA FOR HIGH-SPEED COMMUNICATIONS

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School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

2019

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

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Boon Chirn Chye

Authorship Attribution Statement

This thesis contains material from 1 paper published in the following peer-reviewed journal / from papers accepted at conferences in which I am listed as an author.

Chapter 4 is published as L. Kong, Y. Chen, C. C. Boon, P.-I. Mak, and R. P. Martins, “A wideband inductorless dB-linear automatic-gain control amplifier using a single-branch negative exponential generator for wireline applications,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 10, pp. 3196-3206, Oct. 2018.

The contributions of the co-authors are as follows:

- Prof Boon provided the initial project direction and edited the manuscript drafts.
- I prepared the manuscript drafts. The manuscript was revised by Prof Mak and Prof Martins.
- Prof Chen assisted on analyzing the data and organized the flow of the manuscript.
- The schematic and layout design of the circuit was accomplished by me.
- I conducted the measurement of the fabricated circuit, including both frequency domain and time domain testing.

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SUMMARY

In the transceivers of both wireless communication and wireline communication, automatic gain control (AGC) system is widely used to provide a constant output power independent of the input signal strength. The variable gain amplifier (VGA), as the core block of AGC, is not only required to provide a wide gain variation range but also desirable for a dB-linear gain characteristic. Due to the absence of the intrinsic exponential relationship in standard CMOS technology, it is difficult to realize an accurate dB-linear characteristic with low power consumption and small die area. In addition, if a broad bandwidth is demanded for high-speed communications, the design becomes more challenging.

In this thesis, novel ideas are proposed to extend the gain range effectively with minimum hardware. Based on a thorough review of the state-of-the-art architecture, the approach that simultaneously tunes the transconductance and output resistance of the amplifier is brought forward. If both of the parameters can be tuned in the same direction, either increasing or decreasing with the control while preserving an exponential feature in each, the total gain range would be the summation of the changes, leading to an extended gain tuning range as well as savings in the power budget. With this idea, a wideband VGA designed for 60 GHz wireless communication is constructed. Fabricated with 65 nm CMOS process, the VGA achieves an upper cut-off frequency around 4 GHz while consuming a power as low as 3.5mW.

However, such architecture of the proposed VGA imposes a constraint on use of broadband techniques, leading to an inadequate bandwidth for modern

wireline communication. Therefore, another method to improve the exponential approximation range is presented, which exploits the convex and concave functions together as an inverse S-shaped curve. The negative exponential generator (NEG) makes full use of the dynamic operating regions of the transistors, such that wide tuning range is achieved with minimum hardware. An inductorless 10 Gb/s AGC amplifier for wireline communication is then designed with the proposed NEG to provide a gain variation range of 58 dB, while adopting several broadband techniques to extend the bandwidth beyond 7 GHz. Again, fabricated with 65 nm standard CMOS process, the AGC demonstrates a competitive performance compared with the state-of-the-art works, where high dynamic range, wide bandwidth as well as low power consumption are achieved.

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CHAPTER 1

INTRODUCTION

1.1 Background and Motivation

The rapid growth of data volume has promoted the evolution of multi-gigabit data transmission in recent years through both wireless [1], [2] and wireline [3] communications. Since the loss of transmission channel is usually undetermined and transceiver always has a limited dynamic range, amplifier whose gain is tunable receives considerable attention so as to assist other fundamental blocks to fulfill the transmitting or receiving task. Such amplifiers can be divided into two categories, namely programmable gain amplifier (PGA) and variable gain amplifier (VGA). While PGAs are controlled by digital signals step-by-step [4]-[7], VGAs are tuned continuously by an analog control signal [8]-[20]. As a result, VGAs are the preferred choice in automatic gain control (AGC) system, because by simply adding an auxiliary feedback loop, the VGA can be controlled adaptively, and the system manages to provide an output signal of fixed amplitude regardless the input signal strength [21]-[36].

Due to the nonlinear model of AGC system, VGAs with dB-linear gain characteristic are highly desirable in order to achieve a constant settling time under various conditions [37]-[42]. Although technologies involving bipolar

junction transistor (BJT) or heterojunction bipolar transistor (HBT) can realize such feature with their intrinsic current-voltage relationship, standard CMOS technology is more attractive in concern of cost and integrability. Lack of the intrinsically available exponential feature in MOSFET, tremendous works have been done to approximate the exponential function with its linear and square-law characteristic. If low-complexity circuitry is utilized, only finite approximation range and low dB-linear accuracy can be achieved. To improve the gain variation range, additional circuits need to be added in or new approximation functions must be sought for.

Meanwhile, the bandwidth of VGAs and thus AGC is another concern. During the last decade, mobile communication has moved upwards to radio-frequency and millimeter-wave bands, in order to avoid congestion of the radio spectrum as well as to boost the bit rate with a much wider channel bandwidth. At the same time, wireline communication, such as optical transceivers, backplane serial links, etc. also experiences increasingly rapid growth of data rate up to several tens of gigabits. Therefore, for either wireless communication or wireline links, broadband feature is highly demanded.

1.2 Major Contributions of the Thesis

This thesis reviews and summarizes the state-of-the-art works on VGAs and AGCs for both wireless and wireline communications. The architecture of VGAs and their exponential characteristic realization methods are compared and categorized from new perspectives. With a thorough understanding of the existing works, novel approaches to realize the exponential function in CMOS

technology are proposed.

The first approach is to simultaneously tune the transconductance and output resistance of an amplifier, such that a wide gain variation range is attained with low power consumption. Based on this idea, a wideband VGA whose bandwidth is around 4 GHz is designed for wireless communication.

Furthermore, a standalone exponential generator is proposed, which makes use of the dynamic transition between operating regions of MOSFET. Mathematically, a convex function is combined with a concave function as an inverse S-shaped curve to piecewise approximate the exponential function. By employing the proposed exponential generator, a 10 Gb/s AGC system for wireline communication is designed. Fabricated in 65 nm standard CMOS technology, it achieves low power consumption, small active area, and wide gain variation range compared to other works published in recent years.

1.3 Organization of the Thesis

In this thesis, automatic gain control circuitry and its core block, variable gain amplifier are introduced. The importance of designing broadband VGAs with wide tuning range is thus revealed.

In Chapter 2, the architecture of AGC system is firstly reviewed, thereby explaining why dB-linear VGAs are desirable. Then the architecture of the-state-of-the-art works are reviewed and categorized, where tuning method and control method are taken as the major considerations to classify them. Lastly, the evolution of exponential generation in CMOS technology is discussed and approximation functions are compared.

In Chapter 3, the design of wideband VGA for wireless communication is presented in detail. Beginning with an introduction of VGA in wireless transceivers and design considerations, the actual implementations of each block are revealed. The proposed exponential generation method is presented, with both mathematical verifications and circuit implementations. The idea to exploit both transconductance and output resistance is illustrated and realized with the transistors operating in triode region. Then the proposed approach is applied to the variable gain cell, achieving a gain range of more than 20 dB. Broadband techniques, such as active inductor, are implemented in both the variable gain cell and fixed gain cell, such that a wide bandwidth is obtained. In the end, the measurement result is given, indicating that the designed VGA is suitable for high-speed wireless communication, such as IEEE 802.15.3c and IEEE 802.11ad.

In Chapter 4, the design of AGC system for wireline communication is demonstrated. The receiver architecture and its signal format are briefly introduced, followed by a comparison between AGC and limiting amplifier. Then the advantage of AGC is clarified, while the design considerations are pointed out. After that, the circuit design of AGC is depicted block by block. To begin with, a new exponential approximation function is introduced in order to design a VGA with standalone exponential generator. Instead of shifting the same functions over different control ranges, one convex and one concave function are combined as an inverse S-shaped curve, such that the variation range is extended with minimum number of devices, and flexibility of choosing different tuning range or accuracy is provided. By making use of the proposed exponential generation method, the designed VGA achieves a dB-linear gain tuning range as

high as 40 dB. Other building blocks, including the post amplifiers, DC offset cancellation circuit, and feedback control loop are elaborated. At last, measurement results of both open-loop VGA and closed-loop AGC are presented, showing a performance that complies with the requirement of 10 Gb/s wireline communication, such as 10 Gigabits Ethernet.

Finally, Chapter 5 concludes the thesis by summarizing the entire studies, and future works are suggested.

CHAPTER 2

LITERATURE REVIEW

2.1 AGC Architecture

In this section, we will review the architecture of AGC and arrive at the conclusion that if the VGA has a dB-linear gain characteristic, the time for adjusting the gain of VGA in response to an input amplitude change will remain constant.

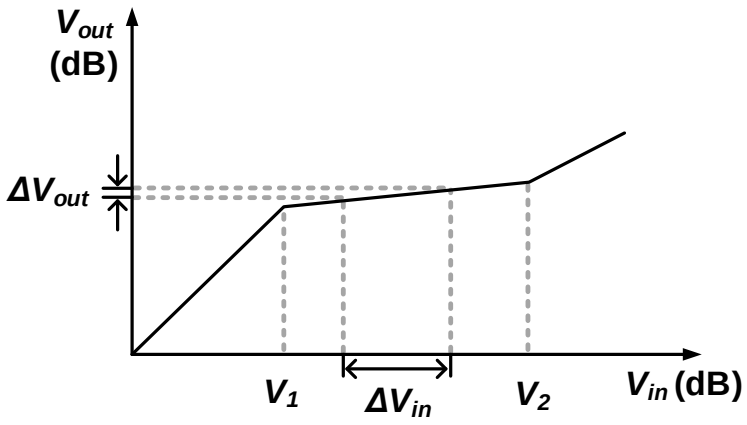


Figure 2. 1 AGC characteristic

Figure 2. 1 illustrates the input-output characteristic of an AGC system in logarithmic scale of the axes. When the input level is below its sensitivity voltage, V_1, the AGC works like a fix gain amplifier, where any change in V_{in} results an identical change in V_{out}. As the input level increased to the range $V_1 \leq V_{in} \leq V_2$,

the AGC system attempts to maintain a constant V_{out}, fulfilling the goal of an AGC. In practice, it is unlikely to keep the output level ideally constant. A small output difference ΔV_{out} is observed when a large input difference ΔV_{in} is given. The 'compression ratio', or the 'flatness factor' can be defined as in [37]

$$M = \frac{change\ in\ input\ level\ in\ dB\ scale}{change\ in\ output\ level\ in\ dB\ scale}$$

If V_{in} is continually increased beyond V_2, the normal operation of AGC ceases and the output level may increase with a compressed factor, due to current or voltage limit of one or more stages. The lower and upper limits, i.e. V_1 and V_2, define the dynamic range of the AGC system and are determined by both the feedforward gain amplifier and the feedback loop.

As the fundamental building block of an AGC system, VGA's gain characteristic determines the variations in settling time for different incoming signal amplitudes. A constant settling time is usually desired, since it leads to the maximum loop bandwidth for fast signal acquisition and maintains the AGC stability over different operating conditions. While most of the research works on the behavior of AGC assume an exponential characteristic of the VGA as prerequisite [37]-[41], [42] employs a modeling method similar to log-domain filters and demonstrates many interesting results for different types of VGAs and loop filters. A simplified model used for AGC loop analysis is shown in

Figure 2. 2, where the gain characteristic of the VGA is defined by a monotonic function $G(V_C)$ and a fix gain of A_v is lumped up to present any post amplifying stage. The feedback loop consists of a peak detector, whose output is proportional to the amplitude of V_{out} with a linear coefficient of k_P, and a loop

filter with a transfer function $H(s) = G_m/sC$ since it is usually realized by an integrator. Then, the gain control voltage is derived as

$$V_C(t) = \int_0^t \frac{G_m}{C}\left(V_{ref} - k_P V_{out}\right)d\tau \tag{2.1}$$

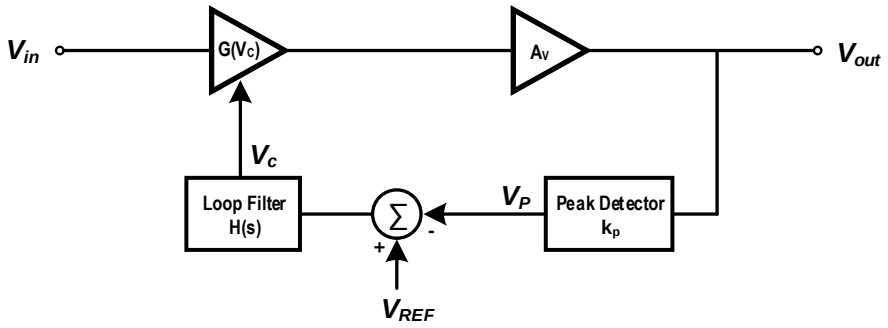


Figure 2. 2 Model of AGC system

The output amplitude in logarithm scale can be written as

$$V_{out,dB} = 20\log[G(V_C)] + V_{in,dB} \tag{2.2}$$

Take derivatives of both sides, obtaining

$$\frac{dV_{out,dB}}{dt} = \frac{20}{ln10}\frac{1}{G(V_C)}\frac{dG(V_C)}{dV_C}\left[\frac{G_m}{C}\left(V_{ref} - k_P V_{out}\right)\right] + \frac{dV_{in,dB}}{dt} \tag{2.3}$$

which describes a nonlinear system response unless certain constraints are placed. One practical constraint is to force the coefficient in the first term of (2.3) to be a constant. Since G_m and C are fixed values in a conventional design, it requires

$$\frac{1}{G(V_C)}\frac{dG(V_C)}{dV_C} = k_1 \tag{2.4}$$

where k_1 is a constant. Therefore, the gain characteristic of the VGA must obey the exponential function, i.e.

$$G(V_C) = k_2 e^{k_1 V_c} \tag{2.5}$$

where k_2 is another constant. As a result, the AGC becomes a high-pass first-order linear system [42] with a time constant of

$$\tau = \frac{C}{k_1 G_m V_{ref}} \tag{2.6}$$

2.2 State-of-the-Art VGAs

2.2.1 G_m-tuning and R_{load}-tuning VGAs

A typical amplifier can be treated as a transconductance amplifier with a load resistor, providing a gain equal to the multiplication of the both. Therefore, if variable gain is required, either the transconductance or the load resistance shall be tuned, as shown in Figure 2. 3, such that the overall gain is adjustable. While some VGAs achieve a wide range by tuning its load resistance, more designs realize the feature by varying the effective transconductance, and even both of the parameters. We will review and categorize the state-of-the-art works in the following discussion.

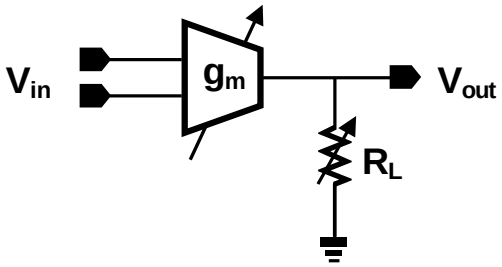


Figure 2. 3 Tuning method of variable gain amplifier

2.2.1.1 G_m-tuning VGAs

Although the simplest way to change the transconductance is to tune the current source directly [43], [44], this method changes the DC operating point as

well. As a result, the output common code will be varying under different gain settings. Besides adjusting the tail current, source degeneration [Figure 2. 4(a)] is a popular topology widely used in VGA designs [19]-[21]. By replacing the passive degenerative resistor with a MOS resistor, the degeneration factor changes almost linearly with the control voltage applied to its gate. The voltage gain of a single stage can be expressed as

$$A_v = \frac{g_{m1,2}R_o}{1+\frac{1}{2}g_{m1,2}R_s} \tag{2.7}$$

where $g_{m1,2}$, R_o and R_s represent the transconductance of the input transistors M_1 and M_2, output resistance of M_6 and M_7, and source degenerative resistance of M_3, respectively, and

$$R_s = \frac{1}{\mu C_{ox}\left(\frac{W}{L}\right)_3 (V_{ctrl} - V_{s,3} - V_{th,3})} \tag{2.8}$$

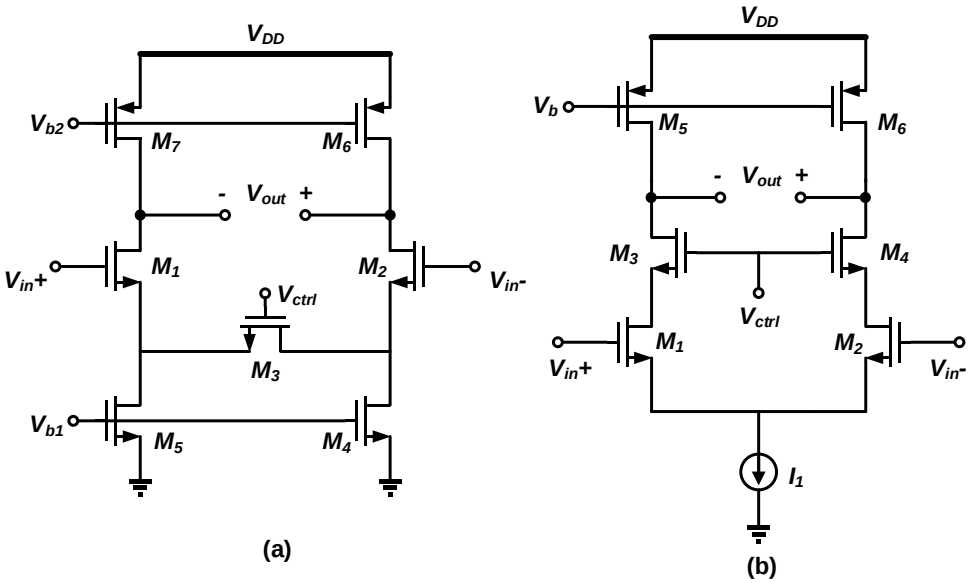


Figure 2. 4 Gm-tuning topologies with single-ended control: (a) source degeneration amplifier [19] and (b) cascode amplifier [16]

Therefore, V_{ctrl} determines the resistance of the source degenerative factor and thus the effective transconductance of the amplifier. Meanwhile, cascode topology as shown in Figure 2. 4(b) is adopted in [16] and [17], for the same purpose to vary the transconductance of the amplifier stage. The input differential pair, M_1 and M_2, operates either in the triode or saturation region based on the external control voltage, V_{ctrl}. When V_{ctrl} is low, the two transistors are forced to work in the triode region and a low gain is obtained. On the contrary, when V_{ctrl} is high enough, the input transistors switch to the saturation region and provide a high gain. In other words, by adjusting the control voltage, the effective transconductance of the amplifier changes.

Apart from the single control topologies mentioned above, differential control voltage can be incorporated with Gilbert cell to alter the effective transconductance [23]-[34], [45]. One possible implementation is to apply the control voltage to the bottom pair (M_5 and M_6) and the input signal to the top pairs (M_1 to M_4), as shown in Figure 2. 5(a). The resultant gain is the difference between the two voltage-controlled amplifiers, given by

$$A_v = \left(g_{m1,2} - g_{m3,4}\right)R_{L1} \tag{2.9}$$

where $g_{m1,2}$ and $g_{m3,4}$ are corelated to V_{ctrl}. Interestingly, the order can be exchanged while still obtaining the same result [46]. As illustrated in Figure 2. 5(b), the input voltage is converted to current by means of M_5 and M_6, which is then routed through M_1-M_4 to the output nodes. Degeneration resistor can be added to the input differential pair in order to obtain a linear voltage-to-current conversion [23]-[26]. The advantage of (a) is that this arrangement is also suitable for folded-Gilbert cell [27]-[33], [45], thereby alleviating the challenge of low

power supply in advanced process technology.

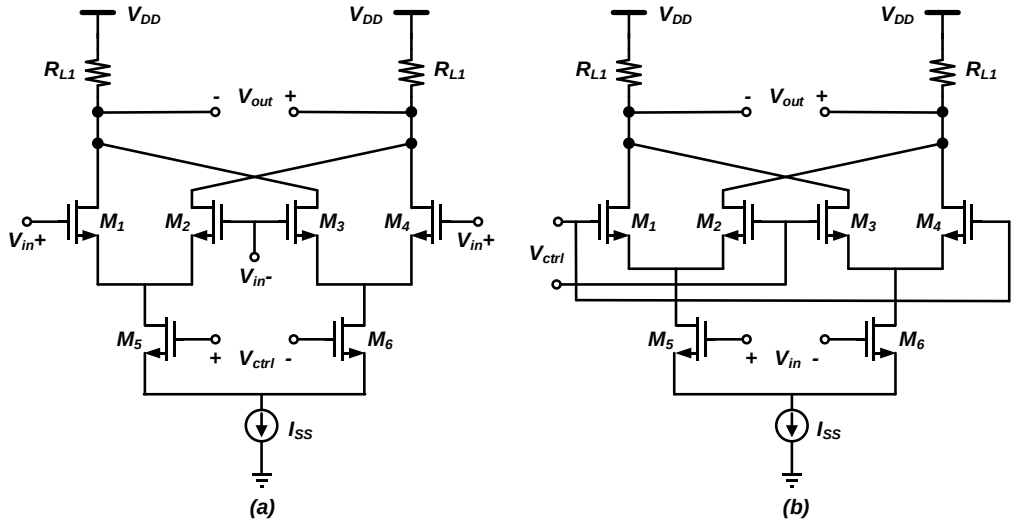


Figure 2. 5 G_m-tuning topologies with differential control: Gilbert cell with (a) lower transistor pair as control [25] and (b) upper transistor pairs as control [33]

2.2.1.2 R_{load}-tuning VGAs

Tuning the resultant output resistance of the amplifier provides another approach to design VGAs. The straightforward way to utilize MOS resistor as load is feasible [22], [47], but the tuning range is limited and bandwidth under different gain settings varies significantly. To accommodate high-speed transceiver design, Cherry-Hooper (CH) amplifier is employed in [18] to extend the gain variation range while achieving a broadband feature. A classic CH amplifier incorporates local feedback in the drain network to improve the speed. As depicted in Figure 2. 6, R_F establishes a feedback around M_2 by sensing the output voltage and returning a proportional current to X [48]. Neglect all second-order nonidealities, the voltage gain is given by

$$\frac{V_{out}}{V_{in}} = g_{m1}R_F - \frac{g_{m1}}{g_{m2}} \tag{2.10}$$

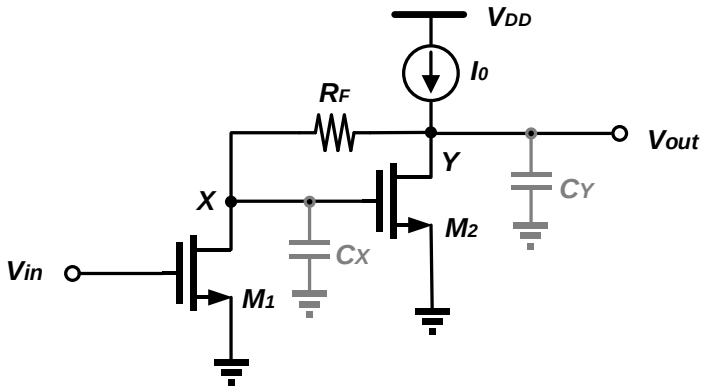


Figure 2. 6 Classic Cherry-Hooper amplifier [48]

If $R_F \gg 1/g_{m2}$, the resultant gain approximates to $g_{m1}R_F$, which is equivalent to a common-source amplifier with a load resistance R_F, while the resistance at both node X and Y are low, yielding only high-frequency poles. The major issue of Cherry-Hooper amplifiers is the large voltage headroom it requires, making it difficult to apply in low-voltage application. [18] makes use of the modified structure and employs MOS resistors to realize the variable gain, arriving at a modification as shown in Figure 2. 7. The resistive shunt-feedback is replaced with a pair of PMOS transistors (M_5 and M_6) working in the triode region. In addition, another pair of PMOS transistors (M_7 and M_8) is paralleled with the load R_d to further extend the gain tuning range. In such a way, the gain variation range is increased, and the bandwidth of the amplifier does not vary much when the control voltage changes. However, the gain control signal is applied to the feedback resistor, which results in a linear relationship between input and output. Hence, innovative method to employ exponential characteristic into Cherry-Hooper topology is desired.

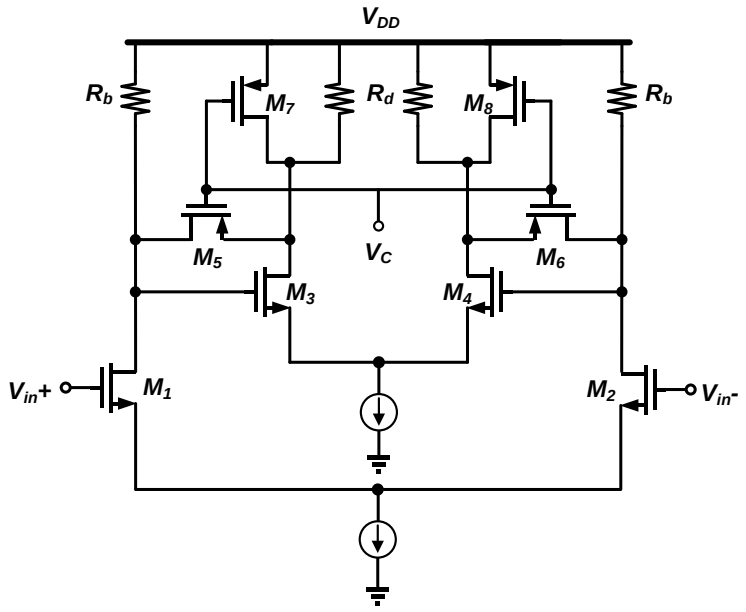


Figure 2. 7 R_{load}-tuning VGAs based on Cherry-Hooper amplifier [18]

[49] and [50] also focus on the load of the amplifier, making it tunable by controlling the body and gate, as shown in Figure 2. 8(a) and (b), respectively. In either of the design, its load consists of a diode-connected transistor and a paralleled tuning transistor, between which the current is steered. Because the variable gain that a single cell can provide is limited, little difference is observed on its bandwidth. However, multiple cells must be cascaded to attain an adequate gain range, which in return degraded its bandwidth significantly.

Last but not least, it is possible to tune the transconductance and the output resistance simultaneously. The architecture shown in Figure 2. 9 is widely used in plenty of VGA works [10]-[14]. With a tunable current tail controlling the transconductance of the differential pair, the load adopts a pair of diode-connected NMOS. Therefore, the overall gain of the amplifier is $A_v = g_{m1,2}/g_{m3,4}$. If $g_{m1,2}$ and $g_{m3,4}$ vary in different directions, which is to say one

of them is increased while the other is decreased, a wide gain variation range could be expected.

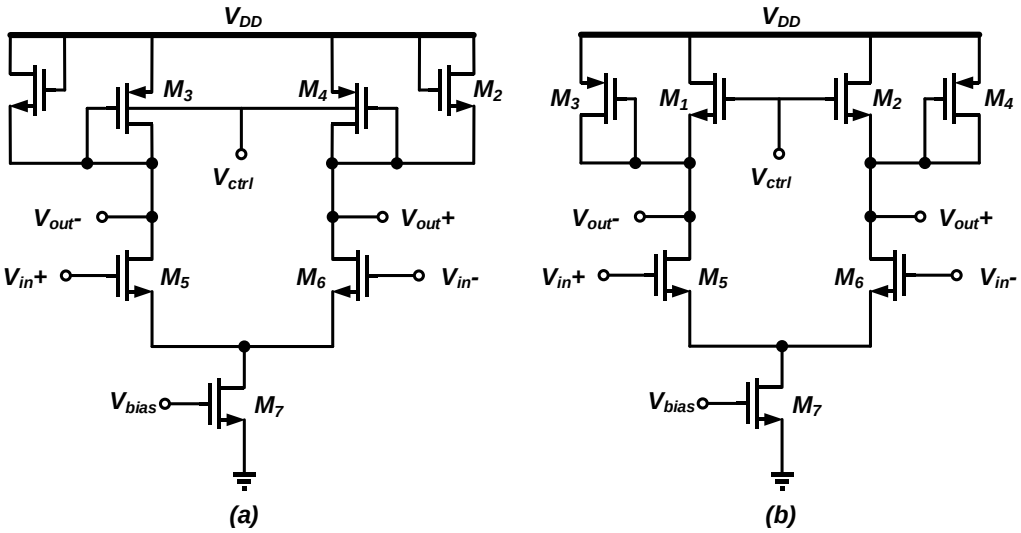


Figure 2. 8 R_{load}-tuning VGAs with (a) body-tuned [49] and (b) gate-tuned [50]

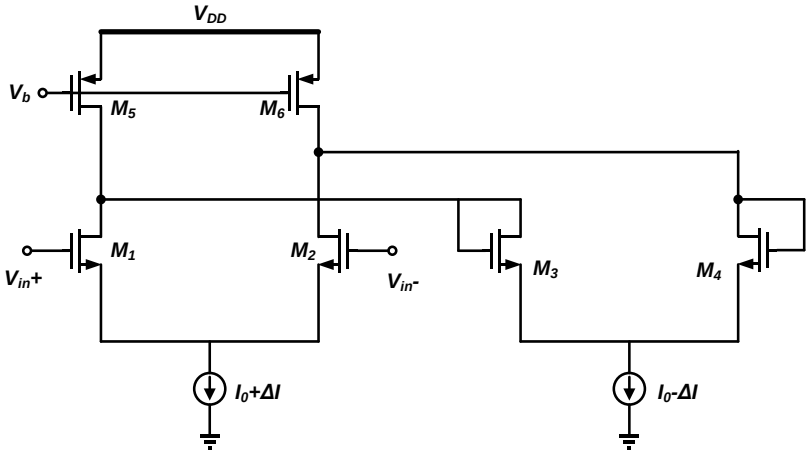


Figure 2. 9 G_m and R_{load} dual-tuning amplifier architecture [10]

2.2.2 Standalone Gain Control Block and Integrated VGAs

The desirable feature of dB-linear characteristic also affects the architecture of VGAs. Generally, the state-of-the-art VGAs can be categorized into two groups, one of which requires a standalone exponential generator to convert the

linear control voltage to an exponential output, while the other possesses the exponential feature with the amplifier itself.

Due to lack of intrinsic exponential relationship in CMOS technology, the architecture of g_m-tuning amplifiers discussed above are mostly incorporated with external exponential generator. The generator either employs an intrinsic exponential device, such as parasitic BJT [17], [32], [51] or subthreshold MOS [44], or makes use of approximation functions, such as Taylor series [19], rational approximation [33], etc. After obtaining the pre-distorted exponential control voltage, the amplifiers whose gain vary linearly with the control voltage would be able to provide a dB-linear gain characteristic. Regardless of those nonidealities, such as mismatch and process variation, Gilbert cell preserves a superior linear-relationship between the control voltage and total gain, thereby able to maintain the exponential feature created by the external block. In contrast, the voltage gain of source degeneration topology can be treated as linear only when $g_{m1,2}R_s \gg 1$, which means large input transistors and degenerative resistor must be employed, leading to a limited bandwidth and voltage gain. However, if the VGA is designed for narrow-bandwidth applications, this circuitry manages to provide higher linearity and consumes less power compared to Gilbert cell.

The advantage of standalone exponential generator is that the separate control block is isolated from the signal path. Consequently, the performance of amplifier, including frequency response, linearity, power consumption, etc. can be optimized independently. Moreover, according to different requirements for each application, different exponential generators with different accuracy and gain range can be selected, which gives the designers a lot of flexibility. The

integrated dB-linear VGAs, on the other hand, usually have simple structures, thereby reducing the size and complexity of the designs. However, the architecture is more fixed with its corresponding exponential algorithms.

The body-tuned and gate-tuned VGAs mentioned in Section 2.2.1.2, for instance, demand a careful selection on the size of paralleled PMOS and NMOS load, presenting a severe trade-off between the exponential accuracy and variation range. Even with the optimized sizing, cascading multiple cells is inevitable since very limited gain range can be provided by one cell. [16] and [36] take advantages of the transistors operating in triode region, tuning their transconductance and output resistance respectively, so as to achieve a pseudo-exponential gain characteristic while amplifying the signal simultaneously. Last but not least, an interesting approach proposed in [20] also saves the trouble to design a standalone exponential generator, by proving that cascading numbers of linear amplifiers could approximate the exponential function successfully. Nevertheless, without gain error compensation, an adequate gain range is hard to accomplished even with tens of stages.

2.3 Evolution of Exponential Realization

With the absence of exponential characteristic in CMOS technology, it is challenging to design the VGAs to meet the gain variation range, gain-control accuracy, bandwidth and linearity requirements. Although one can obtain the linear-in-decibel relationship with parasitic BJTs or subthreshold biasing condition, the application is limited due to its low-speed and large-noise contribution. In this session, we discuss and compare several approximation

approaches to generate the exponential function widely used for CMOS.

Pseudo-exponential function can be expressed as

$$e^x = \frac{1+\frac{1}{2}x}{1-\frac{1}{2}x} \tag{2.11}$$

which provides an accurate approximation of less than 5.5% error with $-0.85 \leq x \leq 0.83$. A simple implementation is to control the transconductance of the input differential pair and diode-connected load by simultaneously tuning their current tails [10], [12], as shown in Figure 2. 9. However, the gain variation range is limited per stage due to the square root relationship between transconductance and drain current, such that multiple stages need to be cascaded in order to achieve a wide gain tuning range. Moreover, both bandwidth and linearity will be affected when the gain is adjusted, making it less favorable for constant bandwidth and high linearity applications. Another implementation is to employ high gain amplifier with closed-loop differential feedback resistors. A differential-ramp based architecture is proposed in [52], where the feedback resistance can be gradually changed by paralleling more and more resistors. Although wider tuning range is achieved, the bandwidth is limited by the closed-loop topology and the ramp generator requires a large number of control lines. The pseudo-exponential function can also be realized by cascading two stages, whose gain equal to the numerator and the inverse of denominator respectively [21]. However, using transistors in triode region still introduces nonlinearity for large input and output signals.

Another approximation method is given by the second-order Taylor series expansion,

$$e^x \approx 1 + x + \frac{1}{2}x^2 \tag{2.12}$$

The approximation error is less than 5.5% for $-0.6 \leq x \leq 0.85$. Its voltage-mode implementation, however, suffers from nonlinearity issues due to the mobility degradation and mismatch effect (especially for short-channel devices), while the constraint on the operating region also limits its approximation range [53]. On the other hand, the current-mode implementations [53], [54] usually require a number of current mirrors, multipliers or squarers, demanding tens of transistors. In practice, a voltage-to-current convertor is required to generate a linear current output with respect to the input control voltage, which is then injected to current square circuit to create the second-order term. The resultant current is then summed by a certain dc current and used to control the linear VGA blocks [19]. Because of the extra circuits involved to achieve an overall exponential current, large chip area and high power consumption are inevitable.

A new approximation function is proposed in [20] based on the limit definition of the exponential function.

$$e^x = \lim_{n\to\infty}\left(1 + \frac{x}{n}\right)^n \tag{2.13}$$

where n is the number of cascaded linear stages, and a larger n leading to a wider accurate region. Three identical stages are cascaded to verify the idea, each of which uses transistors in triode region as source degeneration resistor to realize linear gain control [Figure 2. 4(a)]. As a result, a gain variation range about 30 dB and a gain error within ±0.5dB are achieved without other approximation range extension technique. Nevertheless, bandwidth limitation resulting from its parasitic capacitance is server, while non-standard CMOS process exacerbates

the cost of implementation if gain error compensation is employed.

The three approximation functions discussed above are simulated and compared with the idea exponential function. Figure 2. 10(a) and (b) depict the variation range and approximation error of each function, respectively.

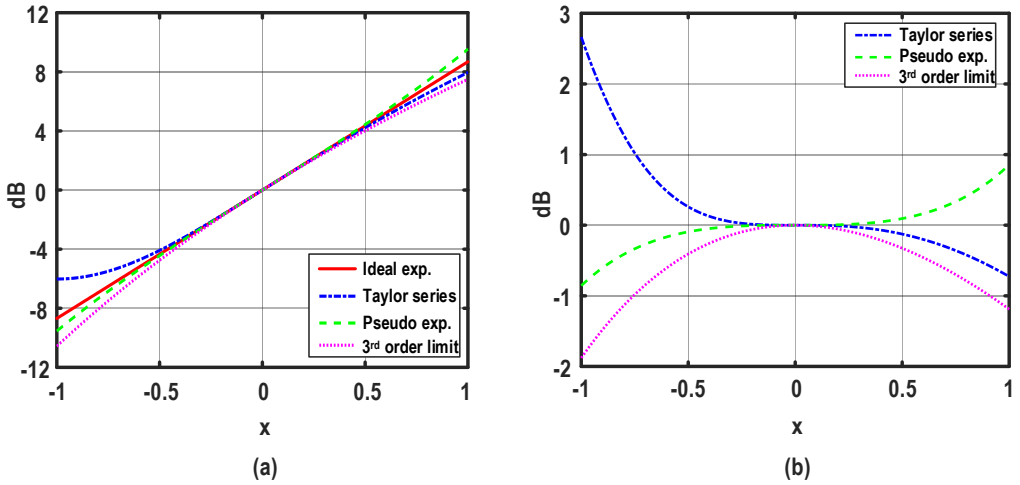


Figure 2. 10 (a) Comparison of the commonly used approximation functions and (b) gain errors of each approximation functions

Because of the limited accuracy for a single piece of approximation function, many improvement works are done to enlarge the validation range of the exponential approximation functions. One approach is to improve the accuracy of approximation functions by adding in higher-order terms. A modification of pseudo-exponential function is presented in [55] where second-order of rational approximation is utilized, given by

$$f(x) = \frac{x^2 + 6x + 12}{x^2 - 6x + 12} \tag{2.14}$$

The accurate approximation range is largely extended, where gain error is less than 5.5% for $-2 \leq x \leq 2$, but extra blocks such as current ratio generator are mandatory. The other approach is to shift and scale the same approximation

function over two adjacent regions, thereby fitting the same exponential curve with different x ranges. The piecewise approximation is realized with equation (2.11), (2.13) and (2.14) in [15], [20] and [33], respectively. For integrated topology adopted in [20], the shifting and scaling process is achieved by paralleling another source degenerative transistor with a different threshold voltage. Despite its simplicity, it imposes certain requirement for the process to ensure an accurate linear-in-dB gain control. A switching technique is adopted to fulfill the idea regarding to rational approximation, which to choose both the respective numerator and denominator for different control regions. This certainly increases the complexity of the exponential generation circuit and introduces error because of mismatch and nonlinearity of the MOS transistors.

The new approximation functions are again simulated and compared with the ideal exponential curve. Figure 2. 11 plots the variation range and approximation error of the advanced approximation approaches. It is obvious that the acceptable range is extended compared to the first group.

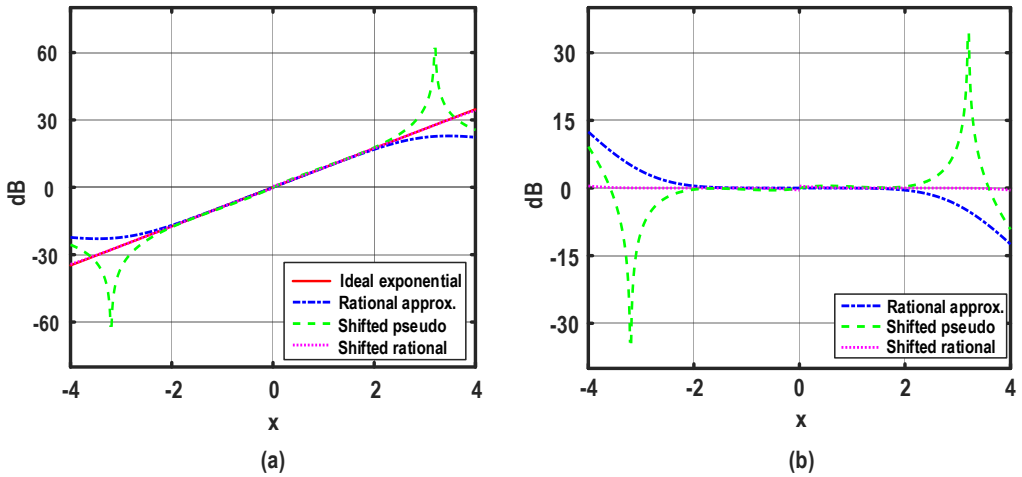


Figure 2. 11 (a) Comparison of advanced approximation functions and (b) their gain errors

To summarize, Table I lists all the approximation functions reviewed in this section. The complexity to implement are indicated, while their accuracy range of 5.5% error and 1 dB error are given.

Table I Summary and Comparison of the Existing Approximation Functions

Exponential approx. methods	No. of devices in references	Equation	x for error ≤ 5.5% / x range	x for error ≤ 1 dB / x range	Need extra switching logic
Taylor series	23 MOSFETs* + 1 CS** + 1 R*** [19]	$1+x+\frac{1}{2}x^2$	-0.6 < x < 0.85 / 1.45	-0.75 < x < 1.15 / 1.9	No
Pseudo exponential	12 MOSFETs + 1 CS [10]	$(1+\frac{1}{2}x)/(1-\frac{1}{2}x)$	-0.85 < x < 0.83 / 1.68	-1.05 < x < 1.05 / 2.1	No
Linear equation multiplication	24 MOSFETs [20]	$(1+\frac{x}{3})^3$	-0.55 < x < 0.62 / 1.17	-0.75 < x < 0.9 / 1.65	No
Rational approx. (1st-order)	70 MOSFETs + 14 CSs [15]	$(1+\frac{15}{16}x)/(1-\frac{5}{16}x)$ or $(1+\frac{5}{16}x)/(1-\frac{15}{16}x)$	-2.1 < x < 2.1 / 4.2	-2.3 < x < 2.3 / 4.6	Yes
Rational approx. (2nd-order)	38 MOSFETs [55]	$f(x)=\frac{x^2+6x+12}{x^2-6x+12}$	-2 < x < 2 / 4	-2.3 < x < 2.3 / 4.6	Yes
Enhancement rational approx. (2nd-order)	84 MOSFETs [33]	$e^{-2}f(x+2)$ or $e^{2}f(x-2)$	-4 < x < 4 / 8	-4.6 < x < 4.6 / 9.2	Yes
Parasitic BJT	3 MOSFETs + 2 BJT + 2 Rs [28]	e^x	$-\infty < x < \infty$ / ∞	$-\infty < x < \infty$ / ∞	No

* MOSFET is a metal-oxide-semiconductor field-effect transistor. ** CS is a current source. *** R is a resistor.

CHAPTER 3

DESIGN OF WIDEBAND VGA FOR HIGH-SPEED WIRELESS COMMUNICATION

3.1 VGA in Wireless Receiver

3.1.1 Architecture of Typical Wireless Receivers

Figure 3. 1 presents the architecture of a conventional wireless receiver. After the signal is received by antenna, low noise amplifier (LNA) is first employed to amplify the signal, followed by two mixers to down-convert the signal to low frequency as well as to separate the I- and Q-path. Because of interfering signals and transmission loss, the quality of down-converted signal is not good enough to be sent directly to ADC for processing. Analog baseband circuits are thus important so as to improve the quality of interested signal before digital processing. While channel selection filter (CSF), such as low-pass filter (LPF), band-pass filter (BPF), etc. filters out those interferences, VGA adjusts the signal level to where it is within the ADC's dynamic range. For communication standards with a channel bandwidth of several tens of megahertz, such as IEEE 802.11a/b/g/n, the cut-off frequency of the analog baseband is decided by the

CSF only. As a result, the bandwidth of VGA must attain an excess bandwidth, roughly 10 times wider than that of the CSF, in order not to affect the designated poles of the CSF [4]. In contrast, for broadband applications whose channel bandwidth are several hundreds of megahertz, the poles of VGA are considered together with those of CSF in order to achieve an overall transfer response like high-order filter but with tunable gain [1], [56]. Although this solution saves both power consumption and chip area, the tunability of the analog baseband is lost where a specific design is only suitable for the dedicated application. Therefore, the topology involving a wideband VGA with a tunable filter is preferable to accommodate a multi-standard receiver or versatile design.

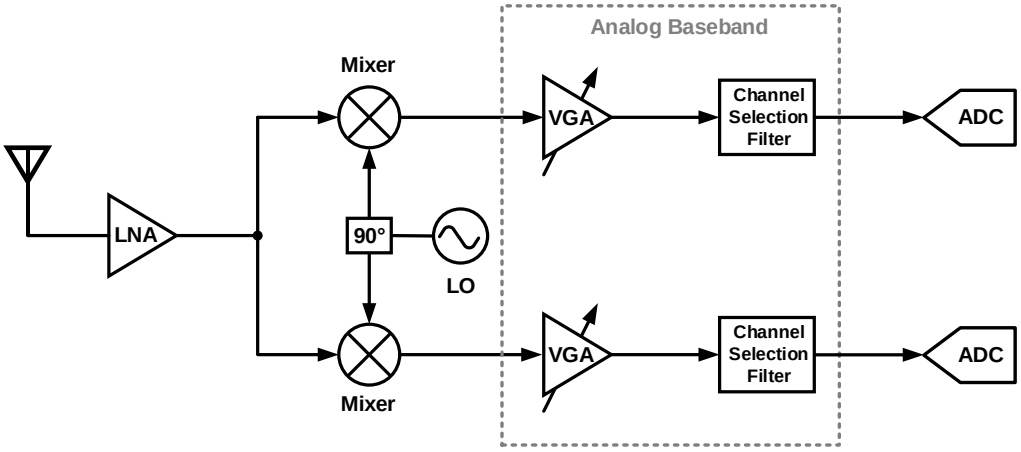


Figure 3. 1 Block diagram of wireless receiver front-end

3.1.2 60 GHz Broadband Wireless Communication

Broadband wireless communications have been received considerable attentions in order to fulfil the rapid growth of data volume and significantly increased transmission rate. To achieve a data rate of multi-Gb/s, the unlicensed frequency band at 60 GHz is extensively explored, such that single channels with

a bandwidth over gigahertz could be deployed without causing spectrum congestion. For wireless personal area network (WPAN), the task group IEEE 802.15.3c was established and defined the standard to operate in the 57-66 GHz range, where each channel has a bandwidth of 2.16 GHz with 1.76 GHz of signal spectrum [57]. If a direct conversion is adopted in the receiver architecture, the analog baseband should have an upper cut-off frequency of 880 MHz. Similarly, IEEE 802.11ad, or WiGig, for wireless local area network (WLAN) also adopts the 60 GHz millimeter wave frequency band, covering from 57 to 71 GHz which is subdivided into six channels. With either single carrier or OFDM modulation, the transmission rate is up to multiple gigabit per second, making it possible to transmit uncompressed UHD video over wireless network. For such a high frequency and wide bandwidth, the frond-end circuits take most of the chip area by using lots of inductors and consume most of the power to offer a high signal to noise ratio. Hence, it is highly desirable that the VGA is compact and power efficient, which helps to ensure the overall design is within the area and power budget. In this chapter, our aim is to design an inductorless wideband VGA that is suitable for 60 GHz wireless communication.

3.1.3 Design Considerations

Besides the bandwidth requirement, there are other design specifications we need to take care of, such as noise performance, linearity, power consumption, etc. We will discuss them subsequently.

Noise The input-referred noise (IRN) or noise figure (NF) determines the sensitivity of the VGA by setting the minimum input level that maintains an

acceptable signal-to-noise ratio (SNR) for processing. For cascaded stages, the noise from the front stages contributes much more than those at back, since the latter ones are divided by the gain of preceding stages. Therefore, arranging high gain stages in front of low gain stages may help improve the overall noise performance.

Linearity It is important that the VGA operates in non-saturated region, such that the information carried with signal amplitude is well delivered. The linearity is evaluated by either the 1 dB compression point (P1dB) or the third-order interception point (IP3), which have a difference around 10 dBm. Different from noise performance, the linearity of a cascaded system is mainly determined by the last stage while lower gain of the front stages help to have a better linearity. Consequently, trade-off exists between noise and linearity.

Power consumption Low power consumption is always attractive as it extends the battery life and generates less heat. However, other parameters could be degraded a lot as a result of low supply voltage or limited current density. Therefore, choice need to be made in order to balance among each specification.

Robustness It is desirable that the circuit provides a universal performance under various circumstances. Process variation and temperature effect are thus taken into considerations, verified by Monte Carlo simulation or corner simulations.

3.2 Novel Exponential Approximation with Double Tuning

Consider the circuit shown in Figure 3. 2, a common source amplifier, M_1, is biased in the triode region. I_0 is an ideal current source and R_L is the load resistor.

Now we would like to study how the input common mode voltage effects the transconductance of the transistor and further the gain of the amplifier.

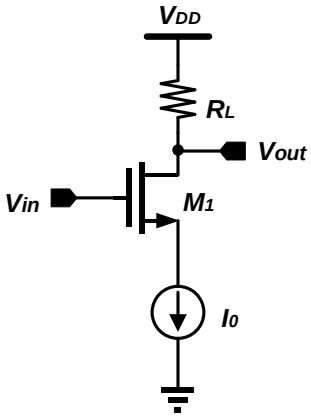


Figure 3. 2 Triode-biased common source amplifier

For a MOS device working in the triode region, its drain current is given by

$$i_D = K\left[(v_{GS} - V_T)v_{DS} - \frac{1}{2}v_{DS}^2\right] \tag{3.1}$$

where $K = \mu C_{ox}\, W/L$. μ is the charge-carrier effective mobility; C_{ox} is the gate oxide capacitance per unit area; W is the gate width; L is the gate length and V_{TH} is the threshold voltage. The equation can be rewritten as

$$(v_G - v_S - V_{TH})(v_D - v_S) - \frac{1}{2}(v_D - v_S)^2 = \frac{i_D}{K} \tag{3.2}$$

Since the current source is ideal, v_D is independent of the gate voltage. In order to produce the same drain current when v_G changes, v_S must change accordingly. Rearrange (3.2) as

$$v_S^2 - 2(v_G - V_{TH})v_S + \left[2(v_G - V_{TH})v_D - v_D^2 - \frac{2i_D}{K}\right] = 0 \tag{3.3}$$

Then, v_S can be expressed w.r.t. v_G:

$$v_S = (v_G - V_{TH}) \pm \sqrt{(v_G - v_D - V_{TH})^2 + \frac{2i_D}{K}} \tag{3.4}$$

Since the overdrive voltage $v_{ov} = (v_G - v_S - V_{TH}) > 0$, only the one with minus sign is applicable, and we have

$$v_{DS} = -(v_G - v_D - V_{TH}) + \sqrt{(v_G - v_D - V_{TH})^2 + \frac{2i_D}{K}} \tag{3.5}$$

The transconductance, g_m, is the derivative of i_D w.r.t. v_{GS}, thus

$$g_m = \frac{\partial i_D}{\partial v_{GS}} = K v_{DS} \tag{3.6}$$

Substitute equation (3.5) into equation (3.6), obtaining

$$g_m = K\left[-(v_G - v_D - V_{TH}) + \sqrt{(v_G - v_D - V_{TH})^2 + \frac{2i_D}{K}}\right] \tag{3.7}$$

Then it can be simplified in the form that

$$g_m = K'\left(-x + \sqrt{x^2 + 1}\right) \tag{3.8}$$

with

$$K' = \frac{K}{\sqrt{2i_D/K}} \tag{3.9}$$

$$x = \frac{(v_G - v_D - V_{TH})}{\sqrt{2i_D/K}} \tag{3.10}$$

According to Taylor series,

$$\sqrt{x^2+1} \approx 1 + \frac{x^2}{2} \tag{3.11}$$

Hence,

$$g_m = K' e^{-x} \tag{3.12}$$

The comparison between Taylor series approximation and the new approximation function, $f(x) = -x + \sqrt{x^2+1}$, is illustrated in the figure below, showing the new equation has a wider approximate range and less gain error especially when x increases to 1. For a gain error of less than 0.5 dB, the x range is from -0.75 to 0.75, which is corresponding to a gain range of 13dB.

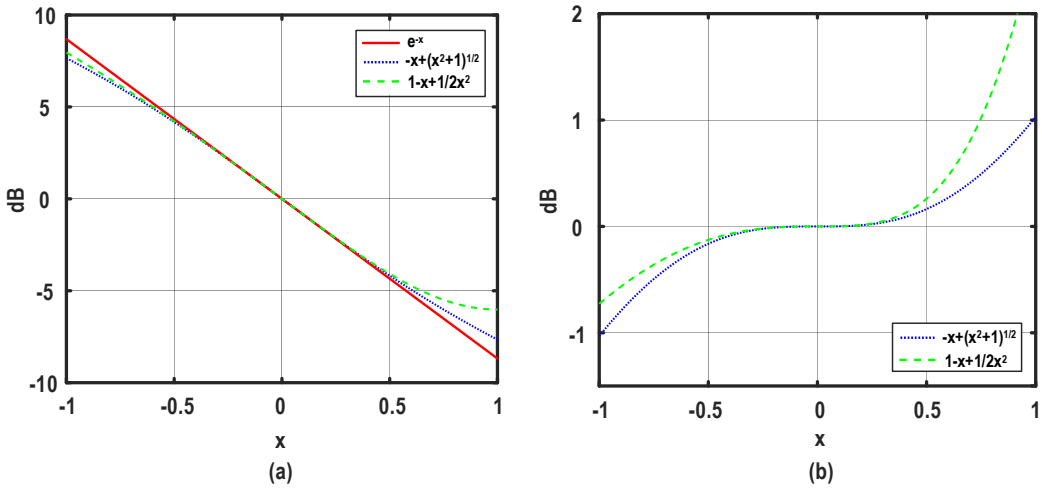


Figure 3. 3 (a) Comparison between the proposed approximation equation with Taylor series and (b) their dB-linear errors.

Meanwhile, different from the amplifiers working in the saturation region, the output resistance of the triode transistor changes accordingly when its bias voltage is changed, and its value is comparable to the load resistor such that one cannot neglect the output resistance of its own. The drain-to-source output conductance of the triode operating transistor is calculated from (3.1), i.e.

$$g_{ds} = \frac{\partial i_D}{\partial v_{DS}} = K(v_{GS} - V_{TH} - v_{DS}) = \sqrt{2i_D K} \cdot x \qquad (3.13)$$

The overall output resistance of the amplifier is given by

$$R_{total} = \frac{1}{\frac{1}{R_L} + g_{ds}} \qquad (3.14)$$

If the load is replaced by a diode connected transistor as shown in Figure 3. 4, the output resistance can be rewritten as

$$R_{total} = \frac{1}{g_{ds1} + g_{m2}} = \frac{1}{\sqrt{2i_D K_1} \cdot (c + x)} \qquad (3.15)$$

with

$$c = \sqrt{K_2/K_1} \qquad (3.16)$$

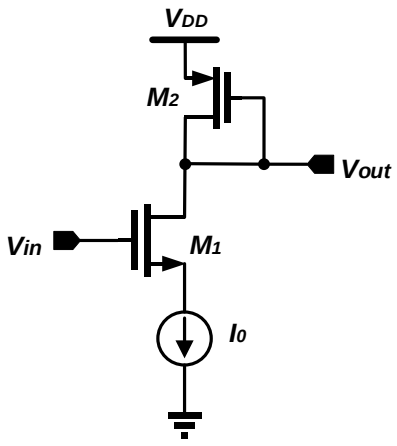


Figure 3. 4 Triode-biased NMOS with diode-connected PMOS

Although g_{ds} is linearly proportional to the variable x, after paralleled with the load resistor, the resultant output resistance can be modified to dB-linear like curve if a certain value of c is chosen. Figure 3. 5 plots the function of

$g(x) = 1/(c + x)$ in dB scale when different c is given. It is found that within the same variable range as $f(x)$, $0 \leq x \leq 1$, a smaller change in $g(x)$ and a better dB-linearity are observed as c is increased. It is found that within the same variable range, $0 \leq x \leq 1$, a smaller change in $g(x)$ and a better dB-linearity are observed as c is increased.

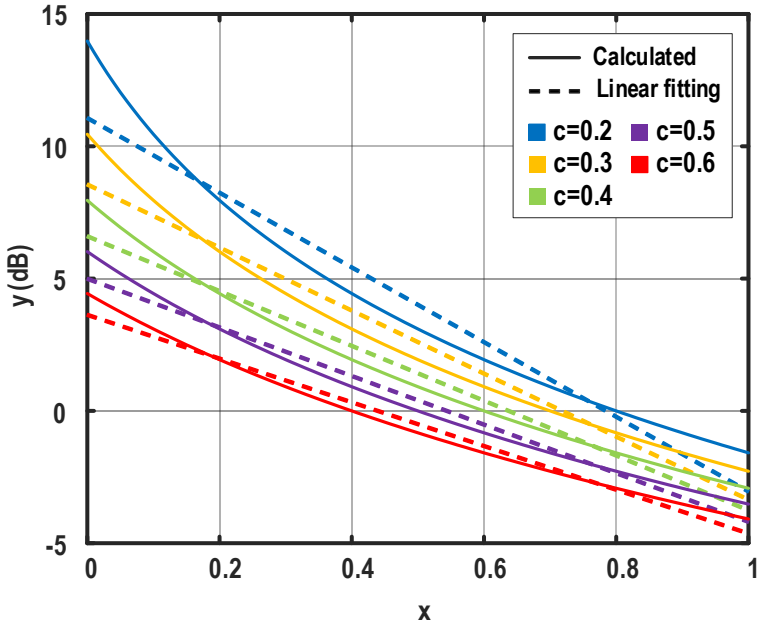


Figure 3. 5 The effect of parameter *c* on dB-linearity of $g(x) = 1/(c + x)$

Therefore, it is clear when the gate voltage applied to a transistor operating in triode region linearly increased, its transconductance decreases exponentially, while its output resistance also decreases and is nonnegligible. Recall that the overall gain of the amplifier depends on both transconductance and output resistance, converted to dB scale obtaining

$$Gain\ range(dB) = change\ in\ gm\ (dB) + change\ in\ R_{total}\ (dB)$$

We can make use of the changes in both to achieve a wider gain variation range above 20 dB without sacrificing its dB-linear accuracy.

3.3 Proposed dB-Linear Variable Gain Cell

The circuit schematic of the proposed wideband gain cell is shown in Figure 3. 6, which adopts a source coupled differential pair operating in the triode region and active inductors as load to extend its bandwidth. Designed in a standard 65 nm CMOS process, deep N-well is not available in this process and thus all body of NMOS are tied to GND.

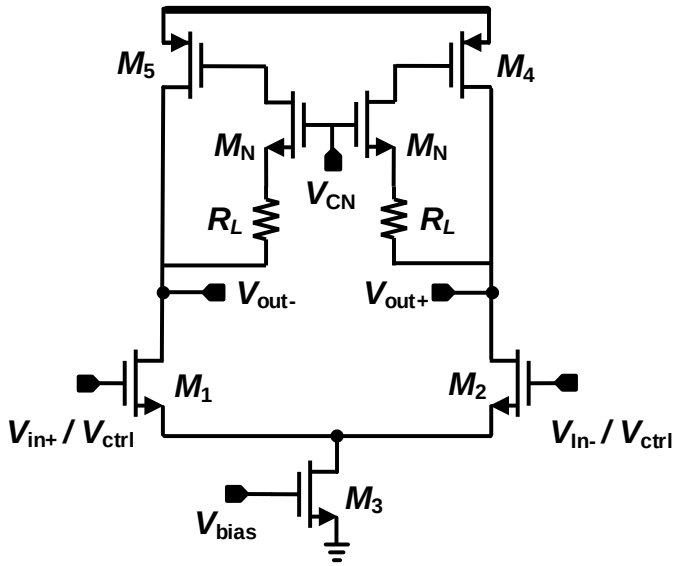


Figure 3. 6 Schematic of proposed variable gain cell

3.3.1 Gain Error Compensation

The red curve in Figure 3. 7 depicts the operating algorithm of the input differential pair. As the control voltage increasing, the overdrive voltage tends to increase, while the voltage at the output node is invariant due to the same

operating condition of the load transistor. However, the current flows through must be constant, forcing the source voltage of the input pair to be elevated, such that the drain-source voltage across the transistor is decreased. Together with the increased overdrive voltage, the input pair operates from moderate triode region to deep triode region and the resultant current remains constant.

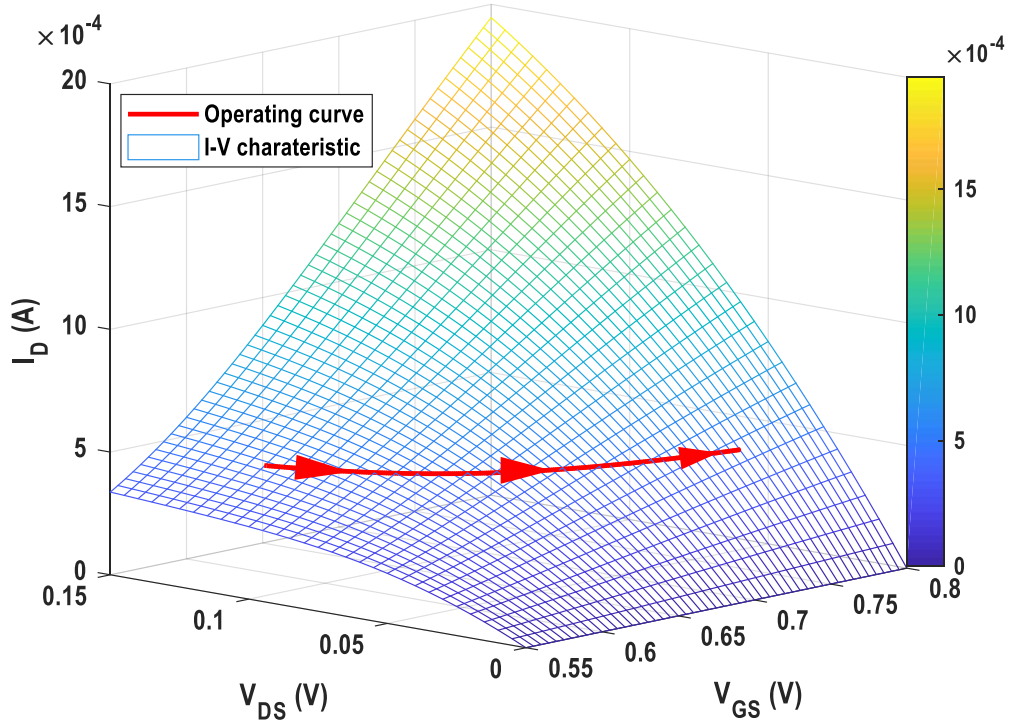


Figure 3. 7 I-V characteristic of the input transistor and its operating curve

The above mathematical analysis in Section 3.2 is based on the traditional characteristic equation, where all second-order effects and nonidealities are neglected. In order to have a more accurate analytical result which is consistent with the simulation result, these factors must be considered and included properly in the modified equation. First, for short channel devices, the channel-length modulation (λ) effect is severe. Nevertheless, such second-order effect will only

affect the drain current in the saturation region, whereas our interest lays on its triode operation, so that the effect of λ has no impact on our proposed circuit. Next, the body effect may also deviate the result from calculated, since the bulk of the input device is tied to the ground instead of its source. However, it is observed that the changes in the source voltage of the differential pair is trivial, resulting in a relatively constant threshold voltage (change less than 10 mV or 2%) throughout the entire working region. Therefore, it is reasonable to ignore body effect in our analysis. Lastly, with device dimensions continuing to scale down to sub-micrometre, short-channel effects, such as threshold voltage variation, mobility degradation with vertical field, velocity saturation, etc., should not be neglected [46]. Examining on the proposed circuit, mobility degradation manifests itself strongly because the overdrive voltage is substantially high. This phenomenon can also be revealed from the current-to-voltage characteristic of the simulation result plotted in Figure 3. 7. Therefore, a more accurate equation to model the short channel device is given by

$$i_D = \frac{\alpha K[(v_{GS} - V_{TH})v_{DS}]}{1 + \theta(v_{GS} - V_{TH})} \tag{3.17}$$

where θ is a fitting parameter to describe the effect of mobility degradation with vertical field, and α is another fitting parameter to fit the calculated results with simulation results better. From the simulation, it is found that θ and α are 0.54 and 0.75 respectively. Thereafter, the transconductance is expressed as

$$g_m = \frac{\partial i_D}{\partial v_{GS}} = \frac{\alpha K v_{DS}}{[1 + \theta(v_{GS} - V_{TH})]^2} \tag{3.18}$$

Realizing that i_D is always equal to half of the tail current and v_D is fixed due to invariant bias condition for the load transistor, we can solve v_S from the new current-voltage equation (3.17)

$$v_S = \frac{1}{2}\left[\left(v_G - V_{TH} + v_D - \frac{\theta i_D}{\alpha K}\right)\right.$$

$$\left. - \sqrt{\left(v_G - v_D - V_{TH} + \frac{\theta i_D}{\alpha K}\right)^2 + \frac{4 i_D}{\alpha K}}\right] \qquad (3.19)$$

Therefore, its drain-source voltage and overdrive voltage are given by

$$v_{DS} = \frac{1}{2}\left[-(v_G - V_{TH} - v_D) + \frac{\theta i_D}{\alpha K}\right.$$

$$\left. + \sqrt{\left(v_G - v_D - V_{TH} + \frac{\theta i_D}{\alpha K}\right)^2 + \frac{4 i_D}{\alpha K}}\right] \qquad (3.20)$$

$$v_{0V} = \frac{1}{2}\left[(v_G - V_{TH} - v_D) + \frac{\theta i_D}{\alpha K}\right.$$

$$\left. + \sqrt{\left(v_G - v_D - V_{TH} + \frac{\theta i_D}{\alpha K}\right)^2 + \frac{4 i_D}{\alpha K}}\right] \qquad (3.21)$$

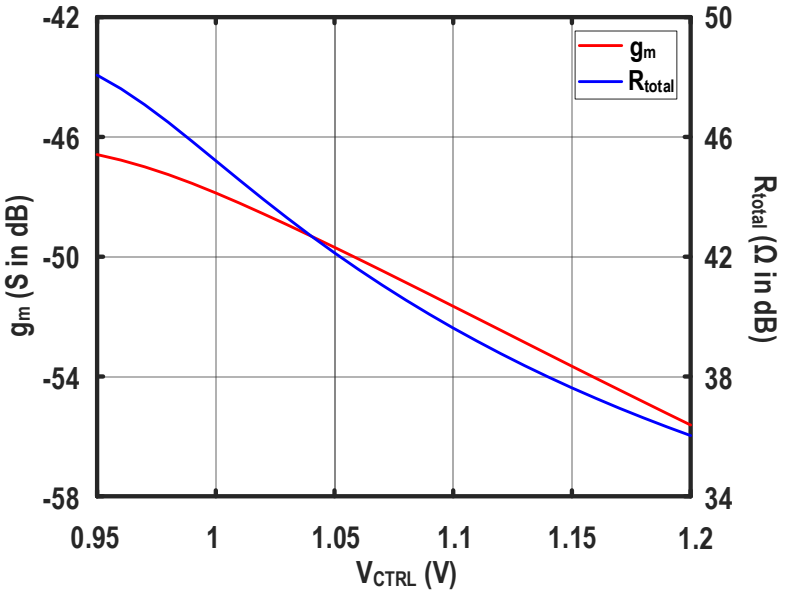


Figure 3. 8 Simulation results of g_m and R_{total} versus V_{CTRL}

With the active inductor as load, its load resistance is equivalent to a diode-connected transistor at low frequency. Therefore, given a desired variation range and dB-linear error, the size of M_4 and M_5 can be decided. The simulation results of the input transconductance and overall output resistance are plotted in Figure 3. 8. The variation range of g_m is from -46.6 to -55.6 dB, providing a change of 9dB, while R_{total} is designed to vary from 36 to 48 dB, providing a change of 12dB. As a result, a total of 21dB can be expected from a single gain cell.

Interestingly, the changes of transconductance and output resistance in dB scale present a concave and a convex curve respectively, making them complementary to each other. The dB-linear error of g_m is positive when the error of R_{total} is negative as shown in Figure 3. 9, and vice versa, the error of g_m is negative when the error of R_{total} is positive. Overall, a combination of the transconductance and output resistance changes can be expected, with a smaller gain error.

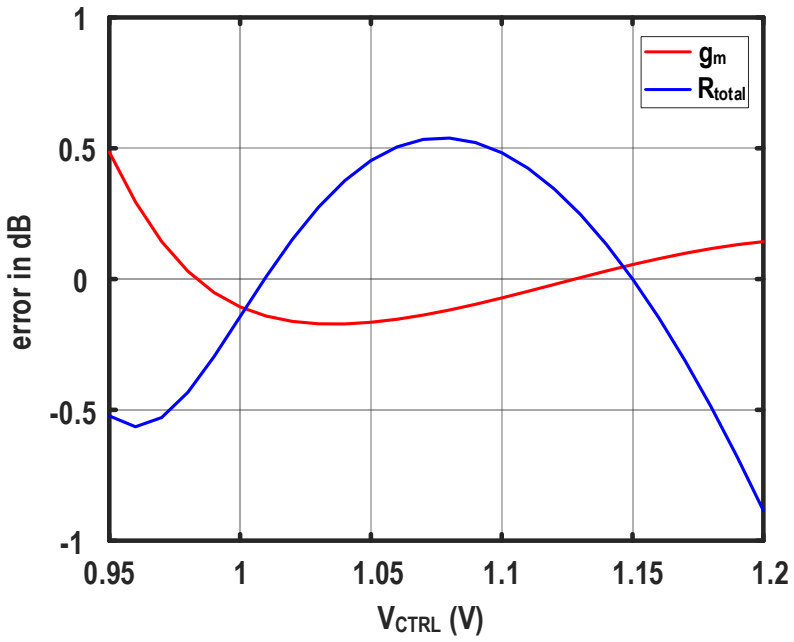


Figure 3. 9 dB-linear error of g_m and R_{total}

To determine the best size of the transistors to use in the proposed design, simulation results of gain characteristics are compared as shown in Figure 3. 10. When smaller size of the input transistors is used, the transistors enter into the triode region later since higher overdrive voltage and drain-to-source voltage are required to attain the same current. Meanwhile, the slope of gain variation is gradual, leading to a lower gain range within a limited control voltage, i.e. below the supply voltage of 1.2V. As the aspect ratio of the input transistors increases, triode operation occurs at a lower control voltage while the slope becomes steeper. Therefore, the gain variation range is extended, but with a larger gain error. To have a balance in the trade-off between the gain range and gain error, W/L=200 is selected in our design.

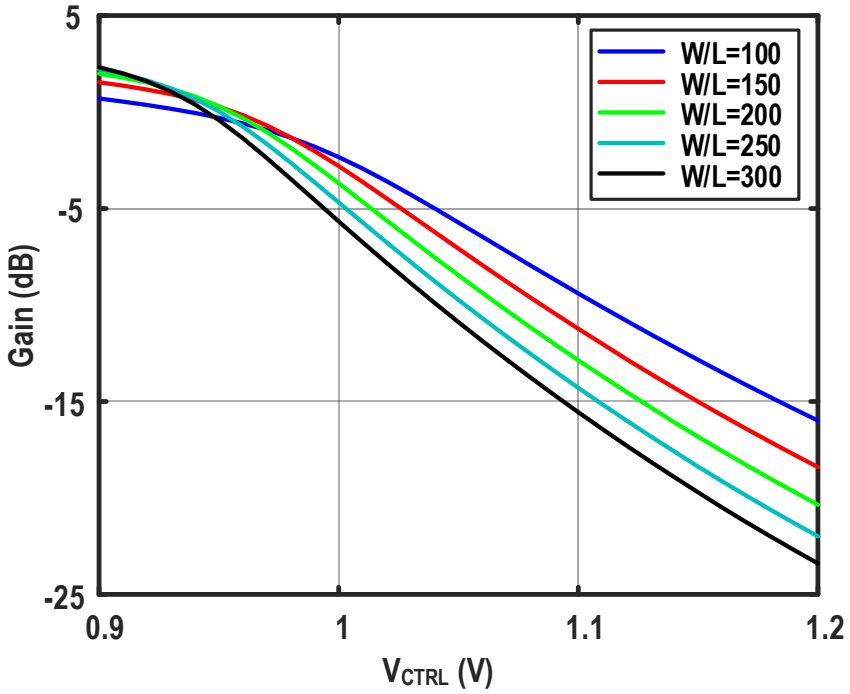


Figure 3. 10 Gain characteristic vs. different size of input transistors

3.3.2 Bandwidth Extension with Active Inductor

The upper cut-off frequency of the amplifier is usually limited by the parasitic capacitance associated with the output node. On-chip inductors can be added in series with the load resistor, thus resonating with the parasitic capacitance and extending the bandwidth. However, passive inductors occupy extremely large die area compared to MOSFET. To solve this problem, active inductors are employed to fulfil both the chip area limitation and bandwidth requirement [58], [59].

Figure 3. 11(a) depicts a simple active inductor realized by the source follower, where the gate of transistor M_1 is connected to a series resistor R_S. Taking its gate-source parasitic capacitance into consideration, the output impedance seen from the source node can be written as

$$Z_{out} = \frac{R_s C_{GS} s + 1}{g_m + C_{GS} s} \tag{3.22}$$

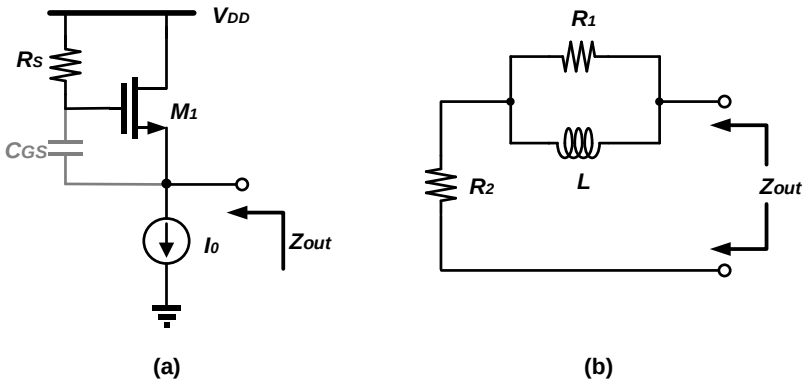


Figure 3. 11 (a) Inductive output provided by a source follower, and (b) equivalent network of (a).

The output impedance is equivalent to a diode-connected transistor when $s = 0$, while $Z_{out} = R_s$ when s goes into infinity. If $R_s \gg 1/g_m$, an inductive behavior is expected from the circuit. Then the output impedance can be modeled as a lossy inductor in series with a resistor, as shown in Figure 3. 11(b), where

$$R_1 = R_s - \frac{1}{g_m} \tag{3.23}$$

$$R_2 = \frac{1}{g_m} \tag{3.24}$$

$$L = \frac{C_{GS}}{g_m}\left(R_s - \frac{1}{g_m}\right) \tag{3.25}$$

The large voltage headroom active inductor consumes is the primary disadvantage which restrains itself for low supply voltage applications. However, the input transistors in our design are biased in triode region instead of conventional saturation-biased. Therefore, such disadvantage becomes an advantage in our design. Moreover, to incorporate a flexibility of peaking magnitude, a MOS resistor is added in series with the passive resistor, arriving

the final design in Figure 3. 6. By tuning the gate voltage M_N, the resultant R_s in equation (3.23) and (3.25) is changed, and thus the inductance provided by the active load.

The frequency response under different gain settings is shown in Figure 3. 12. With the help of active inductor, bandwidth is extended, and the peaking is controlled within 3dB. The peaking is designed to appear at a relatively high frequency, in order to compensate the loss in other cell, which will be explained in detail later.

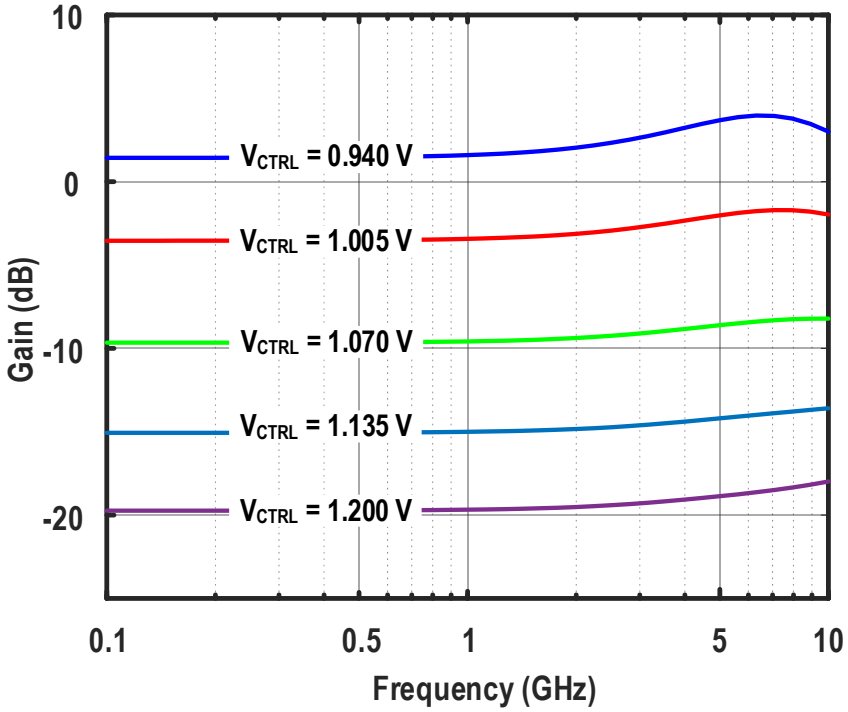


Figure 3. 12 Frequency response of variable gain cell under different gain settings

From the figure above, it is obvious that the peaking under different gain setting affects the frequency response in different ways. To study whether the peaking will affect the dB-linearity, simulations of gain characteristic at various

frequencies are conducted. As depicted in Figure 3. 13, the chosen frequencies are 100 MHz, 2 GHz, 4 GHz, and 6 GHz, respectively. Although the magnitude of gain varies slightly, the overall dB-linearity maintains, presenting a ±0.5 dB error with V_{ctrl} varying from 0.94 V to 1.2 V regardless frequency.

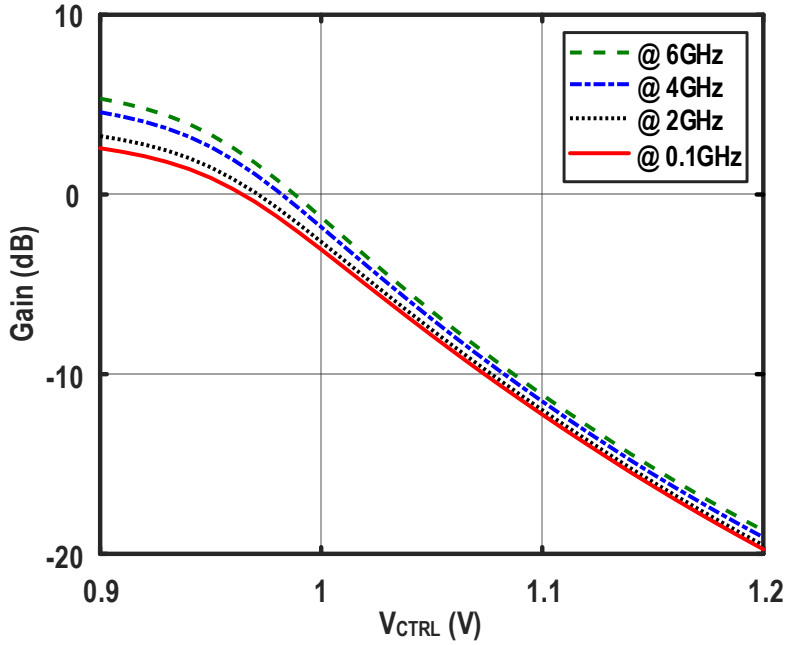


Figure 3. 13 Gain characteristic at different frequencies

3.4 Design of Fixed Gain Cell

As the variable gain cell possesses a broadband feature and exploits the triode-region operating transistors, the absolute gain of a single cell is low, where most part of its gain range is negative. Therefore, a fixed gain cell to boost the overall gain is required. A similar topology to the variable gain cell is used, except that the input differential pairs are biased in their saturation regions, as shown in Figure 3. 14.

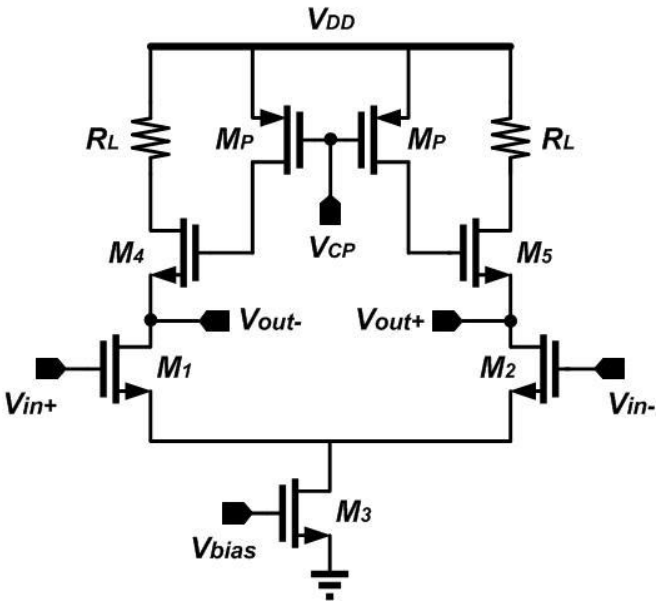


Figure 3. 14 Schematic of fixed gain cell

The major function of this cell is to provide an enough gain, such that the overall VGA can present a reasonable gain range. Therefore, passive resistor, R_L, is added in series with diode connected load, to increase the low frequency gain [50]. Active inductors are implemented again to alleviate the effect of parasitic capacitance, where PMOS in triode region is employed as the peaking resistor and the amount of peaking can be controlled by tuning the gate voltage of PMOS.

Figure 3. 15 plots the simulation results of the fixed gain cell. The low frequency gain is nearly 9dB, and bandwidth is extended with acceptable peaking. The active inductor is responsive to the control voltage of the series resistor, V_{CP}, such that the circuit is adjustable under PVT variation.

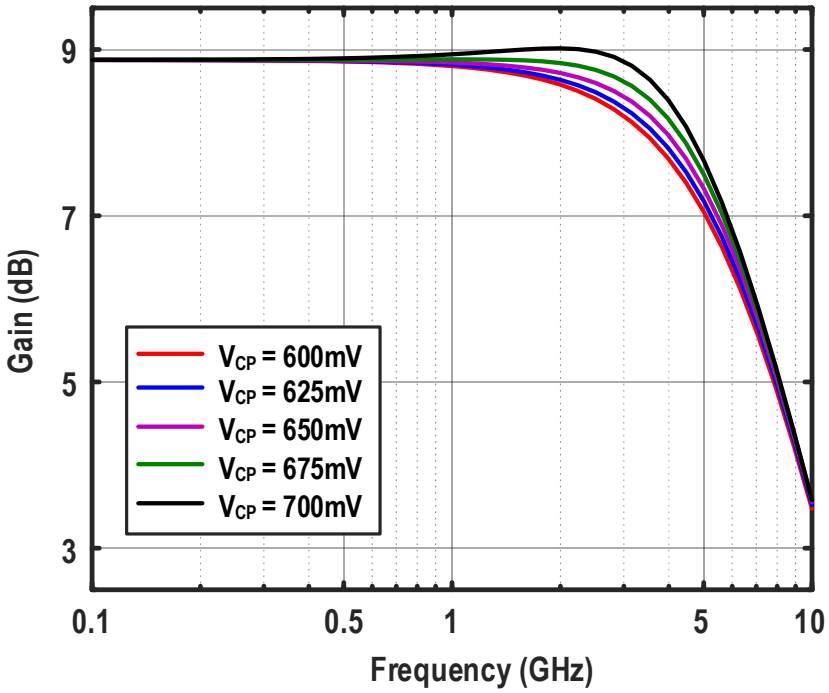


Figure 3. 15 Frequency response of fixed gain cell

3.5 Overall VGA Architecture

To obtain a practical gain variation range, two variable gain cells and two fixed gain cells are needed to achieve a 42dB gain variation from -20dB to 22dB. The configuration is given in Figure 3. 16, where one variable gain cell is connected to one fixed gain cell to form a single stage, followed by another identity stage. A wideband buffer is added for testing purpose.

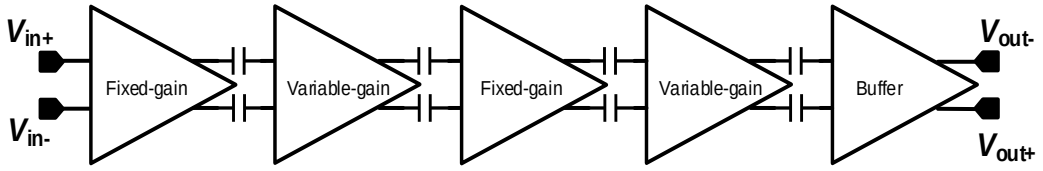


Figure 3. 16 Architecture of the overall VGA

3.5.1 Stage Design of Proposed VGA

Consider a single stage, which includes one fixed gain cell and one variable gain cell. Since the input DC voltage of variable gain cell is used to control the overall gain, the cells must be ac coupled with capacitors, occupying large area but solving the DC offset problem in return. Fixed gain cell is placed preceding variable gain cell in consideration of noise performance and constant input common mode voltage.

Figure 3. 17 plots the frequency response of a single stage, in comparison with that of a solo fixed gain cell and variable gain cell. The high-frequency peaking in the variable gain cell compensates the early drop-off in the fixed gain cell. As a result, the overall frequency response is flat and extended beyond that of the fixed gain cell.

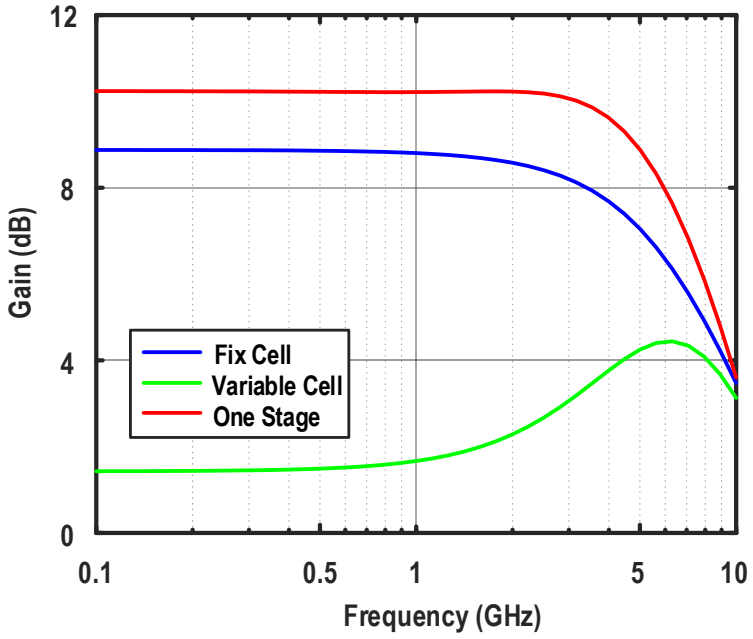


Figure 3. 17 Frequency responses of one stage compared with separate cells

The overall peaking can still be adjusted by either NMOS gate voltage in the

variable gain cell (V_{CN}) or PMOS gate voltage in the fixed gain cell (V_{CP}). Taking the peaking control in the variable gain cell as an example, simulation results are plotted in Figure 3. 18. With V_{CN} decreased from 1.2V to 1.1V, the overall peaking is increased from 0 to 0.5dB, while the bandwidth is increased from 5.8G to 6.4G.

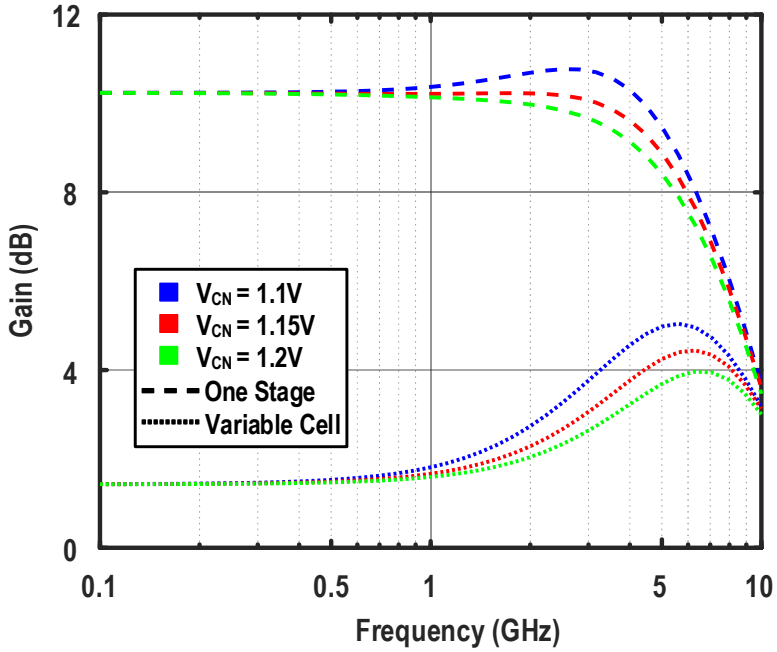


Figure 3. 18 Adjustable peaking in one stage

Finally, after two identical stages are cascaded, the gain characteristic under different temperatures and various corners are simulated, shown in Figure 3. 19 and Figure 3. 20 respectively. We can tell that the dB-linearity is robust; temperature variation will only lead to changes in gain range and different process corner will result in the gain characteristic line shift up or down.

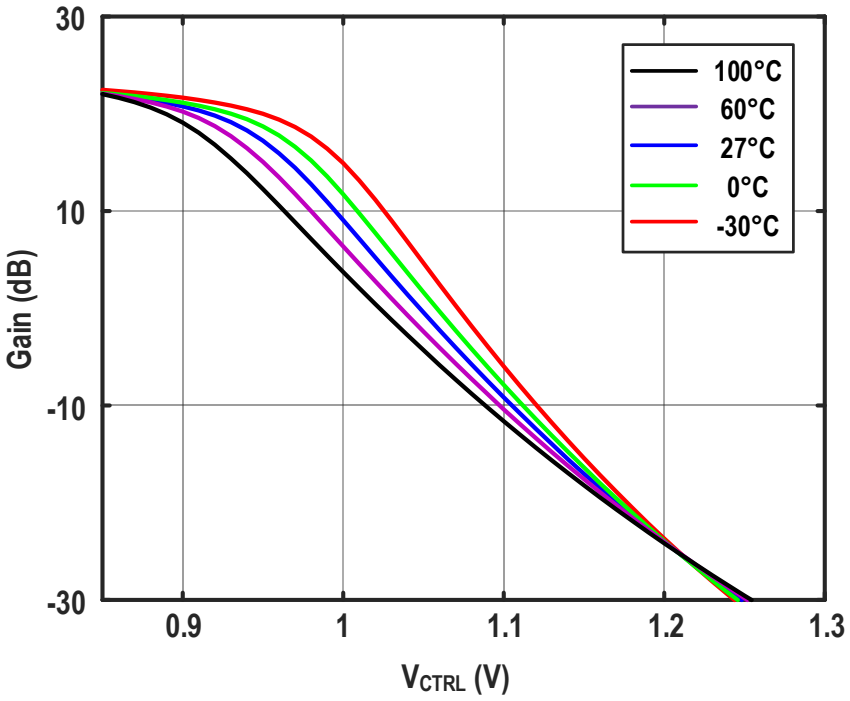


Figure 3. 19 Gain characteristic with temperature variation

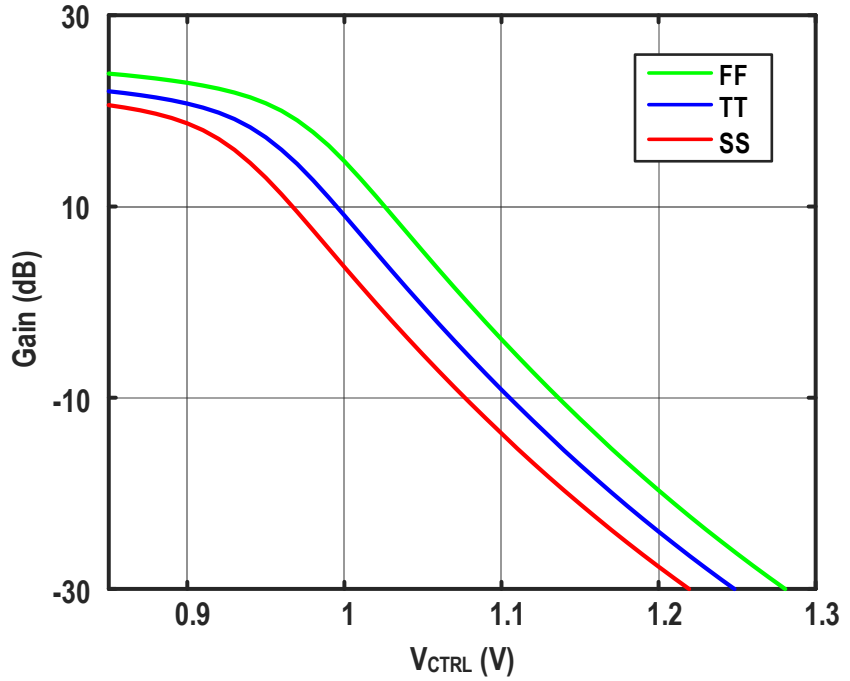


Figure 3. 20 Gain characteristic with different corners

3.5.2 Output Buffer

Since the testing equipment for high frequency measurement usually adopts a standard input impedance of 50 Ω, an output buffer is required to perform output matching and keep the design from large capacitance loading. Generally, the output buffer is designed with no gain, such that the bandwidth is wide enough not to degrade the overall upper cut-off frequency. Meanwhile, the input capacitance of the buffer shall be small enough that it will not exceed the driving ability of the preceding stage.

The f_T doubler shown in Figure 3. 1 provides the same voltage gain as simple differential stage, but its input capacitance is roughly reduced to half. This is because the output of previous stage sees a parallel of two identical transistors, M_1 and M_2 for example, leading to a resultant capacitance equal to half of the gate-source capacitance. Therefore, this topology is widely used as an output butter, which is also adopted in our design.

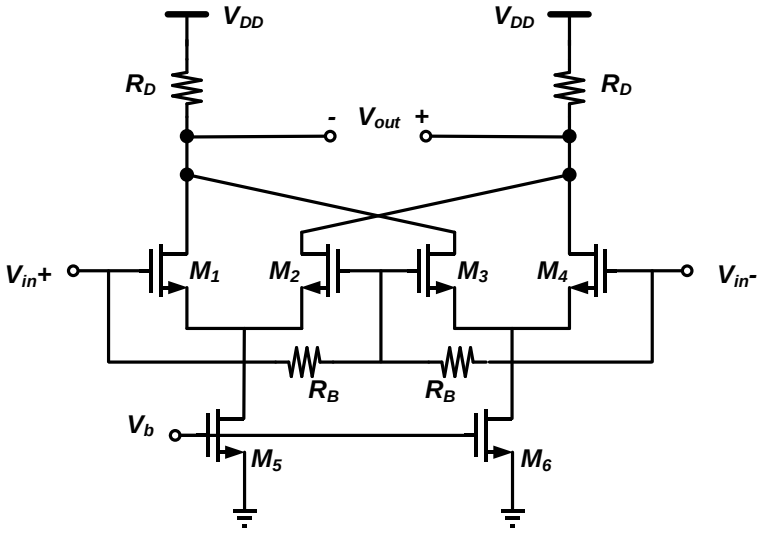


Figure 3. 21 f_T doubler output buffer

3.6 Experimental Result

The circuit was fabricated with Global Foundry 65nm CMOS process and had been measured on the probe station. The frequency response under different gain settings is given in Figure 3. 22. Compared with the simulated ones, the gain range shrinks slightly, and the bandwidth decreases a bit, but the amplifier still manages to achieve a 40 dB gain range with a 4 GHz upper cut-off frequency.

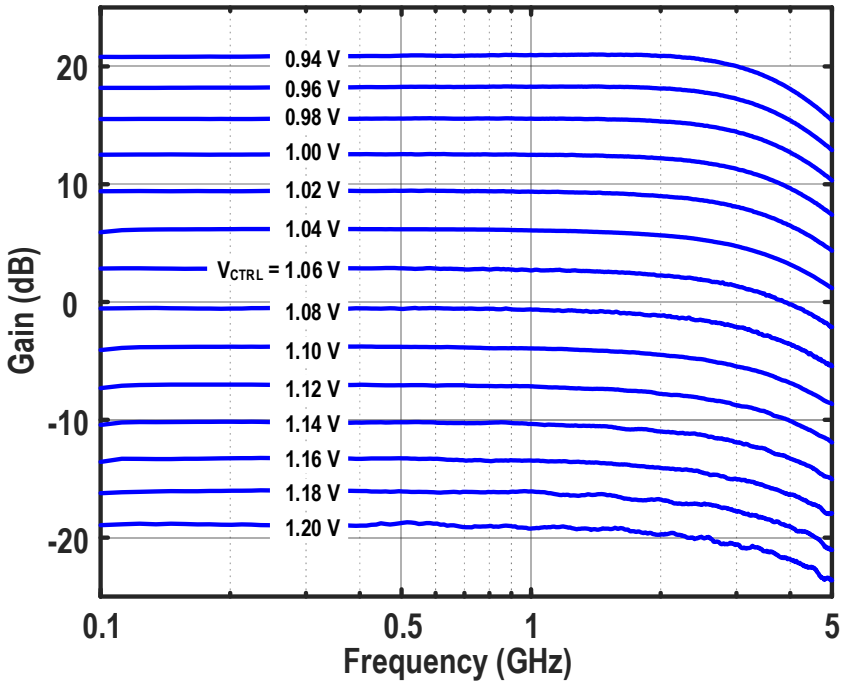
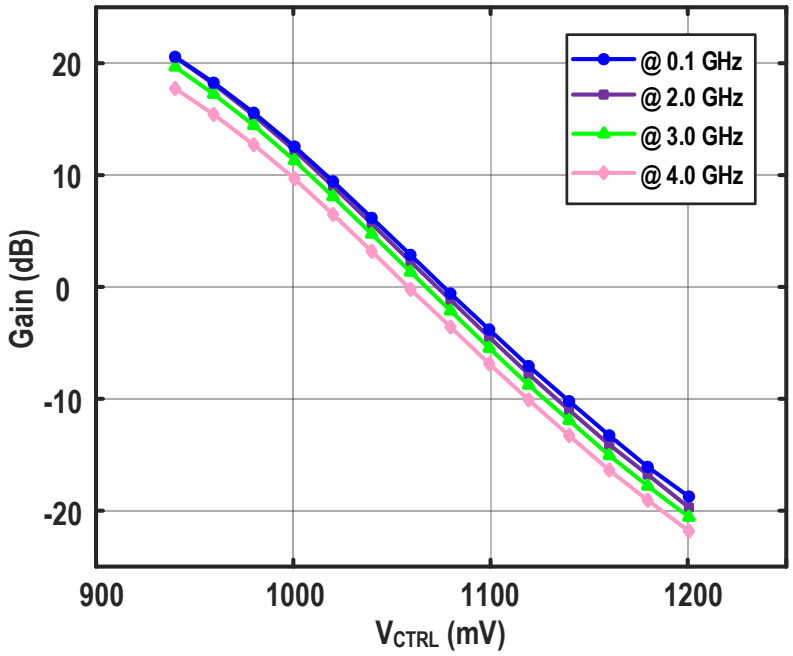
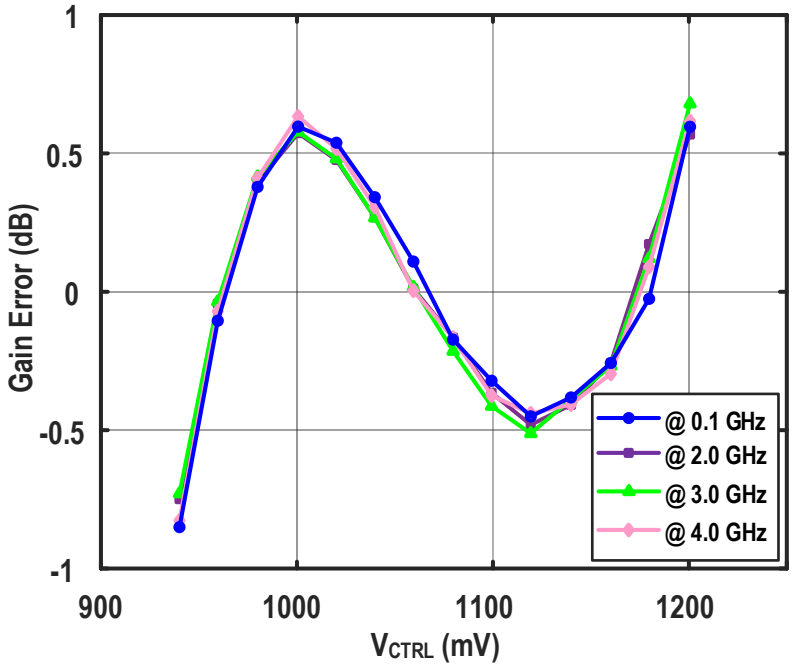


Figure 3. 22 Measured frequency response

Figure 3. 23 shows the gain characteristic of the amplifier plotted from measurement results [Figure 3. 23(a)] and its gain error [Figure 3. 23(b)]. The dB-linear characteristic at different frequencies is well behaved, especially for V_{ctrl} varying from 0.94V to 1.2V. Within this range, gain error is calculated to be less than 1dB.



(a)



(b)

Figure 3. 23 (a) Measured gain characteristic under different frequencies and (b) their corresponding gain errors

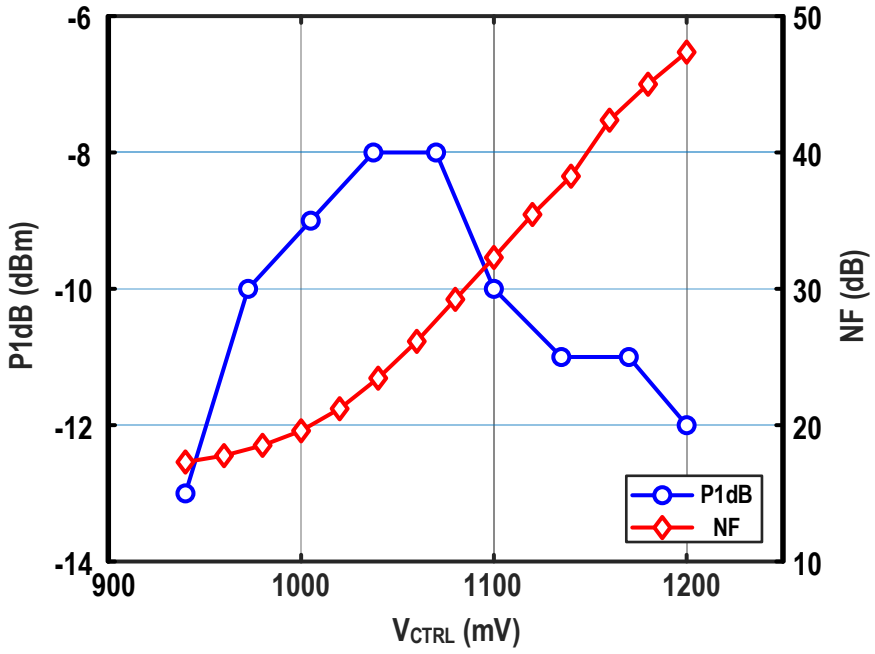
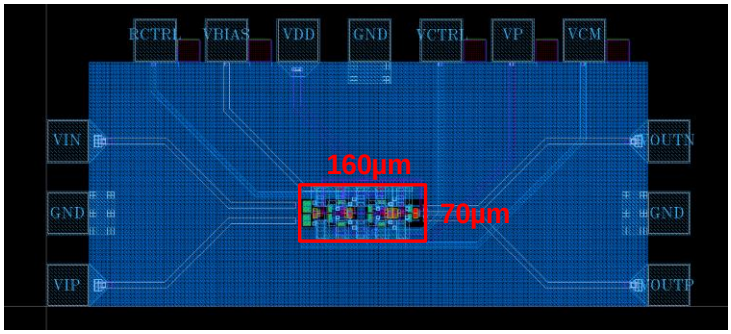


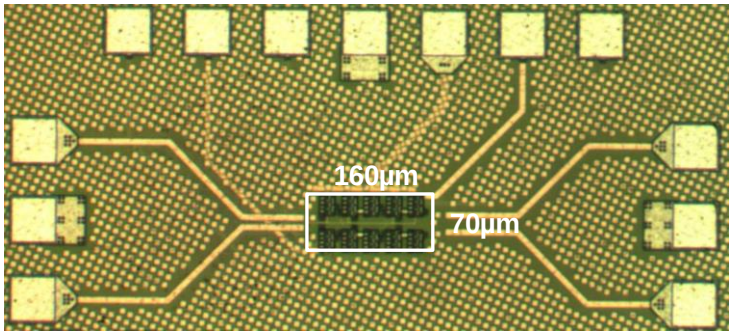
Figure 3. 24 Measured NF and P1dB

Figure 3. 24 depicts the noise figure and input P1dB of the designed VGA for various gain settings. The noise figure increases from 17dB to 47dB with decreasing gain, while input P1dB increases first and decreases for the second half control range. P1dB corresponds to the power where the signal amplitude saturates the input or output node. Under the highest gain setting, the output swing is much larger than the input swing. Consequently, the maximum allowable swing at output will reach first, setting the P1dB. As the overall gain decreases, the amplifier reduces its amplifying effect on the input signal. Thus, to attain the same output swing, larger input signal is needed, leading to an increasing P1dB. However, when the input power reaches a certain degree, the input node will be saturated.

Lastly, the layout and the die photo are given in Figure 3. 25(a) and (b), respectively, showing an active area of only 0.012 mm^2.



(a)



(b)

Figure 3. 25(a) Layout and (b) die photo of the designed VGA

Table II presents the comparison between this work and other state-of-the-art works whose bandwidth is beyond 1 GHz. Compared to other wideband VGAs published in recent years, the bandwidth of the proposed design is further extended. Due to use of active inductors and frequency compensation, the chip area is not increased compared to other wideband design. Although the gain error is not as good as [21], a much larger gain variation range is achieved. Last but not least, the power consumption of the designed VGA is small, owning to the simple method to generate the exponential characteristic. Overall, the designed VGA fulfills the requirement of 60 GHz high-speed wireless communication.

Table II Performance Comparison with Other State-of-the-Art Designs

	TMTT'14 [1]	TMTT'13 [7]	TCASI'12 [18]	TMTT'16 [50]	***This work***
Control method	Digital	Digital	Analog	Analog	**Analog**
dB-linear	Yes	Yes	No	Yes	**Yes**
Gain range (dB)	0.1 ~ 19.6	-10 ~ 8	-10 ~ 50	2 ~ 24	**-20 ~ 20**
Gain error (dB)	0.7	-	-	±0. 3	**±1**
BW (GHz)	0.7	1.9	2.2	2.2	**4**
IP_{1dB} (dBm)	5.6	-12.5	-13 to -55	-2 to -22	**-8 to -13**
Noise	IRN = -145 dBm/Hz	NF = 20 to 27 dB	NF = 17 to 30 dB	NF = 24 to 29 dB	**NF = 17 to 47 dB**
Power (mW)	9.5 ~ 10.8 *	12.2	2.5	3.48	**3.5**
Size (mm^2)	0.156 *	0.048	0.014	0.01	**0.012**
Technology	90 nm CMOS	0.18 μm BiCMOS	90 nm CMOS	65 nm CMOS	**65 nm CMOS**

* including low-pass filter

3.7 Summary

In this chapter, the functionality of VGA block in wireless transceiver and its design considerations are briefly discussed, followed by a detailed explain on the design of proposed VGA. The design goal is stringent as it targets at wideband, low power, wide tuning range at the same time. The method to tune transconductance and overall load simultaneously helps to solve the problem efficiently, while active inductor boosting at different frequency maximizes the bandwidth of cascaded amplifiers. As a result, a linear-in-dB gain variation range beyond 40 dB and a bandwidth over 4 GHz are achieved, with an extremely low power of less than 4 mW.

CHAPTER 4

DESIGN OF AGC SYSTEM FOR HIGH-SPEED WIRELINE COMMUNICATION

4.1 VGA in Optical Receivers

In this section, the architecture of optical transceiver will be introduced, followed by a brief description of the signal modulation which are commonly employed. With the understanding of signal format, design considerations of the post amplifier are revealed. Then the two types of amplifiers (LA and AGC) are compared, giving the facts why AGC amplifier is preferred in the system.

4.1.1 Architecture of Typical Optical Receivers

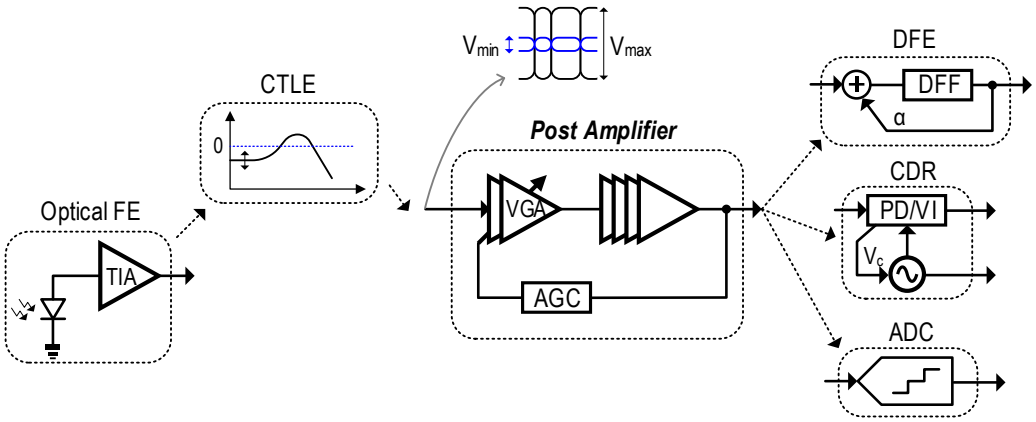


Figure 4. 1 Architecture of optical receiver

Because of the increasing demand to transmit information from one place to another, high-speed transceivers operation at tens of gigabits per second are of great research interest to fulfill the data transfer volume. In both optical and backplane communication networks, serial link transceivers are widely used due to their low cost and high bandwidth. Figure 4. 1 shows the architecture of a typical optical receiver which employs serial link. The photodiode receives the optical signal from the fiber or free space, and generates a current output which is proportional to the strength of the optical signal. The small current is then fed into the transimpedance amplifier (TIA) and produces a voltage signal, completing the conversion from optical signal to electrical signal in voltage domain. Subsequently, as the signal suffers from channel loss during transmission, equalizer (EQ) and post amplifier (PA) are necessary to rebuild the waveform, such that the clock and data recovery circuit (CDR) can extract the information of the original data correctly. For the application of backplane routing, the architecture is similar expect that it could save the trouble of optical-electrical conversion, utilizing voltage information to transmit data directly.

The transmission channel, such as fiber and cable, usually acts as a low-pass filter which possesses much more loss at high frequency than low frequency. The defection in high frequency components will result in inter-symbol interfere (ISI) and thus affect the quality of signal. To solve this problem, equalizer that presents a peaking at high frequency is employed to compensate the channel loss, such that the overall transfer function is flat. On the contrary, post amplifier deals with both low and high frequency components, amplifying the entire spectrum of interest to a desired level homogeneously. A post amplifier can be either a

limiting amplifier (LA) or an automatic gain control (AGC) amplifier. While LA has a preset gain that will be enforced on any level of input signal, the gain of AGC amplifier can be adjusted according to the actual received signal strength, avoiding saturation of large incoming signals.

4.1.2 Signal Format

Binary amplitude modulation, or non-return-to-zero (NRZ) is widely adopted in most optical and backplane communication systems for ease of detection [48]. Logical ONEs and ZEROs are simply represented by two distinguishable voltage levels, each of which lasts for a bit period of T_b seconds. In the long run, it is reasonable to assume that the number of ONEs and ZEROs are equal. However, consecutive ONEs and ZEROs, called "run", may exist and create difficulties to transceiver circuits, especially operations such as AC coupling, DC offset cancellation, and CDR. To alleviate such problem, 8B/10B coding can be employed to limit the maximum run length within 5 bits. A number of standards, including 10-Gigabit Ethernet, adopts such coding to relax many aspects of the design requirements.

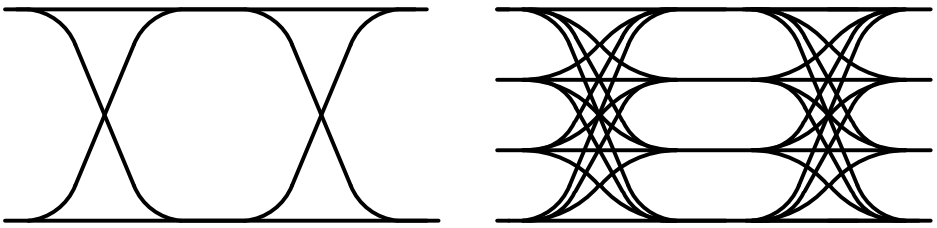


Figure 4. 2 Ideal eye diagram of (a) NRZ and (b) PAM4 signal

Eye diagram is a powerful tool to examine the quality of received or

transmitted data. It accumulates all edges and levels, by folding all bits into a short interval which must be multiple times of the bit period, as shown in Figure 4. 2. Both low-pass and high-pass filtering may affect the eye diagram, leading to eye closure or heavy jitter. If the bandwidth is limited, all rising and falling edges experience slow transition, as shown in Figure 4. 3(a). Then eye opening decreases and jitter increases, since the waveform of each period will not overlap on each other. On the other hand, the output levels may droop significantly for long runs with the present of high-pass filtering [Figure 4. 3(b)]. “DC wander” happens when no transition occurs during a considerable period of time, resulting in a large DC shift and increases in decision errors. Therefore, both lower and upper cut-off frequencies need to be designed carefully to obtain clear eye diagram with minimum ISI.

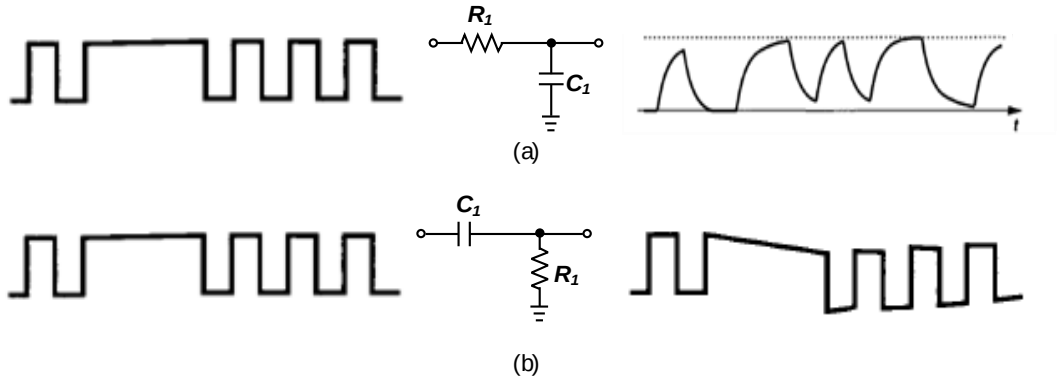


Figure 4. 3 (a) Low-pass and (b) high-pass effect on NRZ signal

Besides the simplest 2-level NRZ signal, multiple levels signal format attracts more and more attention as it brings the possibility to multiply the data rate without increasing the baud rate. Pulse amplitude modulation (PAM4) signaling uses four distinguish levels during transmission [Figure 4. 2(b)], with every

transmission decoded into two bits, thereby doubling the data rate. Nevertheless, the difference between each level is one third of NRZ signaling, in return alleviating the SNR requirement of the system. With a given channel, one can choose the better signal format by comparing the channel loss at their Nyquist frequency [60].

4.1.3 Comparison Between LA and AGC Amplifier

Recall that there are two types of PA, i.e. LA and AGC amplifier. If PAM-4 signaling is used, AGC amplifier must be selected to maintain the linearity of the four-level amplitude [3]. Otherwise, the signal will be distorted by LA due to its saturation nature of operating principle, resulting in unequal spacing between the four levels. Given different peak-to-peak amplitudes of input signal, the lowest and highest level are magnified to the maximum, while the two levels in the middle will reach different levels at the output. Such dependency of channel loss and input condition brings difficulties in setting of decision thresholds and therefore should be avoided.

On the other hand, NRZ signaling has no data information from its amplitude and doesn't have the issue of level distortion if LA is used. However, AGC amplifier is still a better choice in view of the jitter performance [61-63], because over-amplification from LA introduces more jitter and phase distortion, which adds difficulties to the operation of CDR. AGC, in contrast, is able to adjust the gain of its VGA: when the input power is within the AGC dynamic range, the amplifier provides a linear phase response and low deterministic jitter by operating in the linear region; when the input power is further increased, the gain

is set to the lowest level so as to avoid excessive noise amplification and reduce random jitter. As a result, a wider dynamic range and a clearer eye diagram can be achieved with the help of AGC.

4.2 Novel Exponential Generator with Inverse S-Shaped Curve

Although combining approximation functions and successively approximation by shifting and scaling work effectively to enlarge the dB-linear gain range, our aim is to design a simple circuit without compromise on gain variation range and dB-linear accuracy by taking advantage of dynamic operating regions of the MOSFETs.

4.2.1 Mathematical Approach

The proposed negative exponential approximation is based on the general function,

$$g_n(x) = a_n + b_n x + c_n\sqrt{d_n + e_n x + f_n x^2} \tag{4.1}$$

where x is an independent variable, and a_n to f_n are coefficients. At $x = 0$, the Taylor series expansion up to the second-order is used for the last term in (4.1) and we have

$$\sqrt{d_n + e_n x + f_n x^2} \approx \sqrt{d_n} + \frac{e_n}{2\sqrt{d_n}}x + \frac{d_n f_n - \frac{e_n^2}{4}}{2d_n^{\frac{3}{2}}}x^2 \tag{4.2}$$

Therefore, (4.1) is rearranged as

$$g_n(x) \approx \left(a_n + c_n\sqrt{d_n}\right) + \left(b_n + \frac{c_n e_n}{2\sqrt{d_n}}\right)x + c_n\frac{d_n f_n - \frac{e_n^2}{4}}{2d_n^{\frac{3}{2}}}x^2$$

$$= O_n + P_n x + Q_n x^2 \tag{4.3}$$

Assuming $-P_n/O_n = \sqrt{2Q_n/O_n} = K_n$, where $P_n < 0$, the proposed exponential approximation becomes

$$g_n(x) \approx O_n e^{-K_n x} \tag{4.4}$$

To give a fair mathematical comparison with Table I, equation (4.1) is normalized to

$$G_n(x) = A_n + B_n x + C_n\sqrt{D_n + E_n x + F_n x^2} \approx e^{-x} \tag{4.5}$$

where A_n to F_n are the normalized coefficients. Thereafter, by adjusting the different groups of the normalized coefficients (A_1 to F_1) and (A_2 to F_2), one concave function $G_1(x)$ and the other convex function $G_2(x)$ can be obtained to approximate the same ideal e^{-x} around the origin, as shown in Figure 4. 4. Their approximation regions may vary slightly, but both approximation errors decrease as x approaches "0".

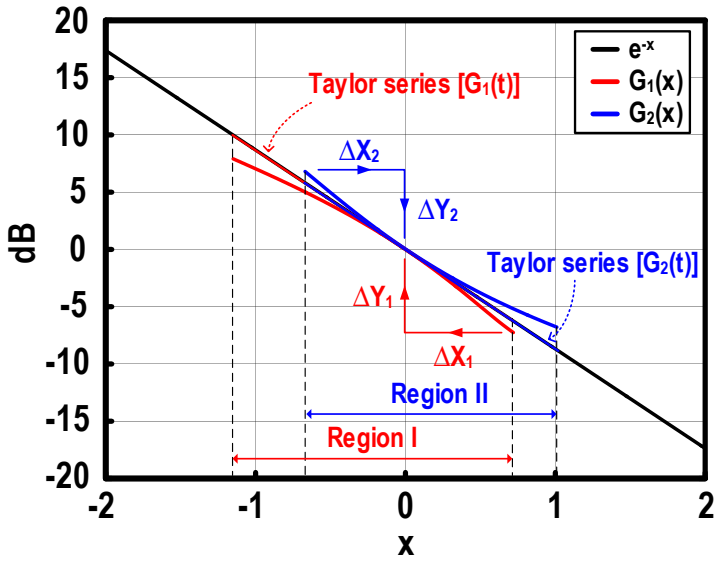


Figure 4. 4 Concave and convex single-function generation

To increase both the available control input and the dB-linear gain range, two shifted single functions, $G_{1s}(x)$ and $G_{2s}(x)$, are combined as a dual Taylor series approximation at the reference point [$x = 0$ in Figure 4. 5]. There are two ways to achieve these coefficients: (i) we preset pure mathematical coefficients and design the circuit parameters to accommodate them; (ii) we initially design the circuit parameters to obtain the gain error within ±1dB, and then calculate these coefficients. The latter is adopted in this work. We shift $G_1(x)$ towards $-x$ direction by an amount equal to ΔX_1, and then move upwards $G_1(x + \Delta X_1)$ by ΔY_1 in $+y$ direction. $G_{1s}(x)$ is obtained and plotted in Figure 4. 5 with the red curve, which remains the concave feature over Region I. Inversely, $G_2(x)$ is shifted by ΔX_2 in $+x$ direction, and $G_2(x + \Delta X_2)$ is moved down by ΔY_2 vertically. We obtain $G_{2s}(x)$, shown in blue, which is a convex function over Region II. The Taylor series of $G_{1s}(x)$ and $G_{2s}(x)$ are both parallel with the ideal exponential line, and the entire curve that we proposed is constructed within a certain gain error, called an "inverse S-shaped curve".

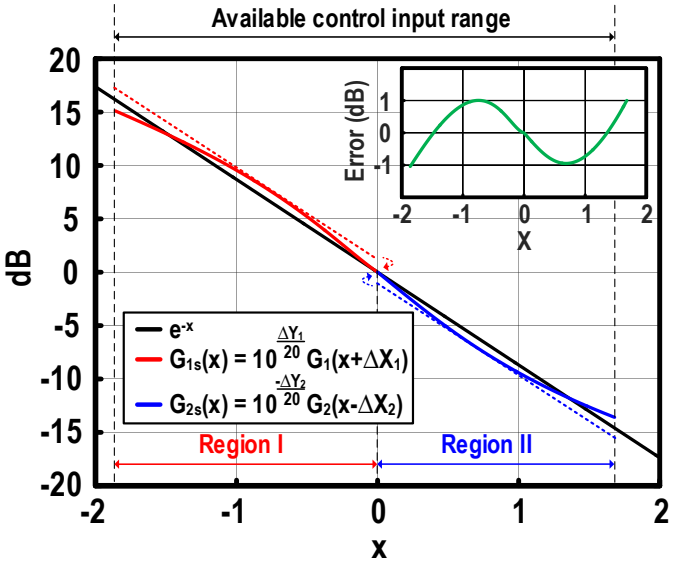
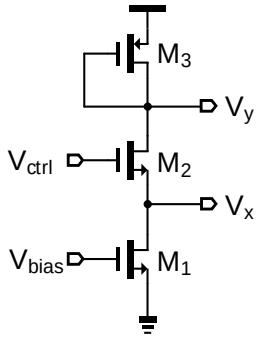


Figure 4. 5 Combination of concave and convex functions

4.2.2 Implementation of the Exponential Generator

Figure 4. 6 describes the schematic of the proposed negative exponential generator (NEG) and the size of each transistor. Composed of only three MOSFETs, it realizes a dB-linear characteristic between the differential control voltage ($V_{yx} = V_y - V_x$) and the single-ended control input voltage (V_{ctrl}).



W_1	0.8μm
W_2	2.8μm
W_3	0.96μm
$L_{1\text{-}3}$	1μm

Figure 4. 6 Schematic of the proposed NEG

First and foremost, it is instructive to explore the circuit qualitatively. The NEG is turned on when V_{ctrl} is increased slightly above the threshold voltage of M_2, and current starts to flow through all of the three transistors. Since V_{bias} is relatively high, V_x must be low to produce the same current in M_1 and M_2, leading to triode-region operation of the bias transistor (M_1) and saturation-region operation of the control transistor (M_2). We define this operating condition as "Region I", illustrated in Figure 4. 7 (a). As V_{ctrl} continues to be increased, the current through NEG increases, with V_x increased while V_y decreased. Once V_{ctrl} is raised high enough, M_1 enters saturation region, thereafter the branch current and thus V_y fixed in an ideal case. Given a much larger aspect ratio of M_2, it is forced to operate in the triode region to produce the same current as M_1. Such operating condition is defined as "Region II". If V_{ctrl} is kept increasing, the

drain-source voltage across M_2 has to decrease in order to compensate the increase in its gate-source voltage. In both Region I and II, the diode-connected transistor (M_3) remains in the saturation region.

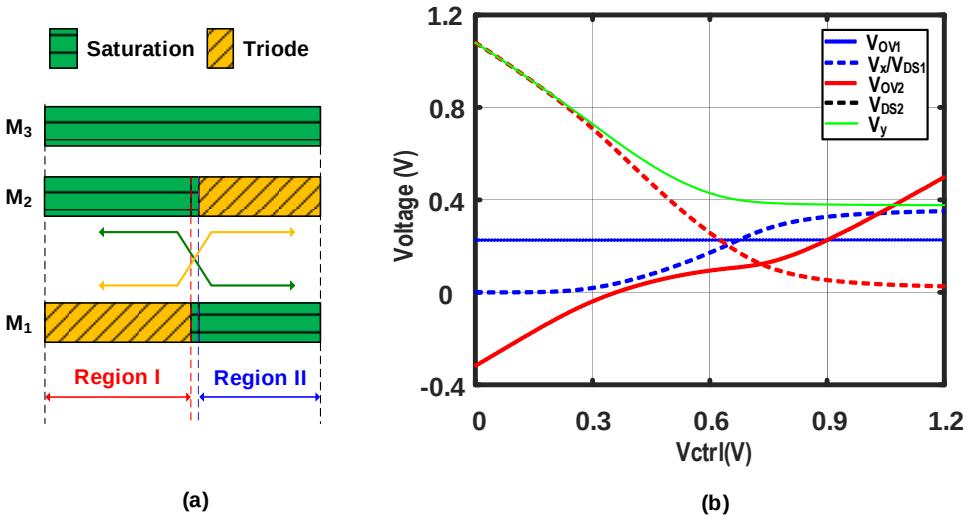


Figure 4. 7 Operating mechanism of the proposed NEG

As a result, the difference between V_y and V_x reduces monotonically while V_{ctrl} increases, as shown in Figure 4. 7 (b). With proper sizing and biasing, it can be proved that both of Region I and Region II approximate the ideal exponential line and together constitute an inverse S-shaped curve. Nevertheless, a transition between Region I and II may exist around the transition voltage (V_m), where both M_1 and M_2 are operated in the same region. In such a condition, the relationship between V_{yx} and V_{ctrl} is purely linear, instead of dB-linear. Thus, we should avoid the occurrence of additional regions, or narrow it.

Next, we start to derive the mathematical relation between V_{yx} and V_{ctrl}, based on the I-V characteristics of MOSFETs in different operating regions, for both regions I and II. Because the substrate and source of M_1 are both tight to ground,

its threshold is constant, and the traditional model matches well with the simulation result. The I-V equations of M_1 operating in the triode and saturation region are given by

$$I_{d1,I} = K_1\left[(V_{bias} - V_{th1}) \cdot V_x - \frac{1}{2}V_x^2\right] \tag{4.6}$$

$$I_{d1,II} = \frac{1}{2}K_1(V_{bias} - V_{th1})^2 \tag{4.7}$$

respectively, where $K_1 = \mu_n C_{ox} W_1/L_1$. μ_n is the charge-carrier effective mobility; C_{ox} is the gate oxide capacitance per unit area; W_1 and L_1 is the gate width and gate length respectively, and V_{th1} is the threshold voltage at $V_{SB} = 0$.

Differently, the source voltage of M_2 keeps changing with the control voltage, while its substrate is tight to ground all the time. The variant voltage across its source affects its threshold voltage, making the first-order I-V relationship deviated from simulation result. Therefore, the I-V equation is modified with several fitting parameters added in to achieve a better consistency between the calculated and simulated result. The following equations are found to match with its saturation and triode operations, respectively.

$$I_{d2,I} = \alpha_1 K_2\left(V_{ctrl} - V_x - V_{thf} + \beta_1 V_{th2}\right)^2 \tag{4.8}$$

$$I_{d2,II} = \alpha_2 K_2\left[\gamma\left(V_{ctrl} - V_x - V_{thf} + \beta_2 V_{th2}\right)\left(V_y - V_x\right) - \frac{1}{2}\left(V_y - V_x\right)^2\right] \tag{4.9}$$

where $K_2 = \mu_n C_{ox} W_2/L_2$, and $V_{thf} = V_{th2} + \eta V_x$ is the threshold voltage with substrate bias present. The body effect parameter (η) of 0.09 is extracted from the simulation. The corrected coefficients of saturation region, α_1 and β_1, are found to be 0.25 and 0.28. The corrected coefficients of linear region, α_2, β_2 and

γ, are found to be 0.77, 0.16 and 0.97, respectively. Based on the above equations, the current of M_1 and M_2 is calculated and compared with the simulation result across the entire working regions. The consistency is accpetable with an error of no more than 10%, as shown in Figure 4. 8.

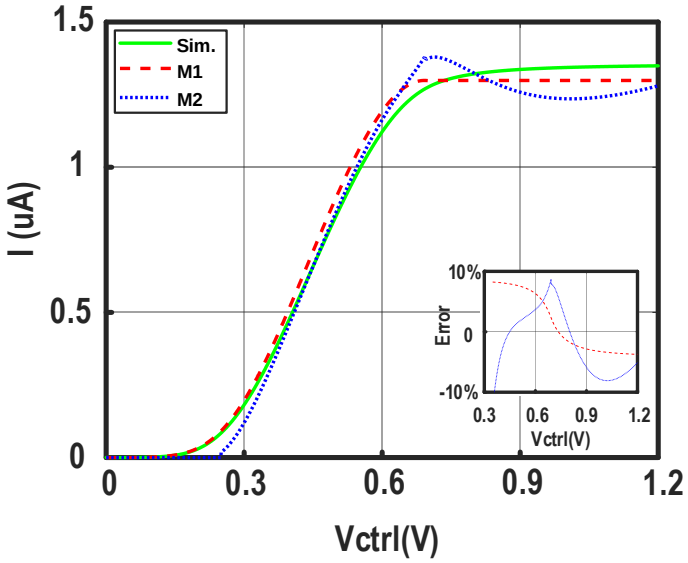


Figure 4. 8 Comparison between simulated and calculated current

Furthermore, it is obvious that no matter which operating regions M_1 and M_2 fall, M_3 is always working in the saturation with its current given by the conventional equation

$$I_{d3} = \frac{1}{2}K_3\left(V_{DD} - V_y - |V_{th3}|\right)^2 \tag{4.10}$$

and the current relationship $I_{d1} = I_{d2} = I_3$ always holds. We will use these equations to find how the output voltage change with the control voltage.

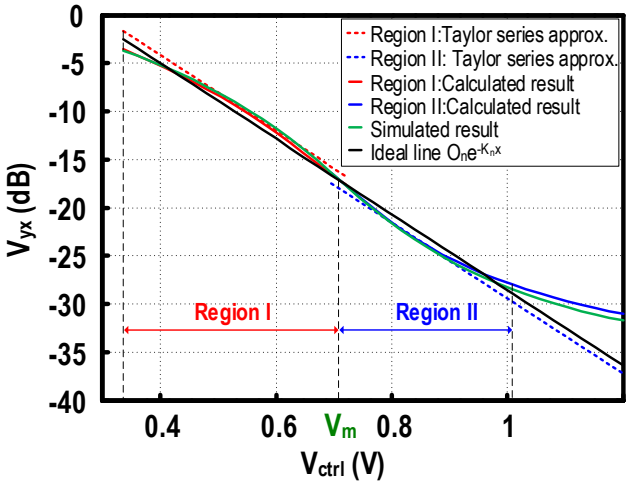
Suppose M_1 and M_2 works in the triode and saturation region respectively. With equation (4.6), (4.8), (4.10) and the above current equation, we obtain

$$V_{yx,I} = a_1 + b_1 x_1 + c_1\sqrt{d_1 + e_1 x_1 + f_1 x_1^2} \tag{4.11}$$

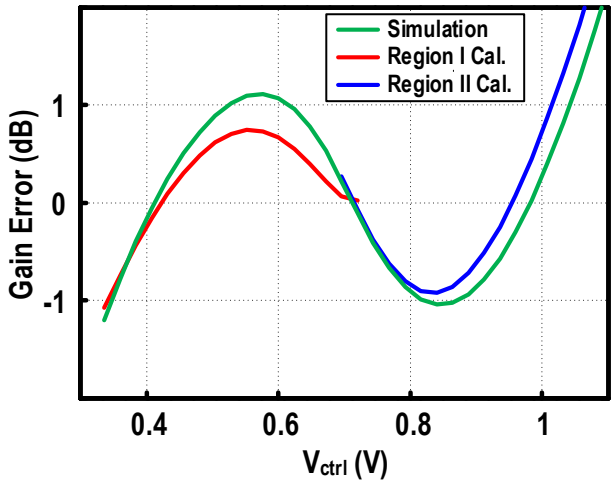
The coefficients and x_1 of (4.11) are derived as

$$\begin{cases} a_1 = V_{DD} - |V_{th3}| + \dfrac{\left(m\sqrt{K_2'/K_3} - 1\right)(V_{bias} - V_{th1})}{1 + m^2\left(K_2'/K_1\right)} \\ \qquad - \dfrac{\sqrt{K_2'/K_3} + m\left(K_2'/K_1\right)}{1 + m^2\left(K_2'/K_1\right)} V_{01} \\ b_1 = -\dfrac{\sqrt{K_2'/K_3} + m\left(K_2'/K_1\right)}{1 + m^2\left(K_2'/K_1\right)} \\ c_1 = -\dfrac{m\sqrt{K_2'/K_3} - 1}{1 + m^2\left(K_2'/K_1\right)} \\ d_1 = (V_{bias} - V_{th1})^2 + 2m\left(K_2'/K_1\right)(V_{bias} - V_{th1})V_{01} \\ \qquad - \left(K_2'/K_1\right)V_{01}^2 \\ e_1 = 2m\left(K_2'/K_1\right)(V_{bias} - V_{th1}) - 2\left(K_2'/K_1\right)V_{01} \\ f_1 = -K_2'/K_1 \\ x_1 = V_{ctrl} - (1 - \beta_1)V_{th2} - V_{01} \end{cases} \tag{4.12}$$

where $K_2' = \alpha_1 K_2$ and $m = 1 + k = 1.09$. V_{01} is a purely-mathematical coefficient for shifting the single point where the Taylor series is conducted in Region I. The calculated value of (4.11) and its corresponding gain error in Region I are plotted in Figure 4. 9 (a) and (b). At $V_{ctrl} = 0.59$ ($x_1 = 0$), (4.11) is expanded to approximate $O_1 e^{-K_1 x_1}$ by the second-order Taylor series, as shown in the dotted line.



(a)



(b)

Figure 4. 9 (a) Simulated and calculated V_{yx} curves versus $V_{ctrl.}$ (b) Simulated and calculated gain errors versus V_{ctrl}.

Similarly, if M_1 works in the saturation region while M_2 works in the triode region, with equation (4.7), (4.9), (4.10), obtaining

$$V_{yx,II} = a_2 + b_2 x_2 + c_2 \sqrt{d_2 + e_2 x_2 + f_2 x_2^2} \qquad (4.13)$$

where

$$\begin{cases} a_2 = -\dfrac{\beta_2}{2\beta_2(k+1)-1}\left[V_{02} - (1-\gamma)V_{th2} - (k+1)V_y\right] \\ b_2 = -\dfrac{\beta_2}{2\beta_2(k+1)-1} \\ c_2 = 1 \\ d_2 = \dfrac{2I_{d1}}{\alpha_2 K_2[2\beta_2(k+1)-1]} \\ \quad + \left(\dfrac{\beta_2}{2\beta_2(k+1)-1}\left[V_{02} - (1-\gamma)V_{th2} - (k+1)V_y\right]\right)^2 \\ e_2 = \dfrac{2\beta_2^2}{[2\beta_2(k+1)-1]^2}\left[V_{02} - (1-\gamma)V_{th2} - (k+1)V_y\right] \\ f_2 = \dfrac{\beta_2^2}{[2\beta_2(k+1)-1]^2} \\ x_2 = V_{ctrl} - V_{02} \end{cases} \tag{4.14}$$

where V_{02} is a purely-mathematical coefficient for shifting the single point where the Taylor series is conducted in Region II. Again, as shown in Figure 4. 9 (a) and (b), the calculated $V_{yx,II}$ and gain error in Region II, together with the calculated results in Region I, match with the simulated inverse S-shaped curve. By using the second-order Taylor series, equation (4.13) is expanded to approximate $O_2 e^{-K_2 x_2}$ at $V_{ctrl} = 0.85$ $(x_2 = 0)$. The simulated inverse S-shaped curve, which is the composite of dual Taylor series, approximates the ideal exponential line and the gain error is <±1 dB, as plotted in Figure 4. 9 with the green curve.

So far, we have approved that the output voltage changes exponentially with a linear control voltage if M_1 and M_2 work in different operating regions. So how can we minimize or even eliminate the transition region where both of them work in the saturation or triode region? Assuming M_1 switches from triode region to saturation at a control voltage V_{ctrl1}, while M_2 switches from saturation region to triode at another control voltage V_{ctrl2}, at the point of switching, we have

$$V_{DS1} = V_{GS1} - V_{TH1} \Rightarrow V_X = V_{bias} - V_{TH1} \tag{4.15}$$

$$V_{DS2} = V_{GS2} - V_{TH2} \Rightarrow V_Y = V_{ctrl2} - V_{TH2} \tag{4.16}$$

where V_{DSx}, V_{GSx} and V_{THx} are the drain-source voltage, gate-source voltage and threshold voltage of transistors, respectively. Figure 4. 10 introduces the optimization procedure to shrink the gap in beween.

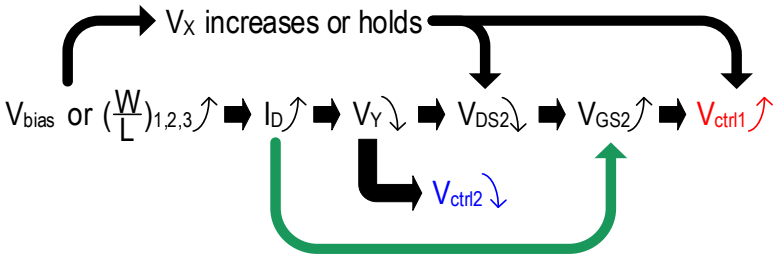


Figure 4. 10 Optimization procedure to eliminate transition regions

The current flowing through the NEG increases with an increaseing V_{bias}, leading to a decrease in V_Y. According to (4.15), V_{ctrl2} shall have a lower value, which means M_2 starts triode operation earlier. On the other hand, V_X is also increased with V_{bias} given by (4.16), together with the decrease in V_Y, resulting in a drop of the drain-source voltage across M_2. The gate-source voltage of M_2, therefore, must be larger to produce the increased current, indicating an increase of V_{ctrl1}. Consequently, both of the transistors have a wider triode-region operating, as illustrated in Figure 4. 11(a). A new region, namely "Region III", may occur where both of the transistors work in the triode region. Vice versa, if the bias voltage is decreased, saturation-region operating of M_1 and M_2 are extended, as shown in Figure 4. 11(b). The saturation region of M_1 may overlap with the same region of M_2.

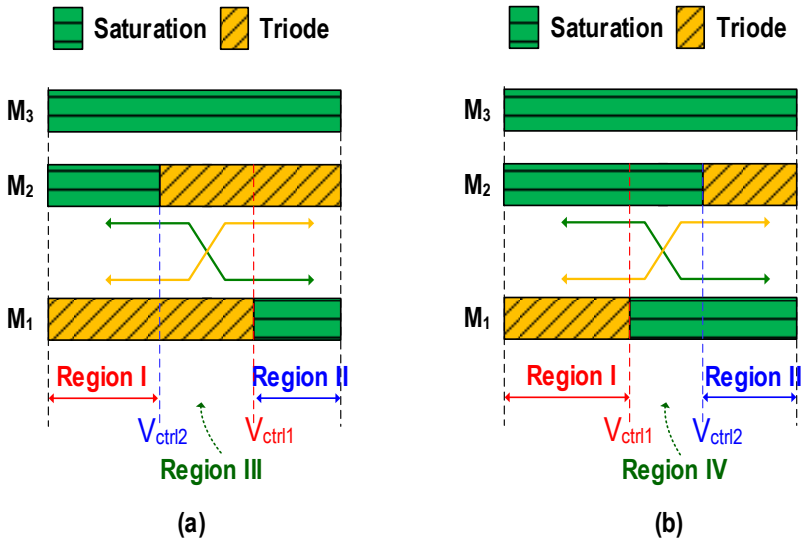


Figure 4. 11 Operating conditions when both transistors working in (a) triode region and (b) saturation region

Increasing or decreasing the aspect ratio of transistors has the same effect as altering the bias voltage in a similar manner, since it leads to an increase or decrease of the current flowing through the single-branch in NEG, respectively.

To compare fairly with the prior exponential approximations in Table I, two equations (4.11) and (4.13) are normalized to (4.5). The two groups of the coefficients (A_1 to F_1) and (A_2 to F_2) in $G_1(x)$ and $G_2(x)$ are listed in Table III.

Table III Parameters of Two Sets of Functions

Coefficient	$G_1(x)$	$G_2(x)$
A_n	1.8	-1.95
B_n	-1.15	-2.74
C_n	-1	1
D_n	0.64	8.73
E_n	-0.22	10.2
F_n	-0.37	7.6

The additional advantage that the inverse S-shaped curve brought is the flexibility to choose between a smaller gain error and a wider gain range. As illustrated in Figure 4. 12, given different requirements of gain errors, the slope of the ideal line varies, and the same goes with K_1 and K_2. If a more precise approximation is desired, the slope of these lines must be steeper while each approximation region is closer to the center. For instance, if the gain error is desired to be reduced from 1 dB to 5.5%, the ideal line is rotated clockwise with its slope changed from K_{1dB} to K_{5p5}. The dual Taylor series approximation lines, therefore, must be altered accordingly (from blue to red as illustrated in Figure 4. 12), leading to a narrower deviation from the one-piece ideal line, as well as a reduction of maximum gain error from GE_{1dB} to GE_{5p5}. To achieve this movement, $x_1(V_{01})$ and $x_2(V_{02})$, at which points the Taylor series is expanded for each region, need to be moved towards the center, indicated by the arrow in Figure 4. 12.

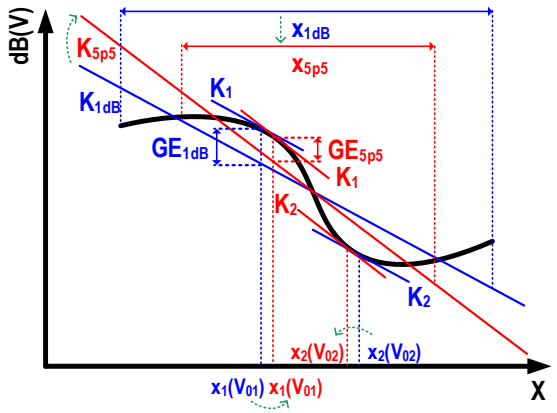


Figure 4. 12 Trade-off between gain range and gain error

To get the x ranges with different gain errors, the shifting and scaling behaviors of $G_1(x)$ and $G_2(x)$ observed in Figure 4. 5 are repeated. If we preset

the gain error ≤5.5%, the horizontal shift and vertical scale values ($\Delta X_1, \Delta Y_1$) and ($\Delta X_2, \Delta Y_2$) is calculated to be (0.42, 4.117) and (0.44, 4.328), respectively. An overall x range of 2.27 (from -1.15 to 1.12) is achieved. If a gain error 1 dB is desired, the movement values can be derived as ($\Delta X_1, \Delta Y_1$) = (0.72, 7.257) and ($\Delta X_2, \Delta Y_2$) = (0.67, 6.807), therefore yielding an x range of 3.53 (from -1.85 to 1.67). Compared with the approximation functions in Table I, the available x range and dB-linear gain range are extended effectively due to the combination of the concave and convex functions.

Further to NEG, it is also possible to design a positive exponential generator (PEG) with the same principle. The bias transistor and control transistor are replaced by PMOS while the load transistor is changed to NMOS, as shown in Figure x(a). As a result, current flowing through the PEG decreases with an increased V_{ctrl}, and voltage across the drain to source of M_2 increases. With proper sizing and biasing, the difference of V_y and V_x presents an exponential growth, realizing a positive dB-linear characteristic.

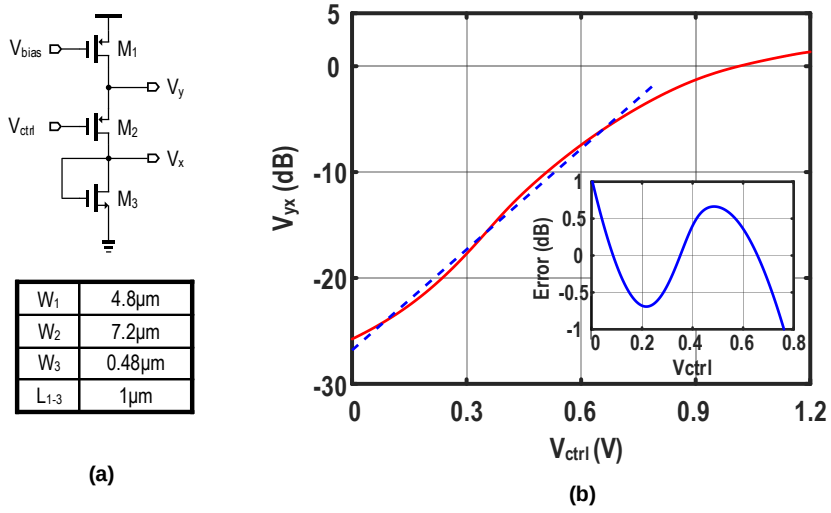


Figure 4. 13 (a) Schematic of the positive exponential generator. (b) Simulated output (V_{yx}) versus V_{ctrl}

4.3 Design of Wideband VGA

4.3.1 Reliability of the Proposed NEG

The analysis in the last section elaborates how to minimize the gap between Region I and Region II, which helps to achieve a wider gain variation range with a smaller gain error. However, it also exposed another issue that the proposed NEG is susceptible to PVT variations. To solve this problem, an adaptive bias circuit is designed to provide the bias transistor a proper voltage under various conditions. The circuit, shown in Figure 4. 14, consists of a constant-g_m biasing circuit and an additional branch to offset the temperature effect to NEG.

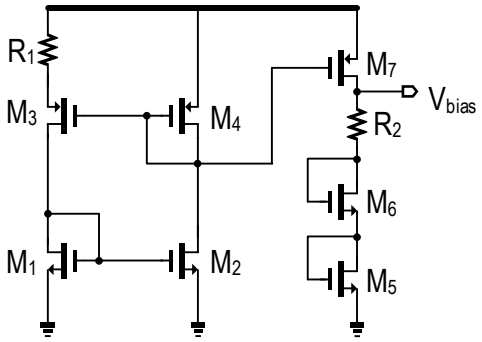


Figure 4. 14 Biasing circuit of the NEG

In consequence, the inverse S-shaped curve and the exponential feature of the NEG is well maintained under different conditions. Figure 4. 15(a) and (b) plot the simulated dB-linear performance and dB-linear gain error of the NEG, respectively, under typical condition and worst-case scenarios. A shift of the characteristic curve is observed, but a consistent 20 dB voltage variation, which is from -5.5 to -25.5 dB, is achievable with the worst gain error kept around 1 dB.

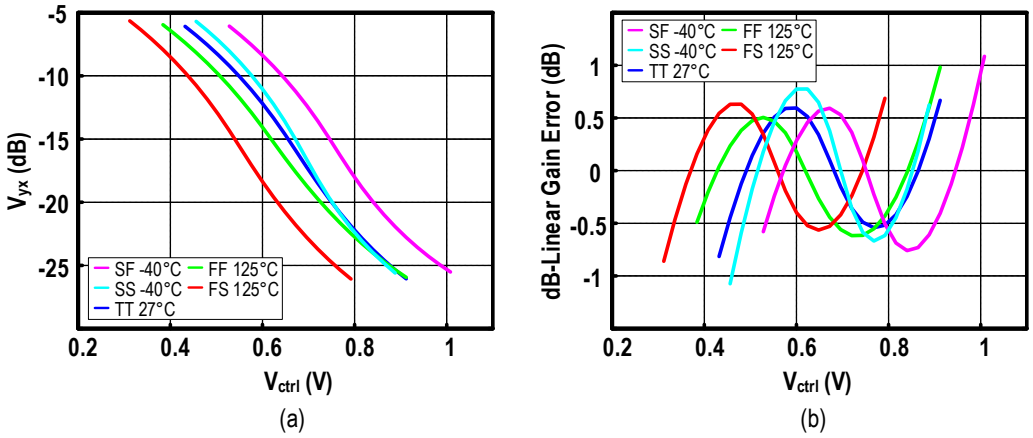


Figure 4. 15 Corner and temperature effects on the NEG

4.3.2 Variable Gain Cell

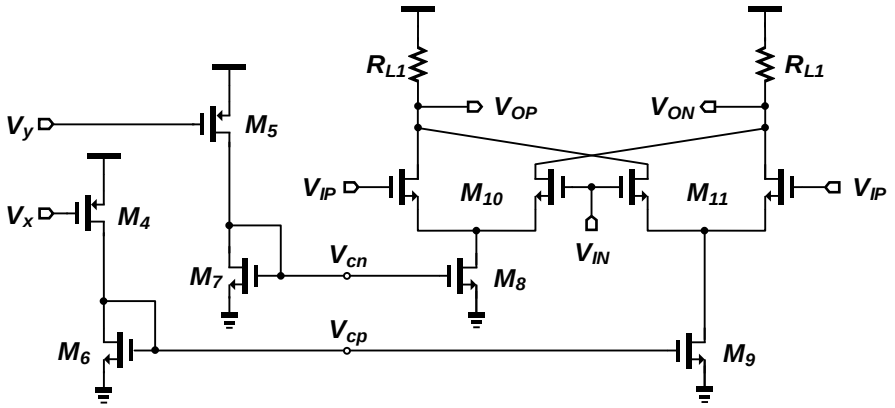


Figure 4. 16 Schematic of the proposed pseudo-folded Gilbert cell

Figure 4. 16 depicts the schematic of variable gain cell which is connected to the NEG. A pseudo-folded Gilbert cell is introduced to further reduce the number of devices. Two single branches (M_4-M_7) work as level shifters, transferring the exponential relationship from V_{yx} to ($V_{cpn} = V_{cp} - V_{cn}$), as shown in Figure 4. 17, and then controlling the gain cell. As signal path is directly injected to the gilbert amplifier, PMOS is only implemented in the part of DC control and biasing circuit, while the core amplifier is fully realized by NMOS and resistors. Because

all transistors work in the saturation region, we have

$$V_{cp,cn} = \sqrt{2I_{6,7}/K_{6,7}} + V_{th6,7} \tag{4.17}$$

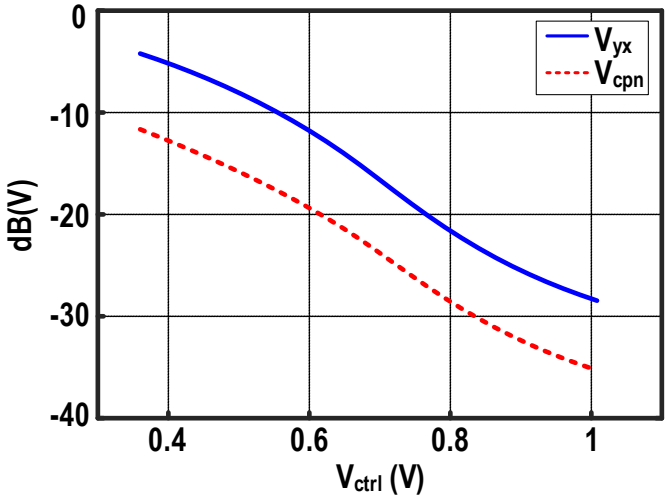


Figure 4. 17 Transfer of dB-linear control voltages

where

$$I_{6,7} = I_{4,5} = \frac{1}{2}K_{4,5}\left(\left|V_{x,y} - VDD\right| - \left|V_{th4,5}\right|\right)^2 \tag{4.18}$$

Since the two branches are identical to each other, it becomes

$$V_{cpn} = \sqrt{K_{4,5}/K_{6,7}}V_{yx} \tag{4.19}$$

If converted to the logarithm domain, i.e.

$$V_{cpn,dB} = 20\,log\sqrt{K_{4,5}/K_{6,7}} + V_{yx,dB} \tag{4.20}$$

which indicates that $V_{cpn,dB}$ persists a constant difference from $V_{yx,dB}$ and varies linearly with respect to V_{ctrl} in dB scale, as shown in Figure 4. 17.

The gain of the VGA cell is given by

$$A_v = -(g_{m10} - g_{m11})R_L \tag{4.21}$$

where

$$g_{m10,11} = \sqrt{\frac{1}{2}K_{10,11}K_{8,9}\left(V_{cn,cp} - V_{th8,9}\right)} \tag{4.22}$$

Therefore,

$$A_v = \sqrt{\frac{1}{2}K_{10,11}K_{8,9}R_L V_{cpn}} \tag{4.23}$$

The above equation proves a linear transfer between the voltage difference in the current tails and the differential gain of the VGA. From equations (4.19) and (4.23), it is obvious that the gain of the amplifier varies linearly with V_{yx}. Given that V_{yx} changes exponentially, the gain of the amplifier follows the same equation. Moreover, since small changes are observed in the total current of M_8 and M_9, pseudo-folded Gilbert cell which has no current tail is employed. The power supply thus can be low and the impact on the output common-mode voltage is negligible. By cascading two identical gain cells (M_8-M_{11} and R_{L1}) with the same bias (V_{cp} and V_{cn}), a doubled gain variation range of more than 40 dB could be achieved. The frequency response of the cascaded gain cell with different control voltages is plotted in Figure 4. 18, presenting a dB-linear gain range from -40 to 4.5 dB with a consistent -3 dB cut-off frequency of 10GHz.

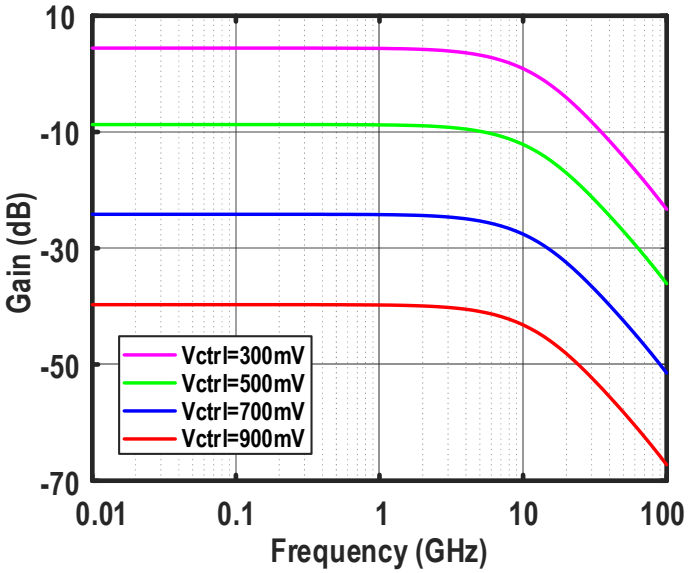


Figure 4. 18 Frequency response of the variable gain amplifier under different gain settings

To evaluate the robustness of the variable gain cell, the corner simulation similar to that of NEG is conducted again, with the results shown in Figure 4. 19. Different from a simple shifting effect for NEG, the gain characteristic curve also undergoes a slope change. However, a dB-linear gain range of 40 dB is still achievable under all operating conditions, with a maximum gain error around 1.6 dB. It is worth to note that the inverse S-shape of the gain curves under different scenarios are well maintained, half of which are convex while the other half are concave. This can also be proven from the gain error curves, where three intercept points exist between each simulation line and its corresponding idea line, indicating the homogeneous effect on both Region I and Region II.

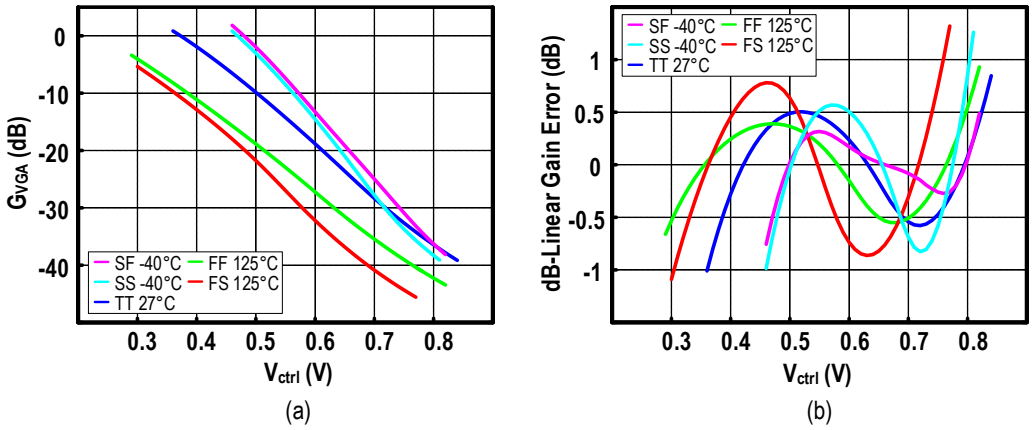


Figure 4. 19 Corner and temperature effects on the variable gain amplifier

Monte Carlo simulation is conducted to further verity the effect of process variation and mismatch. Figure 4. 20(a) and (b) present the gain curves and maximum dB-linear gain error distribution for 100 Monte-Carlo simulations, respectively. The standard deviation of the gain curves is found to be 1.55, while the mean value of the maximum dB-linear gain error is 0.97 with a standard deviation of 0.35.

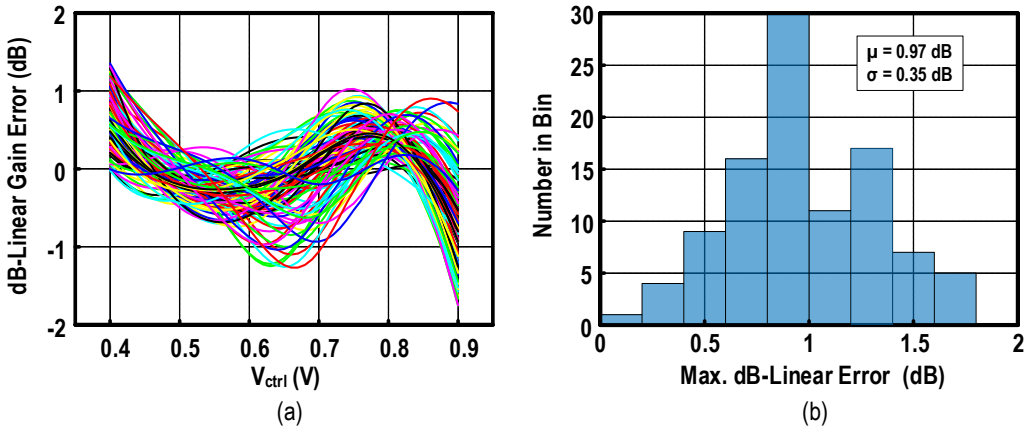


Figure 4. 20 Monte-Carlo simulation results versus V_{ctrl}: (a) gain error of V_{VGA} and (b) maximum dB-linear error histogram (100 Monte-Carlo simulation results)

4.4 Post Amplifiers

Since the variable gain stage cannot provide an adequate gain without degrading its bandwidth, post amplifiers are cascaded to raise the total gain by a fixed value independent of gain settings. The post amplifier consists of eight identical cells as a compromise among gain, bandwidth and power consumption.

4.4.1 Cell Design of Post Amplifier

The schematic of each cell is shown in Figure 4. 21, adopting the capacitive and resistive degeneration, where the capacitor is realized by two transistors in concern of layout symmetry. The equivalent transconductance can be expressed as

$$G_m = \frac{g_m}{1 + g_m\left(\frac{R_S}{2} \| \frac{1}{C_S s}\right)}$$

$$= \frac{g_m(R_S C_S s + 1)}{R_S C_S s + 1 + g_m R_S/2} \tag{4.24}$$

which indicates that a zero at $1/R_S C_S$ and a pole at $(1 + g_m R_S/2)/R_S C_S$ are brought in. Therefore, if the zero created by the transconductance coincident with the dominant pole of the amplifier, i.e. $1/R_D C_L$, where C_L is the cumulated capacitance at the output node, the bandwidth of the overall amplifier is extended to $(1 + g_m R_S/2)/R_S C_S$. That is to say the upper cut-off frequency is increased by a factor of $(1 + g_m R_S/2)$. Meanwhile, a reduction in the gain at low frequencies is observed due to the source degeneration resistor, with the same factor of $(1 + g_m R_S/2)$. With the same effect on gain reduction as decreasing the load resistance, the input capacitance of a single cell is neutralized by the

degenerated capacitor, thereby making cascading multiple stages possible.

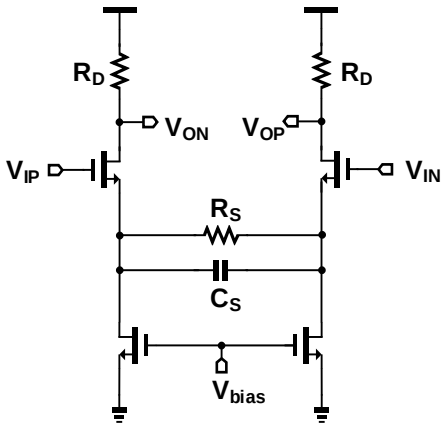


Figure 4. 21 Schematic of post amplifier cell

In summary, capacitive degeneration helps increasing the effective transconductance of the differential pair at high frequencies, to compensate the gain roll-off resulting from the pole at the output node, while the linearity of the amplifier is improved by the resistive degeneration [48].

In our design, one such stage consumes a power of 2.35 mW and provides a gain of 3.3 dB with a -3dB bandwidth around 25 GHz. If higher than 20 dB of gain is required, eight cells are required to be cascaded. However, the bandwidth will be highly affected, given by the equation [64]

$$BW_{tot} = BW_c \sqrt[m]{2^{1/n} - 1} \tag{4.25}$$

where m is equal to 2 for first-order cell cascading and n is number of cells. As a result, the bandwidth of the entire PA will fall below 8 GHz. The comparison between the frequency response of single cell and cascaded cells are shown in Figure 4. 22. After connected with the variable gain stage, the bandwidth will be degraded again, which is unfavorable to the application of 10 Gb/s communication. Therefore, advanced bandwidth extension technique must be

employed. For multistage design like ours, active feedback is a wise choice.

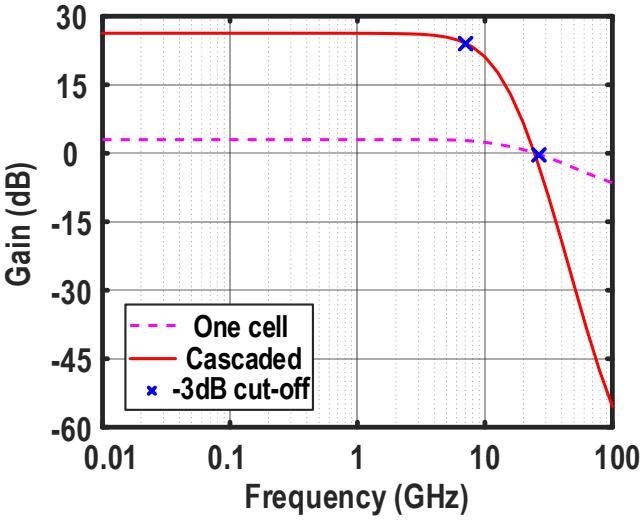


Figure 4. 22 Frequency response of one cell and cascaded amplifiers

4.4.2 Multistage Post Amplifier with Active Feedback

A cascade of gain stages can incorporate active feedback to achieve a broader bandwidth [64], [65], which also commonly used in many VGA designs[29], [33]. Figure 4. 23 depicts a basic second-order active feedback topology, consisting two feedforward transconductance stages and one feedback transconductor, where each G_m stage can be realized as a simple differential pair. The feedback circuit, $-G_{mF}$, senses the output voltage and returns a proportional current to node X.

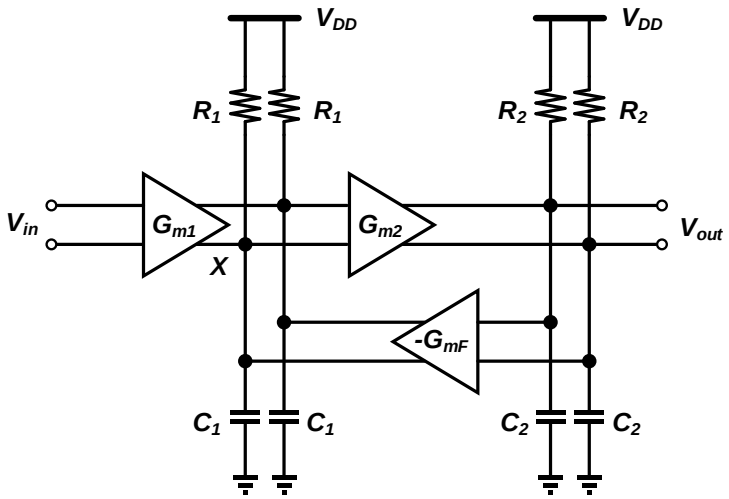


Figure 4. 23 Second-order active feedback topology

We can write [48],

$$G_{m2}\left[G_{m1}V_{in}R_1 - G_{mF}V_{out}\left(R_1||\frac{1}{C_1 s}\right)\right] = V_{out}\left(\frac{R_2C_2s+1}{R_2}\right) \quad (4.26)$$

It follows that [64]

$$\frac{V_{out}}{V_{in}}(s) = \frac{A_0\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (4.27)$$

where

$$A_0 = \frac{G_{m1}G_{m2}R_1R_2}{1 + G_{m2}G_{mF}R_1R_2} \quad (4.28)$$

$$\zeta = \frac{1}{2}\frac{R_1C_1 + R_2C_2}{\sqrt{R_1R_2C_1C_2(1 + G_{m2}G_{mF}R_1R_2)}} \quad (4.29)$$

$$\omega_n^2 = \frac{1 + G_{m2}G_{mF}R_1R_2}{R_1R_2C_1C_2} \quad (4.30)$$

For a maximally-flat Butterworth response, we choose $\zeta = \sqrt{2}/2$, obtaining a -3-dB bandwidth of $\omega_{-3dB} = \omega_n$. Hence,

$$A_0\omega_{-3dB}^2 = \frac{G_{m1}G_{m2}}{C_1C_2} \tag{4.31}$$

Since G_{m1}/C_1 and G_{m2}/C_2 are dominated by C_{GS} and on the order of $2\pi f_T$, we have

$$A_0\omega_{-3dB} = f_T\frac{f_T}{f_{-3dB}} \tag{4.32}$$

where $f_{-3dB} = \omega_{-3dB}/(2\pi)$. In other words, active feedback increases the gain-bandwidth product beyond the f_T of the technology by a factor equal to the ratio of f_T and the cell bandwidth.

Beside the basic second-order active feedback, multistage amplifier makes it possible to organize the feedback in many different ways. Thus, there are numbers of researches [65]-[70] done to improve the feedback topology aiming for wider bandwidth, lower peaking while sustainably high gain. [65] first invented the interleaved topology by adding in additional feedback cells among cascaded third-order active feedback stages. [33] then made use of it as a transimpedance load for the variable gain stage and accomplished the first 10G/s inductorless AGC amplifier. [66] and [67] utilize second-order active feedback and extra feedback stages in between, making it a fully interleaved architecture. In [68], Cherry-Hopper (CH) amplifiers are used as the feedforward amplifier while third-order interleaved feedback stages are inserted to interconnect the cascaded CH stages. Furthermore, [69] and [70] combines the second-order and third-order feedback together as the third-order nested feedback while still

adopting the interleaved topology.

Generally, when the feedback factor is increased, a upper -3dB cut-off can be expected, but in the meantime, it introduces high-frequency peaking and reduces low-frequency gain. In our design, the interleaved topology as [66] is adopted together with the capacitance degeneration cell. The feedback factor is chosen such that peaking is well controlled at high frequency range. The overall post amplifier consumes a power of 20mW and provides a gain of 23dB up to 10GHz.

4.5 DC Offset Cancellation

Due to the high gain provided by the post amplifier, DC offset cancellation circuit is necessary to guarantee that the DC difference between two differential nodes will not saturate the amplifier. It is possible to detect and compare the peak value of the differential signal. Any difference between them indicates a DC offset occurrence [71]. However, the speed of peak detectors is an issue for high-speed amplifiers, which will affect the accuracy of such architecture. Therefore, traditional method of high-pass response is widely used for tens of Gb/s applications, which employs a low-pass filter followed by a transconductance stage, as shown in Figure 4. 24. Then the low-frequency gain of the amplifier can be expressed as

$$A_{DCOC}(s) = \frac{1}{A_F}\left(\frac{1+\frac{s}{\omega_0}}{1+\frac{s}{A_F A_v \omega_0}}\right) \tag{4.33}$$

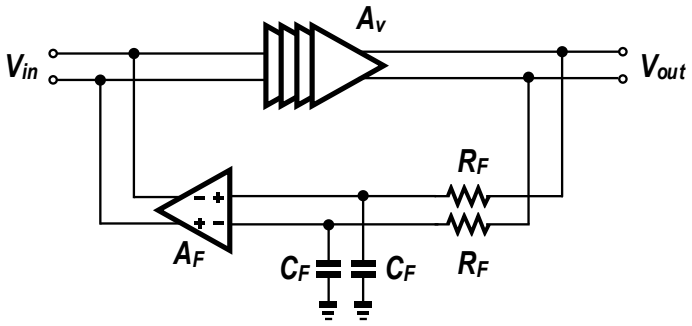


Figure 4. 24 DC offset cancellation circuit

where A_v is the feedforward gain, A_F is the feedback gain, and ω_0 is the cut-off frequency of the feedback network. Thus, the lower cut-off frequency is given by

$$f_c = \frac{A_F A_v + 1}{2\pi C_F R_F} \tag{4.34}$$

where C_F and R_F are the capacitor and resistor value used for passive first-order filter to extract the output DC level. It is obvious that the corner frequency is related to not only to the feedback gain and time constant but also the feedforward gain. Consequently, when the gain of the variable gain stage is adjusted, the high-pass corner will move accordingly. [72] focuses on designing a tunable DC offset cancellation network that tune the corner with gain setting, achieving a uniform lower cut-off frequency across the entire gain range. Considering our design, the variable gain stage only provides a maximum gain of less than 10 dB, while post amplifier is responsible for most of the gain. Therefore, the output of DCOC can be connected to the input of PA instead of involving the variable gain stage. Furthermore, recall that if the lower cut-off frequency of the amplifier is not as low as required, dc wander will manifest and destroy the quality of eye diagram. In order to support 2^7-1 PRBS pattern with 10 Gb/s, the lower -3dB cut-off frequency is designed below 150 kHz under any gain settings.

4.6 Complete AGC system

The system-level architecture of the AGC is presented in Figure 4. 25, including feedforward gain amplifiers, feedback control loop and DC offset cancellation network. VGA stage whose gain is controlled by a pre-distorted signal, $V_{ctrl,\,dB}$, from the exponential generation circuit is at the most front-end, providing a constant output level for the following stages. The signal is then amplified to a desired amplitude by the post amplifiers (PAs). Non-linearity and saturation must be avoided in order to fulfill the purpose of an AGC. Bandwidth is another design challenge since BW limitation brings inter-symbol interference (ISI) and the requirement for AGC is higher than LA for the same data rate due to saturation features of LA. A f_T doubler buffer [Figure 3. 21] for testing purpose is built at the end of AGC to drive the 50Ω input impedance of the testing equipment.

The feedback control loop senses the signal amplitude by a peak detector (PD), and compares its output, V_{PD}, with a predefined reference voltage, V_{REF}. The difference is then amplified and accumulated by the off-chip capacitor to generate the control voltage, V_{ctrl}, and be fed to the exponential generation circuit to complete the loop. The charging and discharging process of the capacitor will only stop itself when the output of peak detector is identical to the reference voltage, leading to a constant output power regardless of the incoming signal strength.

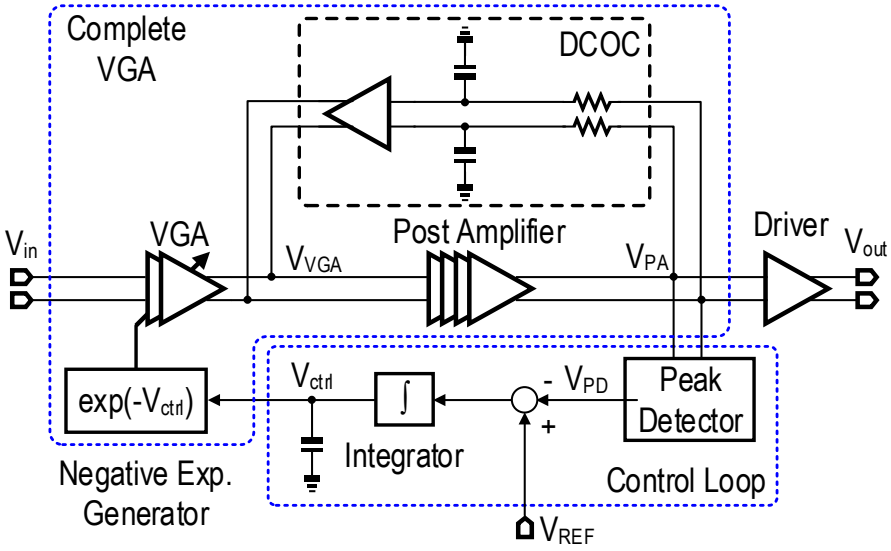


Figure 4. 25 Architecture of the complete AGC amplifier

4.6.1 Feedback Control Loop

To establish a feedback control voltage that forces the final output swing of VGA equal to a fixed reference, the output strength must be detected and monitored, thereby tuning the gain of variable gain stage accordingly. The output voltage of PD, V_{PD}, after smoothened by the low-pass filter, is compared with the external reference (V_{REF}), which is set according to the transfer characteristic of the peak detector. The difference is amplified by the error amplifier, leading to a charge or discharge of the capacitor. The capacitor accumulates the error until the output of PD is identical to the preset reference, and stores the correct voltage to control the VGA.

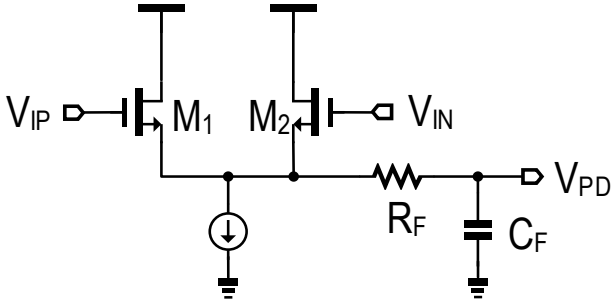


Figure 4. 26 Schematic of source-coupled peak detector

The conventional peak detector involving a source-coupled differential pair is adopted in our design, with the schematic shown in Figure 4. 26. The common source is the output of the PD, whose voltage is given by

$$V_s = V_{in,cm} - V_{th1,2} - \frac{1}{2}\left(\sqrt{\frac{I_s}{2K_{n1,2}}} + \sqrt{\frac{I_s}{2K_{n1,2}} - V_{in,pp}^2}\right) \qquad (4.35)$$

where $V_{in,cm}$ and $V_{in,pp}$ is the common-mode and peak-to-peak voltage of the input signal, respectively. $V_{th1,2}$ is the threshold voltage of M_1 and M_2, and $K_{n1,2} = \mu_n C_{ox}(W/L)_{1,2}/2$. I_s is the tail current of the input differential pair. As a result, the output changes almost linearly with the input. The characteristic of the PD is shown in Figure 4. 27. When the input swing is from 50 mV to 1.5 V, the corresponding output is from 445 to 710 mV.

Subsequently, the output voltage shall be compared with the reference voltage to obtain the difference. A linear transconductor, as shown in Figure 4. 28, is employed to provide such function. To avoid destroying the uniform settle time of the AGC, degenerative resistor R_S is added to enhance the linearity of the transconductor.

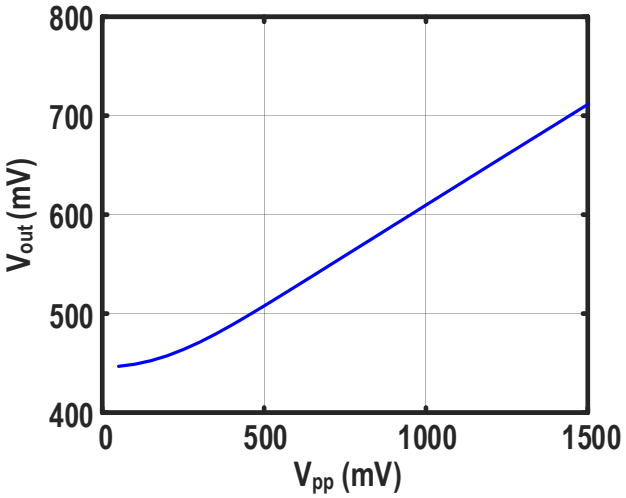


Figure 4. 27 Output voltage of PD versus input voltage amplitude

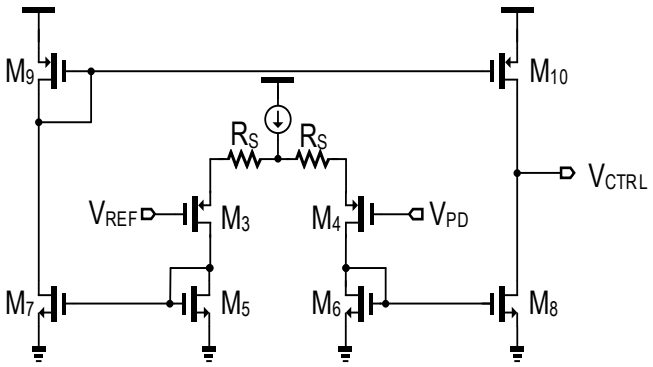


Figure 4. 28 Schematic of feedback transconductor

Moreover, a selector is placed between the control circuit and exponential generation block for testing purpose, such that the open-loop and closed-loop performance could be measured independently.

4.6.2 Dynamic Range of AGC

The dynamic range of the AGC is not only determined by the gain variation range, but also its linearity, noise figure, etc. When a desired output swing or V_{REF} is set, the smallest input signal is the level which can be amplified to the

desired level with the highest gain setting, or which has enough power to suppress the noise without resulting in a high BER, whichever is larger. The largest acceptable signal is the level that can be amplified or attenuated to the desired level with the lowest gain setting, or that starts to saturate the amplifier, whichever is smaller. The dynamic range may vary under different settings of swing reference, if the gain variation range is larger than the difference between its sensitivity and saturation. A largest dynamic range then exists when a reference is set at where maximum gain range of the amplifier can be utilized.

Figure 4. 29 depicts the input referred noise (IRN) of the amplifier. When the overall gain is equal to 30 dB at $V_{ctrl} = 250mV$, the IRN is found to be $4.26\text{nV}/\sqrt{\text{Hz}}$. As the control voltage increases, or say the gain decreases, IRN increases intensively. However, since low gain mode is only used for large input signal, it will not weaken the SNR thus the BER performance.

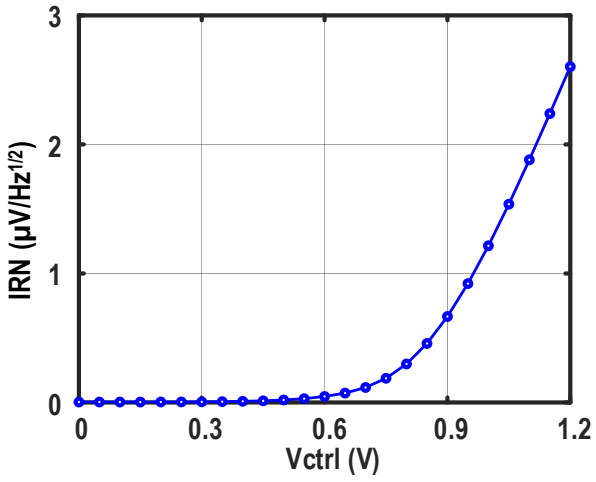


Figure 4. 29 Noise performance under different gain settings

The input and output saturation levels are found through linearity simulation with PRBS input in time domain. Under each gain setting, the input amplitude is

increased step by step while the output level is recorded and plotted as Figure 4. 30. It is found that saturation occurs at the output nodes when providing a high gain while input saturation emerges first for low gain. Therefore, by choosing a moderate level of reference voltage, around -6 dBm, a widest dynamic range can be achieved.

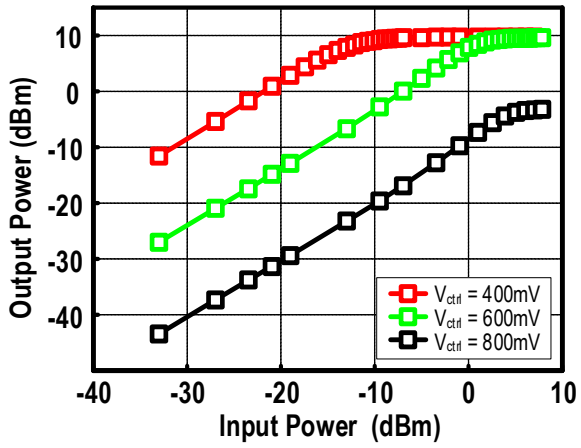


Figure 4. 30 Simulated compression behaviour of the AGC amplifier under different control voltages

4.7 Experimental Result

The complete AGC amplifier was fabricated in 65-nm CMOS. The die photograph (Figure 4. 31) shows a tiny active area of 0.045 mm^2 by avoiding any passive inductors.

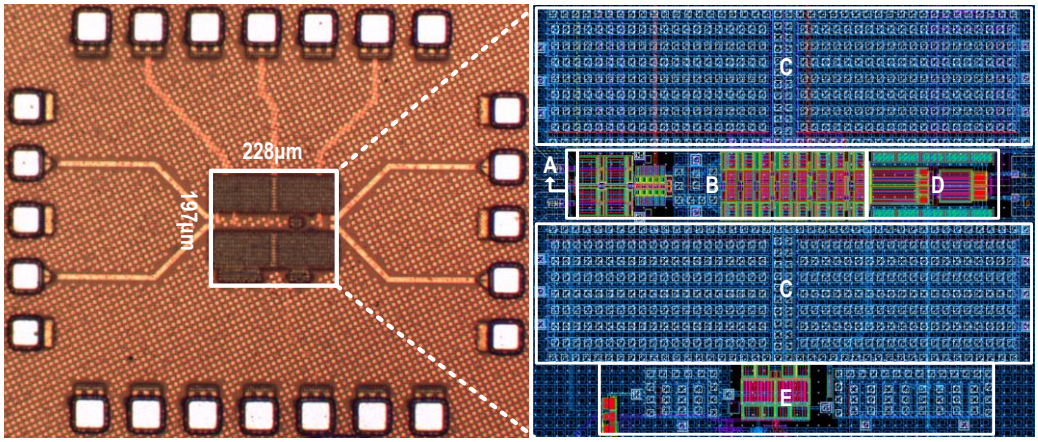


Figure 4. 31 Die photo of the fabricated AGC amplifier (left), and its zoomed-in layout (right)

The frequency response under various control voltages (Figure 4. 32) is measured by the Keysight Network Analyzer (N5247A), presenting a flat in-band gain and a constant 3-dB BW around 7 GHz. The total gain range is 57 dB, from -26 to 31 dB. Figure 4. 33 shows that the dB-linear range is 40 dB, with ±1 dB gain error when the control voltage V_{ctrl} is varied from 0.5 to 1 V. The measured gain error of the inverse S-shaped curve is consistent with that of the calculated and simulated results in Figure 4. 9.

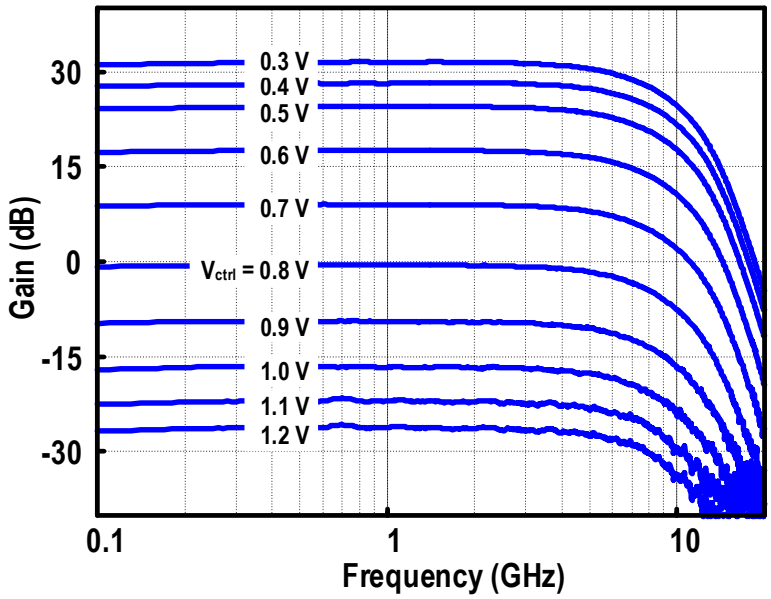


Figure 4. 32 Measured frequency response of the VGA

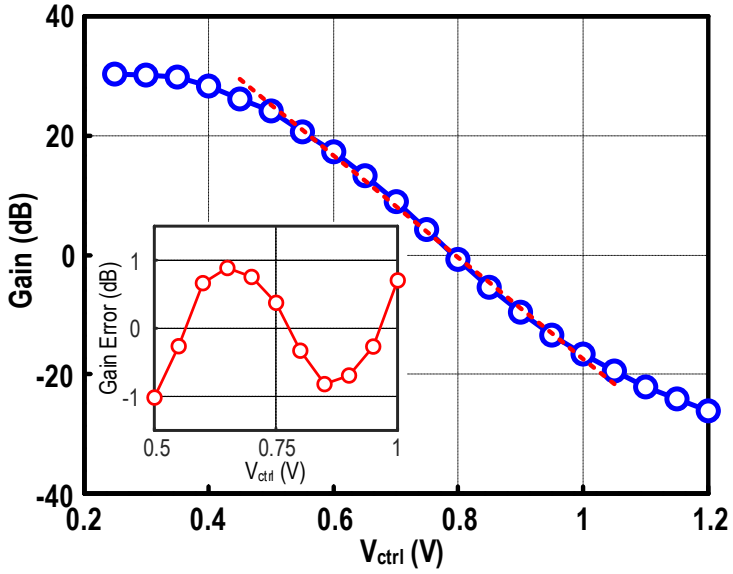


Figure 4. 33 Measured gain and dB-linear error versus control voltage at 300MHz

The time-domain AGC closed-loop measurement was conducted using the Agilent Pattern Generator (J-BERT N4903B) and the Keysight real-time Oscilloscope (DSO91304-A). The eye diagrams captured under different data

rates and various input amplitudes are shown in Table IV and Table V. Despite the variations in the input swing, a constant output is obtained under each data rate.

Table IV Eye Diagrams with Different Input Amplitude

Under 4 Gb/s and 6 Gb/s Data Rate

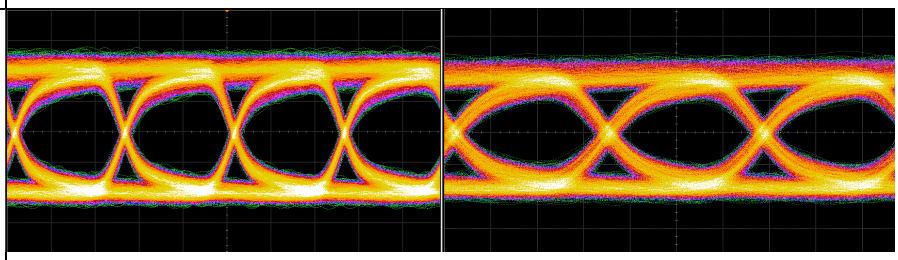
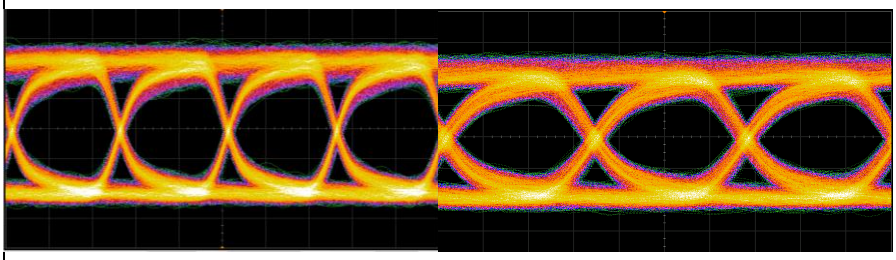
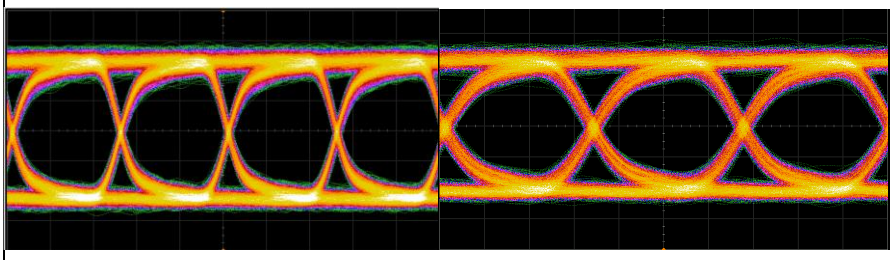
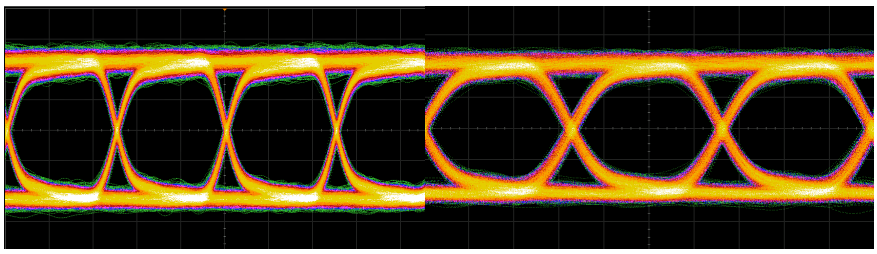
V_{pp}	*4Gb/s*	*6Gb/s*
10 mV		
100 mV		
500 mV		
1 V		

Table V Eye Diagrams with Different Input Amplitude

Under 8 Gb/s and 10 Gb/s Data Rate

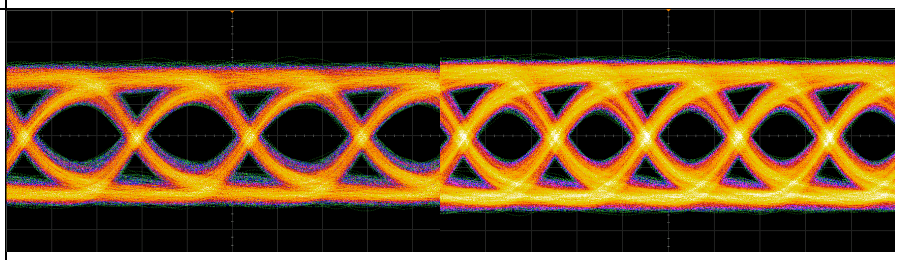
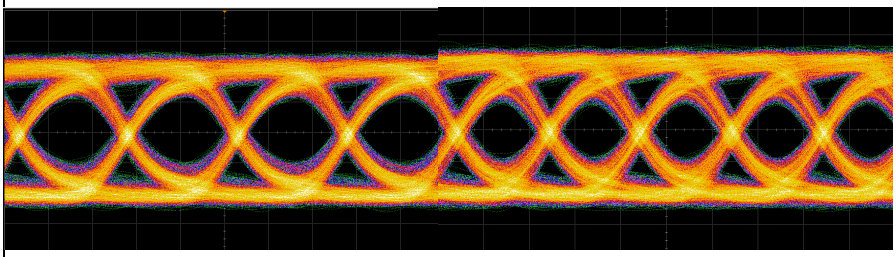
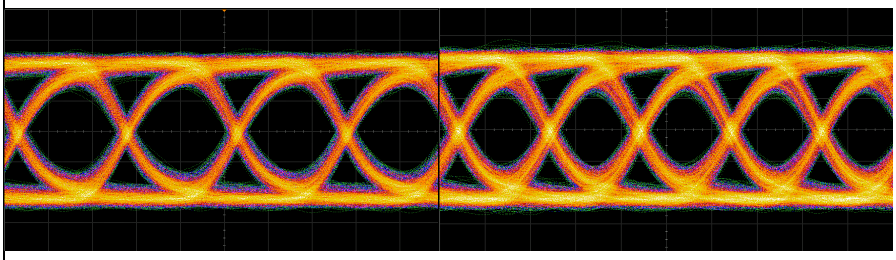
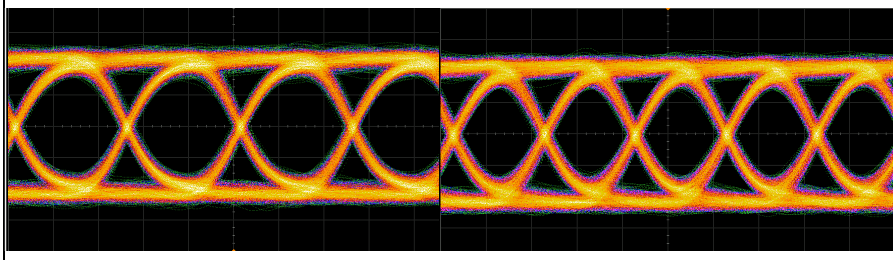
V_{pp}	*8Gb/s*	*10Gb/s*
10 mV		
100 mV		
500 mV		
1 V		

Table VI Eye Diagrams with Different Input Amplitude

Under 12 Gb/s Data Rate

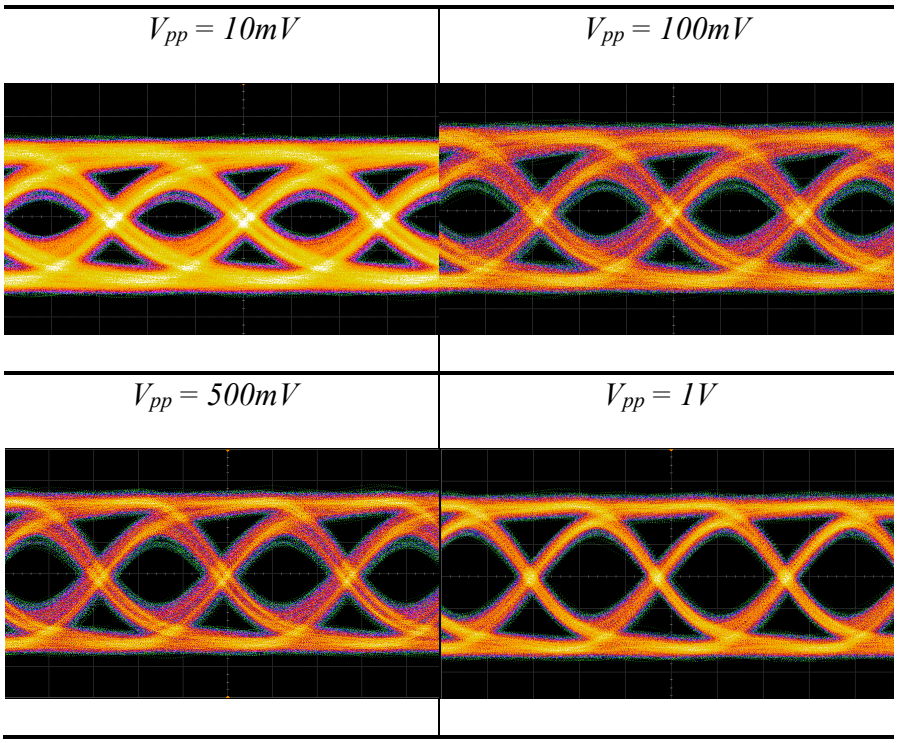


Figure 4. 34 plots the measured bit error rate (BER) for different input swings under a 10 Gb/s PRBS input of 2^7-1 pattern. When the output swing of the overall PA is set at 300 mV_{pp}, the minimum input sensitivity and the input overload swing at BER of 10^{-12} are 10 mV_{pp} and 1 V_{pp}, respectively. Thus, the input dynamic range is 40 dB at BER of $<10^{-12}$.

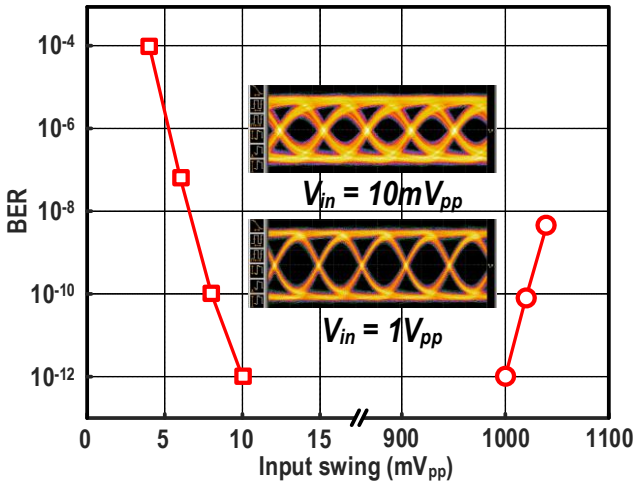


Figure 4. 34 Measured BER versus input swing under 10-Gb/s data rate

The measured peak-to-peak jitters are summarized in Figure 4. 35, where a less than 22.9 ps for 1 V_{pp} input swing, and a maximum of 37.1 ps for 10 mV_{pp} input swing are observed, respectively, covering the data rate from 4 to 12 Gb/s.

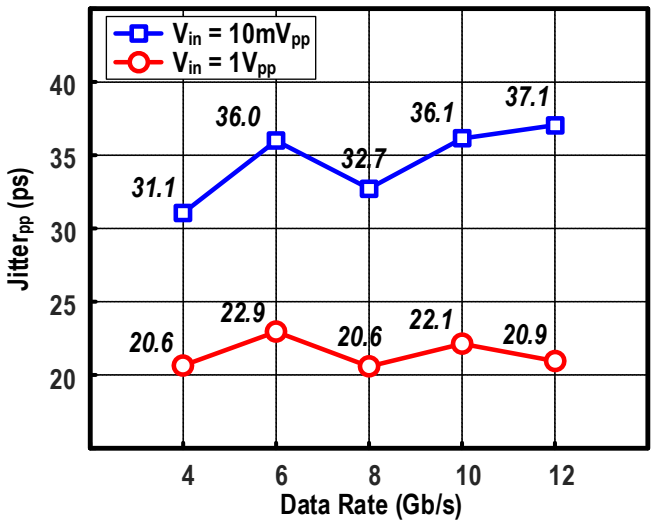


Figure 4. 35 Measured peak-to-peak jitter versus data rate

The entire AGC amplifier excluding the driver consumes a power of 28 mW at 1.2 V. Table VII shows the performance summary and benchmarks this work with the similar prior works. With the novel NEG, it achieves a wide gain range

of 57 dB, 40 dB of which is linear-in-dB, while power consumption and size are both superior to others.

Table VII Performance Summary and Benchmark with the State-of-the-Art

Parameters	This Work	JSSC'16 [33]	JSSC'12 [29]	ISSCC'06 [28]
Technology	65nm CMOS	130nm CMOS	130nm SiGe BiCMOS	180nm CMOS
Data rate (Gb/s)	10	10	5	10
Inductors	No	No	No	Yes
Jitter (ps)	< 36	< 44	< 40	< 25
PRBS	2^7-1	2^{31}-1	2^{15}-1	2^7-1
BW (GHz)	0.0001 to 7.0	0.0001 to 5.0	0.0002 to 7.5	N/A
In-band gain peaking (dB)	0	0	2	N/A
Exponential generator	**Negative (e^{-x})**	Positive (e^x)	Positive (e^x)	Positive (e^x)
	Dual Taylor Series	Rational Approximation	BJT	Parasitic BJT
	3 MTs	84 MTs	6 MTs + 2 BJT + 2 Rs	3 MTs + 2 BJT + 2 Rs
Gain range (dB)	57 (-26 to 31)	40 (-15 to 25)	40 (-10 to 30)	58 (-37 to 21)
dB-linear gain range / error	40 dB / ±1 dB	40 dB / ±1 dB	40 dB / ±0.3 dB	45 dB / ±1 dB
AGC dynamic range at BER<10^{-12}	**40**	24	40	35
Power (mW)	**28**	50	72	54
Energy efficiency	**2.8 pJ/bit**	5.0 pJ/bit	14.4 pJ/bit	5.4 pJ/bit
Active area (mm^2)	**0.045**	0.4	1	1.32

4.8 Summary

In this chapter, the design of VGA for wireline communication is presented, followed by a more complete structure of AGC. Further to the VGA for wireless communication, the requirement on bandwidth is even challenging for the application of 10 Gb/s link. Therefore, the topology which integrates the gain control block and core amplifier together is less favorable, since the signal path

will be affected by the gain control circuits. Consequently, a standalone gain control block is proposed, utilizing two pieces of approximation functions to achieve an extended dB-linear tuning range. With careful design of the subsequent gain stages, 57 dB gain range and 7 GHz bandwidth are achievable, provided the power consumption less than 30 mW.

CHAPTER 5

CONCLUSION AND FUTURE WORKS

5.1 Conclusion

The expanding growth of data transmission has urged the development of high-speed communications via both wireless and wireline channels. CMOS technology, as the most competitive integration process, attracts circuit designer of all areas to implement an integrated system on a single chip. Thus, although lack of intrinsic exponential feature in CMOS transistors, designing dB-linear VGAs or constant settling-time AGCs with CMOS technology is not trivial.

In this thesis, the state-of-the-art works are examined thoroughly, then summarized and compared in Chapter 2, from aspects of tuning scheme, topology of core block, and exponential realization method. Since some tuning schemes are only applicable to certain VGA architectures, bandwidth extension techniques are difficult to be integrated, limiting them to low-speed applications. The topology with standalone exponential generator allows the bandwidth of amplifier to be optimized independently, but it is still challenging to generate a wide while accurate exponential output with simple CMOS circuit. Therefore, our aim is to design wideband VGAs/AGCs for high-speed communications with minimum hardware, low power consumption and small chip area.

In Chapter 3, a novel approach to realize dB-linear VGA is proposed, where both the transconductance of the amplifier and the output resistance are tuned simultaneously. Different from conventional amplifiers, the input pair is biased in the triode region where its output resistance must be considered. When tuning the transconductance of the transistors, their output resistance changes in the same direction as well. Furthermore, active inductor is implemented to extend the cut-off frequency. As a result, the amplifier consumes a low power of only 3.5 mW, but achieves a gain variation range over 40 dB while providing a high-speed around 4 GHz. The measurement results show good consistencies with simulation results, validating that the design is suitable for WLAN and WPAN 60 GHz wireless communications.

In Chapter 4, a wideband AGC working up to 12 Gb/s is designed for wireline communications. Since the exponential realization method proposed in Chapter 3 imposes a limitation on the amplifier architecture, a standalone exponential generator is proposed, such that other broadband techniques can be exploited independently to attain an upper -3 dB cut-off frequency of 7 GHz. The exponential generator adopts an extremely simple topology with only three transistors, but offers a wide tuning range by taking full advantage of dynamic operating regions of the transistors. With the combination of convex and concave function as an inverse S-shaped curve, a gain range over 50 dB and a gain error within 1 dB are obtained. Other building blocks, including the post amplifiers, DC offset cancellation network and feedback control loop, are discussed subsequently. The complete AGC amplifier, fabricated with standard 65 nm CMOS technology, is measured in both open-loop and closed-loop modes,

showing a good performance result that is suitable for 10 Gb/s serial links, such as 10 Gb Ethernet.

5.2 Future Works

Although the circuit presented in this thesis demonstrates a competitive performance compared to the state-of-the-art works, a few improvements can be considered and implemented.

As in most of the amplifiers, the DC offset cancellation circuit occupies a large chip area due to the constraint of lower cut-off frequency. Either by AC coupling, as in Chapter 3, or by low frequency feedback, as in Chapter 4, passive capacitors are inevitable. Therefore, new method to alleviate DC offset must be sought. While one peak detector already exists in the AGC system, it is possible to add another identical block, such that the peak levels of the differential signal can be measured separately and compared to cancel the offset. However, a fast and accurate peak detector is required, which may aggravate the power consumption significantly.

Regarding to the AGC design in Chapter 4, it would be better if more internal nodes are accessible during testing, especially the control voltage when the loop is closed, which indicates how the loop is established. Moreover, we only use NRZ signal for time domain measurement due to the limitation of testing equipment. If PAM4 signal is available, the eye diagram should be further examined with PAM4 signal, thus to verify the linear amplification of the designed circuit.

Moreover, although process, voltage, temperature (PVT) variations and Monte

Carlo simulations are conducted for both designs, only the core circuits were involved in the experiment with external biasing. Therefore, it is suggested that biasing circuits shall be designed for each biasing point to fully completed the design and effect of PVT variations on the incorporated biasing should also be considered while studying the robustness of the proposed circuits.

In Chapter 4, it is proposed that to use two different functions to approximate the ideal exponential curve over different range. This idea could be expanded by increasing the number of approximation function used, such that piecewise approximation may be achieved across a considerably large region. The difficulty lies on not only how to successively approximate the exponential curve, but also developing the algorithm on switching circuit that chooses the corresponding control range.

Last but not least, for exponential approximation, gain error compensation can be realized with the help of convex and concave functions. As illustrated in Figure 5. 1, the convex function can be compensated by a concave function while an inverse S-shaped curve can be compensated by a S-shaped curve. It is not necessary that the two tuning schemes are realized in the same way, but they must vary in the same direction, either monotonic increasing or monotonic decreasing, across the same range of x. The two counterparts can be transconductance and load resistance, similar to the design in Chapter 3, two cascading stages, or two exponential generators controlling one variable gain cell. If this idea is realized, an extended gain variation range and a diminishing gain error would be acquired simultaneously.

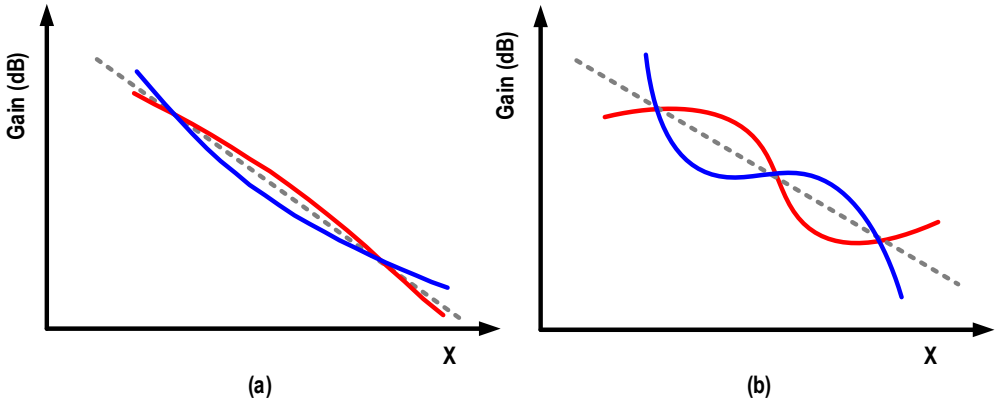


Figure 5. 1 Gain error compensation of (a) convex and concave curves and (b) S-shaped and inverse S-shaped curves

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