Study of Microstructures and Mechanical Properties of Lead-free Solder Joints

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Abstract

Reliability of solder joints is a most critical issue in electronic packaging. There is the urgent need to understand reliability of lead-free solder joints because lead-free solders are replacing the conventional tin-lead solders due to environmental concerns and legislation to ban use of lead in electronic products. In soldering process, formation of thin intermetallic compounds (IMC) due to reaction between the solder and substrate is essential to achieve a good metallurgical bond. However, excessive IMC growth in service could cause premature failure of the joint. Therefore, the primary objective of the project was to understand IMC growth in lead-free solder joints. Bulk solders were studied but special attention was paid to the solder-substrate interface. The project aimed to study 95.5Sn-3.8Ag-0.7Cu solder because it is a type of lead-free solder especially recommended by the National Electronic Manufacturing Initiative, but 99.3Sn-0.7Cu solder was also studied because the binary alloy contains single type of IMC and thus makes it easier to monitor the IMC growth quantitatively.

Various factors influencing IMC growth were studied, including temperature, time, stress and surface finishes of the substrate. Great effort was made to study effect of the factors on IMC growth separately in a controlled manner. For example, study of the bulk Sn-Ag-Cu solder either by varying temperature to 60, 125 and 190 °C at a fixed time of 1 hr or by change of heating time at a fixed temperature of 190 °C clearly reveals the effect of temperature and time on the IMC growth. Worth special note is that a new technique was adopted to monitor IMC growth in-situ. The technique made it possible to show quantitatively that initial growth of IMC in the Sn-Cu solder is linear with time. This is in contrast with the observation that the growth of IMC at the solder-substrate interface is proportional to square root of time, highlighting the fact that the mechanism for IMC growth in bulk solders is different from that in the presence of a substrate.

Extensive researches were carried out to study IMC growth in the Sn-Ag-Cu solder joints with either Cu or FR4 as substrate during various thermal loading conditions, including isothermal aging (125, 150 and 175 °C), thermal cycling (-40 to 125 °C) and thermal shock tests (-55 to 125 °C) up to 2000 cycles. Ripening of interface IMC was

found to be a common phenomenon. Cracking along the solder/coating interface was observed during the non-isothermal tests, and this is consistent with the finding of microtensile tests that isothermal aging embrittles the interface. The most noteworthy observation from this part of study is that given the same maximum heating temperature of 125 °C thermal shock results in considerably faster interface IMC growth than thermal cycling while isothermal aging produces negligible interface IMC growth. This observation together with other experimental evidence leads to the conclusion that stresses induced by the temperature change help to accelerate atomic diffusion and interface IMC growth.

No existing method is available to study the effect of stress on IMC growth in a controlled manner. Therefore, a novel C-ring technique was developed and shown to provide consistent and reliable results for the study on the effect of stress on interface IMC growth. When an in-plane tensile and compressive stress was applied to the Sn-Ag-Cu joint on Cu substrate with various surface finishes, the growth of IMC was generally faster in the interface subjected to compressive stress than that subjected to tensile stress. In addition, the IMC growth rate was found to increase with the magnitude of applied compressive stress. The observation further supports the conclusion that stress plays an important role in influencing the diffusion rate and IMC growth. Furthermore, the controlled study clarifies that it is compressive stress that promotes IMC growth. A possible explanation on the stress effect is offered in terms of the effect of compressive stress on promoting diffusion of Cu, Ni or Pd from the coating and substrate towards the IMC. The C-ring technique is also shown to be applicable to other studies, for example, to study of Sn whisker growth. In-plane compressive stress was found to promote Sn whisker growth. In contrast, exerting in-plane tensile stress on the Sn electrolytic coating surface retards the Sn whisker growth.

List of Abbreviations and Symbols

Abbreviations of Organizations

DTI	Department of Trade and Industry
EPA	Electronics Packaging Association
IPC	Institute for Interconnecting and Packaging Electronic Circuits
ITRI	International Tin Research
JEITA	Japan Electronics and Information Technology Industries Association
JIEP	Japan Institute of Electronics Packaging
METI	Ministry of Economy, Trade and Industry
MITI	Ministry of Trade and Industry
NCMS	National Center for Manufacturing Sciences
NEDO	New Energy and Industrial Technology
NEMI	National Electronics Manufacturing Initiative
NPL	National Physical Laboratory
OEM	Original Equipment Manufacturer
RoHS	Reduction of Hazardous Substrate
SOLDERTEC	Soldering Technology Centre
WEEE	Waste Electrical and Electronic Equipment
UK	United Kingdom

Abbreviations of Units of Measure and Other Terms

ASTM	American Society for Testing and Materials
ATC	Accelerated Thermal Cycling
BGA	Ball Grid Array
CTE	Coefficients of Thermal Expansion

°C	Degree Celsius
DSM	Direct Strain Measurement
EBSD	Electron Backscatter Diffraction
EDX	Energy Dispersive X-ray
ELFR	Early Life Failures Rate
ENEPIG	Electroless Nickel Electroless Palladium Immersion Au
ENIG	Electroless Nickel Immersion Au
EPMA	Electron Probe Micro Analysis
FE-SEM	Field Emission Scanning Electron Microscopy
FIB	Focus Ion Beam
FIT	Instantaneous Failure Rate
FR-4	Flame Resistant 4
hr	Hour
GPa	Giga Pascal
IC	Integrated Circuit
I/O	Input/Output
K	Kelvin
MCM	Multi Chip Modulus
MDS	Mechanical Deflection System
min	Minutes
mm	Millimeter
MPa	Mega Pascal
PCB	Printed Circuit Board
PCBA	Printed Circuit Board Assemblies
PTH	Pin Through Hole
PWB	Printed Wiring Circuit Board

QFP	Quad Flat Package
sec	Second
SEM	Scanning Electron Microscopy
SMT	Surface Mount Technology
TC	Thermal Cycling aging
TEM	Transmission Electron Microscopy
TPB	Three Point Bend
TS	Thermal Shock aging
Wt%	Weight percentage
XRD	X-Ray Diffraction
UBM	Under Bump Metallization
μm	Micrometer

Symbols

A	Area
B	Constant
C_r	Concentration of at the surface
C_o	Equilibrium concentration
C_i	Concentration for grain i
$\overline{C}$	Average concentration
D	Diffusion coefficient
D	Mean diameter
D_o	Outside diameter of C-ring before stressing
D_{of}	Outside diameter of stressed C-ring
E	Young's Modulus of C-ring

E_{cu}	Young's Modulus of commercial pure Cu
E_s	Young's Modulus of solder
E_{sn}	Young's Modulus of Tin
f	Applied stress level
f(t)	Failure density function
$\bar{h}$	Average thickness
L	Mean separation between grains
L_x	Length in projection x
Ln	Natural logarithm
m	Atomic mass
N_A	Avogadro's number
$N_p(t)$	Total number of grains
n	Number of sample
p	Constant
Q	Activation energy
Q_a	Apparent activation energy
R	Gas constant
R	Stress ratio
r	Grain radius
r	Equivalent radius
$\bar{r}$	Grain mean radius
r_i	Radius of grain i
T	Absolute temperature
T_h	Homologous temperature
T_m	Homologous meting temperature
t	Thickness

t	Time
x	Measurement in vertical direction
y	Measurement in horizontal direction
Z	A correlation factor for curved beams
α, β	Phase designations
α	Proportional constant
α_1	Linear Coefficient of thermal expansion for chip
α_2	Linear Coefficient of thermal expansion for solder joint
α_3	Linear Coefficient of thermal expansion for substrate
Δ	Change of diameter
σ_{cu}	Stress applied on Cu C-ring
σ_s	Yield stress of solder
σ_{ysn}	Yield stress of Tin
$\bar{\delta}$	Mean separation between grains
γ	Interface energy
ν	Consumption rate
ρ	Density
Ω	Molar volume
%	Percentage

Chapter 1: Introduction

1.1 Background

The implementation of lead-free solder manufacturing has become increasingly important in recent years due to legislations to ban lead (Pb) in electronic products in the near future. The National Electronic Manufacturing Initiative (NEMI) organization recommends 95.5Sn-3.9Ag-0.6Cu (±0.2%) as the lead-free alloy candidate to replace 63Sn-37Pb (Cannis and Syed, 2001, Bradley et al., 2002, Chung et al., 2002, NEMI, 2003). Following this announcement, a lot of research work on this family of lead-free alloy has been carried out (Tonapi et al., 2002, Amagai et al., 2004, Nurmi et al., 2004, Lu et al., 2005, Wable et al., 2005).

Several studies (Plumbridge et al., 2001, Wade et al., 2001, Kim et al., 2002, Mutoh et al., 2002) have reported that mechanical properties such as yield strength, tensile strength, creep-rupture and creep at elevated temperature of Sn-Ag-Cu lead-free solder are superior to 63Sn-37Pb solder. Electronic components are soldered to copper (Cu) pad or terminal and are often plated with various types of surface finishes. Ni-based metallization and Au coating are commonly used to give a diffusion barrier layer and oxidation protection layer. A thin intermetallic compound (IMC) layer will be formed between tin (Sn) in the molten solder and surface finish layer and base metal during the reflow process. The melting adhesion is realized through this metallurgical bond and interfaced reaction.

In service, solder joints in an electronic assembly often fail by cyclic thermal loading. The failure is caused by thermal mismatch deformation resulting from differences in coefficient of thermal expansion (CTE) of different electronic materials. The highest stress from CTE mainly occurs at the solder joint-matellization pad

interface that typically consists of brittle IMC layer. In addition, thermally activated diffusion in the solder material, metallization and IMC take place during thermal cycling (Zhang et al., 2001, Ma et al., 2002, Pang et al., 2002, Zeng and Tu, 2002).

Excessive growth of the IMC layer may deteriorate the solder joints reliability considerably. Therefore, many studies on understanding the metallizations with lead and lead-free solders under different reflow conditions have been carried out (Liu et al., 2000, Ho et al., 2001, Jung and Conrad, 2001a, Lin et al., 2001, Prakash and Sritharan, 2001, Zeng and Tu, 2002). In addition, many researches concerning the development or growth of IMC under various thermal loading conditions and accelerated tests have been reported (Vianco et al., 1997, Zribi et al., 1999, Kishimoto et al., 2001, Jung and Conrad, 2001b, Pang et al., 2001, Zeng et al., 2001).

Understanding thermal aging degradation of the solder joint-to-pad interfaces behaviour in electronic assemblies is a critical concern in solder joint reliability. Therefore, it is important to study the kinetics of IMC thickening process.

In this project, studies concerning the development or growth of IMCs at the interface between the Sn-Ag-Cu lead-free solder and various surface finishes under various thermal loading conditions including isothermal, thermal cycling (TC) and thermal shock (TS) tests were conducted. These tests encompass complex driving mechanisms on the IMC growth. They involve several factors such as temperature, exposure time and stress generated due to CTE mismatch between the assembly materials. Therefore, additional controlled experiments in isolating the effect of each of these factors were very much needed for a controlled study.

Effects of annealing temperature and time on the IMCs growth were studied by conducting the annealing and in-situ IMC growth observation on 95.5Sn-3.8Ag-0.7Cu 99.3Sn-0.7Cu bulk lead-free solders respectively. While for the effect of stress, a novel

technique employs a C-ring specimen was designed to study effect of different stress states on the IMC growth.

Other than the studies on IMC growth, the solder joints subjected to multiple reflow cycles and isothermally aged were used to study the in-situ tensile fracture mechanism of the solder joints.

1.2 Objectives

The primary objective of the project is to understand the effect of various thermal loading conditions on the formation of IMC of the solder joint. In an effort to better understand the IMC formation during these loading conditions that encompassed complicated mechanisms, the effects of heating temperature and time on the solder bar were evaluated separately. A novel technique which employs a specially designed C-ring solder joint specimen was used to carry out a study on the effect of different stress states (in-plane tensile and compressive stresses at different stress levels) on interface IMC growth. The metallization effects on the fracture mechanism of solder joint was studied through the in-situ micro-tensile test using the solder/copper joints that subjected to different process histories and heat treatments.

1.3 Scope

The scope of the project can be broadly divided into the following four areas:

(1) Study of effects of annealing temperature and time on the microstructures of 95.5Sn-3.8Ag-0.7Cu lead-free solder; and IMC growth in 99.3Sn-0.7Cu lead-free solder through a specially designed in-situ observation technique.

(2) Study of the IMC growth under various thermal loading conditions; solder/copper joint (formed by solder paste and Ni/Au coated Cu sheets) for

isothermal aging and; FR4-solder joint (formed by soldering a single solder ball to FR4 substrate with Cu pad coated with Ni/Au) for thermal cycling (TC) or thermal shock (TS) tests.

(3) Study of metallization effects on the fracture mechanism of solder joint through microtensile test using the solder/copper joint.

(4) Study of the effect of in-plane tensile and compressive stresses on the IMC growth at the interface between 95.8Sn-3.5Ag-0.7Cu and various surface finishes using specially designed C-ring solder joint. The novel C-ring technique was also used to study effect of stresses on Sn whisker growth, which is closely related to reliability of lead-free solder joints.

This report is divided into seven chapters. The first chapter covers the background, objectives and scope of the project. Chapter 2 reviews literature about the work on both lead-containing and lead-free solders. Chapter 3 describes the materials used and elaborates on the experimental methods and procedures. Chapters 4 to 6 summarize the major results with some discussions, including some interesting observations on the microstructural evolution study on the bulk solder, isothermal aging and in-situ microtensile test on solder/copper joint, thermal cycle and thermal shock on FR4-solder joint and, stress effect study on interface IMCs using specially designed C-ring solder joint respectively. Lastly, Chapter 7 delivers the conclusions obtained from the studies together with recommendations for further research.

Chapter 2: Literature Review

2.1 Role of Solder Alloys in Electronic Packaging

Solders generally refer to fusible alloys with a liquidus temperature below 400 °C. The elements composing solder alloys include tin (Sn), lead (Pb), silver (Ag), copper (Cu), gold (Au), bismuth (Bi), indium (In), antimony (Sb) and cadmium (Cd). The most commonly used lead-based solder alloys are binary Sn-Pb solder system. Other binary solder systems include Pb-In (Goldman et al., 1977, Chen et al., 1993), Pb-Ag (Liu and Duh, 1991) and Pb-Bi, and the ternary solder systems are like Sn-Pb-Ag (Lee et al., 2001), Sn-Pb-Bi (Yamamoto et al., 1995, Prasad and Mikula, 1999), Sn-Pb-In (Mei et al., 1997), and Sn-Pb-Sb (Evans, 1994). The physical properties for some of the solder alloys are summarized in Table 2.1 (Lau, 1991, Mei et al., 1997, NCMS, 1999). 63Sn-37Pb, 60Sn-40Pb and 62Sn-36Pb-2Ag (Frear, 1990a, Banks et al., 1995) are the common lead-based solder alloys used for electronic packaging assemblies. High lead solders like 3.5Sn-96.5Pb (Fan et al., 2004), 5Sn-95Pb (Wolf et al., 2000) and 10Sn-90Pb (Li et al., 2001) were also used in some of the specially designed component.

Solders are used in different levels of the electronic assembly sequence, where strict electrical, mechanical and thermal performances of solder alloys are required. They provide electrical interconnection of the silicon chip to the substrate, and act as heat dissipation channels and mechanical support for the chip. Solders also act in the same way within and among the different packaging levels in an electronic device. As such, they must be able to accommodate any relative displacement between the silicon ship and substrate as well as the component and the printed circuit board (PCB), and support the stresses that developed by this displacement, as shown in Figure 2.1.

Thermal displacements, resulting from different coefficients of thermal expansion (CTE) between the board and component can lead to thermal fatigue failure in solder (Pang et al., 2001, Yuko et al., 2003, Kanchanomai and Mutoh, 2004, Towashiraporn et al., 2005). Solders experience strains due to the difference in their CTE compared with those of other assembly materials of the component or board, as shown in Figure 2.2.

The repeating temperature cycling and environmental temperature gradients can lead to solder joint fatigue failure. Long-term reliability of solder interconnections is determined by the solder alloys' mechanical strength, resistance to fatigue, creep rupture, and other thermal-mechanical properties.

Table 2.1 Lead-solder alloys (Lau, 1991, Mei et al., 1997, NCMS, 1999, Puttlitz and Stalter, 2004)

Alloy Composition (Wt%)	Liquidus Temperature (°C)	Solidus Temperature (°C)	Yield Strength (MPa)
5In-95Pb	314	292	-
58Bi-42Pb	126	124	-
30In-70Pb	253	240	-
60In-40Pb	185	174	-
80Sn-20Pb	199	183	29.6
63Sn-37Pb	183	183	16.1
60Sn-40Pb	190	183	14.2
25Sn-75Pb	266	183	-
10Sn-90Pb	302	268	13.9
5Sn-95Pb	312	308	-
70In-30Pb	175	165	-
95Pb-5Sb	295	252	-
97Pb-3Sn	318	318	-
40In-40Sn-20Pb	130	121	-
43Sn-43Pb-14Bi	163	144	-
15Sn-82.5Pb-2.5Ag	280	275	-
10Sn-88Pb-2Ag	290	268	-
5Sn-93.5Pb-1.5Ag	301	296	-
1Sn-97.5Pb-1.5Ag	309	309	-
85Sn-10Pb-5Sb	230	188	-
5Sn-85Pb-10Sb	255	245	-
67.5Sn-29Pb-2Ag-1.5Sb	183	198	-
94.9Sn-3.1Ag-1.5Cu-0.5Pb	217	218	38
94.9Sn-3.1Ag-1.5Cu-0.2Pb	216	217	40
94.9Sn-3.1Ag-1.5Cu-0.1Pb	216	217	42

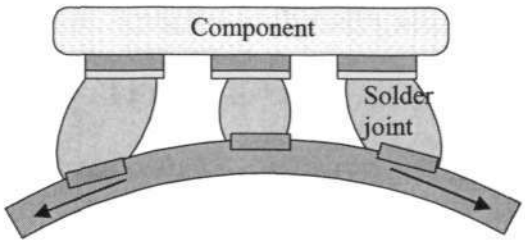


Figure 2.1 Solder joints subjected to tensile loading due to substrate flexing (bending) during handling of the assembly

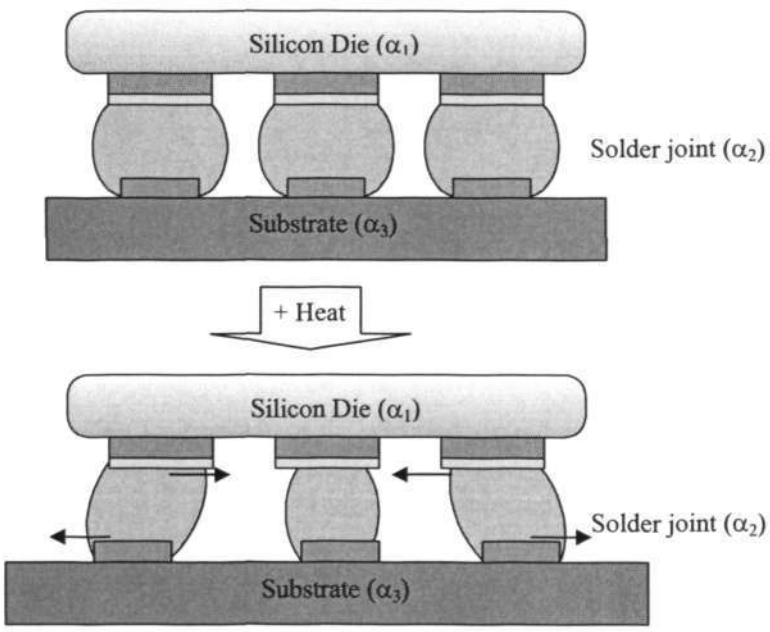


Figure 2.2 Solder joints subjected to shear strain during thermal cycling due to CTE mismatch between the chip (α_1), the solder joint (α_2) and the substrate (α_3)

From a manufacturing perspective the melting temperature of solder, i.e. the liquidus temperature, is perhaps the first and most important factor to be considered. The low operating temperature of the assembly equipment is to prevent the underfill materials, encapsulation epoxy resins, and die attach materials from degrading during

soldering process. Low soldering temperature will also help to prevent excessive growth of brittle IMCs that deteriorate the component. The relatively low melting temperature of 63Sn-37Pb eutectic solder, i.e. at 183°C permits most of the assembly equipment to be designed at low operating temperature.

To form a proper metallurgical bond between two metals, wetting must take place. This means that a specific interaction must take place between the liquid solder and the solid surface of the parts to be soldered. The ability of the molten solder to flow or spread during the soldering process is of prime important for the formation of a proper metallic bond.

As wettability is crucial to the efficiency of manufacturing and the reliability of electronic device (Guo et al., 2000, Chang et al., 2003, Liu and Lin, 2006), the interfacial energy and surface energy between the molten solder, flux and substrate that determine the solderbility of the solder should be low enough to permit the formation of proper solder joint (Abtew and Selvaduray, 2000). It is well known (Tu et al., 2002, Zeng and Tu, 2002) that lead in the Sn-Pb solder lowers the surface and interfacial energies of the solder and further results in excellent wettability of this family of solders on most of the substrates.

In order to maximize the interconnection density and at the same time without sacrificing the electrical performance of the component or system, the intermediate level of interconnection based on hybrid circuit technologies was developed. This high-density intermediate level packaging which is usually called Multi Chip Modulus (MCM) packaging has more recently become of interest for general. Since this high performance microelectronic system is developed for heavy usage such as high

performance supercomputer, the reliability of the solder joint becomes more stringent and crucial for the overall system performance.

2.2 Lead-free Solder for Electronic Packaging

2.2.1 Driving Force for Adoption of Lead-free Solder

Sn-Pb solders have been used widely in the immense electronic material world due to their unique characteristics such as low cost, good wettability (as mentioned above) and ease of manufacture. However, the safe use and disposal of lead-containing electronic products have become a hot issue of considerable interest from both environmental group and the legislative bodies. Starting with legislative activity in the United Stated during 1990's (Cannis and Syed, 2001), to the European Commission Directives and Japan appliance recycling restrictions of today, the industry has never been far from some sort of lead elimination requirement during the past decade.

On 13th June 2000, the European Commission adopted a proposal for a directive on Waste Electrical and Electronic Equipment (WEEE) and a proposal for a directive on the restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment (Barnes, 2005). RoHS proposal was designed to tackle the fast increasing waste steam of electrical and electronic equipment and complements based on European Union measures on landfill and incineration of waste. In order to prevent the generation of hazardous waste, the initial RoHS proposal for directive on the restriction of the use of certain hazardous substances required the substitution of various heavy metals and brominated flame retardants in new electrical and electronic equipment 1st January 2008 onwards (IPC, 2000, Tonapi et al., 2002). However in year

2002, both the council and the parliament gave official agreement to change the final implementation date of RoHS to July 2006 (EU, 2003).

Due to the impending legislative restrictions on the use of lead in electronics, there is a tremendous amount of interests in eliminating lead from the solders used in the electronic packaging industry. National Physical Laboratory (NPL) in the United Kingdom is undertaking a three-year program sponsored by the Department of Trade and Industry (DTI) (Richards, 2000). It aims to provide UK industry with state-of-the-art information, new test methods and best practice guides to aid development and assembly of lead-free microelectronics products. Soldering Technology Centre (SOLDERTEC) at International Tin Research Institute (ITRI) continues to investigate important issues in lead-free technology as they arise for the benefit of the industrial membership.

In Japan, the Japanese Ministry of Trade and Industry (MITI) proposed in May 1998 take-back (recycling) legislation (IPC, 2000, Pfahl, 2003). The Japanese Electronics Packaging Association (EPA) and government "suggest" reduced use of lead in part and increased recycling. MITI called for the use of lead to be reduced by half by 2000 and by two-thirds by 2005 (IPC, 2000). The Japanese Home Electronics Recycling Law, which was revised in 1998, calls for Original Equipment Manufacturer (OEMs) in Japan to be prepared to collect and recycle for major products by 1st April, 2001 (Richards et al., 1999).

To accelerate the reduction and elimination of toxic substances, including lead, the New Energy and Industrial Technology Development Organization (NEDO) project was started with sponsorship by the Ministry of Economy, Trade and Industry (METI) of Japan in 1999 (Fukuda et al., 2003). Within this government-industry framework, the

Japan Electronics and Information Technology Industries Association (JEITA) roadmap was developed. JEITA (Richards et al., 1999) roadmap focuses on practical implementation of lead-free products to accelerate their use by Japanese electronics manufacturers and help collect lead-free material characteristics (Richards et al., 1999). In June 2003, as a result of several years of research and development, METI publicly announced the establishment of Japanese Industrial Standard (JIS) for test methods for lead-free solders. The standard includes method for measuring the melting temperature ranges, mechanical characteristics, and wetting properties of lead-free solder (Fukuda et al., 2003).

Facing the market pressure from Japan and pending legislation in Europe, the US PCB industry peers over the possibilities of being forced into making a transition. In 1997, National Center for Manufacturing Sciences (NCMS) published a study conducted with several major OEMs for nearly 80 solder alloys but none were considered drop-in replacements (IPC, 2000). The move toward lead-free solder alternatives is gearing up with the completion of the National Electronics Manufacturing Initiative Lead-free Project in December 2000 (NEMI, 2000). Believing in that the move to lead-free electronics assemblies is inevitable, IPC published its 4th draft of lead-free roadmap in June 2000 (IPC, 2000). This IPC roadmap covers a guide for assembly of lead-free electronics, and content that supporting the voluntary removal of lead from electronics.

2.2.2 Lead-free Solder Standardization

The preferred solution for lead-free alternatives must satisfy the soldering process compatibility and solder joint reliability performance expectation. The

expectation is that the lead-free solder replacement candidates must give compatible process performance to the eutectic Sn-Pb solder alloy currently used in terms of acceptable wetting, adequate electrical and thermal conductivity, and compatible with other metallizations. The lead-free solder joints are also expected to possess similar, if not better, long-term solder joint reliability performance compared to Sn-Pb solder joints.

However, up to now, no lead-free replacements can satisfy all the criteria, and selection of lead-free soldering alloys would depend on the specific applications. The electronics industry is beginning to converge on a few preferred lead-free solder replacement candidates. A relatively large number of lead-free solders thus far proposed are either the binary system (Sn-Ag, Sn-Cu, Au-Sn, Sn-Sb, Sn-In and Sn-Bi) (Miric and Grusd, 1998, Yoon et al., 2004, Islam et al., 2005, Kim et al., 2005b, Kumar et al., 2005, Yoon and Jung, 2005a, Yoon and Jung, 2005b) or the ternary system (e.g., Sn-Ag-Cu, Sn-Bi-Cu, Sn-Bi-In and Sn-Bi-Ag) (Suganuma, 2001, Kim et al., 2005a, Luo et al., 2005, Magagnin et al., 2005) or quaternary system (e.g., Sn-Ag-Bi-Cu, Sn-Ag-Sb-Cu and Sn-Bi-Ag-Sb) (Suganuma, 2001, Lee et al., 2005).

It is noticed that the basic building block element for any of the lead-free alloys can be identified as Sn, and potential substitutes for Pb are Ag, Sb, In, Cu, Zn or Bi. Unfortunately there is a lack of international standards and methodologies for evaluating the quality and reliability of lead-free solders. Thus, the three large industrial areas, the USA, Japan and Europe, try to establish their own standards and develop their own lead-free solders.

In Japan, Japan Institute of Electronics Packaging (JIEP) used to actively involved in research work on the lead-free solder with low melting point such as Sn-

8Zn-3Bi, Sn-3Ag-(6,8)In, and Sn-9Zn-Al (Fukuda et al., 2003). However, following a conference held by Sony late May in 2001, it appeared that Japan's industry were moving away from their previous Bi and Zn containing lead-free alloy to 96.5Sn-3Ag-0.5Cu (Cannis and Syed, 2001). Majority of the companies use Sn-Ag-Cu system with the composition of 96.5Sn-3Ag-0.5Cu for reflow soldering and hand soldering (Fukuda et al., 2003). The same system is also used in wave soldering, however some companies use Sn-Cu. JEITA recommended 96.5Sn-3Ag-0.5Cu more than Sn-Ag followed by Sn-Zn-Bi for solder and solder balls, and more favoring 96.5Sn-3Ag-0.5Cu for wave soldering as compared to Sn-Cu (Knott and Mikula, 2003).

In Europe, SOLDERTEC at ITRI (Bath et al., 2000, Nimmo, 2002) tries to coordinate the European research programs on lead-free solders. Their recommendation of lead-free solders are alloys within the composition range of Sn-(3.4-4.1)Ag-(0.45-0.9)Cu which includes the four most commonly available solders and they are 95.5Sn-4Ag-0.5Cu, 95.5Sn-3.8Ag-0.7Cu, 95.9Sn-3.6Ag-0.5Cu and 95.8Sn-3.5Ag-0.7Cu. Although the properties of all four alloys are expected to be similar the current preference is for those with the slightly higher silver content.

However, realizing that the choosing of a single lead-free solder alloy would significantly benefit the industry, effort was put into reviewing the research that had been done with lead-free solders in the United States, Europe and Japan (NEMI, 2000). Finding no drop-in replacement for Sn-Pb solder, the NEMI group announced the Sn-Ag-Cu alloy of 95.5Sn-3.9Ag-0.6Cu (±0.2%) and 99.3Sn-0.7 as standardized lead-free material for reflow application and wave solder production respectively on 24th January 2000 (Handwerker, 2001, NEMI, 2002, NEMI, 2003). Following this announcement, a lot of the research work on these lead-free solders especially the Sn-Ag-Cu has been carried out (Bradley et al., 2002, Handwerker, 2002, NEMI, 2004). The Sn-Ag-Cu lead-

free solder is getting common and has the momentum to meet the implacable legislation schedule set by WEEE and Reduction of Hazardous Substances (RoHS) in July 2006.

2.2.3 Sn-Ag-Cu Lead-free Solder

With legislation in the pipeline to restrict the use of lead in electronic products, the search for lead-free replacement solders was in earnest. One popular alloy, already used for high temperature solder applications, is the binary 96.5Sn-3.5Ag whose eutectic temperature is at 221 °C. Several sources have also reported good mechanical properties and thermal fatigue properties (Foley et al., 2000, Kikuchi et al., 2001, Plumbridge et al., 2001, Wade et al., 2001) on this lead-free solder. Although the processing and properties of this alloy are well known, its liquidus temperature is about 40 °C higher than that of 63Sn-37Pb solder. This can cause manufacturing incompatibilities in microelectronic packaging technology especially for polymer-based devices that are susceptible to cracking due to moisture contamination. Incompatibilities in packaging technology are the main obstacle that have hindered the manufacturer from switching the lead-solder to lead-free solder due to involvement of high capital investment. In order to make Sn-Ag base alloys more compatible with Sn-Pb manufacturing procedures, ternary additions were examined in an effort to decrease the liquidus temperature. A third alloy addition is Cu, which decreases the liquidus temperature and in addition provides a eutectic point that helps to limit the mushy range. Presence of eutectic point is desired for ideal solder system, because eutectics are preferred due to their ease of manufacture and reliability at high temperature as a result of a sharp melting point and narrow mushy range (Lewis et al., 2002).

Even though Sn-Ag-Cu failed to be a drop-in replacement for Sn-Pb solder, it was well accepted as a lead-free solder. This is because Sn-Ag-Cu contains elements common to those already in use in current soldering technology and its lower melting temperature will make the changeover of lead-solder to lead-free solder easier to implement and will also help lower the assembly cost. These advantages have made it to be chosen as one of the most favorable lead-free systems. However, uncertainty about the precise composition of the Sn-Ag-Cu ternary eutectic still exists. Since 1959, a number of Sn-Ag-Cu ternary eutectic compositions have been examined and proposed (Kim et al., 2002c, Lewis et al., 2002) and this ambiguity has resulted in difficulties in understanding the solidification phenomena in soldering which can provide information to control the microstructure. However, since the announcement of NEMI group, Sn-Ag-Cu alloy with a composition of 95.5Sn-3.9Ag-0.6Cu (±0.2%) which is the closest to the recently reported ternary eutectic, 95.6Sn-3.5Ag-0.9Cu (Loomans and Fine, 2000) and 95.43Sn-3.66Ag-0.91Cu (Moon et al., 2000) has become the focus of most of the lead-free solder development activities. The melting temperature of this ternary eutectic was reported to be in a range from 217 to 219 °C (Miric and Grusd, 1998, Kim et al., 2002b) rather than a specific melting point as for binary eutectic alloys. This is due to the slight variation in the composition. Although there is slight variation in the alloy composition, the ternary eutectic transformation of this lead-free solder alloy family follows the reaction below (Loomans and Fine, 2000, Anderson et al., 2001, Plumbridge et al., 2001, Kim et al., 2002c, Lewis et al., 2002):

$$\text{Liquid} \rightarrow \text{Sn-}\beta + Cu_6Sn_5 + Ag_3Sn \qquad [2.1]$$

Due to free growing crystals, it is believed that each of the solid phases involved in this ternary eutectic transformation reaction has a distinct morphology (Lewis et al., 2002). With comparable cooling rate about 1 °C/min, the Ag_3Sn phase was reported

(Kim et al., 2002c, Lewis et al., 2002) to be generally in platelike shape, yet it appears in both platelike and fibrous shapes under relative fast cooling rate faster than about 1 °C/sec. For the Cu_6Sn_5 phase, Lewis et al. (Kim et al., 2002c, Lewis et al., 2002) only mentioned that its shape is generally in hexagonal rod without considering the cooling rate and this description is similar to the observation on the 95.9Sn-3.8Ag-0.3Cu solder bump in the flip-chip assembly (Frear, 2001). Other than the two fore mentioned IMCs within the Sn-matrix of the bulk solder, Ni_6Sn_5, Ni_3Sn_4, Cu_6Sn_5 and Cu_3Sn (Lin et al., 2001, Zeng et al., 2001, Zribi et al., 2001, Ho et al., 2002) were found to be formed between the solder and Cu pad with and without Ni coating.

2.2.4 Technical Issues

Solders are primarily used in the level 1 and 2 of the packaging process. At level 1 packaging, the solder provides electrical and mechanical connections between the silicon chip and the bonding pad. Recently, the use of solder bumps on the surface of the silicon chip has become widespread reality in the packaging industry due to the higher number of I/O (input and output) terminals that can be attached to a given area. This packing concept is called flip chip connection where the silicon chip is turned upside down and mounted on an appropriate substrate through solder bumps, as shown in Figure 2.3. In level 2 of the packaging, the component is mounted to printed wiring circuit board (PWB) and solder is the primary means of interconnection material. Practically, most of the microelectronic devices are mounted on the PWBs using solder. There are two primary means of attaching electronic components to PWBs, i.e., pin-through-hole (PTH) and surface mount technology (SMT). The assembly and soldering of Printed Circuit Board Assemblies (PCBA) can involve pure surface mount

components or mixed technology assemblies where both SMT and PTH are used, either in single sided or double sided PCBA configuration.

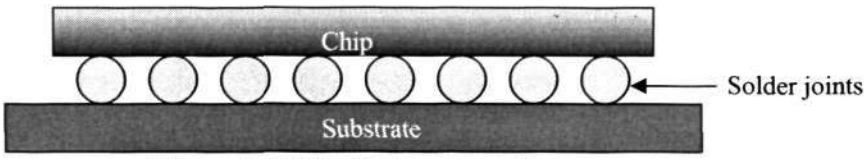


Figure 2.3 Flip Chip connection

Soldering of surface mounted devices is commonly called reflow soldering. The primary purpose of the reflow process is to melt the solder paste, wet the surface to be joined, and then solidify the solder into strong metallurgical bond. However, prior to this melting phase, several other procedures occur and the sequence of the action is shown in Figure 2.4. On the other hand, PTH soldering is done by wave soldering, where the assembly is transported over a molten solder bath from which the solder rises and forms solder joints by capillary action. The properties of the solder that are important are invariably process dependent. The formulation and printability of the solder paste are critical parameters for reflow soldering, while viscosity and density of the molten solder significantly influence the performance of the wave soldering process.

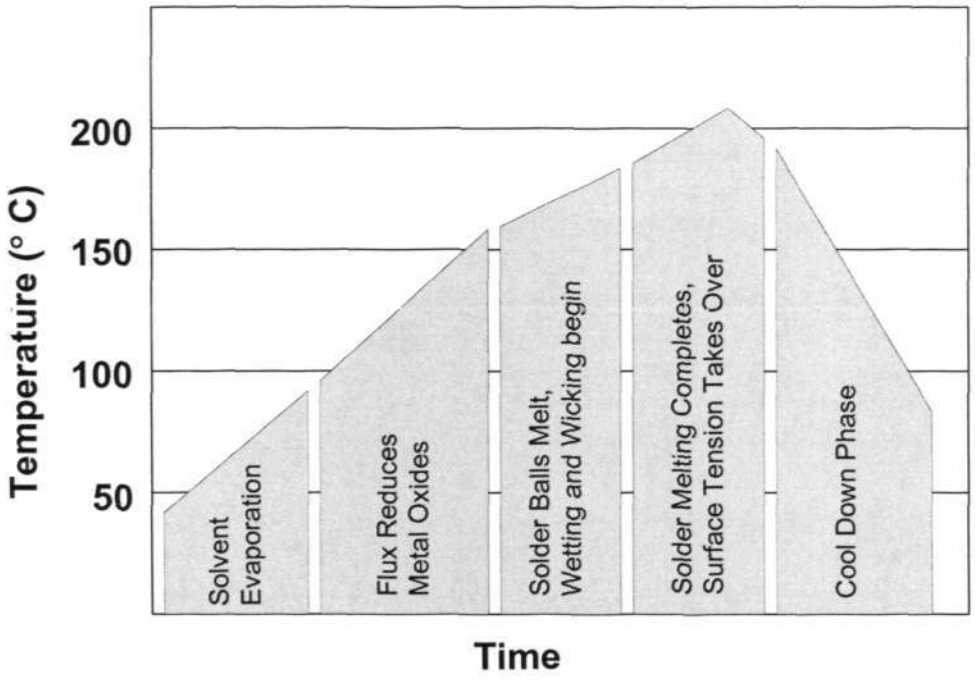


Figure 2.4 Solder reflow phases

As Sn-Pb solders have been used in the electronics application for more than 50 years, they are almost exclusive in the manufacture and assembly of electronic circuit boards. It has been well known that Pb provides many technical advantages in electronic packaging industry. It reduces the surface tension of pure Sn and prevents the formation of white-β Sn to gray-α Sn upon cooling. In addition, Pb serves as a solvent metal, enabling the other joint constituents such as Sn and Cu to form intermetallic bonds rapidly by diffusing in the liquid state (Zeng and Tu, 2002). These factors, combined with Pb being readily available at low cost, make it an ideal alloying element with Sn. The board level soldering system that is mainly based on eutectic and near eutectic Sn-Pb solders has been well developed and refined with many years of experience. Hence the cost of conversion to a lead-free solder and its associated reliability impact could be quite significant.

Moving to a lead-free environment will also have an impact on PCB substrate construction especially for the commonly used polymeric substrate family. The recommended lead-free solder alloys, Sn-Ag-Cu for reflow and Sn-Cu for wave soldering will raise the soldering temperature by as much as 40 °C, which will obviously have an impact on a number of materials and steps in the PCB assembly process. This relatively high process temperature as compared to conventional Sn-Pb solder will easily hit the glass transition temperatures of most of the polymeric substrates and which further cause a drastic drop in the modulus value of the polymeric material (Sunappan and Collier, 2003, NEMI, 2005). On the component side, there are concerns with temperature ratings, thermal mismatch, and thermal shock considerations that will significantly affect the reliability of the system.

2.3 Metallization for Lead-free Solder

In the electronic packaging industry, Cu has been widely used as a useful electrode material due to the excellent electrical and thermal conductivities. However, due to the replacement of lead-free solder, various surface finishes have to apply to Cu to improve the solderability and reliability of the solder joint. As discussed previously, most of the lead-free solder replacement candidates preferred by the electronic industry are basically Sn rich alloys and have relatively high melting temperatures. These high Sn content solder alloys react more rapidly with Cu under bump metallization (UBM) at higher reflow temperature, forming a thick Cu-Sn IMC layer.

As Ni is known to react much slower with Sn (Kim et al., 1999), a lot of research work concerning the lead-free surface finishes has been carried out on the study of Ni-based metallization. These Ni-based metallizations include electroless

Ni/Pd, electroless Ni/Pd immersion Au (ENEPIG), electroless Ni immersion Au (ENIG) and electroless Ni/P (Jang et al., 1999, Ghosh, 2000, Liu et al., 2001, Zribi et al., 2001, Strandjord et al., 2002). Even though, the IMC growth has found to be minimized by the introduction of Ni as a diffusion barrier layer on Cu bond pad, it has been reported (Chan et al., 2001, Zeng and Tu, 2002, Sriyarunya, 2004, Yoon et al., 2004) that formation of Ni-Sn IMC and Ni-P layer can strongly affect solderability and the strength of the solder joint (Kim et al., 2005a). The concern of the interaction between the Sn-rich solders and the electroless Ni-based metallization and its relatively high processing cost have gained the momentum to work on several alternative lead-free surface finishes. These surface finishes include Sn-Cu, Sn-Ag, Sn-Bi, electroless Ni electroless Pd immersion Au (ENEPIG), immersion Sn and immersion Ag metallizations. The first three candidates offer competitive cost Sn-Pb surface finishes, but suffers from various shortcomings with respect to their properties and performance. The Sn-Cu surface finish is prone to whisker formation (Zeng and Tu, 2002). Sn-Ag surface finish is constrained by high cost, plating chemical instability, limiting process window and difficulty of wastewater treatment (Sriyarunya, 2004). Sn-Bi surface finish can suppress the whisker growth (Schetty, 1998) but the present of Bi causes technical problems like crack or lift-off (Suganuma, 1999). In addition, the big discrepancy in electro-chemical property between Sn and Bi has made the control difficult for electroplating of Sn-Bi especially for mass production (Zhang et al., 2000). ENEPIG surface finish is a refinement of Ni/Pd finish that offers somewhat enhanced performance due to a quicker wetting time. However, as Pd and Au are very expensive materials, only component for specific application that required ultra-thin surface finish uses ENEPIG finish. An advantage of the use of immersion Ag as opposed to the Au and Pd containing coating is the lower material cost, and generally able to produce good solderability and increases the board finish (Stam and Davitt, 2001, Arra et al., 2004).

Unfortunately, Ag is prone to significant dissolution by molten solder during processing. Ag also has a potential to diffuse over surface under conditions of high humility and applied potential in the process will results in electromigration failure of the solder joint (Vianco et al., 1997).

As compared to other lead-free alternatives as mentioned above, pure Sn surface finish is unique. It has co-existed with Sn-Pb as a solderable material for centuries (Zhang et al., 2000, Xu et al., 2002). Sn is the main constituent of solder joints and is comparable with many lead-free solder such as Sn-Ag and Sn-Bi. In addition, it also exhibits excellent control and uniformity of plating thickness. Furthermore, Sn recovery is well established in the recycling industry. The connector industry has been plating pure Sn for more than 50 year, and the plating technique introduced was electrolytic plating. The electrolytic Sn coatings are generally soft, ductile and have relatively low melting point. However, electroplated Sn is known to grow whisker which can be detrimental for the microelectronic application (Xu et al., 2002, Dittes et al., 2003, Galyon and Gedney, 2004). Several remedies have been proposed to overcome the problem of whisker formation: alloying with small percentage of other alloys, hot dipped Sn, baking of Sn after coating and introducing chemical displacement process to produce immersion Sn (Galyon and Gedney, 2004). Other than limited whisker growth, immersion Sn is found to be suitable for products that require thicker Sn surface finish. It also helps to improve solderbility for processes at multiple cycles and higher temperature, enhanced surface flatness and fine pitch compatibility. Therefore, it is expected that the use of immersion Sn as a surface finish will grow substantially and become a high volume technology.

2.4 Formation of Sn Whiskers

Formation of metal whiskers has started to draw the attention from the scientific community as early as in the 1940s (Cobb, 1946). In the early stage, cadmium (Cd) whisker was found to grow and result in failures of Cd plated condenser and multi-channel telephone transmission lines (Galyon, 2003, Gaylon, 2004). Since then, a series of long-term investigations into the general topic of whisker formation was carried out by Bell Laboratories (Compton et al., 1951). It was found that whisker form spontaneously, not only on Cd electroplating, but also electroplating Zn, Sn, Al casting alloy and electroplated Ag. After the Compton 1951 paper, most of the research work was focused on Sn electroplating on a variety of substrate. Sn and Sn alloy electroplates became one of several surface finishes of choice in the electronic industry. This is because they provide desirable properties; such as excellent solderability, contact resistance, electrical conductivity and corrosion resistance.

In the 1950s, whisker fundamentals were addressed and some of the basic concepts currently used to describe whisker formation and growth were proposed. In 1954, Koonce and Arnold from Bell Laboratories published the first electron microscope micrographs of Sn whisker and they concluded that whisker growth from the base not from the tip. This fundamental observation is accepted today without reservation. To account for the Koonce-Arnold observation, a numbers of dislocation theories were proposed. As a whole, the basic idea was to construct a dislocation mechanism that moved toward the film surface and deposited a layer of atoms at that surface. The continual operation of the dislocation mechanism would grow the whisker (Eshelby, 1953, Gaylon, 2004). However, many of these 1950s proposals were perhaps little more than well-informed speculation at the time and still debated today. Other than these fundamental studies, the researchers also started to discuss about the Sn

whisker mitigation strategies such as fusing and hot dipping. In 1959, Arnold (Arnold, 1959) reported on the beneficial effects from alloying Sn films with Pb. Based on this work, the predominant whisker mitigation strategy for electrodeposited Sn films becomes Pb co-deposition.

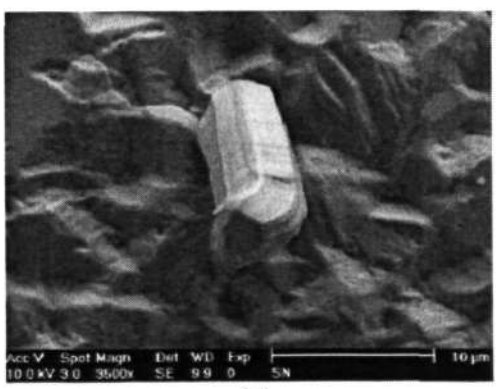
Since then, there were fewer whisker publications during the 1960s and 1970s. The research focus was shifted from the theoretical study to the area related to whisker mitigation practices. However, one of the important theoretical publications was by K. N. Tu (Tu, 1973) in 1973. In his report, he attributed the growth of Sn whisker to the internal stress generated by the IMC formed at the boundary between the Cu substrate and Sn film. Over the next 30 years, K. N. Tu and co-authors have continued to contribute to whisker related publications. In 1993, K. N. Tu offered a new theoretical concept in whisker growth. In this report (Tu, 1993), he proposed that a "weak oxide" layer enabled the localized relief of internal stresses by permitting whisker growth through a crack in the oxide layer. A few years later, by accommodating Tu's "weak oxide" concept, a major whisker paper was published by Lee and Lee (Lee and Lee, 1998) in 1998. This paper showed the first published cantilever beam stress measurements for Sn film on Cu substrate with and without annealing treatment. The procedure adopted for stress measurement was based on the recognition that the formation of three-film composite of Sn/Cu-Sn IMC/ Cu substrate of the Sn deposition. Lee and Lee also managed to propose a dislocation mechanism that closely matched the mechanism proposed by Eshelby in 1953.

In the 21st century, Sn whisker study has renewed the interest of researchers due to the pending of regulations requiring Pb removal from electronic component. The conversion to lead-free processes and products in the electronic industry has resulted in an increasing use of pure tin (Snugovsky et al., 2004) coating on leads and surface

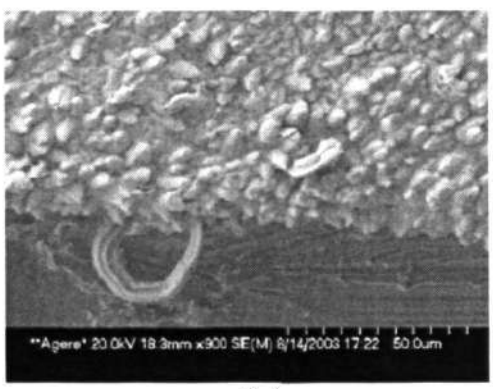
finish of various components. Based on property, performance and cost criteria, pure tin surface finish is one of the most nondisruptive and economical way for replacing Sn-Pb in lead-free applications (Osenbach et al., 2005). Unfortunately, pure Sn and high Sn content alloy plating finishes have received significant scrutiny due to reliability concerns associated with Sn whisker (Choi et al., 2002, Zhang et al., 2004).

Sn whisker is mostly reported to be a single crystal (Lee and Lee, 1998, Zhang et al., 2000, Brusse et al., 2002, Sheng et al., 2002, Dittes et al., 2003, Galyon, 2003, Osenbach et al., 2004). However, there are uncertainties about this finding as less definite statements such as "mostly single crystal" and "typically single crystal" were used in some of the publications (Lau and Pan, 2002, Osenbach et al., 2005) to describe the Sn whiskers.

Often, Sn whisker is found to grow spontaneously from the surface of Sn and high Sn content alloys (Lee and Lee, 1998, Osenbach et al., 2005). The Sn whisker can be in many different shapes, e.g., filament, nodule, column, needle, and hillock as shown in Figure 2.5.



(a)



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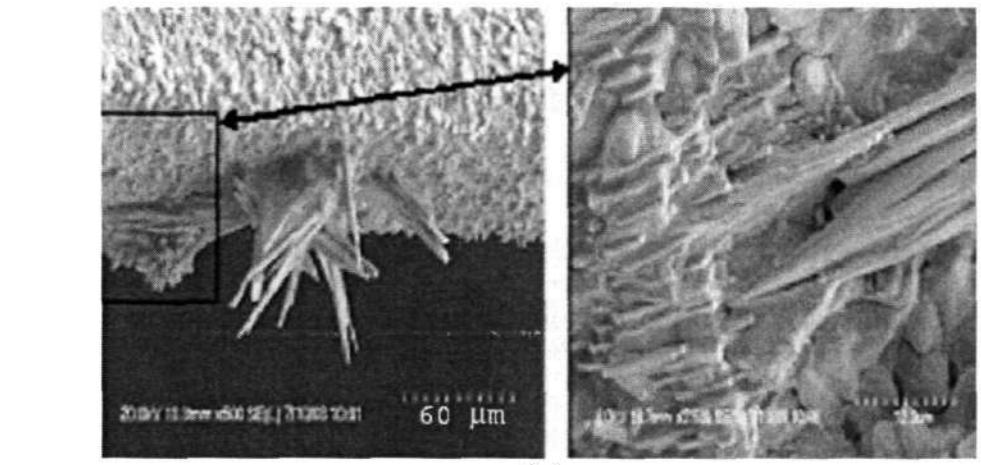
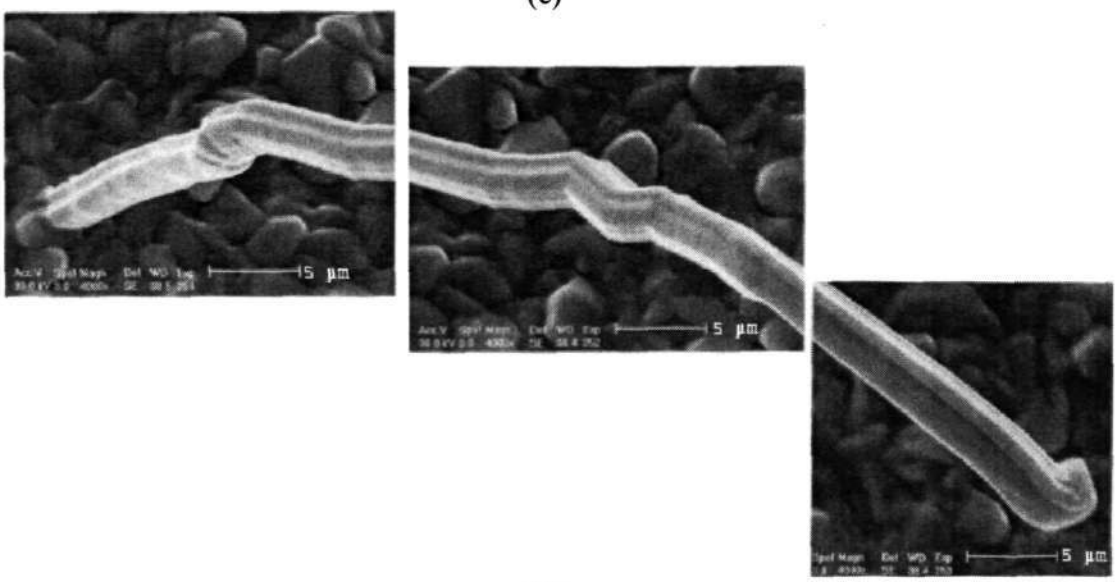


(c)



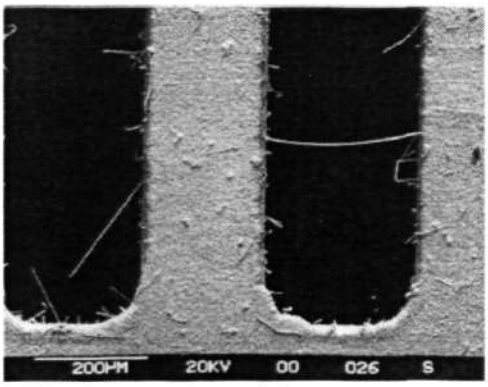
(d)

Figure 2.5 SEM images of (a) A short whisker on pure Sn surface finish. (Zeng and Tu, 2002). (b) Irregular shape of Sn whisker (curve backward), nodules or hillock of Sn whiskers found on device after 1702 hr of storage at room ambient (Osenbach et al., 2005). (c) Flower clusters of Sn whiskers on lead of a device after 672 hr of exposure to 60 °C/93%RH (Osenbach et al., 2005). (d) A long kinked Sn whisker from Sn deposit (Lee and Lee, 1998)

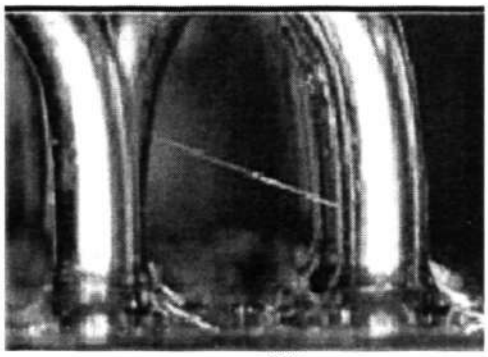
Sn whisker can grow between adjacent conductors of different potential and cause either a transient short as the whisker is burned open, or permanently short (Yen et al., 2001, Zeng and Tu, 2002) as shown in Figure 2.6. Even if shorting the adjacent lead-frames does not occur, whisker protrusion act as an antenna in high-frequency

circuit that will affects the circuit performance (Galyon and Gedney, 2004). On top of that, Sn whisker can be broken loose from their substrate and as debris causes mechanical problems with slip rings, optical devices, microelectromechanical devices (MEMS) and similar component (Brusse et al., 2002). Because Sn whisker is both technological important and scientifically intriguing, it formation and growth continue to receive extensive academic and industrial interests. Even though a significant amount of work on Sn whisker have been done, expert in the electronics and electroplating industry still have not reached a consensus upon a single accepted explanation of the mechanism(s) that drives whisker formation. However, there are some commonly accepted factors. Generally speaking, there is agreement that whisker growth occur from the base of the whisker and not the tip (Lee and Lee, 1998, Zeng and Tu, 2002, Dittes et al., 2003). Most agree that Sn whisker is a case of surface relief phenomena, i.e., the growth of whisker relieves the compressive stress in the Sn matrix on which they grow (Tu, 1993, Sheng et al., 2002). The origin of the compressive stress can be chemical, thermal and mechanical. The sources of these stresses including:

a) Residual stresses of the Sn coating; depends on purity of the Sn plate, grain size and grain crystallographic orientation of the Sn plate and Sn-plating thickness.
b) IMC formation; formation of IMC such as Cu_6Sn_5 between Cu and Sn film can alter the lattice spacing in the Sn layer
c) Substrate surface finish; can be affected by pre-plate chemical treatment on the substrate and the process used to form the substrate.
d) External applied stress; bend radii of the plated surface for lead formation.
e) Environment stress; post-plating thermal treatment (baking) was imposed to release residual stresses of the coating, storage condition that depends on temperature and humidity levels and thermal cyclic loading during operation



(a)



(b)

Figure 2.6 (a) SEM image showing Sn whisker grown on eutectic Sn-Cu finish on leadframe. One of the whiskers shorts two of the leadframe legs (Zeng and Tu, 2002). (b) Photomicrograph showing a Sn whisker grown across the tin-plated hook terminals of an electromagnetic relay (Brusse et al., 2002).

2.5 Sn Whisker Mitigation

The possibility of whisker formation is always present in high Sn content coating. Even though, to date, there is no industry-accepted test method to measure the propensity of a given product or process to form whiskers. Various industry and consortia in United Stated, Japan and Europe have initiated studies to define and validate through experimental evidence to determine measures which can be taken to mitigate Sn whisker formation. Some of the common recommendations (Zhang et al., 2000, Brusse et al., 2002, Lau and Pan, 2002, Galyon, 2003, Sriyarunya et al., 2004) are as listed below:

(a) Use Ni barrier undercoat to minimize the IMC and stress

(b) Use lager gain matte Sn instead of bright Sn

(c) Use thicker Sn coating thickness (approximately 10 μm)

(d) Alloying with small percentage of other metals (e.g., Pb, Bi)

(e) Reflow Sn or "fuse" surface coating to remove the internal stress and to re-dissolve the surface oxide layer

(f) Produce thicker Sn oxide layer

(g) Consider Sn dipping for large-pitch component

Nonetheless, the implementation of the aforementioned mitigation techniques has not been shown to completely prevent whisker formation. Therefore, there is a need to achieve and verify through direct investigation a consensus understanding of the fundamental mechanisms of whisker formation. Only when such fundamental knowledge is acquired can manufacturers and users confidently utilize material and processes will mitigate the risk of whisker induced failures. If the compressive stress theory of the initiation and growth are valid, then the alloying metals may absorb or reduce compressive stress within the plating. If external stresses are severe, such as CTE mismatch during product service life, then nucleation and growth could still occur in such alloyed coating. Therefore understanding the various stress scenarios under which whisker will form on alloyed surfaces should be of high priority.

2.6 Mechanical Properties of Lead-free Solders

Solder is used by the microelectronics industry and is usually available in three basic forms: bulk solders for operations such as wave soldering, solder paste for operations such as surface mount reflow, and solder balls or solder columns for applications such as ball grid array, column grid array and flip chip packages. Solder paste contains solder particles that typically range from 4 to 8 μm in diameter, formulated with flux. Solder balls typically range from 0.1 to 1.0 mm in diameter. While bulk solder production is metallurgically straightforward, solder ball production does require more sophisticated techniques, and the alloy must be amenable to fabricate

the balls in the sizes mentioned above. As the drive to miniaturization continues, it is expected that there will be requirements to produce balls that are even smaller in diameter, especially for BGA and flip-chip applications. Since solder used in electronic industry exists in various forms, the design of specimen plays an important role in the representability and validity of the research result. The specimen design is the first important aspect for a test method. The specimens currently used to test the thermal mechanical properties and the fatigue life of solder joints can be divided into three categories as: bulk solder, simplified shear sample and SMT solder joints.

2.6.1 Comparison of Various Specimens

In general, bulk solder specimens, as shown in Figure 2.7 (a) (Weinbel et al., 1987, Vaynman et al., 1988, Guo et al., 1992, Abell and Shen, 2002, Kanchanomai et al., 2002b, Mutoh et al., 2002, Kanchanomai and Mutoh, 2004), are prepared by two methods: to cast directly or shape by as-cast original solder bar. The entire specimen is made up of solder. Obviously, bulk tensile specimen can be used to get the mechanical properties of solder alloys. The mechanical properties obtained are useful as the reference data for the correlated tests. The material properties, such as yield strength, ultimate tensile strength, CTE and elastic modulus for wide variability of lead-free solders are listed in Table 2.2.

Table 2.2 Physical properties of lead-free solder alloys (Lau, 1991, Jones et al., 1998, NCMS, 1999, Puttlitz and Stalter, 2004, Lee et al., 2005)

Alloy Composition (Wt%)	Liquid (°C)	Solidus (°C)	Ultimate Tensile Strength (MPa)	0.2% Yield Strength (MPa)	Elongation (%)	Elastic Modulus (GPa)	CTE (μm/m°C)
40.5Sn-56Bi-2Ag-1.5Sb	145	137	68.6	62.5	27	-	13.15
40Sn-55.5Bi-3Ag-1.5Sb	147	137	64.7	59.7	45	-	-
40Sn-55Bi-3Ag-2Sb	150	138	67.6	61.9	44	-	-
41Sn-57Bi-2Ag	147	140	71.6	65.4	31	-	14.39
41Sn-57Bi-2In	140	127	58.2	50.4	72	-	15.85
41Sn-57Bi-2Sb	141	150	30.6	27.2	48	15.7	-
42Sn-58Bi	139	139	35	26	46	12	17
42Sn-56Bi-2In	126	140	30.6	27.2	48	15.7	18.74
42Sn-56.7Bi-1In-0.3Cu	138	132	62	58	38	-	-
48Sn-2Ag-46Bi-4Cu	146	137	69.4	67.6	3		14.38
56Sn-41Bi-3Ag	217	138	70	64	39	-	-
63Sn-37Pb*	183	183	31	27	48	-	26
50Sn-50In	118	125	≈20	-	≈25	-	-
77.2Sn-20In-2.8Zn	180	106	37	35	31	-	-
77.2Sn-3.5Ag-20In	187	175	35	33	42	-	22
78.4Sn- 9.8Bi-9.8In -2Ag	195	163	106	100.4	7	-	11.86
78Sn-19.5Bi-2.5Ag	196	138	93	83	17	-	-
83.6Sn-8.8In-7.6Zn	195	178	44	42	14	-	-
90Sn-2Bi-8In	215	206	55	49	25	-	-
90Sn-7.5Bi -2Ag-0.5Cu	238	229	61	57	19	-	-
91.8Sn-4.8Bi-3.4Ag	216	211	71	46	16	-	22
93.5Sn-2Bi-3Sb-1.5Cu	231	225	65	51	28	-	-
93.5Sn-3Ag-1Bi-1Cu-1.5Sb	224	220	63.8	57.6	21	-	19.9
93Sn-3Ag-2Bi-2Sb	226	219	64	48	36	-	-
94Sn-2.5Ag- 2Bi-1.5Sb	226	219	56	48.7	21	-	-
95Sn-5Sb	241	234	35.2	25.7	22	44.5	20.09
95.5Sn-2.5Ag-2Bi	221	215	52	46	26	-	-
95.4Sn-3.1Ag-1.5Cu	216	217	-	39	-	47	-
95Sn-3.5Ag-1.5In	220	214	34	32	26	-	22
95Sn-3Ag-2Bi	220	216	55	38	30	-	22
86.5Sn-3.08Ag-10.05Sb	231.3	228.2	-	-	-	<26	-
95Sn-3Ag-2Sb-2Cu	224	221	53	46	32	-	-
96.2Sn-2.6Ag-0.8Cu-0.5Sb	226	211	26	23	9	-	22
96.5Sn-3.5Ag	221	221	27	23	24	26	22
97Sn-2Cu-0.8Sb-0.2Ag	230	219	30	26	27	-	-

* Eutectic lead-solder for reference

However, the use of result obtained in this manner to model the service life of a real electronic assembly might not be appropriate due to the size effect. This is because bulk solder samples are usually about 10^4 to 10^5 times larger by volume than the solder joints. This might results in large error to predict the service reliability of the solder

joints by using the data obtained from the bulk specimens. As a result, a new concept of "representative volume" (Bonda and Noyan, 1992, Bonda and Noyan, 1996) was presented to verify whether the deformation of such large specimens represents that of the small solder joints. The "representative volume" is defined as the smallest volume which represents the average inelastic and in homogeneous deformation of the entire body (Bonda and Noyan, 1996). The bulk test specimens can only be used to predict the behavior of the solder joints if the solder joint is larger than the "representative volume".

By taking into consideration of the volume effect, Darveaux and Banerji (Darveaux and Banerji, 1992) employed solder assemblies for test, as shown in Figure 2.7 (b). In this case, the test specimen is very near to actual soldered assemblies. A simplified shear joint is usually fabricated from two or three pieces of plates joined by solder and often called a single or double shear specimen, as seen in Figure 2.7(c)-(e) (Mei et al., 1991, Solomon, 1991, Mei and Morris, 1992, Sandstrom et al., 1993, Hong et al., 1996, Xie et al., 1996, Lee et al., 2003, Sun et al., 2005, Telang and Bieler, 2005). The ring-pin or ring plug type, as shown in Figure 2.7(f) (Frear, 1989, Frear, 1990b, Nir et al., 1991, Pao et al., 1993, Sandstrom et al., 1993, Foley et al., 2000, Stam and Davitt, 2001), is a simplified shear specimen. The plate or beam materials chosen in the shear samples are mostly Cu. The simplified shear specimen produces systematic data for the correlation of the fatigue life for the strain applied onto the solder joint. Hence, in the case of a single shear specimen, such results on fatigue studies should be more reliable and repeatable.

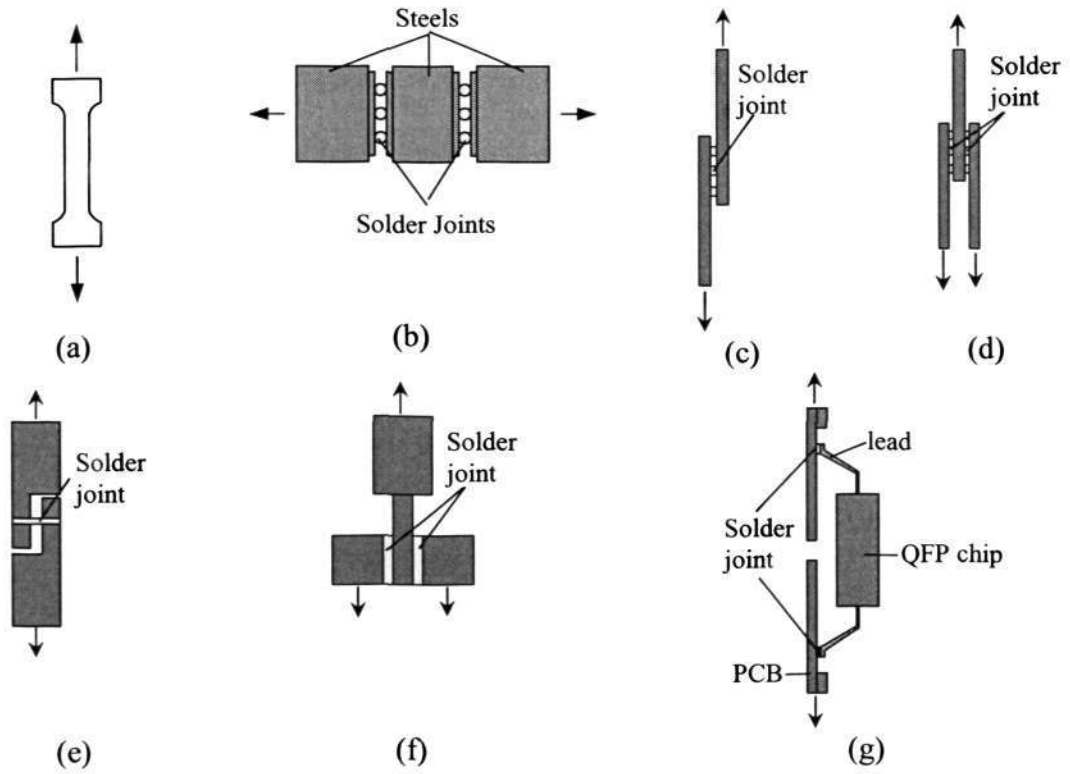


Figure 2.7 Schematic of different specimens currently used in the tests of mechanical properties (a) bulk solder (b) tensile ball (c) single shear (d) double shear (e) lap shear (f) ring-pin (g) SMT solder joints

2.7 Microstructure of Lead-free Solder Joints

The properties of the solder joint are influenced by its chemical composition and microstructure. The effect of microstructure on the mechanical properties of solder joints is of great interests in research work. It has been reported (Jung and Conrad, 2001a) that, under the influence of temperature and stresses, a heterogeneous coarsening process takes place continually changing the microstructure of the solder joint. Many researchers who worked on both leaded (Morris et al., 1997, Jang and Paik, 1998, Kishimoto et al., 2001) and lead-free solder alloys (Ghosh, 2000, Lin et al., 2001, Wade et al., 2001, Zhang et al., 2001, Zribi et al., 2001, Amagai et al., 2002, Joo and Yu, 2002, Kanchanomai et al., 2002a, Kim et al., 2002c, Kim et al., 2003,

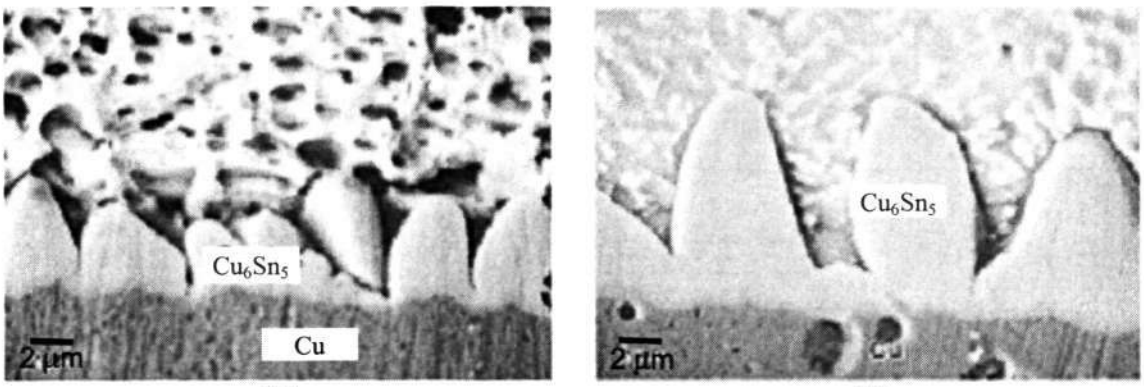
Kanchanomai and Mutoh, 2004, Wu et al., 2004, Sun et al., 2005)) pointed out that the microstructure strongly influences the fatigue resistance and other mechanical properties of a solder alloy. As a whole, the solder microstructure is determined by the solidification behavior of the solder and the reaction at the solder and base-metal interface. If the solder is used at a high homologous temperature, as it ordinarily is, the microstructure may evolve during service.

2.7.1 Intermetallic Reactions between Metallizations and Solder Joints

The interaction between the solder and bonding surface such as Cu substrate and other surface finishes will significantly affect the strength of the solder joint. The addition of impurity causes a completely new crystalline phase to be formed. These new phases are normally referred to as IMCs. The formation of thin IMC layer due to reaction between the solder and substrate during device fabrication, is desirable to achieve a good metallurgical bond, nevertheless excessive IMC growth may have a deleterious effect. Often, the IMC layer is brittle in nature, and moreover, its microstructure differences from the solder and the substrate makes the situated in the both sites of the IMC layer more sensitive to stress. These will make the crack initiation and propagation much more easily at the IMC layer and make it prone to mechanical failure under relatively low load (Tu et al., 1997, Miric and Grusd, 1998, Chan et al., 2001, Lin et al., 2001, Zhang et al., 2001, Amagai et al., 2002, Lu et al., 2005). Therefore, it is necessary to study the interfacial reaction and formation mechanism of IMC layer.

2.7.2 Kinetic Analysis of Soldering Reaction

Kim et al. (Kim et al., 1995) have observed a very unusual morphology of the growth of the interface Cu-Sn IMC grain in soldering reaction. The growth of interface Cu-Sn IMC is not in typical layer form but has a scallop-type appearance as shown Figure 2.8, and is accompanied by Ostwald ripening reaction among the scallops. They (Kim and Tu, 1996) pointed out that, the growth of the scallop-like grains is supplied by two fluxes of Cu atoms: the flux of interfacial reaction and flux ripening.



(a) (b)

Figure 2.8 Scallop-like morphology of Cu-Sn IMC at the interface of solder/Cu for (a) Sn-Pb (b) Sn-Ag solder (Kim and Tu, 1996)

Cu

To consider the flux of Cu atoms due to the ripening reaction between scallop-like Cu_6Sn_5 grains, it is assumed that the grain is a hemisphere. Due to the curvature difference, the concentration gradient of Cu is set up in the molten solder between grains with different radii. That causes the ripening flux of Cu atoms going from the small grain to the larger grain, which permits the large grains to grow while the small ones shrink and disappear. Since the Cu_6Sn_5 grains are close together, and the mean separation between grains is smaller than the mean grain radius. Therefore, the

diffusion flux fields of adjacent grains will overlap, and the growth rate of grains will be dependent upon the grain-to-grain separation distances.

In order to obtain the ripening flux of Cu atoms between closer grains, they consider the i^{th} Cu_6Sn_5 grain and its nearest neighbors. Since the diffusion fields of Cu atoms between adjacent grains overlap each other, the tendency for dissolution or growth is determined mainly by the surrounding grains (Tu et al., 2003). For simplicity, they considered the ripening between the i^{th} Cu_6Sn_5 grain and one neighboring grain with mean curvature. Figure 2.9 shows the concentration variation between the i^{th} Cu_6Sn_5 grain and the mean grain. Although the Cu_6Sn_5 grains grow in spherical symmetry, the grains are dispersed only at the interface between solder and Cu in two dimensions. Therefore, they assumed a linear geometry of the system to determine the ripening flux.

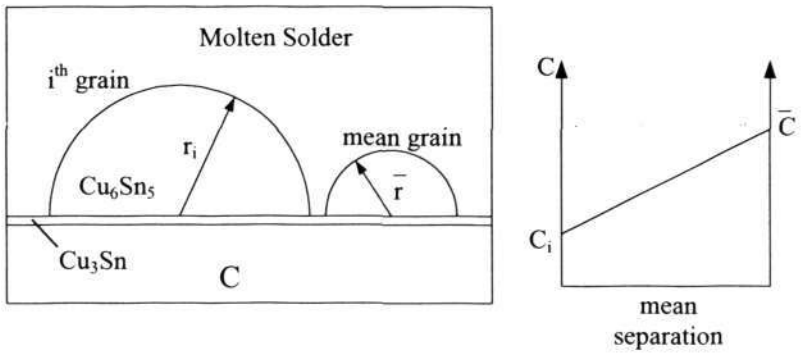


Figure 2.9 Schematic representation of the concentration variation between grains with different radius (Kim and Tu, 1996)

The ripening reaction between the Cu_6Sn_5 grains is not a constant volume process because it is accompanied by the interfacial reaction between the solder alloy and Cu. Between the Cu_6Sn_5 grains, there are molten solder channels extending nearly all the way to the solder/Cu interface (Kim et al., 1995, Kim and Tu, 1996). While a

thin layer of Cu_3Sn compound forms between the solder and Cu, the thickness of the layer is only in sub-micron size. Therefore, Cu atoms can diffuse through the Cu_3Sn and dissolve quickly into the molten solder through the channels between the Cu_6Sn_5 grains rather than through the Cu_6Sn_5 grains themselves. During the reaction, these channels serve as fast diffusion and dissolution paths of Cu in molten solder. However, because the Cu_6Sn_5 is not a layer compound, it cannot be the layer model to determine the flux of the interfacial reaction. In order to determine the interfacial reaction flux of Cu atoms, it was assumed that the total loss of Cu from the substrate is equal to the total amount of Cu dissolved through channels (Tu et al., 2002, Tu et al., 2003).

Finally, the growth of the scallop-like Cu_6Sn_5 grains in the soldering reaction of eutectic Sn-Pb on Cu is expressed as in equation [2.2] (Kim and Tu, 1996), which consists of fluxes of interfacial and ripening reactions. The first term on the right hand side of the equation is the ripening term, and the second term is the interfacial reaction term

$$r^3 = \int \left(\frac{\gamma \Omega^2 D C_0}{3 N_A L R T} + \frac{\rho \Omega A \nu(t)}{4 \pi m N_p(t)} \right) dt. \qquad [2.2]$$

where r is the grain radius for a Cu_6Sn_5 grain, C_0 is the equilibrium concentration of Cu in the solder, γ is the interfacial energy per unit area between Cu_6Sn_5 and molten solder, Ω is the molar volume of Cu_6Sn_5 , R is a gas constant, and T is the absolute temperature, D is the diffusivity of Cu in the molten solder, ρ is the density of Cu, A is the total area of the solder/Cu interface, m is the atomic mass of Cu, N_A is the Avogadro's number, $\nu = dh/dt$ is the consumption rate of Cu in the reaction, $N_P(t)$ is the total number of grains at interface, $L = \bar{\delta}/r$ where $\bar{\delta}$ is mean separation

between grains and since the mean separation between grains is smaller than the mean grain radius, $\bar{\delta} < \bar{r}$, the $\bar{\delta} < L\,r$, Where $0<L<1$.

Other growing kinetic in molten state, Jung and Conrad (Jung and Conrad, 2001b) has discussed about the growth kinetics of the Cu_6Sn_5 and Cu_3Sn IMCs in their study on the microstructure coarsening of Sn-Pb solder joint. The solid state growth of the IMCs during annealing was parabolic in form and was described by the equation

$$h = h_i + At^p = h_i + B\exp\left(\frac{-Q_a}{RT}\right)t^p \qquad [2.3]$$

where h is the thickness at time t, h_i the initial thickness, Q_a is the apparent activation energy, and B and p are constants. For a bulk diffusion growth process, one expects

$$h - h_o = \alpha\sqrt{Dt} \qquad [2.4]$$

where α is a proportional constant of the order of unity, and $D = D_o\exp(-Q/RT)$ is the diffusion coefficient.

Strict equivalence between equation [2.3] and [2.4] gives $p = 0.5$, $Q_a=pQ$ and $B = \alpha\sqrt{Dt}$.

2.7.3 Intermetallic Growth Mechanism

Other than the study on the growing kinetics and thickening process, the understanding of IMC growth mechanism has caught the attention of others (Jang et al., 1999, Chada et al., 2000, Guan et al., 2000, Young et al., 2001, Yoon et al., 2004, Kim et al., 2005b, Kumar et al., 2005, Magagnin et al., 2005, Yoon and Jung, 2005a, Yoon and Jung, 2005b). Study of Jang et al. (Jang et al., 1999) on the Sn-Pb/Ni-P reaction in

flip-chip assembly show that both Ni_3P and Ni_3Sn_4 grow with the increase of annealing time at temperature ranges from 200 to 240 °C. Their analyses show that the Ni_3P thickness versus square root time at various annealing temperatures displayed a linear relationship. This finding makes them to assume that the growth is controlled by a diffusion process. Guan et al. (Guan et al., 2000) have performed study on the effect of time on the IMC growth at the interface of 63Sn-37Pb, 40Sn-60Bi and 40Sn-58Bi-2Ag solder alloys and Cu substrate under aging at lower temperature, 90 °C and 120 °C. The aim of their study was to understand the IMC growth mechanisms involved in the aging environment. They pointed out that if the growth of Cu_6Sn_5 and Cu_3Sn was controlled by volume diffusion or by stationary boundary diffusion, the increase of the IMC layer during aging should follow the square root time law, $h \cong \sqrt{Dt}$. Where D is the diffusion coefficient and t is annealing time. The same assumption was made by Chada et al. and Young et al. (Chada et al., 2000, Young et al., 2001). Their work on the Sn-Ag/Cu, and Sn-Cu-Ni/Cu and Sn-Pb/Cu systems with the aging temperature at 100 °C, 170 °C, 226 to 292 °C. The IMC growth was also argued to be a thermally activated process and their data show that the $-\ln(D)$ vs $1/T$ for the IMC formation exhibit the linear relationship, where T is the dwell temperature.

In the later studies (Yoon et al., 2004, Kim et al., 2005b, Kumar et al., 2005, Yoon and Jung, 2005a, Yoon and Jung, 2005b), most of the research works were more on trying to understand the IMC growth mechanism of various lead-free solder systems through the characterization of the interface IMCs under various conditions. In one of the studies, Yoon et al. (Yoon et al., 2004) discussed about the interface reaction of eutectic 99.3Sn-0.7Cu lead-free with Cu substrate and Cu substrate coated with Au/Ni-P during reflow with different reaction time. Their later study (Yoon and Jung, 2005a) was to investigate the interface reaction between hypo-eutectic 99.6Sn-0.4Cu lead-free

solder with Cu substrate and Cu substrate coated electroless Ni immersion Au (ENIG) during aging at 150 °C. In Kim et al.'s work (Kim et al., 2005a), they focused their study on the formation and growth of IMCs at the interface between 96.5Sn-3.0Ag-0.5Cu lead-free solder and electroless Ni-P UBM. Scanning electron microscopy (SEM), electron probe micro analysis (EPMA) and Transmission Electron Microscopy (TEM) were employed to investigate the microstructure and phase analysis of their system. A less popular electroless Co-P immersion Au surface finish was proposed by Magagnin et al. (Magagnin et al., 2005) as a diffusion barrier for high Sn content solder. Magagnin et al performed the IMCs characterizations at the interface between this Co-P coating with both Sn-Ag-Cu and Sn-Pb solders. While the diffusion barrier properties of another more common surface finish, Au/Ni-P for the 96.5Sn-3.5Ag lead-free solder was investigated by Kumar et al. (Kumar et al., 2005). Kumar et al. reported that Au/Ni-P acts a good diffusion barrier for the 96.5Sn-3.5Ag lead-free solder during the reflow at 245 °C for 60 sec as well as during prolong annealing at 160 and 180 °C. However the diffusion barriers properties of this surface finish degraded at higher annealing temperature at 200 °C due to present of Ni-Sn-P layer.

2.8 Reliability of Lead-free Solder Interconnection

Solder joints reliability is one of the most critical issues in electronic package since the failure of solder joints results in the failure of the whole device. When an electronic device is in operation, the solder connections are subjected to mechanical stresses and strains that are mainly caused by the CTE mismatch between the component and the board. However, in the case of flip chip packages this will occur between the silicon die and the substrate. If room temperature represents the unstrained conditions, as the temperature of the system rises, the board expands more than the

component, resulting in the solder ball connection being subjected to shear strain. Moreover, as the system is switched "on" and "off" during operation, it is also subjected to thermal cycling. The combinations of these two conditions will cause the solder connections to develop cyclic shear stresses and straining which subsequently result in fatigue failure of the component. If the stress caused by CTE mismatch exceeds the yield stress of the solder material, plastic deformation will occur in the solder connection. The CTE mismatch can also result in a constant static loading on the solder connection. Since even room temperature is greater than $0.6T_m$ for most solders, this results in the solder connection being loaded under conditions where it can be susceptible to creep. Solder joint can also be subjected to tensile loading, typically when the board or substrate is in bending. This can happen during mechanical handling of the product, and sometimes when the finished product is clamped in the test fixtures for testing after assembly or even during transportation. Therefore, it is necessary to assess the reliability of the solder connection can withstand without failure.

2.8.1 Solder Fracture

To provide information which will lead to improvements in the reliability of the solder joints, a number studies have dealt with topics such as isothermal fatigue, creep-fatigue interaction, microstructural effects and thermal cycling behavior on both solder joints as well as bulk material (Akay et al., 1997, Choi et al., 2000, Zhao et al., 2001b, Kanchanomai et al., 2002a, Kanchanomai et al., 2002c, Pang and Low, 2002, Wu and Huang, 2002, Pang et al., 2004). Zhao et al. (Zhao et al., 2001a, Zhao et al., 2001b) reported that the fatigue loading will cause a significant reduction in grain size for both leaded and lead-free solders due to either to dynamic recrystallization or subgrain formation. They found that in the case of high stress ratio ($R \geq 0.5$) and low frequency,

intergranular crack path, microcracking along slip bands in grain and cavities, and microcracks along grain boundaries are observed in Sn-Ag solder. While at the low stress ratio ($R<0.3$), transgranular fracture is dominant, striation-like pattern are found.

A literature on creep phenomena for a few of lead-free solder alloys has been given by Igoshev and Kleiman (Igoshev and Kleiman, 2000). It is believed that at homologous temperature higher than about $0.4T_m$, grain boundaries represent a system of glide planes which generally become active simultaneously with crystallographic glide systems within the grain. Thus, under the action of applied stress, grain boundary sliding takes place and this naturally contributes to the plastic strain. The grain boundary sliding causes extreme heterogeneity of plastic deformation at temperatures where it takes place. This can lead to reduction in the polycrystal compatibility by formation of voids at grain boundaries if the grain boundary sliding is covered by the dislocation glide or by stress directed diffusion of vacancies; i.e. due to diffusion creep. When the polycrystal integrity is affected, the nucleation and, especially, the growth of grain boundary voids as cavities or cracks. The nucleation and growth of intergranular cavities finally leads to intergranular fracture typical of creep. The recent paper of Wade et al. (Wade et al., 2001) has reported that the largest creep rupture strength of Sn-Ag-Cu and Sn-Ag alloys can be attributed to the formation of the large fraction and volume of IMC particles, adversely, the relatively small creep-rupture of Sn-Cu alloy was caused by the sparse distribution of large rod-like precipitates.

2.8.2 Solder Joint Reliability

The reliability of electronic assemblies depends on the reliability of their individual elements, e.g., integrated circuit (ICs), active component, passive

component, PWB, connectors etc. On top of that, the reliability of the mechanical, thermal, and electrical interfaces between the elements is equally important in determining the overall reliability of the assembly. Reliability experience with electronic components has given rise to the "bathtub" reliability curve as shown in Figure 2.10 (Tummala, 2001), where the instantaneous failure rate (hazard rate) is plotted against the operating time in hours. The bathtub curve has three failure regions with distinct characteristics, which are associated with failures due to "infant mortality" or "early life failures rate (ELFR)", random failures in "steady state" operation or called the "intrinsic fail" region, and failure due to "wear out". Appropriate burn-in or environmental stress screening procedure can reduce the "infant mortality" failure (Tummala et al., 1997). Normal operation of mature product defines the low steady-state (random) failure region. The random steady-state region is characterized by a constant, or near constant, failure rate of mature assemblies in normal operation. The failure is of course, neither random nor steady sate and has meaning only in a purely statistical sense. The failure rate in this region is in part dependent on the complexity of the product. In the wear-out phase the accumulated damage from normal operation becomes large enough to cause rising failure rates. Without appropriate design attention, premature wear out failure can occur easily.

The reliability of the solder joint attachments of electronic components surface mounted to circuit board substrates requires explicit attention in the design phase as well as during manufacturing. Solder joints in use can be subjected to a variety of loading conditions that can lead to premature failure in inadequate designs. The loading conditions such as cyclic differential thermal expansion, vibration due to transportation and handling, thermal shock that caused by rapid temperature change during cooling from soldering operations or from severe use environments, and mechanical shock from

accidental misuse or severe use condition could exist either singly, sequentially, or even simultaneously. Even though vibration shock does occur in practical applications, it is the exceptions rather than the norm in terms of main cause failure. The failure mechanism of primary concern for the solder joint reliability is cyclic differential thermal expansion that results in fatigue damage.

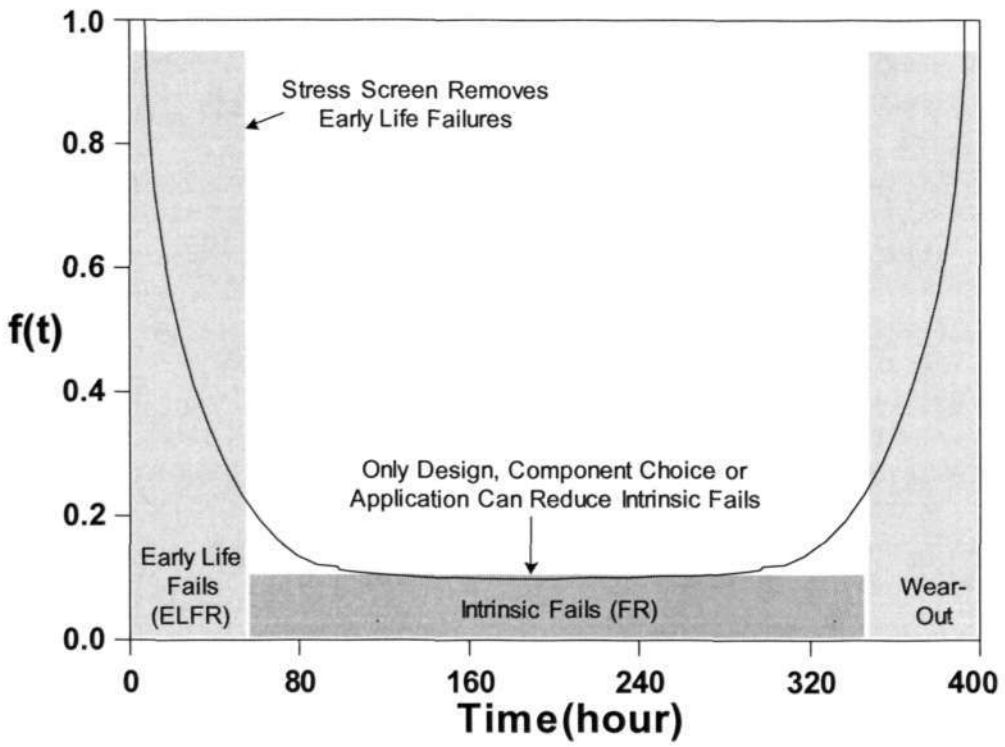


Figure 2.10 A typical "bathtub" curve representing a failure density function f(t).

2.8.3 Accelerated Test

Since thermal and mechanical reliability of solder joint in electronic packaging is one of the major issues that hinder the development of advanced packages towards small print and high density connections with robust reliability. Accelerated thermal cycling (Hou et al., 2001) method is widely adopted to validate the reliability of solder joints in various electronic products, such as consumer, computer, telecommunication, automobile, aerospace, etc. Thermal cycling provides reliability data with significantly simpler test arrangements. In functional cycling the shape of the cyclic waveform is defined by the thermal environment of the product, special care is necessary for thermal cycling to achieve proper test conditions. The cyclic waveform for the typical thermal cyclic (TC) test needs to have heating and cooling ramps rate below 30 °C/min. To simulate more stringent operating environment, the thermal shock (TS) test with higher cooling and heating rates was adopted. Other than the ramping rate, the waveform can have a significant effect on the dwell times at the temperature. The preferred waveform is trapezoidal because it is closest to actual use conditions and has well-defined dwell at the temperature extremes, but sinusoidal and even sawtooth waveform have been used. For sinusoidal waveforms, there is difficulty in determining the effective dwell time. While for sawtooth waveforms some stress relaxation and creep occurs during the up and down ramps, it is so small for all practical purpose with its zero half cycle dwell time for accelerated test of this nature. Thus, sawtooth thermal cycling is more akin to low frequency vibration than to thermal expansion mismatch fatigue. However, it is a relatively time consuming and expensive process and the testing process normally takes more than a month to complete. The competitive nature of the electronic packaging industry pushes companies to shorten the product development cycle while maintaining the highest level of reliability and quality. Hence, a highly accelerated testing method

that reduces the cycle time is greatly sought for the understanding of wear-out reliability characteristics of microelectronic packages.

Other than the thermal cyclic loading test, different accelerated isothermal mechanical cycling approaches were developed as alternatives to ATC. It should be noted that isothermal cycling excludes any effects of thermal cycling. The direct strain measurement (Kang et al., 2001) method was proposed by Xie (Xie et al., 1996) to obtain the fatigue performance data of solder joints for reliability analysis. In the approach a slit was cut in a PCB, and the uniaxial mechanical cycling strain was applied to the solder joint directly to simulate the un-slit PCB assembly subjected to thermal cycling. However, for this method with application to the advanced area-array Ball Grid Array (BGA) type packages is that the stress distribution around the solder joint is in multi-axial stress-state and cannot be simplified as pure shear like the peripheral leaded quad flat package (QFP) devices. Lau and Pao (Lau and Pao, 1997) established a three-point bending (TPB) methodology. The PCB was supported at both ends and mechanical loading was applied at the center of the PCB assembly. Load versus deflection graph was then plotted to determine the load where solder joint failure occurs. Since the failure mechanism is over-stress and not wear-out, this method is more applicable to simulate manufacturing, handling, shipping, and rework conditions. Recently, some research efforts (Sealing and Dasgupta, 1999, Sharma et al., 1999) have been tried to develop the accelerated vibration method. However, the creep response of solder alloy under the high frequency excitation loading is quite different from that obtained under the low frequency ambient temperature loading. In contrast, the mechanical deflection system (MDS) shows better potential alternative to ATC, because this mechanical approach is capable of accelerating solder joints failures to within days instead of months. Most importantly, MDS is meant to mimic solder joint

failure mechanisms similar to those from the ATC tests. This method was first proposed by Zubelcwicz (Zubelewicz et al., 1995) and developed by Pang et al (Pang et al., 1999) and this testing methodology was only established for the purpose of assessing the reliability of solder joints in the plastic QFP devices. However, there is still lacks of fundamental study and failure analysis on the lead-free solder interconnection, subjected to thermal cycling, isothermal and thermal loadings.

Chapter 3: Materials and Experimental Procedures

3.1 Materials

Two types of lead-free solders, Sn-Ag-Cu and Sn-Cu were studied in this project. However, Sn-Ag-Cu lead-free solder was the major focus of this project. The Sn-Ag-Cu lead-free solder was studied in three different conditions: cast-extruded bar, solder ball and solder paste. The Sn-Cu lead-free solder was studied in the cast-bar condition only. Chemical compositions of the solders are listed in Table 3.1.

Table 3.1 Chemical compositions of the lead-free solders used

Solder Form	Chemical Composition (Wt%)		
	Sn	Ag	Cu
Cast-bar	99.3	-	0.7
Cast-extruded bar	95.5	3.8	0.7
Solder Ball	95.5	3.8	0.7
Solder Paste	95.8	3.5	0.7

3.2 Annealing of Bulk Solder

3.2.1 Annealing Temperature and Time

The ternary 95.5Sn-3.8Ag-0.7Cu cast-extruded lead-free solder bar was used for the annealing or aging study. The study was carried out at three annealing temperatures 60, 125 and 190 °C (at an interval of 65 °C). The lowest annealing temperature at 60 °C is low enough not to cause any significant thermally activated mechanism such as creep to occur. 125 °C is the peak temperature for most of reliability test for the electronic components. The highest annealing temperature of 190 °C is about 30 °C below the melting point of this 95.5Sn-3.8Ag-0.7Cu lead-free solder that ranges from 217 to 219

°C. The highest temperature used is relatively high but it is not expected to result in significant creep due to absence of external load. The annealing time was fixed to one hour for annealing at 60 and 125 °C. While at 190 °C, the annealing time was in the increment of the power of two; 1^2, 2^2, 3^2, 4^2 and 5^2 hours.

The as-received cast-extruded bar was sectioned into blocks of 25 mm × 15 mm × 15 mm size. The blocks were subjected to annealing in Memmert UM300 oven. The oven was allowed to stabilize at the required temperature before putting in the specimen for annealing. When the required annealing time was reached, the oven was switched off and the specimen was allowed to cool naturally in the enclosed chamber to the room temperature.

3.2.2 Metallographic Preparation

The annealed samples were sectioned as shown in Figure 3.1 to study the microstructures in both longitudinal and transverse directions. The specimens were cut using the precision diamond coated narrow gauge low speed circular saw. Lubricant was supplied continuously during cutting to minimize excessive deformation on the specimen.

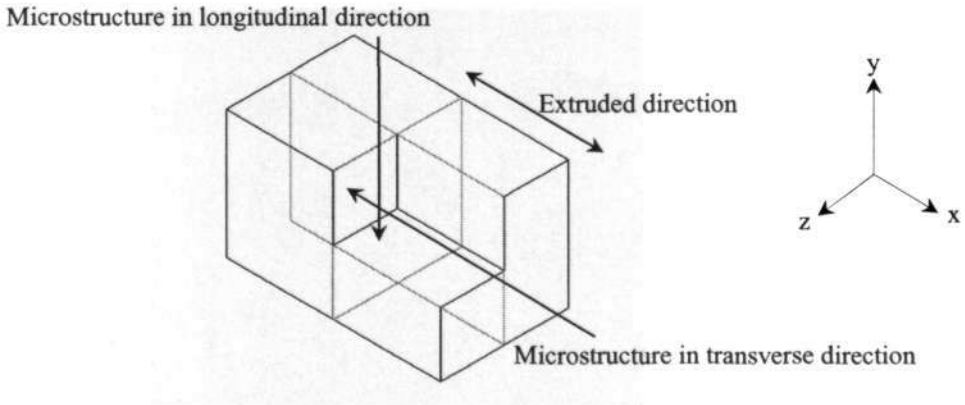


Figure 3.1 Sectioning of cast-extruded bar for study of microstructures

The specimen was then cold mounted using room-temperature curing resin. Cold mounting was used to prevent the effect of heat induced during the normal hot mounting process. The cured specimen was ground with silicon carbide paper of grits 180 to remove the deformation layer on surface. Only the core of the specimen was used for microstructure observation.

After the mass material removal, the specimen was coarse ground with 400, 600, 1000 and 1200 grits of silicon carbide paper to obtain parallel and flat surfaces. Careful cleaning of the specimen was performed in between steps to prevent cross contamination of the abrasive particles.

After fine grinding process, the specimens were polished with 3 μm diamond suspension at a constant rotating speed of 150 revolutions per minute. At this stage, frequent visual inspection is required to determine the progress of the polishing. The surface of the specimen should be free from embedded silicon carbide from the previous grinding processes.

After removing most of the embedded particles, the specimens were further polished using 1 and 0.3 μm alumina suspension at a constant rotating speed of 150 revolutions per minute. Slight pressure was applied at the beginning of 1 μm polishing stage to further remove remaining embedded silicon carbide and diamond particles.

The specimen was etched with 5 parts HCl 37% in 95 parts methanol for 5 to15 sec. The microstructures of the specimens in both transverse and longitudinal directions were examined using the optical microscope.

3.3 In-situ Observation of IMC Growth in Bulk Solder

The 99.3Sn-0.7Cu lead-free solder bar was sectioned into blocks of 10 mm × 12 mm × 5 mm in size. The block was ground to about 3 mm thick and polished to 0.06 μm finish using colloidal silica suspension.

It is challenging to carry out in-situ observation of IMC growth. Great effort was therefore made to equip an optical microscope with Linkam THMS600 heating stage and Linkam TMS93 temperature controller, making it possible to observe the change of IMC sizes directly while the solder sample is being heated. Figure 3.2 shows the set-up of the system. The temperature was controlled to 210, 215 and 220 ºC for the study. The very high temperatures were used for the purpose of completing the experiments within a day.

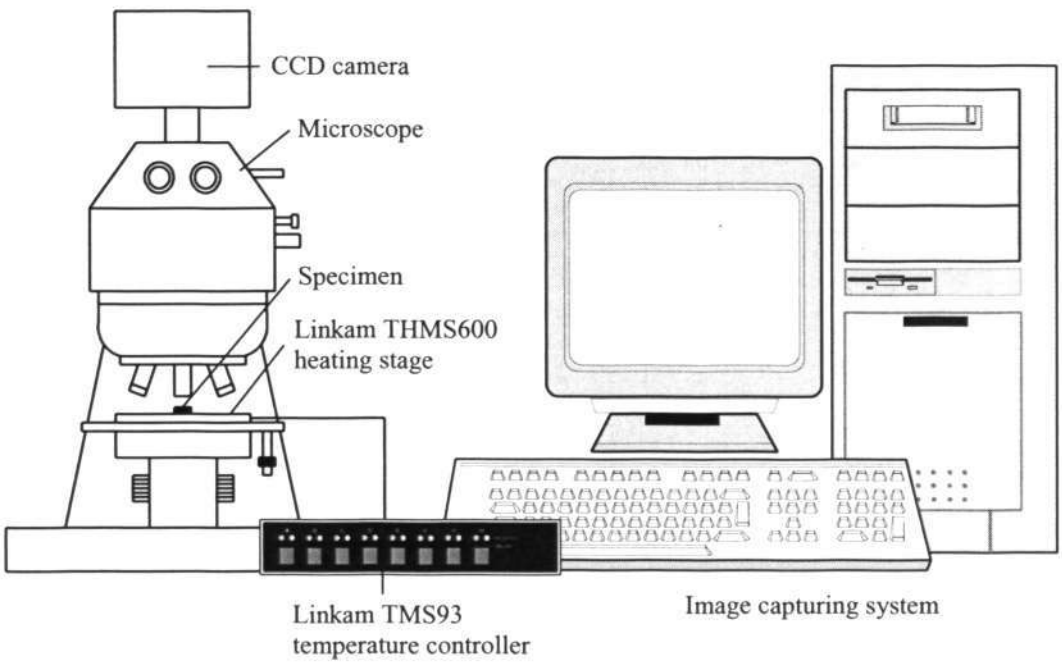
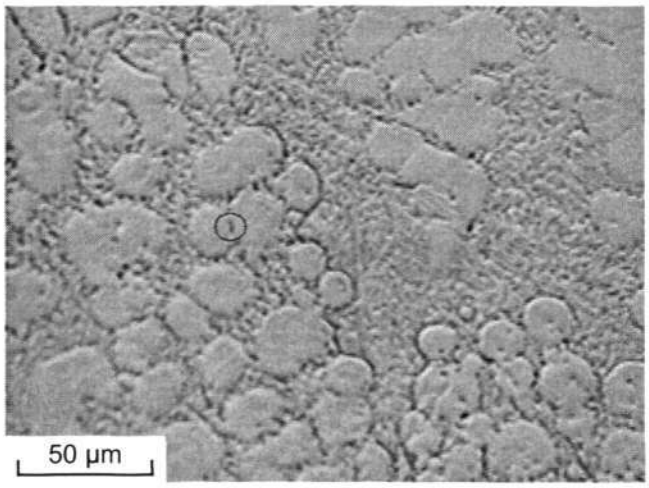


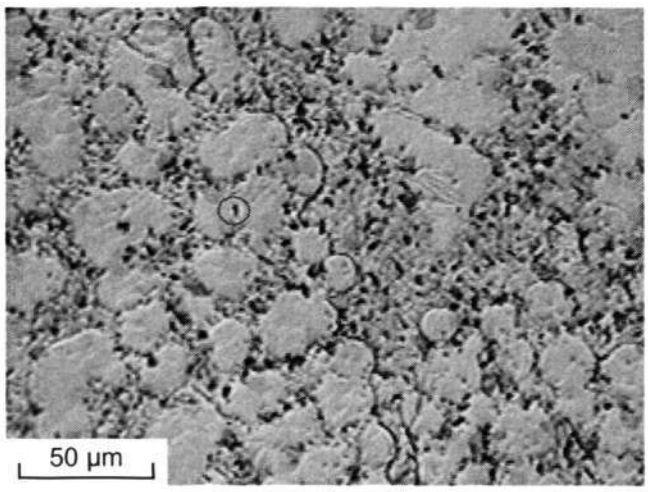
Figure 3.2 Illustration of the optical microscope system equipped with Linkam THMS600 heating stage and Linkam TMS98 temperature controller.

The specimen was heated using the Linkam THMS600 heating stage placed under the optical microscope with video capturing software. The microstructure on the same area of the specimen was observed in-situ with a CCD camera and the digitized images were recorded. A few optical micrographs obtained in the in-situ observation are shown in Figure 3.3 to demonstrate how the technique can be used to monitor the evolution of IMC particles.

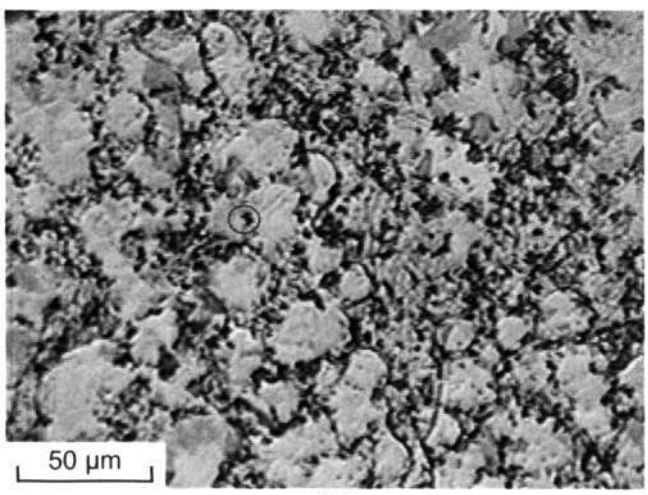
Since much longer time is needed to complete the experiment at lower temperatures 190 and 200 °C, ex-situ observation of IMC growth was performed. For ex-situ IMC growth observation, the specimen was heated in the Lenton WHT6/30(0) oven, and the same area of the specimen was observed at different heating time intervals to monitor the evolution in microstructures.



(a)



(b)



(c)

Figure 3.3 Optical micrographs showing the evolution of microstructure in 99.3Sn-0.7Cu. (a) microstructure in as-received condition; (b) and (c) microstructure of the same area after being heated at 215 ºC for 40 min and 97 min showing coarsening of IMCs (one of them is circled).

3.4 Isothermal Aging of Solder/Copper Joint

A solder/copper joint specimen, as shown in Figure 3.4, was formed by soldering two pieces of L-shaped Cu sheets. The soldered surfaces of the Cu sheets were coated with about 2 to 3 μm of electroless Ni and about 0.06 μm of immersion Au (ENIG coating layer). Two Cu sheets were placed in the stainless steel fixture and aligned with the guiding stainless steel blocks as shown in Figure 3.5. Solder paste was applied in between the gap where the two Cu sheets were overlapped. The solder paste used was 95.8Sn-3.5Ag-0.7Cu (brand name is KESTER 905/11%). The fixture was put on a ceramic plate and reflowed in the HELLER 1800 Reflow oven. The reflow profile is as shown in Figure 3.6.

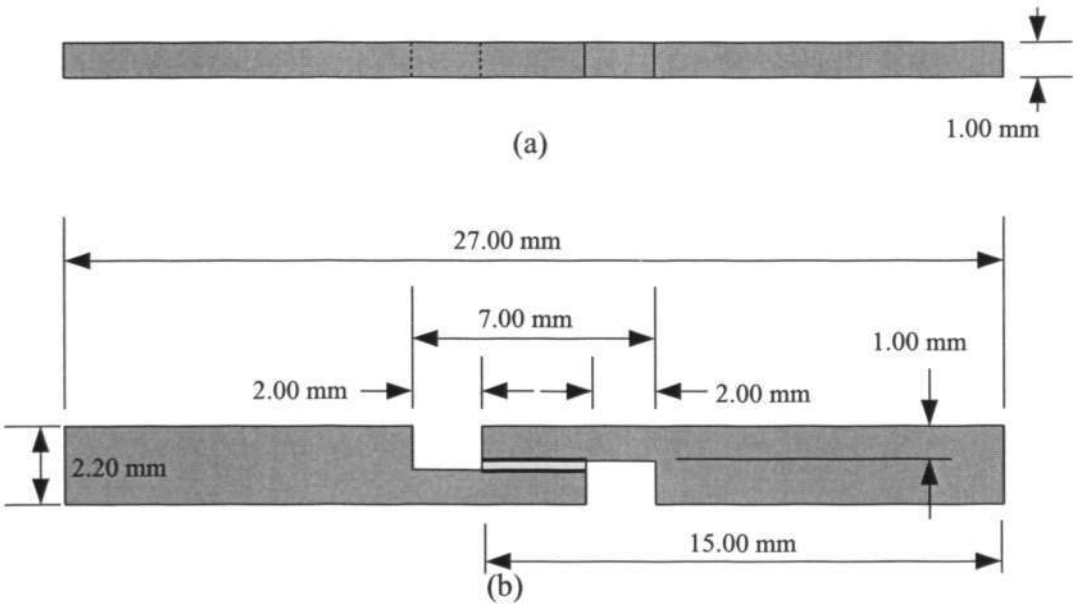


Figure 3.4 The schematic diagram of the solder/copper joint specimen (a) plane view and (b) side view

After reflow, the specimen was ground with silicon carbide paper to remove the excessive solder at the joining portion. The solder/copper joint specimens were isothermally aged in Lenton WHT4/120 oven at 125, 150 and 175 °C for 24, 72, 144

and 336 hr. When the required aging time was reached, the specimen was taken out from the oven and allowed to cool to the room temperature.

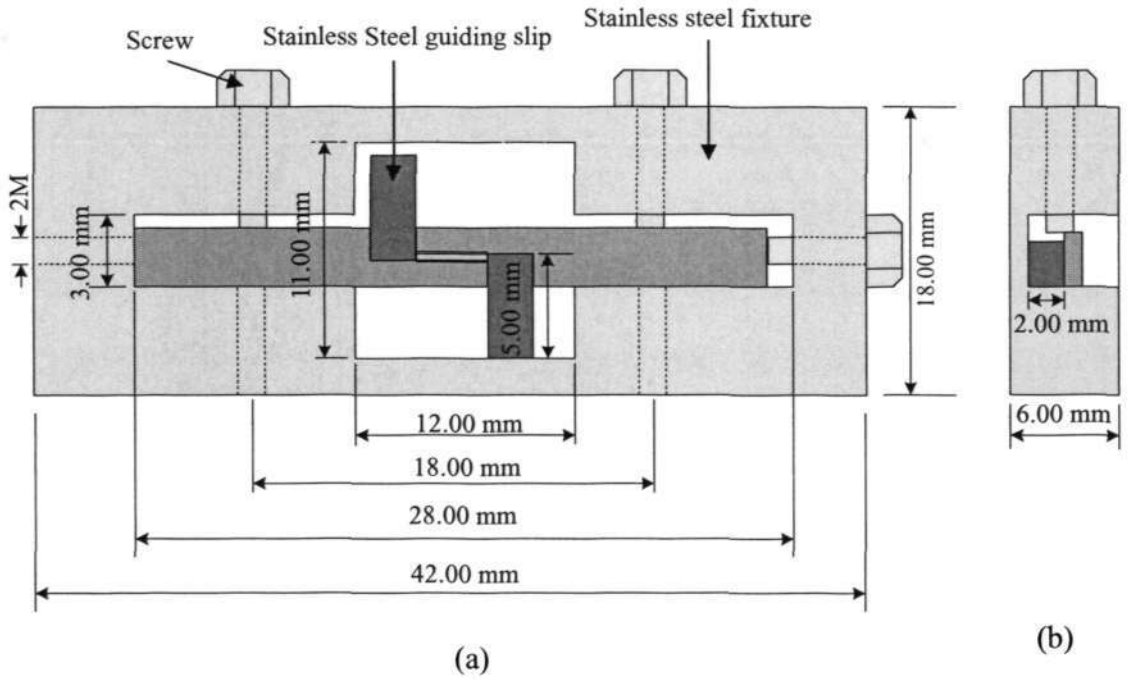


Figure 3.5 The schematic diagram of the stainless steel fixture used to align the solder/copper joint specimen during reflow process. (a) plane view and (b) side view

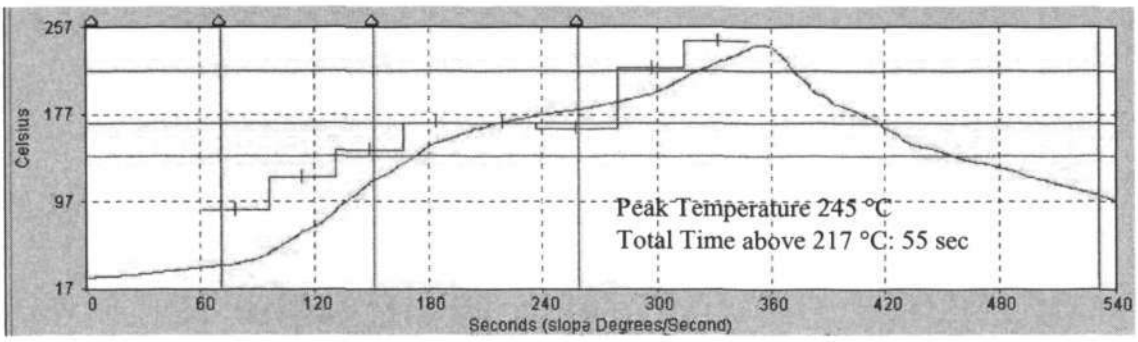


Figure 3.6 Reflow profile for solder/copper joint specimen

The common metallographic practice as described in section 3.2.2 was carried out for the aged specimens. The specimens were observed using JEOL JSM – 6340F

Field Emission Scanning Electron Microscopy (FE-SEM) and the composition of each phase was investigated by Energy Dispersive X-ray (EDX) microprobe analysis.

Tensile testing of the solder joints was carried out using a microtensile tester. The microtensile tester was installed inside a scanning electron microscope to make it possible to carry out in-situ observation of the deformation and fracture processes. Both as-reflowed and thermally aged joints were used in the study.

3.5 Thermal Cycling and Thermal Shock Aging of FR-4 Solder Joint

The FR4-solder joint specimen, as shown in Figure 3.7, was formed by soldering a single solder ball to two FR-4 substrates printed with Cu pad coated with Ni/Au. The FR-4 substrate was cut into small pieces of 13 mm × 4 mm × 0.32 mm in size. A 95.5Sn-3.8Ag-0.7Cu lead-free solder ball with diameter of 0.5 mm was placed and secured with no-clean flux to the substrate. No-clean flux also helps to remove contamination and prevent oxidation during reflow process.

The FR4-substrate with the solder ball attached was put through the HELLER 1800 Reflow oven for the first reflow process. The reflow profile is shown in Figure 3.8. After the first reflow, the other piece of FR4-substrate was aligned to the reflowed solder ball with no-clean flux and subjected to a second reflow process. The fabrication process of the FR4-solder joint specimen is illustrated in Figure 3.9.

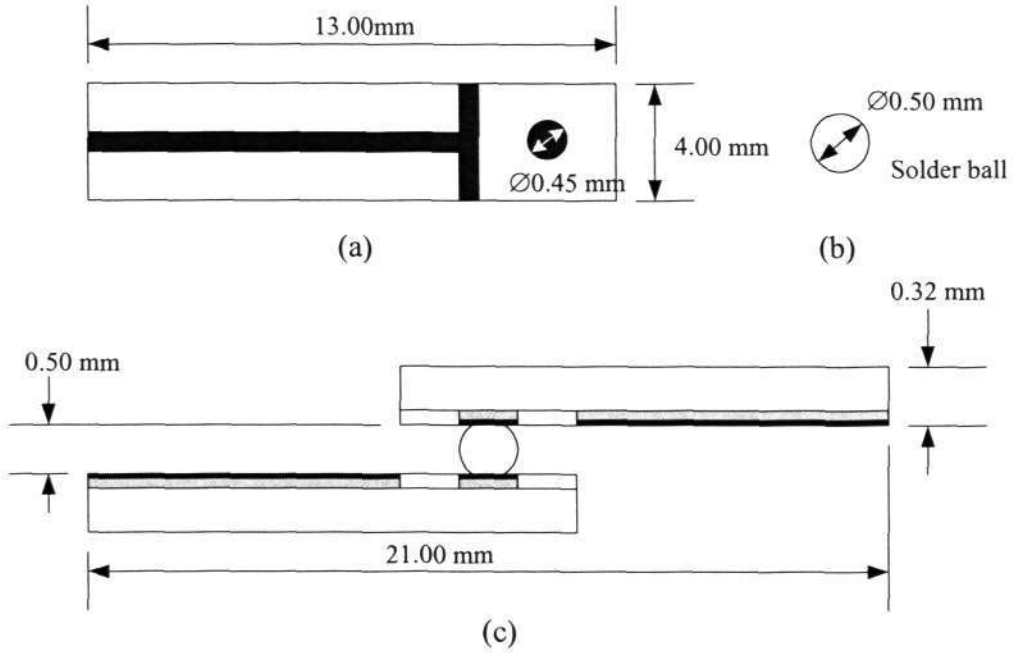


Figure 3.7 Schematic diagram of the FR4-solder joint specimen. (a) The FR4-substrate with Cu pad coated with Ni/Au. (b) 95.5Sn-3.8Ag-0.7Cu solder ball (c) FR4-solder joint specimen.

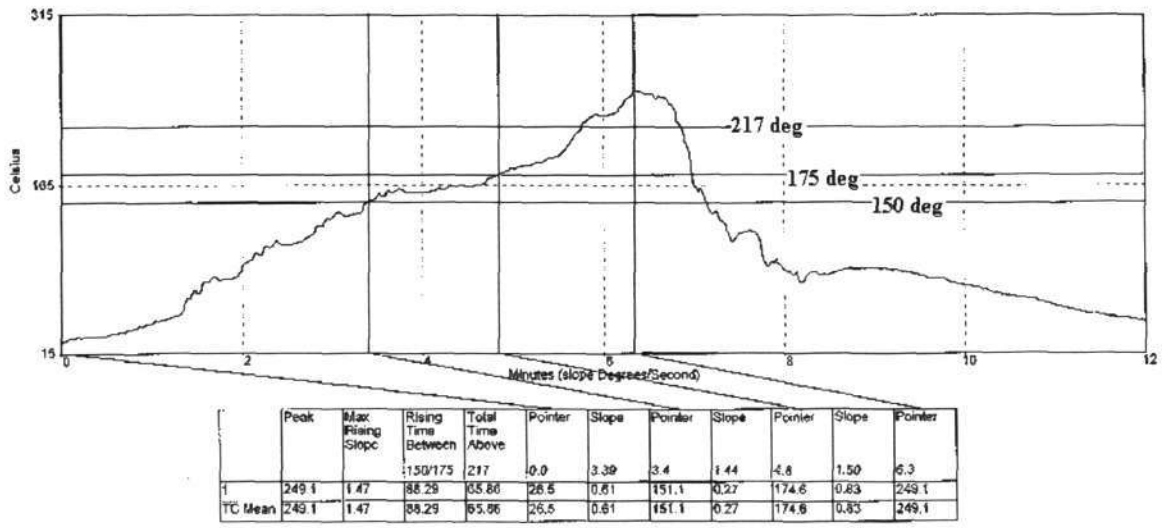


Figure 3.8 Reflow profile for FR4-solder joint specimen

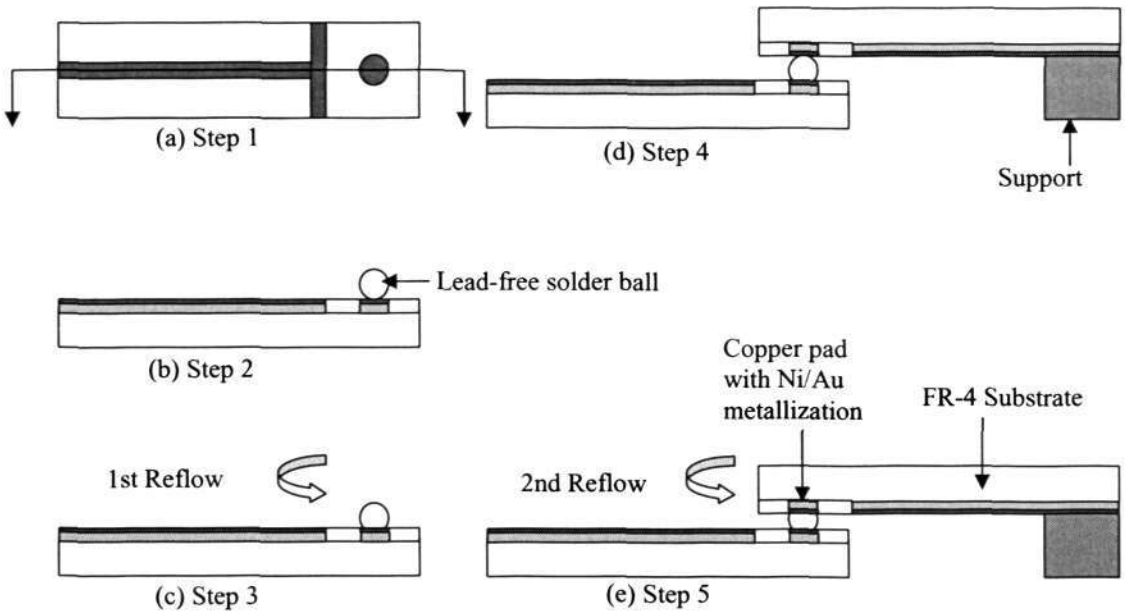


Figure 3.9 Schematic diagram showing fabrication process of FR4-solder joint specimen. (a) The FR4-substrate was sectioned into smaller pieces. (b) Solder was placed and secured on the Cu pad coated with Ni/Au with no-clean flux. (c) The FR4-substrate with solder ball attached was subjected to the first time reflow. (d) The other FR4-substrate was aligned to the reflowed solder. (e) The FR4-solder joint specimen was formed through the second reflow.

For the thermal cycling aging (TC), the specimens were put into the WEISS cycling chamber for aging up to 500, 1000 and 2000 cycles. A cycle of TC was 56 min and temperature varied from -40 to 125 °C. The temperature ramp rate was about 12.7 °C min^{-1} to the maximum temperature of 125 °C. After holding the specimen at the maximum temperature for 15 min, the temperature was lowered down at the same rate to the minimum temperature of -40 °C. The specimen was held at the minimum temperature for another 15 min and then the next cycle started. The TC profile is shown in Figure 3.10 together with the profile for the thermal shock aging (TS).

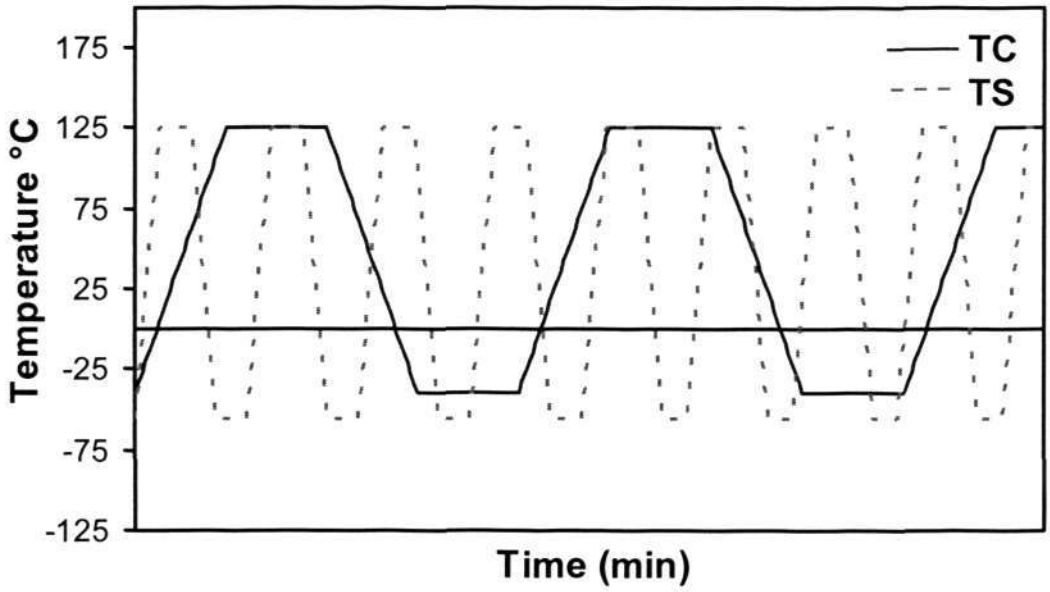


Figure 3.10 Temperature profiles for TC and TS

TS was conducted using the Vötsch Industrietechnik VT 7012 S3 cycling chamber. As shown in Figure 3.10, a cycle of TS was 17 min with temperature varied from -55 to 125 °C. The lowest temperature used for TS is -55 °C instead of -40 °C as used for TC, because it is the common microelectronic industry practice to use the two different lowest temperatures for TC and TS. The temperature ramp rate was fixed at 51.4 °C min^{-1} and holding time at the maximum and minimum temperatures was 5 min.

3.6 IMC Thickness Measurement

The average thickness of the interface IMC was determined using digital imaging techniques. The area and the length of the IMC layer in projection direction X were defined using the Imaging System Analysis 3.2 Software. The process of the IMC thickness measurement is illustrated in Figure 3.11.

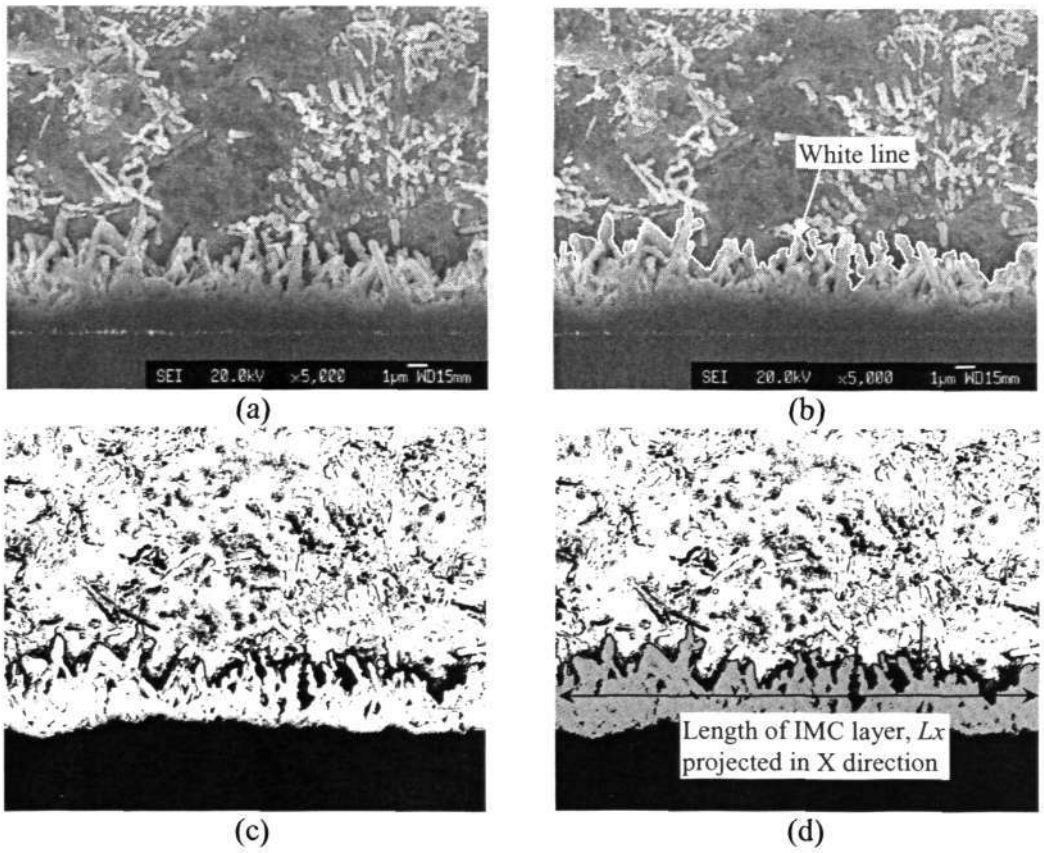


Figure 3.11 SEM image showing the microstructure across the solder/coating interface (a) prior to editing; (b) with interface IMC layer outlined with white line; (c) with "enrich" contrast. (d) The IMC layer (shaded area) was used for thickness calculation.

The thickness of IMC is never even along the interface. Therefore, an average value of thickness has to be used in the study of IMC growth. The average thickness can be calculated using equation [3.1],

$$\bar{h} = \frac{\sum_{i=1}^{n} h_i}{n} \qquad [3.1]$$

However, in reality, it is impractical to measure thickness of each individual IMC for the calculation. In the project, a much easier method was used to estimate the average IMC thickness by calculating the thickness as the area of IMC (A) divided by

the projected length of the IMC along the interface direction (L_x), as shown in equation [3.2],

$$\bar{h} = A / L_x \qquad [3.2]$$

3.7 Study of Stress Effect on IMC Growth

3.7.1 C-ring solder Joint Specimen Preparation

The substrate used in this study was a commercial pure Cu with chemical composition as given in Table 3.2. The Cu substrate was machined into an open ring in the shape of letter C and two holes were drilled in the lower and upper ends of the C-ring, as schematically shown in Figure 3.12. This specially designed C-ring makes it possible to apply in-plane tensile and in-plane compressive stresses easily, as described later. After machining, the C-ring was polished with 1 and 0.3 μm alumina suspension to achieve good surface finish.

Table 3.2 Chemical composition of commercial pure Cu bar

Chemical composition of material (Wt%)	
Cu	>=99.90
O	0.0125
Ag	0.0025
S	0.0006

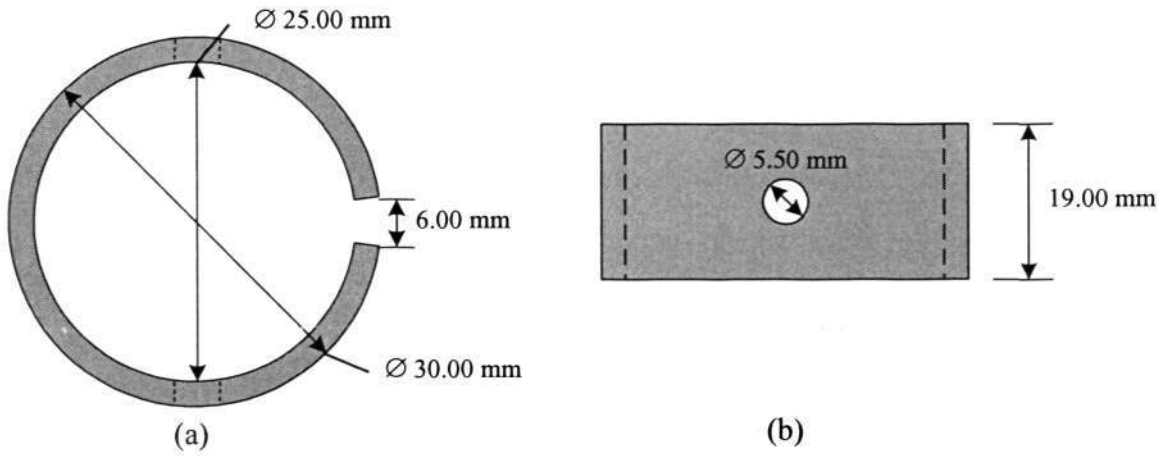


Figure 3.12 Geometric dimensions of C-ring specimen. (a) Side view. (b) Plane view

Four types of surface finishes were used in this study: (a) the bare Cu substrate (without any coating); (b) Cu substrate coated with electroless Ni plating and immersion Au (ENIG); (c) Cu substrate coated with immersion Sn; and (d) Cu substrate coated with electroless Ni/Pd plating and immersion Au (ENEPIG).

The ENIG plating process was performed in laboratory scale. ENIG plating process started with soaking the C-ring specimen in 8 parts sulphuric acid in 92 parts deionized water for 20 min to remove the organic residues. Next, the C-ring was immersed in the mildly agitated mico-copper etchant at 50 ºC for 1 min. This etching process helps to produce uniform surface texture for further processing.

After rinsing with deionized water, the C-ring was immersed in the ruthenium (Ru) activation chemical with pH level of 0.8 at 85 °C for 3 min. The Ru layer acts as an initiation layer for the subsequence Ni plating. For Ni plating thickness to about 3 μm, the C-ring was immersed in the low phosphorous electroless Ni solution at 91 ºC with pH level at 4.5 for 20 min. Lastly, the C-ring was submerged into the immersion Au plating solution at 75 °C with pH level at 7 for about 10 min for Au plating about 0.06 μm thick.

Plating of Immersion Sn and ENEPIG were conducted by a plating company according to industry mass production scale. The plating process flows are shown in Figures 3.13 and 3.14 respectively. Thickness of the immersion Sn ranges from 0.8 to 1.2 μm. Thickness for the electroless Ni, Pd and immersion Au layers ranges from 5 to 8 μm, 0.3 to 0.6 μm and 0.03 to 0.08 μm respectively.

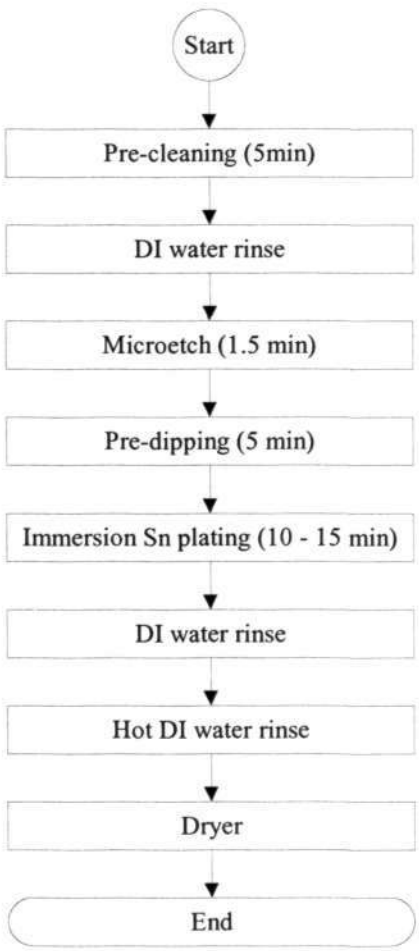


Figure 3.13 Flow chart showing process for immersion Sn plating

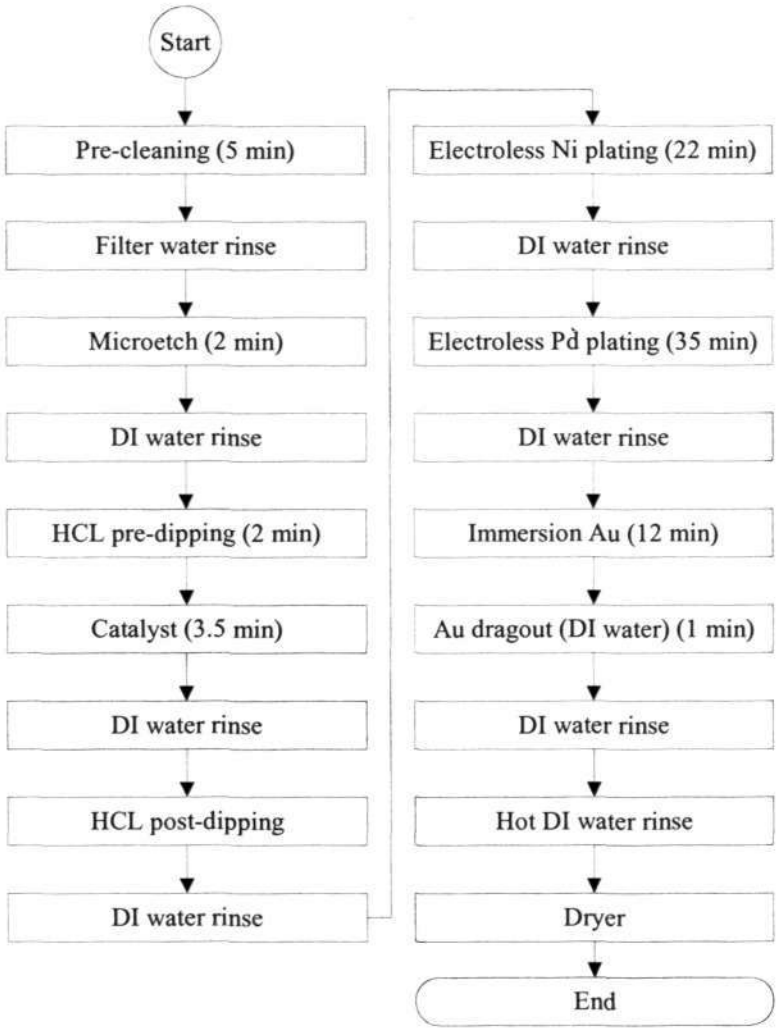


Figure 3.14 Flow chart showing process for ENEPIG plating

The solder/coating diffusion couples were formed by soldering the 95.8Sn-3.5Ag-0.7Cu solder paste on the C-ring using the HELLER 1800 Reflow oven. The heating profile is shown in Figure 3.15.

The regions where the diffusion couples to be formed were enclosed using thermal tape as shown in Figure 3.16. Solder paste was applied within the enclosed regions for C-ring coated with ENIG, immersion Sn and ENEPIG. Additional pre-cleaning process was used to remove the oxide layer on bare Cu C-ring before applying the solder paste.

The bare Cu C-ring was first soaked in 8 parts of sulphuric acid in 92 parts deionized water for 20 min to remove the organic residues. Next, a chemical polishing process was performed by immersing the Cu C-ring in the mildly agitated Iron (III) chloride solution the micro-copper etchant at 50 ºC for 1 min. This micro etching process helps to remove the oxide layer and to level the surface of Cu C-ring.

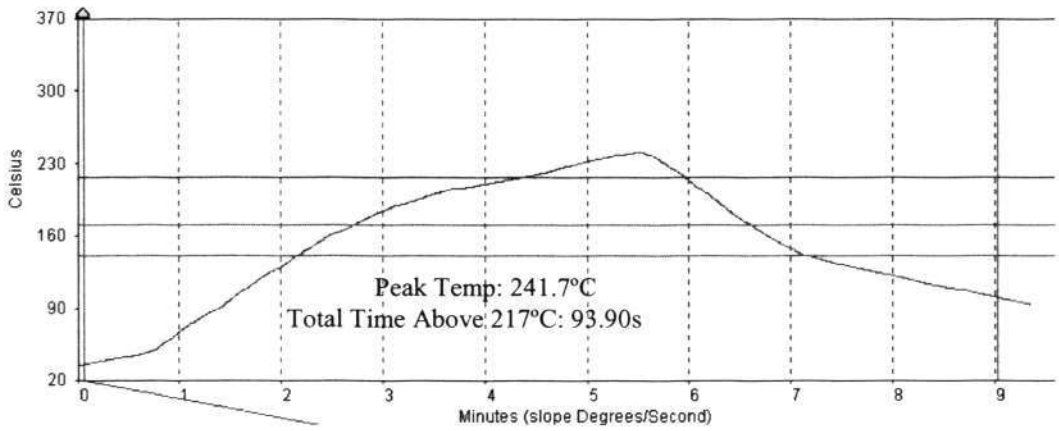


Figure 3.15 Reflow profile for the C-ring Solder joint

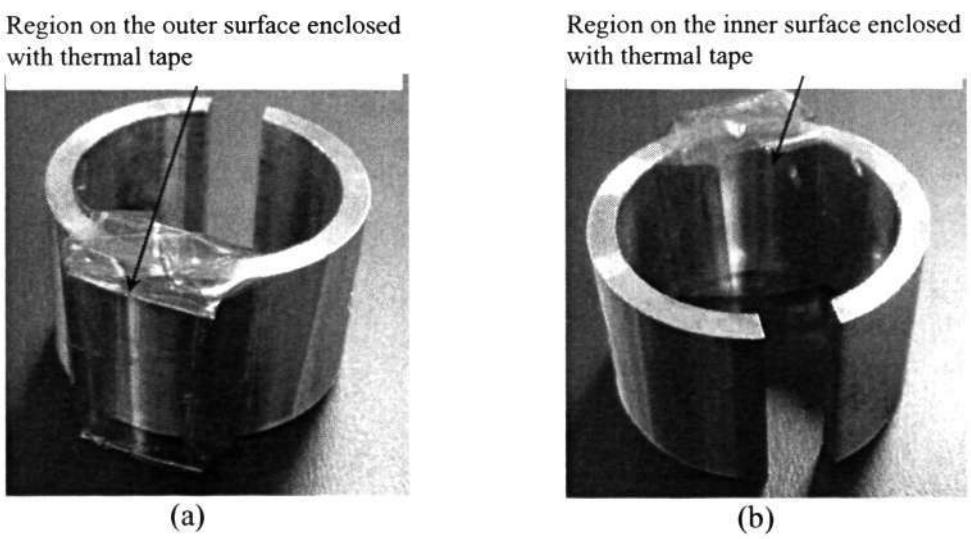
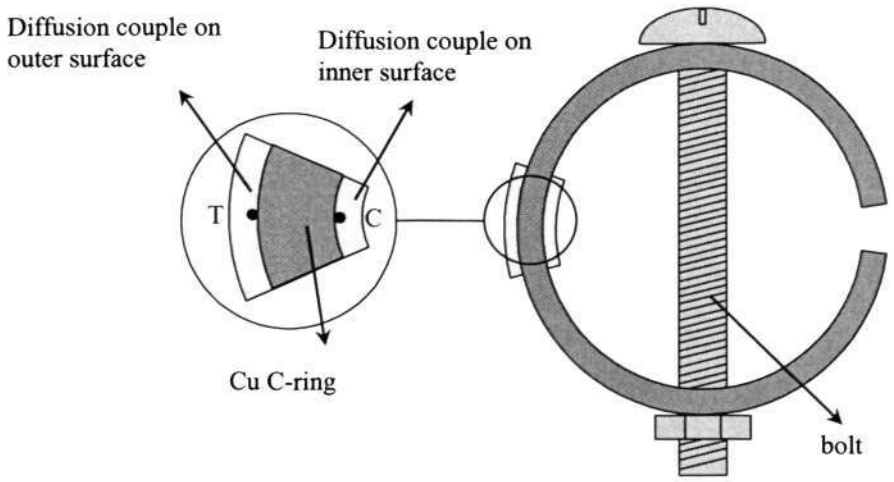
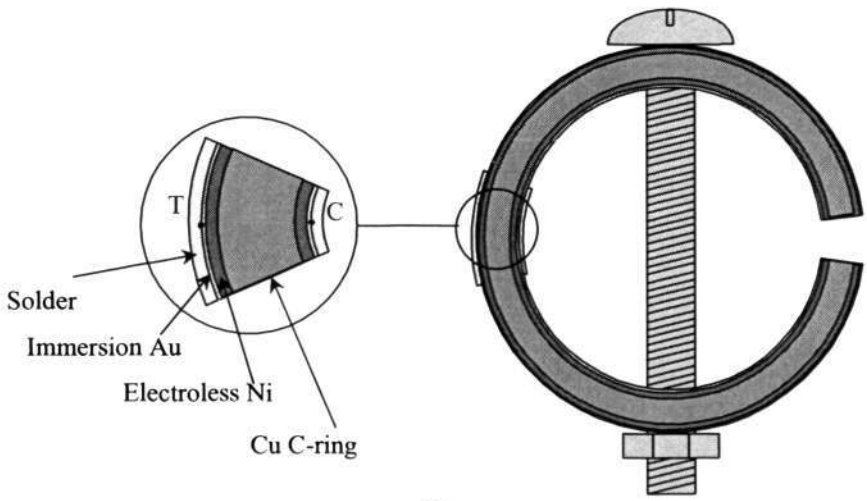


Figure 3.16 Photographs showing the center region on both the (a) inner and (b) outer surfaces enclosed with thermal tape.

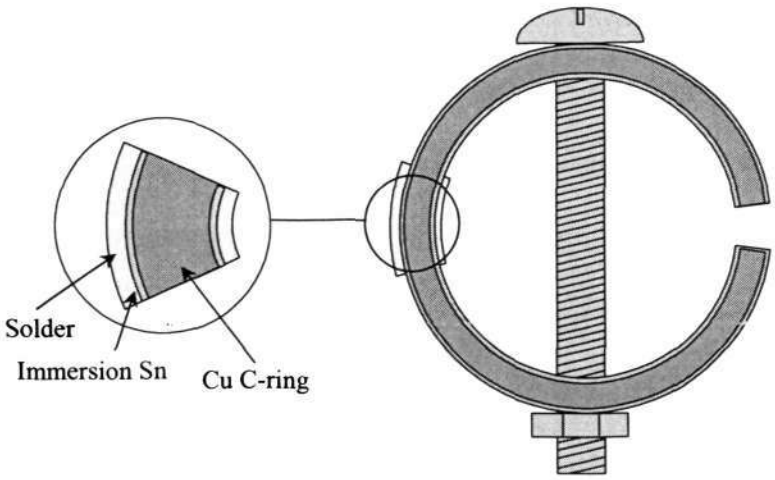
The schematic diagrams of the C-ring solder joint with the four different types surface finishes are show in Figure 3.17. The positions of the solder/coating diffusion couples were located at regions where the maximum in-plane tensile and in-plane compressive stresses were exerted when stress was applied through tightening the bolt, as indicated as points T and C in Figure 3.17(a).



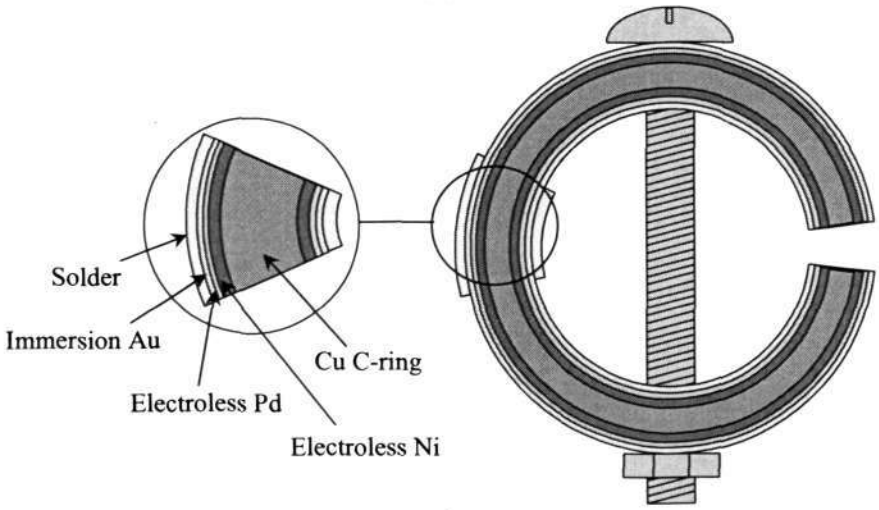
(a)



(b)



(c)



(d)

Figure 3.17 Schematic diagram showing C-rings with four different surface finishes. (a) bare Cu; (b) ENIG coated; (c) immersion Sn coated; and (d) ENEPIG coated. In-plane tensile and compressive stresses are exerted on the inner and outer diffusion couples by tightening the C-ring with a bolt.

3.7.2 Determination of Applied Stress Level

The applied stress level (f) depends on the amount of reduction in C-ring diameter (Δ) as given in a formula specified in ASTM G38:

$$\Delta = \frac{f\pi D^2}{4EtZ} \qquad [3.3]$$

$$D_{of} = D_o - \Delta \quad [3.4]$$

$$D = D_o - t \quad [3.5]$$

where

D_o = outside diameter of C-ring before stressing, mm

D_{of} = outside diameter of stressed C-ring, mm

D = mean diameter, mm

E = Young's Modulus of C-ring, MPa

f = desired stress, MPa (within the proportional limit)

t = wall thickness of C-ring, mm

Z = a correlation factor for curved beams, as shown in Figure 3.18

Δ = reduction of D_o due to bolt tightening, mm

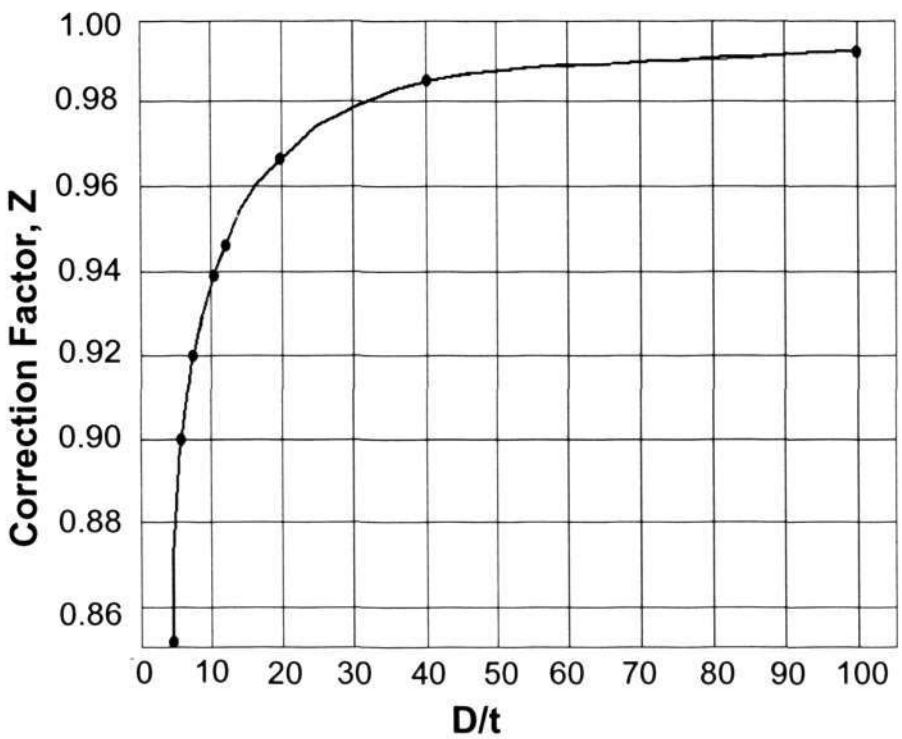


Figure 3.18 Correlation factor Z for curved beams (ASTM G38)

Equation [3.3] is applicable only if the applied stress level (*f*) falls within the proportional limit of the materials. Therefore, yield stress value of the solder was used to determine the equivalent maximum stress level (*f*) to be applied on the Cu C-ring.

For most metals that are stressed at a level below yield stress, the stress-strain relationship follows Hooke's law,

$$\sigma = E\varepsilon \qquad [3.6]$$

At the interface, solder and Cu substrate experience same amount of strain when the diameter of C-ring was reduced by tightening of the bolt. Therefore, the following relationship can be obtained,

$$\frac{\sigma_s}{E_s} = \frac{\sigma_{cu}}{E_{cu}} \qquad [3.7]$$

where

E_{cu} = Young's Modulus of commercial pure Cu, 130 GPa

E_s = Young's Modulus of solder at 125 °C, 26 GPa

σ_s = Yield stress of solder at 125 °C, 24 MPa

σ_{cu} = Stress applied on Cu C-ring

By considering the yield strength of solder, the maximum allowable applied stress on the Cu C-ring, σ_{cu} was estimated to be about 120 MPa according to the equation. However, the Cu substrate will yield at this applied stress level. Therefore, the maximum allowable applied stress is limited by yield stress of Cu, which is 69 MPa.

The C-ring solder joint specimen was annealed at 125 °C for 100, 168, 336, 1000, 2000 and 4000 hr at two stress levels of 25 and 50 MPa (note they are below the maximum allowable stress). These stress levels are the stress exerted on the Cu C-ring,

σ_{cu}. At these applied stress levels, the corresponding stress on the solder was calculated to be about 5 and 10 MPa respectively.

For the metallographic sample preparation, the C-ring solder joint specimen was ground with silicon carbide paper to remove about 1.5 mm thick of the material from the side surface. After this material removal, the C-ring specimen was prepared according to the common metallographic practice as described in section 3.2.2. The microstructure and chemical composition of the specimens were evaluated using the equipments and techniques described in section 3.4.

3.8 Study of Sn Whisker Growth Using Sn Coated C-ring

The Cu C-ring was plated with electrolytic Sn coating according to the industry mass production scale. Plating time of 15 min and current density of 2.6 Amp/dm^2 were used to produce the Sn coating layer of about 30 μm in thickness. The flow chart for the plating processes is shown in Figure 3.19.

The Sn whisker growth study was carried using both stressed (5 MPa) and unstressed (as-plated) C-rings either at room temperature and at 60 °C. The objective was to study effect of applied stress and temperature on growth of Sn whiskers. For room temperature condition, the specimen was stored in desiccator.

The regions of the specimen that subjected to maximum in-plane tensile and compressive stresses (Figure 3.20) were evaluated using JEOL JSM – 5600LV Scanning Electron Microscopy at different time intervals.

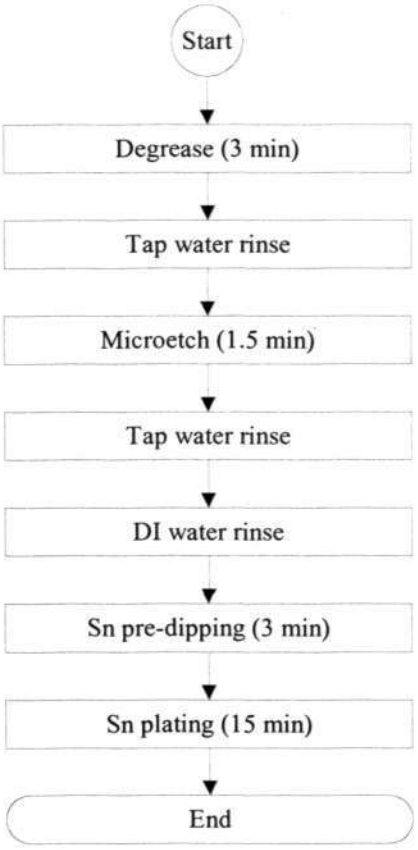


Figure 3.19 Flow chart showing processes for electrolytic Sn plating

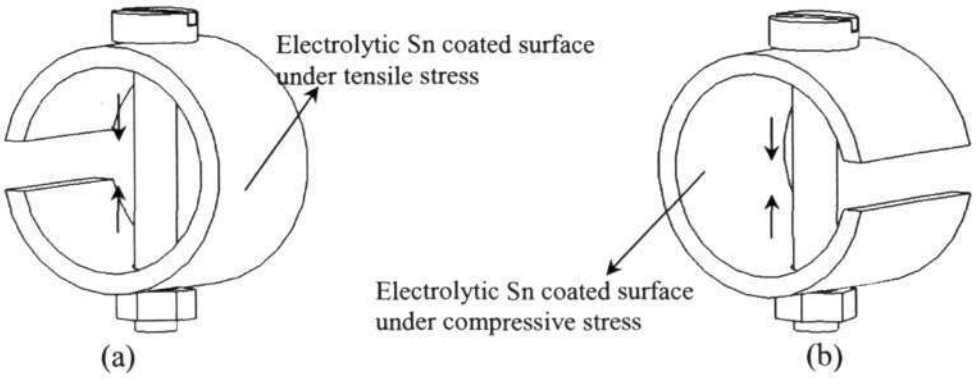


Figure 3.20 A schematic drawing of electrolytic Sn coated C-ring showing the regions subjected (a) in-plane tensile and (b) in-plane compressive stresses. These regions were evaluated under SEM for Sn whisker growth study.

Chapter 4: Microstructural Evolution during Annealing of Bulk Solders

4.1 Introduction

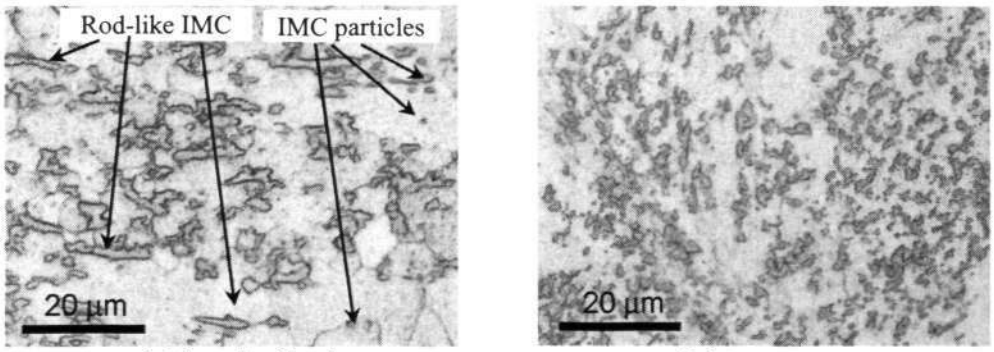
In service, solder joints in an electronic assembly often fail due to cyclic thermal loading. Therefore, researches concerning the growth of IMC under various thermal loading conditions such as thermal cycling (TC) and thermal shock (TS) were carried out in the project and the results are presented in the next chapter. This chapter focuses on presenting results on evolution of IMCs during isothermal annealing of two bulk solders (95.5Sn-3.8Ag-0.7Cu and 99.3Sn-0.7Cu). TC and TS involves change of temperature and thermal stresses and thus encompass complex driving mechanisms on the IMC growth. It is hoped that the study of isothermal annealing makes it easier to understand the effect of individual factors such as temperature and heating time on the growth of IMCs.

The IMC growth in 99.3Sn-0.7Cu solder was studied through a specially designed in-situ observation technique, as described in Chapter 3. This binary solder was chosen for the study because it consists of single type of IMC that helps to eliminate the need to characterize the IMC particles to be monitored. Since the IMC growth rate of the individual particle was to be studied, the challenge of this study was to monitor the individual growth rate of the IMC particles at different time intervals through out the heating process.

4.2 Effect of Annealing on 95.5Sn-3.8Ag-0.7Cu Solder

4.2.1 As-received Microstructure

The 95.5Sn-3.8Ag-0.7Cu solder bar was cast and extruded in the as-received condition. Its microstructures were observed in both longitudinal and transverse directions (see Figure 3.1 in chapter 3). Figure 4.1 shows that the as-received microstructure consists of mainly rod-like IMCs elongated in the extruding direction.



(a) longitudinal (b) transverse

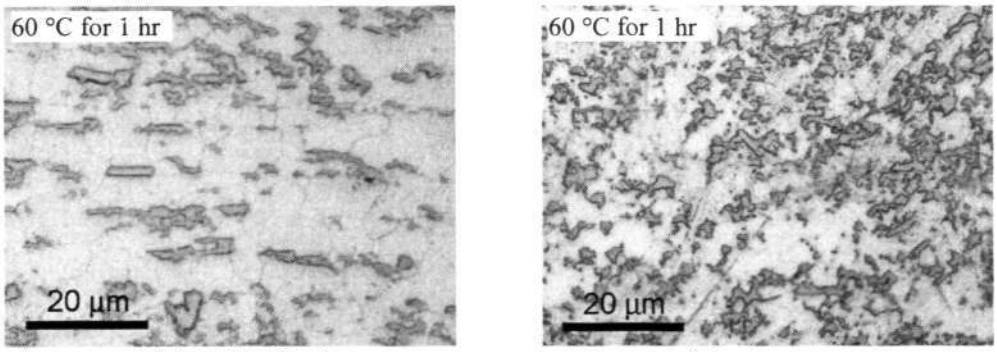
Figure 4.1 Optical micrographs showing the microstructures of the as-received 95.5Sn-3.8Ag-0.7Cu solder bar in (a) longitudinal direction (extruding direction is horizontal); (b) transverse direction.

4.2.2 Annealed Microstructures

Annealing was performed on the 95.5Sn-3.8Ag-0.7Cu solder to investigate the evolution of IMCs at different homologous temperatures (T_h) for various annealing times. Figures 4.2 to 4.4 show the optical micrographs of the microstructures after an hour of annealing at 60, 125 and 190 °C (corresponding to about 0.68, 0.81 and 0.94 to the melting point of the solder at T_m=490 K).

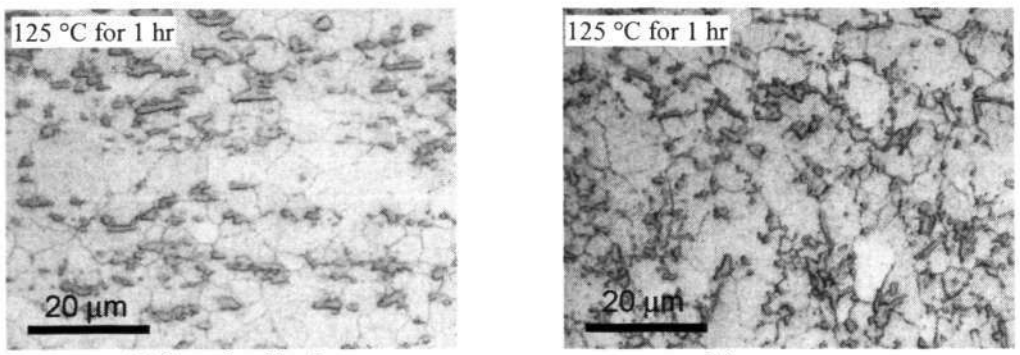
For annealing temperatures at 60 °C (0.68 T_m) and 125 °C (0.81T_m) as shown in Figures 4.2 and 4.3 respectively, no significant change of microstructures in either

longitudinal or transverse direction as compared to the as-received condition (Figure 4.1). At higher annealing temperature of 190 °C ($0.94T_m$), the rod-like IMC was found to evolve into more rounded shape (Figure 4.4).



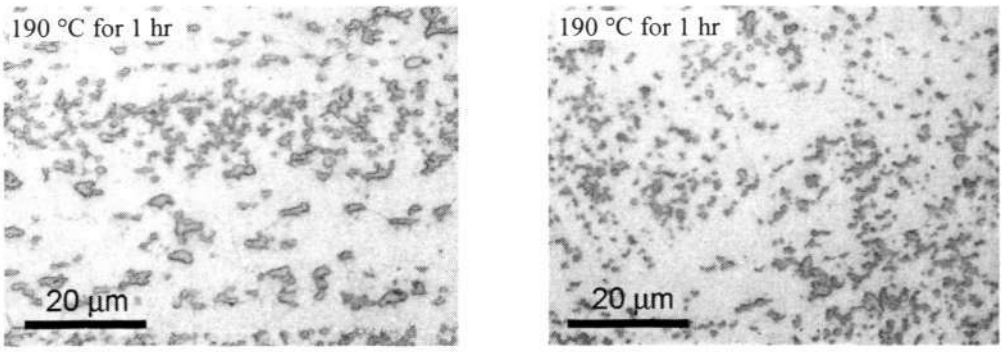
(a) longitudinal (b) transverse

Figure 4.2 Optical micrographs of the 95.5Sn-3.8Ag-0.7Cu solder bar annealed at 60 °C for 1 hr in (a) longitudinal and; (b) transverse directions



(a) longitudinal (b) transverse

Figure 4.3 Optical micrographs of the 95.5Sn-3.8Ag-0.7Cu solder bar annealed at 125 °C for 1 hr in (a) longitudinal and; (b) transverse directions

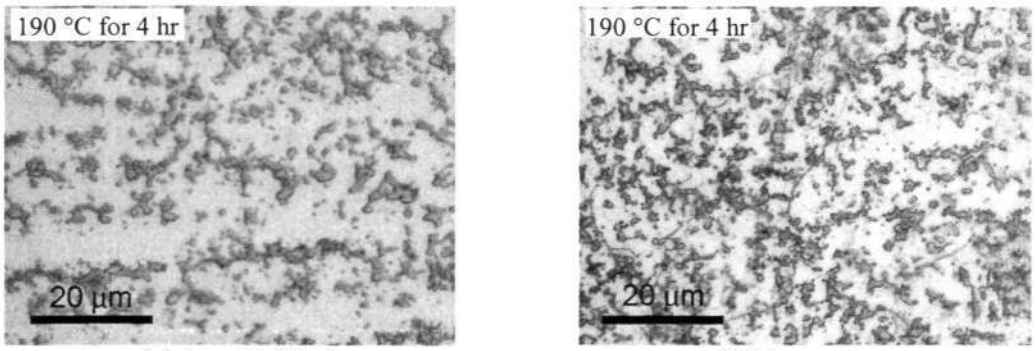


(a) longitudinal (b) transverse

Figure 4.4 Optical micrographs of the 95.5Sn-3.8Ag-0.7Cu solder bar annealed at 190 °C for 1 hr in (a) longitudinal and; (b) transverse directions showing IMCs more circular in shape.

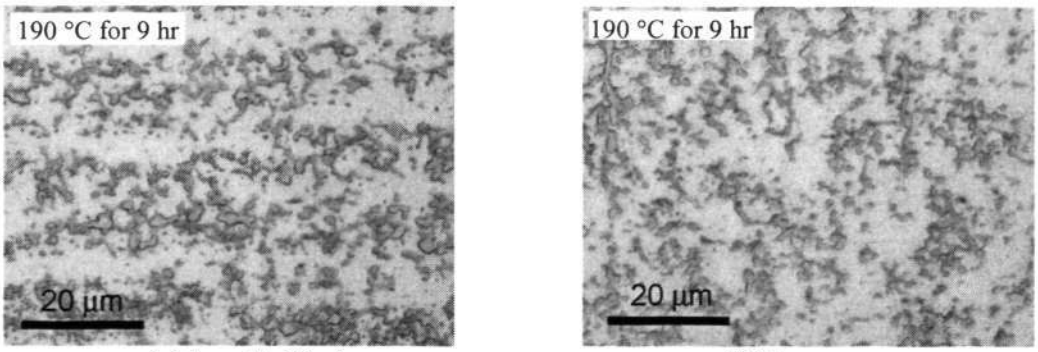
Since annealing temperature at 190 °C has shown significant change in microstructure, the annealing process at the same temperature for 2^2, 3^2, 4^2 and 5^2 hr was carried out. The results showed that the IMCs were larger in size but smaller in number for longer annealing time. This can be seen by comparing the microstructure of the specimen annealed at 190 °C for 1 hr (Figure 4.4) with those that annealed at the same temperature but for longer duration as shown in Figures 4.5 to 4.8.

The evolution of microstructure was found to stabilize after 9 hr of annealing at 190 °C. There were no significant differences between the microstructures of the specimens that annealed for 9, 16 and 25 hr at 190 °C.



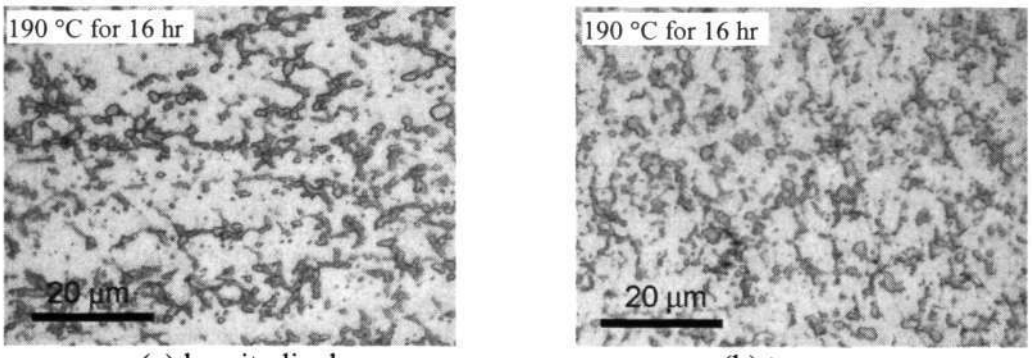
(a) longitudinal (b) transverse

Figure 4.5 Optical micrographs of the 95.5Sn-3.8Ag-0.7Cu solder bar annealed at 190 °C for 4 hr in (a) longitudinal and; (b) transverse directions



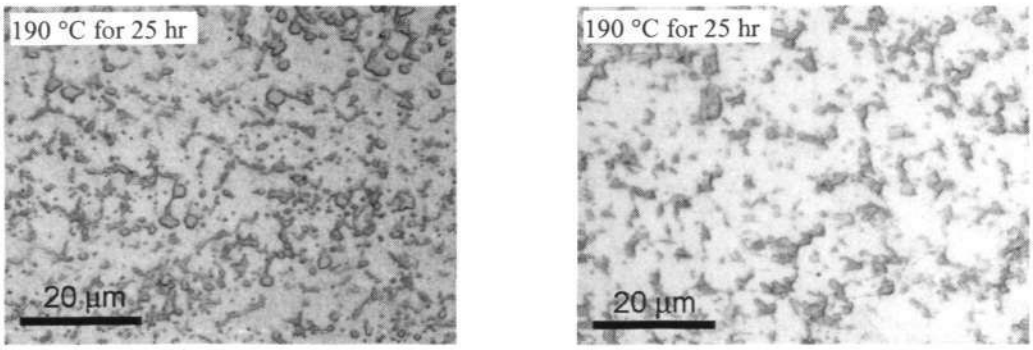
(a) longitudinal (b) transverse

Figure 4.6 Optical micrographs of the 95.5Sn-3.8Ag-0.7Cu solder bar annealed at 190 °C for 9 hr in (a) longitudinal and; (b) transverse directions



(a) longitudinal (b) transverse

Figure 4.7 Optical micrographs of the 95.5Sn-3.8Ag-0.7Cu solder bar annealed at 190 °C for 16 hr in (a) longitudinal and; (b) transverse directions



(a) longitudinal (b) transverse

Figure 4.8 Optical micrographs of the 95.5Sn-3.8Ag-0.7Cu solder bar annealed at 190 °C for 25 hr in (a) longitudinal and; (b) transverse directions

4.3 In-situ Observation of IMC Growth in 99.3Sn-0.7Cu

4.3.1 Microstructure and Chemical Analysis

The SEM images showing the microstructures of the well-polished specimens under as-received and heated at 215 ºC for 524 min are shown in Figures 4.9 and 4.10. Dendritic and cellular dentritic structures were observed from both specimens. In addition, eutectic lamellar structures were observed from the as-received specimen. After subjecting to annealing at 215 ºC for 524 min, the IMC particles have grown in size (Figure 4.10).

As annealing time increased, the boundary of the IMC particles becomes less defined. This was due to the presence of oxide layer that formed during the heating process. The oxide layer appears as yellow or brownish colour under the optical micrograph, as shown in Figure 4.11. The formation and accumulation of the oxide layer during the heating process has affected the clarity and contrast of the images. The presence of the oxide layer caused the tracing of the IMC particle difficult, especially after long exposure time.

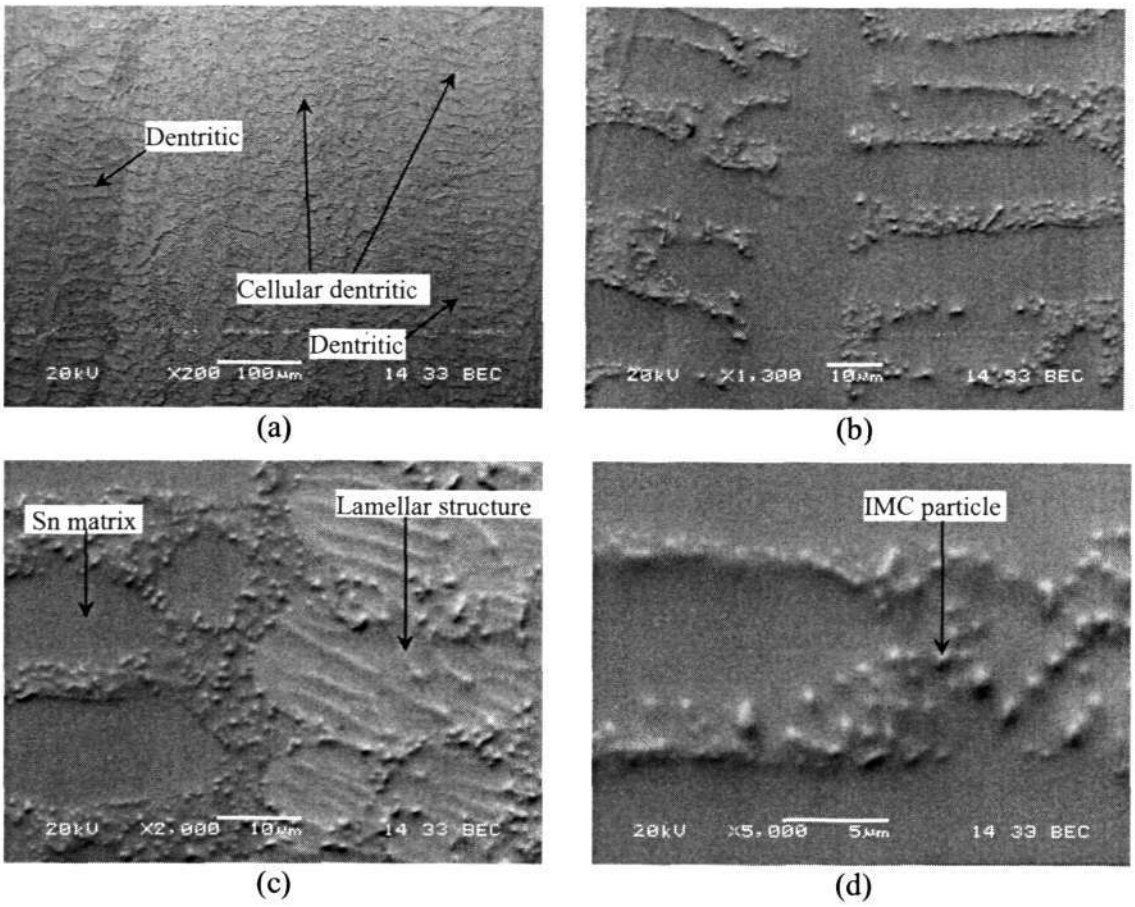


Figure 4.9 SEM (BSE) micrographs of the as-received 99.3Sn-0.7Cu solder showing the (a) overall view; (b) close-up of dendritic structure; (c) close up of the boundary between the lamellar and planar Sn matrix phase and; (d) close up of IMC particles

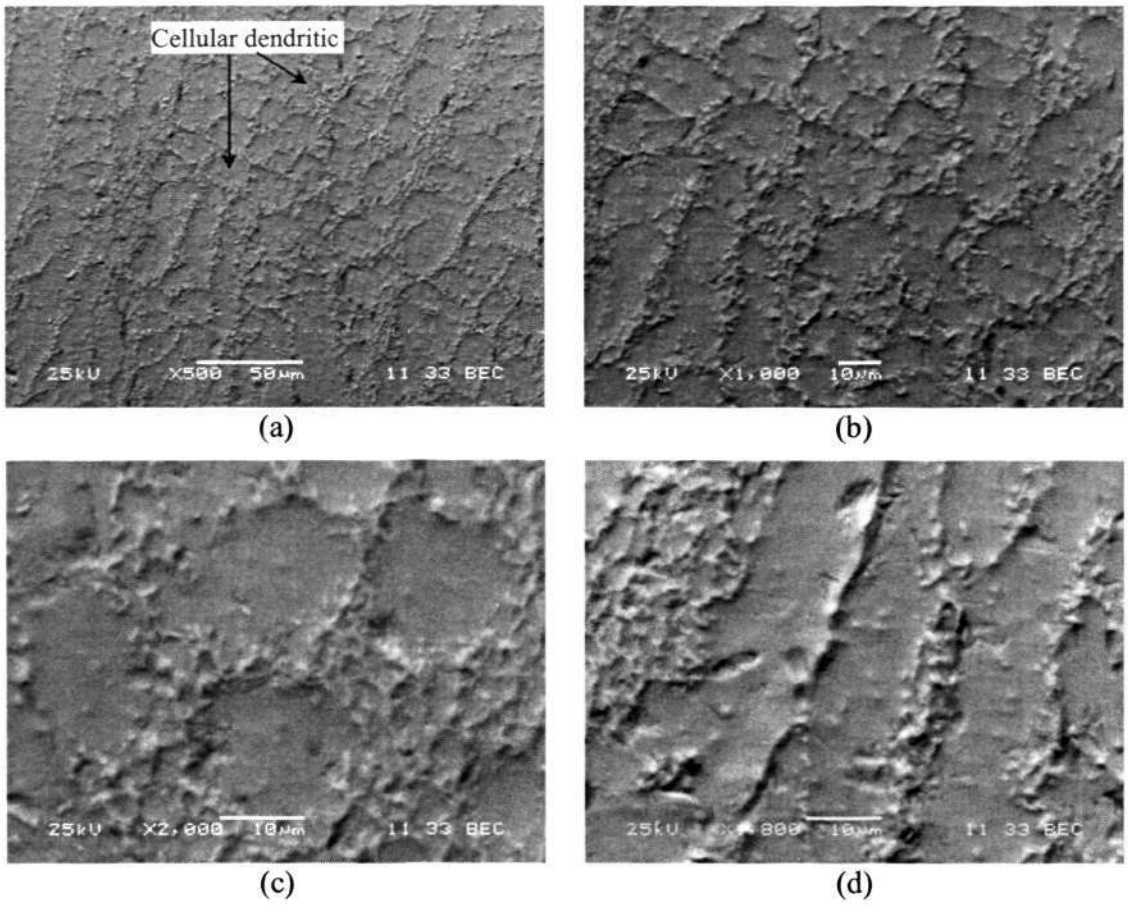


Figure 4.10 SEM (BSE) micrograph of 99.3Sn-0.7Cu solder heated at 215 °C for 524 min (a) overall view; (b) close up and; (c) further close-up views of (a) showing the cellular cells more clearly; (d) another close-up of (a) showing columnar cell

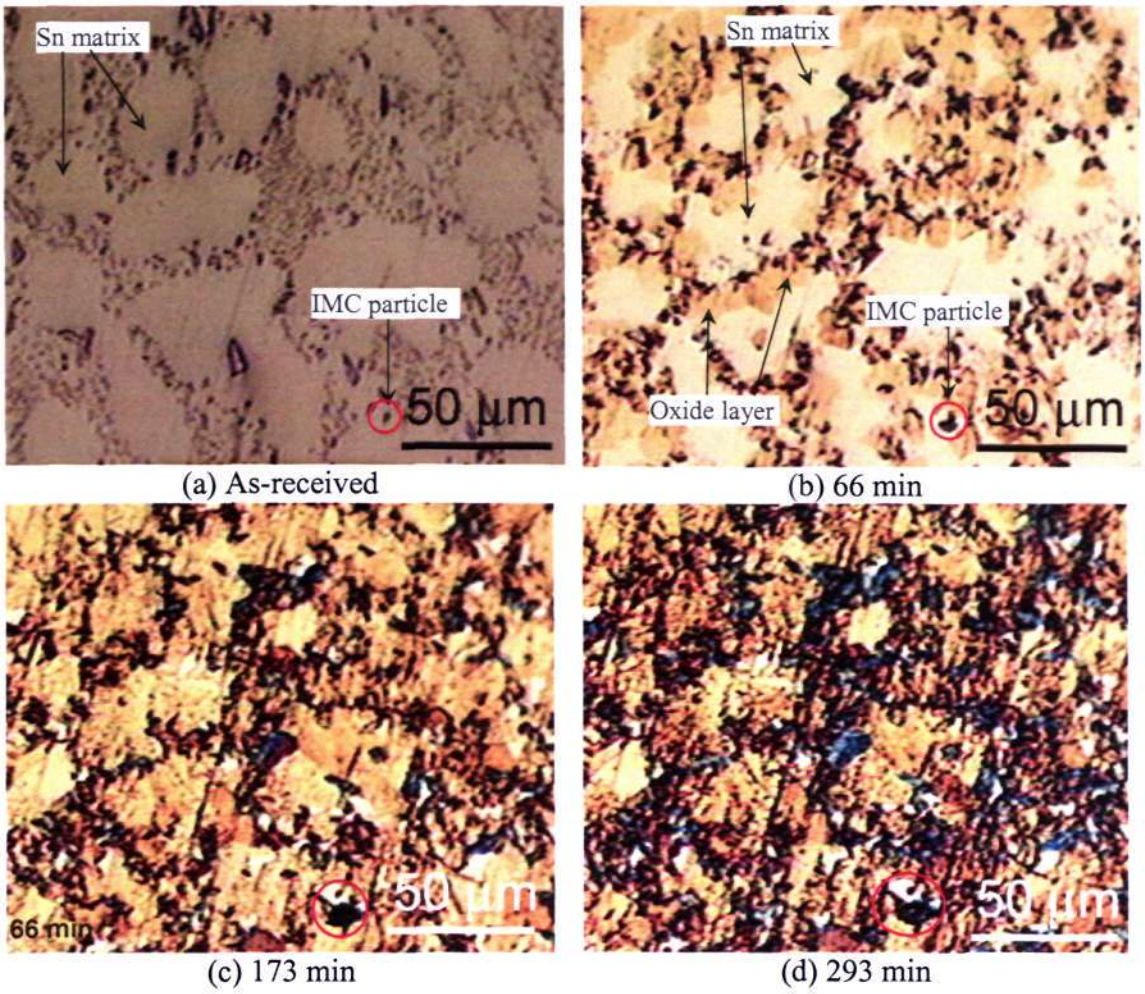


Figure 4.11 Optical micrographs of 99.3Sn-0.7Cu solder showing the evolution of microstructure at the same region under different stages during heating process; (a) as-received condition and; heated at 215 °C for (b) 66 min; (c) 173 min and (d) 293 min. The oxide layer in yellowish and brownish colour can be found at the surrounding of the IMC particles. Individual growth rate of IMCs (one of them in circled) was monitored at different time intervals through out the heating process.

The compositions and phases present in the specimens were examined through the EDX and XRD analysis. Another piece of specimen that re-solidified in furnace after being heated 1 hr at 260 °C was included for the composition analysis. Much larger IMC particles from this re-solidified specimen helped to intensify the EDX

signals (Figure 4.12). The XRD spectrum of the re-solidified specimen is shown in Figure 4.13.

The XRD results on the as-received specimen and specimen that heated at 215 ºC for 524 min are shown in Figures 4.14 and 4.15. The XRD analysis on the heated and re-solidified specimens show small peaks corresponding to Cu_6Sn_5 η-phase. However, the same peaks were not observable from the as-received specimen due to relative weak signals from the much smaller IMC particles. This was corresponded to the EDX result shown in Figure 4.12, where Cu was only detectable from re-solidified specimen.

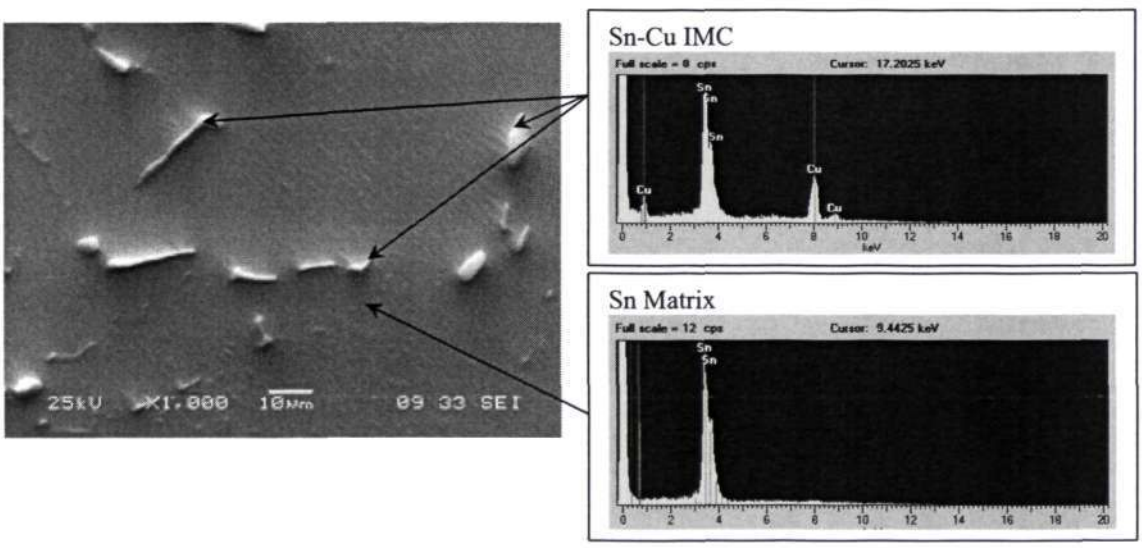


Figure 4.12 EDX analyses on composition of 99.3Sn-0.7Cu solder re-solidified in furnace (after being heated to 260 ºC for 1 hour).

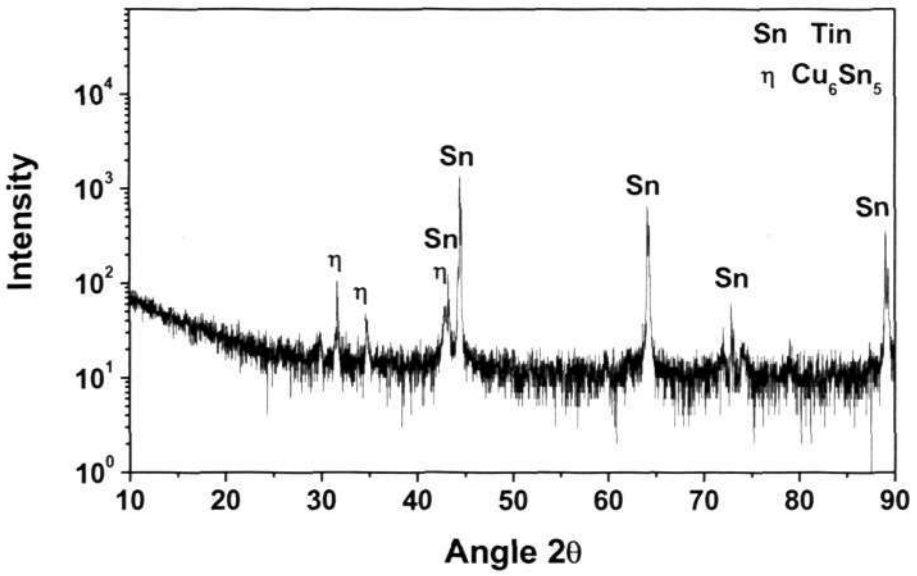


Figure 4.13 XRD pattern of the 99.3Sn-0.7Cu solder re-solidified in furnace.

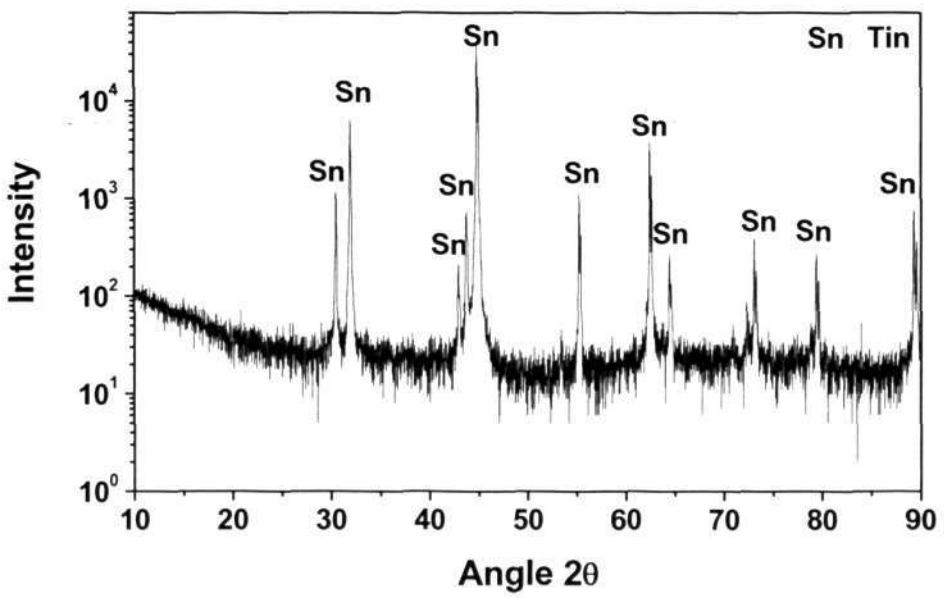


Figure 4.14 XRD pattern of the as-received 99.3Sn-0.7Cu solder

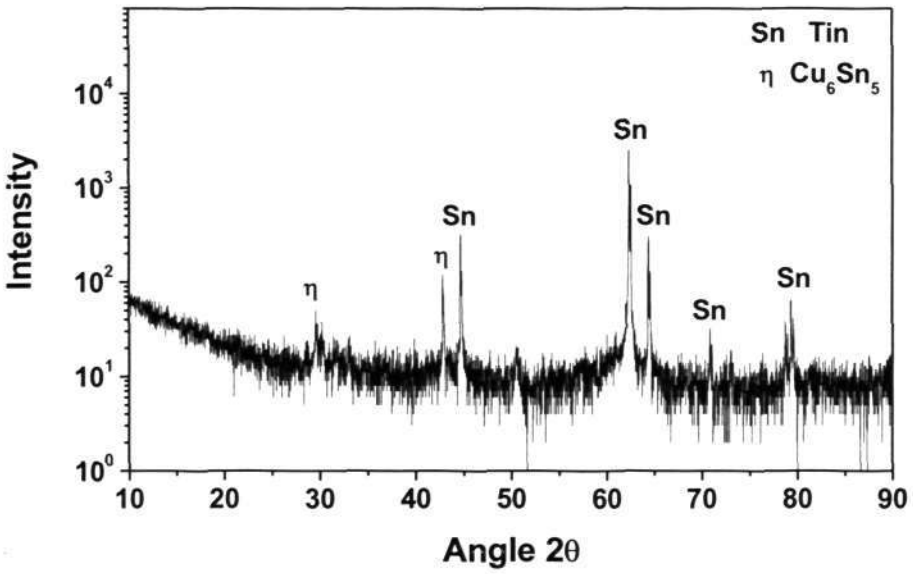


Figure 4.15 XRD pattern of the 99.3Sn-0.7Cu solder heated at 215 °C for 524 min

4.3.2 IMC Growth Rate

The size of the IMC was determined by making two measurements, x and y on the particle as indicated in Figure 4.16. The equivalent radius, r, is defined as,

$$r = \frac{\sqrt{xy}}{2} \qquad [4.1]$$

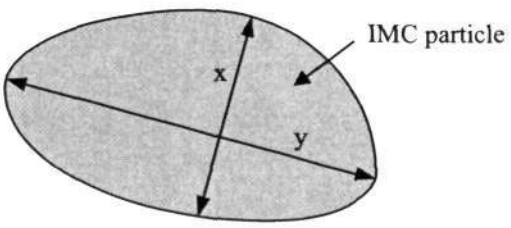


Figure 4.16 Diagram showing the measurements made on the IMC particle

The value of r for individual IMC monitored in-situ during heating at different temperatures is plotted as a function of heating time. Figures 4.17 to 4.21 show the results obtained for heating temperatures of 190, 200, 210, 215 and 220 °C. All the figures show that the initial growth of all IMC particles displays a nearly linear

relationship and the growth tends to level off after an extended heating period. As can be seen from Figure 4.20, at fixed heating temperature of 215 °C, curves of almost all the four IMC particles monitored show the linear relationship for the first 70 min but after which they level off with further increase of heating time.

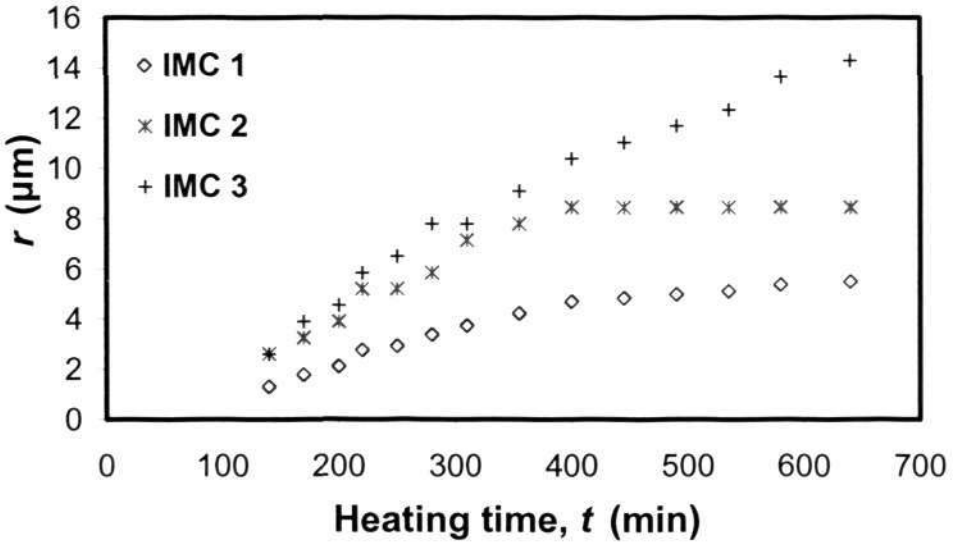


Figure 4.17 Growth of IMCs with respects to heating time at 190 ºC

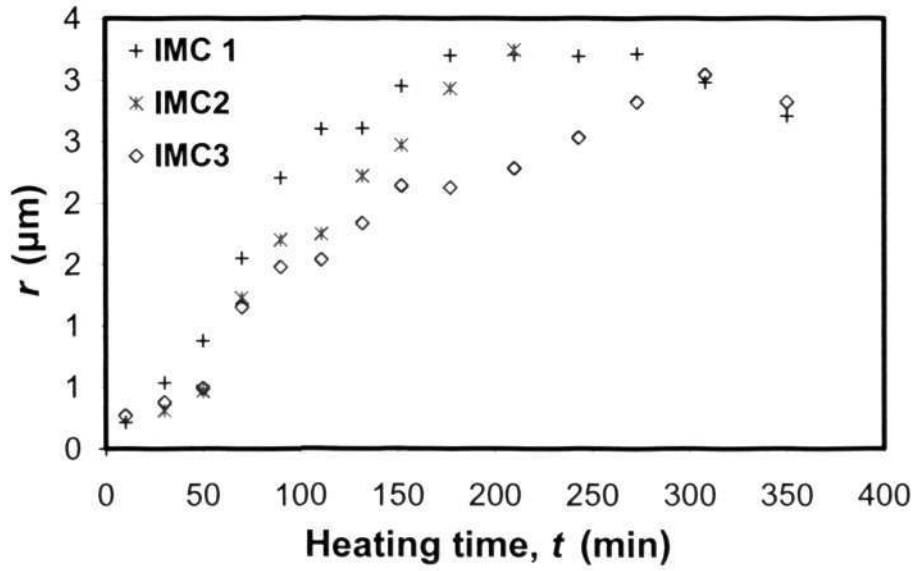


Figure 4.18 Growth of IMCs with respects to heating time at 200 ºC

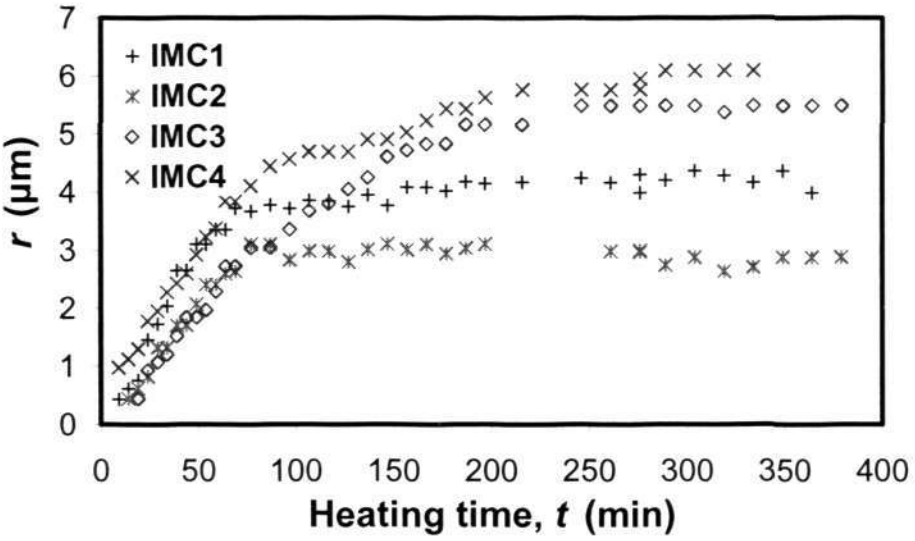


Figure 4.19 Growth of IMCs with respects to heating time at 210 °C

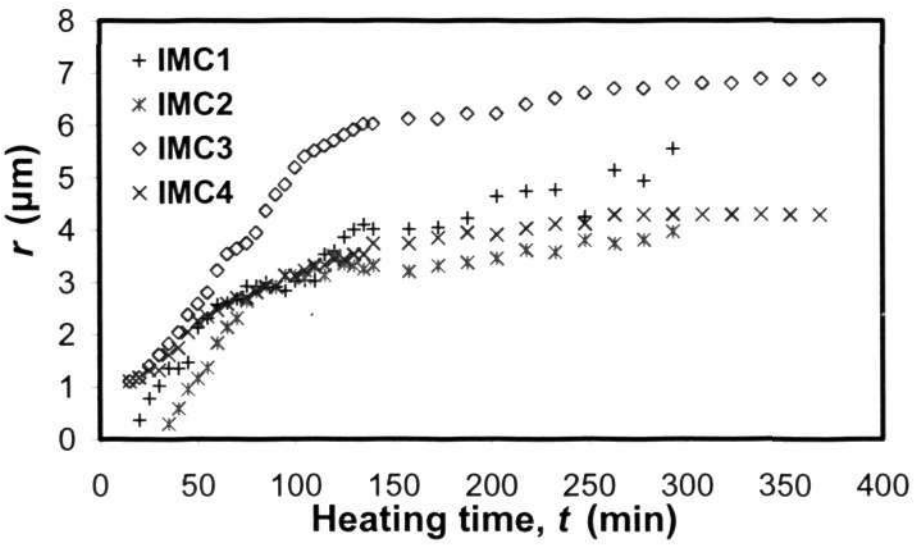


Figure 4.20 Growth of IMCs with respects to heating time at 215 °C

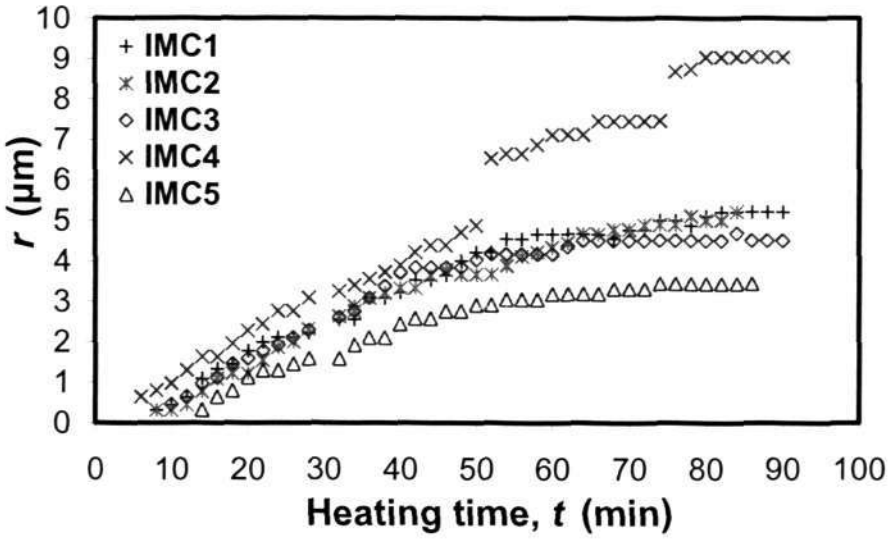


Figure 4.21 Growth of IMCs with respects to heating time at 220 °C

The in-situ observation of IMC growth at various temperatures makes it possible to evaluate the quantitative relationship between the IMC growth rate and temperature. Figure 4.22 shows the initial IMC growth rate, V as a function of the heating temperature, T. The figure shows clearly that the IMC growth rate increases with increasing temperature. This is as expected for any diffusion-controlled growth process, because diffusion coefficient, D, increases with temperature as given in the Arrhenius expression,

$$D = D_o \exp(-Q/kT) \qquad [4.2]$$

where D_o is the diffusion constant, Q is the activation energy, k is the Boltzman constant, and T is the absolute temperature. The Arrhenius expression predicts a linear relationship between $logD$ and $1/T$. Therefore, it is worthwhile to examine the relationship between $logV$ and $1/T$. Figure 4.23 shows that the relationship is also linear.

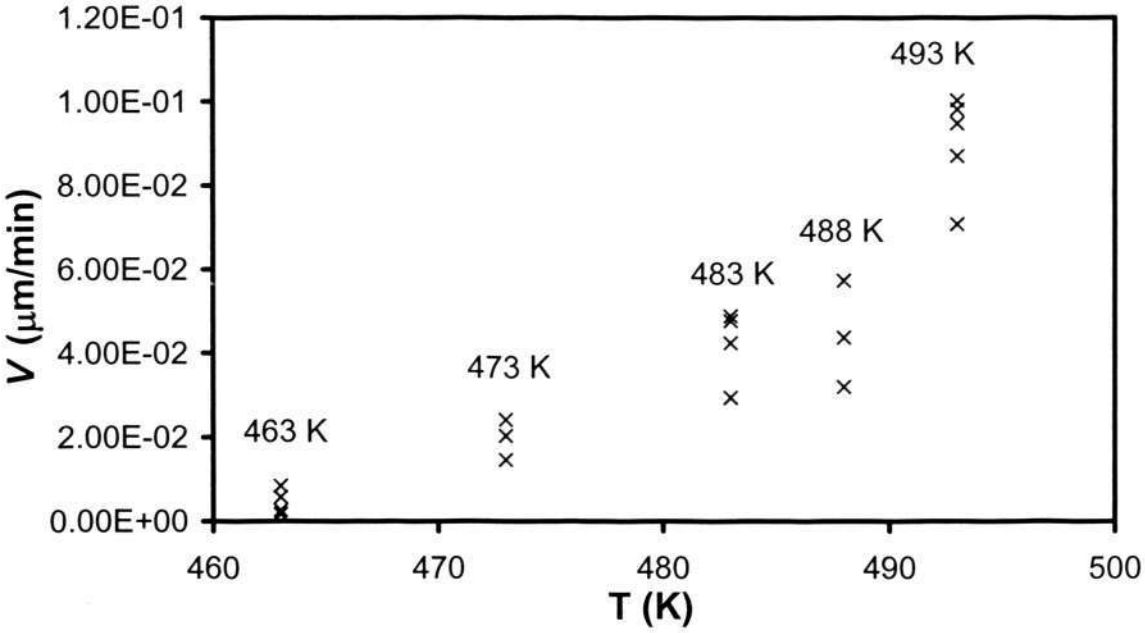


Figure 4.22 Effect of heating temperature on the initial growth rate of IMC particle

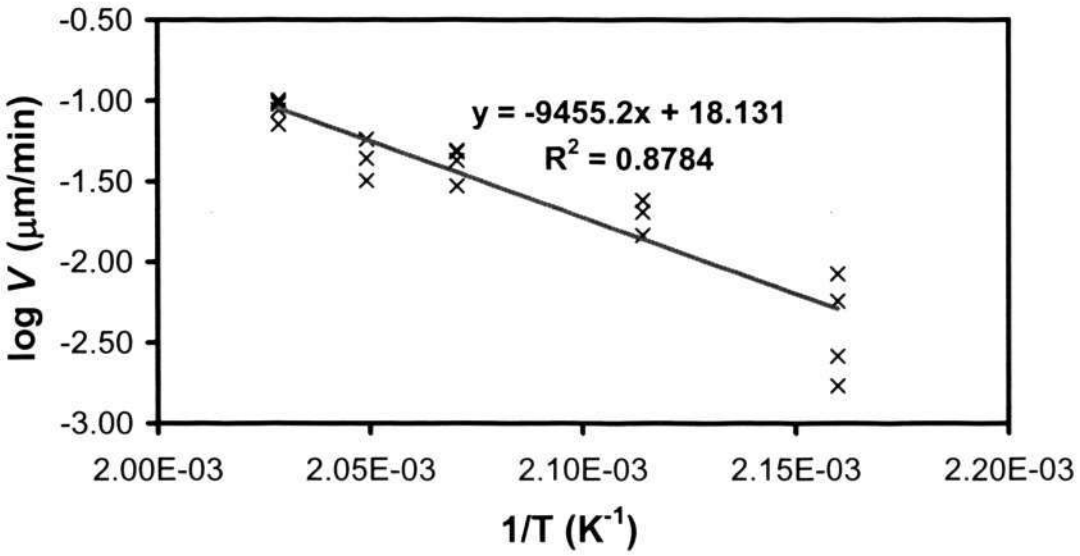


Figure 4.23 Plot of log of initial IMC growth rate with respect to reciprocal of heating temperature

The diffusion and IMC growth processes can be further analyzed. Under condition of non-steady state, the partial differential equation known as Fick's second law is used,

$$\frac{\partial C}{\partial t} = \frac{\partial}{\partial x}\left(D\frac{\partial C}{\partial x}\right) \qquad [4.3]$$

where C is the concentration at distance of x within the solid. It is reasonable to assume that the diffusion coefficient of Cu in Sn is independent of composition, so the above equation can be simplified to

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial x^2} \qquad [4.4]$$

The solution of the equation depends on the boundary conditions. Below is a commonly used solution,

$$\frac{C_x - C_o}{C_s - C_o} = 1 - erf\left(\frac{x}{2\sqrt{Dt}}\right) \qquad [4.5]$$

where *erf* is the Gaussian error function, D is diffusion coefficient at the given temperature, t is time, x is distance, and C_x is concentration at distance x. However, it should be noted that the solution is valid only if both concentration at surface (C_s) and concentration at far-away location (C_o) are constant, as illustrated in Figure 4.24.

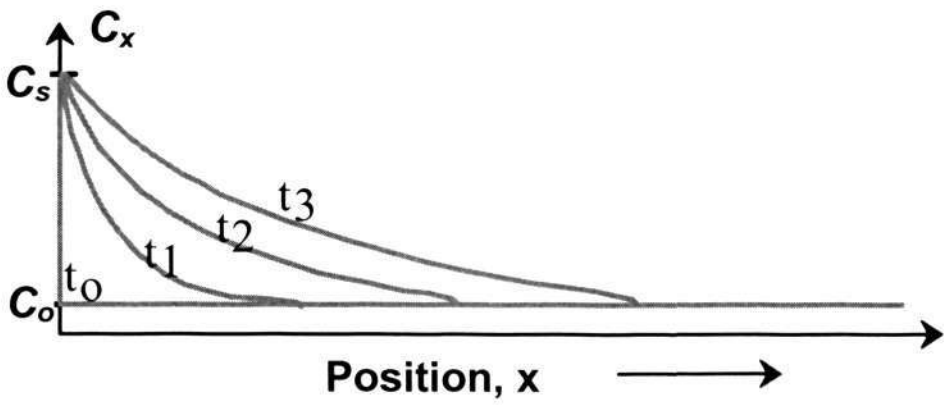


Figure 4.24 Illustration of boundary conditions for deriving equation [4.5].

For IMC growth at the interface between solder and substrate, as studied in Chapter 5, the boundary conditions are applicable, because Ni concentration in the substrate (C_s) is constant (almost 100% for the Ni plating) and Ni concentration at the location far away from the IMC interface (C_o), i.e., in the solder, is also constant (almost zero in the study in Chapter 5). When the Cu-Ni-Sn IMC grows, it always contains the constant concentration of Ni, C_1; therefore,

$$\frac{C_1 - C_o}{C_s - C_o} = \text{constant} \qquad [4.6]$$

The following can be obtained from equations [4.5] and [4.6],

$$\frac{x}{2\sqrt{Dt}} = \text{constant} \qquad [4.7]$$

or

$$x \propto 2\sqrt{Dt} \qquad [4.8]$$

and the relationship can be further simplified to

$$x \propto \sqrt{t} \qquad [4.9]$$

The formula shows that the IMC growth is proportional to $\sqrt{t}$. This is in contrast to the in-situ observation showing that the IMC growth is proportional to t. It can be seen from the above analyses that the discrepancy is caused by different boundary conditions for diffusion.

In the case of IMC growth on substrate (Ni or Cu), the atomic diffusion from the substrate through the IMC is the main controlling process (Guan et al., 2000, Xiao et al., 2001, Young et al., 2001). However, in the present study of IMC growth in bulk solder (i.e., without a substrate), the dominant process is the diffusion of Cu to the interface between the IMC and solder. The study highlights the fact that the controlling

mechanism for IMC growth in bulk solders is different from that in the presence of a substrate.

4.4 Summary and Conclusions

Effect of temperature on the microstructure of 95.5Sn-3.8Ag-0.7Cu lead-free solder was studied using a fixed annealing time of 1 hr but at various annealing temperatures of 60, 125 and 190 °C. Annealing at homologous temperature at $0.68T_m$ (60 °C) or $0.81T_m$ (125 °C) for 1 hour produces no observable microstructural change. However, increase of annealing temperature to homologous temperature at $0.94T_m$ (190 °C) results in IMCs which are smaller in number, larger in size and more rounded in shape, indicating the growth of large IMCs at the expense of the small ones.

Effect of time on the microstructures of 95.5Sn-3.8Ag-0.7Cu solder was studied at a fixed annealing temperature at 190 °C. Coarsening of the IMC was stabilized after exposure to annealing time of 9 hr. Further increasing in annealing time from 9 to 25 hr did not lead to any significant change of IMC.

To further study the effects of annealing temperature and time, IMC growth of the 99.3Sn-0.7Cu lead-free solder was carried out through a specially designed in-situ observation technique. The growth of individual IMC particles with respect to temperature and heating time was monitored. This study helps to understand the IMC growth mechanism better with much closer monitoring of the IMC growth. Generally, the initial growth of all IMC particles displays a nearly linear relationship. The study highlights the fact that the controlling mechanism for IMC growth in bulk solders is different from that in the presence of a substrate.

Chapter 5: Isothermal, Thermal Cycling and Thermal Shock Aging on Intermetallics Growth

5.1 Introduction

Solder joints in electronic assemblies often fail by thermally activated loading during operation. The desire for miniaturization and increase in higher I/O result in much closer solder bump to bump spacing and limit the bump size. This leads to increase in the thermo-mechanical stress in the IC packaging. Especially, the mismatched thermal expansion characteristics of the materials joined by the solder and the thermal aging encountered during service constitute a condition of failure for the constrained solder.

Failure due to thermal aging often related to IMC effects (Kluizenaar, 1990, Jang and Paik, 1998, Frear, 2001, Zhang et al., 2001, Ma et al., 2002, Zeng and Tu, 2002). Understanding aging degradation behavior of the solder joint-to-pad interfaces in electronic packages is a critical concern in microelectronic soldering interconnections.

This chapter deals with the effect of various thermal loading condition on the interface IMC growth between the 95.8Sn-3.5Ag-0.7Cu lead-free solder and the electroless Ni immersion Au (ENIG). In addition, the fracture mechanism of the as-reflowed and isothermally aged solder/copper joints was studied through the in-situ fractography technique.

5.2 Effect of Isothermal Aging on IMC in Solder/Copper Joint

The solder/copper joint formed by reflowing two pieces of Cu sheets with 95.8Sn-3.5Ag-0.7Cu solder paste was used in this study. Before the reflowing process the surfaces of the Cu sheets were coated with electroless Ni of 2 to 3 μm in thickness

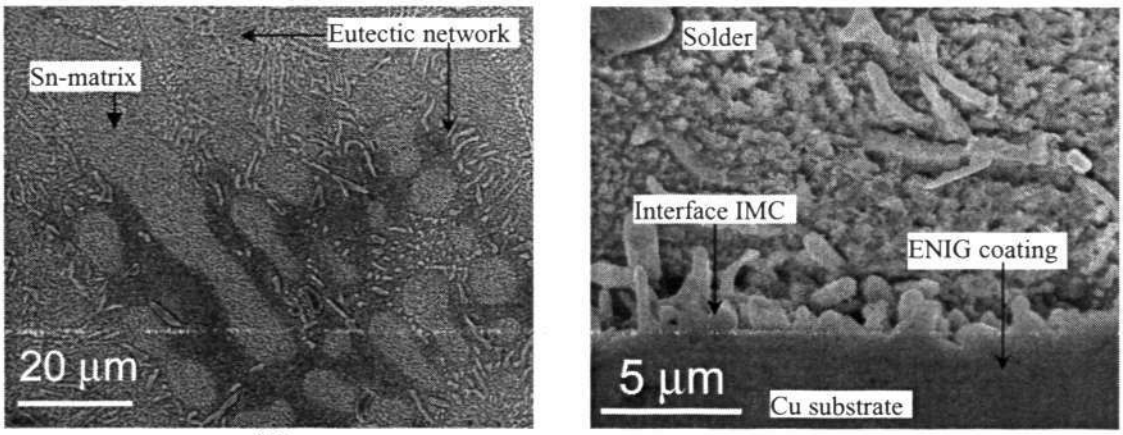
and then immersion Au of about 0.06 μm in thickness (i.e., ENIG coating layer). The solder/copper joint was subjected to isothermal aging at 125, 150 and 175 °C for 24, 72, 144 and 336 hr. Details of the experimental procedure are described in Section 3.4.

5.2.1 As-reflowed Microstructure

The microstructures across the solder/coating interface and within the solder were examined. The as-reflowed solder consists of Sn-matrix and eutectic network, as shown in Figure 5.1(a). The eutectic network contains granular, rod-like and plate-like IMCs. EDX results (Figure 5.2) show that Cu and Sn were detected from the granular and rod-like IMCs, while plate-like IMC consists of Ag and Sn. By referring to other research works on the Sn-Ag-Cu lead-free solder (Loomans and Fine, 2000, Anderson et al., 2001, Lin et al., 2001, Zribi et al., 2001, Ho et al., 2002, Kim et al., 2002a, Kim et al., 2003), the Cu-Sn and Ag-Sn IMCs are Cu_6Sn_5 and Ag_3Sn respectively.

Figure 5.1(b) shows the microstructure across the solder/coating interface. It can be seen from the figure that the interface IMC has needle-like morphology. The EDX analysis of the interface IMC shows it to be is of Cu-Ni-Sn type (Figure 5.3).

It was reported by Ho et al. (2002) that for Sn-Ag-Cu lead-free solder with Ag concentration of 3.9 wt% and Cu concentration ranging from 0.6 to 3.0 wt% (compositions of Ag and Cu for solder used in this study fall within these ranges), $(Cu_{1-y}Ni_y)_6Sn_5$ IMC layer formed between the Ni and solder interface. In the study by Zribi et al. (2001), $(Cu,Ni)_6Sn_5$ IMC layer was also found at the interface between the 93.6Sn-4.7Ag-1.7Cu lead-free solder and Ni/Au surface coating of the as-reflowed package sample.



(a) (b)

Figure 5.1 SEM images showing the microstrutures of the as-reflowed solder/copper joint (a) with solder region; (b) at the solder/coating interface with needle-like IMC layer.

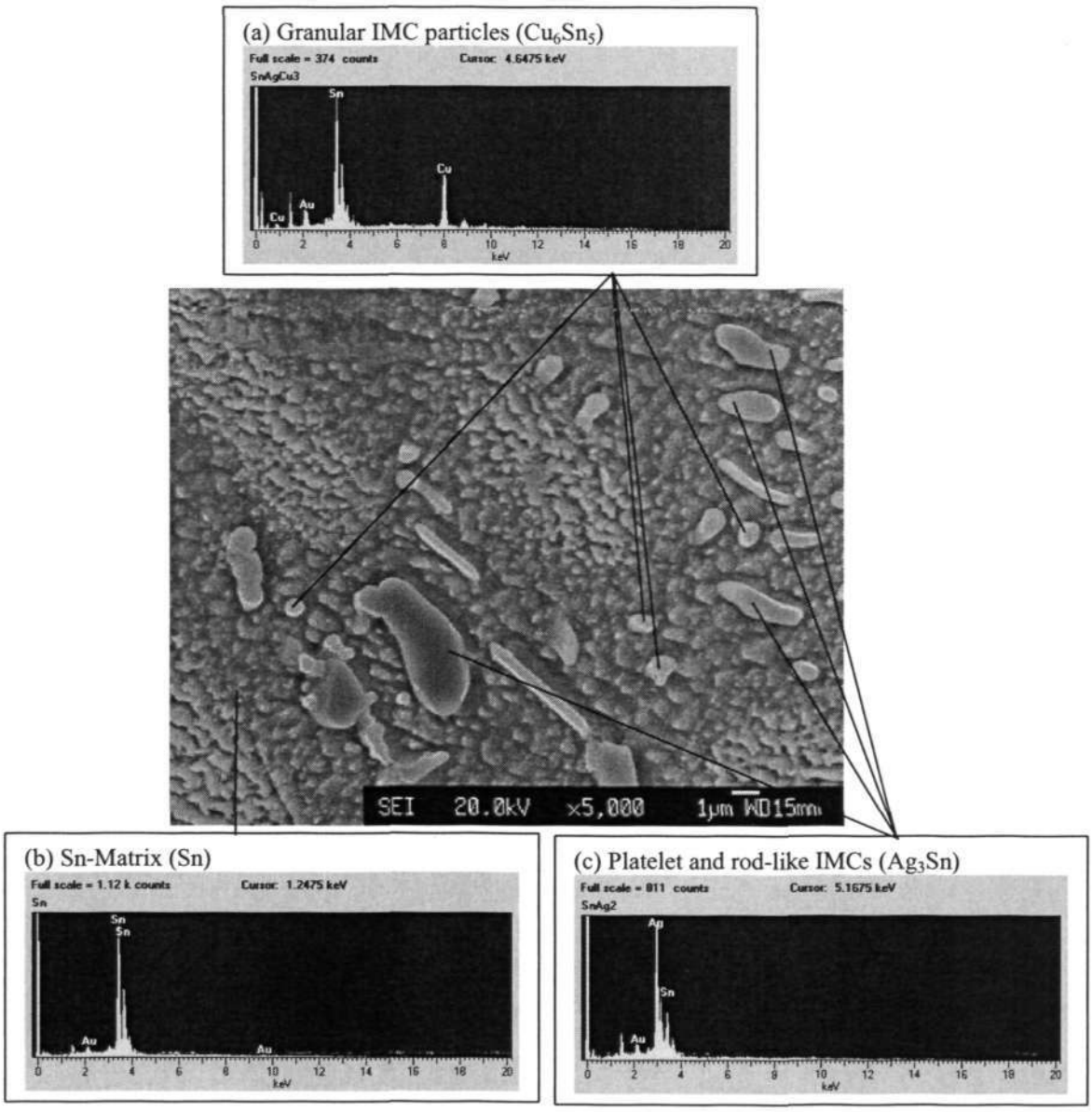


Figure 5.2 EDX spectrums of the (a) granular Cu_6Sn_5 IMC particles; (b) Sn-matrix; (c) platelet and rod-like Ag_3Sn IMCs in the solder region of the as-reflowed solder/copper joint.

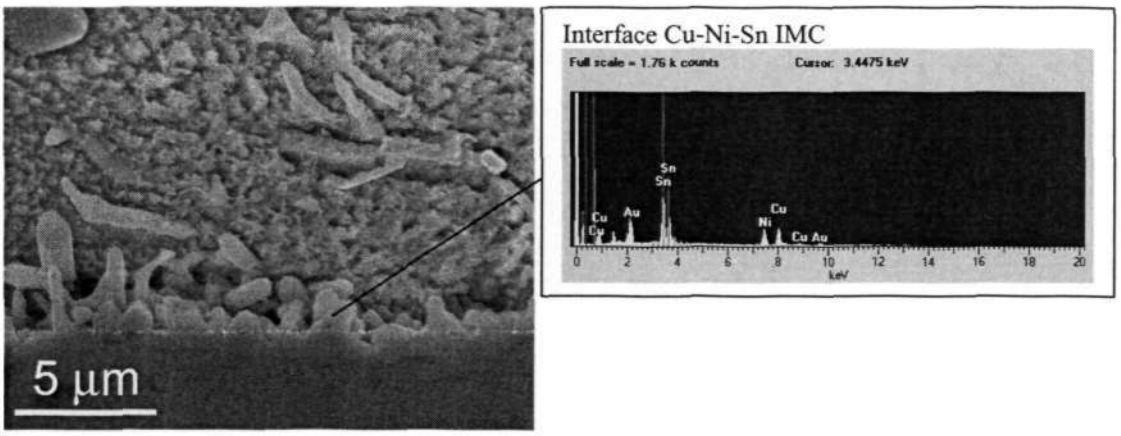


Figure 5.3 EDX spectrum of the interface IMC layer of the as-reflowed solder/copper joint.

5.2.2 Isothermally Aged Microstructure

SEM micrographs of the solder/copper joint exposed to isothermal aging at 125, 150 and 175 °C are shown in Figures 5.4, 5.5 and 5.6.

At 125 °C, when aging time increased, the IMCs tended to decrease in number and grow slightly in size, as shown in Figure 5.4 (a) to (d). No significant growth of needle-like Cu-Ni-Sn IMC layer can be observed (Figure 5.4 (e) to (h)).

Higher isothermal aging temperatures of 150 and 175 °C result in more rapid IMC coarsening and significant growth of the interface Cu-Ni-Sn IMC layer, as shown in Figures 5.5 and 5.6. It is further noted that the morphology of the interface IMC changes from needle-like to more planar and scallop-like shape with the increase of aging time.

The EDX results of the solder/copper joint exposed to isothermal aging at 150 °C for 144 hr and 175 °C for 336 hr show that most of the large and irregular shapes of IMC within the solder were of Cu_6Sn_5 type (Figures 5.7 and 5.8). The large Cu_6Sn_5 IMC was found mostly surrounded by the granular and rod-like Ag_3Sn IMCs.

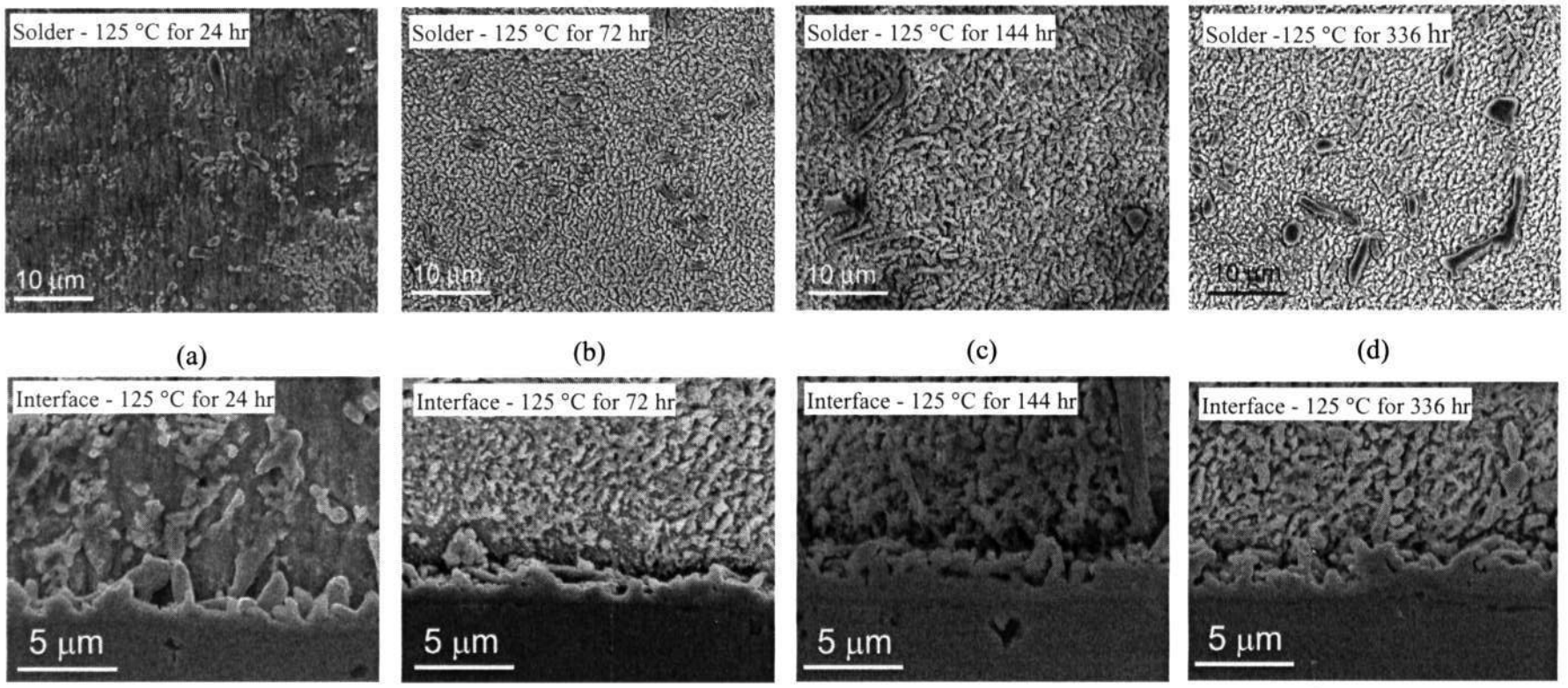


Figure 5.4 SEM images showing the microstrtctures of the solder/copper joint specimens that subjected to isothermal aging at 125 °C for different time intervals. The microstructures of the solder region that aged for (a) 24 hr, (b) 72 hr (c) 144 hr and (d) 336 hr. The micostructures of the interface region aged for (e) 24 hr, (f) 72 hr (g) 144 hr and (f) 336 hr.

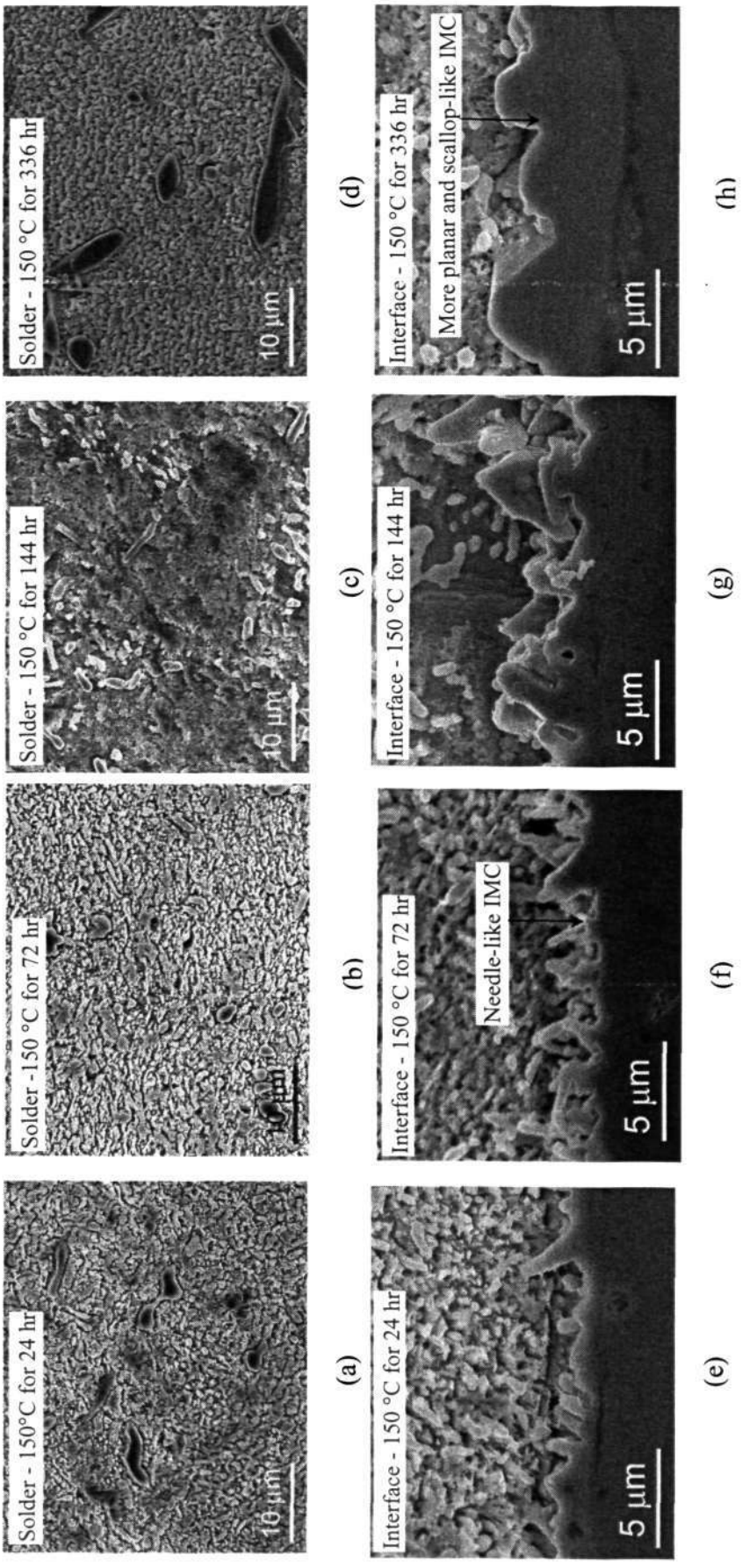


Figure 5.5 SEM images showing the microstrtctures of the solder/copper joint specimens that subjected to isothermal aging at 150 °C for different time intervals. The microstructures of the solder region that aged for (a) 24 hr, (b) 72 hr (c) 144 hr and (d) 336 hr. The micostructures of the interface region aged for (e) 24 hr, (f) 72 hr (g) 144 hr and (f) 336 hr.

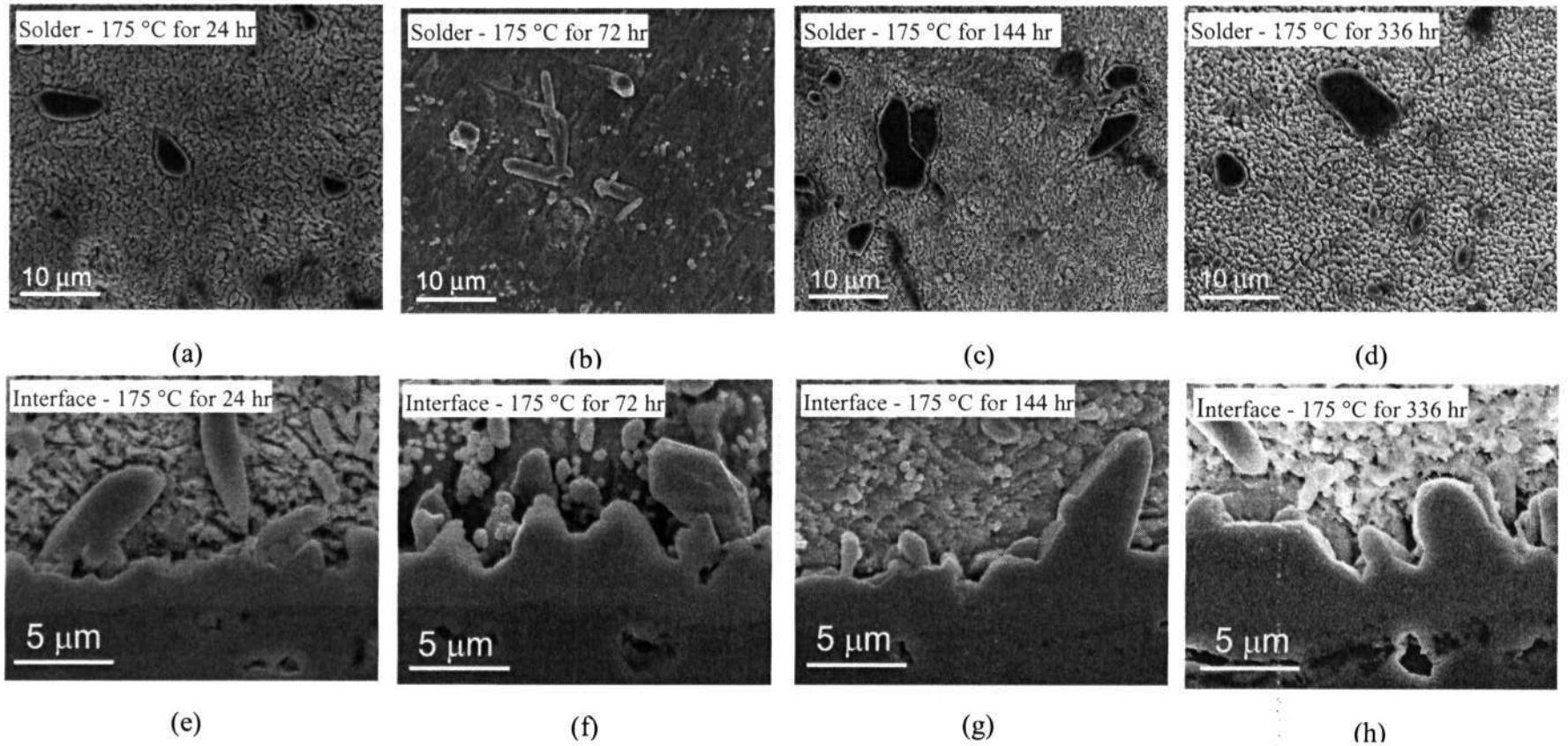


Figure 5.6 SEM images showing the microstrtctures of the solder/copper joint specimens that subjected to isothermal aging at 175 °C or different time intervals. The microstructures of the solder region that aged for (a) 24 hr, (b) 72 hr (c) 144 hr and (d) 336 hr. The micostructures of the interface region aged for (e) 24 hr, (f) 72 hr (g) 144 hr and (f) 336 hr.

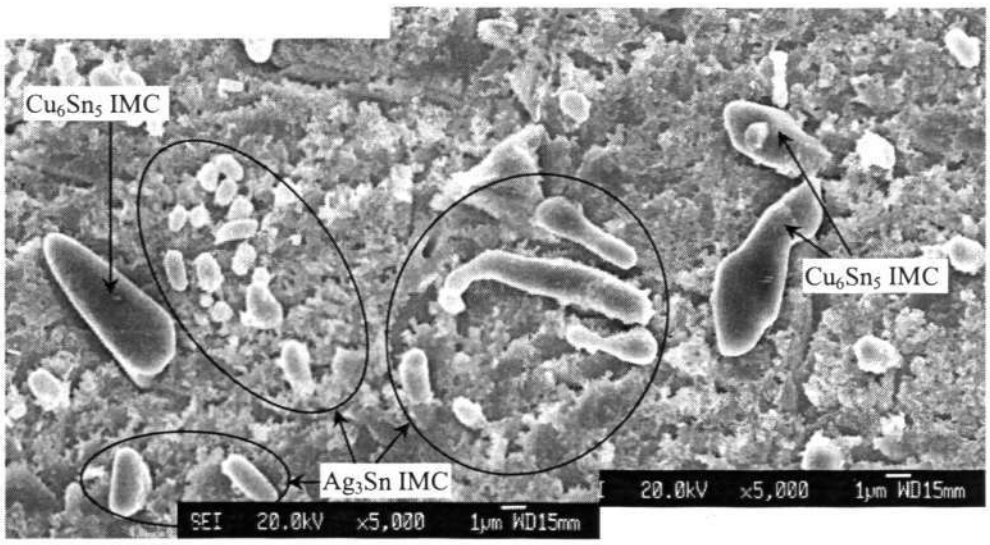


Figure 5.7 SEM image of the solder after isothermal aging at 150 °C for 144 hr showing large Cu_6Sn_5 IMCs surrounded by granular and rod-like Ag_3Sn IMCs.

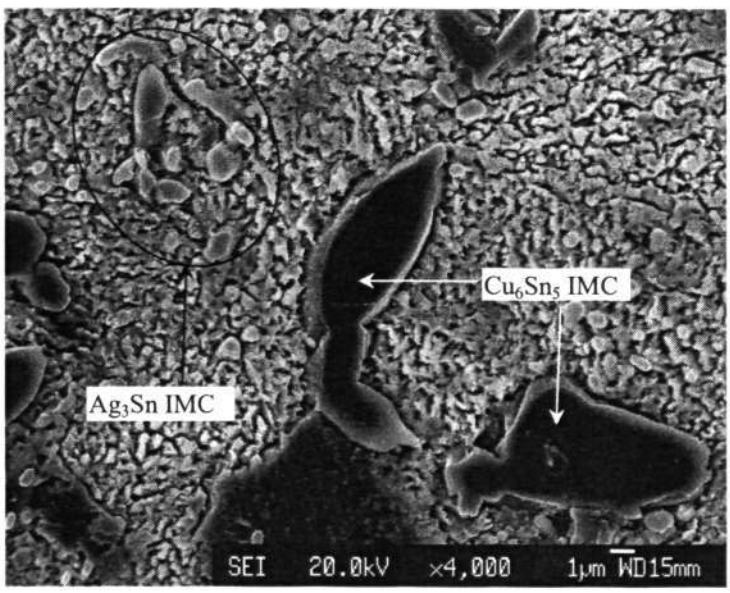


Figure 5.8 SEM image of the solder after isothermal aging at 175 °C for 336 hr showing large Cu_6Sn_5 IMCs surrounded by granular and rod-like Ag_3Sn IMCs.

Ghosh (2000) mentioned in his paper that Ni layer with thickness ranging from 1 to 3 μm should be thick enough to limit the outdiffusion of Cu to the interface at the

process temperature. If so, the existing ENIG coating with thickness about 2 to 3 μm was thick enough to retard the penetration Cu atom from the Cu substrate. If that was the case, the supply of Cu flux for the formation of the Cu-Ni-Sn interface IMC was purely from the Sn-Ag-Cu solder. Based on this assumption, it can be reasoned that the growing of Cu_6Sn_5 IMC was due to the coalescent of neighboring Cu_6Sn_5 IMC granular particles under isothermal aging. Consistently, the granular particles at the surrounding of the large Cu_6Sn_5 IMC were found mostly the Ag_3Sn IMC rather than a mixture of Cu_6Sn_5 and Ag_3Sn IMCs. This phenomenon implied that the large Cu_6Sn_5 IMC grew at the expense of the small Cu_6Sn_5 IMC particles in the solder.

In contrast, Lin and Hsu (2000) highlighted that Cu was seen to penetrate the Ni layer when the thickness of the Ni layer is less than 5 μm. If so, the Cu flux from the Cu substrate of the solder/copper joint used was able to penetrate through the ENIG coating and supplied the Cu for large Cu_6Sn_5 IMC formation during isothermal aging.

In addition to the ENIG coating layer, the Cu-Ni-Sn interface IMC layer between the coating and solder is possible to intervene the inflow of Cu flux from the Cu substrate. However, as described by Tu et al. (2002), there are opened channels between the scallop-like features in the interface IMC layer. The depth of these channels reaches the surface lay beneath the interface IMC layer (Figure 5.9). These channels allowed the Cu flux to penetrate through the partially consumed ENIG coating into the solder region and supplied Cu for the growing of large Cu_6Sn_5 IMC.

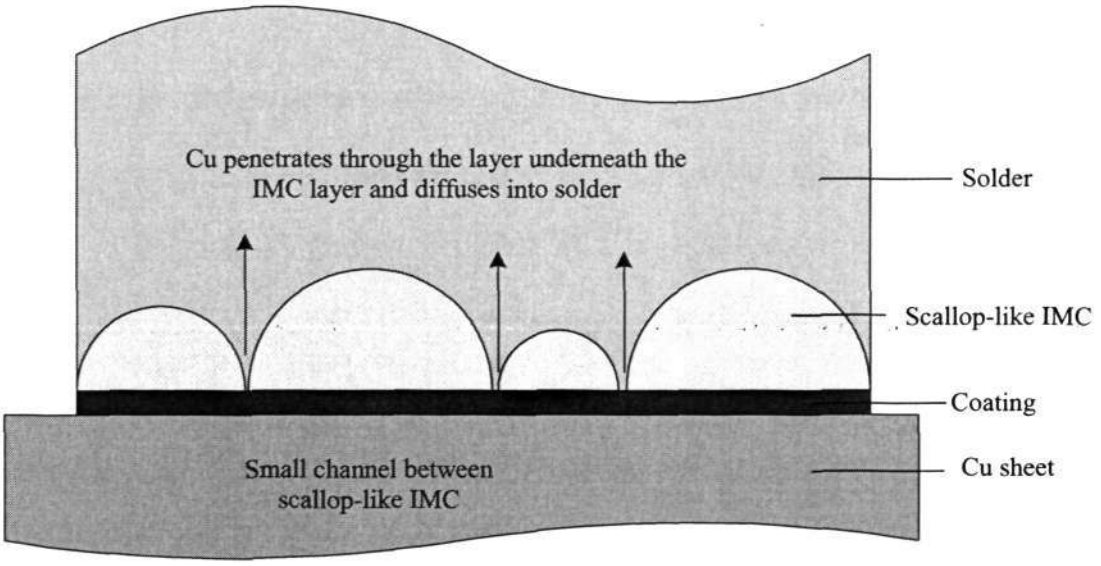


Figure 5.9 Shemetic diagram shows the inflow of Cu flux through the opened channels in between the scallop-like features of the interface IMC layer.

The EDX analysis results (Figure 5.10) at the interface of solder joint after isothermal aging show presence of large elongated Cu-Ni-Sn IMC near the interface. As can be seen clearly from the SEM images at the interface of the solder/copper joint (Figures 5.4 to 5.6), the needle-like Cu-Ni-Sn IMC grew in random orientations. A few long "IMC fingers" can be seen to grow from the interface Cu-Ni-Sn IMC. These large elongated Cu-Ni-Sn IMCs were observed to be detached from the substrate. They might be segments of the Cu-Ni-Sn IMC fingers originally attached to the substrate but appeared to be the detached pieces in the 2-D cross-sectional image.

However, the possibility that they were spalled IMCs, as shown in Figure 5.11, cannot be ruled out. It was reported (Kim et al., 1999, Zeng and Tu, 2002) that spalling of interface IMC into solder was observed after the solder joint went through a reflow process with relatively high temperature or a few reflow cycles. This spalling effect was attributed to the reaction of the metal elements during molten state. Furthermore, it was pointed out by Zeng and Tu (2002) that spalling effect may occur in solid state as well.

The mechanism of the IMC spalling is not fully understood and it is a important subject for further study, because the spalling phenomenon may affect reliability of the solder joint.

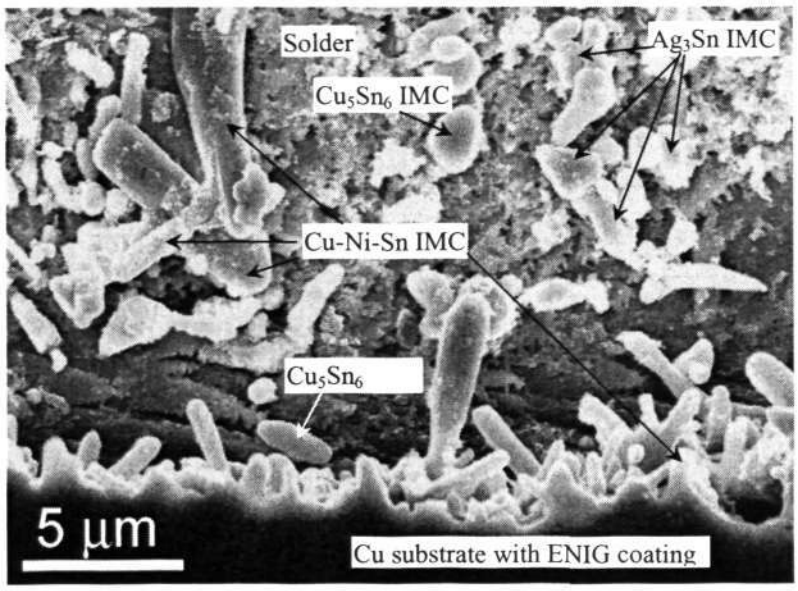


Figure 5.10 The EDX analysis results on the composition of intermetallic compounds at the interface of the solder/copper specimen after subjected to 150 °C for 144 hr

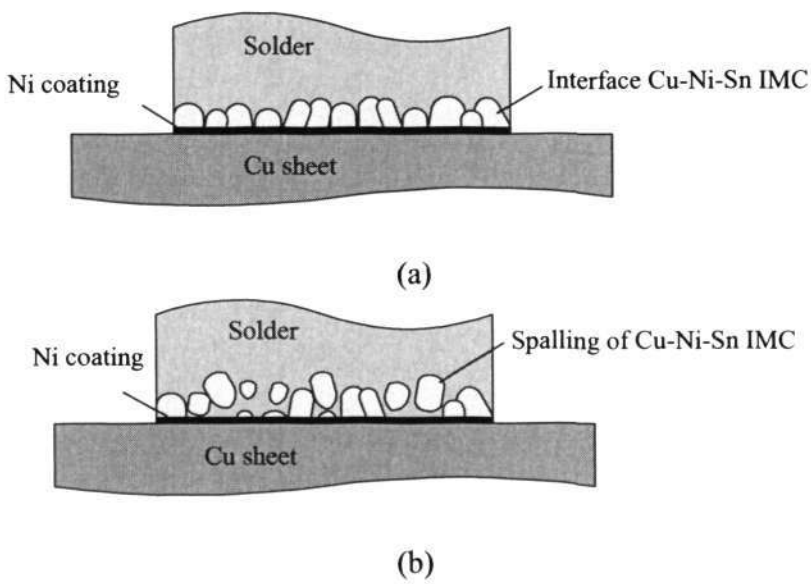


Figure 5.11 Schemitic diagrams depicting the phenomena of (a) ripening among the scallop-like IMC; (b) spalling of elongated-type IMC.

5.2.3 Interface Intermetallic Growth

Since the thickness of the interface IMC layer is an important factor and can affect the reliability of the solder joint, it is necessary to study the interface IMC growth trend as a function of isothermal aging temperature and time. Measurement of IMC thickness is not easy. The technique adopted in the present study is described in detail in Section 3.6.

The growth of the IMC layer is presented by plotting its average thickness with respect to aging time, as shown in Figure 5.12. The figure shows that at aging temperature of 125 °C, there was no significant growth of interface IMC layer even with exposure time of 336 hr. The interface IMC layer growth was more noticable at 150 °C and fastest at 175 °C. This can be attributed to the faster diffusion rate at higher temperature. As a whole, the IMC growth rates at 150 °C and 175 °C exhibit similar trend and the growth levelled off with the increase of aging time.

It was reported (Guan et al., 2000, Xiao et al., 2001, Young et al., 2001) that the atomic diffusion of Cu and Sn through the interface IMC layer is the main controlling process for the IMC growth during aging. The growth process that controlled by volume diffusion or by stationary grain boundary diffusion indicates that the growth kinetic of the interface IMC layer follows the square root time law, as expressed in equation below (see the derivation in Chapter 4),

$$h \cong \sqrt{Dt} \qquad [5.1]$$

where D is the diffusion coefficient and t is the aging time. The diffusion coefficient is given by an Arrhenius expression,

$$D = D_o \exp(-Q/kT) \qquad [5.2]$$

where D_o is the diffusion constant, Q is the activation energy, k is the Boltzman constant and T is the absolute temperature.

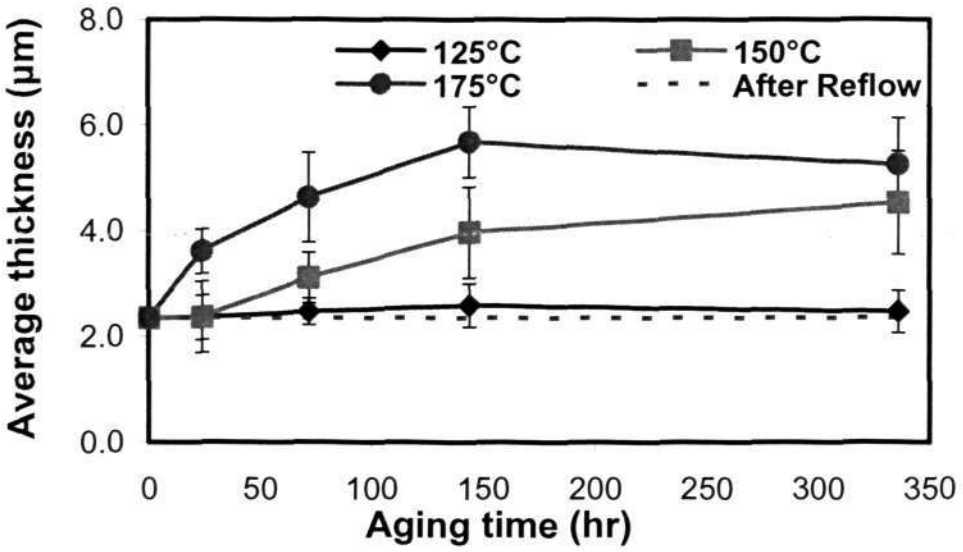


Figure 5.12 The average thickness of the of Cu-Ni-Sn IMC layer formed at the interface of the solder/copper joints that isothermally aged at 125, 150 and 175 °C for different aging time. After aging at 150 and 175 °C, the morphology of the interface Cu-Ni-Sn IMC layer became more irregular which leads to larger range of thickness value.

Based on the fore mentioned IMC growth kinetic, the IMC layer growth trend was reconstructed by plotting the average IMC layer thickness versus the square root of aging time, as shown in Figure 5.13. The plot shows that the growth of the Cu-Ni-Sn IMC layer was linearly proportional to square root of aging time up to 144 hr. The IMC growth trend lost its linear behavior when the aging time increased from 144 hr to 336 hr. The initial IMC growth rate was reconstructed and is shown in Figure 5.14. The last data point at 336 hr of all the three temperatures was discarded. As the plots in Figures 5.13 and 5.14 were derived from Figure 5.12, the range of IMC layer thickness with respect to aging time for all the three plots followed the same trend.

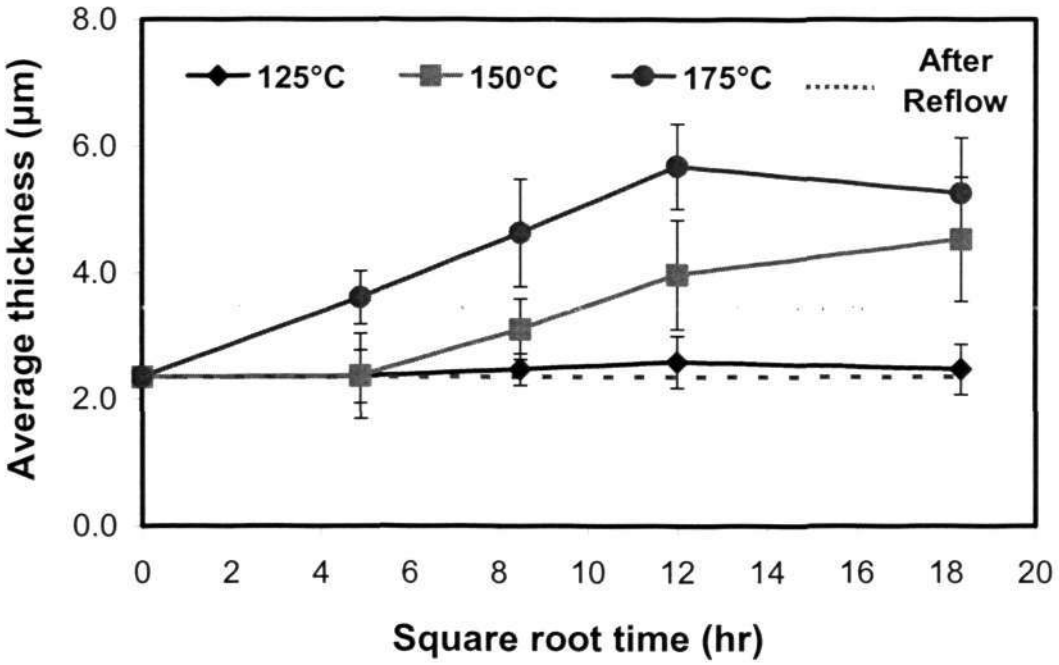


Figure 5.13 The average thickness of the of Cu-Ni-Sn IMC layer with respect to square root of aging time at 125, 150 and 175 °C.

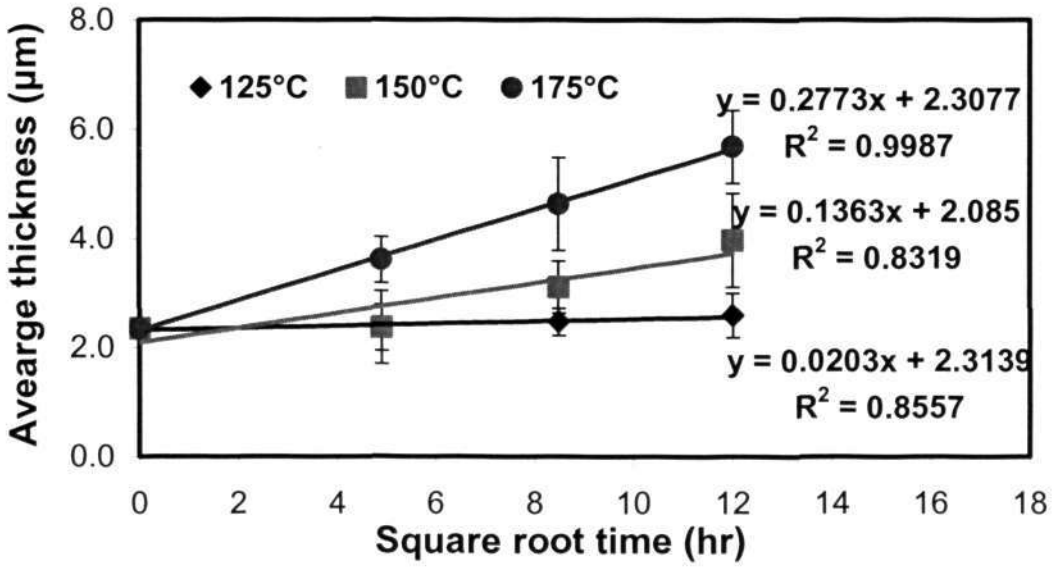


Figure 5.14 The initial IMC growth of Cu-Ni-Sn IMC layer with respect to square root of aging time at 125, 150 and 175 °C

The linear IMC growth trend failed to sustain for the longest aging time due to several reasons:

(a) The growing of Cu-Ni-Sn IMC was retarted by the limited supply of Ni flux from the diminishing ENIG coating;

(b) The ripening process of Cu-Ni-Sn IMC in multiple directions has masked the growing rate in the verical direction; and

(c) The formation of additional $(Ni,Cu)_3Sn_4$ phase between the $(Cu,Ni)_6Sn_5$ phase and ENIG coating that grows in much slower rate can also decrease the overall growth of rate of the IMC layers.

5.3 Effect of Thermal Cycling and Thermal Shock on IMC Growth in FR4-Solder Joint

The FR4-solder joint was formed by soldering a single solder ball to two FR-4 substrates printed with Cu pad coated with Ni/Au. A 95.5Sn-3.8Ag-0.7Cu lead-free solder ball with diameter of 0.5 mm was placed and secured with no-clean flux to the substrate. Details of the sample preparation and TC and TS procedures are described in Section 3.5. After the FR4-solder joint specimens were subjected to 500, 1000 and 2000 cycles of TC and TS, the microstructures across the solder/coating interface and at the regions near the edge and within the solder ball were carefully examined.

5.3.1 As-reflowed Microstructure

The microstructure and EDX results of the as-reflowed FR4-solder joint are shown in Figures 5.15, 5.16 and 5.17. The as-reflowed solder joint contains Sn-matrix and eutectic network, which consists of both granular Ag_3Sn and Cu_6Sn_5 IMCs.

Large Ag_3Sn plate-like IMCs were found mostly at the corners of the solder joint (Figures 5.15 (a) and (c), and 5.16). The formation of large plate-like Ag_3Sn IMC can affect the strength of the solder joint significantly (Kim et al., 2003). The large plate-like Ag_3Sn IMC can provide the secondary crack initiation site or the crack propagation site by interface sliding.

Needle-like of interface Cu-Ni-Sn IMC layer was found at the interface between solder/coating interface for the FR4-solder joint (Figure 5.15 (d)).

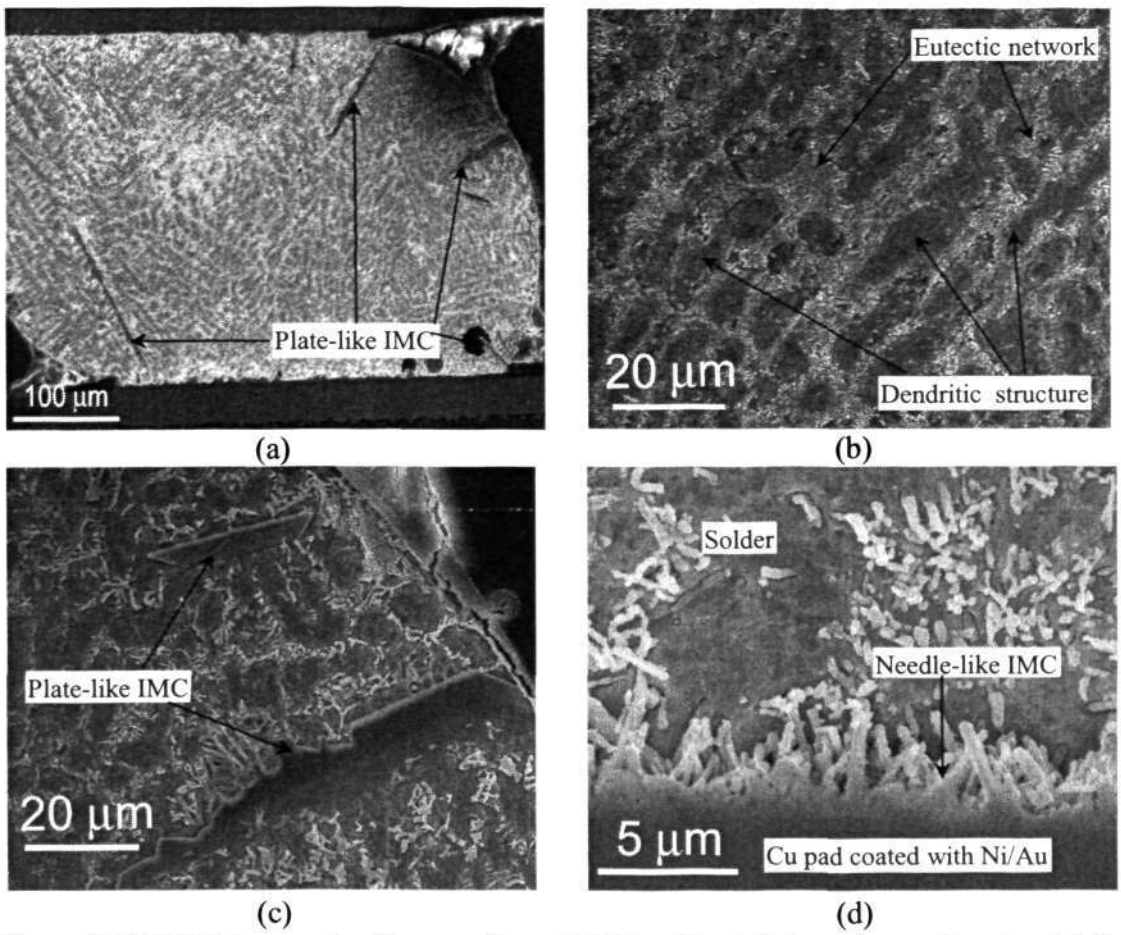


Figure 5.15 SEM images for the as-reflowed FR4-solder joint specimen showing (a) the overall view microstructure of the solder joint; (b) close-up view for the center region of (a); (c) close up view for the edge of the solder joint at the top right hand corner of (a); (d) close-up view of the interface IMC layer across the solder/coating interface

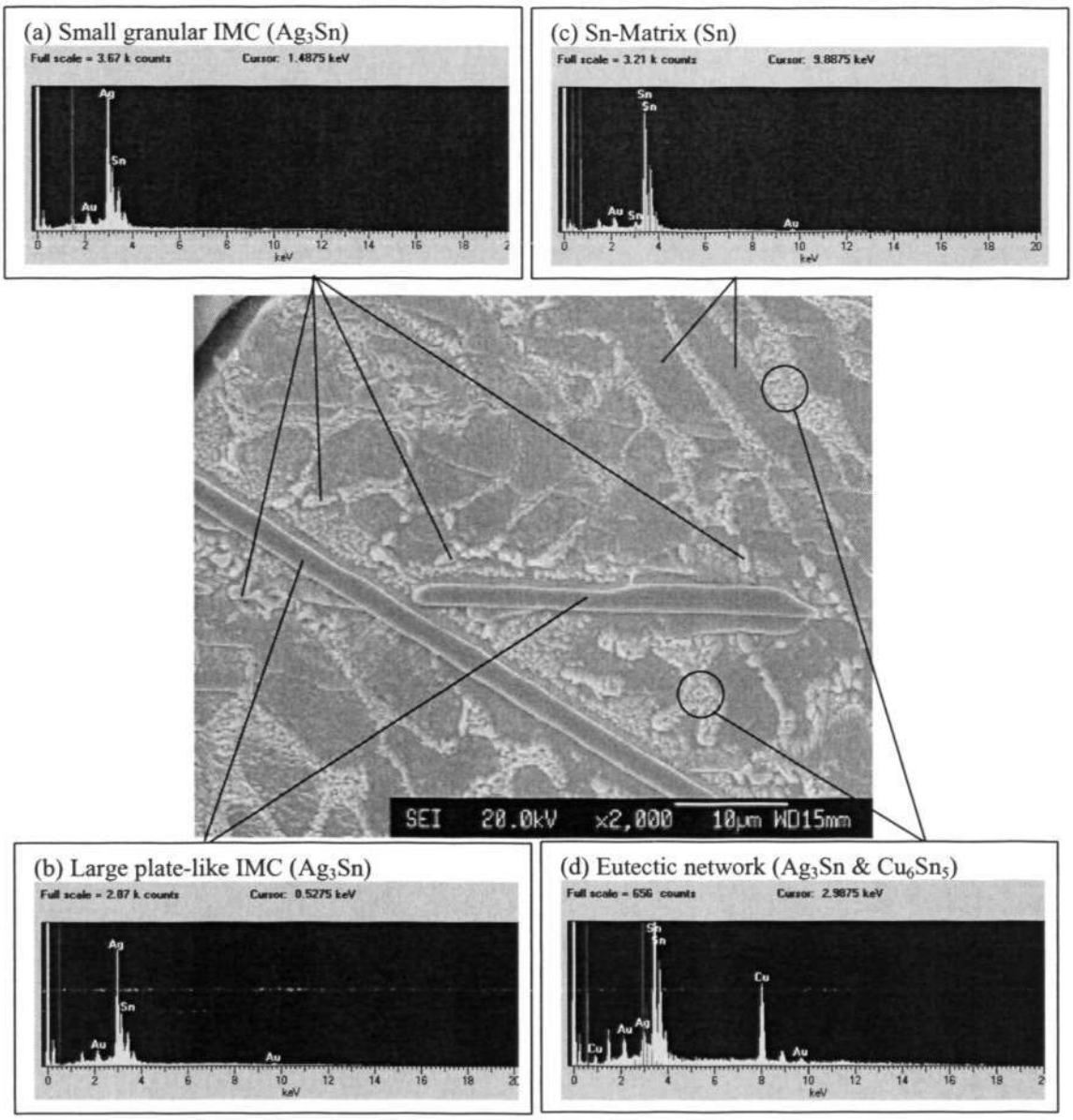


Figure 5.16 EDX spectrums of the (a) small granular Ag_3Sn IMC along the boundaies of the dentrictic structures surrounded the; (b) large-plate-like Ag_3Sn IMC and; (c) Sn-matrix within; (d) the eutectic netwrok consists of both Ag_3Sn and Cu_6Sn_5 IMC particles.

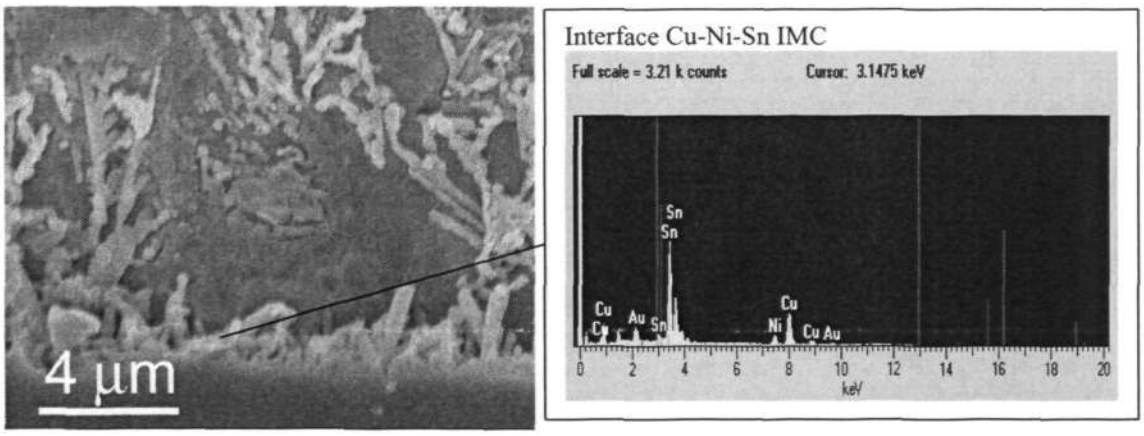


Figure 5.17 EDX spectrum of the interface IMC layer formed between the 95.5Sn-3.8Ag-0.7Cu lead-free solder and Ni/Au coating of the as-reflowed FR4-solder joint specimen.

5.3.2 Effect of TC and TS on Microstructure

SEM images of the FR4-solder joint after TC and TS for 500, 1000 and 2000 cycles are shown in Figures 5.18 and 5.19 respectively. Large plate-like Ag_3Sn IMC was still observable at the corners of the solder joint.

TC and TS do not have significant coarsening effect on the dendritic structure of the FR4-solder joint. As can be seen in Figure 5.20, FR4-solder joint still shows microstructure consisting of dendritic structure after 2000 cycles of TC and TS.

Under both TC and TS, cracks were observed to initiate from the edge of the solder joint and propagated along interface between the IMC layer and Ni/Au coating after 500, 1000 and 2000 cycles (Figures 5.18 (c) and 5.19 (c)). EDX analyses across the solder/coating interface show that cracking occurs at interface with P-containing phase (Figure 5.21).

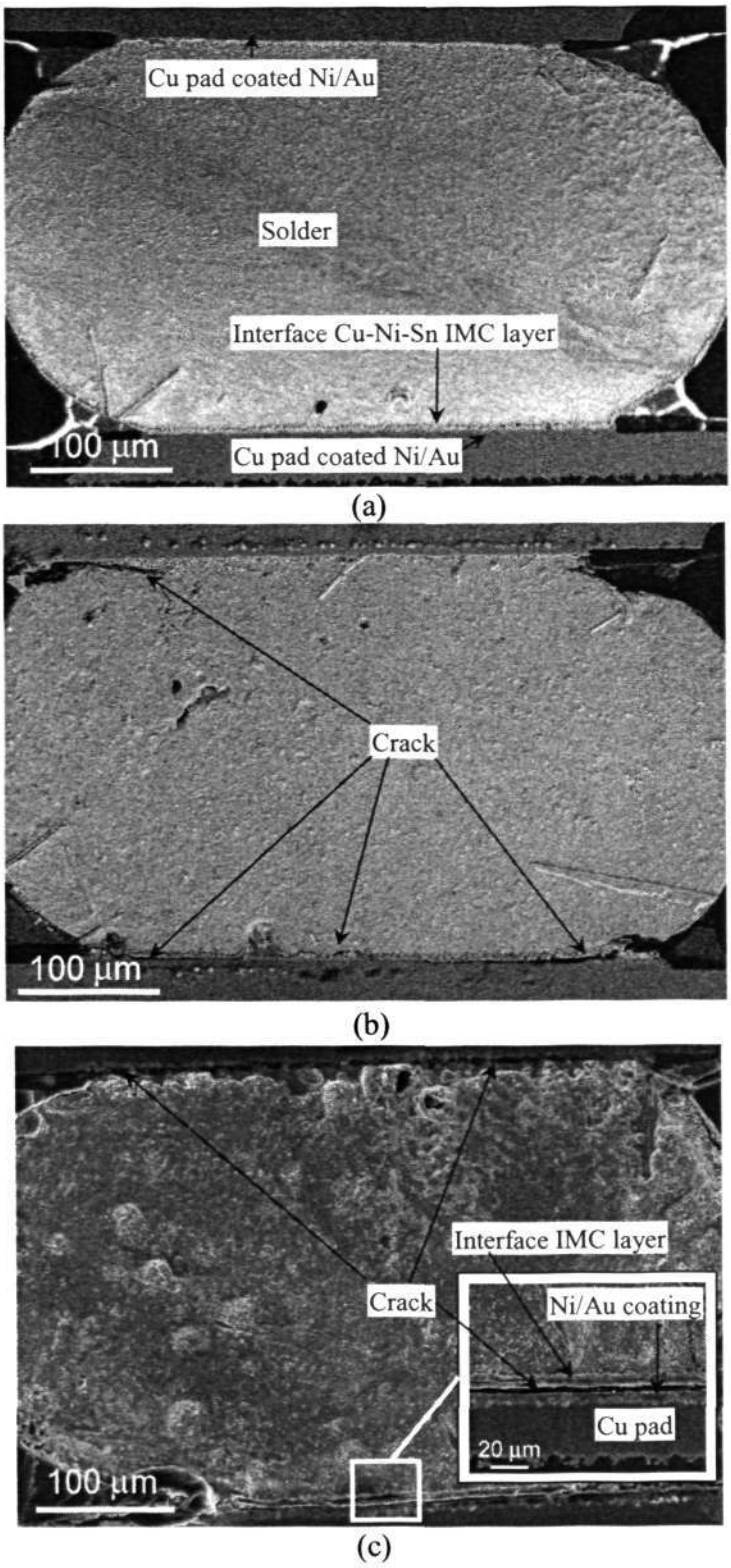


Figure 5.18 SEM images showing the overall cross-sectional views of FR4-solder joints after exposure to (a) 500; (b) 1000 and; (c) 2000 cycles of TC. Cracks can be seen at the interface between IMC layer and the Ni/Au coating. The rectangular insert in (c) shows the close up view of the clack near the interface.

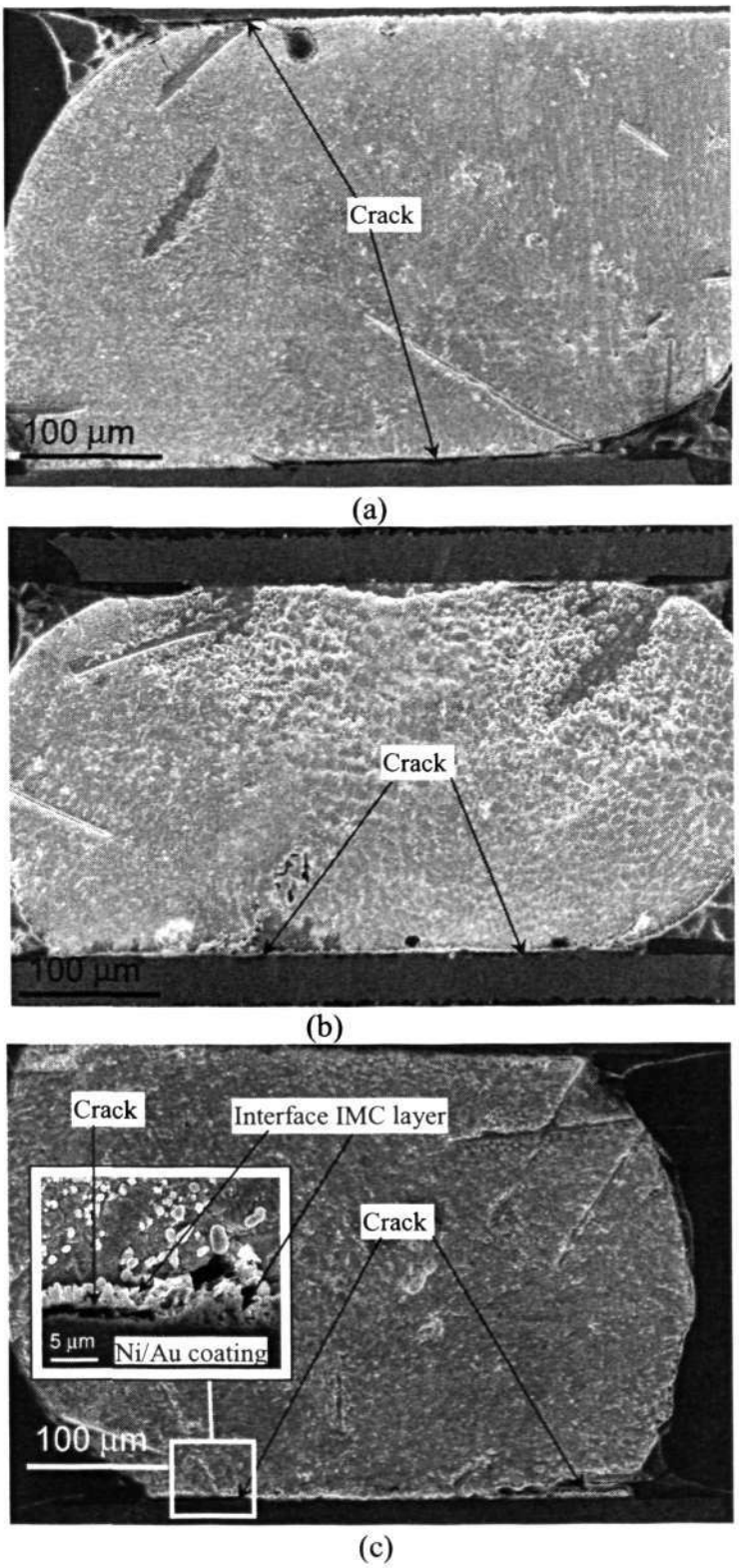
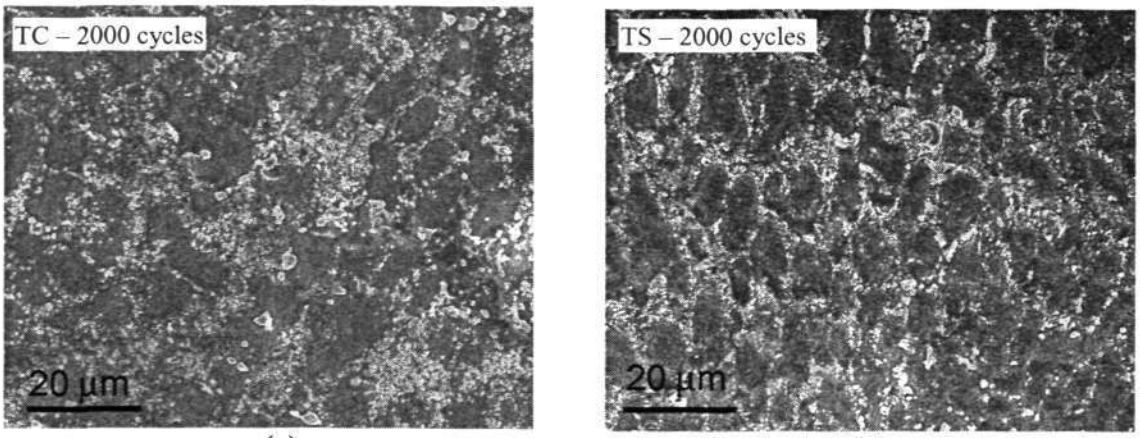
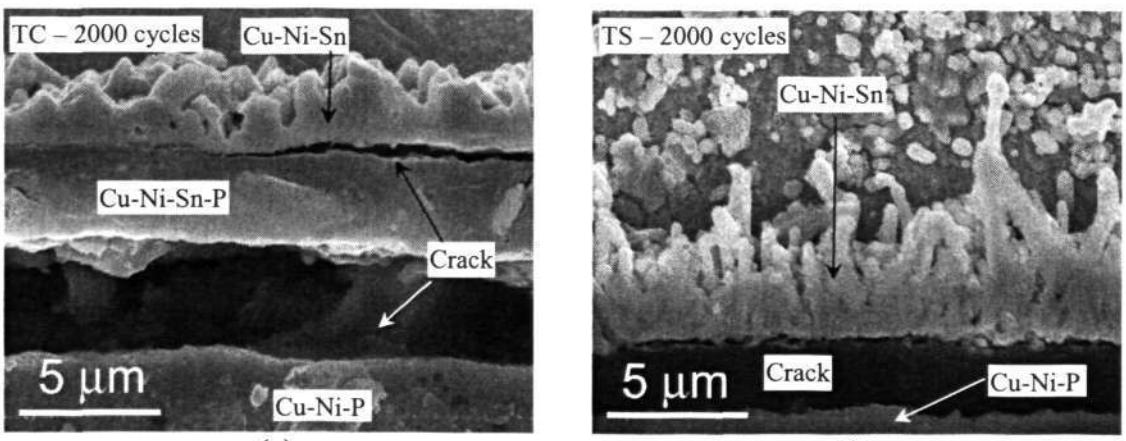


Figure 5.19 SEM images showing the overall cross-sectional views of FR4-solder joints after exposure to (a) 500; (b) 1000 and; (c) 2000 cycles of TS. Cracks can be seen at the interface between IMC layer and the Ni/Au coating. The rectangular insert in (c) shows the close up view of the clack near the interface.



(a) (b)

Figure 5.20 SEM images of the FR4-solder joint after exposure to 2000 cycles of (a) TC and (b) TS showing microstructures with dendritic morphology.



(a) (b)

Figure 5.21 SEM images of the FR4-solder joint after exposure to 2000 cycles of (a) TC and (b) TS tests showing severe cracks near the P-rich layer at the interface between the Cu-Ni-Sn IMC layer and Ni/Au coating

Under TC condition, the needle-like Cu-Ni-Sn IMC layer grew thicker with the increase of aging cycle (Figure 5.22). Figure 5.22 (d) shows that when TC reaches 2000 cycles, the Cu-Ni-Sn IMC layer grew into scallop-like morphology. In contrast, with 2000 cycles of TS, the interface Cu-Ni-Sn IMC layer remained in needle-like morphology (Figure 5.23 (d)) but increased in thickness.

The more moderate TC environment with slower ramp rates and longer holding time at the upper temperature limit of 125 °C allows the growth of interface Cu-Ni-Sn IMC to achieve by a combination of interfacial reaction and ripening processes. In contrast, the stress state is more pronounced in the TS environment (due to faster temperature change). There was only limited available time for the residual stresses to relax in a relatively short cycle time. Therefore, distinct interface IMC growing mechanism might occur under the TS condition.

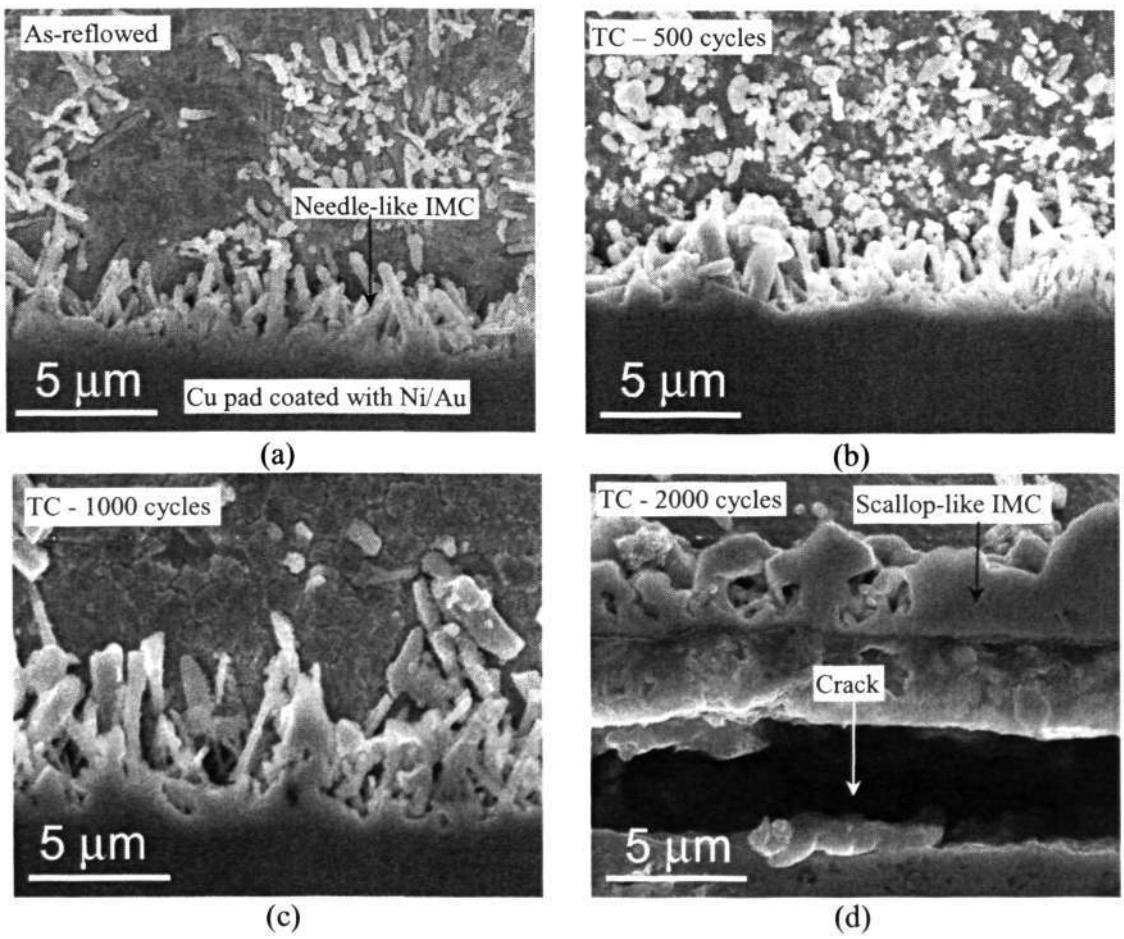


Figure 5.22 SEM images of FR4-solder joint showing the microstructure across the solder/coating interface under (a) as-reflowed condition and after exposure to TC for; (b) 500; (c) 1000 and; (d) 2000 cycles.

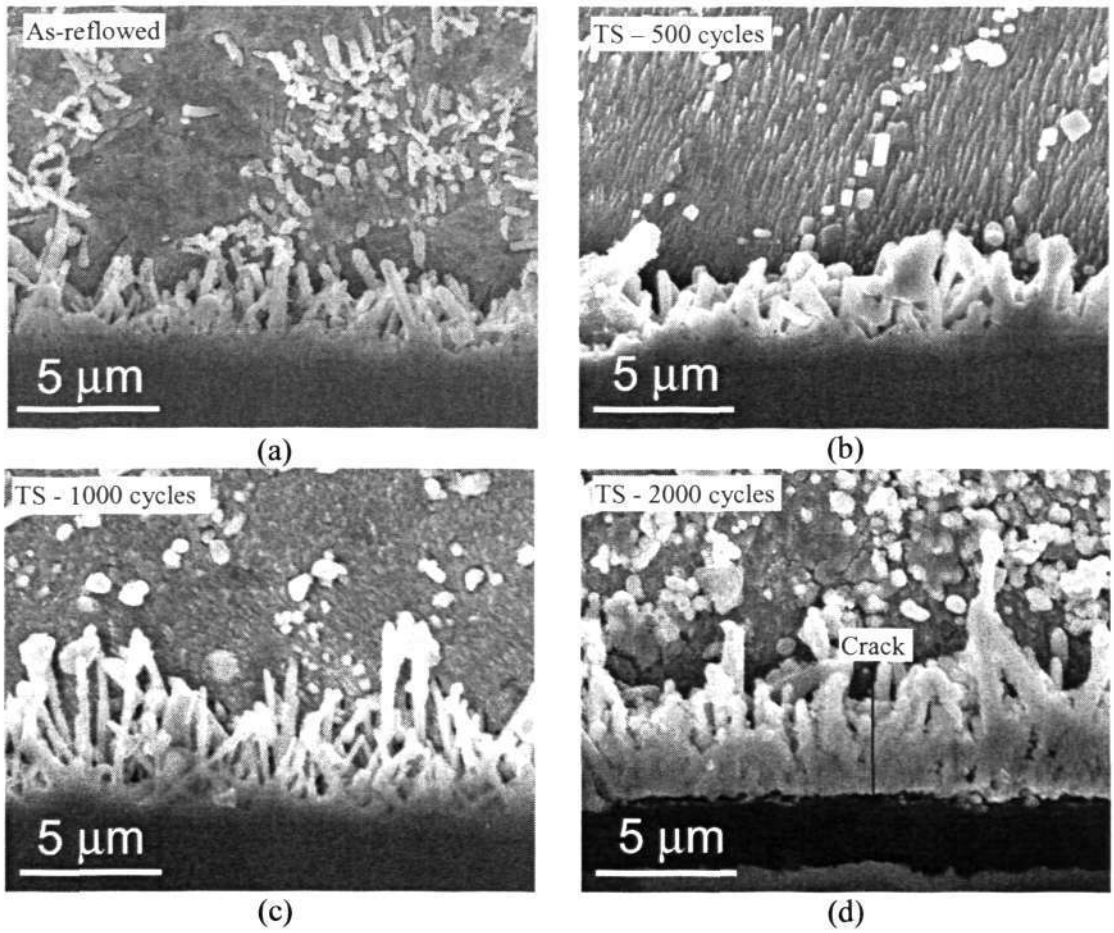


Figure 5.23 SEM images of FR4-solder joint showing the microstructure across the solder/coating interface under (a) as-reflowed condition and after exposure to TS aging for; (b) 500; (c) 1000 and; (d) 2000 cycles.

5.3.3 Intermatallic Growth Kinetics during TC and TS

The IMC growth kinetic analysis is not as simple as for the isothermal aging (section 5.2.3) because the temperature fluctuates with time during TC and TS. Here, the thickness of the interface Cu-Ni-Sn IMC layer is plotted against the square root of total accumulated dwell time at the maximum temperature (125 °C) rather than the total elapsed time required to complete each series of cycles (500, 1000 and 2000). Total accumulated dwell time at the maximum temperature of both TC and TS are considered to be the *effective aging time* that mainly contributes to the IMC growth. Diffusion at

the temperature lower than 125 °C is neglected to simplify the analysis. Figure 5.24 shows the growth of the Cu-Ni-Sn IMC layer for both TC and TS are linearly proportional to square root of *effective aging time*. It is interesting to note that the growth rate for TS is much faster than TC.

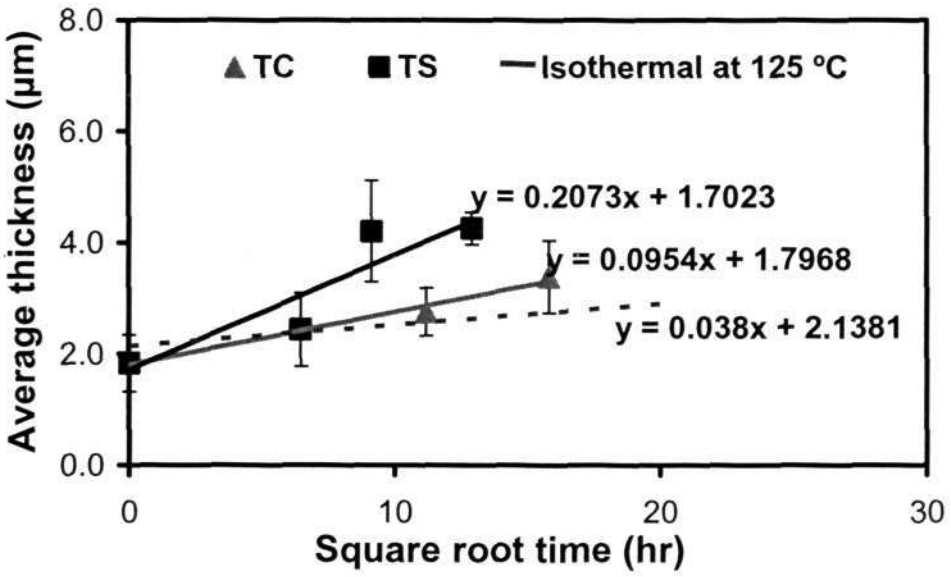


Figure 5.24 Growth of interface Cu-Ni-Sn IMC with respect to square root of total time exposed to 125 °C under isothermal, TC and TS aging tests.

From equation [5.1] indicating that the interface IMC growth kinetic follows the square root time, the IMC growth equations for TC and TS can be expressed as follows,

$$h_{TC} = \beta\sqrt{D_{TC}t} \qquad [5.3]$$

$$h_{TS} = \beta\sqrt{D_{TS}t} \qquad [5.4]$$

where D_{TC} and D_{TS} are the diffusion coefficient for TC and TS respectively, β is a constant and t is *effective aging time*.

From equations [5.3] and [5.4], the ratio of the D_{TC} and D_{TS} can be determined,

$$\frac{h_{TS}}{h_{TC}} = \sqrt{\frac{D_{TS}}{D_{TC}}} = \frac{0.2073}{0.0954} \approx 2 \qquad [5.5]$$

$$\frac{D_{TS}}{D_{TC}} \approx 4 \qquad [5.6]$$

That is to say, diffusion coefficient for TS, D_{TS} is about four times that of diffusion coefficient for TC, D_{TC}. This is a very interesting finding, considering that the solder tested in TC and TS is the same material. The finding indicates that other factors except temperature must play a role in accelerating diffusion in TS test and a plausible assumption is that the higher thermal stresses in TS test result in the much accelerated diffusion. It is not easy to measure the thermal stresses quantitatively; however, it is certain that thermal stresses are higher in TS test than in TC due to the following reasons:

(a) The temperature ramp rate is higher in TS than in TC, leading to greater temperature gradient and thus higher thermal stresses;

(b) The range of temperature change is greater for TS (-55 to 125 °C) than for TC (-40 to 125 °C); and

(c) In each temperature cycle the holding time at the highest temperature of 125 °C is considerably shorter for TS (5 min) than for TC (15 min), leading to much shorter thermal stress relaxation time for TS than for TC.

If the argument is correct, then the IMC growth in the isothermal condition is expected to be the lowest because isothermal aging does not involve fluctuation of temperature and thus does not produce additional thermal stresses. Indeed, it can be seen clearly from Figure 5.24 that the IMC growth is the lowest for the isothermal condition. Vianco et al. (1997) noted that TC and TS can accelerate the IMC growth

process compared to isothermal aging, leading further support to the argument in the present study.

5.4 In-situ Fractography of Solder/Copper Joint

In electronic packaging industry, solders are often used in the industry to attach device chips to packages and to join components to PCB. Mechanical fracture of solder joint is a major cause of failure and decreased reliability in electronic systems. Deformation model that predicts the service reliability of the solder joints often use data obtained from bulk test specimens that usually 10^4 to 10^5 times larger than the solder joint. Based on the concept of the "representative volume", the bulk test specimen can be used to predict the behavior of solder joint if the solder joint is larger than that the representative volume (Bonda and Noyan, 1996). However, the increased miniaturization of electronic component demands solder joint with much smaller size. This has caused the bulk test data fail to satisfy the "representative volume" criteria. Other than the volume effect, testing data from bulk specimen also failed to address the effect of interface IMC in affecting the mechanical fracture of the solder joint.

Therefore, the fine solder/copper joint with ENIG coating was used in this work to study the tensile fracture mechanism of the solder joints through in-situ fractography technique.

The challenge of this study is to monitor the real time fracture phenomenon of the solder/copper joint during testing. Therefore, a technique that combined the capabilities of SEM and mechanical testing device was developed for this study. A microtensile tester was installed inside an SEM to make it possible to carry out in-situ observation of deformation and fracture processes when the tensile test is going on.

5.4.1 Multiple-reflowed Solder/Copper Joint

Reflow soldering is one of the key soldering approaches to produce solder joints. During reflow, reaction between the solder and the surface finish occurs. In a real packaging process, it was normal for the solder joints to experience multiple solder reflow. The interface reaction continues to occur during the subsequent reflow processes. Therefore, there are concerns on the effect of multiple reflow on the reliability of the solder joint.

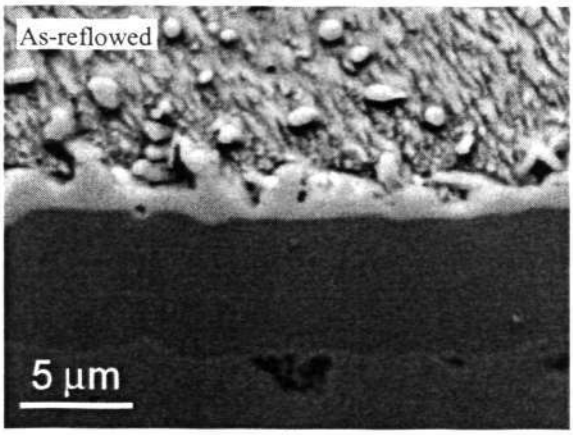
Solder/copper joint specimen with three different reflow conditions, i.e. as-reflowed (one time reflowed), three times reflowed and six times reflowed were tested for the in-situ observation. The solder/copper joint subjected to one time reflow is to simulate the as-reflowed condition. Three times reflow is the typical number of reflow cycles needed to rework the component. Six times reflow is the maximum number of reflow cycles allowed for the some of the components.

Figure 5.25 shows the SEM (BSE) images of the cross-sectional microstructures of the as-reflowed, three times reflowed and six times reflowed solder/copper joint specimens. The as-reflowed and three times reflowed solder/copper joint specimens show both continuous planar and non-continuous blocky Cu-Ni-Sn IMC layer. While slightly blocky IMC layer was observed from the six times reflowed solder/copper joint specimen.

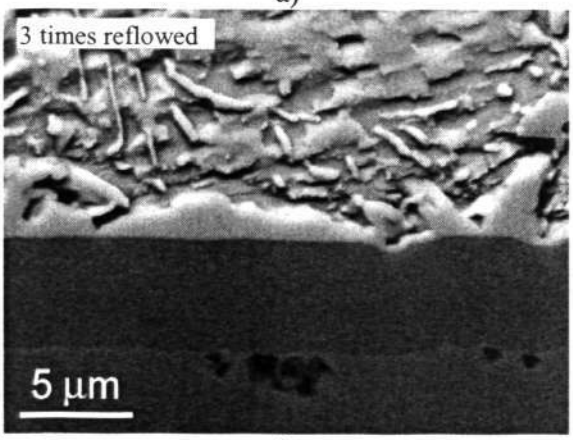
Under all the three reflow conditions, comparable interface IMC layer thickness was observed. Multiple reflow process up to six times has not resulted in excessive thickening of interface IMC layer.

A series of SEM (BSE) images show the fractography of the as-reflowed solder/copper joint during microtensile testing are shown in Figure 5.26. As can be seen

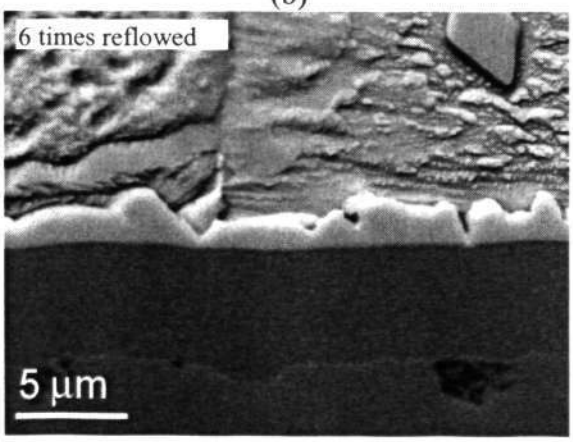
from these fractographs, the fracture of the solder joint was preceded by a moderate amount of area reduction. This is the common type of ductile fracture profile.



a)



(b)



(c)

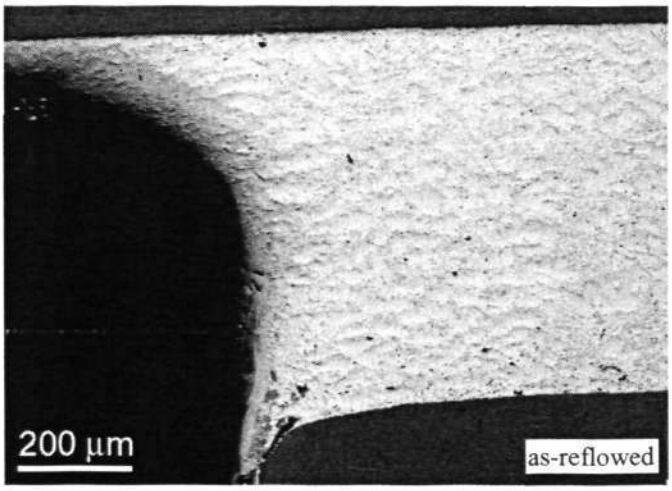
Figure 5.25 SEM (BSE) images showing cross-sectional microstructures of the interface IMC layer of the (a) as-reflowed (b) three times reflowed and (b) six times reflowed solder/copper solder joint specimens

As indicated as point-A in Figure 5.26 (b), crack started near the solder/coating interface when testing stress reaches the ultimate tensile stress at 30 MPa. Closer examination of this crack (Figure 5.27) shows that the cracking occurred at the interface between the IMC layer and the solder.

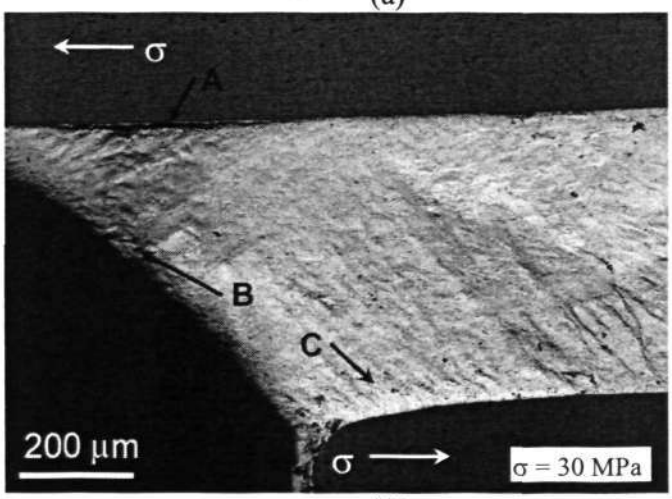
Other than the cracks near the solder/coating interface, some deformations can be observed near the solder free surface (point-B) and within solder region (point-C). Closer examination on one of these areas shows cracking occurred between equiaxial β-Sn grains. The cracking between β-Sn grains indicates that the micro-cracks developed between the β-Sn grains and evolved as a macro-crack when testing continued. The cracking along the grain boundaries between the β-Sn grains can be clearly seen from Figure 5.28.

Addition cracks near to the substrate (point-D) shown in Figures 5.26 (c) and (d) continued to form when the testing proceeded. As deformation continues, the micro and macro cracks continued to grow and coalesce. Cracks coalescence process caused the cracks to propagate within a few deformation areas. Finally, fracture followed by the rapid propagation of crack around the solder free surface (point-B).

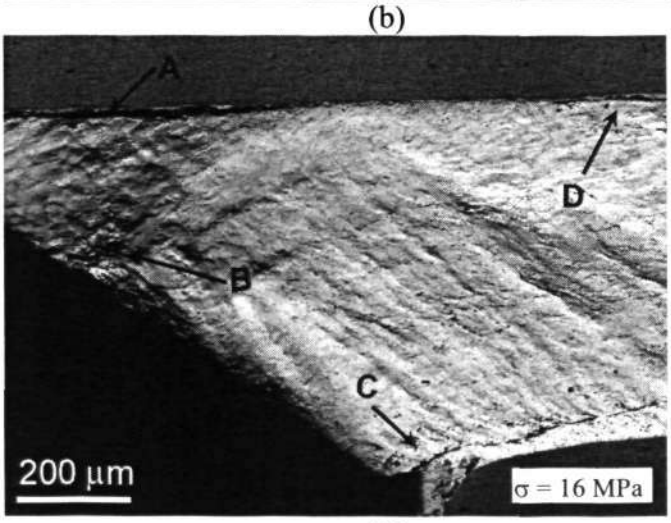
Figure 5.26(e) shows the shear deformation at an angle about 45° with tensile axis at the facture region. This indicated that the fracture had occurred when the stress level reaches its maximum level.



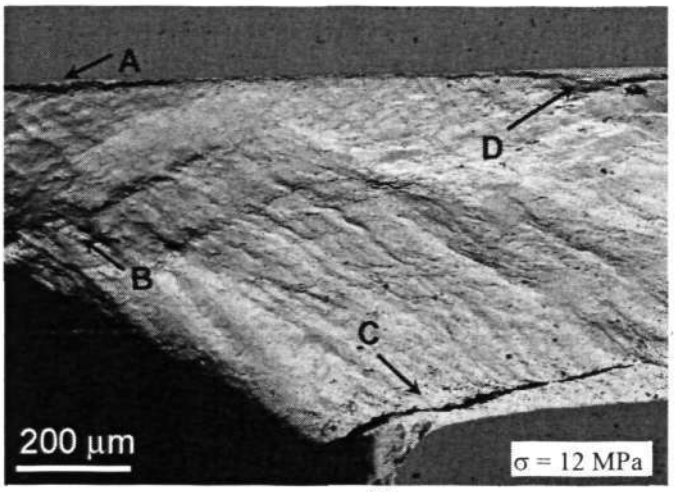
(a)



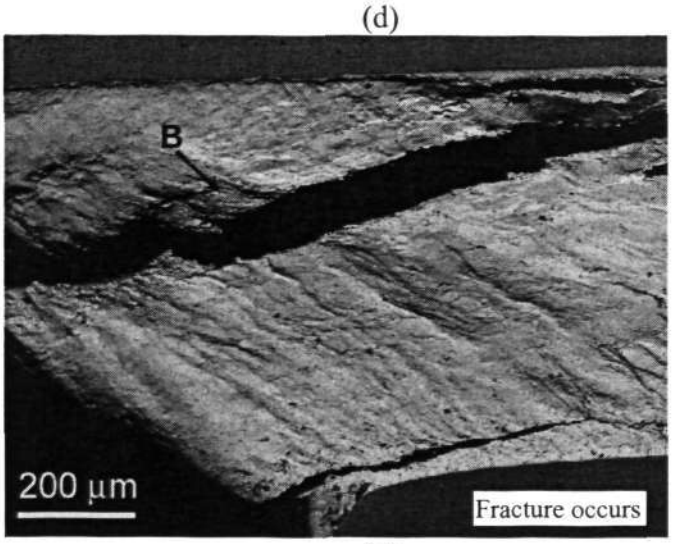
(b)



(c)



(d)



(e)

Figure 5.26 SEM (BSE) images show the fractography of the as-reflowed solder/copper joint at different stages of the micro-tensile test. (a) Initial condition. When tensile stress reaches (b) 30 MPa (Ultimate shear stress), (c) 16 MPa and (d) 12 MPa. (e) Fracture occurrs.

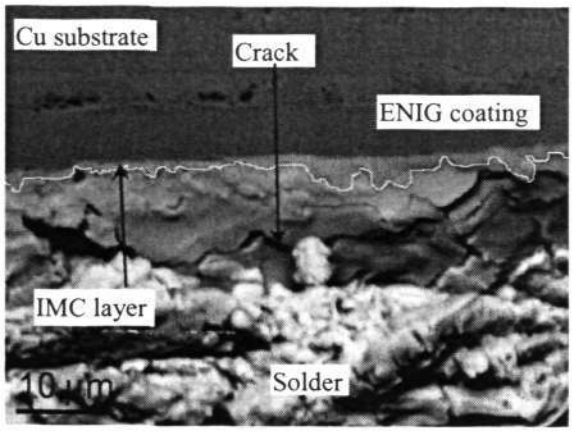


Figure 5.27 SEM (BSE) image of the as-reflowed solder joint showing the close up microstructure across the solder/coating interface (point-A) when the tensile stress reaches 26 MPa. Coalescence of micro-voids and micro-cracks were found within solder near to substrate (IMC layer is outlined in white line).

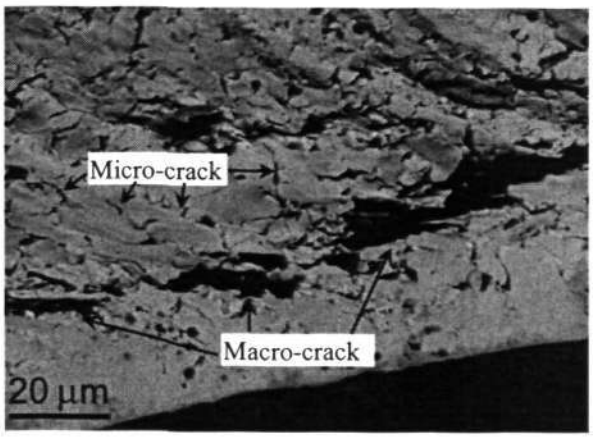
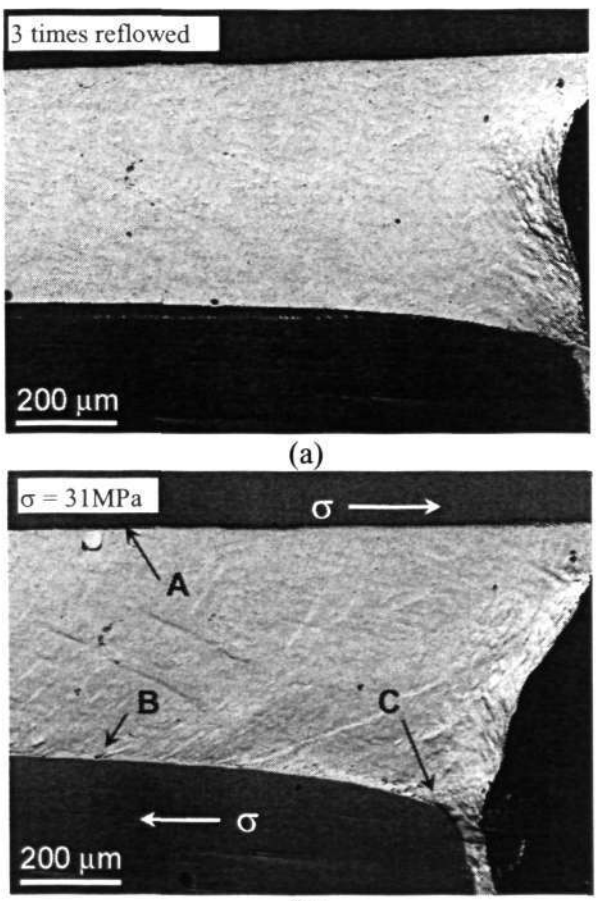


Figure 5.28 SEM (BSE) image of the as-reflowed solder joint showing the close up microstructure of the solder region (point-C) experienced plastic deformation during testing. Micro-cracks developed between β-Sn grains and evolved as a macro-crack.

Figure 5.29 shows a series of fractography of the three times reflowed solder/copper joint during the microtensile testing. Similar to the preceding in-situ observation on the as-reflowed specimen, cracks were first found at the areas near the

solder/coating interface as indicated as point-A, B and C in Figure 5.29 (b). The closer examinations (Figure 5.30) of these interface micro-cracks also show that they were located at the interface between the IMC layer and solder. When testing continues, more cracks were found to propagate along the interface regions (point-A, B, C and D) as shown in Figure 5.29 (c).

When the test continued, micro-voids and micro-cracks formed at point-E (Figure 5.29 (e)). They coalesced and propagated at an angle about 45° with tensile axis and resulted in the fracture of the specimen. The overall fracture mechanism observed from the three time reflowed specimen was found to be similar to the as-reflowed specimen.



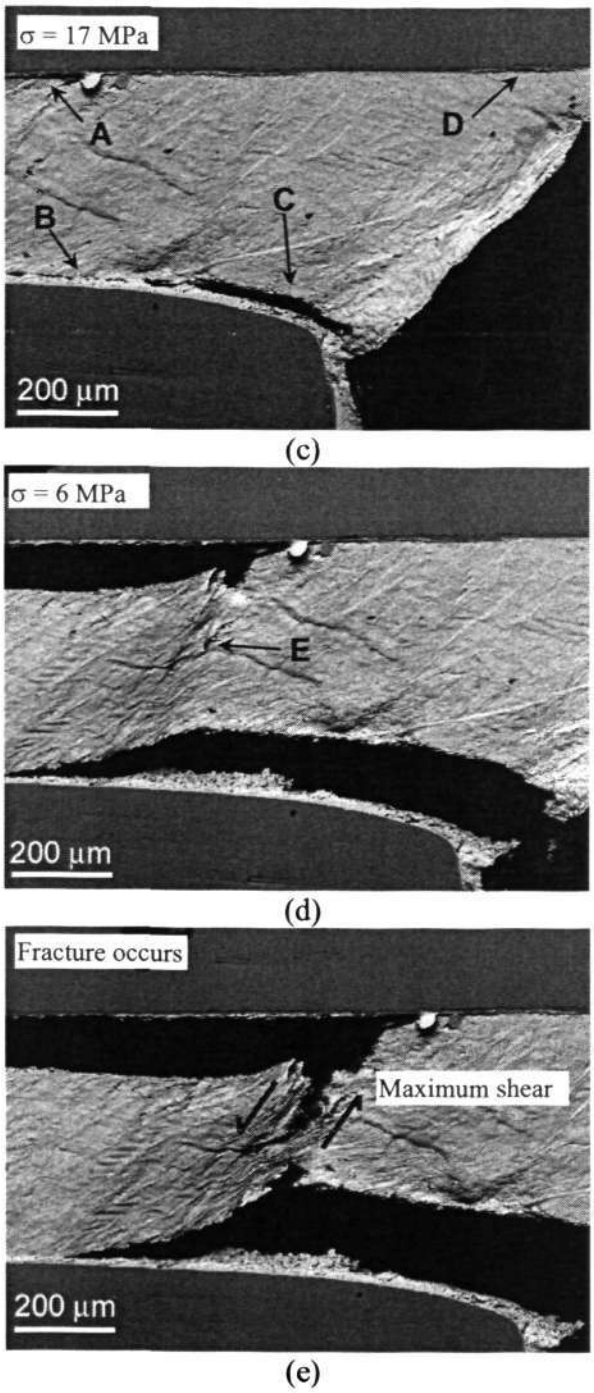


Figure 5.29 SEM (BSE) images show the fractography of the three times reflowed solder/copper joint specimen at different stages of the micro-tensile test. (a) Initial condition. When tensile stress reaches (b) 31 MPa (Ultimate shear stress), (c) 17 MPa and (d) 6 MPa. (e) Fracture occurs.

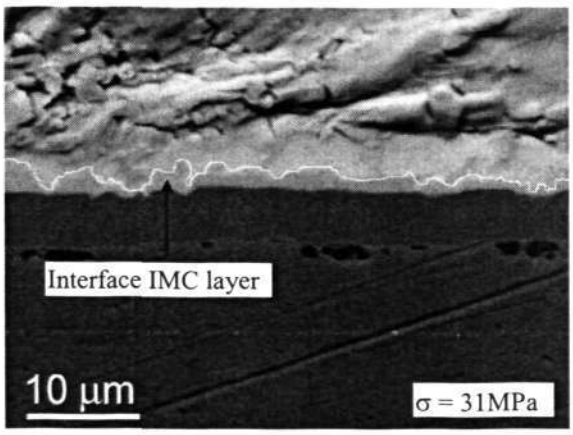
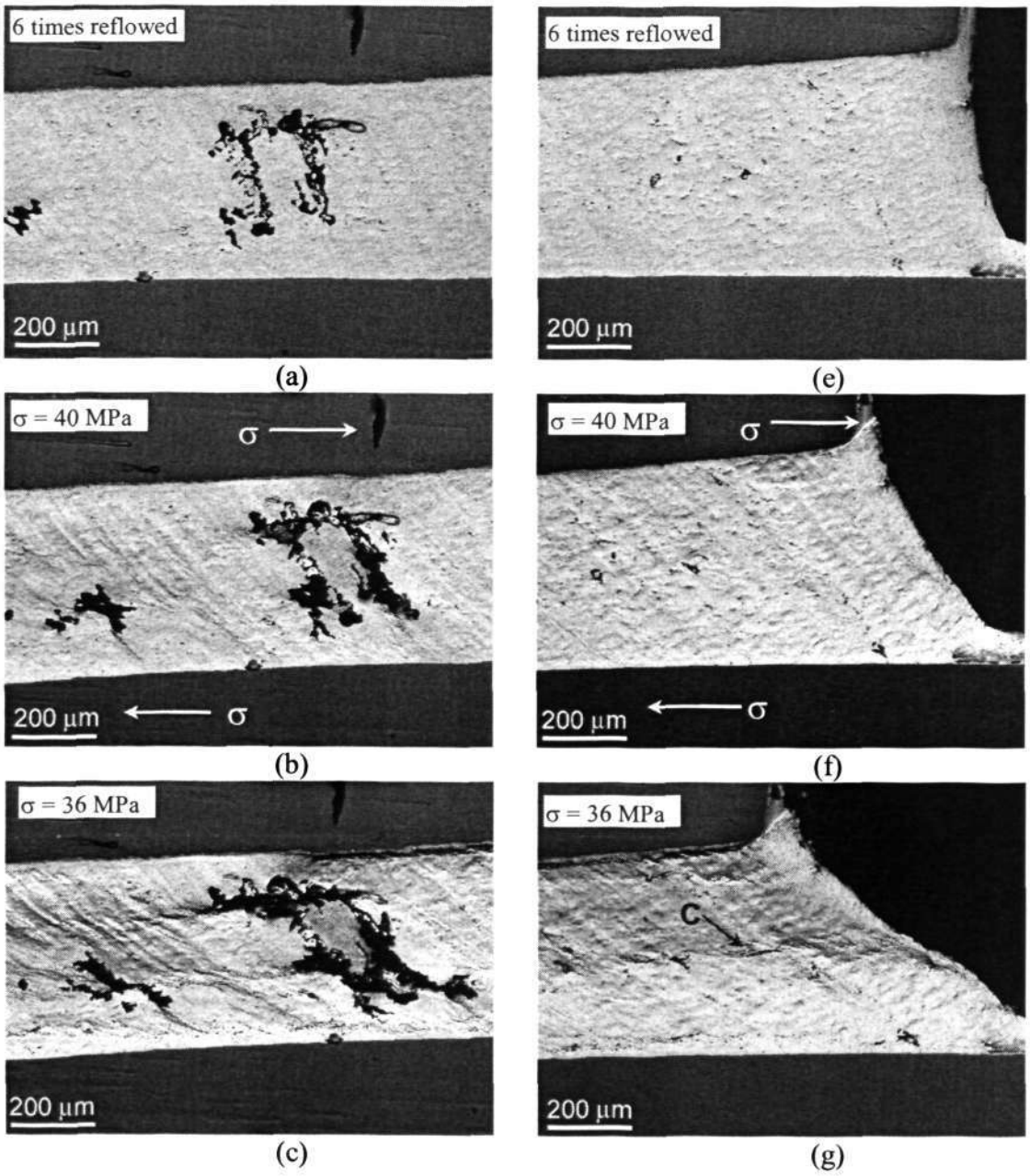


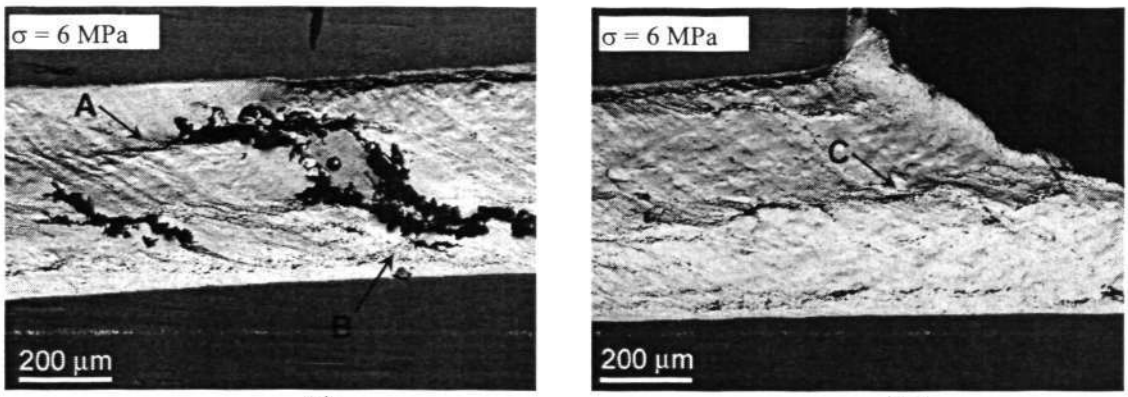
Figure 5.30 SEM (BSE) image shows the close up view of point-B in Figure 5.32 (b). Coalescence of micro-voids and micro-cracks were found within solder near to substrate (IMC layer is outlined in white line).

Large voids as shown in Figure 5.31 (a) can be seen from the solder/copper joint specimen after subjecting to six times reflow. Because of these pre-existing large voids, two series of the SEM (BSE) images show the fractography of the same specimen at two different regions (region with voids and the solder free surface at the right edge) were shown in Figure 5.31.

As shown in Figures 5.31 (a) to (d), the pre-existing voids deformed at the angle about 45° with the tensile axis. The voids coalesced with micro and macro cracks in the vicinity as indicated as point-A and B in Figure 5.31 (d).

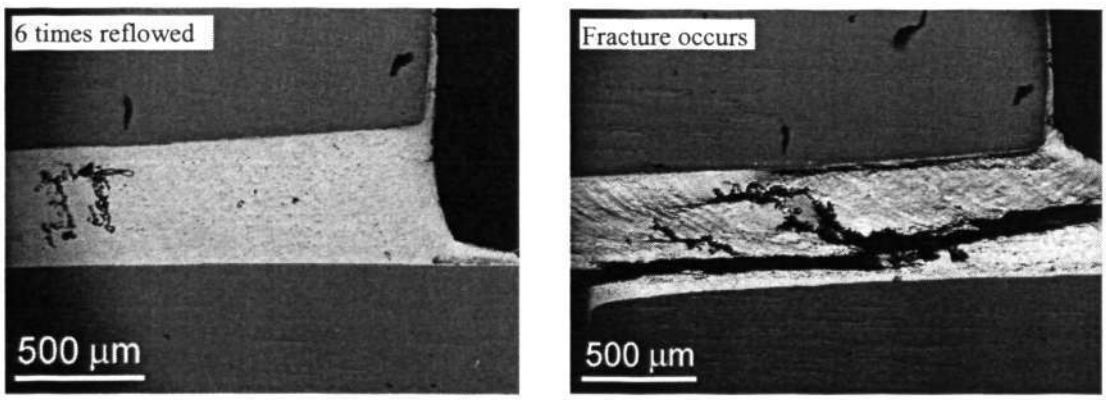
Figures 5.31 (e) to (h) show the propagation of crack near the free surface (point-C) of the solder as a resulted of the coalescence of micro and macro cracks formed during testing. Similar phenomenon was also observed at the other end of the solder joint during testing. The major cracks from the two ends of the specimen propagated rapidly and coalesced with the pre-existing void near the center region of the solder joint and caused fracture to occur (Figure 5.32 (b)).





(d) (h)

Figure 5.31 SEM (BSE) images show the fractography of the six times reflowed solder/copper joint specimen at different stages of the micro-tensile test. The solder region with pre-existing large voids (a) under initial condition, and when tensile stress reaches (b) 40 MPa (Ultimate shear stress), (c) 36 MPa and (d) 6 MPa. The solder free surface at the right edge of the specimen (e) under initial condition, and when tensile stress reaches (f) 40 MPa (Ultimate tensile stress), (g) 36 MPa and (h) 6 MPa.



(a) (b)

Figure 5.32 SEM (BSE) images of the six times reflowed solder joint showing (a) large voids in solder prior to testing and (b) Fracture followed by the propagation of crack through the pre-existing voids.

Under all the three reflow conditions, cracks initiated within the solder and progressed along the boundaries of β-Sn grains and resulted in intergranular fracture. Figure 5.33 shows the representative SEM (SEI) image of the solder/copper joint

fracture surface. Spherical dimples characteristic of ductile fracture was observed from all the three specimens.

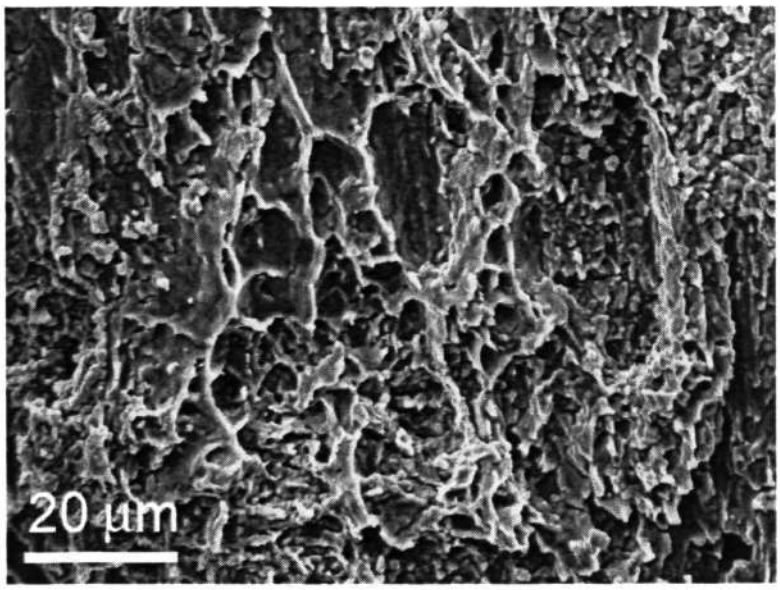


Figure 5.33 SEM (SEI) image showing the typical intergranular fracture on the solder/copper joint fracture surface.

5.4.2 Isothermal Aged Solder/Copper Joint

Effect of isothermal aging on the interface IMC layer of solder/copper joint was carried at three different temperatures at 125, 150 and 175 °C for different annealing times previously in this project. The results of the study were described in detail in section 5.2.

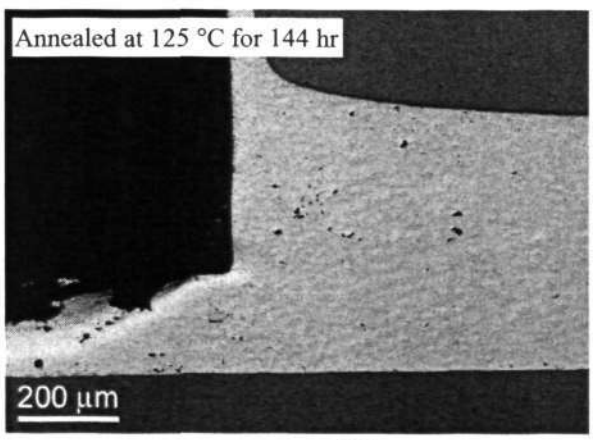
The study showed that increase of isothermal temperature from 125 to 150 °C was able to cause significant alteration of the solder's microstructure through coarsening process. Therefore, the microtensile test was performed on the solder/copper joint that exposed to isothermal aging at 125 and 150 °C for 144 hr for fracture mechanism study.

It was found that the solder/copper joint specimens exposed to isothermal aging at both 125 and 150 °C for 144 hr exhibited similar fracture mechanism. A series of SEM (BSE) images showing the fractography of the solder/copper joint isothermally aged at 125 °C for 144 hr are shown in Figure 5.34.

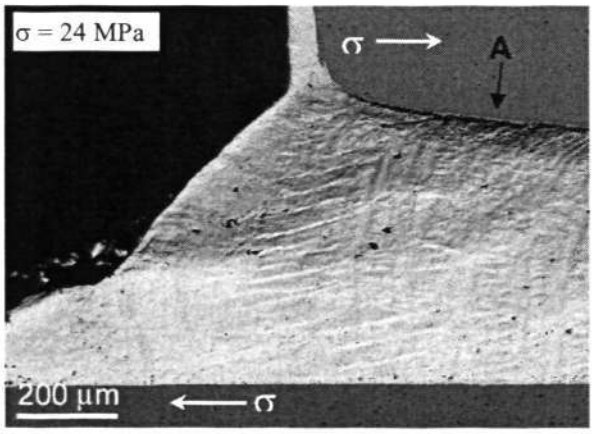
Cracks were observed to start forming near the solder/coating interface when stress reaches the ultimate shear stress of 24 MPa. Closer examination of this crack (Figure 5.35) shows that these cracks propagated along the interface between solder and IMCs grown from the substrate rather than within solder. This indicates that isothermal aging have resulted in the embrittlement interface IMC layer.

Closer examination within the solder region (Figure 5.36) shows that cracking also occurred between coarsened equiaxial β-Sn grains. Cracking between β-Sn grains indicates that the micro-cracks developed between the β-Sn grains and evolved as a macro-crack when testing continued. Cracking along the grain boundaries between the β-Sn grains can be clearly seen from Figure 5.36.

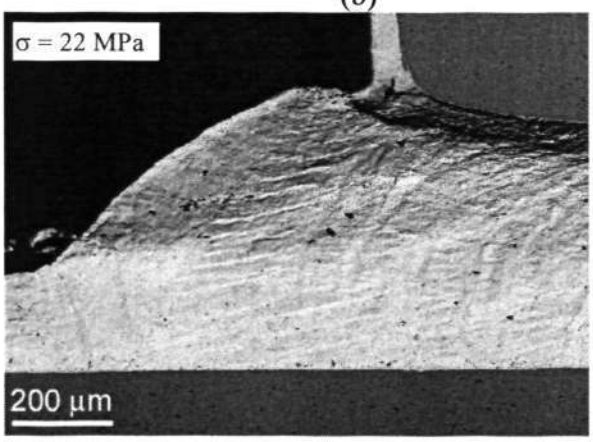
Figure 5.37 show shear deformation at an angle about 45° with tensile axis at the facture region. The same fracture pattern was observed from the solder/copper joint specimens under various reflow conditions (section 5.4.1).



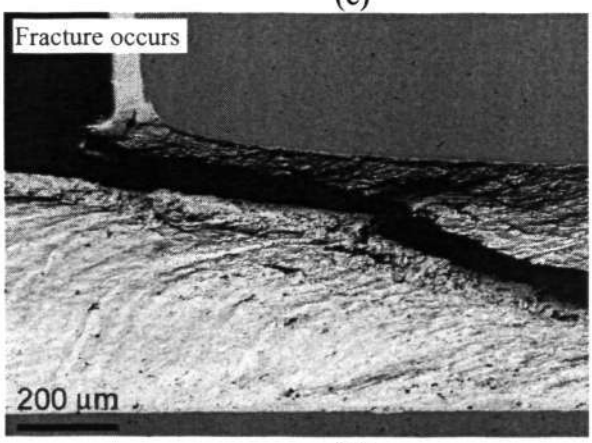
(a)



(b)

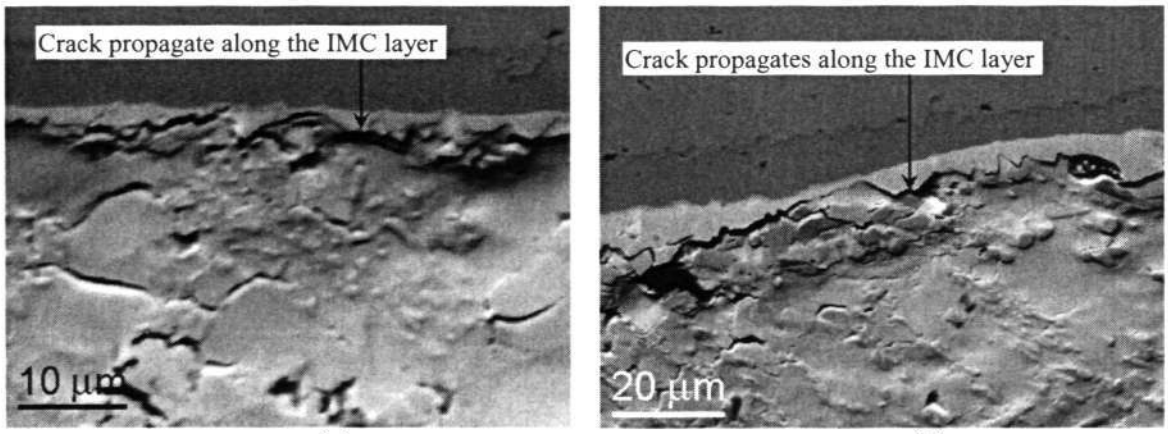


(c)



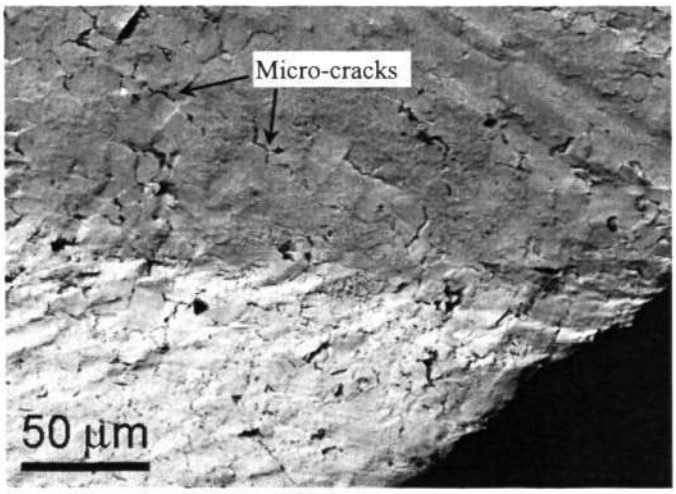
(d)

Figure 5.34 SEM (BSE) images show the fractography of the solder/copper joint specimen exposed to isothermal aging at 125 °C for 144 hr at different stages of the micro-tensile test. (a) Initial condition. When tensile stress reaches (b) 24 MPa (Ultimate shear stress), (c) 22 MPa and, (d) Fracture occurrs.

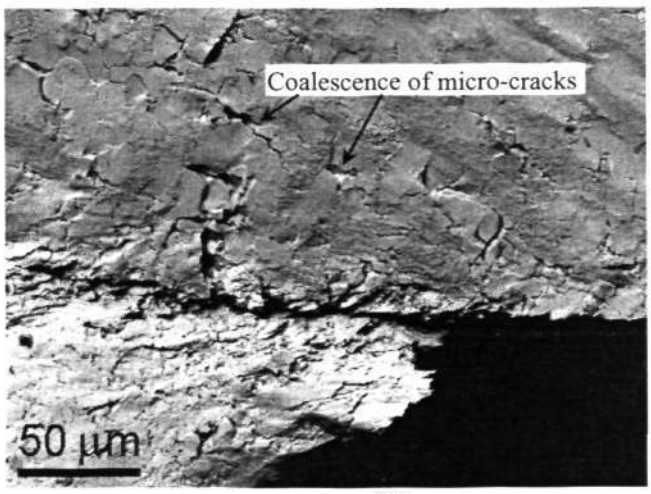


(a) (b)

Figure 5.35 SEM (BSE) images show the close up view of the cracks near the solder/coating interface of the solder/copper joints after exposure to isothermal aging at (a) 125 °C and (b) 150 °C for 144 hr. Both specimens show crack propagates along the IMC layer.



(a)



(b)

Figure 5.36 SEM (BSE) images show the fractography of the solder/copper joint specimen exposed to isothermal aging at 125 °C for 144 hr at two different stages during plastic deformation. Micro-cracks developed between □β-Sn grains and evolved as a macro-crack.

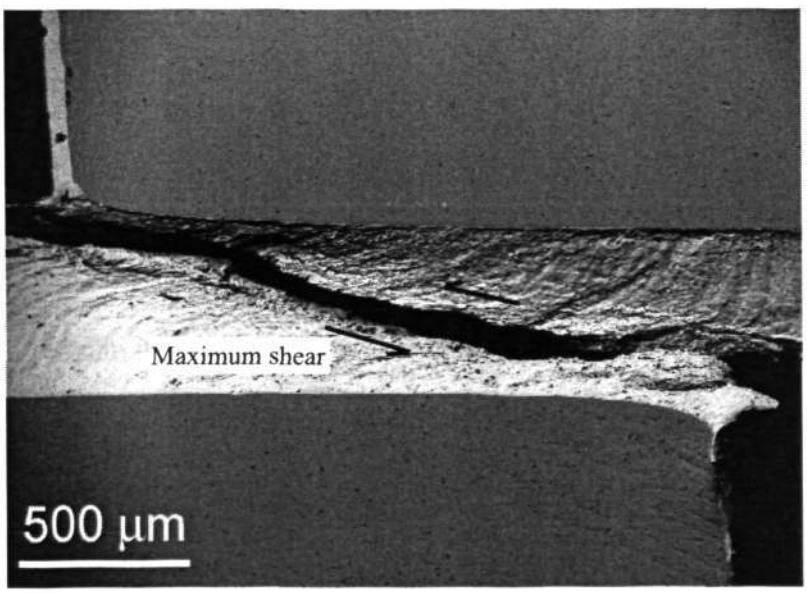


Figure 5.37 SEM (BSE) images show the fractography of the solder/copper joint specimen exposed to isothermal aging at 125 °C for 144 hr when complete fracture occurred. Shear deformation about 45 ° with the tensile axial was observed.

Intergranular fracture was also observed from these isothermally aged solder joints. As can be seen from Figure 5.38, the SEM (SEI) image shows that the solder/copper joint fracture surface consists of spherical dimples characteristic of ductile fracture.

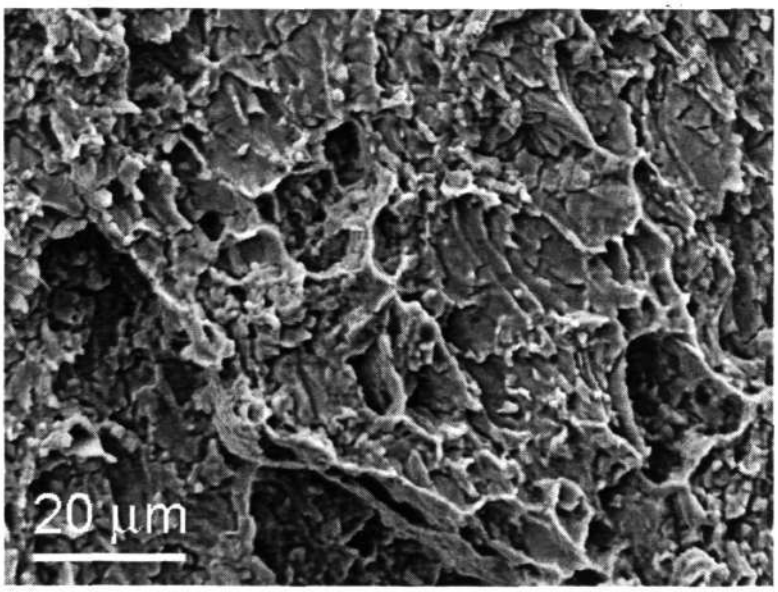


Figure 5.38 SEM (SEI) image showing the typical intergranular fracture of the solder/copper joint fracture surface under both isothermally aged at 125 and 150 °C.

5.5 Summary and Conclusions

Effect of isothermal aging on the IMC of solder/copper joint (95.8Sn-3.5Ag-0.7Cu lead-free solder with ENIG/Cu substrate) was carried at three different temperatures of 125, 150 and 175 °C. Coarsening of IMC in solder occurs at all three temperatures for extended aging time. The increase of temperature results in faster coasening process.

The growth of interface IMC layer was negligible for isothermal aging at 125 °C. The interface IMC growth is proportional to the square root time at 150 and 175 °C.

However, the growth failed to sustain for extend time. This can due to some possible reasons:

(a) The growing of Cu-Ni-Sn IMC was retarted by the limited supply of Ni flux from the diminishing ENIG coating;

(b) The ripening process of Cu-Ni-Sn IMC in multiple directions has masked the growing rate in the verical direction; and

(c) The formation of additional $(Ni,Cu)_3Sn_4$ phase between the $(Cu,Ni)_6Sn_5$ phase and ENIG coating that grows in much slower rate can also decrease the overall growth of rate of the IMC layers.

Effect of nonisothermal aging on the IMC was performed by subjecting the FR4-solder joint (95.5Sn-3.8Ag-0.7Cu with Ni/Au/Cu) to 500, 1000 and 2000 cycles of TC and TS. Coarsening of IMC in solder was not observable under either TC or TS condition. The growth of the Cu-Ni-Sn IMC layer for both TC and TS is linearly proportional to square root of total accumulated dwell time at maximum temperature (125 °C). It is interesting to observe that the interface IMC growth is considerably faster in TS than in TC and the faster growth in TS is attributed to the accelerated diffusion resulted from the higher thermal stresses in TS. The argument of stress-induced IMC growth is further examined in the next chapter.

An in-situ fractography technique was used to study deformation and fracture of the solder/copper joints. Both as-reflowed and isothermally aged joints were tested. The fracture was found to be predominantly intergranular for all the joints. The major fracture path is within the solder near the substrate for the as-reflowed joints (one, three or six times flowed) but along the interface between solder and IMCs grown from the substrate for the joints isothermally aged at 125 and 150 °C, indicating embrittlement of IMCs caused by the aging treatment.

Chapter 6: Effect of Stress State on Interface Intermetallics

6.1 Introduction

As reported in the last chapter, under various thermal loading conditions, the interface IMC growth is negligible under isothermal aging, easily observable under TC condition, and the fastest in the TS condition. The accelerated IMC growth is attributed to higher thermal stresses generated in TC and TS conditions. In order to have a better understanding on the effect of stress on IMC growth, a method has to be developed that allows the effects of temperature to be decoupled from the stress, i.e. stress level can be varied independently of temperature. Therefore, a novel technique was developed to make it easy to carry out quantitative study of the stress effect on interface IMC growth.

In this research, the C-ring technique was used to carry out study on the stress effect on IMC growth at the interfaces between 95.8Sn-3.5Ag-0.7Cu lead-free solder and Cu substrate with four different surface finishes. The four surface finishes are: Cu substrate coated with electroless Ni immersion Au (ENIG), Cu substrate coated of electroless Ni/Pb immersion Au (ENEPIG), bare Cu substrate (without coating), and Cu substrate coated with immersion Sn.

6.2 Interface IMC between Solder/ENIG Coated Cu Substrate

Ni/Au two-layer metallization is one of the most common surface finishes for Cu soldering pads in many electronic packaging assemblies. The introduction of lead-free solder alloy has caused the Ni-based metallization to draw a lot of attentions as an alternative lead-free surface finish. Over the past years, ENIG coating continues to be applied significantly in the electronics industry for its excellent planarity, solderability

and wire bondability during multiple solder reflow, wave soldering and/or aluminum wire bonding operations in the assembly process.

6.2.1 As-reflowed Microstructure

Figure 6.1 shows schematic diagram of the two solder/coating diffusion couples on the inner and outer surfaces of the as-reflowed ENIG coated C-ring solder joint. The cross-sectional microstructures of the interface IMC layers are shown in Figure 6.2. The morphologies and the thickness of the interface IMC layers on the inner (Figure 6.2 (a)) and outer (Figure 6.2 (b)) surfaces were comparable under as-reflowed condition (without the presence of external applied stress). The interface IMC layer shows both continuous planar IMC and discontinuous blocky shaped IMC. The solder on both inner and outer surfaces was heavily etched to make it possible to take a planar view of the interface. The planar view image, as shown in Figure 6.3, reveals islands of small needle-like IMCs surrounded by the large blocky hexagonal-shape IMCs.

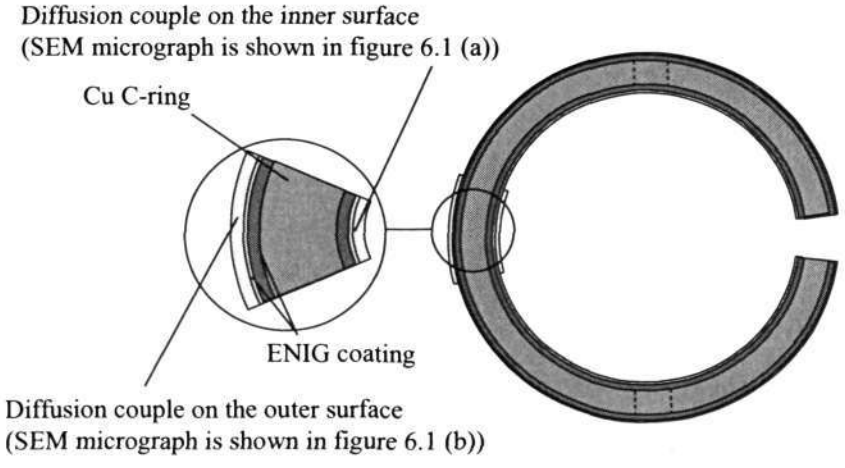
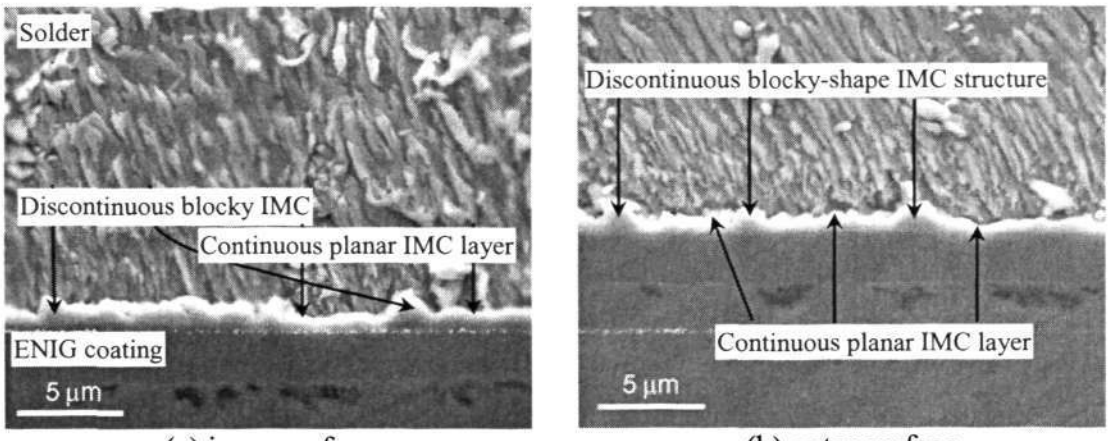
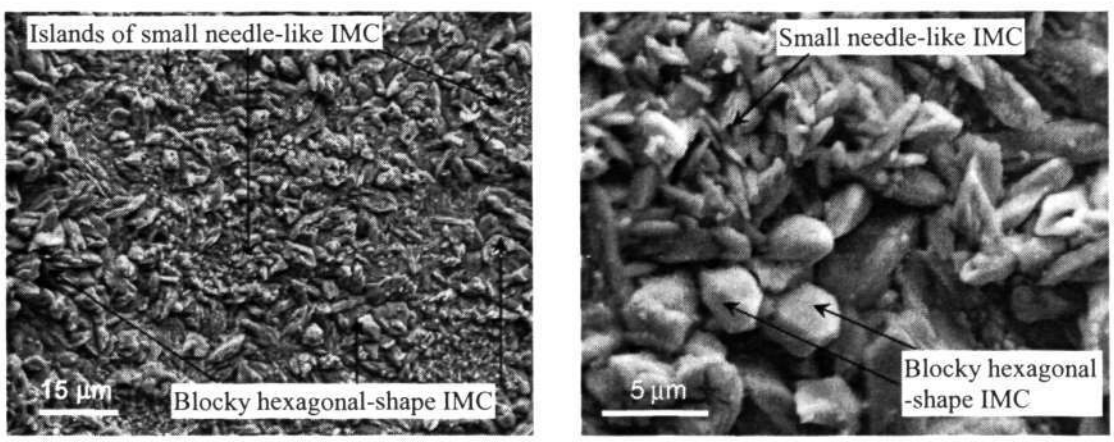


Figure 6.1 Schematic diagram of the as-reflowed ENIG coated C-ring solder joint. The microstructures of the interface IMC layer on the inner and outer surfaces (as indicated in the diagram) are shown in Figure 6.2 (a) and (b) respectively.



(a) inner surface (b) outer surface

Figure 6.2 SEM (SEI) images showing cross-sectional microstructures of interface IMC layer on the (a) inner and; (b) outer surfaces of the as-reflowed ENIG coated C-ring solder joint. Continuous planar IMC layer and discontinuous large blocky IMCs were observed on both surfaces.



(a) (b)

Figure 6.3 SEM (SEI) images of the as-reflowed ENIG coated C-ring solder joint showing the (a) overall planar view of the interface IMC layer consists of islands of small needle-like IMCs surrounded by large and blocky hexagonal-shape IMCs; (b) close up view of the IMC layer.

The EDX results (Figure 6.4) show that Cu, Ni and Sn elements were detected from the as-reflowed interface IMC layer. The distribution of these elements across the

solder/ENIG coating interface are shown in Figure 6.5. Concentration of Sn was highest (≈ 95 %) within the solder region. It maintained at about 65 % across the IMC layer and decreases progressively toward ENIG coating layer and Cu substrate. The concentration of Cu and Ni were low in solder region. Their Concentrations increased and maintained at about 20 % and 15 % in the IMC layer respectively. Concentration of Ni increased progressively from solder to ENIG coating layer and diminished towards the Cu substrate. In contrast, Cu decreased gradually through the ENIG coating and rose tremendously when approaching the coating/Cu substrate interface.

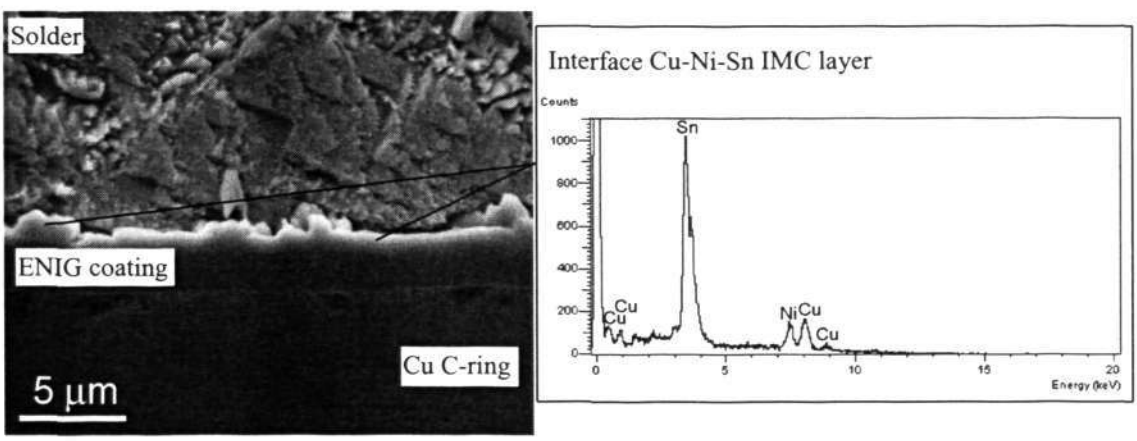


Figure 6.4 EDX spectrum for the IMC layer at solder/coating interface of the as-reflowed ENIG coated C-ring solder joint.

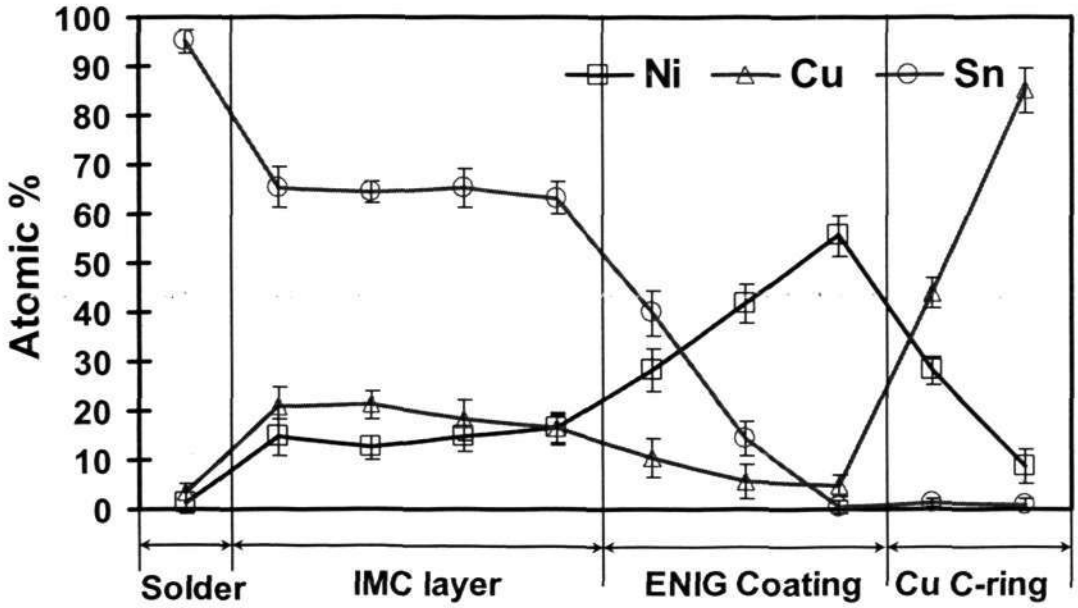


Figure 6.5 Plot of Cu, Ni and Sn distribution profiles across the solder/coating interface of the as-reflowed ENIG coated C-ring.

6.2.2 Effect of in-plane Tensile and Compressive Stresses on Interface IMC

The C-rings were tightened to produce two different stress levels in the solder σ_s, 10 MPa and 5 MPa, to study effect of stress level on the interface IMC growth. The results on C-rings stressed to 10 MPa are reported first. The C-rings in this category were annealed at a fixed temperature 125 °C for varying times (100, 168, 336, 2000 and 4000 hr) to monitor change of the interface IMC thickness with time.

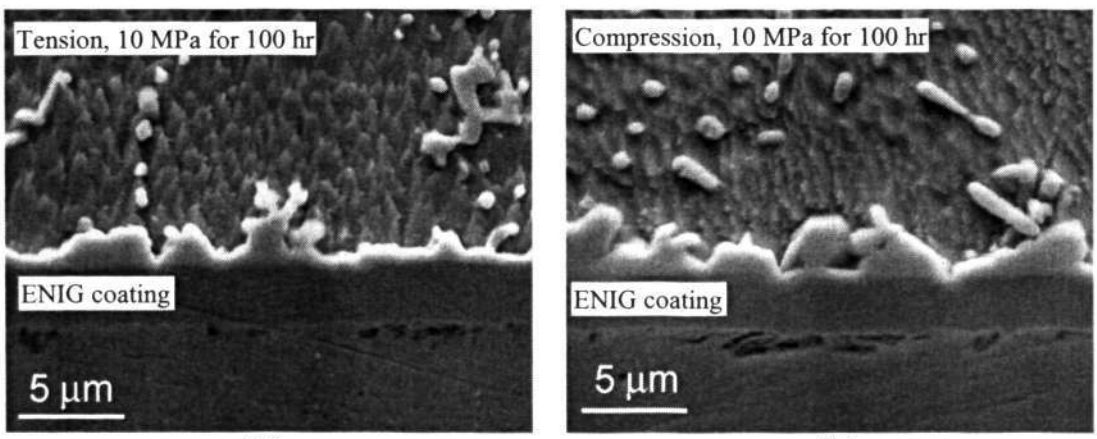
Figures 6.6 to 6.10 show the cross-sectional view of the interface IMCs in the C-rings annealed for different times. Figures 6.6 and 6.7 show no observable difference between the IMC layers that were subjected to tensile and compressive stresses after 100 and 168 hr annealing.

When the annealing time reaches 336 hr, difference in the IMC layer thickness between the compressive and tensile stresses conditions was noticed (Figure 6.8). From

Figures 6.9 and 6.10, the thickness deviation between the IMC layers under tensile and compressive stresses conditions was more prominent with longer exposure annealing times of 2000 and 4000 hr.

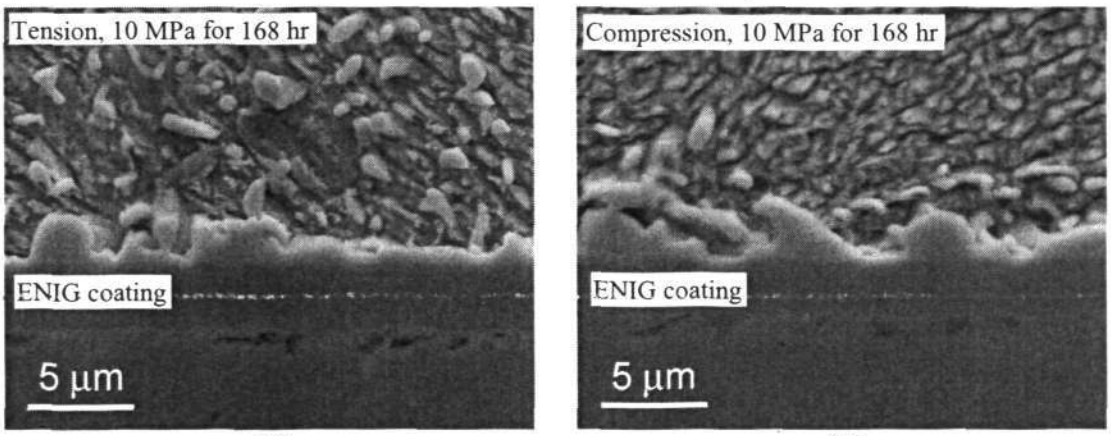
The average IMC layer thicknesses with respects to annealing time under both tensile and compressive stresses conditions are plotted in Figure 6.11. No significant growth of Cu-Ni-Sn IMC layer can be observed under tensile stress condition even with the increase of annealing time. From Figure 6.11, it can be seen that the standard deviations of the IMC layer thickness under tensile stress condition were smaller than the compressive stress condition. This was because tensile stress caused the formation of more planar IMC layer and lead to less deviation in IMC's thickness from one region to another.

In contrast, compressive stress at 10 MPa has resulted in the formation of thicker and more blocky Cu-Ni-Sn IMC layer. The compressive stressed IMC layer grew faster at the initial stage but leveled off with the increase of annealing time. The compressive stresses IMC that consists of blocky hexagonal-shape causes the thickness values to vary more significantly from one region to another.



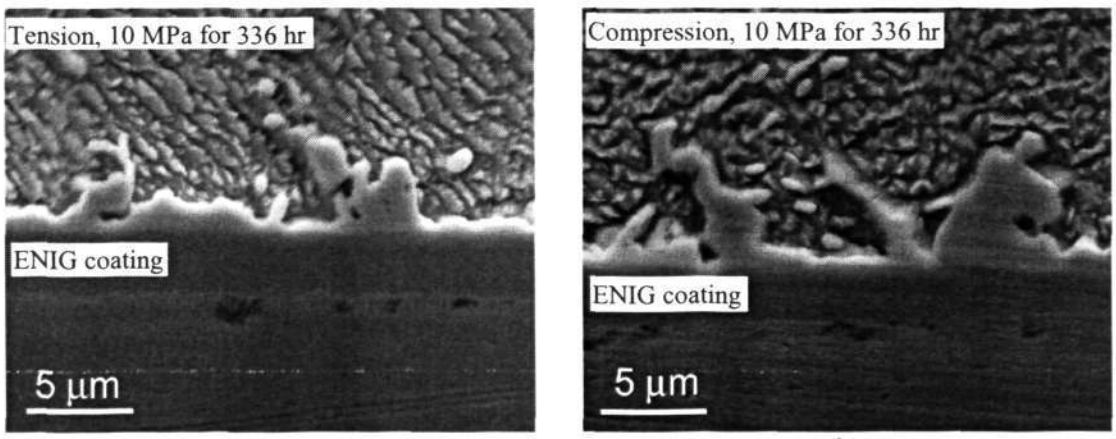
(a) (b)

Figure 6.6 SEM images at solder/ENIG coating interface with σ_s = 10 MPa annealed at 125 °C for 100 hr showing comparable IMC layer thickness under (a) in-plane tension and; (b) in-plane compression.



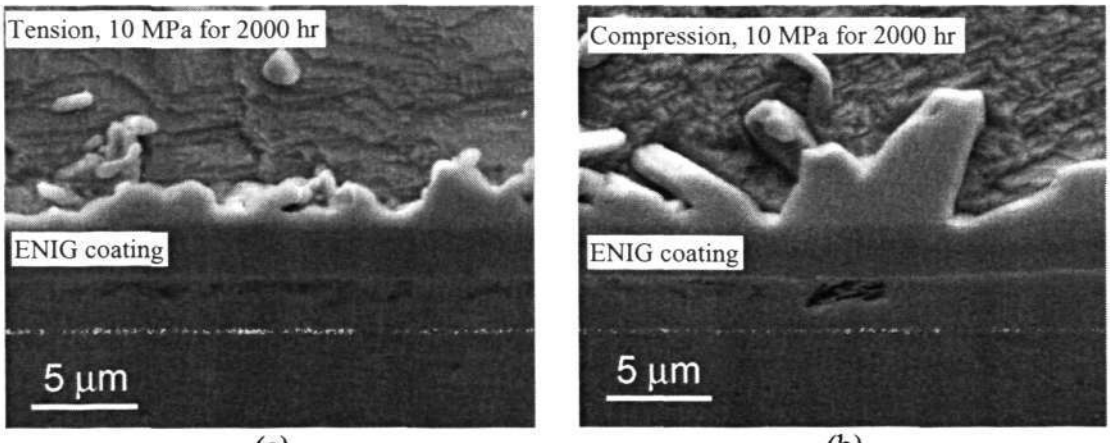
(a) (b)

Figure 6.7 SEM images at solder/ENIG coating interface with σ_s = 10 MPa annealed at 125 °C for 168 hr still showing comparable IMC layer thickness under (a) in-plane tension and; (b) in-plane compression.



(a) (b)

Figure 6.8 SEM images at solder/ENIG coating interface with σ_s = 10 MPa annealed at 125 °C for 336 hr showing IMC layer under (a) in-plane tension was slightly thinner than those; (b) under in-plane compression.



(a) (b)

Figure 6.9 SEM images at solder/ENIG coating interface with σ_s = 10 MPa annealed at 125 °C for 2000 hr showing the IMC layer under (a) in-plane tension and; (b) in-plane compression. The IMC layer under in-plane compression was thicker and more blocky in shape

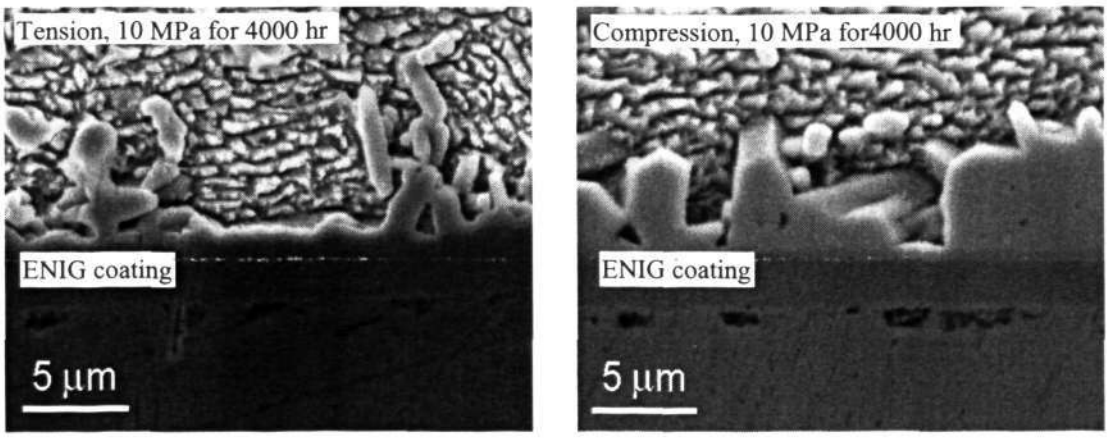


Figure 6.10 SEM images at solder/ENIG coating interface with σ_s = 10 MPa annealed at 125 °C for 4000 hr showing the IMC layer under (a) in-plane tension and; (b) in-plane compression. The IMC layer under in-plane compression was thicker and more blocky in shape.

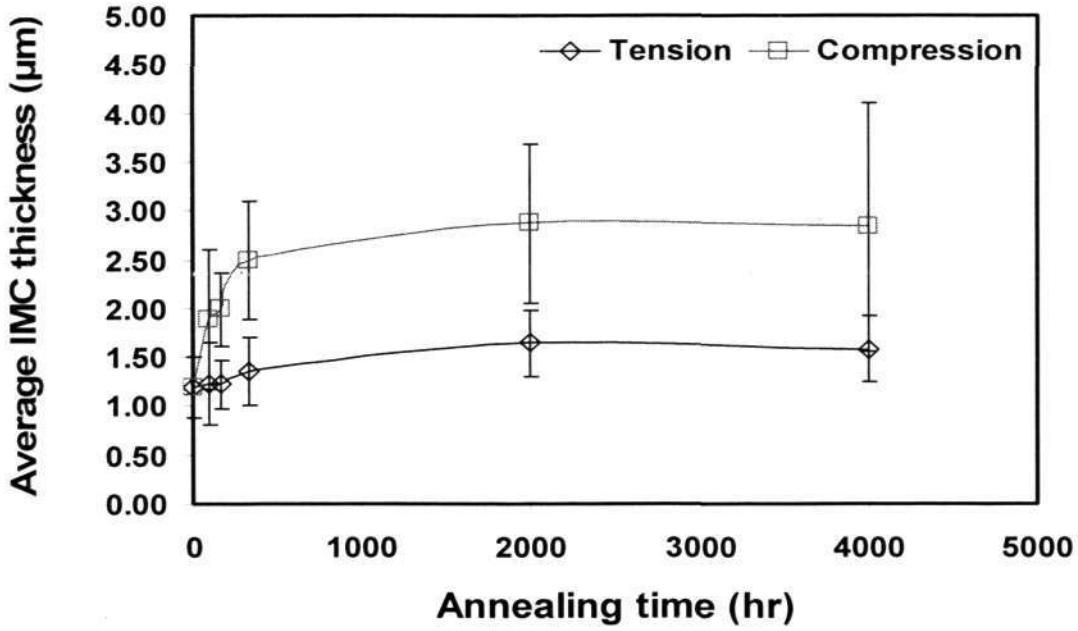


Figure 6.11 Average interface IMC layer thickness of the ENIG coated C-ring specimen under in-plane tensile and compressive stresses conditions with solder stress, σ_s about 10 MPa and annealed at 125 °C for various annealing time.

Figure 6.12 shows the planar view microstructures of the interface Cu-Ni-Sn IMC layer with σ_s = 10 MPa, annealed at 125 °C for 700 hr under both tensile and compressive stresses conditions. As compared to the as-reflowed condition in section 6.2.1 (Figure 6.3 (a)), islands of small needle-like IMCs still observable from the IMC layer under tensile stress condition (Figure 6.12 (a)). The close up view (Figure 6.12 (b)) shows that the islands of small needle-like IMCs were enclosed by circles of big and blocky IMCs. These circles of big and blocky IMCs were enclosed by continuous big planar IMCs.

In contrast, the islands of small needle-like IMCs were no longer found on the compressive stressed IMC layer (Figure 6.12 (c)). Only blocky hexagonal-shape of IMCs in various sizes were observed. Compressive stress resulted in the growth of both blocky hexagonal-shape and needle-like IMCs. The blocky hexagonal-shape IMC grew

slightly in size, while the needle-like IMCs grew and changed from needle-like to small hexagonal-shape.

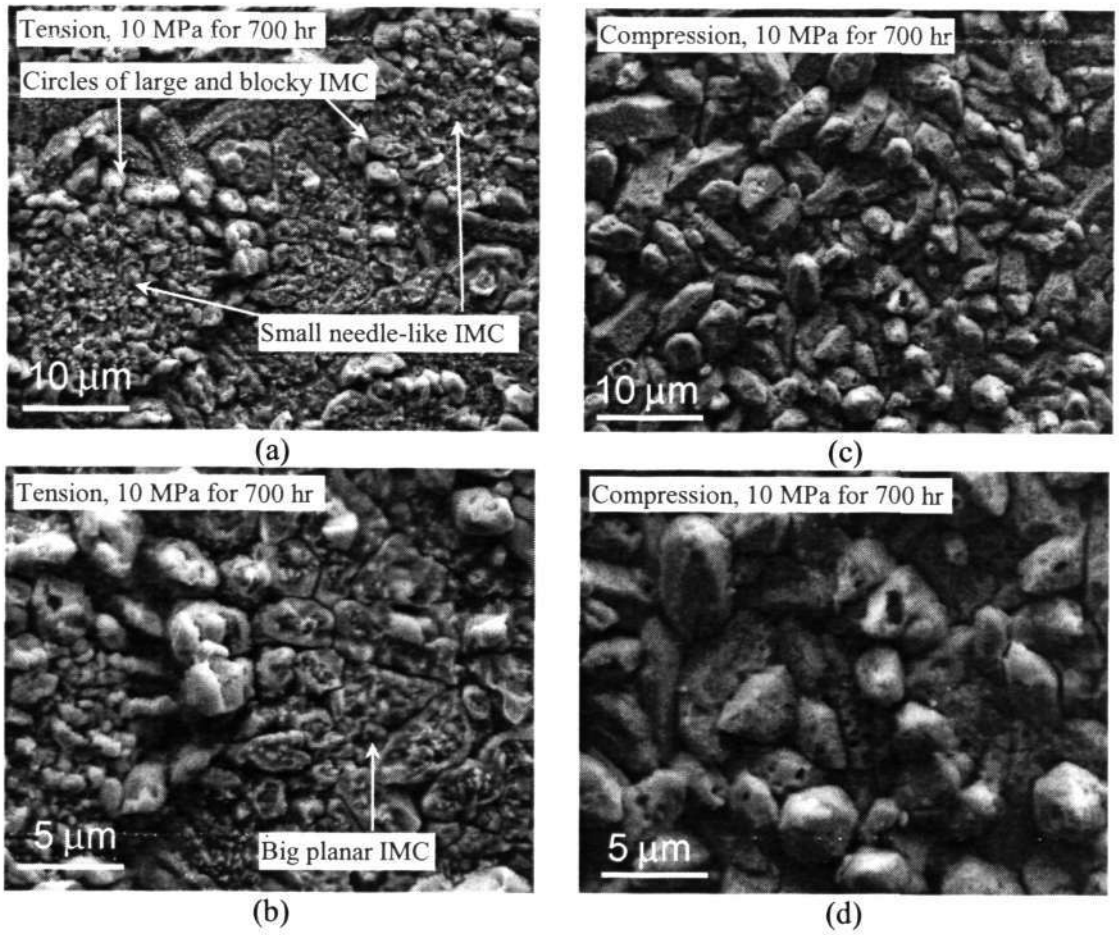


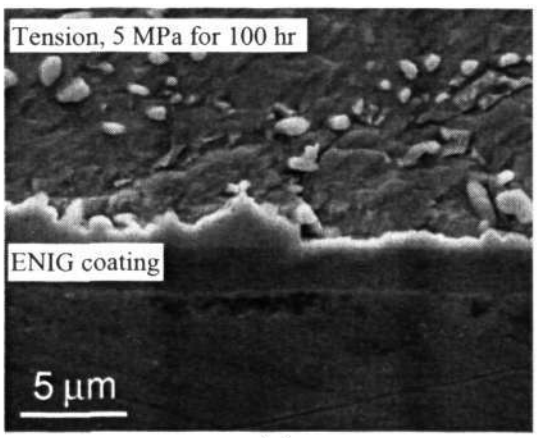
Figure 6.12 SEM (SEI) images of the ENIG coated C-ring solder joint with σ_s = 10 MPa annealed at 125 °C for 700 hr showing the (a) overall planar view of the interface IMC layer under in-plane tension. Island of small IMCs were surrounded by large planar IMC; (b) close up view for the center region of (a); (c)overall planar view of the IMC layer under in-plane compression showing present of blocky hexagonal-shape of IMCs in various sizes; (d) close up view for the center region of (c).

The results presented so far in the section are all for C-rings with stress level of 10 MPa in the solder. The results for C-rings with lower stress level of 5 MPa in the solder are presented below and compared with the results for the higher stress level.

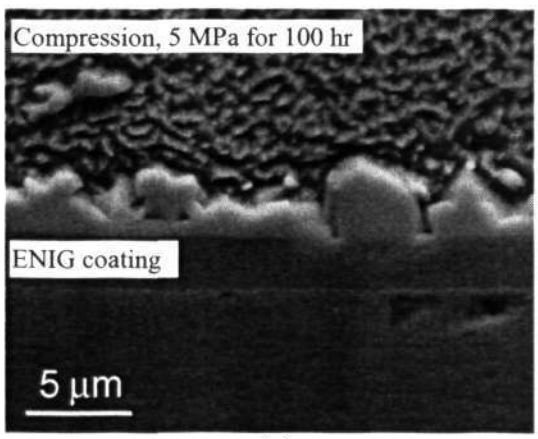
The C-rings stressed to 5 MPa were also annealed at a fixed temperature 125 °C for varying times (100, 336, 2000 and 4000 hr) to monitor change of the interface IMC thickness with time. Figure 6.13 show a series of cross-sectional view microstructures across the solder/ENIG coating interface. Even with lower applied stress level at 5 MPa, the compressive stressed IMC layer grew thicker with the increase of annealing time. However, the growth was less significant as compared to those under higher applied stress level at 10 MPa.

The tensile stressed IMC layer was observed to grow slightly thicker with the increase of annealing time under lower applied stress level. This was not noticeable with higher applied stress level at 10 MPa. As a whole, the tensile stressed IMC layers were still consistently thinner than those under compressive stress condition.

It was also found that the thickness deviation between the tensile and compressive stressed IMC layers was less prominent with lower applied stress level even after exposure to long annealing time of 2000 and 4000 hr. Lower tensile stress allows the IMC layer to grow slightly with the increase of annealing time. In contrast, the compressive stressed IMC layer grew in slower rate under lower stress level.



(a)



(e)

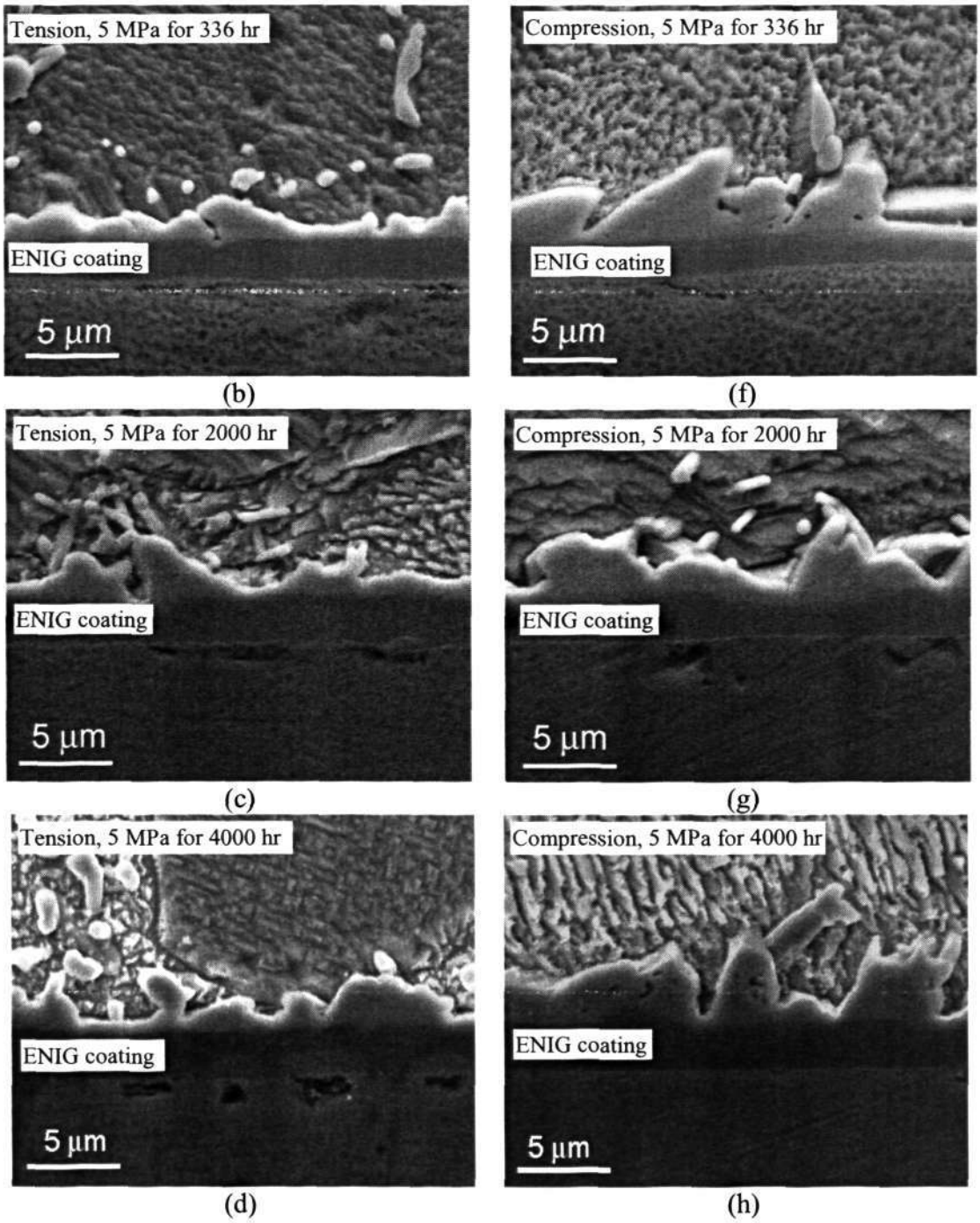
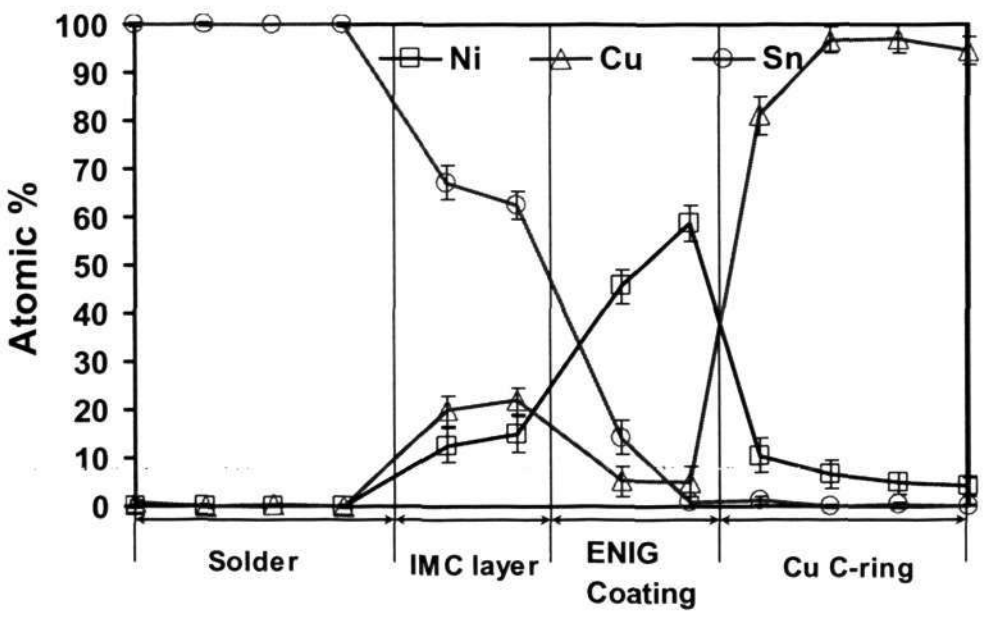
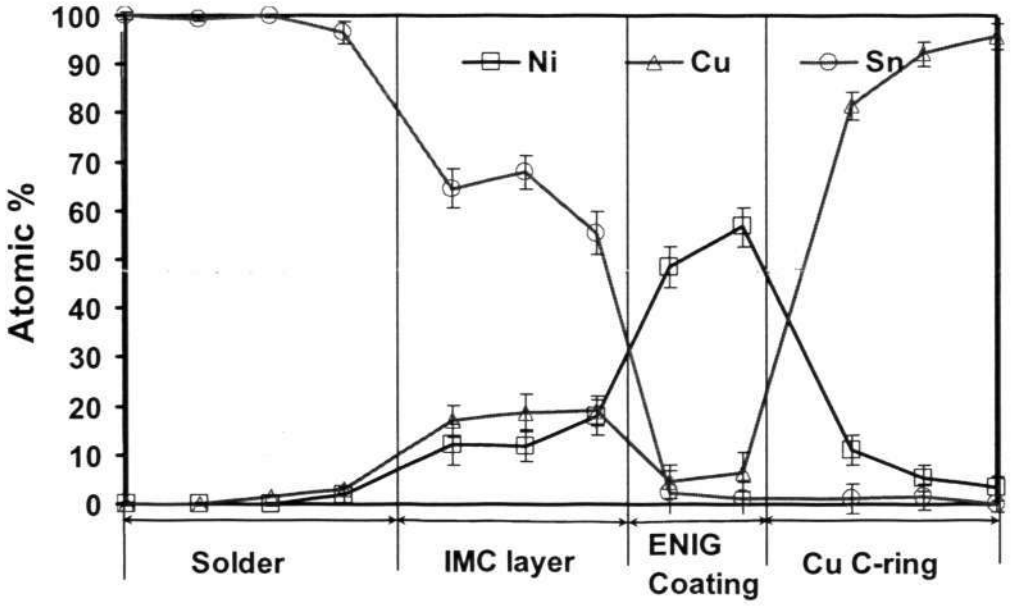


Figure 6.13 SEM images at solder/ENIG coating interface with σ_s = 5 MPa annealed at 125 °C for various annealing times. Consistently thinner tensile stressed IMC layer were observed after exposure to (a) 100 hr; (b) 336 hr; (c) 2000 hr and; (d) 4000 hr of annealing. Thinker and more blocky compressive stressed IMC layer were observed after exposure to (e) 100 hr; (f) 336 hr; (g) 2000 hr and; (h) 4000 hr of annealing.

EDX analysis was carried out to determine the distribution of Cu, Ni and Sn across the solder/coating interface of ENIG coated C-ring with solder stress, σ_s = 5 MPa and annealed at 125 °C for 336 hr under both tensile and compressive stress conditions. Figure 6.14 shows the distribution profiles of Cu, Ni and Sn across the solder/ENIG coating interface showing similar trends under both conditions. The distribution profiles for all the three elements are comparable to those obtained from the as-reflowed condition (Figure 6.5).



(a) region under tension



(b) region under compression

Figure 6.14 Plot of Cu, Ni and Sn concentration distribution profiles across the solder/coating interface of the ENIG coated C-ring with σ_s = 5 MPa annealed at 125 °C for 336 hr under (a) in-plane tension and (b) in-plane compression.

6.3 Interface IMC between Solder/ENEPIG Coated Cu Substrate

ENIG coating used in previous section has been used with great success on many components and boards as it has a flat surface and excellent solderability. However, the use of the ENIG coating has been found to break up during mechanical stress. This effect is known in industry as "black pad" or "mudflat cracking". "Black pad" phenomenon is where the solder leads lift away from a dark gray to black trademark on the underlying Ni surface. This drawback of ENIG coating has gained the momentum to work on several alternative lead-free surface finishes such as Ni/Pd immersion Au (ENEPIG) coating. ENEPIG was found to give a uniform and even IMC layer with Sn-Ag-Cu lead-free solder material. It also offers better adhesion and bonding integrity.

6.3.1 As-reflowed Microstructure

The cross-sectional view microstructure of the as-reflowed interface IMC layer of the ENEPIG coated C-ring is shown in Figure 6.15. The interface IMC layer showing both continuous planar IMC layer and discontinuous rod-like shape IMCs. ENEPIG coating produces thicker IMC layer (2.40±0.74 μm) than the ENIG coating (1.19±0.31 μm) under as-reflowed condition.

The planar view microstructure of the as-reflowed IMC layer clearly shows that the rod-like IMCs with various sizes distributed evenly in random orientation (Figure 6.16). This suggests that the morphologies of the IMC layer (continuous planar IMC layer and discontinuous rod-like IMC) in cross-sectional view were due to the sectioning of the rod-like IMCs in different orientations.

From the EDX analysis (Figure 6.17 (a)), the IMC layer at solder/ENEPIG coating interface was found to be the Sn-Pd IMC. A dark thin P-rich layer was found in the electroless Ni coating layer underneath the IMC layer from the SEM (BSE) image shown in Figure 6.17.

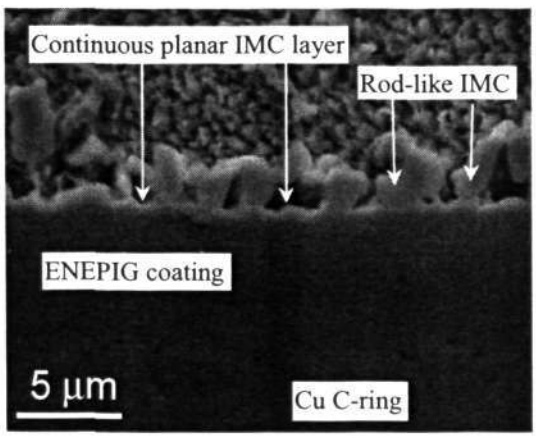
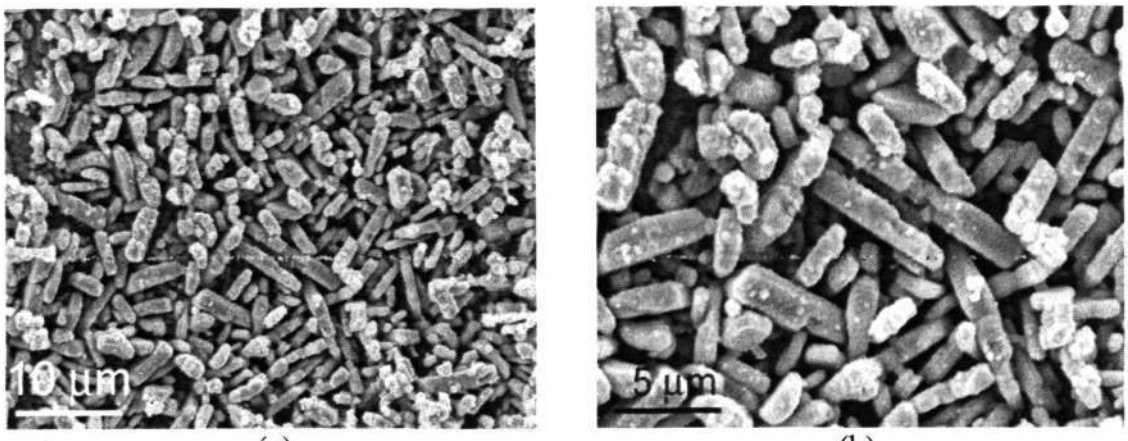


Figure 6.15 SEM (SEI) image of the as-reflowed ENEPIG coated C-ring in cross-sectional view showing continuous planar IMC layer and rod-like IMC at the solder/coating interface.



(a) (b)

Figure 6.16 SEM (SEI) images of the as-reflowed ENEPIG coated C-ring showing (a) the overall planar view of IMC layer consists rod-like IMCs in various sizes distributed evenly in random orientation; (b) close up view of the center region of (a)

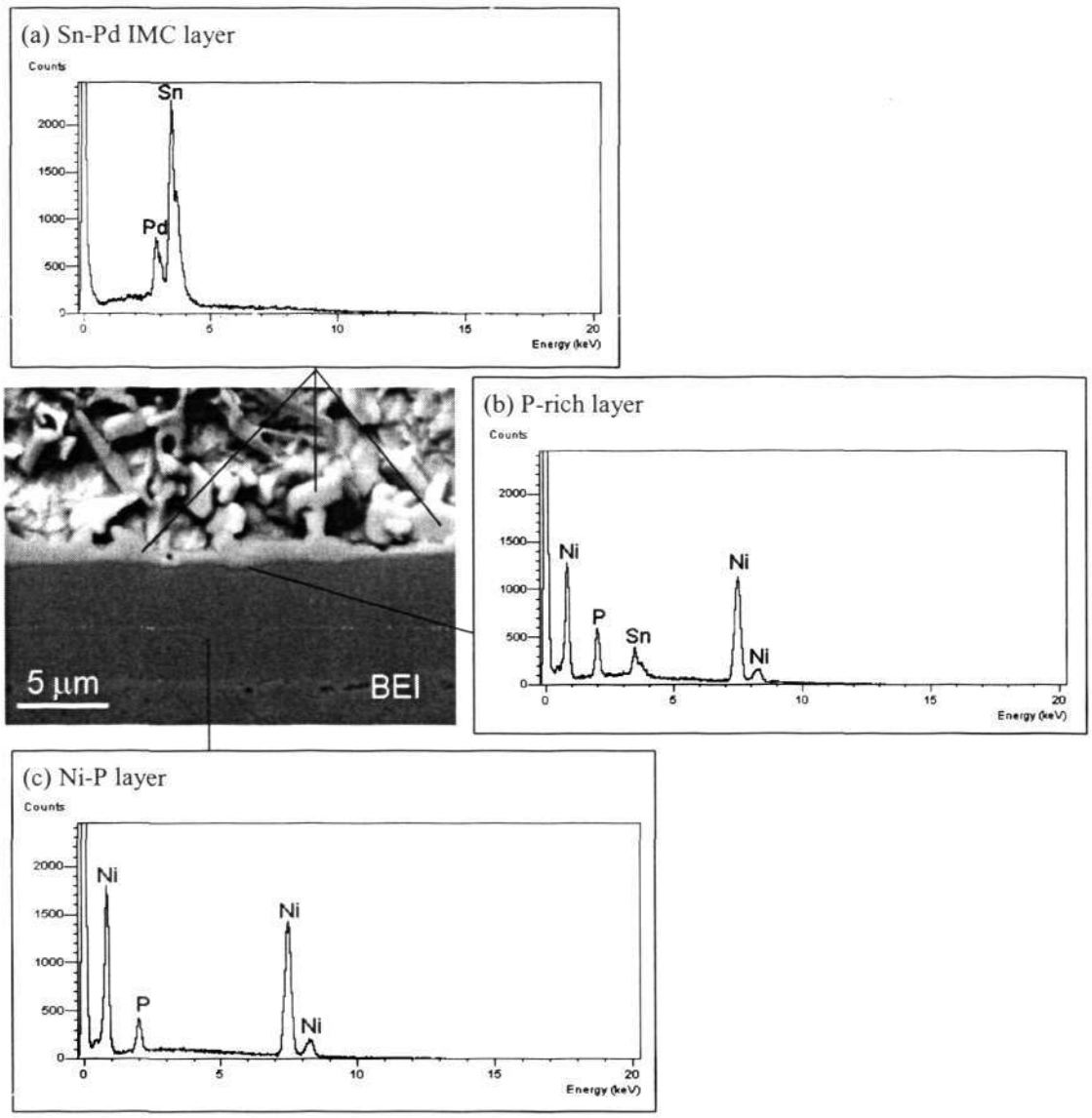


Figure 6.17 EDX spectrum for the (a) Sn-Pd IMC layer at solder/coating interface; (b) dark P–rich layer in electroless Ni layer underneath the IMC layer and; (c) Ni-P coating layer of the as-reflowed ENEPIG coated C-ring solder joint.

6.3.2 Effect of in-plane Tensile and Compressive Stresses on Interface IMC

The cross-sectional view microstructures across the solder/ENEPIG coating interface with solder stress, σ_s about 10 MPa and annealed at 125 °C for 336, 1007 and 4258 hr are shown in Figures 6.18 to 6.20.

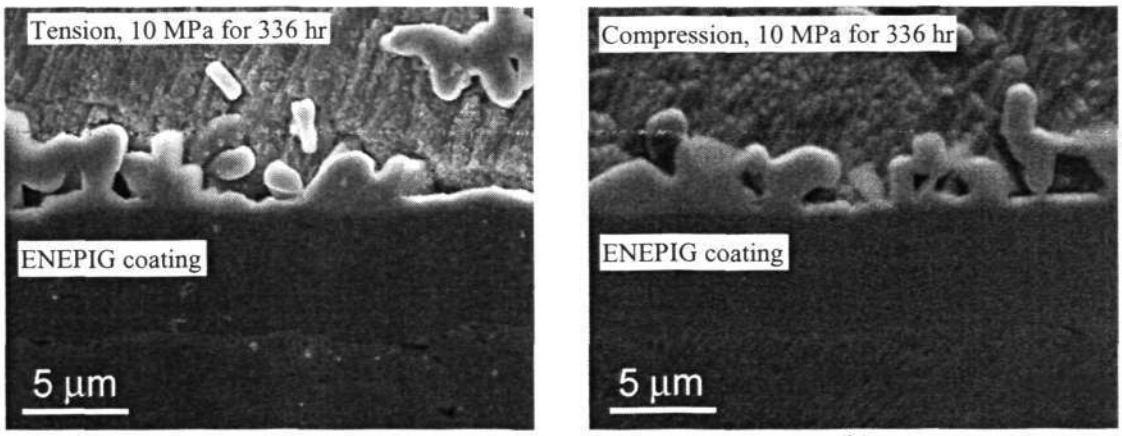
Exposure time of 336 hr has not result in any significant difference between the tensile and compressive stressed IMC layers (Figure 6.18). When annealing time reaches 1007 hr, thicker and more blocky IMC layer was found under compressive stress condition (Figure 6.19). An additional wavy IMC layer was found in between the Sn-Pd and ENEPIG coating under both tensile and compressive stresses conditions.

The EDX results show that the wavy IMC layer consists of Cu, Ni, Sn and Pd elements (Figure 6.21). This wavy Sn-Pd-Cu-Ni IMC layer appeared in darker grey tone in SEM (BSE) image shown in Figure 6.21.

After longer exposure time to 4258 hr, the tensile stressed IMC layer grew denser, but the compressive stress condition still showing thicker and denser IMC layer (Figure 6.20). Both Sn-Pb and Sn-Pd-Cu-Ni IMC layers were observable in both tensile and compressive stresses conditions. The Sn-Pd IMC layer was consistently thicker than the Sn-Pd-Cu-Ni IMC layer. The SEM (BSE) image shown in Figure 6.22 able to distinct Sn-Pb IMC (lighter grey) and Sn-Pd-Cu-Ni IMC (darker grey) layers better.

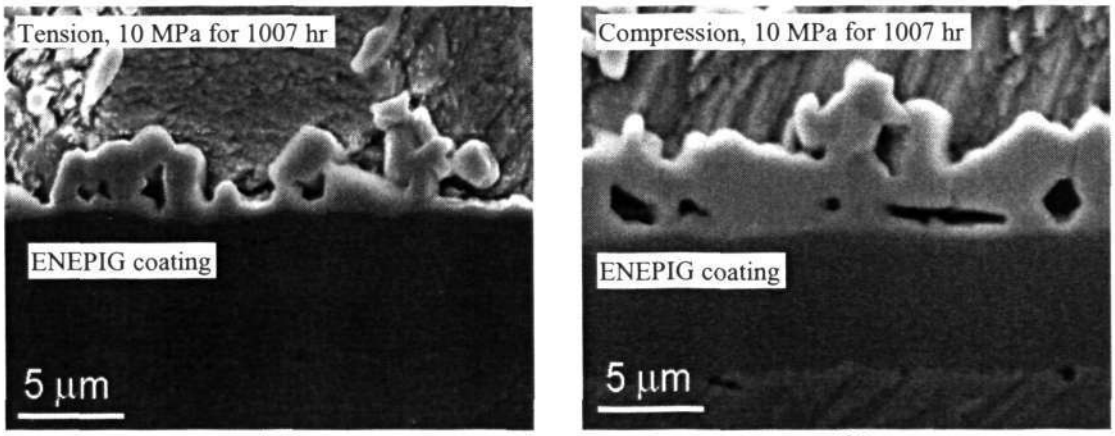
The average IMC layer thickness of ENEPIG coated C-ring solder joints under both tensile and compressive stresses conditions with solder stress, σ_s = 10 MPa and annealed at 125 °C for various exposure times are plotted and shown in Figure 6.23. Coincided with the results obtained from the study on ENIG coated C-ring, the growth of tensile stressed IMC layer was not significant but compressive stress has resulted in faster IMC growth rate. The compressive stressed IMC layer grew with the increase of annealing time, nevertheless the increase of annealing time from 1007 to 4258 hr has not show significant thickening of the IMC layer. However, the thickness range of the IMC layer under in-plane tensile stress condition was smaller as compared to the IMC layer under in-plane compressive stress condition when annealing time reaches 4025 hr.

After long exposure time to 4025 hr, morphology of IMC layer under in-plane tensile stress condition became less irregular due to ripening effect.



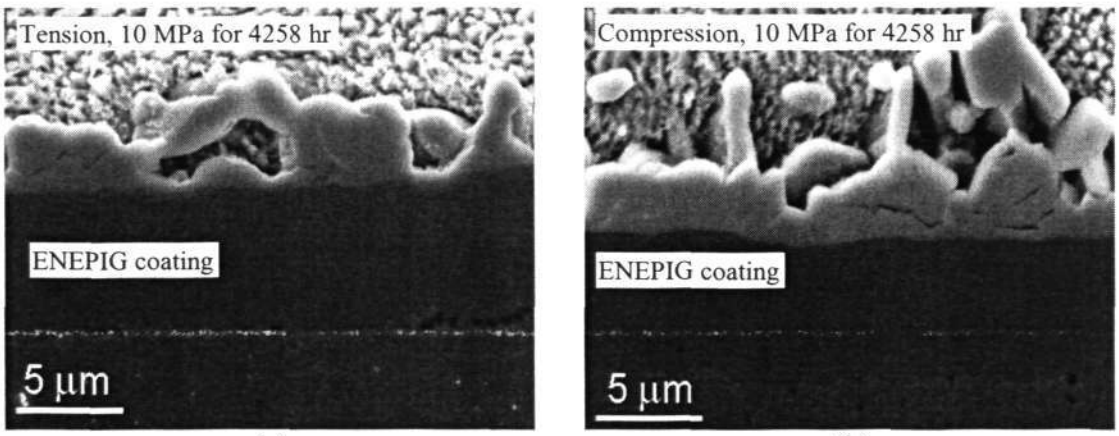
(a) (b)

Figure 6.18 SEM images at solder/ENEPIG coating interface with σ_s = 10 MPa annealed at 125 °C for 336 hr showing comparable IMC layer thickness under both (a) in-plane tension; (b) under in-plane compression.



(a) (b)

Figure 6.19 SEM images at solder/ENEPIG coating interface with σ_s = 10 MPa annealed at 125 °C for 1007 hr showing (a) IMC layer under in-plane tension with rod-like shape IMC layer; (b) under in-plane compression consists of thicker and denser IMC layer.



(a) (b)

Figure 6.20 SEM images at solder/ENEPIG coating interface with σ_s = 10 MPa annealed at 125 °C for 4258 hr showing (a) less dense IMC layer under in-plane tension; (b) denser IMC layer under in-plane compression.

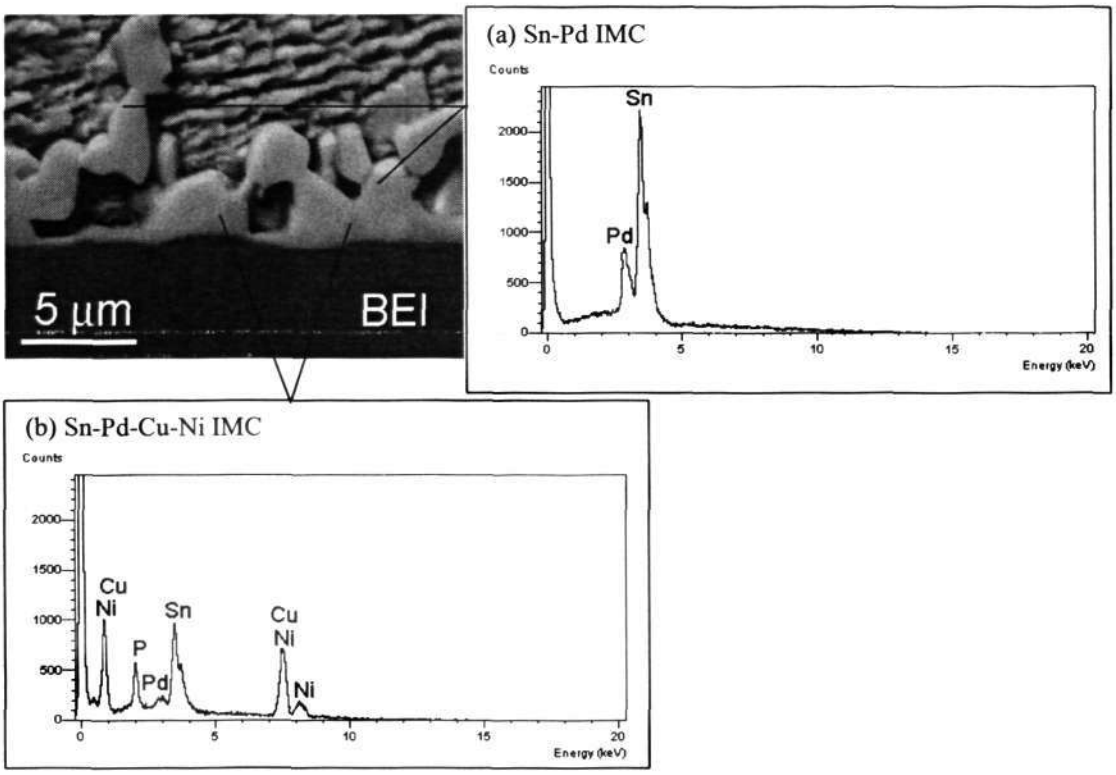


Figure 6.21 EDX spectrum for the (a) Sn-Pd IMC layer (ligter grey) and; (b) Sn-Pd-Cu-Ni IMC (darker grey) at solder/coating interface of the ENEPIG coated C-ring solder joint with σ_s = 10 MPa annealed at 125 °C for 1007 hr.

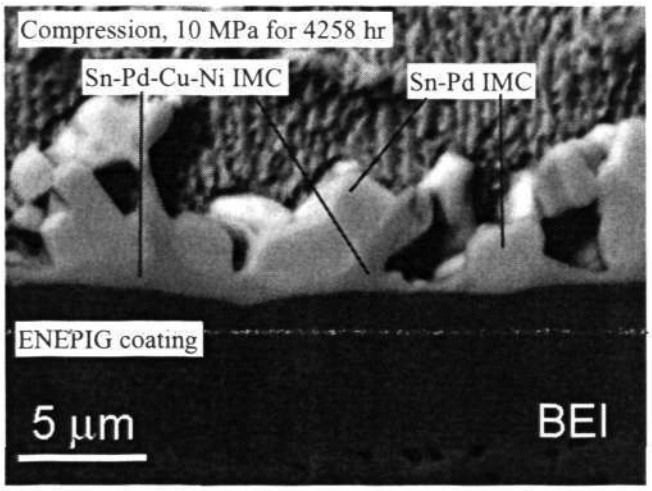


Figure 6.22 SEM (BSE) image of the ENEPIG coated C-ring with σ_s = 10 MPa annealed at 125 °C for 4258 hr able to show the Sn-Pd IMC (lighter grey) and Sn-Pd-Cu-Sn IMC (darker grey) layers more clearly.

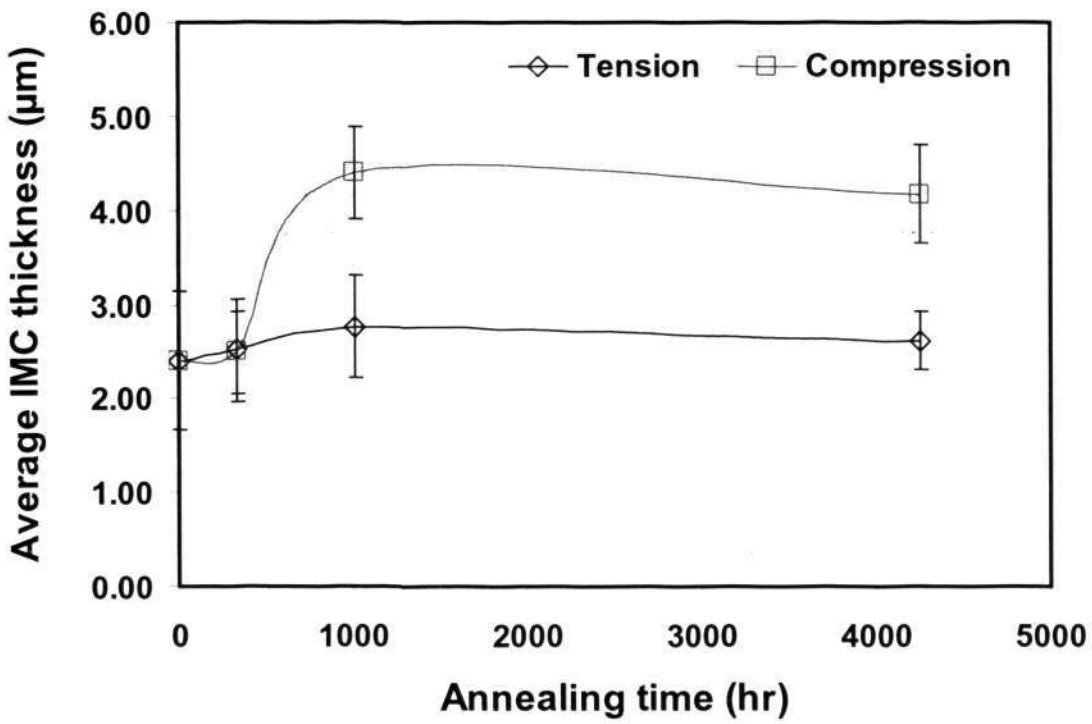
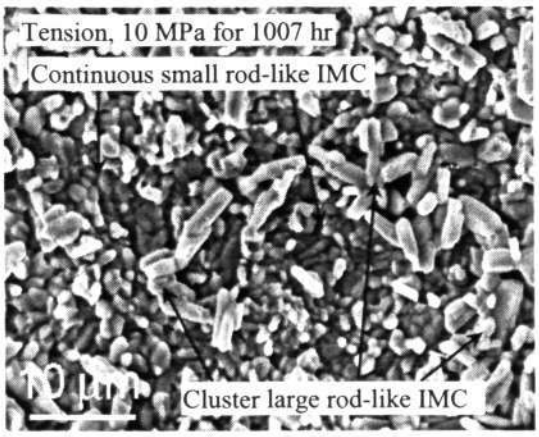


Figure 6.23 Average interface IMC layer thickness of the ENEIG coated C-ring specimen under in-plane tensile and compressive stresses conditions with solder stress, σ_s about 10 MPa and annealed at 125 °C for various annealing time.

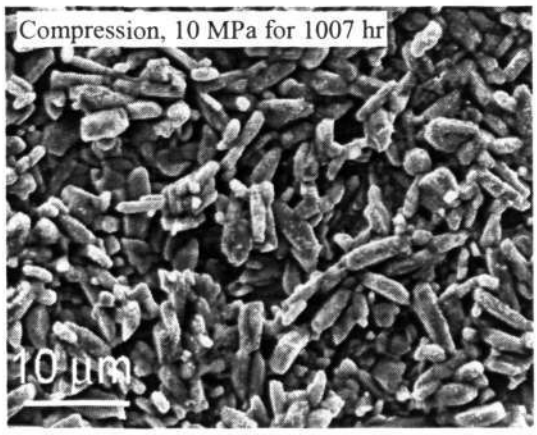
Figure 6.24 shows the planar view microstructures of the interface IMC layer with σ_s = 10 MPa, annealed at 125 °C for 1007 hr under both tensile and compressive stress conditions.

The tensile stressed IMC layer (Figure 6.24 (a) and (b)) shows clusters of large rod-like and small continuous rod-like IMCs appeared in different surface height. Clusters of large rod-like IMCs were found above the smaller continuous rod-like IMC layer. The overall surface height was less uniform as compared to the as-reflowed condition (Figure 6.16).

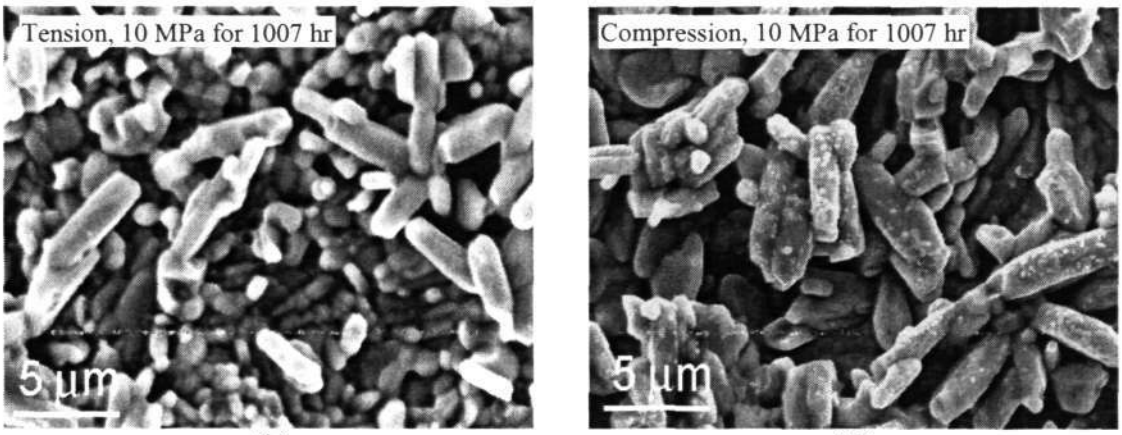
Under compressive stress condition, IMC layer (Figure 6.24 (c) and (d)) shows the rod-like IMCs grew in more congested manner and packed closer to each other. As compared to the tensile stressed IMC layer, the compressive stressed IMC consists of mostly large rod-like IMCs with more uniform surface height.



(a)



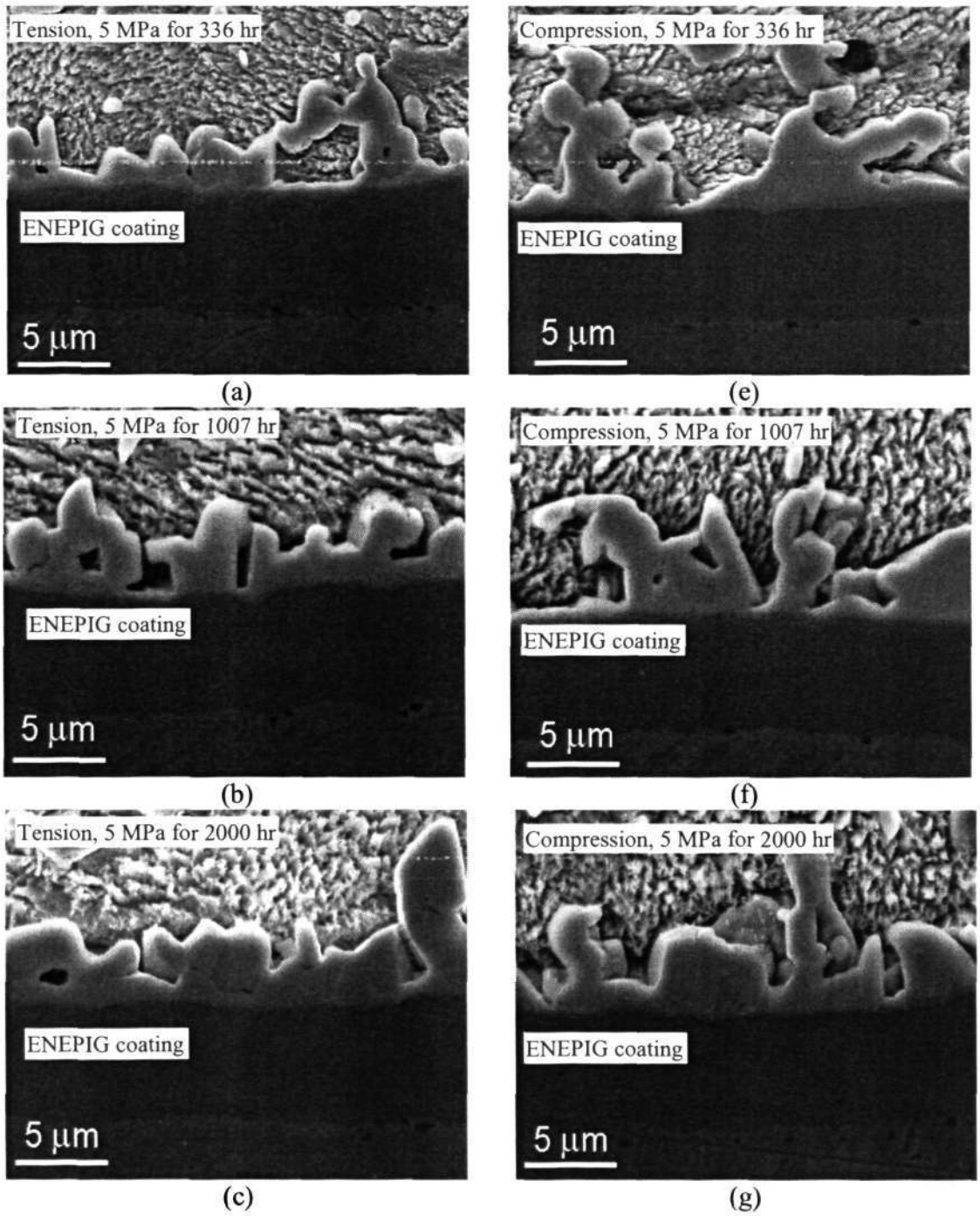
(c)

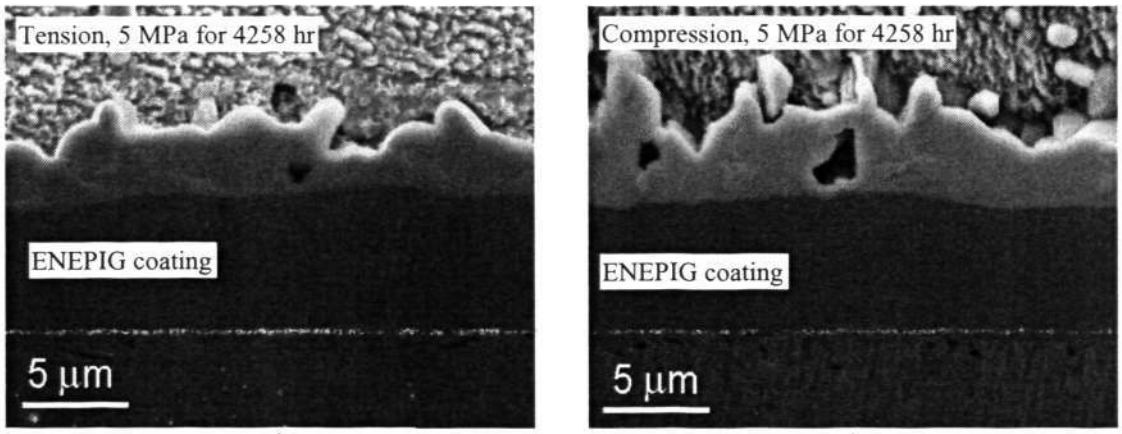


(b) (d)

Figure 6.24 SEM images (SEI) of the ENEPIG coated C-ring solder joint with σ_s = 10 MPa annealed at 125 °C for 1007 hr showing the (a) overall planar view of the interface IMC layer subjected to in-plane tension. Clusters of large rod-like IMCs were found above the smaller continuous rod-like IMC layer; (b) close up view for the center region of (a); (c)overall planar view of the IMC layer under in-plane compression showing evenly distributed and closely packed large rod-like IMCs; (d) close up view for the center region of (c).

Figure 6.25 shows a series of cross-sectional view microstructures across the solder/ENEPIG coating interface with lower applied stress level at σ_s = 5 MPa annealed at 125 °C for 336, 1007, 2000 and 4258 hr. At this lower stress level, no significant difference between the IMC layers under tensile and compressive stresses conditions can be observed. The IMC layers grew denser with the increase of annealing time under both conditions.





(d) (h)

Figure 6.25 SEM images at solder/ENEPIG coating interface with σ_s = 5 MPa and annealed at 125 °C for various annealing times. Comparable IMC layer thickness and morphology were observed under both in-plane tension and compression after exposure to (a) & (e) 336 hr; (b) & (f) 1007 hr; (c) & (g) 2000 hr, and; (d) & (h) 4258 hr of annealing. Under both stresses conditions, the IMC layer density increases with annealing time.

6.4 Interface IMC between Solder/Cu Substrate

Cu surface finish has been widely used in leaded electronic assemblies due to its excellent electrical and thermal conductivities. However, due to the replacement of lead-free solder, various plating finishes have to be applied to the Cu surface to improve the solderability and reliability of the joint. This is because most of the lead-free solder replacement candidates preferred by the electronic industry are basically Sn rich alloys and have relatively high melting temperature. These high Sn content solder alloys react much rapidly with Cu to form a thick layer of Cu-Sn IMC layer.

The bare Cu substrate was chosen as one of the surface finishes in this study because Cu reacts much rapid with the 95.8Sn-3.5Ag-0.7Cu lead-free solder. It was hoped that the effect of stress on interface IMC growth can be magnified by the much rapid reaction of the Cu-Sn IMC layer formation in the bare Cu C-ring system.

6.4.1 As-reflowed Microstructure

The cross-sectional view microstructure of the as-reflowed bare Cu C-ring solder joint is shown in Figure 6.26. The specimen consists of typical scallop-like interface Cu_6Sn_5 IMC layer. Figure 6.27 shows the microstructures of the IMC layer in planar view and regular size of scallop-like IMCs can be seen clearly.

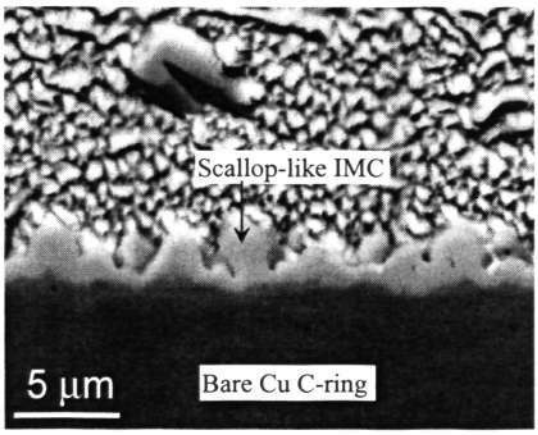
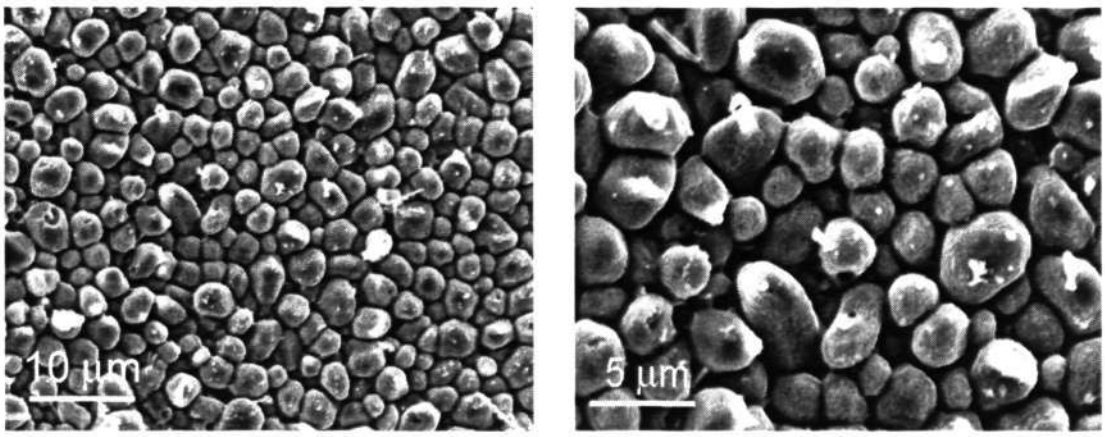


Figure 6.26 SEM (BSE) image of the as-reflowed bare Cu C-ring under cross-sectional view showing typical scallop-like interface Cu_6Sn_5 IMC layer



(a) (b)

Figure 6.27 SEM (SEI) images of the as-reflowed bare Cu C-ring showing (a) the overall planar view microstructure of scallop-like Cu_6Sn_5 IMC; (b) close up view of the center region of (a)

6.4.2 Effect of in-plane Tensile and Compressive Stresses on Interface IMC

The cross-sectional view microstructures across the solder/Cu interface with solder stress, σ_s = 10 MPa and annealed at 125 °C for 100, 168, 336, 1000 and 2025 hr are shown in Figures 6.28 to 6.32. No significant difference between the tensile and compressive stressed Cu-Sn IMC layers can be observed after subjected to first 100 hr of annealing (Figure 6.28).

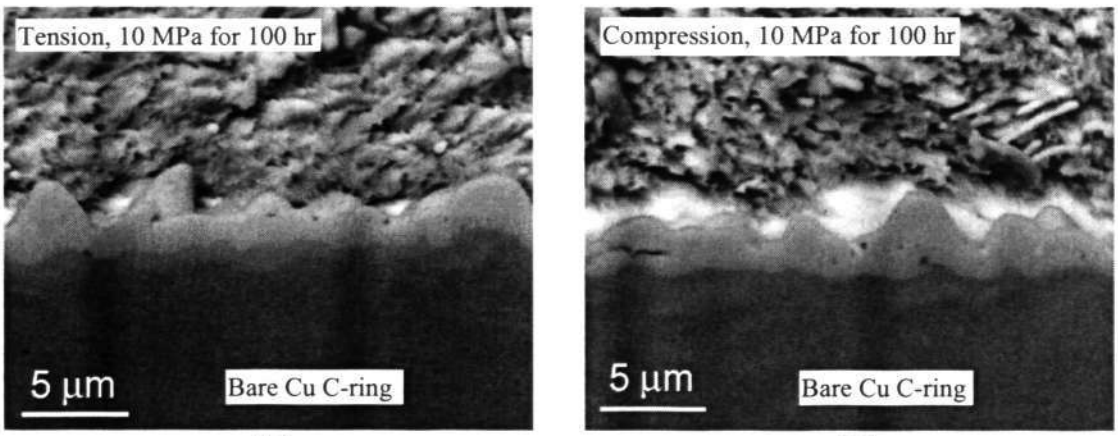
When the annealing time reaches 168 hr and longer (336, 1000 and 2025 hr), additional Cu_3Sn IMC layer can be observed in between the Cu_6Sn_5 IMC layer and Cu substrate under both tensile and compressive stress conditions. The Cu_3Sn IMC layer appeared in darker gray tone as compared to Cu_6Sn_5 IMC in SEM (BSE) images.

Thicker and relatively blocky Cu-Sn IMC layer was found under compressive stress condition. Under tensile stress condition, the IMC layer grew slightly in thickness and became more planar with the increase of annealing time.

The average IMC layer thickness values under both tensile and compressive stresses conditions are plotted and shown in Figure 6.23. As compared to the previous two Ni-based coating surfaces (ENIG and ENEPIG), the Cu-Sn IMC layer for the bare Cu C-ring continued to grow with the increase of annealing time. However, the growth rate slowed down with the increase of annealing time. This phenomenon can be attributed to the formation of Cu_3Sn IMC layer.

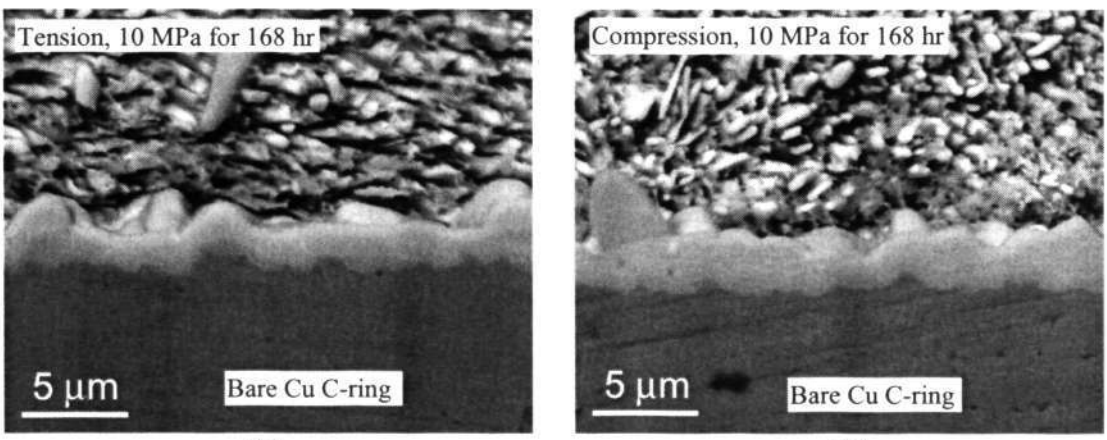
As reported by Bader et al. (Bader et al., 1995), part of the Cu_6Sn_5 IMC was consumed during the process of Cu_3Sn formation, thus the growth of Cu_6Sn_5 was partially masked by the Cu_3Sn formation. Furthermore, the growth of Cu_6Sn_5 has slowed down due to decreasing supply of both the interfacial and ripening Cu fluxes. At the initial condition, there are small channels extending all the way to Cu_3Sn/Cu

interface. Since the Cu_3Sn layer is so thin, these channels serve as fast diffusion paths for the Cu and Sn from the Cu substrate and solder to feed the interface reaction. However, with the increase of annealing time, the number and the opening area of the channels reduced. These caused the decrease in Cu atom supply and slow down IMC growth.



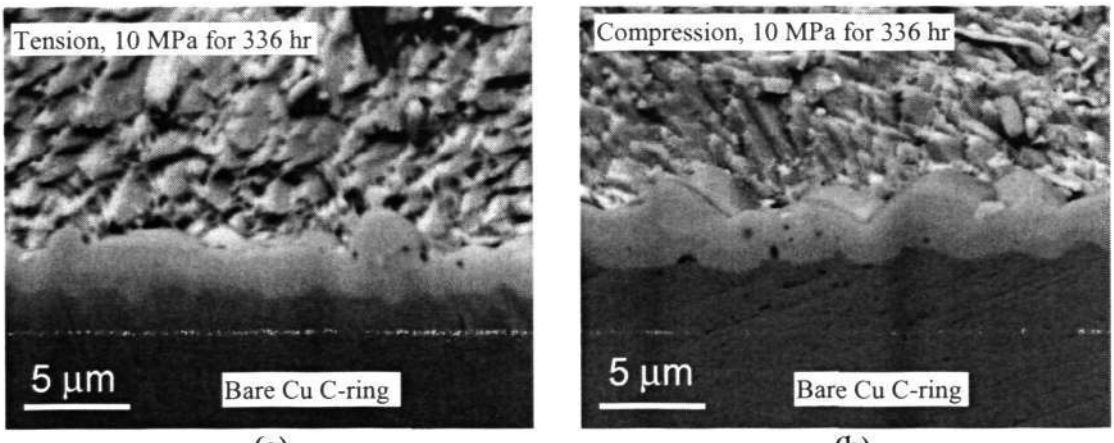
(a) (b)

Figure 6.28 SEM (BSE) images across the solder/Cu interface of the bare Cu C-ring with σ_s = 10 MPa and annealed at 125 °C for 100 hr showing comparable IMC layer (a) under in-plane tension and; (b) in-plane compression.



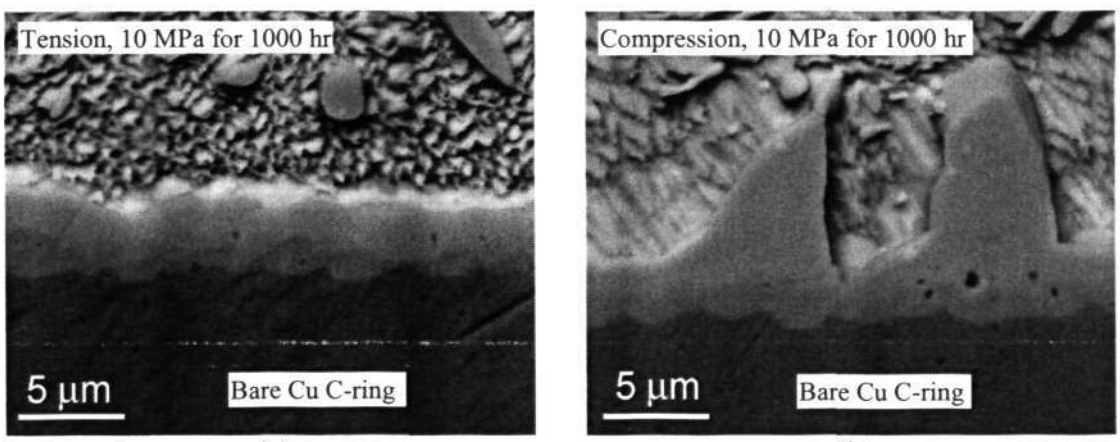
(a) (b)

Figure 6.29 SEM (BSE) images across the solder/Cu interface of the bare Cu C-ring with σ_s = 10 MPa and annealed at 125 °C for 168 hr showing (a) slightly thinner IMC layer under in-plane tension and; (b) thicker IMC under in-plane compression.



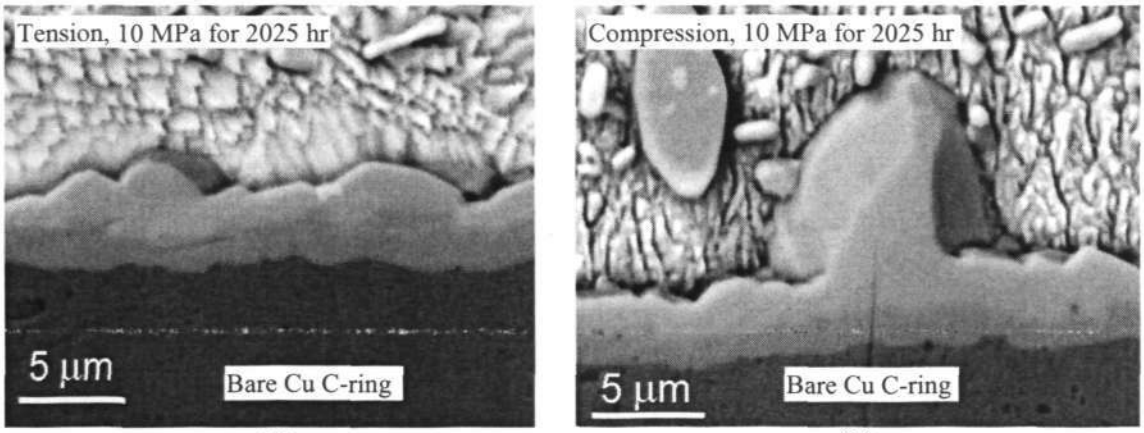
(a) (b)

Figure 6.30 SEM (BSE) images across the solder/Cu interface of the bare Cu C-ring with σ_s = 10 MPa and annealed at 125 °C for 336 hr showing (a) slightly thinner IMC layer under in-plane tension and; (b) thicker IMC under in-plane compression.



(a) (b)

Figure 6.31 SEM (BSE) images of interface IMC layer between the solder and bare Cu substrate with σ_s = 10 MPa for 1000 hr showing (a) thinner and more planar IMC layer under in-plane tension and; (b) more blocky IMC layer under in-plane compression.



(a) (b)

Figure 6.32 SEM (BSE) images across the solder/Cu interface of the bare Cu C-ring with σ_s = 10 MPa and annealed at 125 °C for 2025 hr showing (a) thinner and more planar IMC layer under in-plane tension and; (b) thicker and more blocky IMC layer under in-plane compression.

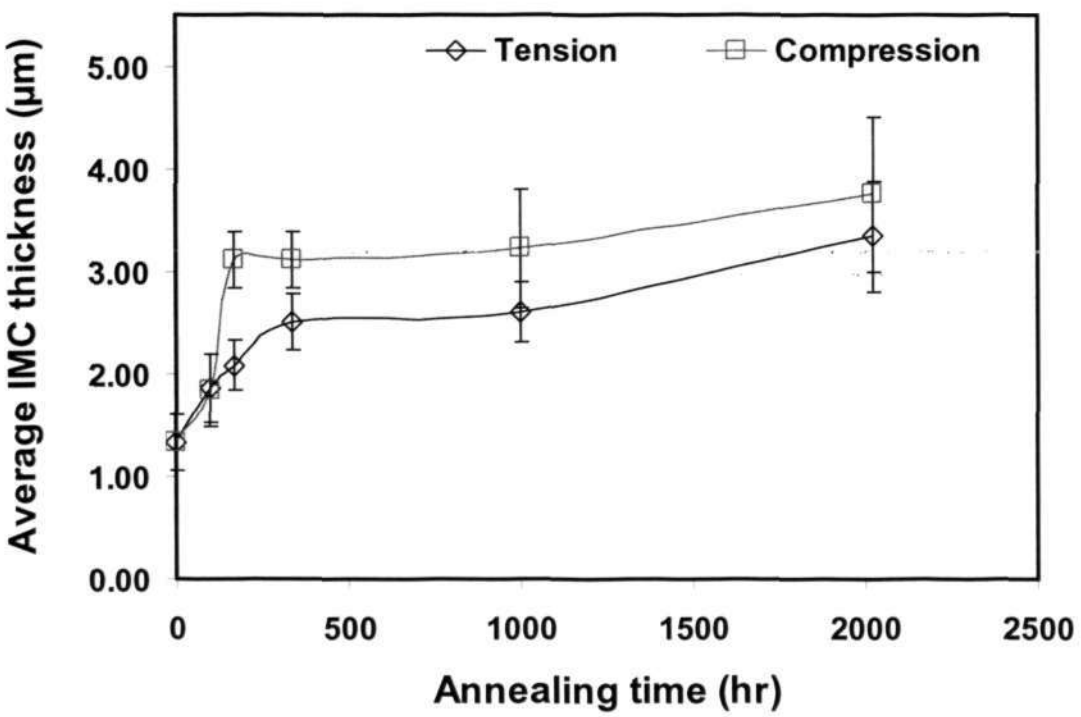
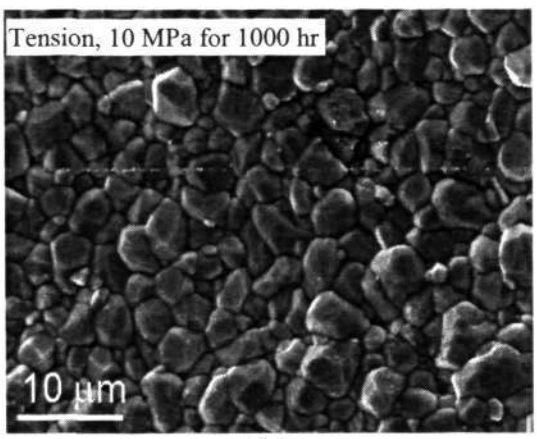


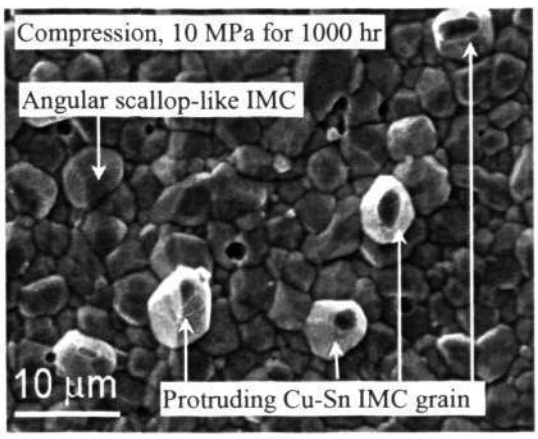
Figure 6.33 Average interface IMC layer thickness of the bare Cu C-ring specimen under in-plane tensile and compressive stresses conditions with solder stress, σ_s = 10 MPa and annealed at 125 °C for various annealing time.

Figure 6.34 shows the planar view microstructures of the interface Cu-Sn IMC layer with σ_s = 10 MPa and annealed at 125 °C for 1000 hr under both tensile and compressive stresses conditions. Scallop-like Cu-Sn IMC still observable under tensile stress condition but the individual IMC grain appeared to be more angular in shape (not as round as the as-reflowed condition). The angular scallop-like IMC was bigger in size and were more closely packed to each other (Figure 6.34 (a) and (b)).

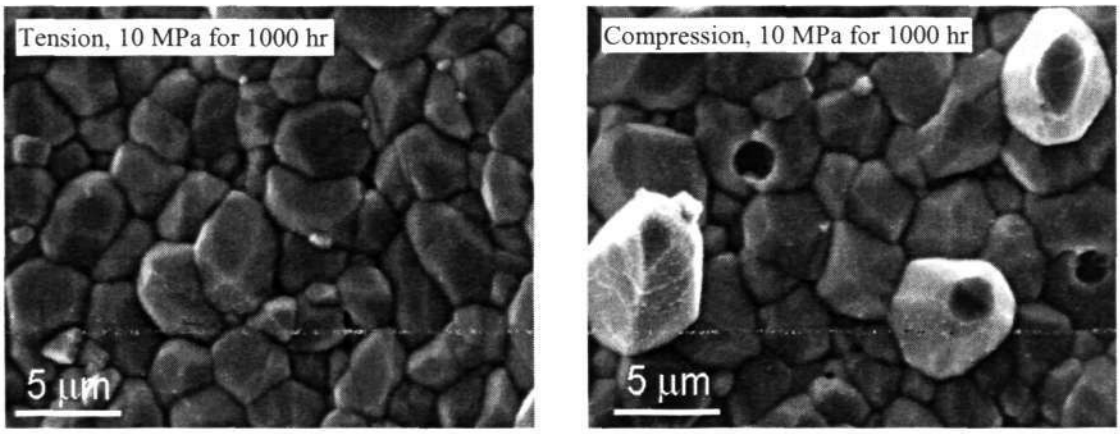
Angular scallop-like Cu-Sn IMC was also observed under the compressive stress condition. However, additional stand alone Cu-Sn IMC gains were found protruding from the IMC layer as indicated in Figure 6.34 (c) and (d).



(a)



(c)



(b) (d)

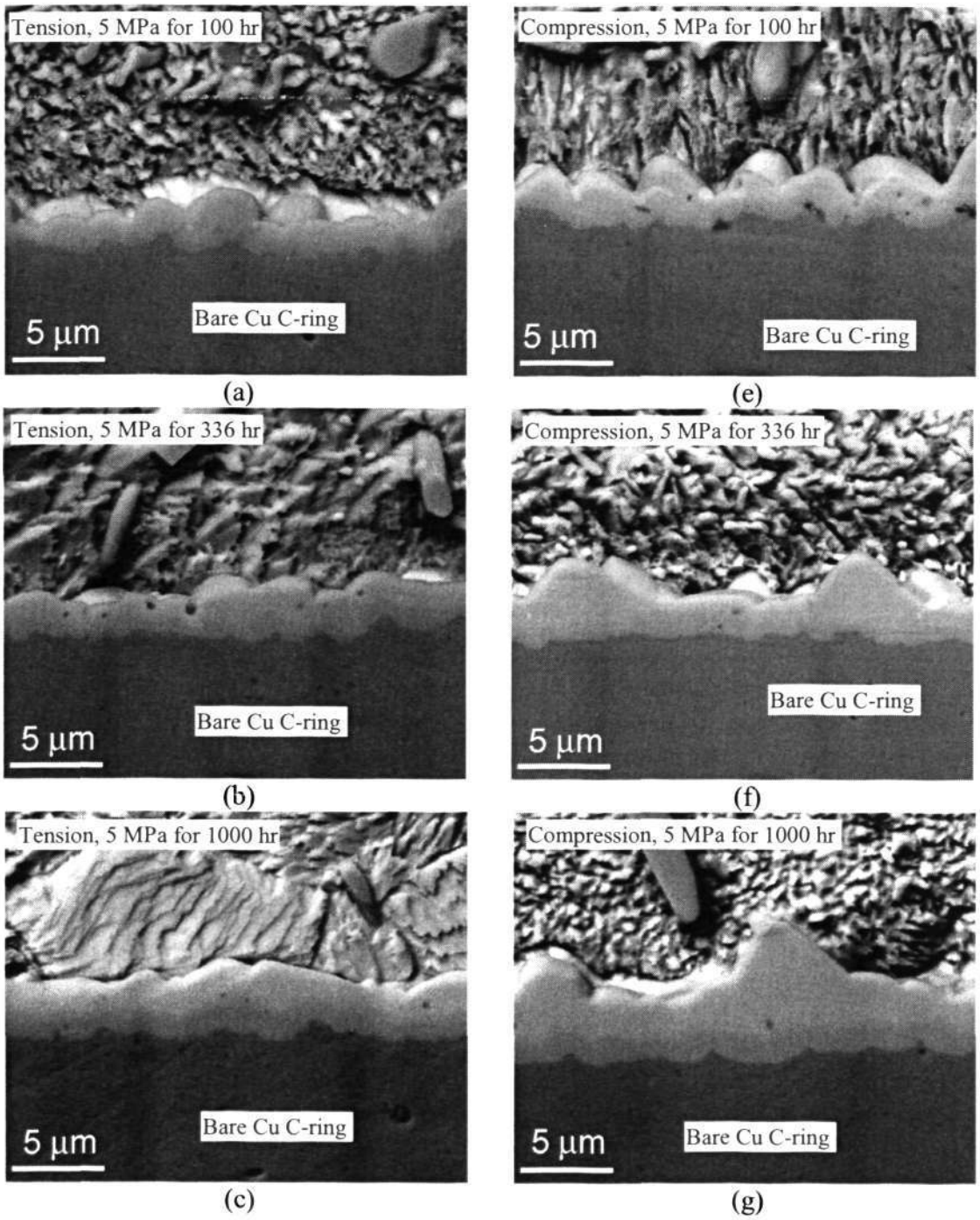
Figure 6.34 SEM images (SEI) of the bare Cu C-ring solder joint with σ_s = 10 MPa annealed at 125 °C for 1000 hr showing the (a) overall planar view of the interface Cu-Sn IMC layer subjected to in-plane tensile stress consist of larger and more angular scallop-like Cu-Sn IMCs; (b) close up view for the center region of (a); (c) the overall planar view of the IMC layer under in-plane compression stress showing the similar angular scallop-like IMC but with additional stand alone Cu-Sn IMC grains protruding from the IMC layer; (d) close up view for the center region of (c).

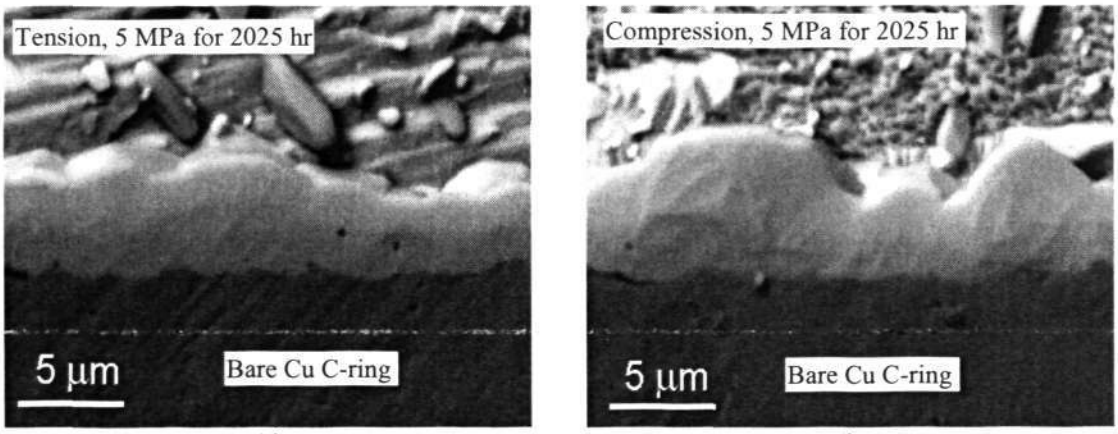
Figure 6.35 shows a series of the cross-sectional view microstructures across the solder/Cu interface with lower applied stress level at σ_s = 5 MPa and annealed at 125 °C for 100, 336, 1000 and 2025 hr. The compressive stressed IMC layer grew with the increase of annealing time. However, the growth was less significant as compared to those with higher applied stress level at 10 MPa.

The tensile stressed IMC layer also grew with the increase of annealing time but they were consistently thinner than those under compressive stress condition. In addition, the thickness deviation between the tensile and compressive stressed IMC layers was less prominent at lower applied stress level.

The lower thickness deviation between the tensile and compressive stressed IMC layers was due the change of their growth rate under lower stress level at 5 MPa.

Lower tensile stress allows the IMC layer to grow slightly faster with the increase of annealing time. While lower compressive stress has resulted in slower IMC growth.





(d) (h)

Figure 6.35 SEM images at solder/Cu interface with σ_s = 5 MPa annealed at 125 °C for various annealing times. Consistently thinner in-plane tensile stressed IMC layer were observed after exposure to (a) 100 hr; (b) 336 hr; (c) 1000 hr; and (d) 2025 hr of annealing. Thinker and more blocky in-plane compressive stressed IMC layer were observed after exposure to (e) 100 hr; (f) 336 hr; (g) 1000 hr; and (h) 2025 hr of annealing.

6.5 Interface IMC between Solder/Immersion Sn Coated Cu Substrate

Pure Sn is another potential candidate for lead-free surface finish. Sn can be electroplated, immersion coated or applied as a molten metal. The latest case is not common because of the extreme process temperature. Electroplated Sn coating has been introduced in connector industry for a long period of time as this coating is generally soft, ductile and have relatively low melting point. Unfortunately, the electroplated Sn surface finish is prone to Sn whisker formation.

Immersion Sn coating has a better acceptance as a lead-free surface finish, because it can mitigate Sn whisker growth. The immersion Sn also shares some other advantages such as providing a planar surface and a processing temperature that is not damaging to the circuit.

6.5.1 As-reflowed Microstructure

The cross-sectional and planar views microstructures of the as-reflowed immersion Sn coated C-ring solder joint are shown in Figures 6.36 and 6.37 respectively. Typical scallop-like interface Cu_6Sn_5 IMC as those observed from bare Cu substrate (section 6.4.1, Figures 6.26 and 6.27) was also formed at interface between solder and the immersion Sn coating.

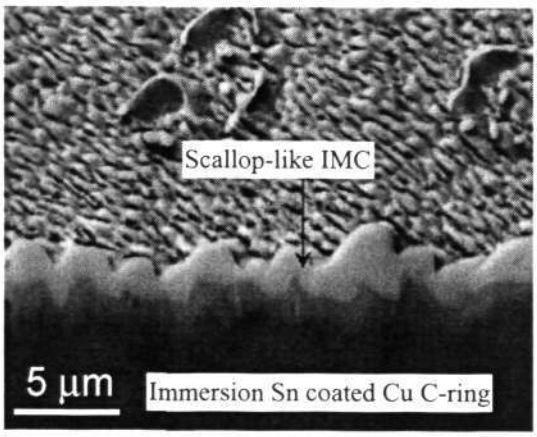
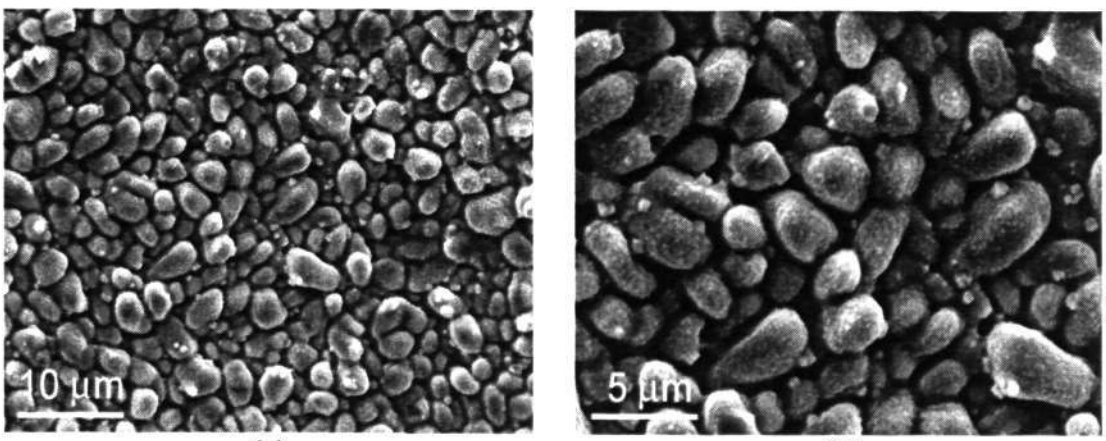


Figure 6.36 SEM (BSE) image showing the cross-sectional view microstructure of the as-reflowed immersion Sn coated C-ring solder joint consists of typical scallop-like Cu_6Sn_5 IMC layer across the solder/coating interface.



(a) (b)

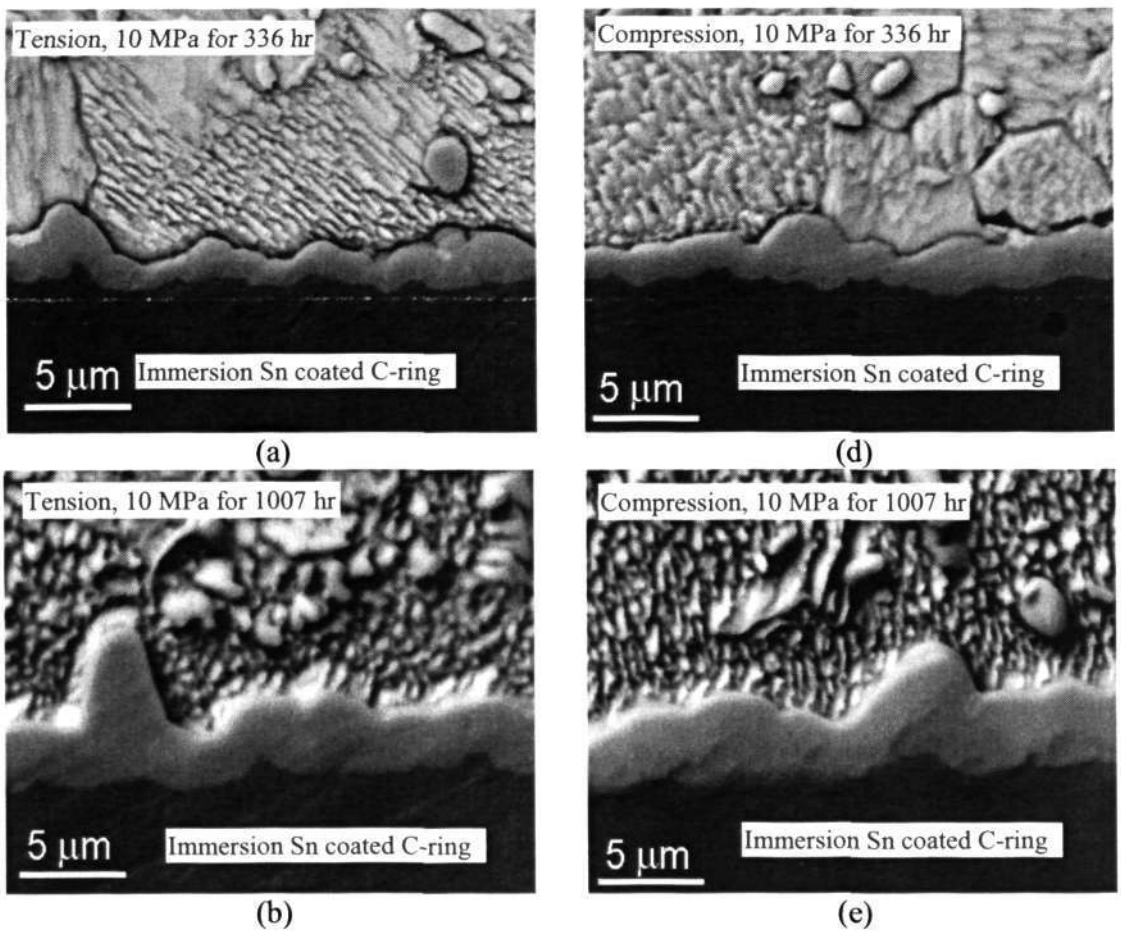
Figure 6.37 SEM (SEI) images of the as-reflowed immersion Sn coated C-ring solder joint showing (a) the overall planar view microstructure of the typical scallop-like Cu_6Sn_5 IMC; (b) close up view of the center region of (a)

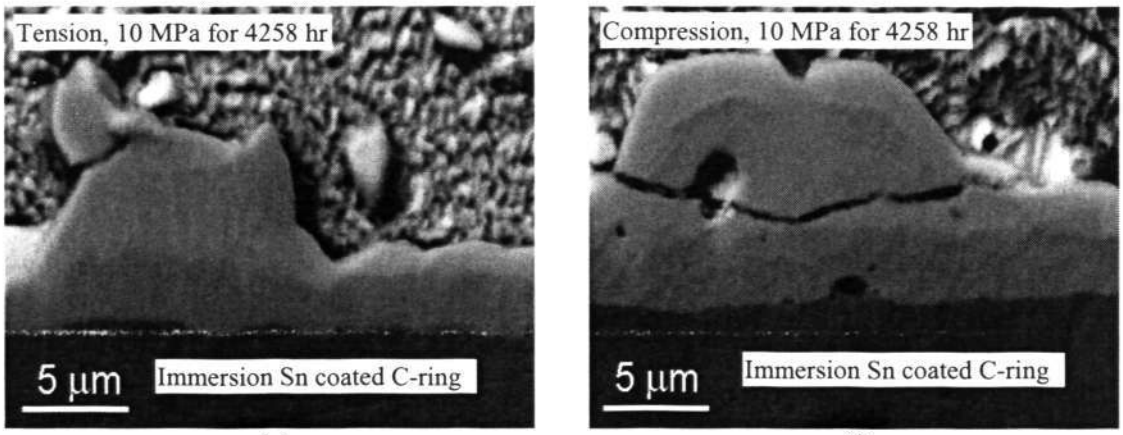
6.5.2 Effect of in-plane Tensile and Compressive Stresses on Interface IMC

Figure 6.38 shows a series of cross-sectional view microstructures across the solder/immersion Sn coating interface with solder stress, σ_s = 10 MPa and annealed at 125 °C for 336, 1007 and 4258 hr. Surprisingly, no significant difference in Cu-Sn IMC layer between the tensile and compressive stresses conditions can be observed even when the annealing time reaches 4258 hr (Figure 6.38 (d) and (h)).

The additive in the immersion Sn coating to prevent the Sn whisker growth might have neutralized the effect of compressive stress at the interface.

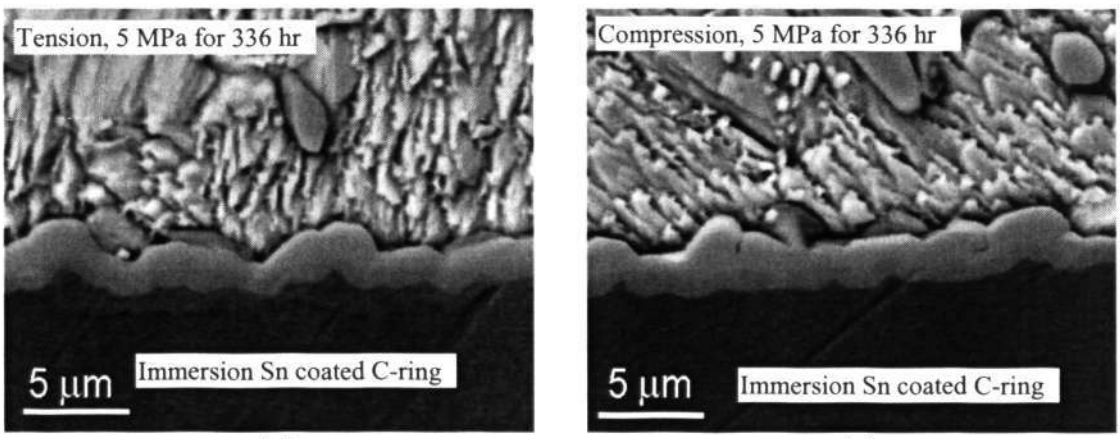
Similar phenomenon was also observed from the study with lower applied stress level at about σ_s = 5 MP and the related microstructures are shown in Figure 6.39.





(c) (f)

Figure 6.38 SEM (BSE) images at solder/coating interface of the immersion Sn coated C-ring solder joint with σ_s = 10 MPa and annealed at 125 °C for various annealing times. Comparable Cu-Sn IMC layer thickness and morphology were observed under both in-plane tension and in-plane compression after exposure to (a) & (d) 336 hr; (b) & (e) 1007 hr and; (c) & (f) 4258 hr of annealing. Under both stresses conditions, the IMC layer thickness increases with the increase of the annealing time.



(a) (e)

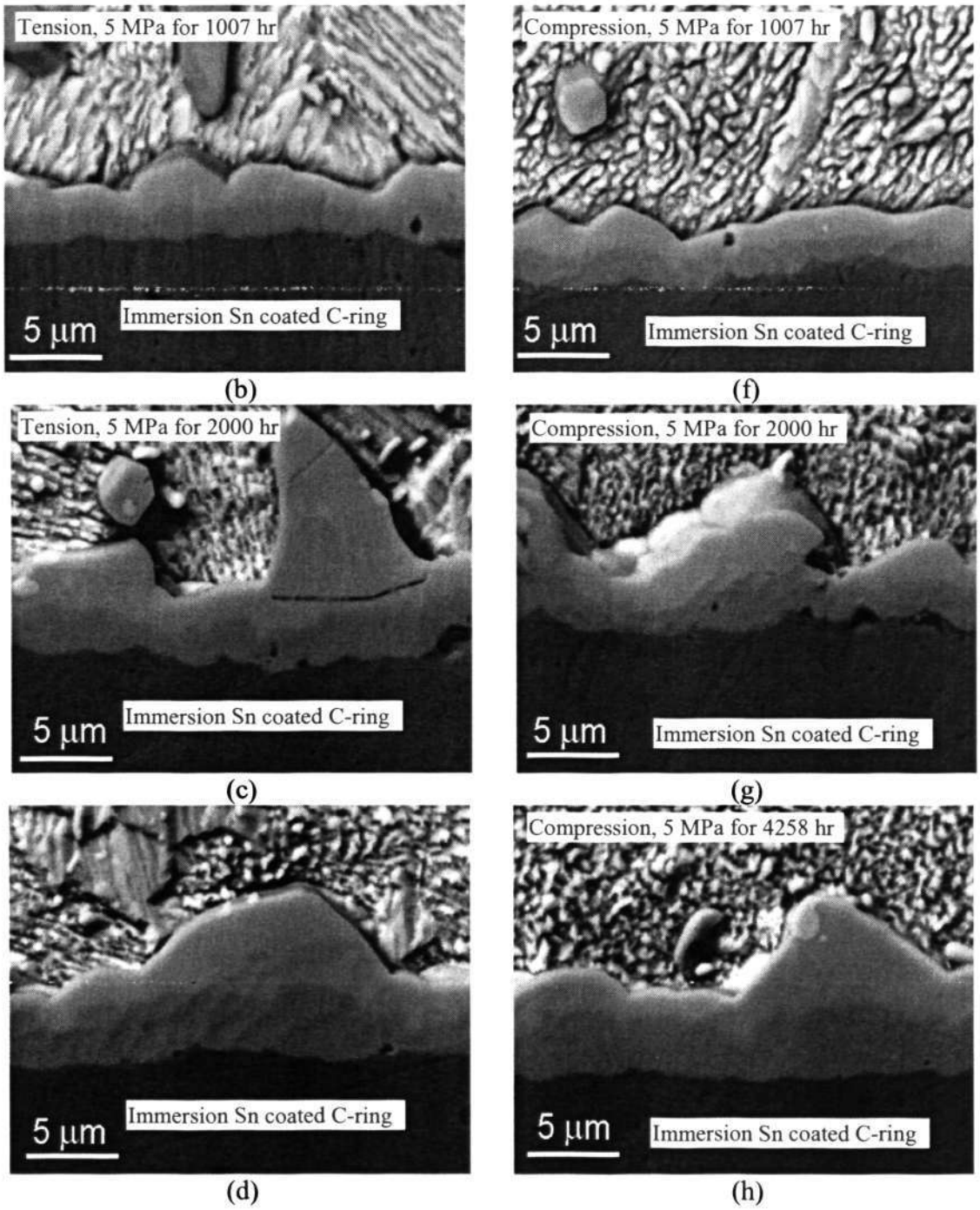


Figure 6.39 SEM (BSE) images at solder/coating interface of the immersion Sn coated C-ring solder joint with σ_s = 5 MPa and annealed at 125 °C for various annealing times. Comparable Cu-Sn IMC layer thickness and morphology were observed under both in-plane tension and in-plane compression after exposure to (a) & (e) 336 hr; (b) & (f) 1007 hr; (c) & (g) 2000 hr and; (d) & (h) 4258 hr of annealing. Under both stresses conditions, the IMC layer thickness increases with increase of the annealing time.

Figure 6.40 shows planar view microstructures of the interface Cu-Sn IMC layer with σ_s = 10 MPa and annealed at 125 °C for 1007 hr under both tensile and compressive stresses conditions. Both tensile and compressive stressed IMC layers showing very similar microstructure. Increase of annealing time has resulted in the formation of larger and more angular scallop-like Cu-Sn IMC together with lots of big and small voids.

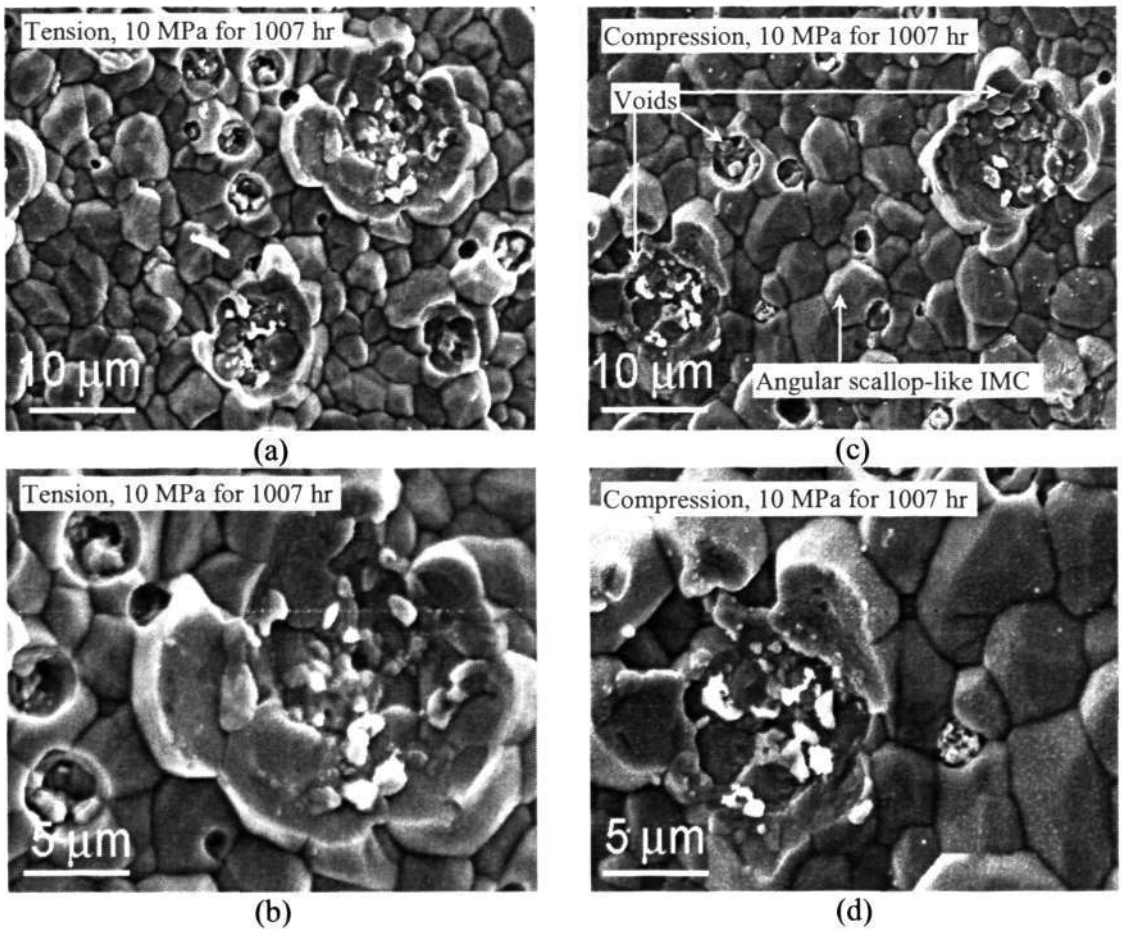


Figure 6.40 SEM (SEI) images of the immersion Sn coated C-ring solder joint with σ_s = 10 MPa annealed at 125 °C for 1007 hr showing the overall planar view of the interface Cu-Sn IMC layer under (a) in-plane tension; (c) in-plane compression consist angular scallop-like IMC with plenty of big and small voids; (b) and (d) are the close up view of (a) and (c) respectively.

6.6 Sn Whisker Growth Study Using C-ring Specimen

The conversion to lead-free processes and products in the electronic industry has resulted in an increasing use of pure Sn coating on leads and surface finish of various components. Sn provides desirable properties and performances, such as excellent solderability, ductility, electrical conductivity and corrosion resistance (Lee and Lee, 1998). Unfortunately, pure Sn and high Sn content alloy plating finishes have received significant scrutiny due to reliability concerns associated with Sn whisker (Choi et al., 2002, Zhang et al., 2004).

Because Sn whisker is both technological important and scientifically intriguing, its formation and growth continue to receive extensive academic and industrial interests. Even though a significant amount of work on Sn whisker have been done, experts in the electronic and electroplating industry still have not reached a consensus upon a single accepted explanation of the mechanism that drives whisker formation. However, most researchers agree that Sn whisker is a case of a surface relief phenomena, i.e., the growth of whisker relieves the compressive stress in the Sn matrix on which they grow (Tu, 1993, Sheng et al., 2002).

Since the specially design C-ring specimen allows in-plane tensile and compressive stresses to be applied and varied by controlling the C-ring diameter, this technique was extended to the study the effect of stress on Sn whisker growth. In one hand, the use of C-ring specimens in this study helps verifying the validity of this method in showing the effect of the stress states on IMC growth. On the other hand, it provides a better understanding on the effects of external applied stresses on Sn whisker growth.

6.6.1 Spontaneous Sn Whisker Growth

The center regions on both inner and outer surfaces of the electrolytic Sn coated C-ring (Figure 6.41) were examined using SEM. SEM analysis was not being performed right after the plating process but after the plated C-ring specimen was stored in desiccator for 24 hr.

The SEM images in Figure 6.42 show the morphologies of the inner and outer surfaces of the as-received electrolytic Sn coated C-ring after storing in desiccator for 24 hr. No hillock and Sn whisker can be seen from the overall planar view of the electrolytic Sn coating surface (Figure 6.42 (a)). The overall view of this Sn coating surface with titled angle of about 10 ° are shown in Figure 6.42 (b) & (c). These images are able to show the surface's prickly morphology more clearly.

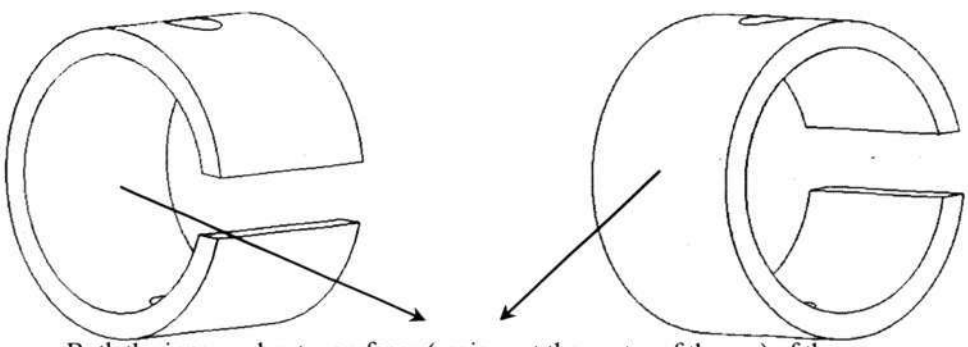
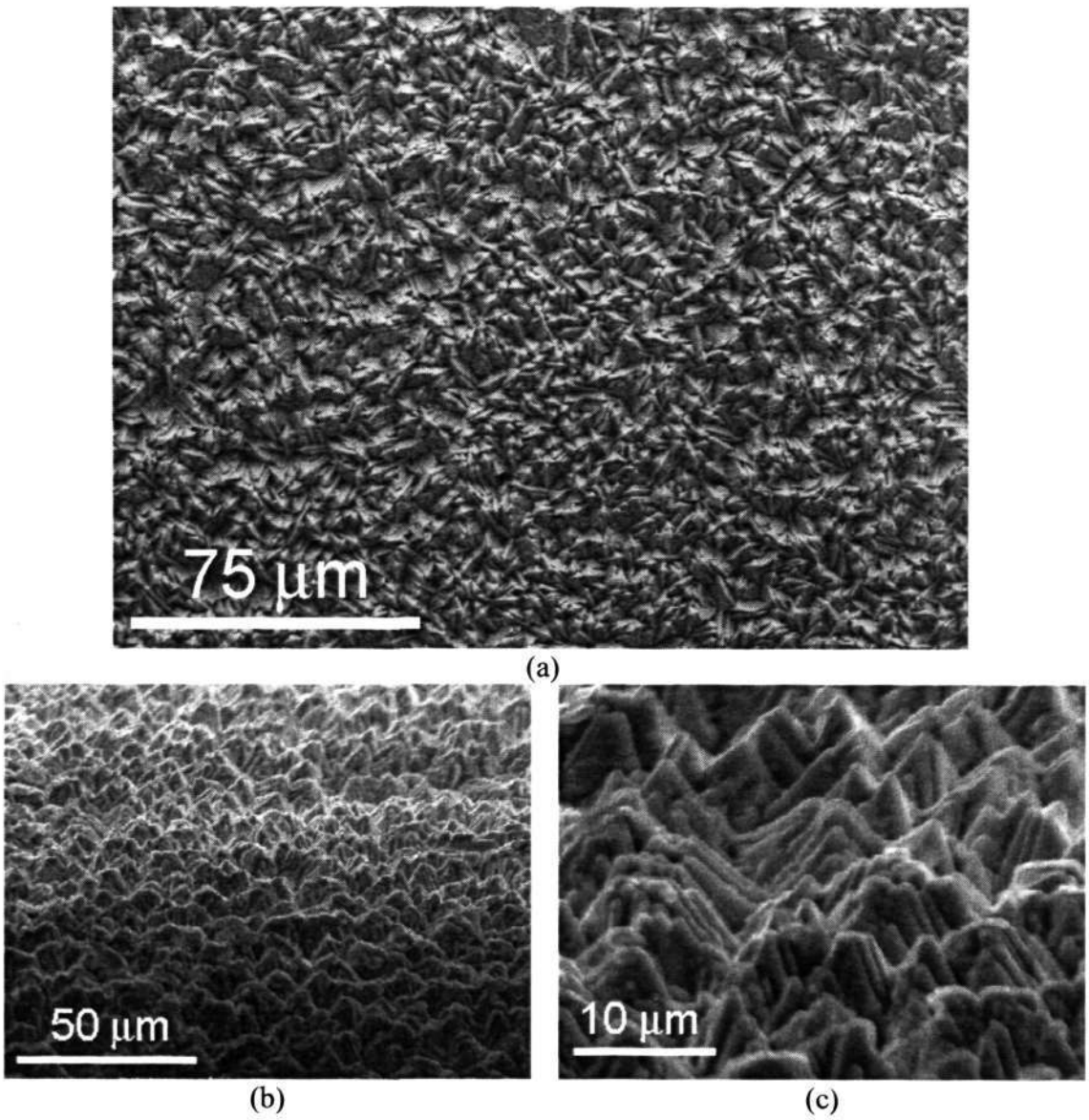


Figure 6.41 Schematic diagram of the C-ring specimen indicates the regions of the electrolytic Sn coated surfaces examined under SEM for surface morphology study.



(a)

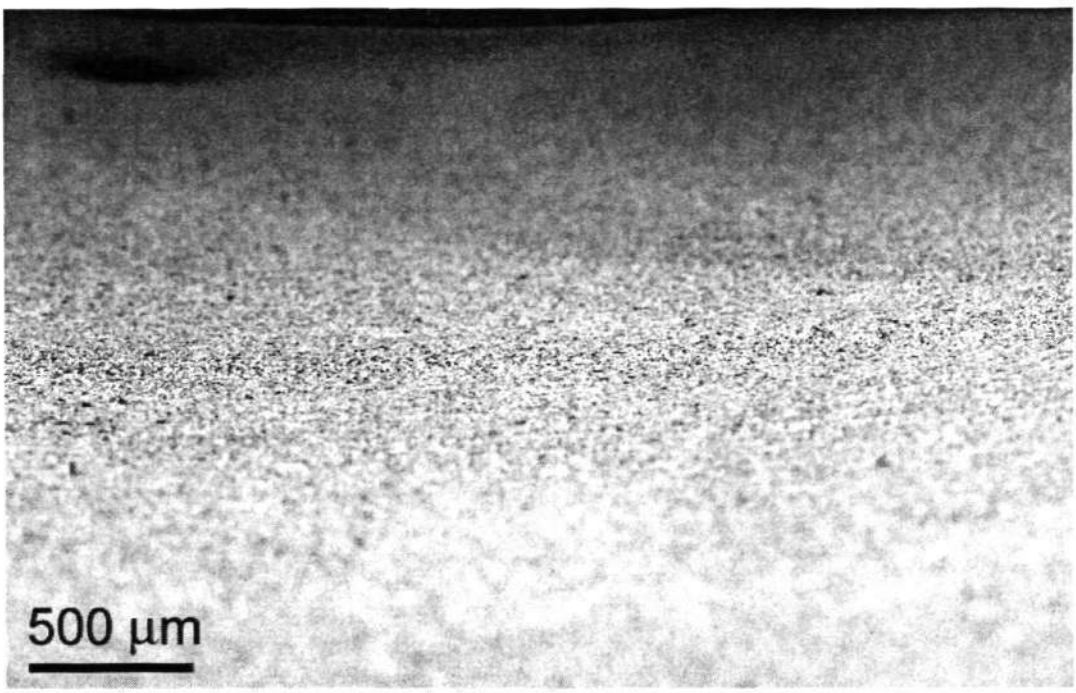
(b)

(c)

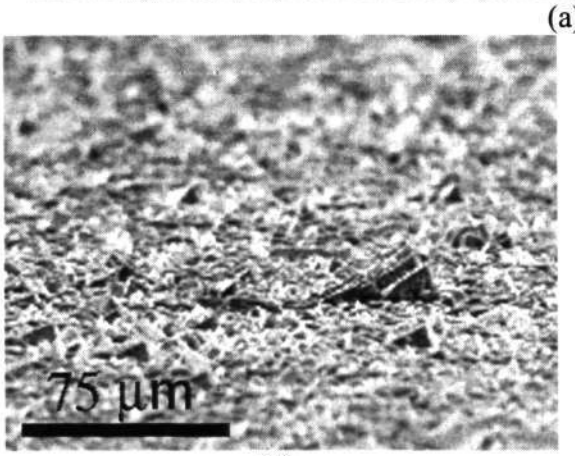
Figure 6.42 SEM images of the electrolytic Sn coated C-ring after storing in desiccator for 24 hr; (a) the overall planar view of the as-received electrolytic Sn coating surface; (b) close up planar view of (a) but with tiled angle of 10 ° showing surface consists of prickly morphology more clearly; (c) further close up view of (b).

The same specimen was reexamined under SEM after storing in the desiccator for another 408 hr without external applied stress. Small hillocks and short Sn whiskers were observed to grow from electrolytic Sn coating layer on both inner and outer surfaces (Figure 6.43). It was being reported (Lee and Lee, 1998) that the residual

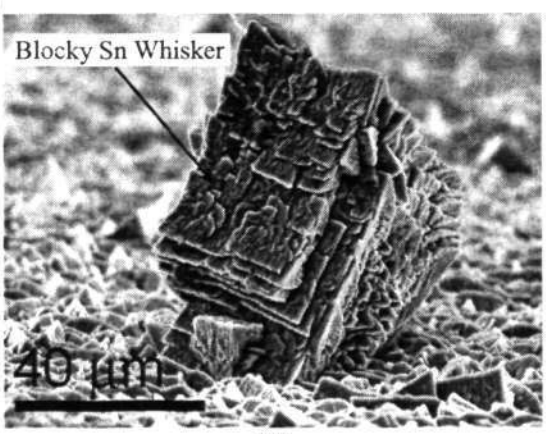
stresses of Sn electrodeposit are the driving force of spontaneous whisker growth as a function of storage time.



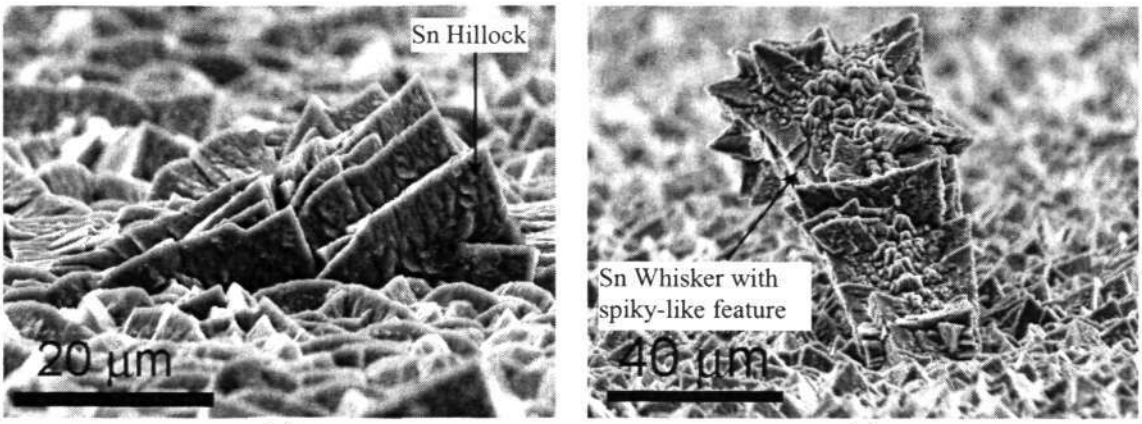
(a)



(b)



(d)



(c) (e)

Figure 6.43 SEM images of the as-received electrolytic Sn coated C-ring after storing in desiccator for 432 hr. (a) The overall view of the coating surface; (b) close up view of the coating surface with some Sn hillocks; (c) further close up view of Sn hillocks; close up views of (d) blocky Sn whisker and ;(e) short spiky-elongated Sn whisker.

Lee and Lee (Lee and Lee, 1998) described that Sn whisker growth is heavily reliant upon the process of diffusion and IMC formation occurring between the Sn layer and the underlying Cu substrate. Cu atoms with high diffusitivity migrate from the substrate material (phosphor bronze) into the Sn layer, preferentially along the Sn grain boundaries. These diffusion elements and the formation of Cu_6Sn_5 IMC induce a compressive stress in the Sn layer as indicated in Figure 6.44. In addition, it was also pointed out that the shear force exerts on the Sn surface oxide is a result of different strains generated in different grains in the direction to the substrate plan. This has caused Sn whisker to grow from the grains whose orientation is different from the major orientation of the Sn film.

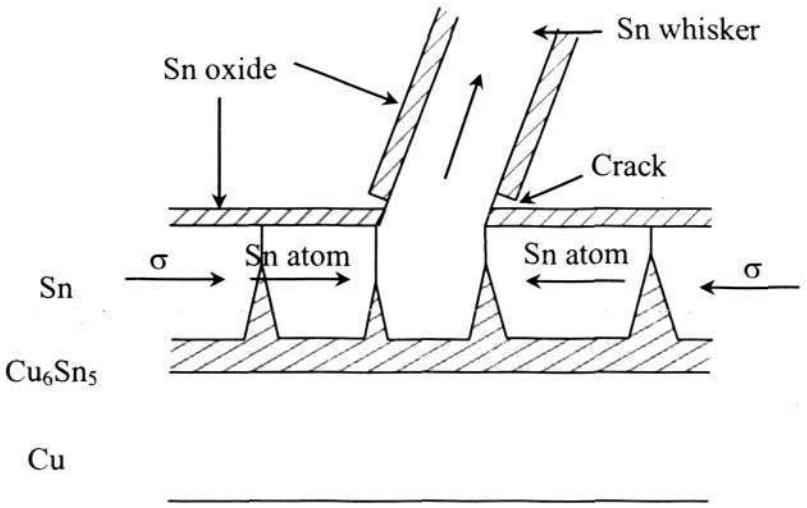


Figure 6.44 Schematic diagram of the cross-section Sn whisker showing Cu_6Sn_5 formed in the grain boundaries and the interface between the Sn film and bronze substrate. The surface of the Sn and the whisker are oxidized except the base of the whisker where the oxide is broken. Diffusion flux of Sn is indicated by arrows in the Sn film (Lee and Lee, 1998).

6.6.2 Effect of Tensile Stress on Sn Whisker Growth at 60 °C and Room Temperature

The center region on the outer surface of the electrolytic Sn coated C-ring as indicated in Figure 6.45, with stress exerted on Sn coating, σ_{sn} = 5 MPa and stored in desiccator for 360 hr was examined under SEM.

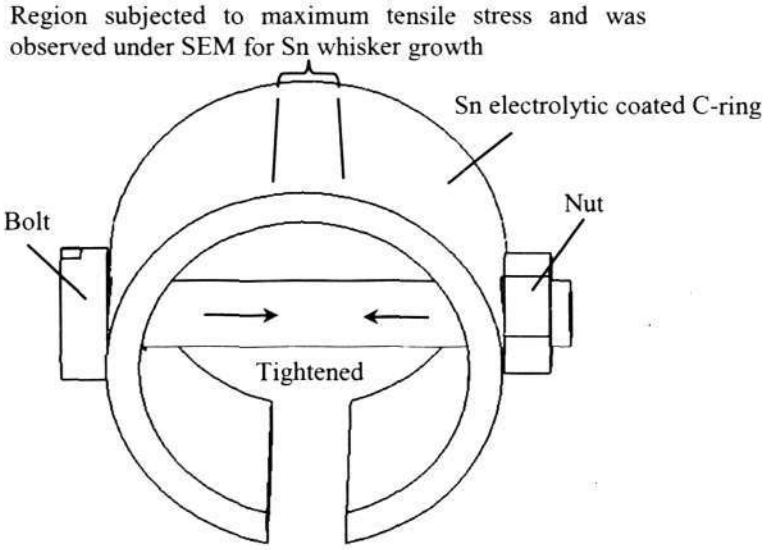


Figure 6.45 Schematic diagram showing the region on the outer surface of the Sn electrolytic coated C-ring that subjected to maximum in-plane tensile was examined for Sn whisker growth.

Short Sn whisker and ranges of Sn hillocks can be observed from the tensile stressed surface after storing in desiccator at room temperature for 310 hr (Figure 6.46). As compared to the unstressed surface (Figure 6.43 (a)), more Sn hillock and less Sn whisker were found on the tensile stressed surface. The counteraction between the compressive residual Sn electrodeposit stress and the external applied tensile stress had retarded the Sn whisker growth.

With storing temperature at 60 °C for 360 hr, Sn hillocks and short Sn whiskers were observed from the tensile stressed surface (Figure 6.47). The density of the hillocks and Sn whisker was comparable to the tensile stressed surface under room temperature.

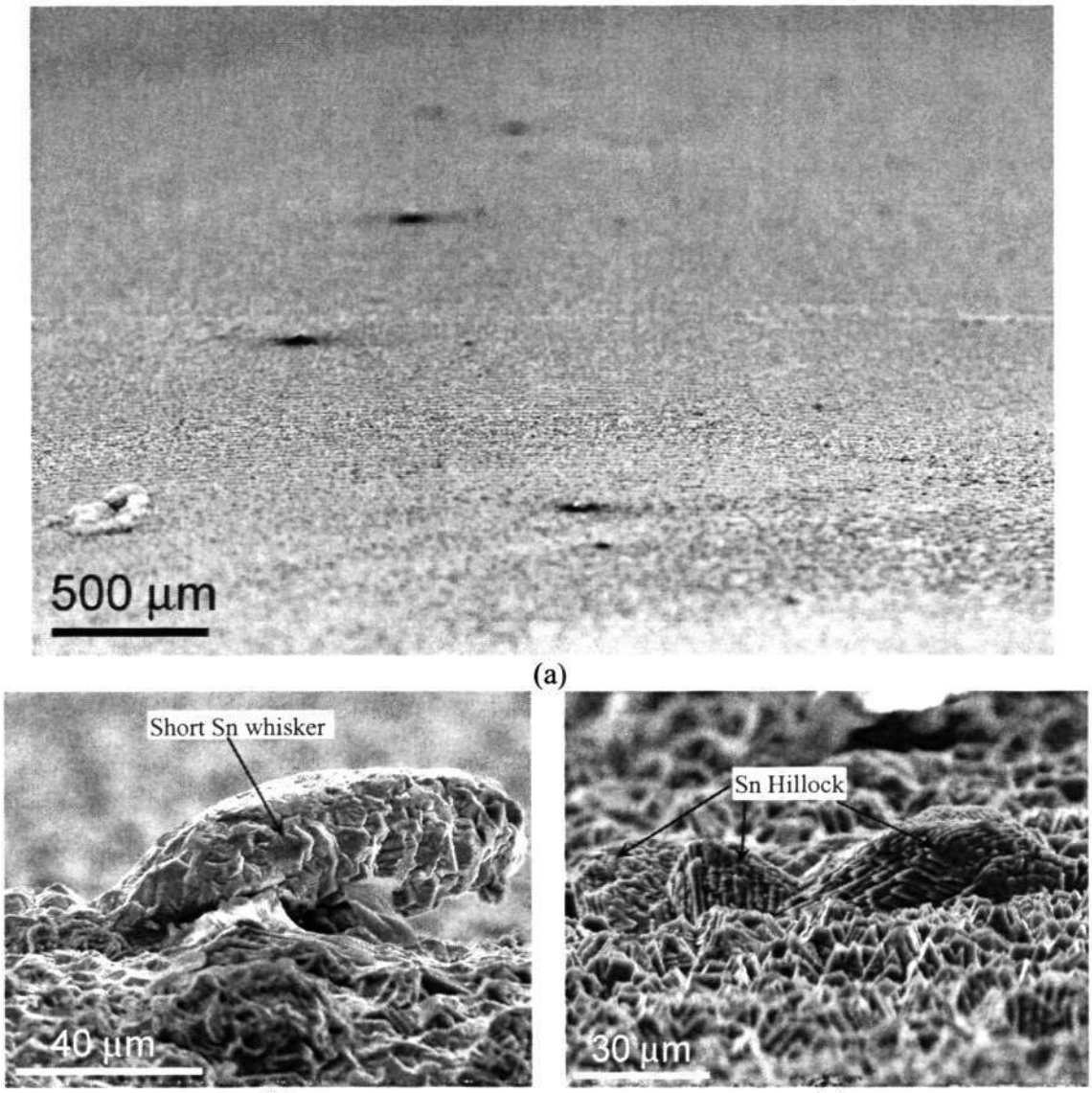


Figure 6.46 SEM images of the electrolytic Sn coating under in-plane tensile stress, σ_{sn} = 5 MPa that stored in desiccators for 310 hr showing (a) the overall view of the coating surface; (b) close up view of a short Sn whisker and; (b) close up view of a range of Sn hillocks.

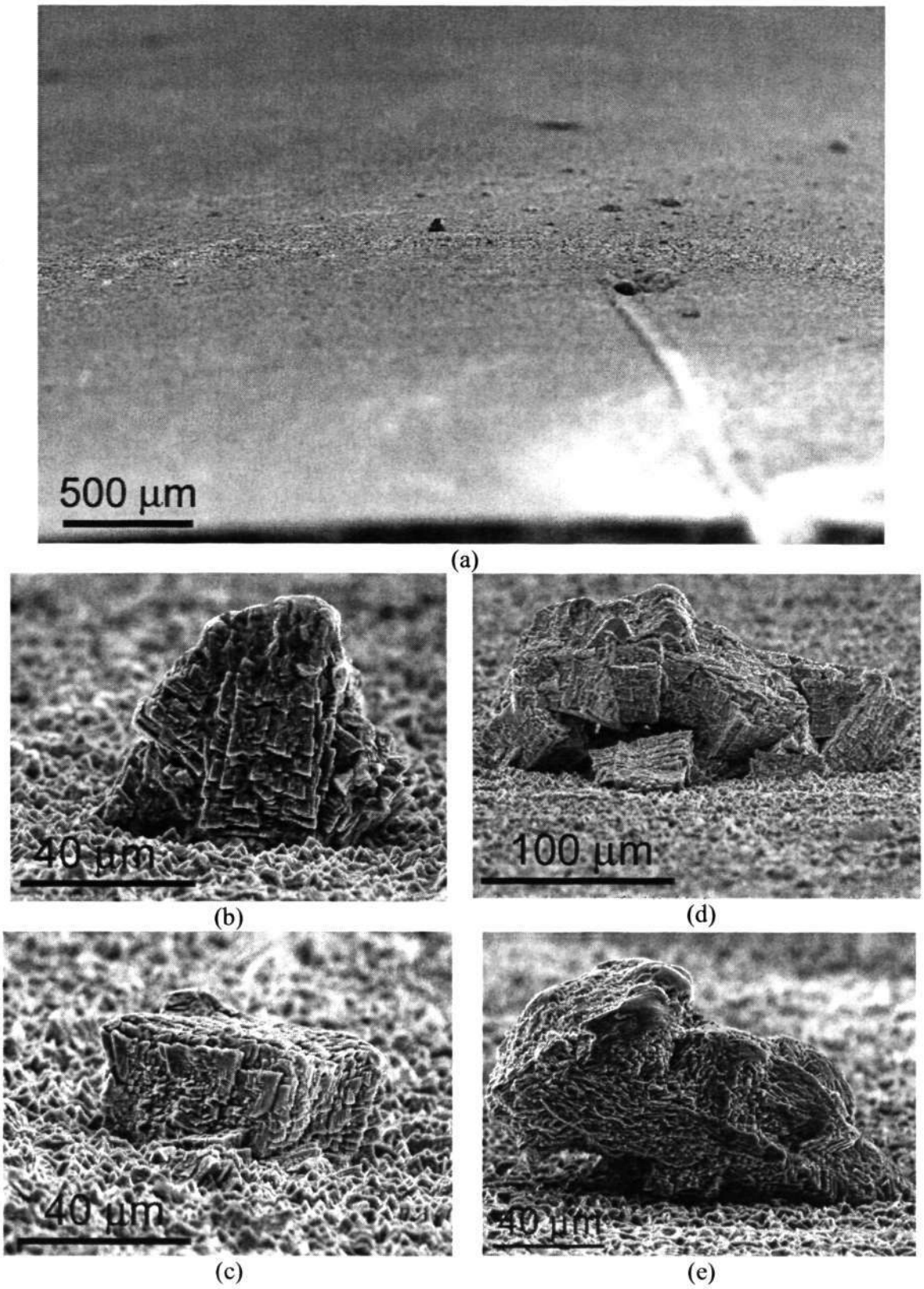


Figure 6.47 SEM images of the electrolytic Sn under tensile stress, σ_{sn} = 5 MPa, stored at 60 °C for 360 hr showing (a) the overall view of coating surface consists of small Sn hillocks and short Sn whiskers; close up view (b) of Sn whisker in triangular shape; (c) Sn whisker in rectangular shape; (d) short blocky Sn whisker and; (e) short Sn whisker.

6.6.3 Effect of Compressive Stress on Sn Whisker Growth at 60 ° C and Room Temperature

Under compressive stress condition, the center region on the inner surface of the electrolytic Sn coated C-ring as indicated in Figure 6.48 was examined under SEM.

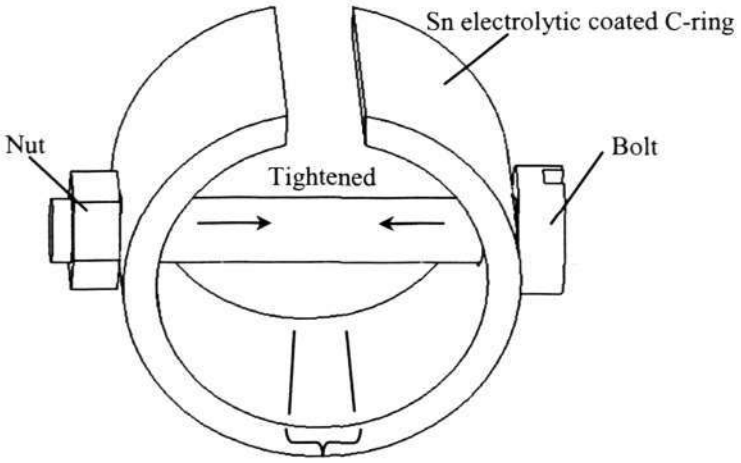


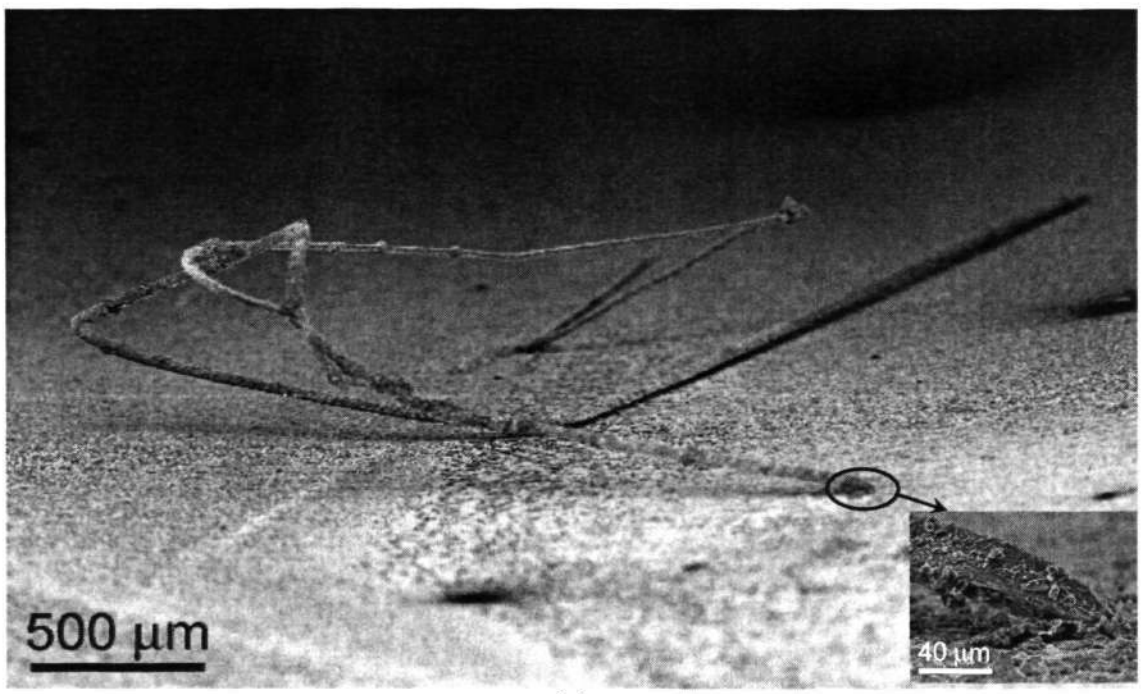
Figure 6.48 Schematic diagram showing the region on the inner surface of the Sn electrolytic coated C-ring that subjected to maximum in-plane compression was examined for Sn whisker growth.

Figures 6.49 and 6.50 show that Sn whiskers with a few millimeters long can be observed from the compressive stressed surface that stored in room temperature and at 60 °C for 310 and 360 hr respectively. Growing and germinating prickly-whisker can also be observed in Figure 6.49 (b) and (c).

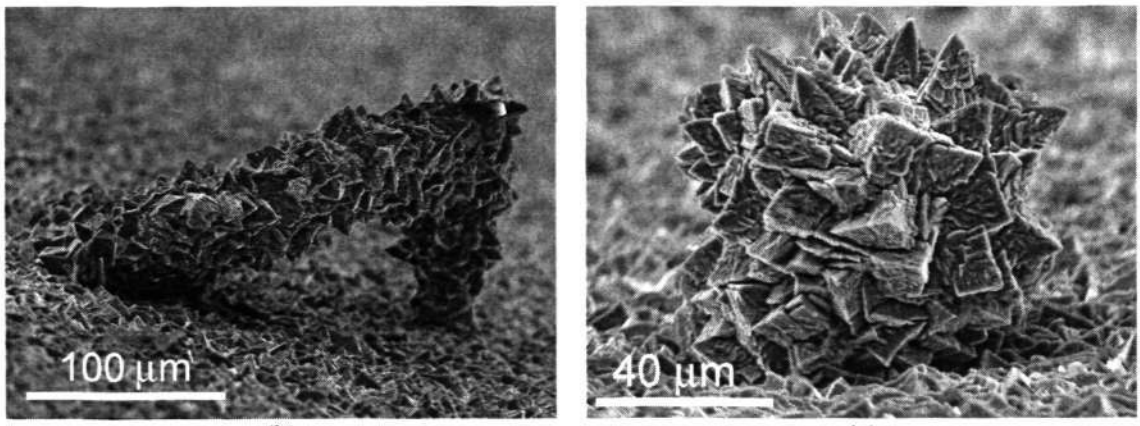
As compared to the tensile stressed surfaces (section 6.6.2), much longer Sn whiskers were found on the compressive stressed surfaces. This show that compressive stress exerted on the inner surface of the C-ring specimen promotes Sn whisker growth.

By observing through the whole compressive stressed surface (region within the two holes), it was found that Sn whisker growth was concentrated at center region of the coating surface for both storing temperatures. This growth distribution pattern shows that the Sn whisker tends to grow at the region with higher compressive stress.

As a whole, this study has demonstrated that the C-ring specimen, with both in-plane tensile and in-plane compressive stresses on the outer and inner surfaces of the same specimen, can be used to predict the Sn whisker formation.

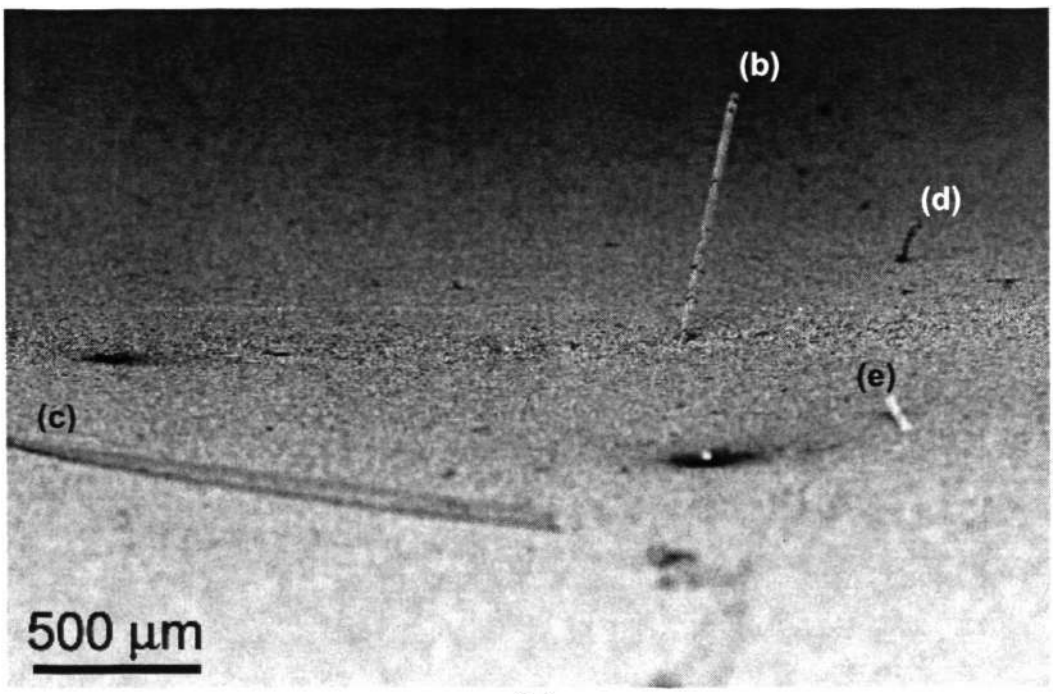


(a)

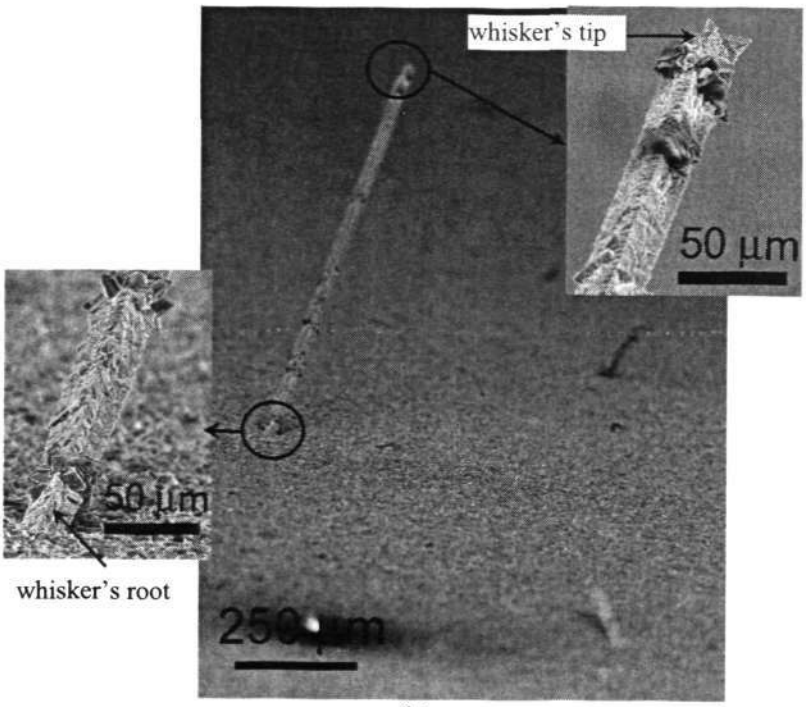


(b) (c)

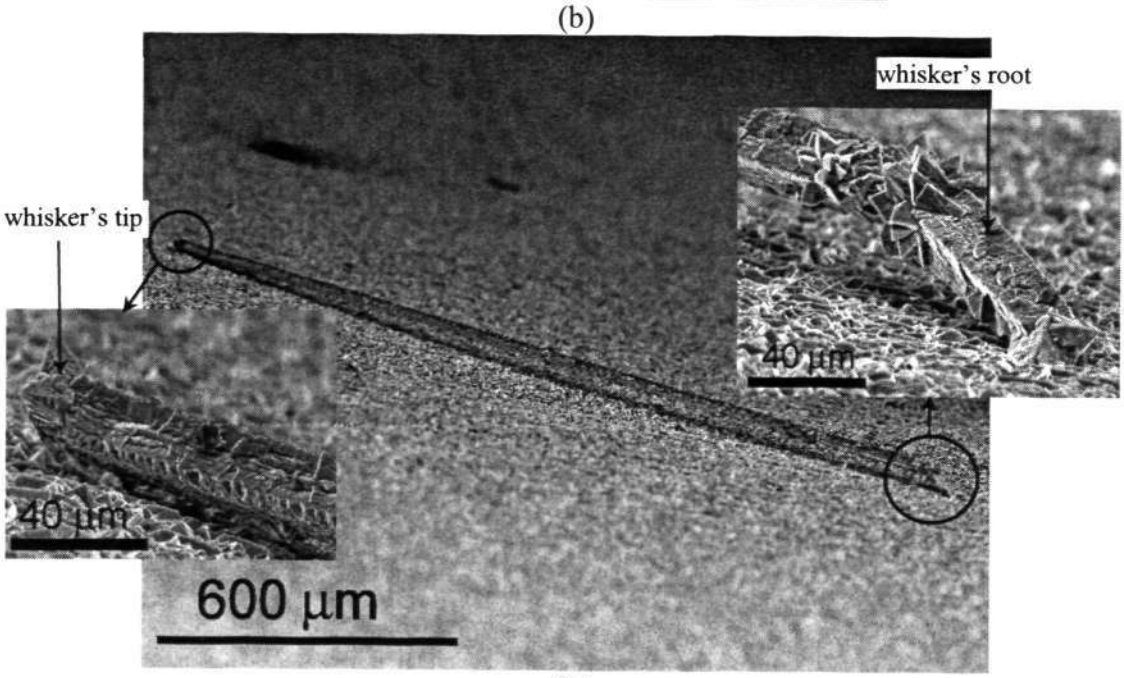
Figure 6.49 SEM images of the electrolytic Sn under compressive stress, σ_{sn} = 5 MPa that stored in desiccators for 310 hr showing (a) the coating surface consists of very long Sn whisker that bent at shape angles; (b) close up view of the growing prickly-whisker bent at shape angle; (c) close up view a germinating prickly-whisker.



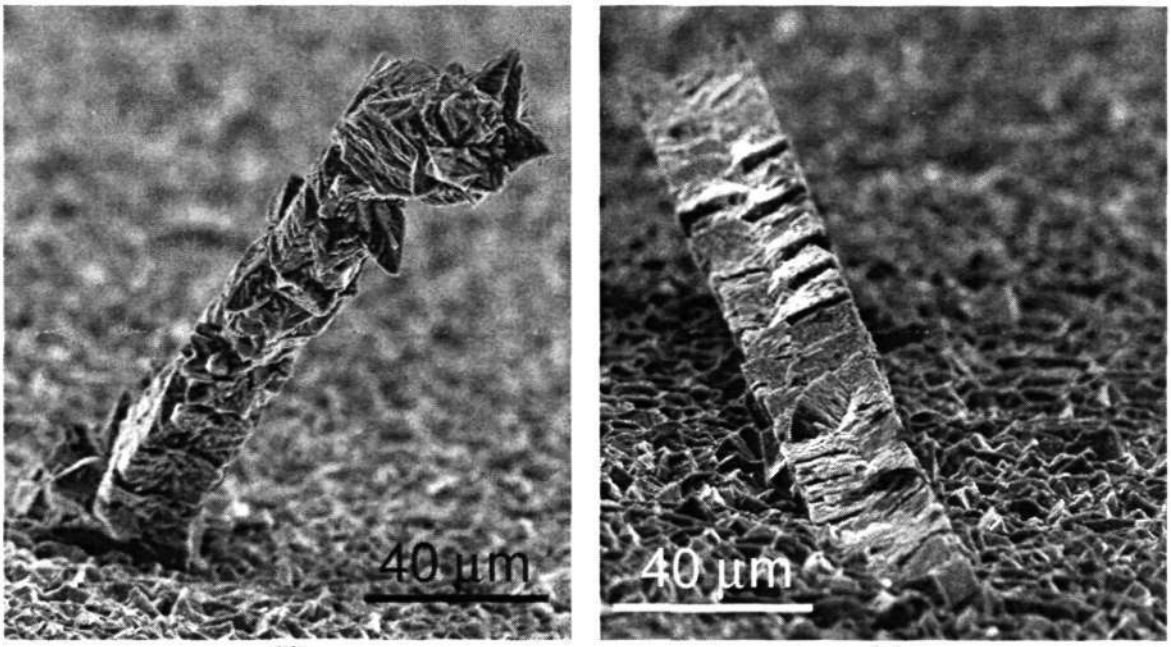
(a)



(b)



(c)



(d) (e)

Figure 6.50 SEM images of the electrolytic Sn coating surface under compressive stress, σ_{sn} = 5 MPa stored at 60 °C for 360 hr. (a) Overall view of the coating surface consists relatively long Sn whiskers. The close up views of (b) & (c) long Sn whiskers and; (d) & (e) short Sn whiskers with spiky-like features along the whisker.

6.7 Discussion and Summary

The specially designed C-ring specimen was shown to provide consistent and reliable results for the study on the effect of stress state on interface IMC growth. When an in-plane tensile and compressive stress was applied to the solder in a controlled manner, the growth of IMC was faster in the interface subjected to compressive stress than that subjected to tensile stress for bare Cu substrate, Cu substrate coated with ENIG, and Cu substrate with ENEPIG coating. In addition, the IMC growth rate was found to increase with the magnitude of applied compressive stress.

The observation strongly supports the argument in the last chapter that stress plays an important role in influencing the diffusion rate and IMC growth. Furthermore, the controlled study clarifies that it is compressive stress that promotes IMC growth.

The project adopts an engineering approach to packaging reliability issue, so the emphasis is not placed on understanding the physics of the stress-driven diffusion mechanism. However, a possible explanation on the compressive stress promoted IMC growth may be offered in terms of the effect of compressive stress on promoting diffusion of Cu, Ni or Pd from the coating and substrate towards the IMC. When the solder-substrate interface is subjected to compressive loading, both solder and substrate experiences the same strain, but the compressive stress is much higher in the substrate because it has greater Young's modulus. The higher compressive stress can be a driving force for outdiffusion of Cu, Ni or Pd towards the solder and thus promotes the IMC growth. However, it is noted that this argument cannot explain well why the applied stress state did not show noticeable difference in the IMC growth for the Cu substrate coated with immersion Sn.

The C-ring technique is shown to be applicable to other studies, for example, to study of Sn whisker growth. In-plane compressive stress was found to promote Sn whisker growth. In contrast, exerting in-plane tensile stress on the Sn electrolytic coating surface retards the Sn whisker growth.

Chapter 7: Conclusions and Recommendations

7.1 Conclusions

7.1.1 Microstructure Evolution during Annealing of Bulk Solders

Effect of temperature on the microstructure of 95.5Sn-3.8Ag-0.7Cu lead-free solder was studied using a fixed annealing time of 1 hr but at various annealing temperatures of 60, 125 and 190 °C. Annealing at homologous temperature at 0.68Tm (60 °C) or 0.81Tm (125 °C) for 1 hour produces no observable microstructural change. However, increase of annealing temperature to homologous temperature at 0.94Tm (190 °C) results in IMCs which are smaller in number, larger in size and more rounded in shape, indicating the growth of large IMCs at the expense of the small ones.

Effect of time on the microstructures of 95.5Sn-3.8Ag-0.7Cu solder was studied at a fixed annealing temperature at 190 °C. Coarsening of the IMC was stabilized after exposure to annealing time of 9 hr. Further increasing in annealing time from 9 to 25 hr did not lead to any significant change of IMC.

To further study the effects of annealing temperature and time, IMC growth of the 99.3Sn-0.7Cu lead-free solder was carried out through a specially designed in-situ observation technique. The growth of individual IMC particles with respect to temperature and heating time was monitored. This study helps to understand the IMC growth mechanism better with much closer monitoring of the IMC growth. Generally, the initial growth of all IMC particles displays a nearly linear relationship. The study highlights the fact that the controlling mechanism for IMC growth in bulk solders is different from that in the presence of a substrate.

7.1.2 Isothermal, Thermal Cycling and Thermal Shock Aging on Intermetallics Growth

Effect of isothermal aging on the IMC of solder/copper joint (95.8Sn-3.5Ag-0.7Cu lead-free solder with ENIG/Cu substrate) was carried at three different temperatures of 125, 150 and 175 °C. Coarsening of IMC in solder occurs at all three temperatures for extended aging time. The increase of temperature results in faster coasening process.

The growth of interface IMC layer was negligible for isothermal aging at 125 °C. The interface IMC growth is proportional to the square root time at 150 and 175 °C. However, the growth failed to sustain for extend time. This can due to some possible reasons:

(a) The growing of Cu-Ni-Sn IMC was retarted by the limited supply of Ni flux from the diminishing ENIG coating;

(b) The ripening process of Cu-Ni-Sn IMC in multiple directions has masked the growing rate in the verical direction; and

(c) The formation of additional $(Ni,Cu)_3Sn_4$ phase between the $(Cu,Ni)_6Sn_5$ phase and ENIG coating that grows in much slower rate can also decrease the overall growth of rate of the IMC layers.

Effect of nonisothermal aging on the IMC was performed by subjecting the FR4-solder joint (95.5Sn-3.8Ag-0.7Cu with Ni/Au/Cu) to 500, 1000 and 2000 cycles of TC and TS. Coarsening of IMC in solder was not observable under either TC or TS condition. The growth of the Cu-Ni-Sn IMC layer for both TC and TS is linearly proportional to square root of total accumulated dwell time at maximum temperature (125 °C). It is interesting to observe that the interface IMC growth is considerably faster

in TS than in TC and the faster growth in TS is attributed to the accelerated diffusion resulted from the higher thermal stresses in TS.

An in-situ fractography technique was used to study deformation and fracture of the solder/copper joints. Both as-reflowed and isothermally aged joints were tested. The fracture was found to be predominantly intergranular for all the joints. The major fracture path is within the solder near the substrate for the as-reflowed joints (one, three or six times flowed) but along the interface between solder and IMCs grown from the substrate for the joints isothermally aged at 125 and 150 °C, indicating embrittlement of IMCs caused by the aging treatment.

7.1.3 Effect of Stress State on Interface IMC Growth

The specially designed C-ring specimen was shown to provide consistent and reliable results for the study on the effect of stress state on interface IMC growth. When an in-plane tensile and compressive stress was applied to the solder in a controlled manner, the growth of IMC was faster in the interface subjected to compressive stress than that subjected to tensile stress for bare Cu substrate, Cu substrate coated with ENIG, and Cu substrate with ENEPIG coating. In addition, the IMC growth rate was found to increase with the magnitude of applied compressive stress. However, the applied stress state did not show noticeable difference in the IMC growth for the Cu substrate coated with immersion Sn.

The C-ring technique is shown to be applicable to other studies, for example, to study of Sn whisker growth. In-plane compressive stress was found to promote Sn whisker growth. In contrast, exerting in-plane tensile stress on the Sn electrolytic coating surface retards the Sn whisker growth.

7.2 Recommendations

The effect of stress state on the interface IMC layer was successfully determined using the specially designed C-ring solder joint specimen. This C-ring solder joint specimen can be further utilized to understand the physics of the stress-driven diffusion mechanism.

The crystallographic study on the tensile and compressive stressed IMC layers is needed to understand the stress-driven diffusion mechanism. This crystallographic study includes the detailed phase identification of the IMC layer, analysis of internal defect structures and the interaction analysis between the elements involved in the diffusion systems.

TEM (Transmission Electron Microscope) and EDSB (Electron Back-scattered Diffraction) can be used to perform the crystallographic study mentioned in the preceding paragraph. However, more stringent sample preparation on the C-ring solder joint specimen is needed for TEM analysis. Therefore, there is a need to develop a methodology for TEM sample preparation. A possible technique to accomplish this purpose could be by using FIB (Focus Ion Beam).

It is important to note that this project was carried out to address the reliability issue in electronic packaging by looking into both the microstructure and mechanical properties of the solder joint. However, the study on the mechanical properties only provides preliminary results and further studies need to be performed. The tensile fracture mechanism of the solder joint through in-situ fractography technique is worth extending. It would be very helpful to test the solder joint under isothermal aging at different temperatures and times, as well as under TC and TS conditions.

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