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Effect of Nickel Silicide Induced Dopant Segregation on Vertical Silicon Nanowire Diode Performance

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ABSTRACT

In this work, Dopant Segregated Schottky Barrier (DSSB) and Schottky Barrier (SB) vertical silicon nanowire (VSiNW) diodes were fabricated on *p*-type Si substrate using CMOS-compatible processes to investigate the effects of segregated dopants at the silicide/silicon interface and different annealing processes on nickel silicide formation in DSSB VSiNW diodes. With segregated dopants at the silicide/silicon interface, VSiNW diodes showed higher on-current, due to an enhanced carrier tunneling, and much lower leakage current. This can be attributed to the altered energy bands caused by the accumulated Arsenic dopants at the interface. Moreover, DSSB VSiNW diodes also gave ideality factor much closer to unity and exhibited lower electron SBH (Φ_{Bn}) than SB VSiNW diodes. This proved that interfacial accumulated dopants could impede the inhomogeneous nature of the Schottky diodes and simultaneously, minimize the effect of Fermi level pinning and ionization of surface defect states. Comparing the impact of different silicide formation annealing using DSSB VSiNW diodes, the 2-step anneal process reduces the silicide intrusion length within the SiNW by ~ 5X and the silicide interface was smooth along the (100) direction. Furthermore, the 2-step DSSB VSiNW diode also exhibited much lower leakage current and an ideality factor much closer to unity, as compared to 1-step DSSB VSiNW diode.

INTRODUCTION

Silicon nanowires (SiNWs) [1-3] are viewed as serious contender for technology nodes beyond 14 nm because SiNWs can provide gate-all-around (GAA) transistor architecture to boost the gate electrostatic control over the channel inversion. In order to take full advantage of the GAA nanowire geometry, vertical nanowires (VSiNWs) are preferred. This is because they occupy smaller estate area than planar transistors at the same technology node, and they resolve the problems, such as gate definition under the wire and gate etching on the wire, faced by lateral nanowires [4].

Contact and series resistances of source/drain regions pose a serious problem for SiNW transistors. In order to alleviate this issue, Schottky Barrier (SB) junctions, formed via rapid thermal annealing (RTA) and/or laser annealing [5-9], are introduced. With its metal-like

resistance, SB junctions offer an alternative to doped S/D regions. However, SB junctions are associated with Schottky Barrier Height (SBH) which impedes the charge carrier flow and affects the device performance. PtSi and rare earth silicides, such as $ErSi_x$ or $YbSi_x$, provide the lowest known SBH for *p*- and *n*-type SB-MOSFETs, respectively [9]. Dopant segregation (DS) technique, whereby a thin and heavily doped silicon layer formed at the silicide/silicon interface during silicidation, was introduced to further reduce the SBH of planar [11] and lateral SiNW [3] transistors.

However, to date, there is no study to investigate the impact of DS technique in SB VSiNW devices and the effect of different RTA silicidation methods on silicide formation. In this paper, we present our findings on nickel silicide (Ni_xSi_y) intrusion length within Dopant Segregated SB (DSSB) VSiNW diodes, the ideality factor values and electron SBH (Φ_{Bn}) of DSSB and SB VSiNW diodes. Nickel was chosen because of its low Si consumption, low formation temperature and low sheet resistance in narrow features [12-13].

EXPERIMENT

The whole fabrication process is presented briefly in Figure 1. Nitride hard mask was first patterned on 8" *p*-type (~ $10^{15}cm^{-3}$) silicon (100) wafers by photoresist nanodots defined using 248 nm lithography. This is followed by photoresist removal and 300 nm Si etch using deep reactive ion etch (DRIE). Thermal oxidation and dilute HF (DHF) etch were performed to reduce the nanowire diameter. VSiNWs with diameter of 40-200 nm were obtained. Non-conformal high density plasma (HDP) oxide deposition followed by RIE oxide etchback was done to obtain a 40 nm oxide spacer around the VSiNWs. The substrate was doped with BF_2 (10 keV/ 4 x 10^{15} $cm^{-2}/0^o$ tilt; activation 1000^oC/ 5 s) to achieve Ohmic contact. HDP oxide deposition followed by DHF etch-back was again used to expose only the VSiNW tip. For the DS split, the VSiNW tip was implanted with Arsenic (four orthogonal implants: 10 keV/ 1 x 10^{15} $cm^{-2}/7^o$ tilt) prior to Ni deposition. For the non-DS split, no Arsenic implant was done. 30 nm Ni was then deposited followed by a 1-step at 450^oC/ 30 s or 2-step at 275^oC/ 30 s and 450^oC/ 30 s rapid thermal annealing (RTA) in nitrogen ambient. The un-reacted Ni was etched away after the first RTA anneal by immersing the wafers in sulfuric peroxide (H_2SO_4:H_2O_2) solution for 5 min. Finally, aluminum metal contacts were formed and sintering (10% H_2: 90% N_2) was performed at 420^oC for 30 mins.

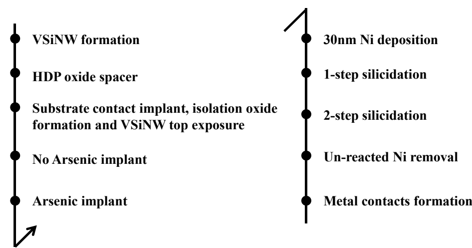

Figure 1. Flow of the VSiNW fabrication process.

DISCUSSION

Figures 2(a) and (b) show the room temperature *I-V* characteristics of 50 nm diameter single SB and DSSB VSiNW diodes fabricated via a 1-step and 2-step RTA silicidation, respectively. The device with DS is plotted using red circle and the device without DS is plotted using black square. The diode forward current ($I_{forward}$) is extracted at V = -2 V and the diode reverse current ($I_{reverse}$) is extracted at V = +2 V. It is evident that $I_{forward}$ and $I_{reverse}$ of DSSB VSiNW diodes show at least 3X increment and 1 order in magnitude reduction, respectively, as compared to that of diodes without DS implant.

In terms of current rectification ratio R_c, calculated as $I_{forward}$/ $I_{reverse}$, the DSSB VSiNW diodes exhibit ~ 7 orders of magnitude higher than SB VSiNW diodes. R_c can be used as a representative of the ambipolar behavior commonly observed in Schottky Barrier devices. A lower R_c value signifies that the device has a strong ambipolar behavior and vice versa. Since the DSSB VSiNW diodes show a much higher R_c value ($\sim 10^{11}$) than devices without DS implant ($\sim 10^4$), this proves that DS implant is able to impede the undesirable ambipolar behavior typical in Schottky Barrier devices.

The mechanism for the increment in $I_{forward}$ and reduction in $I_{reverse}$ can be explained by the formation of dipoles at the silicon/silicide interface due to the Arsenic implant to the VSiNW tip [14]. With the formation of the dipoles, the energy band at the silicon surface near the silicon/silicide interface is altered significantly such that electron tunneling is enhanced and simultaneously, the thermal emission of holes is impeded. Therefore, with the incorporation of DS implant, higher $I_{forward}$ and lower $I_{reverse}$ are achieved.

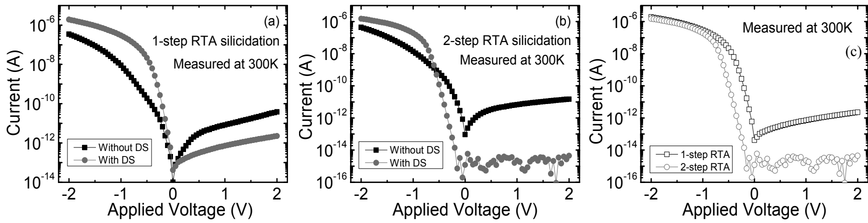

Figure 2. (a) *I-V* measurement data of single VSiNW diode fabricated via (a) 1-step RTA and (b) 2-step RTA silicidation method. Devices with DS implant demonstrate higher $I_{forward}$ and reduced $I_{reverse}$ than devices without DS implant for both silicidation methods. All measured devices have 50 nm diameter and characterized at 300 K. (c) Comparison of *I-V* data between devices with DS implant fabricated using different RTA silicidation methods. Both RTA silicidation exhibit similar $I_{forward}$ but the 2-step RTA silicidation reduces $I_{reverse}$ by ~ 2 orders of magnitude.

Room temperature *I-V* data of the 1-step and 2-step RTA silicided DSSB VSiNW diodes were also compared to demonstrate the effect of different silicidation methods on the diodes' electrical characteristics (Figure 2c). From Figure 2(c), the fabricated devices exhibit similar $I_{forward}$ ~ 1 μA. However, $I_{reverse}$ of the 2-step RTA silicided diode at V = +2 V is ~ 3 orders of magnitude lower than that of the 1-step RTA silicided diode. This shows that the 2-step RTA silicidation is more effective in reducing the $I_{reverse}$, which is similar to the $I_{leakage,S/D}$ (leakage

current between source and channel or drain and channel), one of the critical parameters which determines the overall performance of transistors.

Apart from the improvements in $I_{forward}$ and $I_{reverse}$, other electrical parameters such as ideality factor (η) and Φ_{Bn} have also improved with the DS implant. η and Φ_{Bn} are plotted against the measurement temperatures as shown in Figures 3(a) and (b), respectively. From Figure 3(a), DSSB VSiNW diodes (plotted in red circles and pink inverted triangles) generally exhibit much lower η than those without DS implant. Since deep-level interface defects are introduced into silicon during nickel silicide formation by RTA [15], DS implant is able to passivate these interfacial defects and causes η to be improved close to unity.

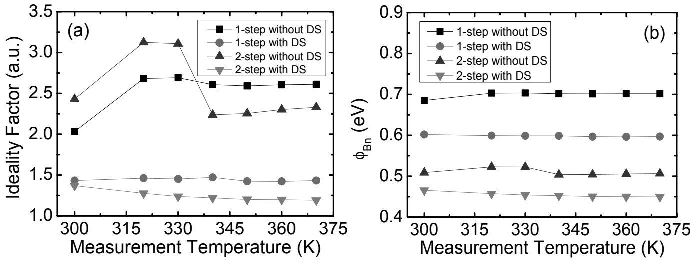

Figure 3. (a) η as a function of measurement temperatures taken from VSiNW diodes with and without DS implant. VSiNW diode with DS implant generally exhibited lower ideality factor values than VSiNW diodes without DS implant. (b) Φ_{Bn} values as a function of measurement temperatures taken from VSiNW diodes with and without DS implant. Incorporation of DS implant is able to effectively reduce the Φ_{Bn} by ~ 0.05 eV to 0.1 eV.

Concurrently, the segregated interfacial dopants cause significant alteration of the interface energy bands as explained earlier. This results in a reduced Φ_{Bn} and increases the electron tunneling probability. As shown in Figure 3(b), diodes with DS (plotted in red circles and pink inverted triangles) generally demonstrate a reduction of 0.05 to 0.1 eV in Φ_{Bn} as compared to devices without DS. Simultaneously, the effect of RTA silicidation method on the ideality factor and Φ_{Bn} is also demonstrated in Figures 3(a) and (b). the 2-step RTA silicided DSSB VSiNW diodes (denoted in pink inverted triangles) distinctively show reduced Φ_{Bn} and lower ideality factor value than the 1-step RTA silicided DSSB VSiNW diodes (denoted in red circles). With the reduction of Φ_{Bn}, the series resistance of the overall *n*-MOSFET device can be minimized and this will lead to an improved electrical performance.

From Figures 4(a) and (b), it is evident in that the 1-step silicidation method produces deeper top silicide length as compared to that of the 2-step silicidation method. The top silicide length is about 113 nm for the 1-step silicidation and 22 nm for the 2-step silicidation process. This signifies ~5X reduction in the silicide length. The reduction in silicide length is also reported for planar [16] and lateral SiNW [17] structures. However, it should be noted that the magnitude of silicide length reduction varies for different structures.
Another interesting observation is the formation of a 'V'-shaped silicide/silicon interface along the (111) Si in the 1-step silicided VSiNW while the interface in the 2-step silicided VSiNW is

relatively smooth along the (100) Si. The continuous supply of nickel atoms, the thermal energy supplied during the 1-step silicidation process and the low energy of Si (111) planes can offer possible explanation for the formed ‘V’-shaped interface. Further details can be found in [18]. The control over the silicide intrusion length is vital for designing VSiNW transistors to minimize the gate to source/drain overlap capacitance. Moreover, it is critical to form an abrupt and smooth silicide/Si interface such that the electric field, between the source/drain and the channel, is identical at every point along the interface to minimize local variation in SBH.

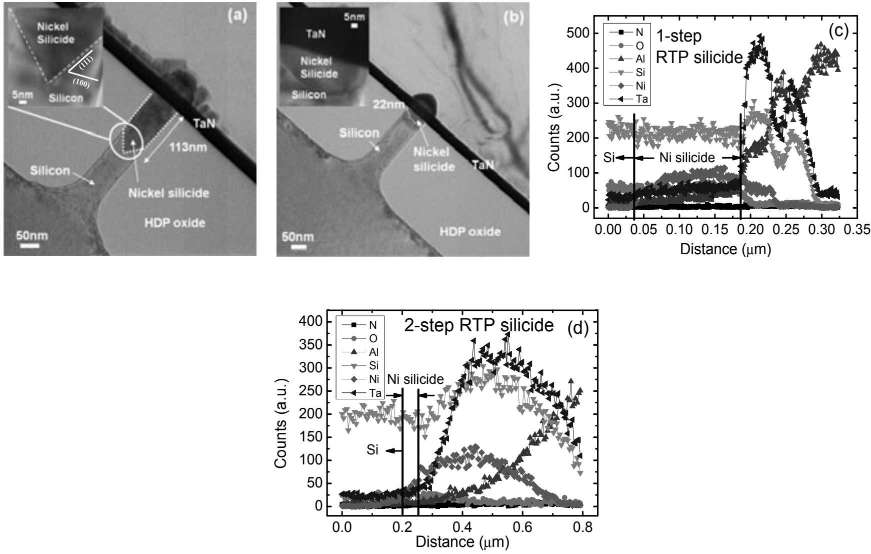

Figure 4. Transmission Electron Micrography (TEM) images of DSSB VSiNW diodes fabricated via (a) 1-step and (b) 2-step silicidation methods. The 2-step silicided diode showed a 5X reduction in the top silicide intrusion length as compared to the 1-step silicided diode. The silicide intrusion length is further confirmed by TEM-EDX line-scan analysis in (c) and (d).

CONCLUSIONS

DSSB and SB VSiNW diodes have been fabricated using all CMOS-compatible processes. With a DS implant amorphisation and 2-step RTA silicidation method, the undesirable silicide intrusion length is reduced by ~5X. From the measured electrical, the fabricated diodes demonstrate an increase in $I_{forward}$ and a significant reduction in $I_{reverse}$ through the introduction of DS into VSiNWs. Furthermore, the DS implant is able to lower η and effectively reduce Φ_{Bn}. Comparing the different silicidation methods used in the fabrication, the 2-step RTA silicided DSSB-VSiNW diode shows lower $I_{reverse}$ than the 1-step RTA silicided DSSB-VSiNW diode. Similarly, the 2-step RTA silicidation method also demonstrate η closer to unity (η =1) and lower

Φ_{Bn} than the 1-step RTA silicidation method. Hence, the combination of DS implant and 2-step RTA silicidation has shown to enhance VSiNW diode electrical performance. In summary, the results of this work pave the way to improve Schottky Barrier nanowire devices for future technology.

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