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Detrimental influence of catalyst seeding on the device properties of CVD-grown 2D layered materials: A case study on $MoSe_2$

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Seed catalyst such as perylene-3,4,9,10-tetracarboxylic acid tetrapotassium (PTAS) salt has been used for promoting the growth of atomically thin layered materials in chemical vapor deposition (CVD) synthesis. However, the ramifications from the usage of such catalyst are not known comprehensively. Here, we report the influence of PTAS seeding on the transistor device performance from few-layered CVD-grown molybdenum diselenide ($MoSe_2$) flakes. While better repeatability and higher yield can be obtained with the use of PTAS seeds in synthesis, we observed that PTAS-seeded flakes contain particle impurities. Moreover, devices from PTAS-seeded $MoSe_2$ flakes consistently displayed poorer field-effect mobility, current on-off ratio, and subthreshold swing as compared to unseeded flakes. © *2014 AIP Publishing LLC*.
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Research interests on 2D layered materials from the family of transition metal dichalcogenides (e.g., WSe_2, $MoSe_2$, and particularly MoS_2) were reignited in early 2010 due to the discovery of emerging phenomena at samples with thickness down to monolayer level. This includes emerging photoluminescence via indirect-to-direct bandgap transition[1,2] and valley polarization.[3–5] The existence of bandgap on the semiconducting member of these materials also allows potential uses in low power electronics[6,7] and logic circuits[8,9] to complement silicon-based technology. However, reliable and scalable production and processing protocols have to be established prior to the realization of marketable applications from layered materials, especially on aspects including synthesis, patterning,[10] thinning,[11–13] etching,[14] and contact engineering.[15–17]

On the synthesis front, chemical vapor deposition (CVD) by sulfidation/selenization of molybdenum/tungsten trioxide are most popular due to the high sample quality and throughput relative to other methods.[18] The use of molecular seeds was also suggested to catalyze the CVD synthesis, allowing larger growth area and domain size while retaining good crystallinity of the sample.[18–20] Among the most commonly used seed catalyst is perylene-3,4,9,10-tetracarboxylic acid tetrapotassium salt (PTAS, see Fig. 1(a); EDX of PTAS is available in supplementary material Fig. S1).[21] Nevertheless, the influence of catalyst seeds such as PTAS on the electrical properties of as-grown 2D layered materials is still unclear. Thus, it is imperative to understand the implications of seeding use before the protocol is implemented in the production of large scale electronics from layered materials.

We investigate herein the effect of PTAS-seeding on the electrical properties of $MoSe_2$ flakes as a case study. The flakes were synthesized by a vapor transport CVD method following previous works[22–24] (see supplementary material Fig. S2).[21] Si chips with 285 nm SiO_2 were used as the substrates; one substrate was used per synthesis and was placed upside-down on a crucible containing MoO_3 powder. The substrates were pre-cleaned (ultrasonication in acetone, UV-ozone, and piranha cleaning) and either (i) used as-is in the synthesis, or (ii) drop-casted with PTAS solution in deionized water (50 μM, 2D semiconductors) for 30 min, dried with N_2 flow, and heated atop hotplate at 50 °C. Identical synthesis parameters were used for both unseeded and PTAS-seeded substrate. Field-effect transistors (FETs) were fabricated with electron-beam lithography and 50 nm Ni, deposited by thermal evaporation, is used as the electrodes. All devices were measured with probe station at 300 K and pressure $<10^{-5}$ mbar. Prior to electrical measurements, the devices were vacuum annealed at 373 K for 2 h to reduce hysteresis.[25] Field-effect mobility is calculated by $\mu_{FET} = (dI_{ds}/dV_g) \times L/(WC_{ox}V_{ds})$, where dI_{ds}/dV_g is transconductance, L/W is the channel length-to-width ratio, $C_{ox} = 1.21 \times 10^{-8}\,\mathrm{F\,cm^{-2}}$ is the gate oxide capacitance, and V_{ds} is the bias voltage.

To understand how PTAS pre-seeding may affect the substrate prior to the synthesis, we conducted atomic force microscopy (AFM) on SiO_2 substrate without and with PTAS seed catalyst dispersion (Figs. 1(b) and 1(c)). We observed that the application of PTAS catalyst induces formation of particle aggregates on the substrate, in agreement to previous reports.[19,20] The particles have an average diameter of 65 ± 9 nm. It was noted that such PTAS particles may remain on the substrate after the growth of MoS_2 nanoflakes (i.e., the particles may withstand >650 °C temperature during synthesis) and even after the removal of the flakes.[19] These PTAS particles were hypothesized to act as the preferential nucleation site for the growth of flakes, hence acting as the "catalyst" of the synthesis.

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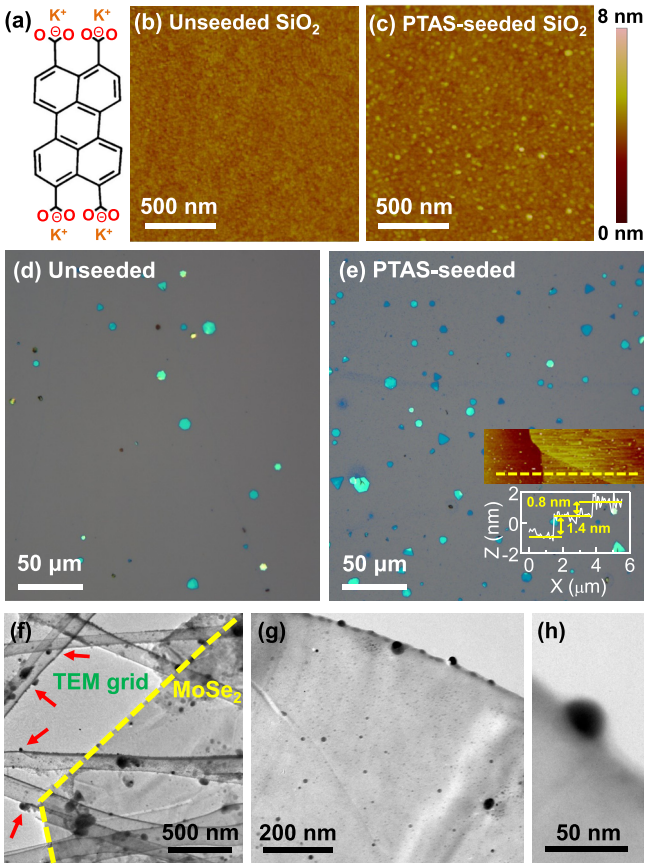

FIG. 1. CVD synthesis of $MoSe_2$ with and without PTAS seed catalyst. (a) Structural formula of PTAS. (b) and (c) are the AFM images of a fresh 285 nm SiO_2 substrate without and with the dispersion of 50 μM PTAS solution, respectively. PTAS seeds are deposited on the substrate as particles with the size of tens of nanometer. (d) and (e) are typical low-magnification optical micrographs of $MoSe_2$ sample synthesized without pre-seeding and with PTAS-seeding, respectively. The use of PTAS aids the repeatability and yield of thin $MoSe_2$ nanoflakes. Inset: AFM image of a flake with bi- and trilayer region. Thickness profile along the yellow dashed line is also shown. (f)–(h) TEM images of PTAS-seeded $MoSe_2$ nanoflakes at various magnifications. Spherical particles were seen on both the nanoflakes and the TEM grid (red arrows in (f)).

Figs. 1(d) and 1(e) show that $MoSe_2$ flakes can be synthesized with and without PTAS-seeding. Isolated flakes with varying thickness were observed, as indicated by the color-contrast of the flakes, ranging from thick (>8 layers, bright blue) and few-layered flakes (dark blue). We use the color-contrast to distinguish the layer number, similar to previous reports[11,26] (supplementary material Fig. S3).[21] Here we notice a benefit of PTAS seeds: pre-seeding improves the yield of few-layered flakes. Moreover, we also notice that the use of PTAS allows higher reproducibility of the synthesis of few-layered flakes. Otherwise, no striking structural differences were identified from the unseeded and the PTAS-seeded flakes via optical microscope.

To study the effect of those PTAS particles on the structure of $MoSe_2$ flakes, we transferred the sample onto a lacey carbon grid for transmission electron microscopy (TEM) as in a previous report.[23] Figs. 1(f)–1(h) show that the flakes contain spherical particles whose sizes are also in tens of nanometer range (40 ± 25 nm; see supplementary material Fig. S4),[21] similar to that of the PTAS particles on the substrate. Furthermore, we also see that the particles also exist on the TEM grid, suggesting that these particles had existed on the substrate separate from the $MoSe_2$ flakes. Thus, it is very likely that these particles correspond to the PTAS seeds as seen in Fig. 1(e). Conversely, $MoSe_2$ samples produced without PTAS seeding did not acquire such particles.[23]

We remark that the attachment of the catalyst particles on 2D layered materials has a precedence in nanowires and nanobelts. Nanowires can also be considered as a low-dimensional nanostructure (i.e., quasi-1D) due to their small diameter of $\leq$100 nm and unconstrained length. Similar to 2D materials, nanowires from semiconductor materials (e.g., group IV elements and II-VI compounds such as ZnO) can be grown from vapor phase synthesis by using catalyst particles via a vapor-liquid-solid (VLS) mechanism.[27] While the details of the VLS mechanism and the 2D material growth are different, the catalyst in both cases has the role of preferential nucleation site and acts as the starting point of the material crystallization.[28] Consequently, catalyst particle often remained at the tip of a nanowire structure after the synthesis in VLS mechanism. However, unlike the case in 2D materials, catalyst in VLS growth has been reported to influence the electrical properties of nanowires. For instance, catalyst particle may diffuse into the structure of the nanowires as an impurity[29,30] and affect the electrical properties of the sample as a dopant[31] and introduce deep-level electronic state.[32]

Fig. 2(a) exemplifies the transfer curves of FETs from the unseeded and the PTAS-seeded $MoSe_2$ bilayer flakes. The unseeded flakes generally outperformed the PTAS-seeded flakes in terms of on-off ratio and subthreshold swing. The low on-off ratio on the seeded flakes was not only due to relatively lower on-state current; in some devices, we also observed a high subthreshold leakage at the off-state ($\sim$nA, dashed black curve).

Figs. 2(b)–2(d) further contrast the FET device performance between the unseeded and the PTAS-seeded $MoSe_2$ flakes in terms of field-effect mobility, on-off ratio, and subthreshold swing. The measurements were performed on 178 devices from multiple synthesis batches to demonstrate that the observed phenomenon is statistically significant. The data are grouped according to the layer number to eliminate any dependence of the electrical properties on sample thickness. Here, we see that the unseeded $MoSe_2$ FETs consistently performed better: higher mobility, higher on-off ratio, and lower subthreshold swing. The unseeded bilayer flakes most commonly has mobility within 0.1–10 $cm^2V^{-1}s^{-1}$ range. Increasing trend of the average and median of mobility with respect to the layer number are also observable, in agreement with previous works on MoS_2.[15,33] In contrast, the mobility of the PTAS-seeded $MoSe_2$ from our synthesis are mostly <1 $cm^2V^{-1}s^{-1}$ for the layer numbers of 2–5.

We hypothesize here possible reasons on how PTAS-seeding could have influenced negatively on the device properties of $MoSe_2$ FETs. First, from Figs. 1(b) and 2(c), the presence of PTAS particle aggregates in itself may be considered as an impurity on the substrate. When the flakes were synthesized, the impurity on the substrate-flakes interface will act as additional Coulomb scattering center.[33] In addition, the incorporation of the particles on the flake structure (Figs. 1(f)–1(h)) will also interfere with the charge

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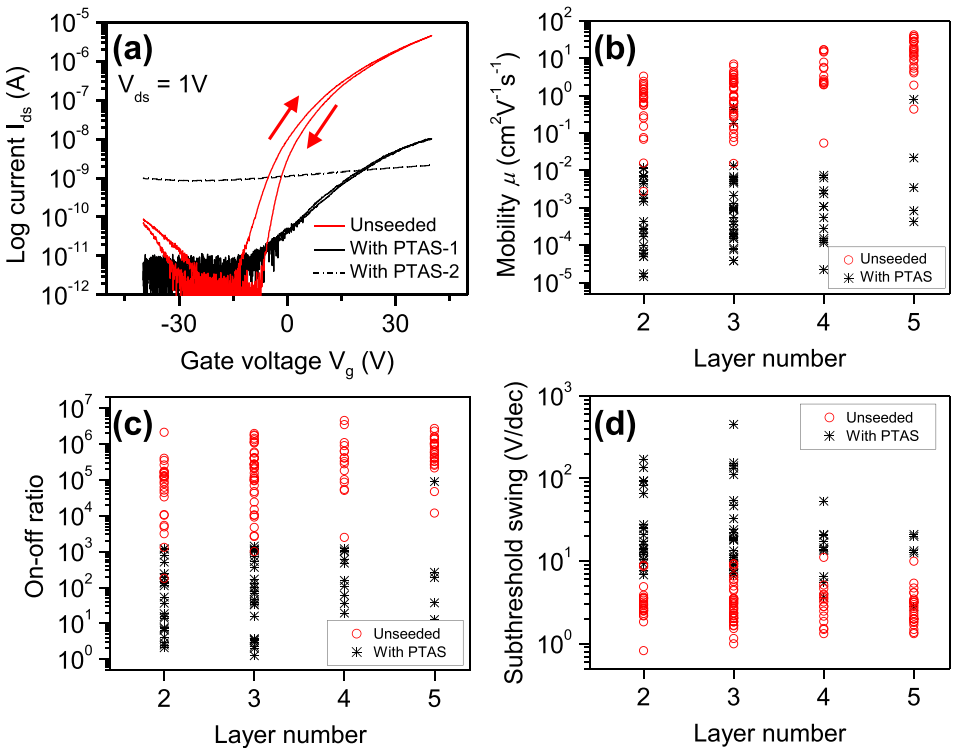

FIG. 2. Comparison between electrical performance of unseeded and PTAS-seeded $MoSe_2$ FETs. (a) I_{ds} vs V_g curves of representatives from the unseeded and the PTAS-seeded bilayer $MoSe_2$. Red arrows denote the direction of the hysteresis. PTAS-seeded $MoSe_2$ not only has lower on-off current ratio, but higher off-current level as well. The electrical performance of the unseeded $MoSe_2$ FET to that synthesized with PTAS seeding is compared in terms of (b) mobility, (c) on-off ratio, and (d) subthreshold swing. In all these parameters, the unseeded $MoSe_2$ exhibited superior performances.

transport on the sample by increasing the scattering rate. These two factors may accumulate to diminish the carrier mobility and the conductivity (thus reducing the on-state current) of seeded $MoSe_2$ devices.

The large subthreshold swing in PTAS-seeded flakes also suggests that the impurity due to PTAS may also contribute to the interface trap density at the substrate-flakes interface. Moreover, the incorporation of PTAS seeds into the $MoSe_2$ flake after the synthesis could create new localized defect states within the bandgap of the $MoSe_2$ devices, analogous to the situation in nanowires as alluded to previously. For an n-type device such as $MoSe_2$, the defect states may still contribute in the conductivity of the device channel even though the gate bias has been applied to a large negative voltage (~ -40 V), causing a high subthreshold/off-state current for some devices.

Our finding implies that synthesis of 2D layered materials without pre-seeding, whenever applicable, is preferred for electrical transport studies and applications in electronics. As an example, we display in Fig. 3 the measurements results from an FET of 5 layered $MoSe_2$ flake. The FET exhibited n-type behavior with a high mobility of $43\,cm^2V^{-1}s^{-1}$ (Fig. 3(a)) and 10^6 on-off ratio at room temperature, with a very small hysteresis during the gate sweep (Fig. 3(b)). The output

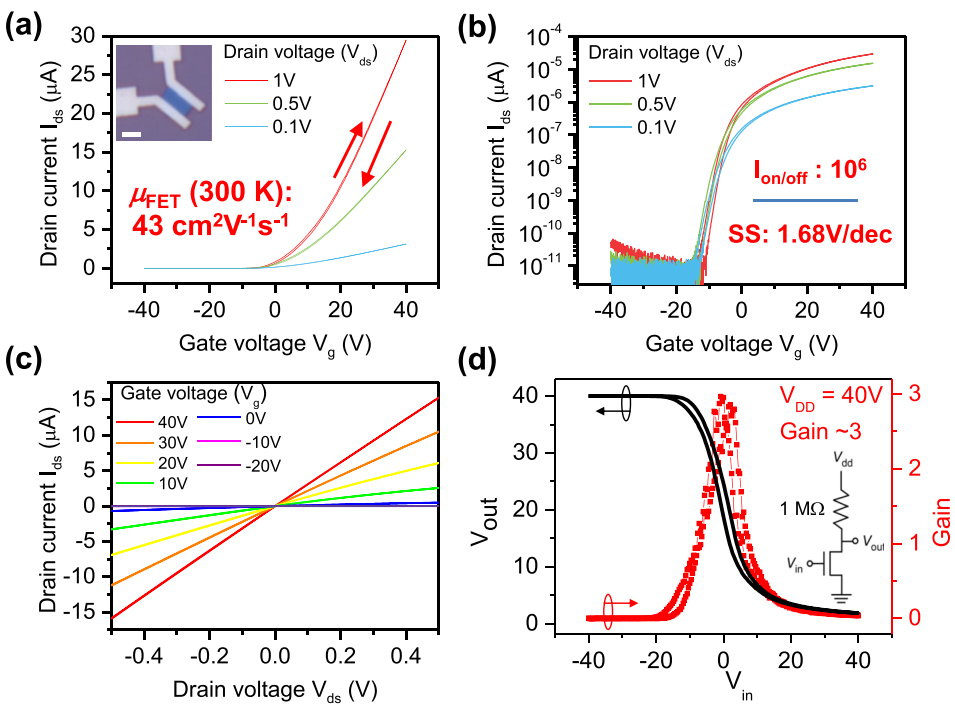

FIG. 3. Electrical characterizations of the unseeded few-layered $MoSe_2$ device. (a) Transfer curves of an unseeded $MoSe_2$ FET. Inset: Optical image of the measured device. Scale bar is 1 μm. (b) Transfer curves of the device in semilog scale. (c) Output curves of the devices. The highly liner curves is due to quasi-ohmic contact within the sample. (d) Inverter applications of the device, with a single FET device structure. Gain of $\sim$3 can be achieved from the unseeded $MoSe_2$.

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curves are linear in Ohmic-like fashion (Fig. 3(c)). The good electrical properties suggest that the unseeded sample may be suitable for implementation in electronic logic circuitry. Consequently, we also show an inverter (NOT gate) application from the unseeded flakes. We could achieve a gain $= -dV_{out}/dV_{in} \approx 3$, where a gain of larger than unity means that the output voltage can be used to drive subsequent inverter elements.

In conclusion, we found that while PTAS seeding improves the yield and repeatability of producing thin $MoSe_2$ flakes, the PTAS-seeded $MoSe_2$ FETs generally performed poorly when compared to the unseeded $MoSe_2$ FETs. This indicates that the electrical performance of the 2D layered materials is compromised with the use of catalyst seeding. However, PTAS seeding might still be favorable for applications where the transport properties are not critical, such as in spectroscopy studies (no significant differences were observed in Raman spectra of seeded and PTAS-seeded flakes[21]). Additionally, the use of seeding may also be adopted for applications if there are major improvements in terms of as-grown sample morphology, domain size, and overall crystalline quality as compared to the unseeded sample, as previously reported in MoS_2.[18,20] On the other hand, considering the immense advantage of pre-seeding in improving the synthesis yield, we believe that it is worthwhile to search for seed catalyst with minimum repercussion on the properties of the material. For instance, one might envision for inspiration from 1D nanowires where self-catalytic synthesis can be performed with catalyst species containing compounds from the material-of-interest from the nanowire, thus circumventing the issues of contamination.[34]

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