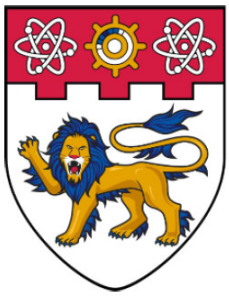

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CONTROL AND OPERATION OF MMCS YANG SHUNFENG 2017

CONTROL AND OPERATION OF MODULAR MULTILEVEL CONVERTERS

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CONTROL AND OPERATION OF MODULAR MULTILEVEL CONVERTERS

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Abstract

The increasing trend of electrical power demands in megacities, industries, and transportation requires medium- or high-voltage power electronics devices to serve as the enabling components for high power conversion, due to design flexibility, better dynamic performance, energy efficiency, and environment friendliness. Multilevel power converters, such as Neutral Point Clamped (NPC) Converters, Cascaded H-Bridge (CHB) Converters, and Modular Multilevel Converters (MMCs), are popular commercialized candidates for such high power applications. Among them, the MMC possesses great performance in terms of functionality, hardware implementation, configuration complexity, output power quality, efficiency, and reliability. It shows considerable research potential in the academic world as well. This thesis aims to investigate the control and operation strategies that related to the control performance, efficiency, nonlinearity, modularity, and reliability of MMCs.

At first, the configuration and operation principles of a three phase MMC is introduced. A comprehensive steady state analysis and the equivalent circuit model, which are applicable to an MMC connected to either a DC or an AC bus, are then presented in this thesis. In addition to better understanding of the MMC operation, the analysis and modeling of the MMC also suggest the conditions that ensure the stability operation of the MMC system. According to the aforementioned analysis and modeling, the control system of the MMC is introduced. The commonly used cascaded control strategy, including output and inner dynamics control loops, has been discussed. The existing modulation methods for MMCs have been summarized, and the phase-shifted pulse width modulation (PS-PWM) are detailed and adopted in this thesis.

The circulating current harmonics in each phase are expected to be suppressed in order to improve the performance and reduce the losses of MMCs. The characteristics of the circulating current harmonics are analyzed and it is revealed

that the circulating current are dominated by even order harmonics. An even-harmonic repetitive control scheme is proposed to eliminate the even harmonics in the differential current. The proposed repetitive controller has excellent harmonic elimination, with benefits of less memory occupation, less delay period, doubled low frequency gain, faster convergence rate and dynamic response, and wider bandwidth at specific frequencies. The full design details of the even-harmonic repetitive control for an MMC system has been presented.

Moreover, the MMC is a multi-input multi-output bilinear system. A non-linear control strategy is preferred for better control performance. The feedback linearization based current control for the MMC is proposed in this thesis to solve the bilinear control problem. The state function model of the MMC is linearized with the help of the feedback linearization technique. The output and inner differential current control loops are decoupled as two independent simple integrators. Classical linear control laws can be easily applied in the two current control loops. The control performance in steady state and during step changes is improved and the controller design process is facilitated.

The centralized control system will reduce the modularity of the MMC in terms of software implementation. And it is not practical in MMC systems with a large number of sub-modules. A distributed control strategy for MMCs is proposed in this thesis. The proposed control strategy is able to achieve all control objectives in conventional control strategies, with significantly reduced data exchanging among central and local controllers through a communication network.

The fault diagnosis and fault tolerant control for an MMC with redundant sub-modules significantly increases the system reliability. A real-time measurement based semiconductor device open-circuit fault diagnosis method has been proposed. This fault diagnosis is implemented in each local controller in the distributed control architecture with local information. It is capable of accurately identifying multiple faults within 3.5 ms without false alarm. Based on the performance analysis of an MMC with bypassed faulty sub-modules, a fault tolerant control is accordingly proposed. The fault tolerant control guarantees the performance of the MMC to be the same as in normal operation. The fault tolerant control can be activated with 5 ms after the fault occurrence. The MMC is able to seamlessly ride through switching device open-circuit faults.

All the theoretical findings are verified in PLECS simulations. The effectiveness and practicalities of the control algorithms are confirmed on a scale down single-phase MMC prototype.

Nomenclature

List of Abbreviation

APOD	Alternative Phase Opposite Disposition
CAN	Controller Area Network
CAN-FD	Controller Area Network with Flexible Data-Rate
CHB	Cascaded H-Bridge
CVCF	Constant Voltage Constant Frequency
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
EtherCAT	Ethernet for Control Automation Technology
FPGA	Field-Programmable Gate Array
GTO	Gate Turn Off
HVDC	High Voltage Direct Current
IGBT	Insulated-Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Transistor
KVL	Kirchhoff's Voltage Law
LS-PWM	Level-Shifted PWM
MIMO	Multi-Input-Multi-Output
MMC	Modular Multilevel Converter
MPC	Model Predictive Control
MTTF	Mean Time To Failure
NPC	Neutral Point Clamped
PD	Phase Disposition
PI	Proportional-Integral
POD	Phase Opposite Disposition
PR	Proportional-Resonant
PS-PWM	Phase-Shifted PWM
PWM	Pulse-Width-Modulation
RC	Repetitive Control
RMS	Root-Mean-Square
SCR	Silicon-Controlled Rectifier
SGCT	Symmetrical Gate Commutated Thyristor

SM	Sub-module
SPWM	Sinusoidal Pulse-Width-Modulation
STATCOM	Static Synchronous Compensator
SVPWM	Space Vector Pulse-Width-Modulation
THD	Total Harmonic Distortion
ZOH	Zero-Order-Hold

List of Acronym

C_{DC}	DC-link capacitance.
C_{SM}	Sub-module capacitance.
D_k	The k^{th} diode in a sub-module.
f/ω	Frequency/Angular frequency.
f_c	Carrier frequency.
f_{cross}	Crossover frequency.
f_d	Frequency deviation.
f_n	Nature frequency.
f_o/ω_o	Frequency/Angular frequency of output voltage.
f_s/T_s	Sampling frequency/period.
$i_{arm,max}$	Maximum arm current.
i_{cirx}	Circulating current in phase leg x ($x \in (a,b,c)$).
i_{cirxk}	The k^{th} order circulating current in phase leg x ($x \in (a,b,c)$).
I_{cirxk}	Amplitude of the k^{th} order circulating current in phase leg x ($x \in (a,b,c)$).
$i_{Cuxk/Clxk}$	Capacitor current of the k^{th} sub-module in the upper/lower arm of phase x ($x \in (a,b,c)$).
$\tilde{i}_{Cux/Clx}$	Ripples of the capacitor currents in the upper/lower arm in phase x ($x \in (a,b,c)$).
I_{DC}	DC input current.
i_{diffx}	Inner differential current in phase x ($x \in (a,b,c)$).
${i_{diffx}}^*$	Inner differential current reference of phase x ($x \in (a,b,c)$).
$i_{diffx,err}$	Differential current tracking error.
${i_{diffx,DC}}^*$	A DC component of ${i_{diffx}}^*$ for active power balance in phase x ($x \in (a,b,c)$).
${i_{diffx,pb}}^*$	One component of ${i_{diffx}}^*$ having the same frequency and phase angle with u_s for active power balance.
${i_{diffx,va}}^*$	One component of ${i_{diffx}}^*$ for capacitor average voltage control.
${i_{diffx,vd}}^*$	One component of ${i_{diffx}}^*$ for arm difference voltage control.
i_o	Output current.
${i_o}^*$	Output current reference.
I_o	Amplitude of output current.
$I_{o,max}$	Maximum output current.
i_s	Common bus (input) current.
I_s	Amplitude of the common bus current.
$I_{s,max}$	Maximum common bus current.
i_{SM}	Sub-module current.
$i_{ux/lx}$	Upper/lower arm current in phase x ($x \in (a,b,c)$).
i_x	Output current of phase x ($x \in (a,b,c)$).
J_n	Bessel function.

K_b	Proportional gain for capacitor voltage balancing control.
K_i	Integral gain of a PI controller.
K_p	Proportional gain of a PI controller.
K_r	Repetitive control gain; Resonant control gain.
L_{arm}	Arm inductance.
$L_{arm,r}$	Arm inductance that leads to current resonance.
L_l	Load inductance.
L_o	Output filter inductance.
m_o	Modulation index
$n_{ux/lx}$	Upper/lower arm insert indices in phase x ($x \in (a, b, c)$).
N	Number of sub-module in each arm.
N_{by}	Number of bypassed sub-modules.
N_{eq}	Equivalent number of sub-modules inserted into the phase leg.
N_f	Number of faulty sub-modules.
N_r	Number of redundant sub-modules.
N_s	Number of samples in one repetitive period.
$N_{ux/lx}$	Number of sub-module inserted in the upper/lower arm in phase x ($x \in (a, b, c)$).
$P_{Cuk/Clk}$	Power flows through the k^{th} capacitor in the upper/lower arm.
$\bar{P}_{Cuk/Clk}$	Average power flows through the k^{th} capacitor in the upper/lower arm.
R_{arm}	Arm equivalent resistance.
R_l	Load resistance.
S_k	The k^{th} switching device in a sub-module.
$SM_{uk/lk}$	The k^{th} sub-module in the upper/lower arm.
$s_{ux/lx}$	Sum of switching functions in the upper/lower arm in phase x ($x \in (a, b, c)$).
$s_{uxk/lxk}$	Switching functions of the k^{th} sub-module in the upper/lower arm in phase x ($x \in (a, b, c)$).
s_{xo}	Switching function of the MMC output.
$s_{x,leg}$	Switching function of the inserted sub-modules in phase x ($x \in (a, b, c)$).
U_{arm}	Total DC voltage of each arm.
${u_{buxk/blxk}}^*$	Reference for capacitor voltage balancing control in the k^{th} sub-module in the upper/lower arm in phase x ($x \in (a, b, c)$).
${U_{buxk/blxk}}^*$	Amplitude of ${u_{buxk/blxk}}^*$.
u_c	Sub-module capacitor voltage.
U_C	Average voltage across a sub-module capacitor.
${u_C}^*$	Capacitor voltage reference.
$u_{Cux/Clx}$	Voltage across the capacitors in the upper/lower arm in phase $x(x \in (a, b, c))$.

$\bar{u}_{Cux/Clx}$	Average voltage across the capacitors in the upper/lower arm in phase $x(x \in (a,b,c))$.
$u_{Cuxk/Clxk}$	Capacitor voltage of the k^{th} sub-module in the upper/lower arm of phase x $(x \in (a,b,c))$.
$U_{C,rpl}$	Capacitor voltage ripples.
U_{Ck}	Amplitude of the k^{th} order capacitor voltage ripple.
u_{diffx}	Differential voltage for i_{diffx} regulation in phase x $(x \in (a,b,c))$.
$u_{diffx}{}^*$	Differential voltage reference for i_{diffx} regulation in phase x $(x \in (a,b,c))$.
$u_{diffuxk/difflxk}{}^*$	Differential voltage reference for the k^{th} sub-module in the upper/lower arm in phase x $(x \in (a,b,c))$.
$U_{diff,DC}$	DC component of u_{diffx}.
$\tilde{u}_{diffx}$	AC components in u_{diffx}.
$\tilde{U}_{diffxk}$	Amplitude the k^{th} order component of $\tilde{u}_{diffx}$.
U_{DC}	DC bus voltage.
u_{load}	Load voltage.
u_{misx}	Mismatch between the inserted phase voltage and common bus voltage in phase x $(x \in (a,b,c))$.
u_s	Common bus (input) voltage.
U_s	Amplitude of the common bus voltage.
u_{SM}	Sub-module voltage.
$u_{SMuxk/SMlxk}$	Output voltage of the k^{th} sub-module in the upper/lower arm of phase x $(x \in (a,b,c))$.
$u_{ux/lx}$	Inserted voltage of the upper/lower arm in phase x $(x \in (a,b,c))$.
$u_{ux/lx}{}^*$	Voltage reference for the upper/lower arm in phase x $(x \in (a,b,c))$.
$u_{uxk/lxk}{}^*$	Voltage reference for the k^{th} sub-module in the upper/lower arm in phase x $(x \in (a,b,c))$.
u_{phx}	Inserted voltage of phase x $(x \in (a,b,c))$.
u_{xo}	Output voltage of phase x $(x \in (a,b,c))$.
$u_{xo}{}^*$	Output voltage reference for phase x $(x \in (a,b,c))$.
U_o	Amplitude of the phase (output) voltage.
$U_{o,max}$	Maximum amplitude of the phase (output) voltage.
$u_{x\_harm\_com}$	Common-mode voltage ripples in the upper and lower arms in phase x $(x \in (a,b,c))$.
$u_{x\_harm\_diff}$	Differential-mode voltage ripples in the upper and lower arms in phase x $(x \in (a,b,c))$.
v_{crk}	Carrier waveform of sub-module k.
α	Phase displacement between the carrier waves and the modulating signal.

β	Angle displacement between the carriers in the upper and lower arms.
ϕ_b	Phase angle of the reference for capacitor voltage balancing control.
ϕ_{cirxk}	Phase angle of the k^{th} order circulating current in phase leg x ($x \in (a, b, c)$).
ϕ_{cr}	Phase shift between two adjacent carriers.
ϕ_{Ck}	Phase angle of the k^{th} order capacitor voltage ripple.
ϕ_{diffxk}	Phase angle of the k^{th} order component of u_{diffx}.
ϕ_{i_o}	Phase displacement between the output voltage and current.
ϕ_s	Phase displacement between the common bus voltage and current.
ϕ_{uxk}	Phase angle of the k^{th} order component of $\tilde{u}_{diffx}$.
θ_{ox}	Initial phase angle of output phase voltages ($x \in (a, b, c)$) ($\theta_{ox} = \phi_o + \phi_x$).
ω_c	Angular frequency of the triangular carrier.
ω_{cf}	Cut-off frequency; Resonant cut-off frequency.
ω_{cirxk}	Angular frequency of the k^{th} order circulating current in phase leg x ($x \in (a, b, c)$).
ω_p	A particular frequency for repetitive control stability check.
ω_{rk}	The k^{th} resonant frequency of the circulating current.
ω_s	Angular frequency of common bus voltage.

Chapter 1

Introduction

1.1 Background and motivation

The electric power demands for megacities, industrial centers, and electric transportation are increasing rapidly, which results in high- or medium voltage levels in power transmission and power conversion applications, such as High Voltage Direct Current (HVDC) transmission and Medium Voltage Motor Drives, for boosted power efficiency and reduced overall costs.

HVDC transmissions, whose voltage level can be up to ±1100 kV, have been developed for a few decades in long-distance large-scale electric power transmission, because of their great power transfer capacity and higher efficiency over transitional AC transmission. In the last decade, the voltage source converter (VSC) based flexible HVDC transmission techniques have been developed because they are suitable candidates for linking remote renewable power plants, such as offshore wind farms or solar power plants in deserts, to the main power grid [2]. Many HVDC transmission lines have been installed or are developing in European countries and China. China has the highest demands for high voltage transmission due to its large area and unbalanced geographic distribution of electric power generation and demands among different areas.

With the advancement in technology, the introduction of all-electric ship or high-speed train is expected to gradually take the advantages of electric propulsion/traction mechanisms [3–5]. The electric propulsion/traction system has the most significant influence on ship/train performance and cost-effectiveness. The increasing trend of electrical propulsion/traction system raises the demand of higher power electric motor drive connecting to distribution systems with rel-

atively high voltage. Not only do the power electronics based electric drives help to improve the dynamic performance, but they also offer features like design flexibility, higher energy efficiency, environment friendliness and reduced space requirement. Many worldwide famous manufacturers and suppliers such as ABB [6], Rockwell [7], General Electric [8], and Siemens [9] have released medium-voltage (3.3 kV to 11 kV) motor drive products for different industrial applications within a power range of 3 MVA to 36 MVA.

In aforementioned high- and medium-voltage applications, the power electronics with fully controlled semiconductor devices is regarded as the key enabling technology that makes the VSC-HVDC transmission and medium voltage motor drives available. Multilevel converters, which are able to offer improved power quality, higher efficiency and reliability, and lower dv/dt rate that dramatically reduces common mode current and electromagnetic interference (EMI) problems [10], are the promising candidates for those applications. Maturely developed multilevel topologies such as Neutral Point Clamped (NPC) multilevel inverters [11, 12], Flying Capacitor Clamped converters [13, 14], and Cascaded H-Bridge (CHB) converters [15, 16] were introduced since 1970s. A promising multilevel converter topology, namely Modular Multilevel Converter (MMC), was introduced by German researchers in [17] in 2003.

Selected topologies, including H-bridge NPC, 5-level active NPC, CHB, and MMC, are briefly evaluated in a medium voltage drive application (6.6 kV 7 MW) for a comprehensive comparison among those topologies. The evaluation in terms of components count, switching frequency, losses, efficiency, harmonics, modularity, and the complexity of implementation, is summarized in Table 1.1.

Components count: Although the component count of CHB and MMC are much higher than that of topologies based on NPC, most components adopted in CHB and MMC are low voltage ones with much lower price and significantly reduced size. However, the total size of CHB and MMC is still larger than that of NPC converters.

Operation range extensibility: NPC based converters are limited by the voltage capability of the semiconductor devices. Commercialized high voltage Insulated-Gate Bipolar Transistor (IGBT) devices are currently manufactured to a rating of 4.5 kV which enables 5L-NPC converters to be constructed to 6.6 kV or 4.16 kV (without the use of devices in series). In contrast, CHB and MMC designs are not limited by the voltage ratings of switching devices. Such designs take full advantage of the benefits that are achievable through high voltage conversion.

Table 1.1: Multilevel converter topologies evaluation.

Topology	**Switch voltage rating**	**Voltage stress on switch**	**No. of switches**	**No. of capacitors**	**No. of clamping diode**
HB-NPC	4.5 kV	2.7 kV	24	6	12
5L-NPC	4.5 kV	2.7 kV	24	5	0
CHB	1.7 kV	0.9 kV	72	18	0
MMC	1.7 kV	1.08 kV	120	60	0
Total device count	**Switching frequency**	**Output voltage level**	**Switching losses**	**Conduct losses**	**Efficiency**
42	0.9 kHz	5	High	Low	99%
29	0.9 kHz	5	Medium	Low	99%
90	0.6 kHz	13	Very Low	Medium	$> 99\%$
180	0.36 kHz	21	Very Low	Medium	$> 99\%$
THD in output current	**Control complexity**	**Reliability**	**Modularity**	**Transformer**	**Easy to be extended**
4%	Medium	Low	No	No	Low
5%	Medium	Low	No	No	Low
0.7%	Medium	High	Yes	Yes	Medium
0.6%	High	High	Yes	No	High

Converters of 6.6 kV, 11 kV and even higher voltage ratings ($\pm$800 kV) are achievable. Because of their modularity, the output voltage level of the CHB and MMC based converters can be easily changed by simply adding or removing sub-modules or power cells.

Electrical connection: The NPC based topologies and the MMC are all suitable for use in common bus systems while the CHB based topology requires a complicated phase-shifted multi-winding transformer to provide an isolated voltage source to each power cell. This high power transformer will not only increase the cost and size of the converter, but also influence the flexibility while expending the operation voltage and power range as well as the system reliability.

Efficiency and output power quality: The NPC, CHB and MMC topologies each exhibit high efficiency approaching 99% at full loads. Conduction losses dominant within the CHB and MMC topologies while switching losses are dominant in the NPC based topologies. The high equivalent switching frequency and output voltage levels for the CHB and MMC yield an output current with low

harmonics. Output filters are generally not required. CHB and MMC also exhibit low dv/dt with resultant reduction in EMI and common mode circulation. The NPC in contrast does not exhibit high 'effective switching frequency'. The first harmonic band is lower and output harmonics are less effectively attenuated. Either the switching frequency has to be increased (resulting in higher switching loss) or external bulky filters are required.

Reliability: The NPC based topologies have relatively low part counts. When evaluated according to the 'Parts-Count' method, the mean time to failure (MTTF) for these topologies is high. Reliability, however, is preferably calculated by the 'Part-Stress' method that takes into consideration the temperature and operating environment of the components. Adequate design margins are essential for reliable design and such design margins are readily provided for in CHB and MMC designs. Such possibility is not available with NPC designs which push the voltage ratings of the devices. Furthermore, conduction and switching losses are concentrated at a relatively few number of devices in NPC converters, which places a great burden on the cooling system and operation temperature tends to be high. In contrast, the CHB and MMC topologies may be designed with robust design margins. Conduction and switching losses are generated evenly at multiple devices. The burden of cooling is reduced, which in turn reduces thermal stress on devices. The CHB topology moreover offers a high degree of redundancy. Redundancy may be added to the MMC topology with the additional redundant modules. The two topologies will continue to operate even if less modules within a phase leg remains operational. Operation with an unbalanced number of modules per phase is also possible with little degradation in performance. The redundancy of CHB and MMC increase the reliability of these topologies significantly. The cost to add such modules is marginal. In contrast, the NPC does not possess natural redundancy. Redundancy may be added through additional stacks in parallel, however, the cost of doing so is prohibitive.

In all, the advantages, such as modularity, flexible scalability, ability to handle high power with relatively low voltage rating semiconductors, capacitor energy distribution, filter-less configuration, redundancy, and grid connection via standard transformer or transformerless, make the MMC one of the most popular multilevel topologies in recent years, with respect to today's technology, in medium and high voltage applications and patents [18–20]. The MMC topology has been deemed as a perfect candidate for HVDC transmission applications [2]. The utilization of MMCs in ship propulsion systems [21, 22] and railway systems [5, 23–27] is pos-

sible as well. Commercial products based on MMC from Siemens, Alstom, and ABB has been applied in industrial applications in recent years such as HVDC transmission [28, 29], static synchronous compensator (STATCOM) [30], battery energy storage [20], static frequency converters [31], and medium voltage motor drives [32, 33].

However, the MMC topology is still relatively new to the market and a knowledge gap has been left between the engineering development and the academic interests. It is likely to be a great opportunity to improve upon existing commercial products, technologies, and strategies particularly in the area of control.

- Besides the system outputs, the internal dynamics of the MMC including the differential current and capacitor voltages have to be properly managed as well to ensure the stable operation of the MMC. The circulating current ripples in the differential current in each phase leg have to be suppressed for improved efficiency and control performance.

- An MMC is a nonlinear multi-input multi-output system with coupled system state variables and inputs. An advanced nonlinear control strategy is expected for better output quality and faster response.

- The control system of an MMC with a large number of sub-modules is normally quite complicated to manage all the capacitor voltages and internal data exchanging through communication network. Besides, in addition to the identical sub-modules that construct the hardware of an MMC, the control system should be modularized as well for more flexible scalabiltiy. Distributed control strategies are expected for more modularized and convenient software implementation.

- Although the redundancy of the MMC improves the system reliability, the fault diagnosis and fault tolerant operation schemes are required to make better use of the redundant sub-modules in different operation scenarios.

With the changeableness to explore, this thesis investigates the control strategies for MMCs relating to the MMC performance, efficiency, nonlinearity, modularity and reliability.

1.2 Major works and contributions

In this thesis, a number of control strategies based on the study of an MMC system are achieved. The major works and contributions of this research are listed as below:

- The MMC configuration and operation principles are introduced. The up-to-date controls and the modulation schemes adopted in MMC systems are reviewed and summarized.
- A general steady state analysis of the MMC systems that adequate for both DC and AC bus connection applications has been originally conducted, and the equivalent circuit models of the MMC have been accordingly presented.
- A scale-down single-phase MMC experimental platform has been developed in the laboratory.
- An even-harmonic repetitive control for circulating current suppression in each phase leg of an MMC has been proposed. The control strategy almost completely suppressed the even-order harmonics in the differential current with improvements such as the halved number of error sampling periods, less chip memory occupation, shorter controller delay period, faster convergence speed, higher low-frequency gain, higher crossover frequency, and wider control bandwidth at desired frequencies, compared with existing repetitive controls. Moreover, in order to improve the overall system performance and stability, an explicit analysis and design of phase lead filters in repetitive controllers has been proposed.
- A feedback linearization based current control for the MMC has been explored. By applying the feedback linearization technique, the nonlinear MMC model can be transferred to a linear one and the current control loops are decoupled to be two simple integrators. The controller for the decoupled current loops can be easily designed following classic linear control laws. Better steady-state performance and dynamic response of the MMC system can be achieved with the presence of the feedback linearization control strategy.
- A distributed control has been proposed to improve the modularity of the MMC in terms of digital control system implementation. Control tasks are

allocated to a central controller and local controllers in sub-modules. With the carefully designed control loops, data exchanging among different controllers can be significantly reduced while all control objectives can still be met. The data exchanging for real-time control is independent of the number of sub-modules in each arm, which greatly reduces the communication burden in an MMC with a large number of sub-modules.

- A switching device open-circuit fault diagnosis and fault tolerant control is proposed to improve the reliability of MMCs with redundant sub-modules. The fault diagnosis is implemented in each local controller and can accurately identify multiple device open-circuit faults within 3.5 ms. The fault tolerant control can take effect within 5 ms after a fault occurrence. The MMC can seamlessly ride through switching device open-circuit faults without severe malfunction or secondary damages.

1.3 Organization of the thesis

This thesis consists of eight chapters organized as follows:

Chapter 1 introduces the background and motivation of this work.

Chapter 2 presents the basic configuration and operation principles of a three-phase MMC. The voltage and current quantities for the three-phase MMC are defined in this chapter. The main circuit component selection is briefly discussed in this chapter as well.

Chapter 3 provides a general steady-state analysis and equivalent circuits for an MMC that can be connected to either a DC or an AC common bus. Then, the control objectives and basic control loops required in an MMC are introduced based on the analysis. The phase-shift PWM modulation scheme is also detailed to manipulate the switching devices according to the modulation signal.

Chapter 4 proposes an even-harmonic repetitive controller to suppress the even-order circulating current in each phase leg. The full design details are presented according to the characteristics analysis of the circulating current.

Chapter 5 explores a feedback linearization based current control to solve the bilinear control problem of an MMC.

Chapter 6 proposes a distributed control for MMCs with a large number of sub-modules in each arm. The control tasks are allocated to a central controller and local controllers. The control loops are elaborately designed so that the data

exchanging among different controllers is significantly reduced.

Chapter 7 designs a switching device open-circuit fault diagnosis method and a fault tolerant control, which makes the MMC seamlessly riding through such faults.

Chapter 8 concludes the work completed and provides future research recommendations based on the achievements of this thesis.

Chapter 2

Operation Principles of Modular Multilevel Converters

This chapter introduces the basic configuration, structure, and operation of a three-phase Modular Multilevel Converter (MMC). Voltage and current quantities are defined according to the MMC structure for the convenience of mathematical analysis in the following chapters. The criteria for the selection of switching devices, DC-link capacitance, and arm inductance are briefly discussed in this chapter for MMC main circuit design.

2.1 Introduction

The promising multilevel topology modular multilevel converter (MMC) firstly presented in [17] is one of the most attractive topologies in many medium and high voltage AC-to-DC , DC-to-AC and AC-to-AC [34–37] conversion applications such as high voltage DC transmission (HVDC) [38–45], static synchronous compensators (STATCOM) [46–50], medium voltage variable speed motor drives [21, 22, 51–60], and energy storage systems [61–66]. The wide adoption of MMCs in industry is mainly due to its flexible expandability, transformer-less configuration, common DC bus, high reliability from redundancy, and so on. However, MMCs also possess some inherent disadvantages, such as complex overall control strategies, sub-module capacitor voltage unbalance, circulating currents in phase legs, and capacitor voltage fluctuation at low frequency. The advantages and disadvantages of the MMC topology are summarized in Table 2.1.

Table 2.1: Advantages and disadvantages of the MMC topology.

Advantages	**Disadvantages**
Simple mechanical construction comparing to other multilevel topologies	Complex energy control strategies to ensure the stable operation of the MMC
Identical modularized configuration makes it expandable and scalable conveniently for applications with different voltage levels	The capacitor voltages and arm inductor current are coupled that makes the system nonlinear and difficult to be properly controlled
High equivalent switching frequency generated by actual low switching frequencies of individual switching devices	Circulating current mainly consisting of second order harmonic exists in each phase leg due to the voltage mismatch between the common bus and inserted sub-modules
Low switching losses and high efficiency	More losses caused by circulating currents in phase legs
Multilevel output voltage with low Total Harmonic Distortion (THD) and bulky filters at the AC side is not required	The DC and AC powers are exchanged and balanced through the sub-module capacitors, which leads to capacitor voltage fluctuation and unbalance (arm current will go through these capacitors)
Stepwise change in the output voltage reducing the Electromagnetic Interference (EMI)	Monitoring all the capacitor voltages and the arm currents depending on different control strategies
Reduction or even elimination of capacitance in DC-link due to that the energy is stored in the converter's sub-modules	Additional control strategies for the voltage balancing of sub-module capacitors and circulating current elimination
High reliability due to the redundancy of extra modules and utilization of reliable low voltage devices in sub-modules	Unacceptable voltage fluctuation on sub-module capacitors when the MMC is operated at low frequencies
Transformer is not required	-
Suitable for common bus structure	-

2.2 Configuration and basic operation of MMCs

An MMC is a voltage source converter normally comprised by numbers of sub-modules. Each sub-module can operate individually and the MMC can be operated for AC-to-DC, DC-to-AC, and AC-to-AC power convention in single-phase

and multi-phase systems when all these sub-modules work as a whole.

2.2.1 Configuration and operation of the sub-module

Sub-modules (SMs), normally identical, are the fundamental elements of an MMC. Popular topologies of sub-modules reported in literature include the half-bridge sub-module, H-bridge sub-module, clamp double sub-module, 3-level neutral point clamped sub-module, 3-level flying capacitor sub-module, and T-type multilevel sub-module, as illustrated in Figure 2.1. Since the half-bridge based sub-module is adopted for the MMC discussed in this thesis, only this topology will be studied in details in this section.

As shown in Figure 2.1 (a), the half-bridge sub-module consists of two semiconductor devices S_1 and S_2, two anti-parallel diodes D_1 and D_2, and one DC-link capacitor C_{SM}. The average voltage across C_{SM} is denoted as U_C. The output terminals of the half-bridge sub-module are located at the middle point of the two switches and the source of S_2. The output voltage of the sub-module is defined as u_{SM}, and the current flowing through the sub-module is i_{SM}, whose positive direction is indicated as it flows into the sub-module from the middle point between

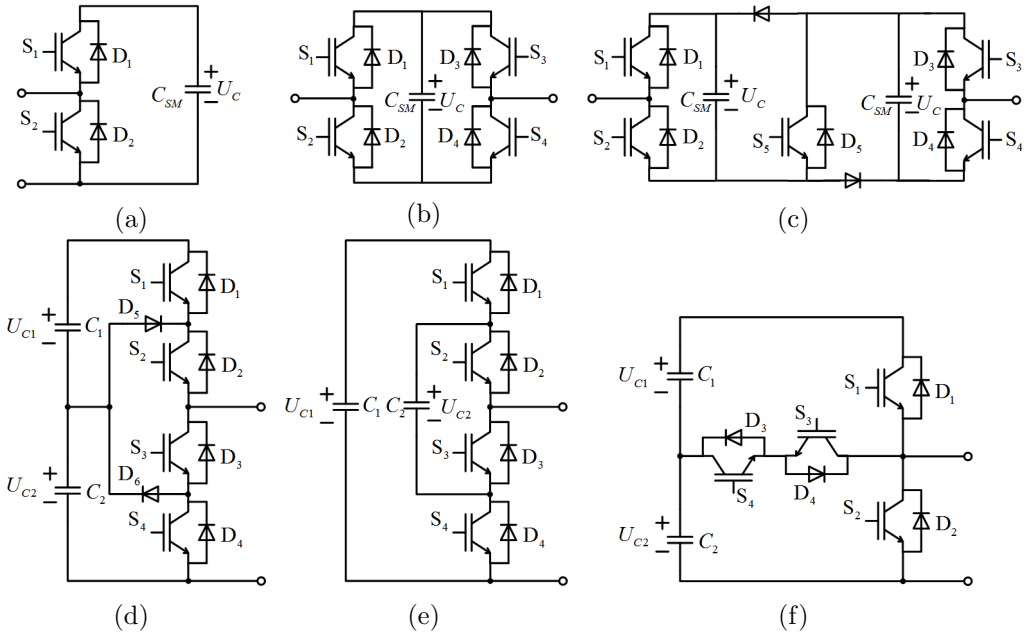


Figure 2.1: Typical sub-modules: (a) half-bridge SM; (b) H-bridge SM; (c) clamp double SM; (d) 3-level NPC SM; (e) 3-level flying capacitor SM; (f) T-type multilevel SM.

S_1 and S_2. These DC-link capacitors are important devices in MMCs' normal operation that provide temporary energy storages for the power transfer from the power source to the loads [67], and vice versa in applications such as regenerative braking.

The operation states of the sub-module depend on the switching patterns of the switches and the direction of i_{SM}. Figure 2.2 shows the six operation states of a sub-module based on the combination of switching functions and current direction. The current paths in the six states are indicated in red in Figure 2.2. In state (a) and (b), S_1 and S_2 are both assigned switch-off signals, and two different operation modes are achieved according to the current direction. As i_{SM} is positive in state (a), D_1 is conducting, and the capacitor C_{SM} is inserted into the circuit and charged by i_{SM}. The output voltage of the SM at this state is U_C. In state (b), i_{SM} is negative and D_2 is conducting so that the capacitor C_{SM} is bypassed. The voltage across the capacitor U_C will maintain the same in this state and the output voltage u_{SM} is zero. Since the power flow is uncontrolled in these two operation states, they are only allowed at the start-up stage of an MMC for automatic sub-module capacitor pre-charging. They are undesirable

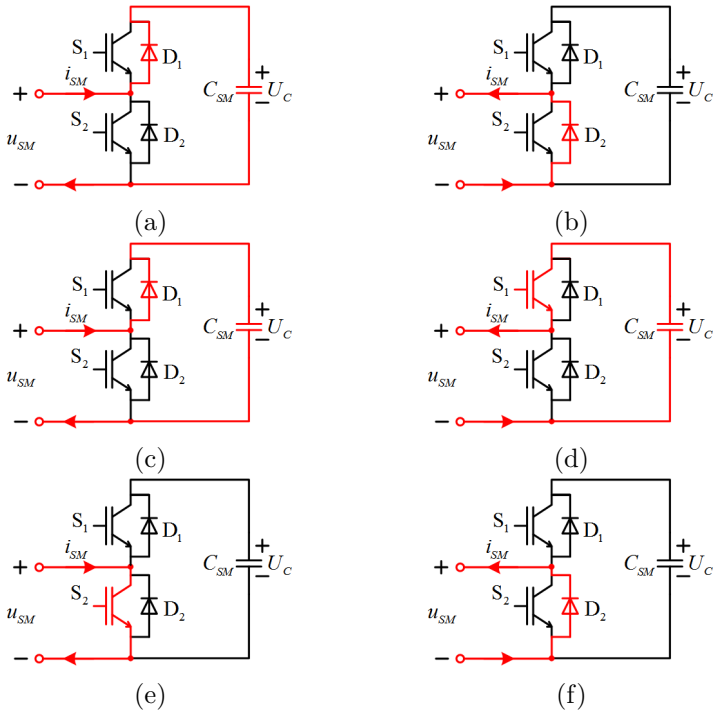


Figure 2.2: Operation states of half-bridge based sub-modules.

Table 2.2: Operation states of half-bridge sub-module

State	Switching function (S_1, S_2)	S_1	D_1	S_2	D_2	Current Direction	Capacitor State	U_{SM}
Abnormal	(0,0)	off	ON	off	off	+	Charge	U_C
		off	off	off	ON	−	Bypass	0
Insert/On	(1,0)	off	ON	off	off	+	Charge	U_C
		ON	off	off	off	−	Discharge	U_C
Bypass/Off	(0,1)	off	off	ON	off	+	Bypass	0
		off	off	off	ON	−	Bypass	0

and labelled as 'abnormal state' in the normal operation of an MMC.

In state (c) and (d), S_1 is turned on while S_2 is given a turn-off signal. In this case, D_2 stays in blocked state due to the reverse voltage applied on it. C_{SM} is always inserted into the circuit in both states and the output voltage of the SM is U_C. The difference between these two states is that C_{SM} is charged when i_{SM} is positive and discharged if i_{SM} flows reversely. These two states can be cataloged into 'insert' or 'on' state of the sub-module. The states (e) and (f) represent the scenario that S_1 is assigned a turn-off signal while a turn-on gating signal is applied to S_2. Symmetrically to 'insert' or 'on' state, the sub-module is in 'bypass' or 'off' state because the capacitor is always bypassed in states (e) and (f). The output voltage of the sub-module is zero regardless of the direction of i_{SM}.

In the case that both gating signals of the two switches are 'on', C_{SM} is shorted and permanent damages of the switches and the capacitor might be caused. This 'shoot-through' state has to be carefully avoided in normal operation and is not illustrated in Figure 2.2.

The operation states of a half-bridge based sub-module are summarized in Table 2.2, where '1' corresponds to a turn-on gating signal and '0' refers to a turn-off gating signal. It is evident that the sub-module is manipulated either to be inserted into the MMC system or bypassed by applying proper gating signals to S_1 and S_2.

2.2.2 Configuration and operation of a three-phase MMC

The schematic diagram of a three-phase MMC is shown in Figure 2.3. There are three phase legs connected in parallel to a common bus and each phase leg consists

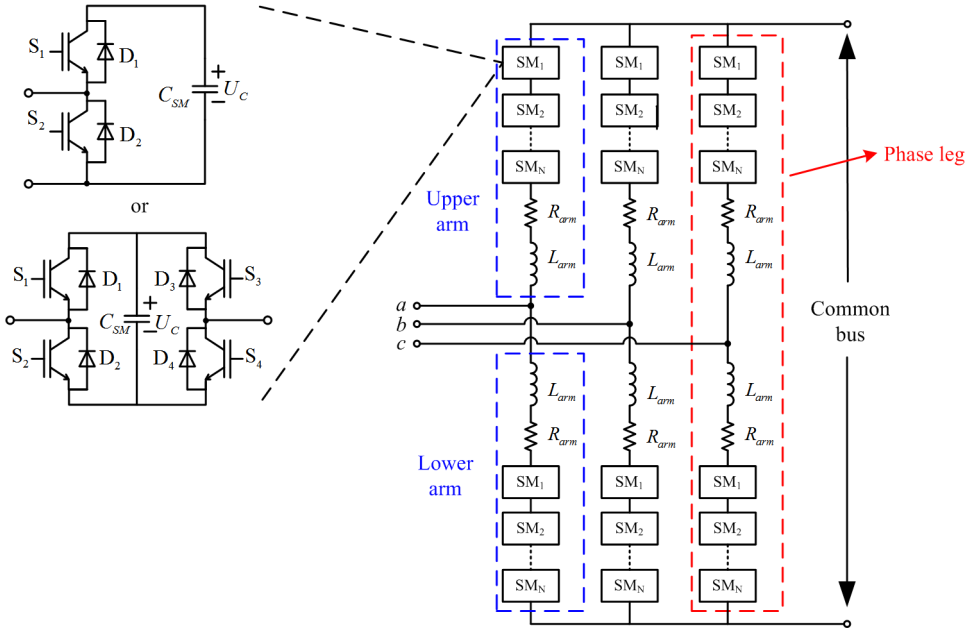


Figure 2.3: Configuration of a three-phase MMC.

of two arms, named as upper arm and lower arm respectively. The common bus can be either a DC bus or an AC bus. Different sub-module configurations can be adopted in the MMC. However, only the sub-modules capable of generating an AC output voltage u_{SM}, e.g. the full-bridge sub-module shown in 2.1 (b), are applicable in the MMC connected to an AC common bus. In this thesis, the common bus is deemed as the input power source of the MMC. The AC output terminals of the MMC are connected to the middle point of the two arms in each phase leg. N sub-modules are connected in series in each arm to generate adequate output voltage level. The number of sub-modules connected in each arm can be designed according to the common bus voltage and the voltage rating of semiconductor devices. Each arm is equipped with an arm inductor L_{arm}. The arm inductance L_{arm}, at a first glance, affects the arm current ripple and, as a result, the output current quality and the semiconductors' ratings [68–70]. In fact, L_{arm} has two basic functions in an MMC system, i.e. circulating current suppression and fault current rise rate limitation (preventing the direct connection of two voltage sources as well). However, extra voltage drop might be introduced by the arm inductance. Furthermore, current resonance is possible at particular frequencies because of the second order LC system formed by the arm inductance and sub-module capacitance. The current resonance phenomenon will be discussed in

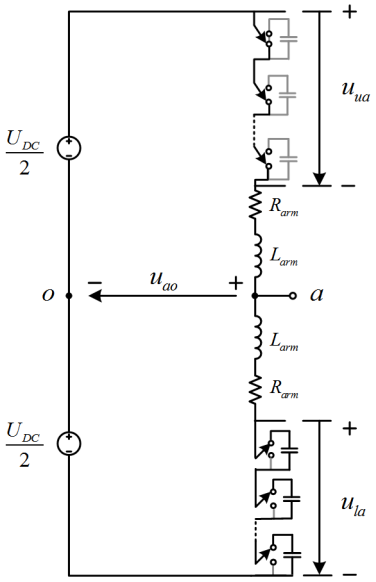


Figure 2.4: Basic operation in phase a of an MMC.

details in Section 4.2. An equivalent resistor R_{arm} is also connected in series in each arm. R_{arm} represents the losses on the switches, diodes, equivalent series resistance (ESR) in C_{SM} and L_{arm}, etc. R_{arm} is relatively small and varying according to the number of sub-modules inserted into each arm. It is normally deemed as a constant resistor in most studies.

Different from conventional voltage source converters which chop the DC voltage to produce the output voltage, an MMC creates output voltage by inserting different numbers of sub-modules into the circuit. Taking phase a as an example, the illustration of the basic operation of an MMC connected to a DC common bus is shown in Figure 2.4, where U_{DC} is the DC bus voltage. The AC output phase voltage is denoted as u_{ao} and the arm voltage generated by the inserted sub-modules are written to be u_{ua} for the upper arm and u_{la} for the lower arm. Equation (2.1) can be obtained according to Figure 2.4, ignoring the voltage drop on arm inductors and resistors.

$$u_{ao} = -u_{ua} + \frac{U_{DC}}{2} = u_{la} - \frac{U_{DC}}{2} \tag{2.1}$$

Substituting $u_{ua} = 0$ and $u_{la} = NU_C$, in other words, all the sub-modules in upper arm are in 'off' state and all the sub-modules in lower arm are in 'on' state, into (2.1), the balanced average voltage across sub-module capacitors can

Table 2.3: Output voltage of an MMC with $N = 4$

SN	n_u	n_l	u_{ao}
I	0	4	$U_{DC}/2$
II	1	3	$U_{DC}/4$
III	2	2	0
IV	3	1	$-U_{DC}/4$
V	4	0	$-U_{DC}/2$

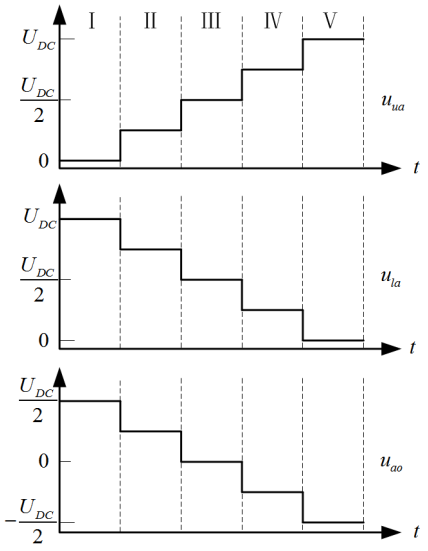


Figure 2.5: Illustration of output voltage waveforms of phase a.

be derived as

$$U_C = \frac{U_{DC}}{N} \tag{2.2}$$

Furthermore, if the numbers of sub-modules inserted in the upper and lower arms are denoted to be N_u and N_l respectively, equation (2.1) can be rewritten as

$$u_{ao} = -N_u \frac{U_{DC}}{N} + \frac{U_{DC}}{2} = N_l \frac{U_{DC}}{N} - \frac{U_{DC}}{2} \tag{2.3}$$

According to (2.3), N_u and N_l can be yield as

$$N_u + N_l = N \tag{2.4}$$

The output phase voltage can be further derived from (2.1), as

$$u_{ao} = \frac{u_{la} - u_{ua}}{2} = \frac{N_l - N_u}{N}\frac{U_{DC}}{2} \tag{2.5}$$

It can be concluded from (2.5) that the maximum magnitude of the output phase voltage is $U_{DC}/2$ and the minimum output voltage step is $U_{DC}/(2N)$. At least $N+1$ output voltage levels can be generated by an MMC with N sub-modules in each arm. Taking $N = 4$ as an example, the output voltage level regarding the number of sub-modules inserted in phase leg a are summarized in Table 2.3 and illustrated in Figure 2.5 based on equations (2.4) and (2.5). The condition $(N_u + N_l)U_C = U_{DC}$ is not always satisfied in real applications because of sub-module capacitor voltage ripples, dead time modulation, etc. Failing to meet this condition leads to the voltage mismatch between the DC bus and inserted voltage in one phase leg. This voltage mismatch will be applied onto the arm inductors and resistors and, as a result, circulating current is inevitably generated inside each phase leg.

2.3 Basic voltage and current quantities in the MMC

In order to analyze the voltage and current quantities in the MMC without losing the generality, an MMC connected to an AC common bus is discussed in this section. A DC bus connected MMC is regarded as a special case that the common bus voltage frequency is zero. The analysis in this section is based on the assumptions as follows:

1. All sub-module capacitor voltages are maintained constant at U_s/N, where U_s is the amplitude of the common bus voltage u_s;

2. All arms in the MMC are identical and the three phase loads are balanced in steady state;

3. The input current (common bus current) is equally distributed into three phase legs and the output current of each phase is equally split into two arms in the same leg.

The structure of the three-phase MMC can be simplified as in Figure 2.6, by replacing the sub-modules in each arm by a controlled voltage source representing the total voltage of inserted sub-modules in this arm. The three phase currents

are represented as i_x $(x \in a, b, c)$ and arm currents are denoted as i_{ux} and i_{lx} for the upper and lower arms in phase x respectively. The arm currents can be defined as

$$i_{ux} = \frac{i_x}{2} + i_{diffx} \quad (x \in a, b, c) \tag{2.6}$$

$$i_{lx} = -\frac{i_x}{2} + i_{diffx} \quad (x \in a, b, c) \tag{2.7}$$

where i_{diffx} is the inner differential current [71, 72] in phase leg x that defined as

$$i_{diffx} = -\frac{i_{ux} + i_{lx}}{2} = \frac{i_s}{3} + i_{cirx} \quad (x \in a, b, c) \tag{2.8}$$

The variable i_{cirx} refers to the circulating current in phase leg x. Applying Kirchhoff's voltage law (KVL) to figure 2.6, the voltage equations in each phase are:

$$\frac{u_s}{2} - u_{xo} - L_{arm}\frac{di_{ux}}{dt} - R_{arm}i_{ux} - u_{ux} = 0 \quad (x \in a, b, c) \tag{2.9}$$

$$\frac{u_s}{2} + u_{xo} - L_{arm}\frac{di_{lx}}{dt} - R_{arm}i_{lx} - u_{lx} = 0 \quad (x \in a, b, c) \tag{2.10}$$

According to equations (2.6) to (2.10), the equations for decoupled output side and input side voltages of the MMC can be derived as follows:

$$2u_{xo} + L_{arm}\frac{di_x}{dt} + R_{arm}i_x + u_{ux} - u_{lx} = 0 \quad (x \in a, b, c) \tag{2.11}$$

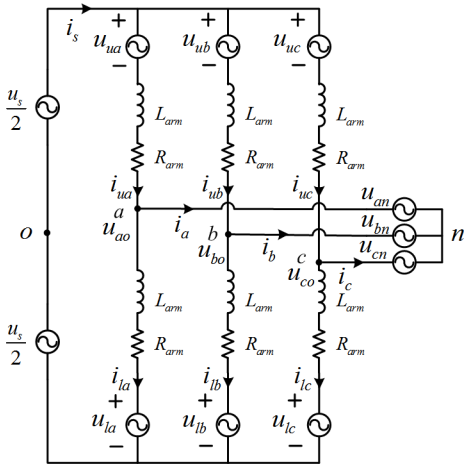


Figure 2.6: Simplified circuit of a three-phase MMC.

$$u_s - 2L_{arm}\frac{i_{diffx}}{dt} - 2R_{arm}i_{diffx} - u_{ux} - u_{lx} = 0 \quad (x \in a, b, c) \tag{2.12}$$

Neglecting the voltage drop across the arm inductance and resistance caused by the arm current, the output voltage of the MMC can be controlled by inserting proper sub-modules in upper and lower arms as

$$u_{xo} \approx \frac{u_{lx} - u_{ux}}{2} \quad (x \in a, b, c) \tag{2.13}$$

The output voltage is the difference of inserted voltage in the lower and upper arms and accordance with the equation (2.5). On the other hand, the inner differential current can be regulated by applying proper voltage, which is controlled by the sum of inserted voltages in the upper and lower arms, onto the arm inductors, as

$$L_{arm}\frac{i_{diffx}}{dt} + R_{arm}i_{diffx} = \frac{u_s - (u_{ux} + u_{lx})}{2} \quad (x \in a, b, c) \tag{2.14}$$

Theoretically, the input and output sides currents are decoupled and can be controlled independently. The interface of the input and output sides is the sub-modules inserted into the upper and lower arms.

It should be noted that the assumption of constant sub-module capacitor voltage is actually never valid. The arm current flows through sub-modules due to switching action and hence charging or discharging of sub-modules capacitor happens depending on the direction of arm current and switching function as summarized in Table 2.2 and Table 2.4. The varying capacitor voltages are inserted into arms by switching actions. As a consequence, the mismatch between the common bus voltage and the phase leg voltage will in turn influence the arm currents. The circular interaction between arm current and capacitor voltage makes the steady state analysis of the MMC complicated. Therefore, comprehensive steady

Table 2.4: Operation states of full-bridge sub-module

State	Switching function (S_1, S_2, S_3, S_4)	Current Direction	Capacitor State	U_{SM}
Insert/On	(1,0,0,1)	+	Charge	u_c
		-	Discharge	
	(0,1,1,0)	+	Discharge	$-u_c$
		-	Charge	
Bypass/off	(1,0,1,0) (0,1,0,1)	±	Bypass	0

state analysis is necessary to estimate the voltage ripple of sub-module capacitors, circulating currents, and harmonics, which will be detailed in Section 3.2.

2.4 MMC main circuit parameters design and components selection

This section briefly presents necessary design criteria for the essential power components in the MMC main circuit, including power semiconductors, sub-module DC-link capacitors, and arm inductors. The voltage level of the industrial applications adopting MMCs, e.g., medium voltage motor drives and HVDC transmission, ranges from 6.6 kV to hundreds of kilo-volts. The current rating in those applications can be up to 3 kA. The design criteria for the number of sub-modules, switching devices, capacitors, and inductors are highly application-depended.

2.4.1 Selection of semiconductor device

Within the aforementioned voltage and current ranges, a wide variety of semiconductors are available for those MMC applications, such as diodes, Silicon-Controlled Rectifiers (SCRs), Gate Turn Off (GTO) thyristors, Integrated Gate-

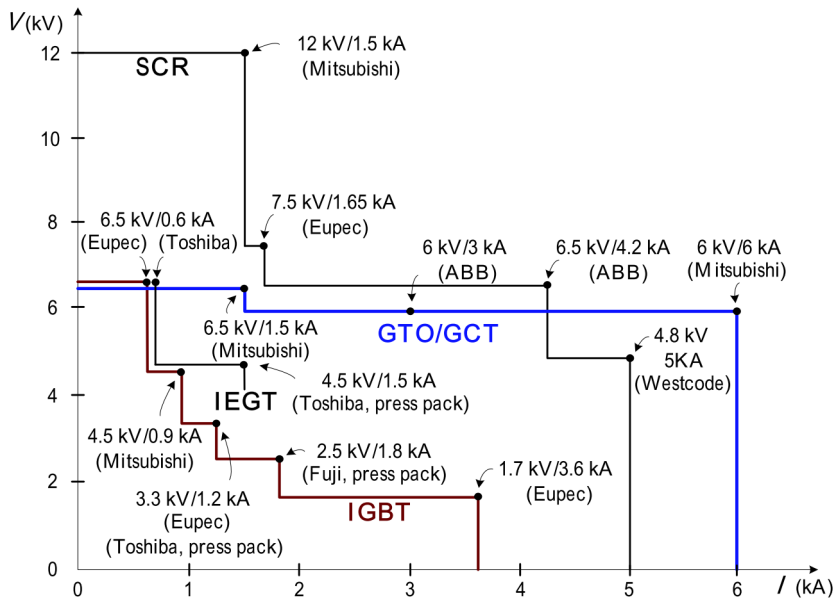


Figure 2.7: Semiconductor electrical characteristics [1].

Commutated Thyristors (IGCTs), Insulated-Gate Bipolar Transistors (IGBTs), and Symmetrical Gate Commutated Thyristors (SGCTs) [1]. A simple comparison of the electrical characteristics of these devices is shown in Figure 2.7. The characteristics of the semiconductor devices affect the design of the MMC in terms of the number of devices, the series or parallel connection, redundancy, switching frequency, efficiency, and the size of the MMC.

Because of the relatively low switching frequency of individual semiconductor devices, the conducting loss is the dominating part of the losses introduced by the switching devices in MMCs. Therefore, slow devices possessing high voltage rating and low on-resistance are preferable in MMC applications. For instance, 1.7 kV IGBTs are suitable for medium voltage drive applications [21] and 4.5 kV IGCTs are the most efficient devices for MMCs in HVDC transmission applications [2]. The current rating of the devices must be considered so that the peak arm current at the maximum operational power has to be handled with the selected devices. The peak value of the arm current in a three-phase MMC can be expressed as

$$i_{arm,max} = \frac{I_{s,max}}{3} + \frac{I_{o,max}}{2} \tag{2.15}$$

2.4.2 Determining the number of sub-modules per arm

The determination of the number of sub-modules per arm N has to take the semiconductor device voltage rating and the sub-module capacitor into account. Normally, a trade-off among the number of sub-modules, DC-link capacitor average voltage, voltage ripples across the capacitor, the overall cost, size and weight of the MMC system has to be made in this design phase. A general design process is presented as follows.

Without the voltage ripples across the capacitor, the total DC voltage of each arm that can be used to generate sufficient external and inner voltages for MMC normal operations is yield as

$$U_{arm} \geq \frac{U_s}{2} + U_{xo} \tag{2.16}$$

where U_{xo} is the amplitude of the output voltage of phase x. The capacitor average working voltage U_C is selected according to the device rating voltage, $\pm 10\%$ capacitor voltage ripple, and voltage margin reserved for the reliable operation of the capacitor and MMC operation under faulty conditions. With the known total arm DC voltage and the capacitor average working voltage, the number of

sub-module per arm can be determined as

$$N \geq \frac{U_{arm}}{U_C} \tag{2.17}$$

2.4.3 Selection of sub-module DC-link capacitance

The sub-module capacitors play an important role in interfacing the input and the output sides power flowing in the MMC. The power flowing through these capacitors introduces ripples in the capacitor voltage. One of the capacitor selection criteria is that the peak voltage ripple is less than 10% of the nominal average voltage applied on the capacitors at rated load condition. Assuming the MMC is perfectly controlled that there is no harmonics in the inner differential current, the dominant voltage ripples on each sub-module capacitor can be simply expressed based on the steady state analysis in Section 3.2.3, as

$$\tilde{u}_C = \frac{f_1(m_o, I_s, \phi_{i_o}, I_o)}{(\omega_o - \omega_s)\, C_{SM}} + \frac{f_2(m_o, I_s, \phi_{i_o}, I_o)}{(\omega_o + \omega_s)\, C_{SM}} \tag{2.18}$$

which is a function of modulation index m_o, the phase displacement between the output voltage and current ϕ_{i_o}, and the amplitudes of the input and output currents (I_s and I_o). The detailed expression of the capacitor voltage ripples can be found in Section 3.2.3. It also should be noted that the dominant voltage ripple is inversely proportional to the frequency difference between the output and input sides $|\omega_o - \omega_s|$ and the capacitance C_{SM}. The selection criteria of the capacitance can be then expressed as

$$\frac{U_{C,rpl}}{U_C} < 10\% \tag{2.19}$$

2.4.4 Selection of arm inductance

The two roles of the arm inductor in the MMC are as follows [68]:

1. Suppress the circulating current to a low level and make them manageable by means of appropriate control methods;

2. Reduce the fault current rising substantially with the presence of an input terminal short circuit fault.

If the circulating current in the MMC is not controlled intendedly, the first criterion of selecting the arm inductance at a given 2^{nd} order frequency circulating

current peak value [68] is

$$L_{arm} \geq \frac{N}{8{\omega_o}^2 C_{SM} U_C} \left(\frac{U_s I_s \cos(\phi_s)}{3 I_{cir2} \cos(\phi_{i_o})} + U_s \right) \tag{2.20}$$

where U_s is the amplitude of the input voltage, ϕ_s is the phase displacement between the input voltage and current, and I_{cir2} is the amplitude of the 2^{nd} order harmonic in the differential current.

Assume the desired fault current rise rate is α in A/s or kA/s, the second selection criterion of the arm inductance can be expressed as

$$L_{arm} \geq \frac{U_s}{2\alpha} \tag{2.21}$$

Furthermore, the circulating current resonances have to be avoided while selecting the arm inductance based on previously designed sub-module DC-link capacitance [69, 71]. The value of inductance that might result in current resonance can be derived according to the resonant current analysis in Section 4.2 as

$$L_{arm,r} = \frac{N}{16{\omega_o}^2 C_{SM}} \frac{2(k^2-1) + {m_o}^2 k^2}{k^2(k^2-1)} \qquad k = 2, 4, \cdots \tag{2.22}$$

where k refers to the harmonic order.

2.5 Summary

This chapter starts with the advantages of MMCs in medium and high voltage industrial applications, such as HVDC transmission and medium voltage motor drives. The disadvantages of the MMCs are also summarized, some of which attract considerable research interests in recent years.

The configuration of MMCs starts from the fundamental element, i.e. the sub-modules. Six types of sub-modules are briefly introduced. Since the half-bridge sub-module is adopted in this thesis, the basic structure and operation principles of a half-bridge sub-module are detailed in this chapter.

Next, the structure of a three-phase MMC, which consists of six arms, is presented in this chapter. Such MMC is able to connect to either a DC common bus or an AC common bus. The sub-modules capable of generating AC output voltage are necessary in MMCs connected to an AC bus. The stable operation of the MMC is achieved when all the sub-modules operate as a whole to generate

the required external and internal voltages. Basic voltage and current quantities, i.e. output voltage, arm voltage, arm current, inner differential current, and circulating current are introduced based on the MMC configuration and some necessary assumptions.

Some basic criteria for main circuit design with practical considerations are presented in this chapter as well, in terms of semiconductor switch selection, the number of sub-modules required in each arm, and the determination of DC-link capacitance and arm inductance. The switching devices are selected with the consideration of the voltage and current rating and the conducting loss. The number of sub-modules per arm highly depends on applications and the components selected in MMC systems. The main consideration of the capacitance selection is that if the DC-link capacitor can store sufficient energy to support the power exchange between the input and output sides of MMCs. The arm inductance is select considering the effects of circulating current suppression, fault current rising rate limitation, and circulating current resonance.

Chapter 3

Modular Multilevel Converter Modeling and Control

3.1 Introduction

Unlike the conventional voltage source power converters whose main control objective is the output power flow, an MMC requires more efforts devoted onto the complex control schemes for itself to ensure stable operation and good performance.

In this section, a generalized steady-state analysis and equivalent circuits of a three-phase MMC is presented in details. Such general model can be used for both single-phase to three-phase AC/AC converters and three-phase DC/AC inverters. The control objectives for the stable operation of the MMC are summarized according to the steady state analysis. The digital control system for the MMC is introduced. The commonly used modulation techniques for the MMC are reviewed. Among those modulation techniques, the phase shifted pulse-width modulation scheme is detailed and finally adopted in this thesis.

3.2 Steady state analysis of the MMC

3.2.1 Assumptions in the steady state analysis

The assumptions adopted in the steady state analysis in this section are as follows:

1. The number of sub-modules are large enough and the switching frequency is high enough to be treated as infinite, so that only the fundamental frequency

components in the PWM patterns of voltages and currents are investigated;

2. All the sub-modules are identical and instantaneous capacitor voltage balance is achieved at all times;

3. The modulation is carried out by simply inserting different number of sub-modules in each arm in a sinusoidal manner;

4. All the phase legs are identical;

5. The amplitudes of all three phase voltages and the three-phase loads are identical;

6. The damping effects and arm losses represented by R_{arm} are constant.

3.2.2 Definitions of the voltage and current quantities

The three-phase MMC shown in Figure 2.3 is used in the steady state analysis. The common bus is regarded as the source or input of the MMC system in the analysis. The source voltage and current are defined as

$$\begin{cases} u_s = U_s \cos(\omega_s t) \\ i_s = I_s \cos(\omega_s t + \phi_s) \end{cases} \tag{3.1}$$

where U_s and I_s are the amplitudes of the input voltage and current respectively, ω_s stands for the angular frequency of the input voltage, and ϕ_s refers to the phase displacement between the input voltage and current. Equation (3.1) is a general definition of the common bus voltage and current quantities. The frequency ω_s and ϕ_s are zero if the MMC is connected to a common DC bus.

The three-phase AC side is deemed as the output side of the MMC and the quantities are defined as

$$\begin{cases} u_{xo} = U_o \cos(\omega_o t + \phi_o + \phi_x) \\ i_x = I_o \cos(\omega_o t + \phi_o + \phi_x + \phi_{i_o}) \end{cases} \tag{3.2}$$

where $x \in a, b, c$, U_o and I_o are the amplitudes of the output voltage and current respectively, which are identical in the three phases. ω_o is the output voltage angular frequency and $\phi_o + \phi_x$ are the initial phase angle of the three output phase voltages at $t = 0$. $\phi_a = 0$, $\phi_b = -2\pi/3$ and $\phi_c = 2\pi/3$ are adopted in the

analysis assuming the three phases are well-balanced. The phase displacement between the output voltage and current is denoted as ϕ_{i_o}. According to the MMC operation introduced in Section 2.2.2, the sub-module DC-link capacitor average voltage in the MMC normal operation is assumed as

$$U_C = \frac{U_s}{N} \tag{3.3}$$

Therefore, the maximum amplitude of the output voltage is yielded by the capacitor voltage, as

$$U_{o,max} = \frac{U_s}{2} \tag{3.4}$$

From (2.9) and (2.10), neglecting the voltage drop on the arm inductance and resistance since it is relatively small compared with the arm voltages, the voltages that should be inserted into the upper and lower arms can be respectively derived as

$$\begin{cases} u_{ux} = \dfrac{u_s}{2} - u_{xo} = \dfrac{U_s}{2}\left[\cos(\omega_s t) - m_o \cos(\omega_o t + \phi_o + \phi_x)\right] \\ u_{lx} = \dfrac{u_s}{2} + u_{xo} = \dfrac{U_s}{2}\left[\cos(\omega_s t) + m_o \cos(\omega_o t + \phi_o + \phi_x)\right] \end{cases} \tag{3.5}$$

where m_o is the modulation index as

$$m_o = \frac{2U_o}{NU_C} = \frac{2U_o}{U_s} \tag{3.6}$$

According to assumption (1) at the beginning of this section, the numbers of inserted sub-modules in the upper and lower arms are also in a sinusoidal pattern and the insert indices can be described as

$$\begin{cases} n_{ux} = \dfrac{\cos(\omega_s t) - m_o \cos(\omega_o t + \phi_o + \phi_x)}{2} \\ n_{lx} = \dfrac{\cos(\omega_s t) + m_o \cos(\omega_o t + \phi_o + \phi_x)}{2} \end{cases} \tag{3.7}$$

The circulating current i_{cirx} in (2.8) is defined as

$$i_{cirx} = \sum_{k\in\mathbb{N}} i_{cirxk} = \sum_{k\in\mathbb{N}} I_{cirxk} \cos\left(\omega_{cirxk} t + \phi_{cirxk}\right) \tag{3.8}$$

where I_{cirxk}, ω_{cirxk}, and ϕ_{cirxk} are the amplitude, angular frequency, and phase angle of the k^{th} order harmonic current i_{cirxk}, respectively.

3.2.3 Sub-module capacitor voltage

As summarized in Table 2.2 and Table 2.4, a DC-link capacitor is either charged or discharged by the arm current if the corresponding sub-module is inserted into the MMC main circuit. According to the average model of the MMC [71], the current flowing through the k^{th} sub-module capacitor in the upper and lower arms of phase x can be defined as

$$\begin{cases} i_{Cuxk} = n_{ux} i_{ux} \\ i_{Clxk} = n_{lx} i_{lx} \end{cases} \tag{3.9}$$

The capacitor voltage can be calculated by integrating the capacitor current as

$$\begin{cases} u_{Cuxk} = \dfrac{1}{C_{SM}} \displaystyle\int i_{Cuxk} dt \\ u_{Clxk} = \dfrac{1}{C_{SM}} \displaystyle\int i_{Clxk} dt \end{cases} \tag{3.10}$$

Assuming there is no circulating current ripples, i.e. $i_{cirx} = 0$, in three phase legs, the capacitor currents can be derived from (2.6) − (2.8) and (3.7), as

$$\begin{cases} i_{Cuxk} = \dfrac{I_s \cos(\phi_s)}{6} - \dfrac{m_o I_o \cos(\phi_{i_o})}{4} + \dfrac{I_s \cos(2\omega_s t + \phi_s)}{6} \\ \quad + \dfrac{I_o \cos[(\omega_o - \omega_s)t + \theta_{ox} + \phi_{i_o}]}{4} - \dfrac{m_o I_s \cos[(\omega_o - \omega_s)t + \theta_{ox} - \phi_s]}{6} \\ \quad + \dfrac{I_o \cos[(\omega_o + \omega_s)t + \theta_{ox} + \phi_{i_o}]}{4} - \dfrac{m_o I_s \cos[(\omega_o + \omega_s)t + \theta_{ox} + \phi_s]}{6} \\ \quad - \dfrac{m_o I_o \cos(2\omega_o t + 2\theta_{ox} + \phi_{i_o})}{4} \\ i_{Clxk} = \dfrac{I_s \cos(\phi_s)}{6} - \dfrac{m_o I_o \cos(\phi_{i_o})}{4} + \dfrac{I_s \cos(2\omega_s t + \phi_s)}{6} \\ \quad - \dfrac{I_o \cos[(\omega_o - \omega_s)t + \theta_{ox} + \phi_{i_o}]}{4} + \dfrac{m_o I_s \cos[(\omega_o - \omega_s)t + \theta_{ox} - \phi_s]}{6} \\ \quad - \dfrac{I_o \cos[(\omega_o + \omega_s)t + \theta_{ox} + \phi_{i_o}]}{4} + \dfrac{m_o I_s \cos[(\omega_o + \omega_s)t + \theta_{ox} + \phi_s]}{6} \\ \quad - \dfrac{m_o I_o \cos(2\omega_o t + 2\theta_{ox} + \phi_{i_o})}{4} \end{cases} \tag{3.11}$$

where $\theta_{ox} = \phi_o + \phi_x$. The DC components in i_{Cuxk} and i_{Clxk} in (3.11) will continuously charge the sub-module capacitor to an extremely high voltage or discharge the capacitor to zero, which consequently leads to the unstable operation of the MMC. Therefore, in order to remain the stable operation of the MMC, the

sum of the DC parts of the capacitor current has to be zero in steady state, which implies the active power balance between the input and output sides of the MMC. If the MMC is connected to a common AC bus, the active power balance requires that

$$\frac{I_s \cos(\phi_s)}{3} = \frac{m_o I_o \cos(\phi_{i_o})}{2} \tag{3.12}$$

On the other hand, the power balance of an MMC connected to a common DC bus ($\omega_s = 0$ and $\phi_s = 0$) is achieved if

$$\frac{I_s \cos(\phi_s)}{6} + \frac{I_s \cos(2\omega_s t + \phi_s)}{6} = \frac{I_s}{3} = \frac{m_o I_o \cos(\phi_{i_o})}{4} \tag{3.13}$$

According to (3.10) and (3.11), the sub-module DC-link capacitor voltage in the upper and lower arms can be obtained as

$$\begin{cases} u_{Cuxk} = U_C + \dfrac{1}{12C_{SM}} \left[\dfrac{A_{2\omega_s}(t)}{\omega_s} - \dfrac{A_{2\omega_o}(t)}{2\omega_o} + \dfrac{A_{\omega_o-\omega_s}(t)}{\omega_o-\omega_s} + \dfrac{A_{\omega_o+\omega_s}(t)}{\omega_o+\omega_s} \right] \\ u_{Clxk} = U_C + \dfrac{1}{12C_{SM}} \left[\dfrac{A_{2\omega_s}(t)}{\omega_s} - \dfrac{A_{2\omega_o}(t)}{2\omega_o} - \dfrac{A_{\omega_o-\omega_s}(t)}{\omega_o-\omega_s} - \dfrac{A_{\omega_o+\omega_s}(t)}{\omega_o+\omega_s} \right] \end{cases} \tag{3.14}$$

where $A_{2\omega_s}(t)$, $A_{2\omega_o}(t)$, $A_{\omega_o-\omega_s}(t)$ and $A_{\omega_o+\omega_s}(t)$ are sinusoidal terms with corresponding angular frequencies defined as

$$\begin{cases} A_{2\omega_s}(t) = I_s \sin(2\omega_s t + \phi_s) \\ A_{2\omega_o}(t) = 3m_o I_o \sin(2\omega_o t + 2\theta_{ox} + \phi_{i_o}) \\ A_{\omega_o-\omega_s}(t) = 3I_o \sin[(\omega_o-\omega_s)t + \theta_{ox} + \phi_{i_o}] - 2m_o I_s \sin[(\omega_o-\omega_s)t + \theta_{ox} - \phi_s] \\ A_{\omega_o+\omega_s}(t) = 3I_o \sin[(\omega_o+\omega_s)t + \theta_{ox} + \phi_{i_o}] - 2m_o I_s \sin[(\omega_o+\omega_s)t + \theta_{ox} + \phi_s] \end{cases} \tag{3.15}$$

The capacitor voltages shown in equation (3.3) can be divided into two parts, i.e. the average capacitor voltage U_C and the voltage ripples $\tilde{u}_C$ that are introduced by the arm currents. The term $A_{2\omega_s}(t)$ has to be canceled according to power balance yield by (3.13), if the MMC is connected to a DC common bus and $\omega_s = 0$ in such case. The voltage ripples across the capacitors in the upper and lower arms can be obtained as

$$\begin{cases} \tilde{u}_{Cuxk} = \dfrac{1}{12C_{SM}} \left[\dfrac{A_{2\omega_s}(t)}{\omega_s} - \dfrac{A_{2\omega_o}(t)}{2\omega_o} + \dfrac{A_{\omega_o-\omega_s}(t)}{\omega_o-\omega_s} + \dfrac{A_{\omega_o+\omega_s}(t)}{\omega_o+\omega_s} \right] \\ \tilde{u}_{Clxk} = \dfrac{1}{12C_{SM}} \left[\dfrac{A_{2\omega_s}(t)}{\omega_s} - \dfrac{A_{2\omega_o}(t)}{2\omega_o} - \dfrac{A_{\omega_o-\omega_s}(t)}{\omega_o-\omega_s} - \dfrac{A_{\omega_o+\omega_s}(t)}{\omega_o+\omega_s} \right] \end{cases} \tag{3.16}$$

$$\begin{cases} A_{2\omega_s}(t) = Km_oI_o\cos(\phi_{i_o})\sin(2\omega_s t + \phi_s) \\ A_{2\omega_o}(t) = 3m_oI_o\sin(2\omega_o t + 2\theta_{ox} + \phi_{i_o}) \\ A_{\omega_o-\omega_s}(t) = \ 3I_o\sin[(\omega_o-\omega_s)t + \theta_{ox} + \phi_{i_o}] \\ \qquad\qquad - 2Km_o{}^2I_o\cos(\phi_{i_o})\sin[(\omega_o-\omega_s)t + \theta_{ox} - \phi_s] \\ A_{\omega_o+\omega_s}(t) = \ 3I_o\sin[(\omega_o+\omega_s)t + \theta_{ox} + \phi_{i_o}] \\ \qquad\qquad - 2Km_o{}^2I_o\cos(\phi_{i_o})\sin[(\omega_o+\omega_s)t + \theta_{ox} + \phi_s] \end{cases} \tag{3.17}$$

According to the active power balance between the input and output sides of the MMC, the amplitude of the input current I_s can be explicitly represented by the amplitude of output current I_o according to equations (3.12) and (3.13). The $A_{2\omega_s}(t)$, $A_{\omega_o-\omega_s}(t)$, $A_{\omega_o+\omega_s}(t)$ and $A_{2\omega_o}(t)$ terms can be rewritten as in (3.17). The constant K is $3/(2\cos(\phi_s))$ in an AC-to-AC MMC and equals to $3/4$ in a DC-to-AC MMC. The following finding can be obtained from equations (3.16) and (3.17):

1. The amplitudes of the capacitor voltage ripples are inversely proportional to the capacitance and their corresponding angular frequencies, and proportional to the output current.

2. Because the frequency terms (ω_s, ω_o, $\omega_o - \omega_s$ and $\omega_o + \omega_s$) appear in the denominators in (3.16), the capacitor voltage ripples might be extremely high if the frequencies of the input and output voltages are close to each other ($\omega_o - \omega_s \approx 0$) or the output voltage frequency is close to zero ($\omega_o \approx 0$). The worst case is that both ω_s and ω_o are close to zero ($\omega_s \approx 0$, $\omega_o \approx 0$, $\omega_o - \omega_s \approx 0$ and $\omega_o + \omega_s \approx 0$).

3. The waveform of capacitor voltage ripples is affected by the modulation index, as well as the power factors of the source and loads. Such impacts are complex and not deeply studied in this thesis.

4. Differential-mode components ($A_{\omega_o-\omega_s}(t)$ and $A_{\omega_o+\omega_s}(t)$) and common-mode components ($A_{2\omega_s}(t)$ and $A_{2\omega_o}(t)$) exist in the capacitor voltage ripples in the upper and lower arms. The differential-mode components are 180° phase-shifted and imply the energy swag between the upper and lower arms. On the other hand, the common-mode components in the capacitor voltage ripples in the upper and lower arms are in phase with each other. Such common-mode components indicate the energy taken from the source and supplied to the loads by the both arms.

3.2.4 Inserted arm voltages

The k^{th} sub-modules are inserted into the upper and lower arms according to the insert indices to generate the output voltage of the sub-modules as

$$\begin{cases} u_{SMuxk} = n_{ux} u_{Cuxk} \\ u_{SMlxk} = n_{lx} u_{Clxk} \end{cases} \tag{3.18}$$

Substituting equations (3.3) and (3.7) into (3.18), the sub-module output voltages can be expressed as

$$\begin{cases} u_{SMuxk} = \dfrac{U_C}{2}\left[\cos(\omega_s t) - m_o \cos(\omega_o t + \theta_{ox})\right] + \\ \qquad \dfrac{I_o}{48 C_{SM}} \left\{ \dfrac{A_1 - A_5}{\omega_s} + \dfrac{A_2 - A_6}{(\omega_o - \omega_s)} + \dfrac{A_3 - A_7}{(\omega_o + \omega_s)} - \dfrac{A_4 - A_8}{2\omega_o} \right\} \\ u_{SMlxk} = \dfrac{U_C}{2}\left[\cos(\omega_s t) + m_o \cos(\omega_o t + \theta_{ox})\right] + \\ \qquad \dfrac{I_o}{48 C_{SM}} \left\{ \dfrac{A_1 + A_5}{\omega_s} - \dfrac{A_2 + A_6}{(\omega_o - \omega_s)} - \dfrac{A_3 + A_7}{(\omega_o + \omega_s)} - \dfrac{A_4 + A_8}{2\omega_o} \right\} \end{cases} \tag{3.19}$$

where

$$\begin{cases} A_1 = K m_o \cos(\phi_{i_o})[\sin(\omega_s t + \phi_s) + \sin(3\omega_s t + \phi_s)] \\ A_2 = \ 3[\sin(\omega_o t + \theta_{ox} + \phi_{i_o}) + \sin((\omega_o - 2\omega_s)t + \theta_{ox} + \phi_{i_o})] \\ \qquad - 2K {m_o}^2 \cos(\phi_{io})[\sin(\omega_o t + \theta_{ox} - \phi_s) + \sin((\omega_o - 2\omega_s)t + \theta_{ox} - \phi_s)] \\ A_3 = \ 3[\sin(\omega_o t + \theta_{ox} + \phi_{i_o}) + \sin((\omega_o + 2\omega_s)t + \theta_{ox} + \phi_{i_o})] \\ \qquad - 2K {m_o}^2 \cos(\phi_{i_o})[\sin(\omega_o t + \theta_{ox} + \phi_s) + \sin((\omega_o + 2\omega_s)t + \theta_{ox} + \phi_s)] \\ A_4 = 3m_o[\sin((2\omega_o + \omega_s)t + 2\theta_{ox} + \phi_{i_o}) + \sin((2\omega_o - \omega_s)t + 2\theta_{ox} + \phi_{i_o})] \\ A_5 = K {m_o}^2 \cos(\phi_{io})[\sin((\omega_o + 2\omega_s)t + \theta_{ox} + \phi_s) - \sin((\omega_o - 2\omega_s)t + \theta_{ox} - \phi_s)] \\ A_6 = \ 3m_o[\sin((2\omega_o - \omega_s)t + 2\theta_{ox} + \phi_{i_o}) - \sin(\omega_s t - \phi_{i_o})] \\ \qquad - 2K {m_o}^3 \cos(\phi_{i_o})[\sin((2\omega_o - \omega_s)t + 2\theta_{ox} - \phi_s) - \sin(\omega_s t + \phi_s)] \\ A_7 = \ 3m_o[\sin((2\omega_o + \omega_s)t + 2\theta_{ox} + \phi_{i_o}) + \sin(\omega_s t + \phi_{i_o})] \\ \qquad - 2K {m_o}^3 \cos(\phi_{i_o})[\sin((2\omega_o + \omega_s)t + 2\theta_{ox} + \phi_s) + \sin(\omega_s t + \phi_s)] \\ A_8 = 3{m_o}^2[\sin(\omega_o t + \theta_{ox} + \phi_{i_o}) + \sin(3\omega_o t + 3\theta_{ox} + \phi_{i_o})] \end{cases} \tag{3.20}$$

Since all the sub-module capacitor voltages in the same arm are assumed to

be identical, the inserted voltage in the upper and lower arms can be obtained by simply multiplying the individual sub-module output voltage by the number of sub-modules in each arm [71, 73], as

$$\begin{cases} u_{ux} = N u_{SMuxk} \\ u_{lx} = N u_{SMlxk} \end{cases} \tag{3.21}$$

It is obvious that there are also common-mode and differential-mode components in the inserted arm voltages for the upper and lower arms. $U_C \cos(\omega_s t)/2$, A_1, A_4, A_6 and A_7 are common-mode components, while $m_o U_C \cos(\omega_o t + \theta_{ox})/2$, A_2, A_3, A_5 and A_8 are differential-mode ones. In order to associate the common-mode and differential-mode components with their frequencies, the inserted arm voltages can be rearranged as

$$\begin{cases} u_{ux} = \dfrac{NU_C}{2}[\cos(\omega_s t) - m_o \cos(\omega_o t + \theta_{ox})] + \\ \qquad \dfrac{NI_o}{48C_{SM}}\left[B_{\omega_s}(t) + B_{3\omega_s}(t) + B_{2\omega_o \pm \omega_s}(t) + B_{\omega_o}(t) + B_{\omega_o \pm 2\omega_s}(t) + B_{3\omega_o}(t)\right] \\ u_{lx} = \dfrac{NU_C}{2}[\cos(\omega_s t) + m_o \cos(\omega_o t + \theta_{ox})] + \\ \qquad \dfrac{NI_o}{48C_{SM}}\left[B_{\omega_s}(t) + B_{3\omega_s}(t) + B_{2\omega_o \pm \omega_s}(t) - B_{\omega_o}(t) - B_{\omega_o \pm 2\omega_s}(t) - B_{3\omega_o}(t)\right] \end{cases} \tag{3.22}$$

where

$$\begin{cases} B_{\omega_s}(t) = \left(\dfrac{1}{\omega_s} - \dfrac{2{m_o}^2}{\omega_o - \omega_s} + \dfrac{2{m_o}^2}{\omega_o + \omega_s}\right) K m_o \cos(\phi_{io}) \sin(\omega_s t + \phi_s) \\ \qquad\qquad + \dfrac{3m_o}{\omega_o - \omega_s} \sin(\omega_s t - \phi_{io}) - \dfrac{3m_o}{\omega_o + \omega_s} \sin(\omega_s t + \phi_{io}) \\ B_{3\omega_s}(t) = \dfrac{K m_o \cos(\phi_{io})}{\omega_s} \sin(3\omega_s t + \phi_s) \\ B_{2\omega_o \pm \omega_s}(t) = -\left(\dfrac{3m_o}{2\omega_o} + \dfrac{3m_o}{\omega_o + \omega_s}\right) \sin[(2\omega_o + \omega_s)t + 2\theta_{ox} + \phi_{io}] \\ \qquad\qquad + \dfrac{2K{m_o}^3 \cos(\phi_{io})}{\omega_o + \omega_s} \sin[(2\omega_o + \omega_s)t + 2\theta_{ox} + \phi_s] \\ \qquad\qquad - \left(\dfrac{3m_o}{2\omega_o} + \dfrac{3m_o}{\omega_o - \omega_s}\right) \sin[(2\omega_o - \omega_s)t + 2\theta_{ox} + \phi_{io}] \\ \qquad\qquad + \dfrac{2K{m_o}^3 \cos(\phi_{io})}{\omega_o - \omega_s} \sin[(2\omega_o - \omega_s)t + 2\theta_{ox} - \phi_s] \end{cases} \tag{3.23}$$

and

$$\begin{cases} B_{\omega_o}(t) = \left(\dfrac{3}{\omega_o-\omega_s}+\dfrac{3}{\omega_o+\omega_s}+\dfrac{3{m_o}^2}{2\omega_o}\right)\sin(\omega_o t+\theta_{ox}+\phi_{io}) \\ \qquad\qquad -2K{m_o}^2\cos(\phi_{io})\left[\dfrac{\sin(\omega_o t+\theta_{ox}-\phi_s)}{\omega_o-\omega_s}+\dfrac{\sin(\omega_o t+\theta_{ox}+\phi_s)}{\omega_o+\omega_s}\right] \\ B_{3\omega_o}(t) = \dfrac{3{m_o}^2}{2\omega_o}\sin(3\omega_o t+3\theta_{ox}+\phi_{io}) \\ B_{\omega_o\pm2\omega_s}(t) = -\left(\dfrac{2K{m_o}^2}{\omega_o+\omega_s}+\dfrac{K{m_o}^2}{\omega_s}\right)\cos(\phi_{io})\sin[(\omega_o+2\omega_s)t+\theta_{ox}+\phi_s] \\ \qquad\qquad +\dfrac{3}{\omega_o+\omega_s}\sin[(\omega_o+2\omega_s)t+\theta_{ox}+\phi_{io}] \\ \qquad\qquad -\left(\dfrac{2K{m_o}^2}{\omega_o-\omega_s}-\dfrac{K{m_o}^2}{\omega_s}\right)\cos(\phi_{io})\sin[(\omega_o-2\omega_s)t+\theta_{ox}-\phi_s] \\ \qquad\qquad +\dfrac{3}{\omega_o-\omega_s}\sin[(\omega_o-2\omega_s)t+\theta_{ox}+\phi_{io}] \end{cases} \tag{3.24}$$

It can be seen in equations (3.22) − (3.24) that the components having frequencies at ω_s, $3\omega_s$ and $2\omega_o \pm \omega_s$ are the same in both the upper and lower arms. In contrast, the components with frequencies ω_o, $3\omega_o$ and $\omega_o \pm 2\omega_s$ in the upper and lower arms have opposite directions.

3.2.5 Phase and output voltages of the MMC

Only the first two terms of the u_{ux} and u_{lx} in (3.22) are preferred to generate the proper output phase voltage and maintain the stable operation of the MMC according to the references. Other terms are undesirable and considered as harmonics. The influence introduced by the harmonics to the phase and output voltages will be discussed in this subsection.

The voltage inserted into the phase leg x is

$$\begin{aligned} u_{phx} &= u_{ux}+u_{lx} \\ &= NU_C\cos(\omega_s t)+\frac{NI_o}{24C_{SM}}\left[B_{\omega_s}(t)+B_{3\omega_s}(t)+B_{2\omega_o\pm\omega_s}(t)\right] \end{aligned} \tag{3.25}$$

Consequently, the voltage mismatch between the common bus voltage and the inserted phase leg voltage (harmonic terms) will be applied on the arm inductors and therefore induce the circulating current in the phase leg. Such voltage

mismatch can be expressed as

$$\begin{aligned} u_{misx} &= u_s - u_{phx} \\ &= -\frac{NI_o}{24C_{SM}}\left[B_{\omega_s}(t) + B_{3\omega_s}(t) + B_{2\omega_o \pm \omega_s}(t)\right] \end{aligned} \tag{3.26}$$

It is clear in (3.26) that the common-mode harmonics in the inserted arm voltages will inevitably induce the inner differential currents at frequencies ω_s, $3\omega_s$ and $2\omega_o \pm \omega_s$, which implies that control loops have to be designed to eliminate the undesirable circulating current ripples in MMCs.

On the other hand, the output voltage of the MMC is derived from (2.13) as

$$\begin{aligned} u_{ox} &= \frac{u_{lx} - u_{ux}}{2} \\ &= \frac{NU_C m_o}{2}\cos(\omega_o t + \theta_{ox}) - \frac{NI_o}{48C_{SM}}\left[B_{\omega_o}(t) + B_{\omega_o \pm \omega_s}(t) + B_{3\omega_o}(t)\right] \end{aligned} \tag{3.27}$$

It can be seen in (3.27) that besides the desired output voltage (the first term of the right-hand side of equation (3.27)), harmonics with frequencies ω_o, $3\omega_o$ and $\omega_o \pm 2\omega_s$, whose amplitudes are inversely proportional to ω_o and ω_s, exist in the output voltage of the MMC as well. Such harmonics might distort the output voltage waveform especially when ω_o and ω_s are close to each other or zero.

3.2.6 Circulating current

Although the circulating current is assumed as zero in the aforementioned steady-state analysis, the voltage mismatch between the common bus and the inserted phase voltage will inevitably introduce current ripples circulating in each phase leg. The currents introduced by the voltage mismatch can be calculated as in (3.28).

It can be observed in (3.28) that both the input and output sides contribute to the circulating current in phase legs. The zero sequence circulating current, having frequencies of ω_s and $3\omega_s$, from the common bus are in phase in three phase legs. On the other hand, the negative sequence ripple currents, whose frequencies are $2\omega_o \pm \omega_s$, are caused by the output side and circulate among the three phase legs. It should be noted that there is no circulating current with fundamental frequency ω_o. The fundamental frequency component in the circulating current has to be zero or orthogonal ($\pm 90°$ phase-shifted) with the output voltage u_{ox} [71]. Failing to satisfy this condition will result in the voltages of upper and lower arm differ

from each other continuously with time. Such fundamental frequency component can be utilized to transfer energy [71] between the upper and lower arms, in order to balance the voltage or energy of two arms in the same phase leg. The fundamental circulating current in phase with the output voltage transfers the energy from the upper arm to the lower arm, and vice versa if the direction of the fundamental circulating current is opposite to that of the output voltage.

$$\begin{aligned} i_{cirx} =& \frac{1}{2L_{arm}} \int u_{misx} dt = \frac{NI_o}{48C_{SM}L_{arm}} \Bigg\{ \frac{Km_o \cos(\phi_{i_o})}{3{\omega_s}^2} \cos(3\omega_s t + \phi_s) \\ &+ \frac{K\cos(\phi_{i_o})}{\omega_s} \left(\frac{m_o}{\omega_s} - \frac{4\omega_s {m_o}^3}{{\omega_o}^2 - {\omega_s}^2} \right) \cos(\omega_s t + \phi_s) \\ &+ \frac{3m_o}{(\omega_o - \omega_s)\omega_s} \cos(\omega_s t - \phi_{i_o}) - \frac{3m_o}{(\omega_o + \omega_s)\omega_s} \cos(\omega_s t + \phi_{i_o}) \\ &- \frac{1}{2\omega_o + \omega_s} \left(\frac{3m_o}{2\omega_o} + \frac{3m_o}{\omega_o + \omega_s} \right) \cos[(2\omega_o + \omega_s)t + 2\theta_{ox} + \phi_{i_o}] \\ &+ \frac{2K{m_o}^3 \cos(\phi_{i_o})}{(\omega_o + \omega_s)(2\omega_o + \omega_s)} \cos[(2\omega_o + \omega_s)t + 2\theta_{ox} + \phi_s] \\ &- \frac{1}{2\omega_o - \omega_s} \left(\frac{3m_o}{2\omega_o} + \frac{3m_o}{\omega_o - \omega_s} \right) \cos[(2\omega_o - \omega_s)t + 2\theta_{ox} + \phi_{i_o}] \\ &+ \frac{2K{m_o}^3 \cos(\phi_{i_o})}{(\omega_o - \omega_s)(2\omega_o - \omega_s)} \cos[(2\omega_o - \omega_s)t + 2\theta_{ox} - \phi_s] \Bigg\} \end{aligned} \tag{3.28}$$

3.3 Equivalent circuit of a three-phase MMC

According to equation (3.22), the equivalent circuit of the three-phase MMC based on aforementioned analysis is shown in Figure 3.1, where

$$\begin{cases} u_{x\_harm\_com} = \dfrac{NI_o}{48C_{SM}} \Big[B_{\omega_s}(t) + B_{3\omega_s}(t) + B_{2\omega_o \pm \omega_s}(t) \Big] \\ u_{x\_harm\_diff} = \dfrac{NI_o}{48C_{SM}} \Big[B_{\omega_o}(t) + B_{\omega_o \pm 2\omega_s}(t) + B_{3\omega_o}(t) \Big] \end{cases} \tag{3.29}$$

are the common- and differential-mode harmonics of the voltages in the upper and lower arms. The three-phase load voltages of the MMC are defined as

$$\begin{bmatrix} u_{an} \\ u_{bn} \\ u_{cn} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} u_{ao} \\ u_{bo} \\ u_{co} \end{bmatrix} \tag{3.30}$$

The inserted voltage in each arm can be divided into four equivalent voltage

source as indicated in Figure 3.1. The first voltage source $0.5NU_C\cos(\omega_s t)$ generates a voltage that makes sure the sum of the voltages of the upper and lower arms is equal to the source voltage. The voltage source $u_x{}^* = m_o NU_C \sin(\omega_o t + \theta_{ox})$ $(x \in a, b, c)$ is the desired AC output voltage. Such voltage sources in the upper

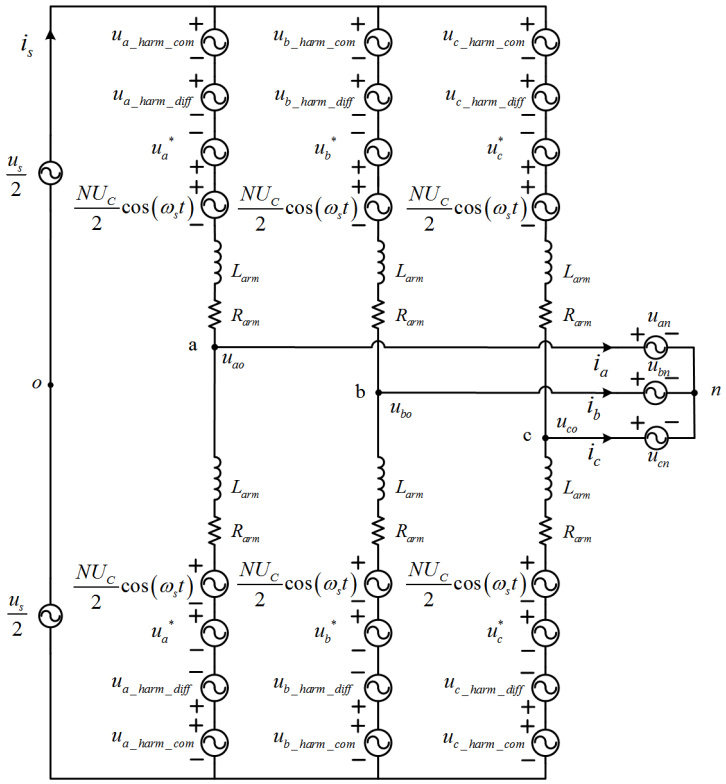


Figure 3.1: Equivalent circuit of the 3-phase MMC.

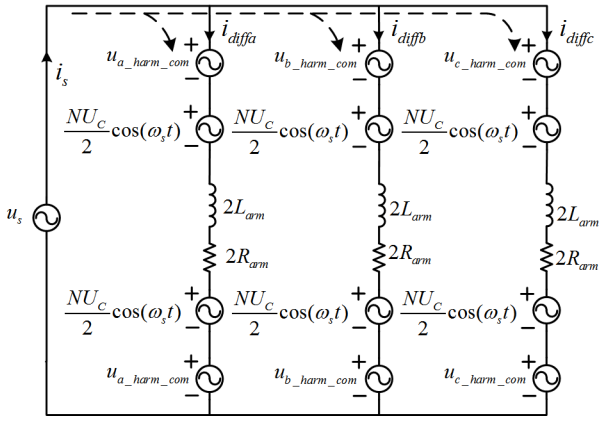


Figure 3.2: Input side equivalent circuit of the MMC.

and lower arms are denoted in opposite directions. The differential-mode and common-mode harmonics voltage sources represent the harmonics in the inserted voltage of each arm. The common-mode voltage sources appear in the input side equivalent circuit while the differential-mode ones appear in the output side equivalent circuit of the MMC.

Figure 3.2 shows the input side equivalent circuit of the 3-phase MMC. Only common-mode components are integrated into the equivalent circuit. Figure 3.3 presents the generation of the source currents in three phases. The common-mode harmonics generate the circulating current inside phase legs that will not flow into AC output of the MMC, and these circulating currents will flow among phase legs and the common bus, as shown in Figure 3.4. Apparently, the zero-sequence currents having frequencies of ω_s and $3\omega_s$ circulate between the common voltage

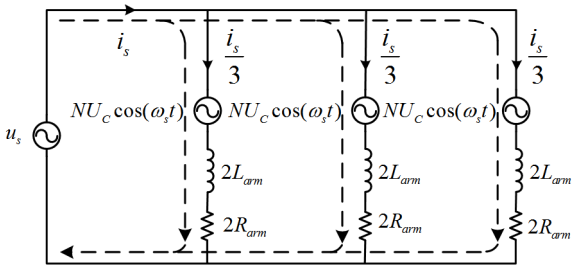


Figure 3.3: Equivalent circuit of the source current.

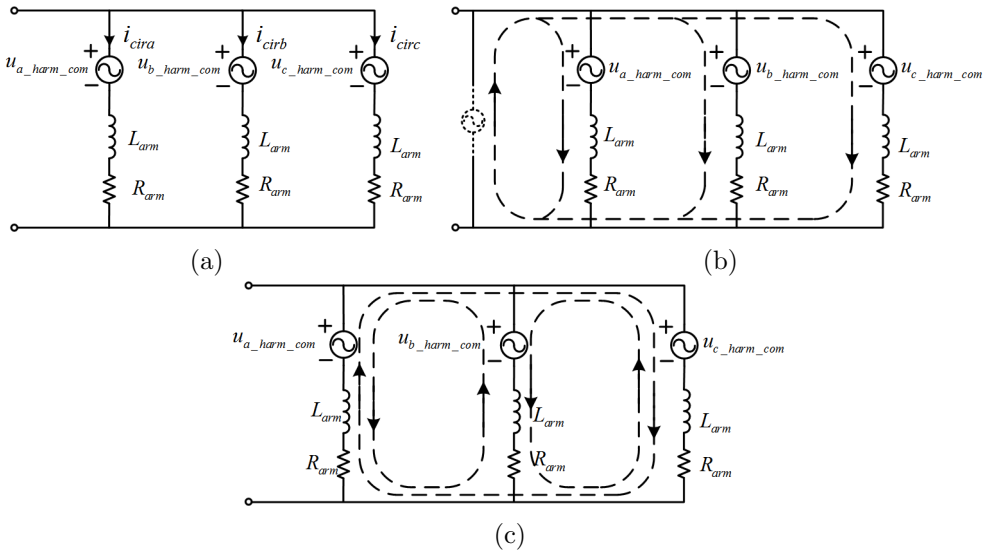


Figure 3.4: Equivalent circuit of the circulating current: (a) equivalent circuit; (b) zero-sequence harmonics path; (c) negative-sequence harmonics path.

bus and phase legs, as shown in Figure 3.4 (b). The negative-sequence currents having frequencies of $2\omega_o \pm \omega_s$ flow among the three phase legs, as presented in Figure 3.4 (c).

Integrating the voltage source $u_x{}^* = m_o N U_C \sin(\omega_o t + \theta_{ox})$ $(x \in a, b, c)$ and the differential-mode harmonics only in the three-phase MMC system, the output side equivalent circuit is obtained as in Figure 3.5 (a). The MMC can provide active and reactive power to the loads by controlling the voltage source $u_x{}^*$. The

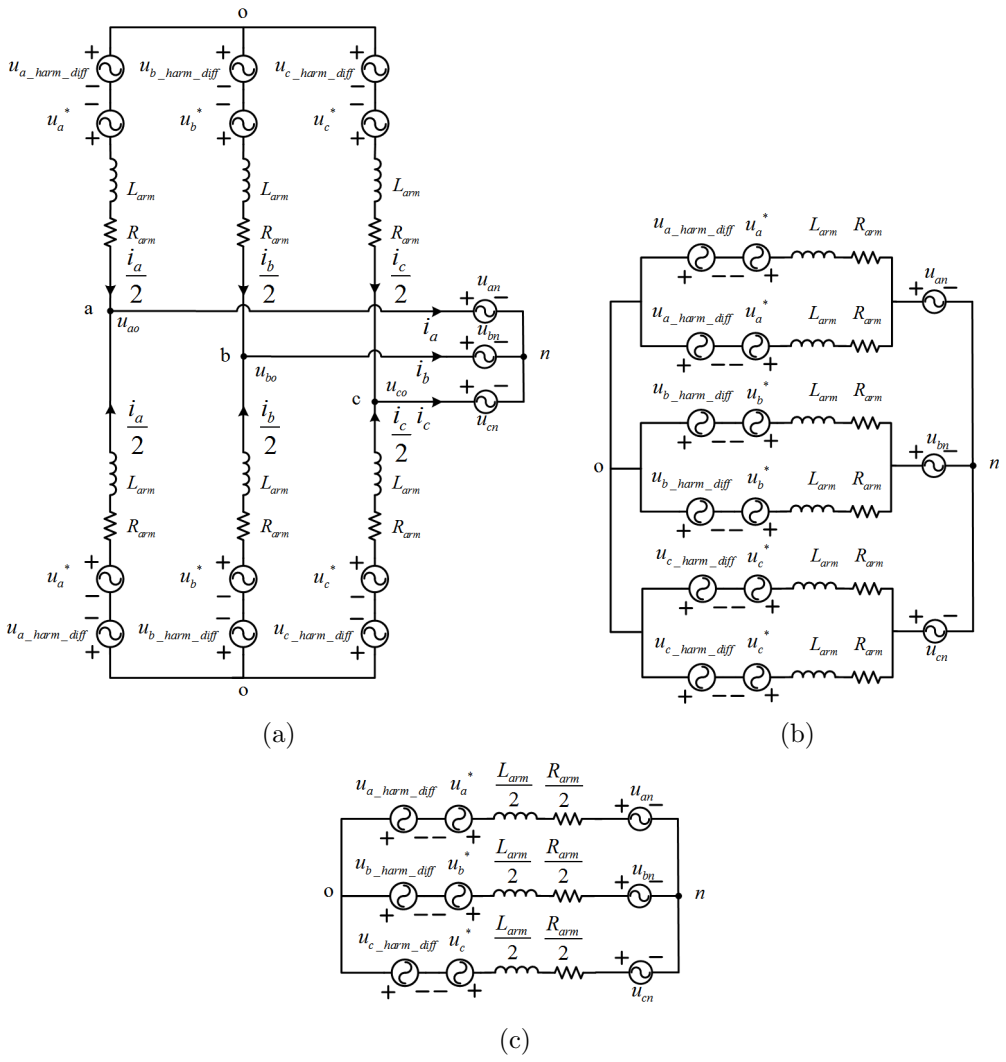


Figure 3.5: Steps of obtaining the output side equivalent circuit of the 3-phase MMC: (a) Original MMC circuit; (b) Paralleled arm circuit; (c) Output side equivalent circuit.

upper and lower arms in this circuit can be assumed as two parallel-connected AC voltage sources with the same amplitude and phase, connecting with equivalent impedance, as shown in Figure 3.5 (b) and (c). In addition to the voltage source $u_x{}^*$, the differential-mode harmonics also exist in the output side equivalent circuit, which contribute to the output voltage distortion.

3.4 Control system for the MMC

Besides the regulation of output power flow, the internal dynamics of the MMC have to be controlled to ensure the stable operation and better performance. Although the advanced control methods such as Model Predictive Control (MPC) [74–81] and nonlinear control [82–84] are found in recent literature , the so called cascaded control schemes are still the mostly adopted ones in MMC controller design [22,52,72,82,85,86]. In this section, only the cascaded control strategy will be discussed in details, whose basic structure is presented in Figure 3.6, including output control, inner differential current control, capacitor voltage averaging and balancing, etc. The capacitor voltage balancing block can be either in front of or behind the modulation scheme, depending on the sorting-algorithm-based or active-control-based voltage balancing methods employed in the control system.

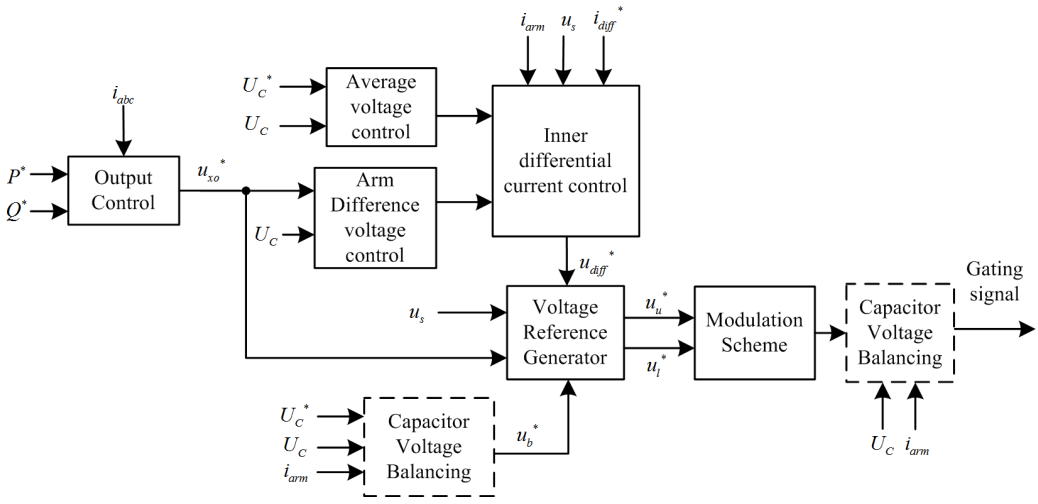
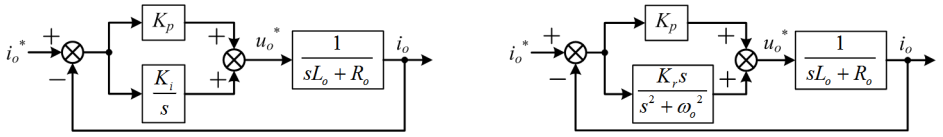


Figure 3.6: Block diagram of the control scheme of the MMC.



(a) (b)

Figure 3.7: Output current control using: (a) A PI controller; (b) A PR controller.

3.4.1 MMC output current control

The control of the MMC output current is one of the most essential components in the MMC control blocks, which is quite similar with control blocks for voltage source converters with other topologies rather than MMCs. It can be implemented independently in each phase based on per-phase average model, and then extended to any arbitrary number of phases. Normally, a proportional-integral (PI) or proportional-resonant (PR) controller can be used to regulate the output current according to the current commands, as presented in Figure 3.7. The output of the current controller is the output voltage reference $u_{xo}{}^*$. The output voltage of the MMC can be yielded as

$$u_{xo} = u_{xo}{}^* - \frac{L_{arm}}{2}\frac{di_x}{dt} - \frac{R_{arm}}{2}i_x \tag{3.31}$$

3.4.2 Inner differential current control

The inner differential current control is intimately linked to the capacitor voltage control and the power balancing between the input and output sides of the MMC. The control block for the inner differential current is illustrated in Figure 3.8. According to equation (2.14), i_{diffx} can be controlled by legitimately adjusting the voltages u_{ux} and u_{lx} [72] to regulate the voltage u_{diffx} across the arm inductance and resistance. The differential current reference $i_{diffx}{}^*$ is comprised of three components, i.e. a current reference $i_{diffx,pb}{}^*$ having the same frequency and phase angle with the input voltage for active power balance, a current refer-

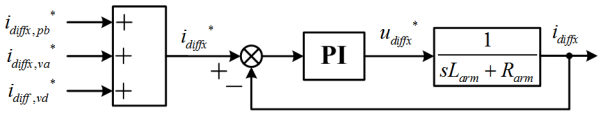


Figure 3.8: Block diagram of the control scheme of the MMC.

ence $i_{diffx,va}{}^*$ for voltage averaging control to maintain the sub-module capacitor voltages at the same level [85], and a current reference $i_{diffx,vd}{}^*$ having the same frequency and phase angle as the output voltage for the differential voltage control between the upper and lower arms [87]. $i_{diffx,pb}{}^*$ can be determined according to (3.12) and (3.13), depending on the input source of the MMC. Both $i_{diffx,va}{}^*$ and $i_{diffx,vd}{}^*$ are generated from the inner capacitor voltage control loops and will be discussed in the next subsection. A current controller, e.g. the PI controller in Figure 3.8, is adopted to regulate the inner differential current of the MMC. The output of the controller, $u_{diffx}{}^*$, is the voltage reference that induces the desired differential current. The voltage applied on the arm inductor and resistor can be expressed as

$$u_{diffx} = L_{arm}\frac{di_{cirx}}{dt} + R_{arm}\left(\frac{i_s}{3} + i_{cirx}\right) = \frac{u_s}{2} - \frac{u_{ux} + u_{lx}}{2} \tag{3.32}$$

Combining equation (3.31) and (3.32), the inserted voltage in the upper and lower arms can be rewritten as

$$\begin{cases} u_{ux} = \dfrac{u_s}{2} - u_{xo} - u_{diffx} \\ u_{lx} = \dfrac{u_s}{2} + u_{xo} - u_{diffx} \end{cases} \tag{3.33}$$

The output phase voltage of the MMC yielded by (3.31) will not be affected by substituting (3.33) into (3.31), which means that u_{diffx} will not influence the output voltage and the controls for inner differential current and output voltage are decoupled.

3.4.3 Inner capacitor voltage control

Besides the output and differential currents regulation, the sub-module capacitor voltages are also controlled for the stable operation of the MMC. The capacitor voltage averaging and differential voltage control are achieved by the voltage controllers given in Figure 3.9. The average capacitor voltage of sub-modules in the same phase leg can be adjusted by the active power difference between the input and output sides of the MMC, with the help of the $i_{diffx,va}{}^*$ term in the inner differential current. The output of the average voltage control can be expressed as

$$i_{diffx,va}{}^* = \left(U_C{}^* - \frac{\bar{u}_{Cux} + \bar{u}_{Clx}}{2}\right)\left(K_p + \frac{K_i}{s}\right) \tag{3.34}$$

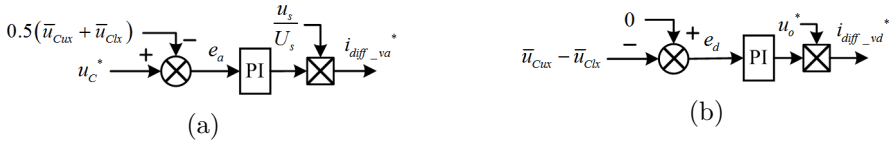


Figure 3.9: Capacitor voltage controls: (a) Capacitor voltage averaging; (b) Differential voltage control.

$$\begin{cases} \bar{u}_{Cux} = \dfrac{1}{N}\displaystyle\sum_{k=1}^{N} u_{Cuxk} \\ \bar{u}_{Clx} = \dfrac{1}{N}\displaystyle\sum_{k=1}^{N} u_{Clxk} \end{cases} \tag{3.35}$$

where $\bar{u}_{Cux}$ and $\bar{u}_{Clx}$ are the average voltages across the capacitors in the upper and lower arms in phase x respectively, and K_p and K_i are the gains for the PI controller. u_{Cuxk} and u_{Clxk} are the voltages across the k^{th} capacitor in corresponding arms.

Furthermore, the component having a frequency of ω_o in the differential current can transfer energy between the upper and lower arms in per phase leg, as discussed in Section 3.2.6, which can be used to control the differential voltage between the upper and lower arms. The differential voltage control loop is presented in Figure 3.9 (b). The output of the differential voltage control can be expressed as

$$i_{diffx,vd}{}^{*} = (\bar{u}_{Cux} - \bar{u}_{Clx})\left(K_p + \frac{K_i}{s}\right) \tag{3.36}$$

Both the outputs of the average voltage and differential voltage control loops ($i_{diffx,va}{}^{*}$ and $i_{diffx,vd}{}^{*}$) are utilized as parts of the inner differential current reference, as indicated in Figure 3.8.

3.4.4 Capacitor voltage balancing

In the normal operation of an MMC, sub-modules are constantly inserted into and bypassed from the main circuit. The current flows in each arm will charge or discharge these inserted capacitors. In practice, it is not possible to charge or discharge these capacitors equally due to the unequal capacitor parameters, PWM pattern, harmonics, dead time, etc. In order to keep the sub-module capacitors on the same voltage level to avoid the distorted output and device damage caused by extremely high voltage across the sub-module capacitors, special efforts have

to be devoted on sub-module capacitor voltage balancing. The widely employed voltage balancing methods can be grouped into two distinct control philosophies, i.e., (a) sorting methods for sub-module capacitor voltage balancing based on a global controller, originally introduced in [17]; (b) individual control methods of each sub-module capacitor voltage with a Phase-shifted PWM approach, as firstly developed in [85]. Both these two philosophies have their own advantages and drawbacks in terms of switching frequency, computational burden, and hardware implementation, resulting in many variations for capacitor voltage balancing. Some other balancing methods with reduced number of voltage sensors or without capacitor voltage measurement are recently proposed in [88, 89].

Sub-module capacitor voltage balancing based on sorting methods

The sorting algorithm based capacitor voltage balancing can be applied in all modulation schemes. The basic idea of sorting methods for capacitor voltage balancing is demonstrated in Figure 3.10. The number of sub-modules should be

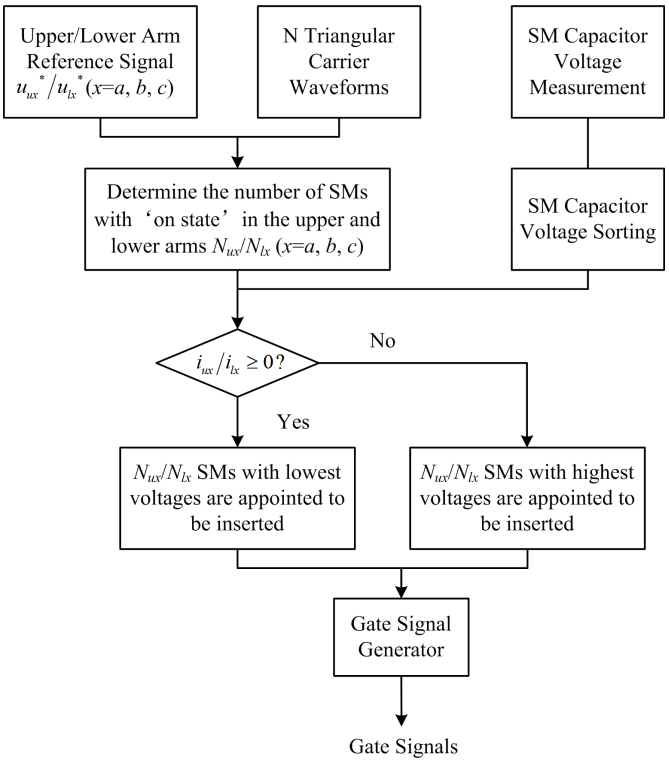


Figure 3.10: Block diagram of the sorting method based voltage balancing.

inserted into each arm is obtained based on the reference signal and the modulation scheme, i.e., N_{ux} and N_{lx}. The voltage across each capacitor in the MMC and arm current are measured periodically in each sampling interval. These sub-modules are sorted in a descending or ascending way based on their capacitor voltages. According to the basic operation described in Section 2.2.2, if the arm current is positive, N_{ux} or N_{lx} sub-modules with lowest capacitor voltages will be inserted into the upper or lower arms to be charged. On the other hand, if the arm current is negative, N_{ux} or N_{lx} sub-modules with highest capacitor voltages will be inserted into the upper or lower arms to be discharged. By applying this sorting method in each control period, the capacitor voltages of sub-modules are passively balanced [17, 90–93].

The balancing algorithm has to be executed in each control cycle to balance the capacitor voltage effectively. Therefore, even if the number of inserted sub-modules in each arm is the same in adjacent control cycles, some unnecessary switching actions of devices in this arm might still be performed due to the balancing algorithm. This phenomenon leads to relatively higher switching frequency of devices and consequently higher switching losses. In order to address this issue, modified balancing algorithms that aim to reduce the device switching losses are proposed in [72,91,94]. A capacitor voltage balancing method for a $\pm$350 kV/1000 MW MMC is presented in [95], where a Balancing Adjusting Number is introduced into the sorting-based capacitor voltage balancing algorithm for a relatively low switching frequency. In order to reduce the switching losses of the MMCs in high power applications, an alternating number controller is designed in [96] to make a trade-off between the switching losses and the effectiveness of the capacitor voltage balancing algorithm. By evaluating the charging capabilities of the driving pulses, the capacitor voltage balancing with fundamental sorting frequency is achieved in [97]. In [98], the capacitor average voltage is regulated according to the energy decomposition of the arms, and the capacitor voltage within each arm is balanced using a sorting algorithm after the modulation. In the aforementioned papers, all the capacitor voltages have to be measured and sorted to implement those balancing algorithms. With an increasing number of sub-modules connected in each arm as in HVDC applications, a plenty of voltage sensors are required and make it difficult and costly in hardware implementation. Moreover, the computational burden of synchronization of all voltage measurements and sorting such a huge amount of numbers could be too heavy to be executed in each control cycle. Accordingly, the cost for implementing the sorting-based balancing method is high.

Some index-based selection methods using tables of switching states [99, 100], max-min function based sub-module selection methods [101, 102], and "The tortoise and the hare" sorting method [103] that allow fast sorting algorithms for a large number of sub-modules are accordingly developed.

Sub-module capacitor voltage balancing based on active control

The original idea of the individual voltage control for sub-module capacitors has been reported in [85], where a proportional controller is adopted to slightly adjust the modulation index for each sub-module in order to force the individual sub-module capacitor voltage following the capacitor voltage reference $u_C{}^*$. Phase-shifted PWM modulation scheme is required to implement such individual voltage control. Noting that the capacitor voltage balancing is actually realized by charging or discharging the capacitors with the help of arm currents, the polarities of arm currents are necessary in the voltage balancing control loop. The block diagram of the active capacitor voltage balancing loop for the k^{th} sub-modules in the upper and lower arms is presented in Figure 3.11. $u_{buxk/blxk}{}^*$ is the reference for individual capacitor voltage balancing control and K_b is the gain of a proportional controller. More voltage balancing methods with individual controllers can be found in [98, 105–107]. Predictive control coupled with individual controllers [39] also shows positive results in voltage balancing control. The active control based sub-module capacitor voltage balancing technique is employed in this thesis.

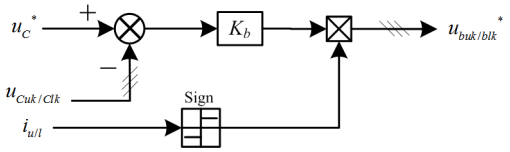


Figure 3.11: Capacitor voltage balancing control.

3.4.5 Modulation schemes for MMCs

The outputs of the output current controller ($u_x{}^*$), the inner differential current controller ($u_{diffx}{}^*$) and the capacitor voltage balancing controller ($u_{buxk/blxk}{}^*$) are

combined to generate the modulation signal for individual sub-module, as

$$\begin{cases} {u_{uxk}}^* = \frac{1}{2}(1 - {u_x}^*) - {u_{diffx}}^* + {u_{buxk}}^* \\ {u_{lxk}}^* = \frac{1}{2}(1 + {u_x}^*) - {u_{diffx}}^* + {u_{blxk}}^* \end{cases} \tag{3.37}$$

The modulation signal in equation (3.37) is fed into the modulation block to generate the gating signals for each switching device. The next task required to control the MMC is to determine the number of sub-modules to be inserted into each arm during every equivalent switching period, according to the modulation signal obtained in equation (3.37). The modulation method defines the switching pattern of the switching devices in sub-modules, in order to produce the desired output voltage and voltage terms for other control objectives. Since the MMCs allow flexible selection of the inserted modules, there are variant modulation methods employed in different applications. The existed modulation methods applied in MMCs are summarized in Figure 3.12, where these modulation techniques are classified into three catalogs, i.e. Staircase based modulation, Carrier based Pulse-Width-Modulation (PWM), and Space vector based PWM schemes.

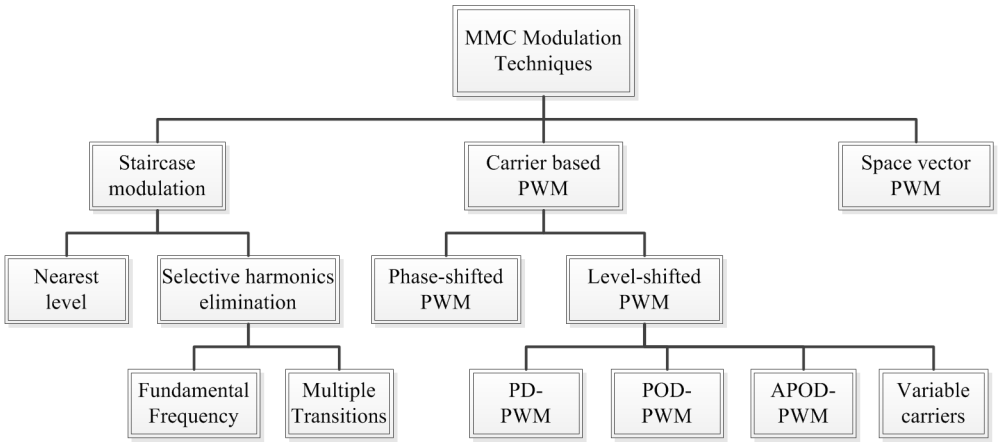


Figure 3.12: Modulation techniques for MMCs.

Many variants of these three catalogs of PWM schemes are developed in recent publications. For MMCs with extremely high number of voltage levels such as MMCs in HVDC applications, square wave or staircase modulation methods are more preferable for low switching frequency [108–110]. The nearest-level modulation and its derivatives reported in [91, 111–115], along with selective harmonic elimination modulation methods [105, 110, 116, 117], are attributed to

staircase modulation schemes. Carrier based sinusoidal pulse width modulation (SPWM) [1, 85, 90, 118–124] techniques are also widely adopted in MMCs, which can be generally classified into two categories: level-shifted and phase-shifted modulations. The space vector pulse-width modulation (SVPWM) [92, 125–129] and other variation of modulation methods [108,130,131] can be also found in different MMC applications. Only the carrier based SPWM method will be detailed in this section since it is adopted in the MMC study in this thesis.

Level-shifted PWM scheme

An MMC with N sub-modules in each arm using level-shifted PWM (LS-PWM) requires N triangular carriers, all having the same frequency and amplitude. The N triangular carriers are vertically dispositioned such that the bands they occupy are contiguous. Figure 3.13 shows the three LS-PWM methods that widely adopted in multilevel converters, i.e., (a) phase disposition (PD), where all carriers are in phase; (b) phase opposite disposition (POD), where all carriers above the zero reference are in phase but in opposition with those below the zero; (c) alternative phase opposite disposition (APOD), where all carriers are alternatively in opposite disposition [1].

Taking PD-PWM methods as an example due to its best harmonic profile, the LS-PWM for an MMC with 4 sub-modules in each arm is illustrated in Figure

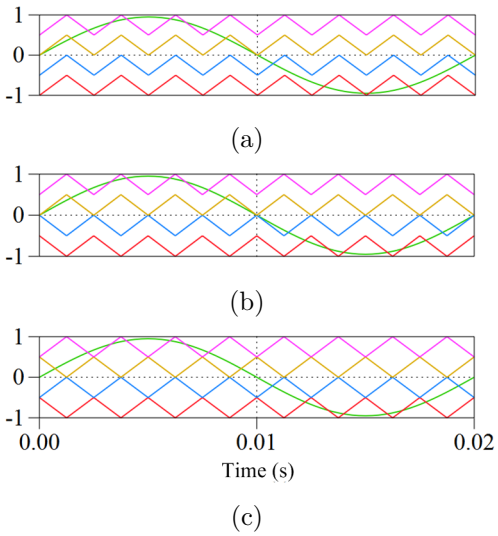


Figure 3.13: Level-shifted PWM: (a) Phase disposition (PD); (b) Phase opposite disposition (POD); (c) Alternative phase opposite disposition (APOD).

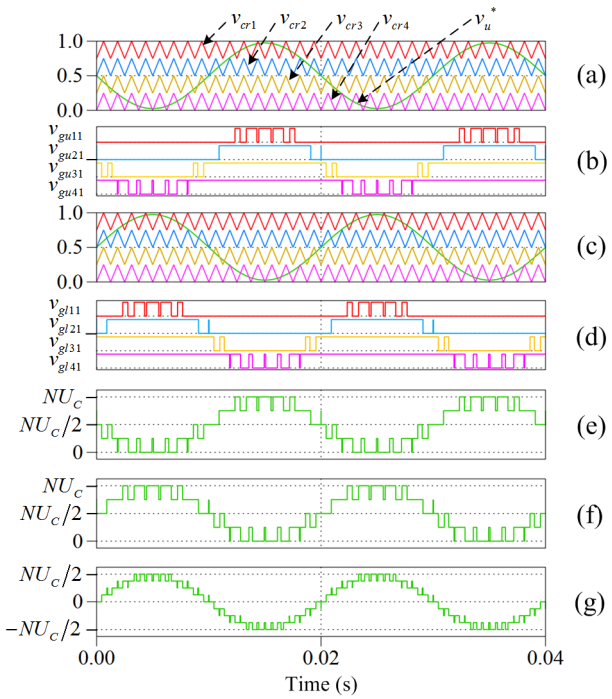


Figure 3.14: PD-PWM for MMCs with 4 SMs in each arm: (a) Modulating signal and triangular carriers for the upper arm; (b) Gating signals for S_1 in upper arm SMs; (c) Modulating signal and triangular carriers for the lower arm; (d) Gating signals for S1 in lower arm SMs; (e) Inserted voltage in the upper arm; (f) Inserted voltage in the lower arm; (g) Output phase voltage.

3.14. The amplitude and frequency of the modulating signal are 0.95 and $f = 50$ Hz respectively. The frequency of these triangular carriers is 800 Hz. In Figure 3.14 (b) and (d), it is clear that the switching frequency of the devices in each sub-module is quite lower than that of the carrier and the switching frequency is not the same for the devices in different sub-modules. In general, the equivalent switching frequency of each arm is the same with the carrier frequency, 800 Hz in this case, as shown in Figure 3.14 (e) and (f). Figure 3.14 (g) indicates that the PD-PWM based equivalent switching frequency of the MMC is $2f_c$ (1600 Hz) and the output phase voltage level is $2N + 1$. The equivalent switching frequency and output voltage level based on POD-PWM and APOD-PWM are f_c and $N + 1$ respectively. PD-PWM provides better harmonic profile in the output voltage but worse one in the inserted phase leg voltage, comparing to POD-PWM and APOD-PWM methods.

In addition to the unequal device switching frequencies, the conduction time

of devices is not evenly distributed either. In order to evenly distribute the power flows and switching and conduction losses in sub-modules, the switching pattern has to rotate among the sub-modules in each arm [90].

Phase-shifted PWM scheme

In general, an MMC with $N+1$ voltage levels requires N triangular carriers if the phase-shifted PWM (PS-PWM) scheme is adopted. In the PS-PWM scheme, all the triangular carriers have the same frequency and the same peak-to-peak amplitude, but there is a phase shift between two adjacent carriers, given by

$$\phi_{cr} = \frac{2\pi}{N} \tag{3.38}$$

The modulating signal is usually a sinusoidal wave with adjustable magnitude, frequency, and phase angle. The modulating signals for sub-modules in each arm

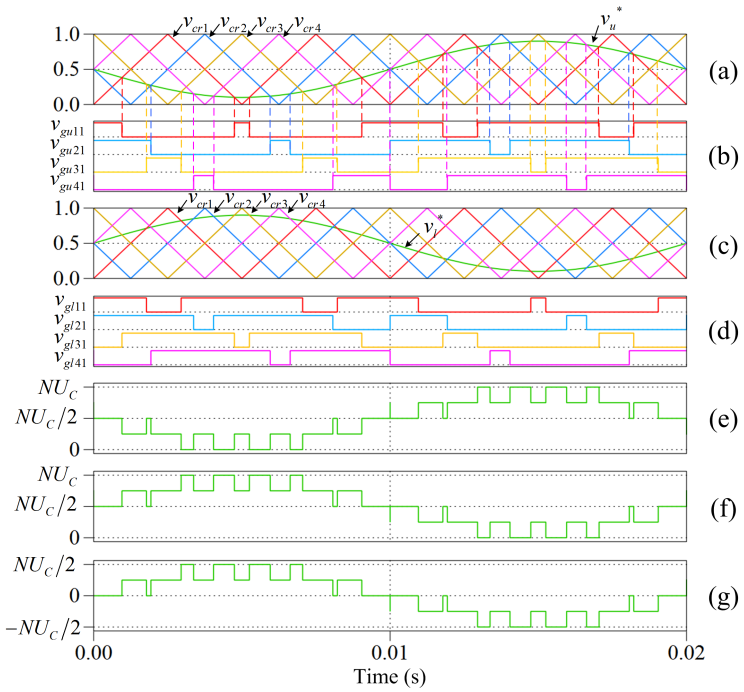


Figure 3.15: Phase-shifted PWM for a five-level MMC: (a) Modulating signal and triangular carriers for the upper arm; (b) Gating signals for S_1 in upper arm sub-modules; (c) Modulating signal and triangular carriers for the lower arm; (d) Gating signals for S_1 in lower arm sub-modules; (e) Inserted voltage in the upper arm; (f) Inserted voltage in the lower arm; (g) Output phase voltage.

are identical and each sub-module in this arm will be individually assigned a phase-shifted triangular carrier. The gate signals are generated by comparing the modulating wave with the carriers.

Figure 3.15 shows the principle of the phase-shifted modulation for an MMC with 4 sub-modules in each arm, where the 4 carriers are required with a 90°phase displacement between any two adjacent carriers. For simplicity, only the gating signal generation in phase a is addressed in Figure 3.15. The reference signal is a sinusoidal wave whose amplitude is 0.8 and frequency is 50 Hz. The modulating signals for the upper and lower arms are generated based on (3.39), as indicated in Figure 3.15 (a) and (c). The carrier v_{cr1}, v_{cr2}, v_{cr3} and v_{cr4} in Figure 3.15 (a) and (c), whose frequency is selected as 200 Hz for clear demonstration purpose, are assigned to one of the sub-modules in each arm respectively. According to the analysis in Section 2.2.1, the gating signals for S_1 and S_2 in each sub-module are complementary in normal operation, and the pattern of the sub-module output voltage is the same with that of the gating signal of S_1 in each sub-module. Therefore, only the gating signals for S_1 in different sub-modules are plotted in Figure 3.15 (b) and (d).

It is clear that the MMC output phase voltage waveform is formed by five voltage levels: $\pm NU_C/2$, $\pm NU_C/4$, 0, as shown in Figure 3.15 (g). Since the switching devices do not switch simultaneously, the magnitude of voltage step change during switching is $NU_C/4$. This leads to a low dv/dt and reduced electromagnetic interference (EMI).

The modulation signals adopted in this subsection for PS-PWM demonstration can be defined as

$$\begin{cases} {u_{ua}}^* = \dfrac{1 - 0.8\cos(100\pi t)}{2} = \dfrac{1 - m_o\cos(\omega_o t + \phi_o + \phi_a)}{2} \\ {u_{la}}^* = \dfrac{1 + 0.8\cos(100\pi t)}{2} = \dfrac{1 + m_o\cos(\omega_o t + \phi_o + \phi_a)}{2} \end{cases} \tag{3.39}$$

The switching function of the i^{th} sub-module in phase x generated by the modulation signals defined in (3.39) and the PS-PWM scheme can be expressed in Fourier series form [118, 119, 132] as

$$\begin{aligned} s_{lxi} =& \frac{1}{2} + \frac{m_o}{2}\cos(\omega_o t + \phi_o + \phi_x) + \sum_{k=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{2}{k\pi}\sin\left[\frac{(k+n)\pi}{2}\right] \times \\ & J_n\left(\frac{m_o k\pi}{2}\right) \times \cos\left\{k\left[\omega_c t + \alpha + (i-1)\frac{2\pi}{N}\right] + n\left(\omega_o t + \phi_o + \phi_x\right)\right\} \end{aligned} \tag{3.40}$$

$$s_{uxi} = \frac{1}{2} - \frac{m_o}{2}\cos(\omega_o t + \phi_o + \phi_x) + \sum_{k=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{2}{k\pi}\sin\left[\frac{(k+n)\pi}{2}\right] \times J_n\left(\frac{m_o k\pi}{2}\right) \times \cos\left\{k\left[\omega_c t + \alpha + \beta + (i-1)\frac{2\pi}{N}\right] + n\left(\omega_o t + \phi_o + \phi_x + \pi\right)\right\} \tag{3.41}$$

where k is the harmonic order of the carrier and n is the harmonic order of the reference. J_n refers to the Bessel function and ω_c is the angular frequency of the carrier. α is the phase displacement between the carrier waves and the modulating signal, and β indicates the angle displacement between the carriers in the upper and lower arms. It is obvious in equations (3.40) and (3.41) that there are unexpected carrier harmonics $k\omega_c$ and side-band harmonics $n\omega_o$ introduced by the PWM pattern of the modulation scheme in the switching functions.

The sum of the switching functions can be denoted as

$$s_{lx} = \frac{N}{2} + \frac{Nm_o}{2}\cos(\omega_o t + \phi_o + \phi_x) + \sum_{i=1}^{N}\sum_{k=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{2}{k\pi}\sin\left[\frac{(k+n)\pi}{2}\right] \times J_n\left(\frac{m_o k\pi}{2}\right) \times \cos\left\{k\left[\omega_c t + \alpha + (i-1)\frac{2\pi}{N}\right] + n\left(\omega_o t + \phi_o + \phi_x\right)\right\} \tag{3.42}$$

$$s_{ux} = \frac{N}{2} - \frac{Nm_o}{2}\cos(\omega_o t + \phi_o + \phi_x) + \sum_{i=1}^{N}\sum_{k=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{2}{k\pi}\sin\left[\frac{(k+n)\pi}{2}\right] \times J_n\left(\frac{m_o k\pi}{2}\right) \times \cos\left\{k\left[\omega_c t + \alpha + \beta + (i-1)\frac{2\pi}{N}\right] + n\left(\omega_o t + \phi_o + \phi_x + \pi\right)\right\} \tag{3.43}$$

Equations (3.42) and (3.43) present normalized multilevel waveforms of inserted voltage in the upper and lower arms by assuming all the sub-module voltage are one. Since

$$\sum_{i=1}^{N}\cos\left((i-1)\frac{2k\pi}{N}\right) = 0, k/N \notin \mathbb{N}^+ = \{1, 2, 3, \cdots\} \tag{3.44}$$

and

$$\begin{aligned}&\sum_{i=1}^{N}\sum_{k/N\in\mathbb{N}^+}\cos\left\{k\left[\omega_c t + \alpha + (i-1)\frac{2\pi}{N}\right] + n\left(\omega_{ox} t + \phi_o + \phi_x\right)\right\} \\ =&N\sum_{k/N\in\mathbb{N}^+}\cos\left[k\left(\omega_c t + \alpha\right) + n\left(\omega_o t + \phi_o + \phi_x\right)\right]\end{aligned} \tag{3.45}$$

the equations (3.42) and (3.43) can be rewritten as

$$\begin{aligned} s_{lx} =& \frac{N}{2} + \frac{Nm_o}{2}\cos(\omega_o t + \phi_o + \phi_x) + \sum_{k/N\in\mathbb{N}^+}\sum_{n=-\infty}^{\infty}\frac{2N}{k\pi}\sin\left[\frac{(k+n)\pi}{2}\right] \\ & \times J_n\left(\frac{m_o k\pi}{2}\right)\times\cos\left[k\left(\omega_c t+\alpha\right)+n\left(\omega_o t+\phi_o+\phi_x\right)\right] \end{aligned} \tag{3.46}$$

$$\begin{aligned} s_{ux} =& \frac{N}{2} - \frac{Nm_o}{2}\cos(\omega_o t + \phi_o + \phi_x) + \sum_{k/N\in\mathbb{N}^+}\sum_{n=-\infty}^{\infty}\frac{2N}{k\pi}\sin\left[\frac{(k+n)\pi}{2}\right] \\ & \times J_n\left(\frac{m_o k\pi}{2}\right)\times\cos\left[k\left(\omega_c t+\alpha+\beta\right)+n\left(\omega_o t+\phi_o+\phi_x+\pi\right)\right] \end{aligned} \tag{3.47}$$

According to the operation principle of the MMC, the normalized output voltage waveform of phase x can be obtained as

$$\begin{aligned} s_{xo} =& \frac{s_{lx}-s_{ux}}{2} \\ =& \frac{Nm_o}{2}\cos(\omega_o t + \phi_o + \phi_x) + \sum_{k/N\in\mathbb{N}^+}\sum_{n=-\infty}^{\infty}\frac{2N}{k\pi}\sin\left[\frac{(k+n)\pi}{2}\right]\times J_n\left(\frac{m_o k\pi}{2}\right) \\ & \times\sin\left[k\left(\omega_c t+\alpha+\frac{\beta}{2}\right)+n\left(\omega_o t+\phi_o+\phi_x+\frac{\pi}{2}\right)\right]\sin\left(\frac{k\beta+n\pi}{2}\right) \end{aligned} \tag{3.48}$$

Similarly, the switching function of the inserted sub-modules in phase leg x is

$$\begin{aligned} s_{x,leg} =& s_{lx}+s_{ux} = N + \sum_{k/N\in\mathbb{N}^+}\sum_{n=-\infty}^{\infty}\frac{4N}{k\pi}\sin\left[\frac{(k+n)\pi}{2}\right]\times J_n\left(\frac{m_o k\pi}{2}\right)\times \\ & \cos\left\{k\left[\omega_c t+\alpha+(i-1)\frac{2\pi}{N}+\frac{\beta}{2}\right]+n\left(\omega_o t+\phi_o+\phi_x+\frac{\pi}{2}\right)\right\} \\ & \times\cos\left(\frac{k\beta+n\pi}{2}\right) \end{aligned} \tag{3.49}$$

From equations (3.46) to (3.49), some conclusions can be obtained as follows:

1. The frequency of all carrier harmonics that appear in s_{lx}, s_{ux}, s_{xo} and $s_{x,leg}$ are at least N times of the carrier frequency ω_c;

2. The remaining fundamental and harmonic contents of reference will contribute to the side-bands to the carrier harmonics;

3. If $N\omega_c$ is an integer multiple of ω_o, the output switching function will not contain sub-harmonics or other frequency components which are non-integer multiples of the fundamental frequency;

4. The amplitudes of the carrier harmonics and side-band harmonics in s_x and $s_{x,leg}$ are mainly defined by the terms of $4N/k\pi$ and J_n, which are independent of N because k/N is a positive integer;

5. The presence of the harmonics and their side-bands in s_x and $s_{x,leg}$ is mainly determined by the terms of $\sin[(k+n)\pi/2]$, $\sin[(k\beta+n\pi)/2]$, and $\cos[(k\pi+n\pi)/2]$;

6. As the dominate harmonics in the MMC output waveform represents the converter switching frequency, the equivalent switching frequency ω_{eq} of the MMC can be decided according to equation (3.48) as follows:

   (a) $\boldsymbol{N\omega_c}$ **:** β is selected as $\beta = \pi$, so that the harmonics in equation (3.48) are canceled when $k+n$ is an even number. In this case, the output voltage level is $N+1$. No harmonic is introduced by the PS-PWM in $s_{x,leg}$, since the harmonics in equation (3.49) are always zero.

   (b) $\boldsymbol{2N\omega_c}$ **:** β is selected as $\beta = 0$, equation (3.48) can be rewritten as in equation (3.50). The harmonics in s_{xo} are zero when n is an even

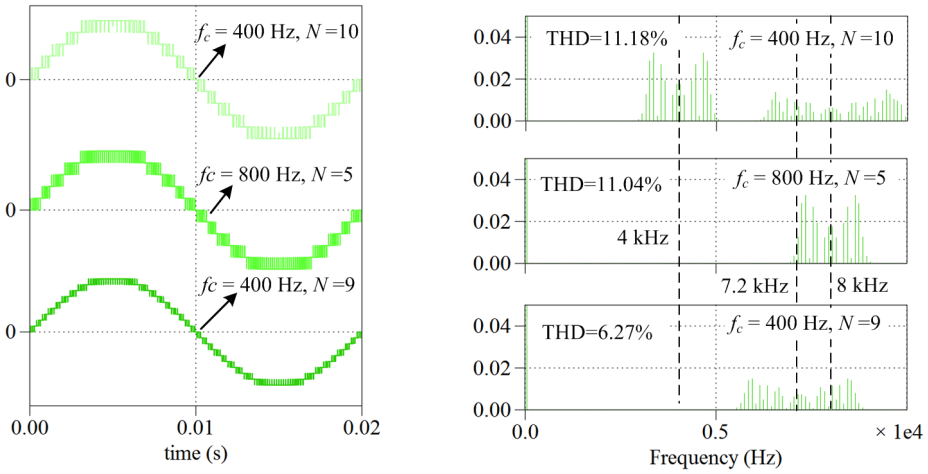


Figure 3.16: MMC outputs with different f_c and N: (a) Output phase voltage; (b) FFT of the output voltage.

integer or both k and n are odd integers. This feature means that if odd number of sub-modules are connected in each arm, the harmonics and side-bands are pushed to the frequency of $2N\omega_c$, $4N\omega_c$, ..., which is twice of that when N is chosen as an even number. By selecting N as an odd number, the equivalent switching frequency of the MMC is $2N\omega_c$, the output voltage level is $2N+1$, and the output harmonics caused by the PS-PWM is significantly reduced as well. On the other hand, the odd order carrier harmonics can be found in $s_{x,leg}$. The simulation results of this feature is shown in Figure 3.16.

β is selected as $\beta = \pi/N$ and N is an even integer, the harmonics in output voltage and inserted leg voltage are similar with those in the case above.

$$s_{xo} = \frac{Nm_o}{2}\cos(\omega_o t + \phi_o + \phi_x) + \sum_{k/N\in\mathbb{N}^+}\sum_{n=-\infty}^{\infty}\frac{2N}{k\pi}\sin\left[\frac{(k+n)\pi}{2}\right]\times J_n\left(\frac{m_o k\pi}{2}\right)\times\sin\left[k\omega_c t + n\left(\omega_o t + \phi_o + \phi_x + \frac{\pi}{2}\right)\right]\sin\left(\frac{n\pi}{2}\right) \tag{3.50}$$

7. In the case of equivalent switching frequency is $2N\omega_c$, the number of sub-modules inserted into each phase leg are no longer always equal to N. Consequently, the carrier harmonics in the inserted leg voltage as well as inner differential current will be higher. In other words, the odd order carrier-frequency harmonics are shifted from the output voltage to the inserted leg voltage.

The aforementioned analysis can be summarized as in Table 3.1. It is clear that the total amount of harmonics caused by the PS-PWM in the output phase voltage and inserted leg voltage is not changed by applying different angle displacements into the carriers for the upper and lower arm and selecting N as an even or odd number. The PS-PWM methods that provide $2N+1$ output voltage levels and $2N\omega_c$ will reduce the harmonics in output phase voltage and then inevitably introduce more harmonics in the inserted leg voltage and the inner differential current. The reduced harmonics in the output voltage will be pushed into the inserted leg voltage consequently resulting in higher inner current harmonics.

Table 3.1: Harmonics in output phase voltage and inserted leg voltage caused by PS-PWM

β	N	n	Output voltage harmonic / order to $N\omega_c$	Inserted voltage harmonic / order to $N\omega_c$	ω_{eq}	Output voltage level
π	Even	Even	No	No	–	–
		Odd	Yes/1, 2, ...	No	$N\omega_c$	$N+1$
	Odd	Even	Yes/1, 3, ...	No	$N\omega_c$	$N+1$
		Odd	Yes/2, 4, ...	No	$2N\omega_c$	$N+1$
0	Even	Even	No	No	–	–
		Odd	Yes/1, 2, ...	No	$N\omega_c$	$N+1$
	Odd	Even	No	Yes/1, 3, ...	–	–
		Odd	Yes/2, 4, ...	No	$2N\omega_c$	$2N+1$
$\frac{\pi}{N}$	Even	Even	No	No	–	–
		Odd	Yes/2, 4, ...	Yes/1, 3, ...	$2N\omega_c$	$2N+1$
	Odd	Even	Yes/1, 3, ...	No	$N\omega_c$	$N+1$
		Odd	Yes/2, 4, ...	No	$2N\omega_c$	$N+1$

3.5 Summary

This chapter starts with a general model for MMCs used as single-phase to three-phase AC/AC converters and three-phase inverters, i.e., MMCs connect to a common DC bus or a common AC bus. The steady state analysis for the general MMC is performed in terms of the sub-module capacitor voltage, inserted arm voltage, phase and output voltages, and circulating current. From the steady state analysis, it is concluded that

- The DC component of the capacitor current contributes to the shifting of the capacitor average voltage, which should be zero in the steady state.
- There are voltage ripples across each sub-module capacitor, which is proportional to output current and inversely proportional to the sub-module capacitance and angular frequencies. Such voltage ripples might be unacceptable in normal operation if the frequencies of the common bus voltage and the MMC output voltage are close to each other or close to zero.
- Harmonics with frequencies of ω_s, $3\omega_s$, and $2\omega_o \pm \omega_s$ exist in the phase leg voltage and harmonics with frequencies of ω_o, $\omega_o \pm \omega_s$, and $3\omega_o$ exist in the output voltage.

- The harmonics in the phase leg voltage induce circulating current in each phase leg. The circulating current with frequency ω_o can be used to transfer the energy between the upper and lower arms.

The equivalent circuits for the three-phase MMC are presented according to the steady state analysis.

Per-phase control system are accordingly introduced based on the MMC model and the steady state analysis. Such per-phase control system can be conveniently extended to any number of phases without significant modification. The control loops for the MMC output current, inner differential current, capacitor voltage averaging, differential voltage between the upper and lower arms, and capacitor voltage balancing are discussed in Section 3.4. Two types of capacitor voltage balancing strategies that are mostly adopted in MMC systems, i.e. the sorting algorithm based method and the active control method are reviewed in that section.

The outputs of these control loops are combined to generate the modulating signals for each sub-module. Such modulating signal is fed into a modulation block to generate the gating signals for each switching device. The general modulation schemes for MMCs, such as Nearest-level modulation, SPWM, and SVPWM, are briefly reviewed in Section 3.4.5. The carrier based SPWM, especially the phase-shifted PWM scheme, is introduced in details since it is adopted in the MMC system in this thesis. The switching functions under the PS-PWM are analyzed with the help of the double Fourier Transform in Section 3.4.5. According to the analysis, the equivalent switching frequencies, output levels, and switching harmonics can be determined by the phase displacement of carriers and the number of sub-modules in each arm, once the carrier frequency is selected. The harmonics introduced by the carrier in the PS-PWM scheme can be arbitrarily put in the phase voltage or output voltage of the MMC by selecting different phase displacement of the carriers in the upper and lower arms and the number of sub-modules in each arm, as presented in Table 3.1.

Chapter 4

Repetitive Control based Circulating Current Suppression for Modular Multilevel Converters

4.1 Introduction

A well-known problem within an MMC system is that the differential current in a phase leg may be distorted by low order circulating harmonics as mentioned in Section 3.2.6. These circulating harmonics are introduced by inherent mismatch between the inserted voltage of each phase leg and the common bus voltage. Such low order harmonics not only increase the current stress of semiconductors and introduce more power losses in phase legs, but also in turn bring disturbances on the sub-module capacitor voltage, which consequently deteriorate the performance of the MMC system [71, 73, 85, 133].

In most applications, the harmonics in the differential current of an MMC are undesirable from efficiency and controllability points of view, except for some special applications such as capacitor voltage ripple shaping [134, 135] and motor drives in low frequency operations [22, 54, 55, 136]. Nevertheless, it is difficult to find a practical passive method such as filters with passive components to mitigate these low-order harmonics in the differential current. Alternatively, some active harmonic suppression methods were proposed in recent literature such as

compensating the inserted voltage in each phase leg based on open-loop control strategies [86,137] and injecting adequate harmonics by feedforward control to reduce the second order harmonics in the differential current [133]. However, these methods highly rely on accurate MMC models and are sensitive to the disturbance and model parameter variation. Feedback control in the d-q or rotating frames were proposed in [72, 138, 139] for second order harmonic suppression of a three phase MMC system. Proportional resonant (PR) controllers can also be adopted to deal with harmonics under both symmetric and unbalanced load conditions as discussed in [42, 140]. However, one evident limitation of those methods is that they can only cope with specific order harmonics, depending on the controller design. Recently, plug in repetitive controllers, which have been widely used in single- and multi-phase PWM inverters [141–143], are employed in [144, 145] to eliminate multiple harmonics in the differential current of MMC systems. However, the circulating current harmonics analysis in Section 4.2 shows that the harmonics in the differential current of an MMC are dominated by only even order components. Therefore, a repetitive controller being able to suppress even harmonics is sufficient in such applications.

This chapter aims to address an active suppression method of the circulating current in an MMC based inverter. A thorough study of the circulating current characteristics in an MMC inverter is firstly presented. Next, the basic principles of a repetitive controller is introduced in Section 4.3, where detailed mathematical analysis and an explicit design method regarding the time advance unit in the phase lead filter in repetitive controls are presented. In addition to ensuring the overall system stability, the repetitive controller design method also suggests the stability range and estimates the best time advance unit that can provide the largest phase margin and excellent closed-loop performance. Then, an improved repetitive controller being able to exclusively cope with the even-order signals is proposed according to the circulating current characteristics for the sake of perfect even harmonics suppression in the differential current and the almost doubled repetitive controller dynamics. The proposed repetitive controller has the same performance regarding even-harmonic elimination and system stability as conventional ones. By halving the number of samplings stored in one repetitive cycle, it possesses additional benefits of less memory occupation, halved repetitive controller delay period, faster convergence speed, and doubled low-frequency gain, according to the comprehensive frequency characteristics analysis in Section 4.4.2. It also features greater tolerance for system frequency variation because of

the wider bandwidths at specific frequencies. Full design details of the even harmonics based repetitive control scheme, including selecting the number of error samples stored in each repetitive cycle to deal with the harmonics with even-order frequencies, determining the crossover frequencies of the low pass filters in the repetitive controller according to the harmonic contents, and selecting controller parameters for the repetitive controller, are provided in Section 4.5.2. The investigation of the controller convergence speed, robustness against the system parameter variation, and system stability is performed.

The effectiveness and the validity of the even-harmonic repetitive control scheme are confirmed in both simulations and experiments in Section 4.5.3 and 4.5.4. The results show that the proposed repetitive controller, compared with the PI and PR controllers, provides better circulating harmonics suppression capability. On the other hand, in comparison to the conventional repetitive controller, the dynamics of the proposed repetitive controller is almost doubled in the startup process and during reference or load step changes. Moreover, the even-harmonic repetitive controller also offers better harmonic suppression when there is a 5% system frequency deviation, compared with that of the conventional ones.

4.2 MMC circulating current harmonics analysis

In the analysis in this section, a three-phase MMC inverter connected to a common DC bus as the system input is considered. The input voltage is $u_s = U_{DC}$. The MMC circulating current harmonics analysis is based on the work introduced in [71]. It is presented in this section to explain the basis of the circulating current harmonics in an MMC. The equations (3.7) and (3.8) can be written as

$$\begin{cases} n_{ux} = \dfrac{1 - m_o \cos(\omega_o t + \phi_o + \phi_x)}{2} = \dfrac{1 - m_o \cos(\omega_o t + \theta_{ox})}{2} \\ n_{lx} = \dfrac{1 + m_o \cos(\omega_o t + \phi_o + \phi_x)}{2} = \dfrac{1 + m_o \cos(\omega_o t + \theta_{ox})}{2} \end{cases} \tag{4.1}$$

$$i_{cirx} = \sum_{k \in \mathbb{N}} I_{cirxk} \cos\left(k\omega_o t + \phi_{cirxk}\right) \tag{4.2}$$

The ripples of the capacitor current can be expressed as

$$\begin{aligned}\tilde{i}_{Cux} =& \frac{1}{2}\left[\frac{I_o\cos\left(\omega_o t+\theta_{ox}+\phi_{i_o}\right)}{2}+\sum_{k\in\mathbb{N}} I_{cirxk}\cos(k\omega_o t+\phi_{cirxk})\right] \\ &-\frac{m_o}{8}\Bigg\{m_o I_o\cos(\phi_{i_o})\cos\left(\omega_o t+\theta_{ox}\right)+I_o\cos\left(2\omega_o t+2\theta_{ox}+\phi_{i_o}\right) \\ &+2\sum_{k\in\mathbb{N}} I_{cirxk}\cos\left[(k+1)\,\omega_o t+\theta_{ox}+\phi_{cirxk}\right] \\ &+2\sum_{k\in\mathbb{N}} I_{cirxk}\cos\left[(k-1)\,\omega_o t-\theta_{ox}+\phi_{cirxk}\right]\Bigg\}\end{aligned} \tag{4.3}$$

$$\begin{aligned}\tilde{i}_{Clx} =& \frac{1}{2}\left[-\frac{I_o\cos\left(\omega_o t+\theta_{ox}+\phi_{i_o}\right)}{2}+\sum_{k\in\mathbb{N}} I_{cirxk}\cos(k\omega_o t+\phi_{cirxk})\right] \\ &+\frac{m_o}{8}\Bigg\{m_o I_o\cos(\phi_{i_o})\cos\left(\omega_o t+\theta_{ox}\right)-I_o\cos\left(2\omega_o t+2\theta_{ox}+\phi_{i_o}\right) \\ &+2\sum_{k\in\mathbb{N}} I_{cirxk}\cos\left[(k+1)\,\omega_o t+\theta_{ox}+\phi_{cirxk}\right] \\ &+2\sum_{k\in\mathbb{N}} I_{cirxk}\cos\left[(k-1)\,\omega_o t-\theta_{ox}+\phi_{cirxk}\right]\Bigg\}\end{aligned} \tag{4.4}$$

It should be noted that the last term in both (4.3) and (4.4) is a DC value $2I_{cirx1}\cos\left(\theta_{ox}-\phi_{cirxk}\right)$ if $k=1$, which reveals that the fundamental circulating current is zero in the steady-state and can be utilized to eliminate the capacitor voltage difference between the upper and lower arms. In steady state, equations (4.3) and (4.4) can be rewritten as

$$\begin{aligned}\tilde{i}_{Cux} =& \frac{1}{2}\left[\frac{I_o\cos\left(\omega_o t+\theta_{ox}+\phi_{i_o}\right)}{2}+\sum_{k\in\mathbb{N}} I_{cirxk}\cos(k\omega_o t+\phi_{cirxk})\right] \\ &-\frac{m_o}{8}\Bigg\{m_o I_o\cos(\phi_{i_o})\cos\left(\omega_o t+\theta_{ox}\right) \\ &+I_o\cos\left(2\omega_o t+2\theta_{ox}+\phi_{i_o}\right) \\ &+2\sum_{k\in\mathbb{N}} I_{cirxk}\cos\left[(k+1)\,\omega_o t+\theta_{ox}+\phi_{cirxk}\right] \\ &+2\sum_{k=2}^{k=\infty} I_{cirxk}\cos\left[(k-1)\,\omega_o t-\theta_{ox}+\phi_{cirxk}\right]\Bigg\}\end{aligned} \tag{4.5}$$

$$\begin{aligned}\tilde{i}_{Clx} =& \frac{1}{2}\left[-\frac{I_o\cos\left(\omega_o t+\theta_{ox}+\phi_{i_o}\right)}{2}+\sum_{k\in\mathbb{N}} I_{cirxk}\cos(k\omega_o t+\phi_{cirxk})\right]\\ &+\frac{m_o}{8}\Bigg\{m_o I_o\cos(\phi_{i_o})\cos\left(\omega_o t+\theta_{ox}\right)\\ &-I_o\cos\left(2\omega_o t+2\theta_{ox}+\phi_{i_o}\right)\\ &+2\sum_{k\in\mathbb{N}} I_{cirxk}\cos\left[\left(k+1\right)\omega_o t+\theta_{ox}+\phi_{cirxk}\right]\\ &+2\sum_{k=2}^{k=\infty} I_{cirxk}\cos\left[\left(k-1\right)\omega_o t-\theta_{ox}+\phi_{cirxk}\right]\Bigg\}\end{aligned} \tag{4.6}$$

The AC voltage applied on the arm inductor and resistor in each arm can be expressed as

$$\begin{aligned}\tilde{u}_{diffx} =& -\frac{N}{16\omega_o C_{SM}}\Bigg\{\left(8+{m_o}^2\right)I_{cirx1}\sin(\omega_o t+\phi_{cirx1})\\ &+{m_o}^3 I_o\cos\left(\phi_{i_o}\right)\sin\left(2\omega_o t+2\theta_{ox}\right)-3m_o I_o\sin\left(2\omega_o t+2\theta_{ox}+\phi_{i_o}\right)\\ &+\sum_{k=2}^{k=\infty}\frac{8\left(k^2-1\right)+4{m_o}^2k^2}{k\left(k^2-1\right)}I_{cirxk}\sin\left(k\omega_o t+\phi_{cirxk}\right)\\ &+2{m_o}^2\sum_{k=3}^{k=\infty}\frac{I_{cirx(k-2)}\sin\left[k\omega_o t+2\theta_{ox}+\phi_{cirx(k-2)}\right]}{k-1}\\ &+2{m_o}^2\sum_{k=1}^{k=\infty}\frac{I_{cirx(k+2)}\sin\left[k\omega_o t-2\theta_{ox}+\phi_{cirx(k+2)}\right]}{k+1}\Bigg\}\end{aligned} \tag{4.7}$$

The matrix representation of these AC components in $\tilde{u}_{diffx}$ and i_{cirx} can be derived. For simplification, complex representation of the current can be defined as

$$i_x = \mathrm{Re}\left(I_o e^{j(\omega_o t+\theta_{ox}+\phi_{i_o})}\right) \tag{4.8}$$

$$i_{cirxk} = \mathrm{Re}\left(I_{cirxk} e^{j(k\omega_o t+\phi_{cirxk})}\right) \tag{4.9}$$

Matrices E_{odd}, E_{even}, X_{odd}, and X_{even} are defined as

$$E_{odd} = \begin{bmatrix} e^{j1\omega_o t} & & & \\ & e^{j3\omega_o t} & & \\ & & e^{j5\omega_o t} & \\ & & & \ddots \end{bmatrix} \tag{4.10}$$

$$E_{even} = \begin{bmatrix} e^{j2\omega_o t} & & & \\ & e^{j4\omega_o t} & & \\ & & e^{j6\omega_o t} & \\ & & & \ddots \end{bmatrix} \tag{4.11}$$

$$X_{odd} = -\frac{N}{16\omega_o C_{SM}} \begin{bmatrix} -j(8+{m_o}^2) & c_1 & 0 & 0 & \cdots \\ a_3 & b_3 & c_3 & 0 & \cdots \\ 0 & a_5 & b_5 & c_5 & 0 \\ \vdots & 0 & \ddots & \ddots & \ddots \end{bmatrix} \tag{4.12}$$

$$X_{even} = -\frac{N}{16\omega_o C_{SM}} \begin{bmatrix} -jm_o\left[3e^{j\phi_{i_o}} - {m_o}^2\cos(\phi_{i_o})\right] & b_2 & c_2 & 0 & 0 & 0 \\ 0 & a_4 & b_4 & c_4 & 0 & 0 \\ 0 & 0 & a_6 & b_6 & c_6 & 0 \\ 0 & 0 & 0 & \ddots & \ddots & \ddots \end{bmatrix} \tag{4.13}$$

where a_k, b_k, and c_k are defined as

$$\begin{cases} a_k = -j\dfrac{2{m_o}^2}{k-1}e^{j(2\theta_{ox})}, & k = 3,4,5,\ldots \\ b_k = -j\dfrac{8\left(k^2-1\right)+4{m_o}^2k^2}{k\left(k^2-1\right)}, & k = 2,3,4,\ldots \\ c_k = -j\dfrac{2{m_o}^2}{k+1}e^{-j(2\theta_{ox})}, & k = 1,2,3,\ldots \end{cases} \tag{4.14}$$

Then the matrix representation of $\tilde{u}_{diffx}$ can be written as

$$E_{odd}X_{odd}\begin{bmatrix} I_{cirx1}e^{j\phi_{cirx1}} \\ I_{cirx3}e^{j\phi_{cirx3}} \\ I_{cirx5}e^{j\phi_{cirx5}} \\ \vdots \end{bmatrix} = \begin{bmatrix} \tilde{U}_{diffx1}e^{j(\omega_o t+\phi_{ux1})} \\ \tilde{U}_{diffx3}e^{j(3\omega_o t+\phi_{ux3})} \\ \tilde{U}_{diffx5}e^{j(5\omega_o t+\phi_{ux5})} \\ \vdots \end{bmatrix} \tag{4.15}$$

$$E_{even}X_{even}\begin{bmatrix} I_o e^{j(\phi_o+\phi_x+\phi_{io})} \\ I_{cirx2}e^{j\phi_{cirx2}} \\ I_{cirx4}e^{j\phi_{cirx4}} \\ \vdots \end{bmatrix} = \begin{bmatrix} \tilde{U}_{diffx2}e^{j(2\omega_o t+\phi_{ux2})} \\ \tilde{U}_{diffx4}e^{j(4\omega_o t+\phi_{ux4})} \\ \tilde{U}_{diffx6}e^{j(6\omega_o t+\phi_{ux6})} \\ \vdots \end{bmatrix} \tag{4.16}$$

where $\tilde{U}_{diffxk}$ and ϕ_{uxk} are the magnitude and phase angle of the k^{th} order component of $\tilde{u}_{diffx}$ respectively.

The even and odd components in the voltage mismatch are decoupled in (4.15) and (4.16). Multiplying both sides of (4.15) and (4.16) with the inverse of E_{odd} and E_{even} respectively, the time-invariant equations relating the currents to the voltages can be expressed as

$$\begin{bmatrix} \tilde{U}_{diffx1}e^{j\phi_{ux1}} \\ \tilde{U}_{diffx3}e^{j\phi_{ux3}} \\ \tilde{U}_{diffx5}e^{j\phi_{ux5}} \\ \vdots \end{bmatrix} = \frac{-N}{16\omega_o C_{SM}} \begin{bmatrix} -j(8+{m_o}^2) & c_1 & 0 & 0 & \cdots \\ a_3 & b_3 & c_3 & 0 & \cdots \\ 0 & a_5 & b_5 & c_5 & 0 \\ \vdots & 0 & \ddots & \ddots & \ddots \end{bmatrix} \begin{bmatrix} I_{cirx1}e^{j\phi_{cirx1}} \\ I_{cirx3}e^{j\phi_{cirx3}} \\ I_{cirx5}e^{j\phi_{cirx5}} \\ \vdots \end{bmatrix} \tag{4.17}$$

$$\begin{bmatrix} \tilde{U}_{diffx2}e^{j(2\omega_o t+\phi_{ux2})} \\ \tilde{U}_{diffx4}e^{j(4\omega_o t+\phi_{ux4})} \\ \tilde{U}_{diffx6}e^{j(6\omega_o t+\phi_{ux6})} \\ \vdots \end{bmatrix} = \frac{-N}{16\omega_o C_{SM}} \times$$

$$\begin{bmatrix} -jm_o\left[3e^{j\phi_{i_o}} - {m_o}^2\cos(\phi_{i_o})\right] & b_2 & c_2 & 0 & 0 & 0 \\ 0 & a_4 & b_4 & c_4 & 0 & 0 \\ 0 & 0 & a_6 & b_6 & c_6 & 0 \\ 0 & 0 & 0 & \ddots & \ddots & \ddots \end{bmatrix} \begin{bmatrix} I_o e^{j(2\theta_{ox})} \\ I_{cirx2}e^{j\phi_{cirx2}} \\ I_{cirx4}e^{j\phi_{cirx4}} \\ \vdots \end{bmatrix} \tag{4.18}$$

Applying $\tilde{u}_{diffx}$ onto the arm inductance and resistance of the two arms, the circulating current of the phase leg x can be derived. The impedance matrix can be written as

$$Z_{odd} = 2\begin{bmatrix} R_{arm}+j\omega_o L_{arm} & & & \\ & R_{arm}+j3\omega_o L_{arm} & & \\ & & R_{arm}+j5\omega_o L_{arm} & \\ & & & \ddots \end{bmatrix} \tag{4.19}$$

$$Z_{even} = 2\begin{bmatrix} R_{arm}+j2\omega_o L_{arm} & & & \\ & R_{arm}+j4\omega_o L_{arm} & & \\ & & R_{arm}+j6\omega_o L_{arm} & \\ & & & \ddots \end{bmatrix} \tag{4.20}$$

The equations for the circulating currents are

$$\begin{aligned} i_{cirx,odd} &= \begin{bmatrix} I_{cirx1}e^{j(\omega_o+\phi_{cirx1})} \\ I_{cirx3}e^{j(3\omega_o+\phi_{cirx3})} \\ I_{cirx5}e^{j(5\omega_o+\phi_{cirx5})} \\ \vdots \end{bmatrix} = Z_{odd}^{-1} \begin{bmatrix} \tilde{U}_{diffx1}e^{j(\omega_o t+\phi_{ux1})} \\ \tilde{U}_{diffx3}e^{j(3\omega_o t+\phi_{ux3})} \\ \tilde{U}_{diffx5}e^{j(5\omega_o t+\phi_{ux5})} \\ \vdots \end{bmatrix} \\ &= Z_{odd}^{-1}E_{odd}X_{odd} \begin{bmatrix} I_{cirx1}e^{j\phi_{cirx1}} \\ I_{cirx3}e^{j\phi_{cirx3}} \\ I_{cirx5}e^{j\phi_{cirx5}} \\ \vdots \end{bmatrix} \end{aligned} \tag{4.21}$$

$$\begin{aligned} i_{cirx,even} &= \begin{bmatrix} I_{cirx2}e^{j(2\omega_o+\phi_{cirx2})} \\ I_{cirx4}e^{j(4\omega_o+\phi_{cirx4})} \\ I_{cirx6}e^{j(6\omega_o+\phi_{cirx6})} \\ \vdots \end{bmatrix} = Z_{even}^{-1} \begin{bmatrix} \tilde{U}_{diffx2}e^{j(2\omega_o t+\phi_{ux2})} \\ \tilde{U}_{diffx4}e^{j(4\omega_o t+\phi_{ux4})} \\ \tilde{U}_{diffx6}e^{j(6\omega_o t+\phi_{ux6})} \\ \vdots \end{bmatrix} \\ &= Z_{even}^{-1}E_{even}X_{even} \begin{bmatrix} I_o e^{j(2\phi_o+2\phi_x)} \\ I_{cirx2}e^{j\phi_{cirx2}} \\ I_{cirx4}e^{j\phi_{cirx4}} \\ \vdots \end{bmatrix} \end{aligned} \tag{4.22}$$

The equation (4.21) can be further rewritten as

$$Z_{odd} \begin{bmatrix} I_{cirx1}e^{j(\omega_o+\phi_{cirx1})} \\ I_{cirx3}e^{j(3\omega_o+\phi_{cirx3})} \\ I_{cirx5}e^{j(5\omega_o+\phi_{cirx5})} \\ \vdots \end{bmatrix} = X_{odd} \begin{bmatrix} I_{cirx1}e^{j(\omega_o+\phi_{cirx1})} \\ I_{cirx3}e^{j(3\omega_o+\phi_{cirx3})} \\ I_{cirx5}e^{j(5\omega_o+\phi_{cirx5})} \\ \vdots \end{bmatrix} \tag{4.23}$$

which is satisfied when either one of the following two conditions is met:

$$Z_{odd} = X_{odd} \tag{4.24}$$

$$Z_{odd}i_{cirx,odd} = X_{odd}i_{cirx,odd} = 0 \tag{4.25}$$

Since the circuit parameters in the condition (4.24) can be arbitrarily selected and the modulation index also varies during normal operation of the MMC, it is not guaranteed that this condition can be always satisfied. On the other hand, the left-hand side of equation (4.25) cannot be zero unless $i_{cirx,odd}$ is a zero vector.

As a consequence it is concluded that there is no odd harmonic in the inner differential current in the normal operation of an MMC.

The detailed current terms can be expressed according to (4.22) as follows.

$$I_{cirx2}e^{j\phi_{cirx2}} = \frac{Nm_o\left\{3{I_o}^2e^{j(2\theta_{ox})}\left[3e^{j\phi_{io}} - {m_o}^2\cos(\phi_{i_o})\right] + 2m_oI_{cirx4}e^{j(2\theta_{ox}+\phi_{cirx4})}\right\}}{96{\omega_o}^2C_{SM}L_{arm} - N\left(12+8{m_o}^2\right) - j48\omega_oC_{SM}R_{arm}} \tag{4.26}$$

For $k \geq 4$, the circulating current can be expressed as

$$I_{cirxk}e^{j\phi_{cirxk}} = \frac{-N\left[a_kI_{cirx(k-2)}e^{j\phi_{cirx(k-2)}} + c_kI_{cirx(k+2)}e^{j\phi_{cirx(k+2)}}\right]}{\left(R_{arm}+jk\omega_oL_{arm}\right)16\omega_oC_{SM} + Nb_k} \tag{4.27}$$

As a_k, b_k and c_k defined in (4.14) are purely imaginary components, the peak value of i_{cirxk} occurs when the imaginary part of the denominator in (4.27) is zero, and the current is only limited by $16\omega_oC_{SM}R_{arm}$ term. In this case, the resonance frequencies can be derived as

$$\omega_{rk} = \frac{1}{4}\sqrt{N\frac{2(k^2-1)+{m_o}^2k^2}{L_{arm}C_{SM}k(k^2-1)}}, \qquad k = 2,4,6,\cdots \tag{4.28}$$

Important conclusions can be obtained as follows:

1. There is no odd harmonic in the inner differential current in the steady state of the MMC;

2. The 2^{nd} order harmonic is mainly caused by the load current;

3. The k^{th} order harmonic ($k > 2$) are generated by the harmonics next to it ($(k-2)^{th}$ and $(k+2)^{th}$);

4. The amplitudes of these harmonics decrease rapidly as the harmonic order increases, as long as there is no current resonance;

5. There is one resonance frequency associated with every harmonic;

6. The resonance frequencies mainly depend on N, L_{arm} and C_{SM};

7. The resonance frequencies are decreasing, approximately as 1 over k, for high order harmonics;

8. The damping effect of R_{arm} is increasing with higher order harmonics as the magnitudes of a_k and c_k are decreasing while R_{arm} remains constant;

9. The maximum resonance frequency is the one with $k = 2$ and $m = 1$;

10. The circulating current might oscillate at one of the resonance frequency and consequently lead to system unstable if it is not properly regulated.

4.3 Repetitive control for power converters

Repetitive control can be employed to suppress the low-order harmonics i_{cir} in the inner differential current. It has been adopted in power converter applications due to their effectiveness on periodic error elimination and periodic disturbance rejection. Conventional repetitive control schemes have been widely adopted in constant voltage constant frequency (CVCF) PWM inverters [143, 146–150] since 2001. Repetitive controllers that exclusively cope with odd order harmonics are introduced in applications such as current active filters [149,150] and CVCF PWM inverters [151]. A dual-mode-structure repetitive control scheme with paralleled odd-harmonic and even-harmonic controllers is proposed in [151] to obtain higher tracking accuracy. The control scheme with different sampling rates is reported in [152] for reduced computation delay and enhanced system stability. Diverse variations of the conventional repetitive controller are introduced in recent literature for different applications. Repetitive controllers subjected to fractional delays are discussed in [153, 154], and a parallel structure fractional repetitive control is developed for PWM inverters where the sampling frequency of the control system is not an integral multiple of the fundamental frequency [141]. A Lagrange interpolation based fractional order repetitive control with the frequency adaptive capability is proposed in [155] for shunt active power filters. The finite impulse response filter based [142] and bandwidth-based [156] repetitive controllers are implemented to regulate the output current of grid connected inverters with system frequency deviation. The repetitive control combined with paralleled multiple resonant controllers is introduced to implement selective harmonic control of grid-connected inverters [157, 158] and CVCF PWM inverters [159, 160]. The combined control scheme that uses a resonant controller to regulate the output voltage for better dynamic response and a repetitive controller to deal with harmonics is detailed in [161]. Moreover, the repetitive control scheme can be also found in other applications, including solar photovoltaic applications [162, 163],

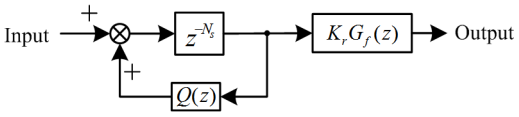


Figure 4.1: Block diagram of a repetitive control scheme.

gird simulator [164], and radio frequency applications [165].

4.3.1 Principle of a repetitive controller

Repetitive controllers (RCs) are effective in dealing with periodic signals, e.g. tracking periodic reference or rejecting periodic disturbances. The structure of a repetitive controller is shown in Figure 4.1, where K_r is the repetitive control gain, N_s is the number of samples in one repetitive period, $Q(z)$ is a low-pass filter to improve the repetitive control system robustness, and $G_f(z)$ is a phase lead filter contributing to the stability of the overall closed-loop system. The input of the repetitive controller will be stored for N_s sampling intervals. The delayed input will be accumulated with the current input and then fed to the plant again for periodic signal regulation. By doing this, the gains of the repetitive controller at characteristic frequencies will be high enough to effectively govern the signals at these frequencies, at the cost of relatively slow response and N_s memory cell occupation. With the presence of time delay block z^{-N_s}, the repetitive controller output generated based on the tracking error is postponed by a time period of N_sT_s seconds. The transfer function of the repetitive controller can be derived from Figure 4.1 and expressed as

$$G_{rc}(z) = \frac{K_rG_f(z)}{z^{N_s} - Q(z)} \tag{4.29}$$

The frequency characteristics of $G_{rc}(z)$ can be expressed as

$$G_{rc}(e^{j\omega T_s}) = \frac{K_rG_f(e^{j\omega T_s})}{e^{j\omega N_sT_s} - Q(e^{j\omega T_s})} \tag{4.30}$$

Since $Q(e^{j\omega T_s}) \approx 1$ at the frequencies lower than its cutoff frequency ω_{cf}, the repetitive controller has high gains at frequencies as

$$\omega = \frac{2l\pi}{N_sT_s}, \qquad 0 < l < \frac{\omega_{cf}}{\omega_o} \tag{4.31}$$

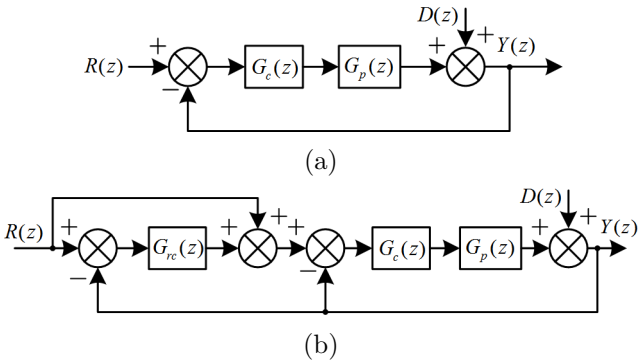


Figure 4.2: Block diagram of: (a) Conventional control scheme for power converters; (b) A plugged-in repetitive control scheme.

As the sampling interval T_s of a digital control system is usually set to be constant, a repetitive controller can be designed to cope with different orders of harmonics by setting $N_s = 2l\pi/\omega_o T_s = lf_s/f_o$, where f_s is the sampling frequency and f_o is the output frequency [143, 151, 166, 167].

4.3.2 Plugged-in repetitive control scheme for power converters

The block diagram of a typical repetitive control scheme is shown in Figure 4.2 (b), where $R(z)$ is the reference, $Y(z)$ is the output, $D(z)$ is the disturbance, $G_{rc}(z)$, $G_c(z)$, and $G_p(z)$ are the z-domain transfer functions of the repetitive controller, the conventional converter controller and the plant respectively. $G_c(z)$ may be a single- or multi-loop controller, depending on different applications. $G_{rc}(z)$ can be designed to cope with odd, even, or both harmonics according to compensation requirements.

The output of the repetitive controller can be derived as

$$Y(z) = \frac{[1 + G_{rc}(z)]\, G_c(z)G_p(z)R(z) + D(z)}{1 + [1 + G_{rc}(z)]\, G_c(z)G_p(z)} \tag{4.32}$$

The tracking error of this closed-loop control system can be expressed as

$$E(z) = R(z) - Y(z) = \frac{R(z) - D(z)}{1 + [1 + G_{rc}(z)]\, G_c(z)G_p(z)} \tag{4.33}$$

Letting the closed-loop transfer function of the conventional control loop shown

in Figure 4.2 (a) to be

$$H(z) = \frac{G_c(z)G_p(z)}{1 + G_c(z)G_p(z)} \tag{4.34}$$

the closed-loop transfer function of the overall control system from $R(z)$ to $Y(z)$ can be obtained as

$$\frac{Y(z)}{R(z)} = \frac{H(z)[z^{N_s} - Q(z) + K_r G_f(z)]}{z^{N_s} - Q(z) + K_r G_f(z)H(z)} \tag{4.35}$$

According to equation (4.35), the overall closed-loop system is stable only if all the roots of the characteristic function $z^{N_s} - Q(z) + K_r G_f(z)H(z)$ are placed inside the unit circle centered at the origin of the z-plane. For simplifying the analysis, one sufficient condition [168] for system stability is usually employed, which can be written as

$$|Q(z) - K_r G_f(z)H(z)| < 1, \ \forall z = e^{j\omega T_s}, 0 < \omega T_s < \pi \tag{4.36}$$

The inequality in (4.36) shows that $Q(z)$, K_r, and $G_f(z)$ all affect the system stability, which makes them important in the repetitive controller design. $Q(z)$ is used to reject high-frequency components in the internal model [143, 151]. It is usually designed to be a low-pass filter with the features of a unity gain at low frequencies and no phase delay. K_r is normally selected to achieve a smaller damping ratio and faster transient response [151], as long as the stability condition in (4.36) can be satisfied. Furthermore, the phase delay in the feedback control system has to be carefully compensated by an elaborately designed phase lead filter to prevent the overall system instability. If the phase lead filter is designed to be $G_f(z) = 1/H(z)$, perfect cancellation is achieved. However, such perfect cancellation is not always possible in practical applications due to system uncertainties, such as inaccurate parameters of the power converter and plant, parameter variation, and load disturbances. Alternatively, $G_f(z)$ can be designed to be a low-pass filter $S(z)$ embedded with a pure time advance unit z^k [169], as

$$G_f(z) = z^k S(z) \tag{4.37}$$

The low pass filter $S(z)$ is able to reject high frequency harmonics and disturbances, while z^k is used to compensate the phase delay caused by $S(z)$ and $H(z)$. In general, in the design process of a repetitive controller, $Q(z)$, $S(z)$, and K_r are firstly designed according to the system requirements, e.g. tracking accuracy,

system dynamics, harmonics elimination, and resonance prevention. After that, the time advance unit is employed to ensure the stability of the overall system. It also should be noted that high-frequency signals cannot be compensated due to the presence of $Q(z)$ and $S(z)$, which brings a trade-off between the tracking accuracy and the system robustness.

4.3.3 Explicit phase lead filter design method in repetitive control

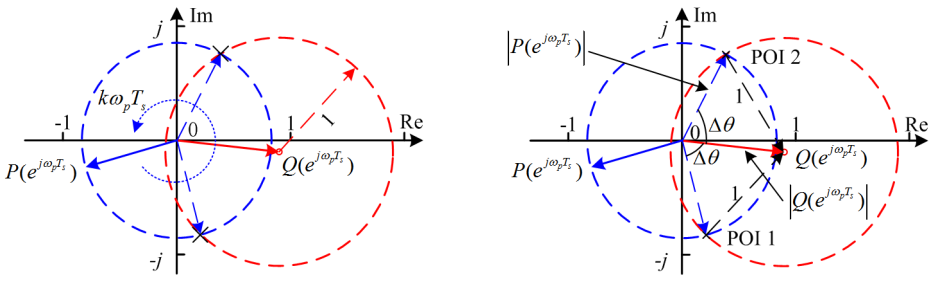
In previous studies [143,151,169], the time advance unit z^k was obtained through empirical design, e.g. by comparing the phase-frequency characteristics of $S(z)H(z)$ and z^{-k} in Matlab or a trial-and-error approach through experiments. There is few theoretical analysis presented to discuss its impact to the system stability. And a quantitative design of the time advance unit for phase compensation of repetitive control is still missing. In this subsection, the role of z^k in the overall system stability will be clearly explained, and an explicit analytical description for selecting the value of k is also presented.

Substituting (4.37) into (4.36), the sufficient condition can be expressed as

$$\left|Q(z) - K_r S(z)H(z)z^k\right| < 1 \tag{4.38}$$

This sufficient condition of the system stability at a particular frequency ω_p can be described geometrically as in Figure 4.3. $Q(z)$ is represented as the phasor $Q(e^{j\omega_p T_s})$, whose magnitude is denoted as $|Q(e^{j\omega_p T_s})|$ and phase angle is $\theta_Q(e^{j\omega_p T_s})$. Another phasor $P(e^{j\omega_p T_s})$ is defined as

$$P(e^{j\omega_p T_s}) = K_r S(e^{j\omega_p T_s})H(e^{j\omega_p T_s}) = |P(e^{j\omega_p T_s})|\angle\theta_P(e^{j\omega_p T_s}) \tag{4.39}$$



(a) (b)

Figure 4.3: Geometrical illustration of stability condition.

The overall system is sufficiently stable if the end of $P(e^{j\omega_p T_s})$ is placed inside the red dashed unity circle, whose center is at the end of the phasor $Q(e^{j\omega_p T_s})$. Without phase compensation, the end of $P(e^{j\omega_p T_s})$ might be placed outside the red dashed circle, as indicated by the solid blue arrow in Figure 4.3 (a), which might result in an unstable closed-loop system. By introducing the time advance unit z^k into the repetitive controller, $P(e^{j\omega_p T_s})$ is rotated anticlockwise around the origin by $k\omega_p T_s$ radian while keeping the same magnitude. It is predictable that the system will be definitely stable at frequency ω_p if $P(e^{j\omega_p T_s})$ can be properly rotated until its end is eventually located inside the red dashed circle. The locus of rotating the end of $P(e^{j\omega_p T_s})$ is indicated by the blue dashed circle centered at the origin. As shown in Figure 4.3 (b), the points of intersection (POI) of the two dashed circles reveal the values of k that may make the system critically stable. The available range of k can be obtained by solving these points. The angles that $P(e^{j\omega_p T_s})$ should be rotated to intersect with the red dashed circle can be derived as

$$\begin{cases} \Delta\theta_1(e^{j\omega_p T_s}) = \theta_Q(e^{j\omega_p T_s}) - \Delta\theta(e^{j\omega_p T_s}) - \theta_P(e^{j\omega_p T_s}) \\ \Delta\theta_2(e^{j\omega_p T_s}) = \theta_Q(e^{j\omega_p T_s}) + \Delta\theta(e^{j\omega_p T_s}) - \theta_P(e^{j\omega_p T_s}) \end{cases} \tag{4.40}$$

where $\Delta\theta(e^{j\omega_p T_s})$ in Figure 4.3 (b) can be obtained as

$$\Delta\theta(e^{j\omega_p T_s}) = \arccos\left[\frac{\left|P(e^{j\omega_p T_s})\right|^2 + \left|Q(e^{j\omega_p T_s})\right|^2 - 1}{2\left|P(e^{j\omega_p T_s})\right|\left|Q(e^{j\omega_p T_s})\right|}\right] \tag{4.41}$$

Note that (4.41) is solvable only if the inequality

$$1 - \left|Q(e^{j\omega_p T_s})\right| \leq \left|P(e^{j\omega_p T_s})\right| \leq 1 + \left|Q(e^{j\omega_p T_s})\right| \tag{4.42}$$

is satisfied, which means that at least one intersection point exists. $\left|P(e^{j\omega_p T_s})\right| < 1 - \left|Q(e^{j\omega_p T_s})\right|$ indicates that the end of $P(e^{j\omega_p T_s})$ is always placed inside the unit circle and the system is always stable at ω_p. And $\left|P(e^{j\omega_p T_s})\right| > 1 + \left|Q(e^{j\omega_p T_s})\right|$ means that the end of $P(e^{j\omega_p T_s})$ is always located outside of the unit circle and might lead to system instability despite the phase compensation by z^k.

Based on the aforementioned analysis, the parameters of the repetitive controller can be designed accordingly. The repetitive control gain K_r is yielded by

$$0 < K_r \leq \frac{1 + \left|Q(e^{j\omega_p T_s})\right|}{|S(e^{j\omega_p T_s})H(e^{j\omega_p T_s})|} \tag{4.43}$$

The range of k in the time advance unit z^k can be derived as

$$\frac{\Delta\theta_1(e^{j\omega_p T_s})}{\omega_p T_s} \leq k_1 \leq k \leq k_2 \leq \frac{\Delta\theta_2(e^{j\omega_p T_s})}{\omega_p T_s} \tag{4.44}$$

where k, k_1 and k_2 are non-negative integers. Equation (4.44) also indicates the phase margin for a given value of k. Furthermore, the overall system has the maximum phase margin and is more robust against load step changes at ω_p if $Q(e^{j\omega_p T_s})$ and the rotated $P(e^{j\omega_p T_s})$ are in phase, according to Figure 4.3. Equation (4.45) suggests the value of k that can provide the maximum system stability margin.

$$k = \frac{\theta_Q(e^{j\omega_p T_s}) - \theta_P(e^{j\omega_p T_s})}{\omega_p T_s} \tag{4.45}$$

Moreover, the time advance unit has to be designed to guarantee the system stability at all frequencies up to Nyquist frequency.

4.4 Even-harmonic repetitive control based circulating current harmonics suppression

In most cases, only the DC component $I_{DC}/3$ in the differential current is preferred to maintain the stable operation of the MMC and minimize the losses. Therefore, in addition to controlling the output power of the MMC, special efforts are also devoted to the inner differential current control to remove i_{cirx}. The circulating current i_{cirx} cannot be completely removed if only a conventional PI controller is employed as in Figure 3.8 (b), for the sake of a tradeoff between the harmonic suppression and system stability.

4.4.1 Even-harmonic repetitive controller for the circulating current suppression

In order to properly regulate the differential current and suppress the circulating harmonics, a repetitive controller is plugged in the current control loop instead of a single PI controller, as shown in Figure 4.4, where $PI(z)$ is the z-domain transfer functions of the PI controller. The inherent computation and PWM delays in a digital control system are modeled as one sampling period delay and a zero-order-hold (ZOH) block respectively [170].

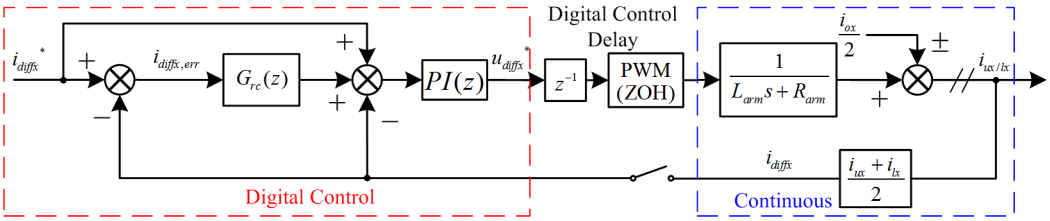


Figure 4.4: Block diagram of the repetitive control scheme for inner differential current control of the MMC.

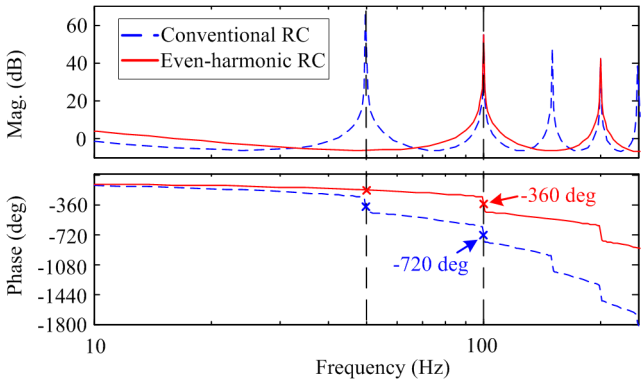


Figure 4.5: Bode diagrams of the conventional and even-harmonic repetitive controllers.

According to the circulating current contents analysis presented in Section 4.2, there are only even order harmonics exist in the circulating current. The repetitive control principle introduced in Section 4.3.2 suggests that, for a conventional repetitive controller designed to cope with odd and even harmonics (fundamental frequency is f_o), N_s has to be selected as $N_s = f_s/f_o$. On the other hand, the even order harmonic repetitive controller can be achieved by setting the number of error samples N_s to be half of that in one fundamental period, i.e. $N_s = f_s/(2f_o)$.

Compared to the conventional repetitive controllers, the even-harmonic repetitive controller has high gains at frequencies that are the even multiples of f_o, while the memory cells required to store these samples are halved and the delay of the repetitive controller is reduced. The magnitude and phase characteristics of the conventional and even-harmonic repetitive controllers are illustrated in Figure 4.5, which shows that the later has high gains at even-order frequencies with less phase delay. Moreover, the performance of the repetitive controller is also improved compared with the conventional ones, which will be discussed in terms of frequency characteristics analysis in the next subsection.

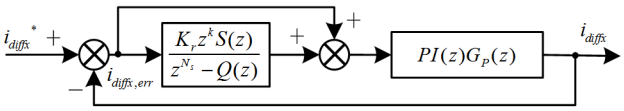


Figure 4.6: Simplified block diagram of the differential current control loop.

4.4.2 Frequency characteristics analysis of the even-harmonic repetitive controller

In order to analyze the differential current control scheme more conveniently and effectively, the overall differential current control loop is eventually simplified as in Figure 4.6. The closed-loop transfer function from the reference to the differential current can be derived as

$$\frac{i_{diffx}}{{i_{diffx}}^*} = \frac{H(z)\left[z^{N_s} - Q(z) + K_r z^k S(z)\right]}{z^{N_s} - Q(z) + K_r z^k S(z)H(z)} \tag{4.46}$$

where $H(z)$ is the closed loop transfer function of the PI control loop. The differential current tracking error can be accordingly derived as

$$i_{diffx,err} = \frac{[1 - H(z)]\left[z^{N_s} - Q(z)\right]}{z^{N_s} - Q(z) + K_r z^k S(z)H(z)} {i_{diffx}}^* \tag{4.47}$$

According to equations (4.46) and (4.47), the repetitive control system is stable if all the roots of the system characteristic equation $z^{N_s} - Q(z) + K_r z^k S(z)H(z)$ are located inside the unit circle at the origin, i.e. the sufficient condition (4.38) is satisfied. As stated in [143], the current tracking error convergence can be derived from (4.47) as

$$z^{N_s} i_{diffx,err} \approx \left[Q(z) - K_r z^k S(z)H(z)\right] i_{diffx,err} \tag{4.48}$$

It is evident that the tracking error of the repetitive control scheme will be $|Q(z) - K_r z^k S(z)H(z)| i_{diffx,err}$ after a time period of $N_s T_s$. The convergence rate of the proposed repetitive controller is accordingly doubled because of the halved N_s compared with that of the conventional repetitive controllers.

As shown in Figure 4.6, the overall control system can be simply divided into two parallel forward paths, i.e. a simple PI controller applied to the plant model, and a repetitive controller cascaded with the PI controller and the plant model. In this section, only the path including the repetitive controller is analyzed. The

transfer function of the repetitive controller path is described as

$$G_{RP}(z) = G_{rc}(z)PI(z)G_P(z) \tag{4.49}$$

It is clear in (4.29) and (4.49) that N_s will affect the open loop gain of the repetitive control path. Since the open loop gain of the repetitive control path is proportional to that of $G_{rc}(z)$, only $G_{rc}(z)$ is discussed here. As the high-frequency gain of a repetitive controller is normally designed to be small to prevent oscillation, only the low-frequency gain is investigated. The magnitude of the time advance unit z^k is one so that it will not affect the gain of the repetitive controller. The low pass filter $Q(z)$ and $S(z)$ are also dedicatedly designed with almost unity gain at low frequencies. Therefore, if the low pass filter $Q(z)$ is designed as in (4.60), the gain of $G_{rc}(z)$ at low frequencies can be rewritten as

$$\left|G_{rc}(e^{j\omega T_s})\right| \approx \frac{K_r}{|e^{j\omega N_s T_s} - 1|} \tag{4.50}$$

Noting that when ω is low, the discrete frequency ωT_s is very close to zero, so that the open loop gain of this repetitive controller can be further simplified as

$$\left|G_{rc}(e^{j\omega T_s})\right| \approx \frac{K_r}{|\cos(\omega N_s T_s) + j\sin(\omega N_s T_s) - 1|} \approx \frac{K_r}{2}\frac{1}{|\sin(\omega N_s T_s/2)|} \tag{4.51}$$

Substituting $N_s = f_s/f_o$ and $N_s = f_s/2f_o$ into (4.51) respectively and noting that $T_s f_s = 1$, it can be found that the gain of the even-harmonic repetitive controller is almost twice of that of the conventional repetitive controller when $f \ll 2f_o$ as implied by (4.52).

$$\frac{|G_{rc}(e^{j\omega T_s})|_{N_s=f_s/2f_o}}{|G_{rc}(e^{j\omega T_s})|_{N_s=f_s/f_o}} \approx \frac{|\sin(\pi f/f_o)|}{|\sin(\pi f/2f_o)|} \approx 2 \tag{4.52}$$

The crossover frequency of the repetitive controller f_{cross} shown in equation (4.53) is inversely proportional to N_s.

$$f_{cross} = \left.\frac{\arcsin\left(K_r/2\right)}{\pi N_s T_s}\right|_{0\le K_r\le 2,\ \omega T_s\approx 0} \tag{4.53}$$

Furthermore, the phase-frequency characteristics of the repetitive controller

can be derived based on (4.30) as

$$\begin{aligned}\angle G_{rc}(e^{j\omega T_s}) &= k\omega T_s + \angle S(e^{j\omega T_s}) - \angle(e^{j\omega N_s T_s} - Q(e^{j\omega T_s})) \\ &\approx k\omega T_s + \angle S(e^{j\omega T_s}) - \angle(e^{j\omega N_s T_s} - 1)\end{aligned} \tag{4.54}$$

The critical frequencies for the even-harmonic repetitive controller are those satisfying nf_o with n being an even integer. The magnitude of $G_{rc}(z)$ will cross 0 dB at these frequencies. The corresponding phase displacements of the proposed and conventional repetitive controllers as

$$\begin{aligned}&\angle G_{rc}(e^{j\omega T_s})\big|_{N_s=f_s/2f_o} - \angle G_{rc}(e^{j\omega T_s})\big|_{N_s=f_s/f_o} \\ &\approx \angle(e^{j\pi f/2f_o} - 1) - \angle(e^{j\pi f/f_o} - 1) = -n\pi, \quad n = 0, 2, 4, \cdots\end{aligned} \tag{4.55}$$

indicating that the even-harmonic repetitive controller introduces less phase delay compared to that of the conventional one. Meanwhile, it could be conveniently verified by (4.50) that the gains of $G_{rc}(z)$ at desired frequencies (e.g. 100 Hz, 200 Hz, ...) are not affected no matter the value of N_s is selected to be f_s/f_o or $f_s/2f_o$. The bandwidth of the proposed repetitive controller f_B at critical even-order frequencies can also be derived by assigning -3 dB to the magnitude of $G_{rc}(z)$, as

$$f_B = \left.\frac{2\arcsin\left(K_r/1.416\right)}{\pi N_s T_s}\right|_{0\le K_r\le 2,\ \omega T_s\approx 0} \tag{4.56}$$

It is obvious that f_B is inversely proportional to N_s as well at low frequencies. Wider bandwidth is helpful in offering better tolerance for system frequency deviation. For instance, a frequency deviation f_d may be introduced making the MMC output frequency to be actually $f = f_o \pm f_d$, the magnitude of $G_{rc}(e^{j\omega T_s})$ at relatively low even-order frequencies can be expressed by

$$|G_{rc}(e^{j\omega T_s})| \approx \frac{K_r}{2}\frac{1}{|\sin[n\pi(f_o \pm f_d)N_s T_s]|} \approx \frac{K_r}{2n\pi f_d N_s T_s} \tag{4.57}$$

where n is an even integer and $n\pi f_d \ll f_o$. Substituting $N_s = f_s/f_o$ and $N_s = f_s/2f_o$ into (4.57), the results indicate that the gains of the even-harmonic repetitive controller at deviated frequencies are twice of those of the conventional controller. In other words, the even-harmonic repetitive controller has wider bandwidths at critical frequencies and consequently better compensating performance when there is a system frequency variation.

The magnitude characteristics of both conventional and even-harmonic repet-

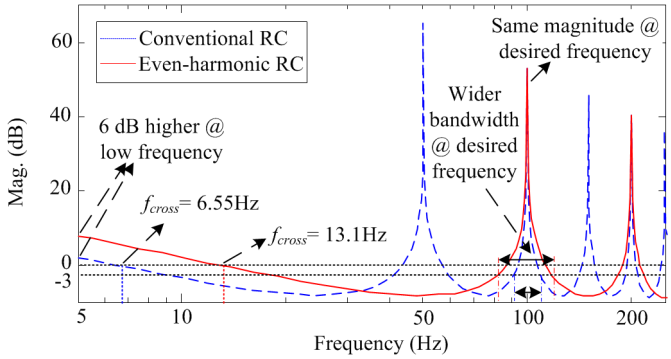


Figure 4.7: The frequency characteristics of $G_{rc}(z)$ with $N_s = f_s/f_o$ and $N_s = f_s/2f_o$.

itive controllers are depicted in Figure 4.7. It can be seen that the frequency characteristics of $G_{rc}(z)$, in terms of low-frequency gain, crossover frequency, magnitudes and bandwidths at desired frequencies, etc., are in accordance with the mathematical analysis.

4.5 Case study and performance verification

The even-harmonic repetitive control scheme for circulating current suppression is designed in this section based on the system parameters of a single-phase MMC shown in Figure 4.8. Half-bridge sub-modules are used in the MMC. The load resistor R_l and load inductor L_l are connected between the middle points of the two arms and DC bus capacitors. The even-harmonic repetitive control scheme can be conveniently applied to any phase of a three-phase MMC system, with the

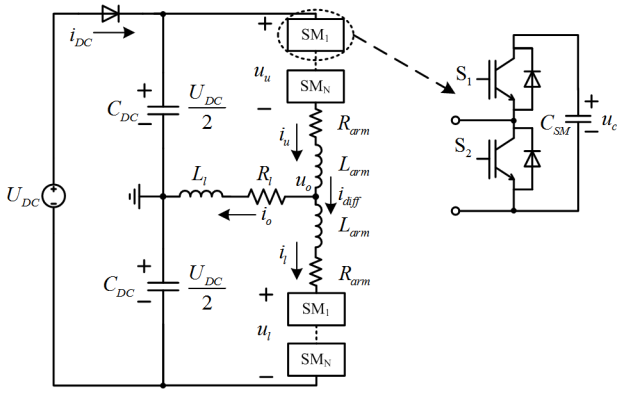


Figure 4.8: Structure of a single-phase MMC based inverter.

same control scheme performance, stability, and robustness, by simply treating each phase leg as a single-phase MMC. The effectiveness of the even-harmonic repetitive controller in a three-phase MMC is verified in simulations. The experimental verification of the even-harmonic repetitive control scheme is performed on a single-phase MMC prototype.

4.5.1 Test system description

The detailed parameters of the MMC system are listed in Table 4.1. The phase-shifted PWM modulation scheme detailed in Section 3.4.5 is employed to generate corresponding gating signals for individual sub-module. The phase displacement of triangular carriers for sub-modules in one arm is $2\pi/N$. By doing so, the output voltage level is $2N + 1$ and the equivalent switching frequency is $2Nf_c$, when N is an odd number. As the equivalent switching frequency of the MMC is $6f_c = 12$ kHz, the sampling frequency is designed to be $f_s = 12$ kHz and the control system is synchronized with it, having a period of $T_s = 1/f_s$. N_s is chosen to be 120 to perform the even-harmonic repetitive controller. In order to implement the individual control to every sub-module, the individual voltage reference and a phase-shifted triangular carrier are assigned to each sub-module.

Table 4.1: Parameters of the single-phase MMC system

Parameter	**Value**
DC bus voltage: U_{DC}	240 V
Amplitude of Output Voltage: U_o	100 V
Load Resistor: R_l	10 Ω
Load Inductor: L_l	6.3 mH
Rated output frequency: f_o	50 Hz
No. of sub-modules in each arm: N	3
Arm inductance: L_{arm}	5 mH
Arm resistor: R_{arm}	0.025 Ω
SM capacitor: C_{SM}	470 μF
Carrier frequency: f_c	2 kHz
PI parameters of the difference current control	$K_p = 3$, $K_i = 10$

4.5.2 Even-harmonic repetitive control scheme design

The discrete transfer function of the plant can be converted from $G_P(s)$ by ZOH transform [170], as

$$G_P(z) = \frac{1}{R_{arm}} \left(\frac{1 - e^{-R_{arm}T_s/L_{arm}}}{z - e^{-R_{arm}T_s/L_{arm}}} \right) \tag{4.58}$$

The closed conventional PI differential current control loop is treated as the plant of the repetitive controller, whose transfer function can be derived as

$$H(z) = \frac{PI(z)G_P(z)z^{-1}}{1 + PI(z)G_P(z)z^{-1}} \tag{4.59}$$

According to the circulating current contents analysis presented in Section 4.2, the amplitude of the circulating current higher than 500 Hz (the 10^{th} order) is negligible in the MMC system employed in this case study, the cut-off frequencies of the low-pass filters in the repetitive controller can be designed appropriately. The low pass filter $Q(z)$ is designed as

$$Q(z) = \frac{z^2 + z + 4 + z^{-1} + z^{-2}}{8} \tag{4.60}$$

whose frequency response can be written as

$$Q(e^{j\omega T_s}) = \frac{2\cos^2(\omega T_s) + \cos(\omega T_s) + 1}{4} \tag{4.61}$$

The cutoff frequency of $Q(z)$ is around 940 Hz, which is almost nineteen times of the MMC fundamental frequency, in order to achieve unity gain at low frequencies and reject high-frequency components. The phase lead filter $z^k S(z)$ is elaborately designed such that the natural frequency of the second order low pass filter $S(z)$ is $f_n = 800$ Hz and the time advance step is $k = 8$ according to the design method presented in Section 4.3.3. The purpose of this phase lead filter is to improve the stability of the overall repetitive control system by achieving the desirable frequency response shown in Figure 4.9 (a). $S(z)$ is used to shape the magnitude characteristics of the plant $H(z)$ so that the gain of $z^k S(z)H(z)$ is 0 dB at low frequencies and monotonically decreases at higher frequencies. The time advance unit z^k is used to compensate the phase delay caused by $S(z)$, the plant, and the control system for larger overall system phase margin [166]. The

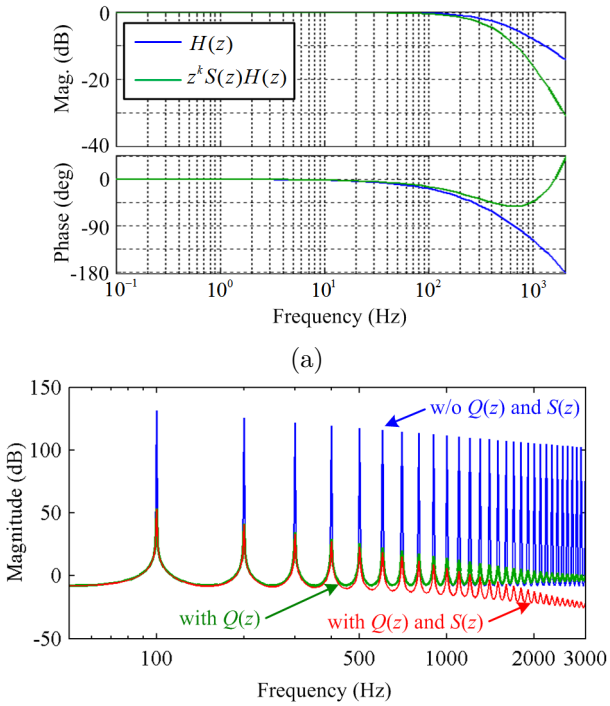


Figure 4.9: Frequency characteristics of: (a) $H(z)$ and $z^k S(z)H(z)$; (b) $G_{rc}(z)$ with or without $Q(z)$ and $S(z)$.

impacts of $Q(z)$ and $S(z)$ on the repetitive control loop gains are illustrated in Figure 4.9 (b).

The Nyquist plots in Figure 4.11 demonstrate the effects of $Q(z)$ and $S(z)$ on system stability and robustness. It can be seen in Figure 4.11 (a) that the system might be unstable if both $Q(z)$ and $S(z)$ are disabled (set to be 1) because the inequality (4.38) cannot be satisfied. With the presence of $Q(z)$ in Figure 4.11 (b), the peak gain of $Q(z) - K_r z^k H(z)$ is reduced to -1.83dB and the system stability is therefore confirmed up to system Nyquist frequency. The even smaller peak gain of $Q(z) - K_r z^k S(z)H(z)$ in Figure 4.11 (c) shows that the robustness of the control system is further improved by $S(z)$. However, as presented in Figure 4.9 (b), the repetitive controller gain is significantly reduced by $Q(z)$ and $S(z)$ at frequencies higher than 1 kHz. Thus, the high-frequency periodic disturbances may not be perfectly compensated because of the low controller gains at those frequencies, which brings a tradeoff between the system robustness and the tracking accuracy [143, 148].

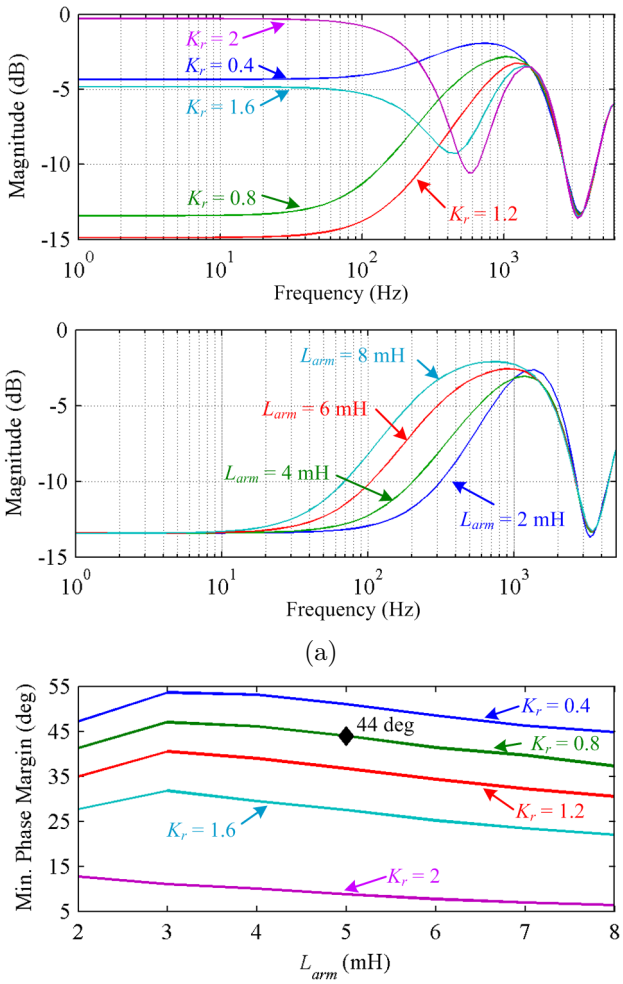


Figure 4.10: Repetitive control system characteristics with different parameters: (a) Magnitude of $Q(z) - K_r z^k S(z) H(z)$ with different K_r and L_{arm}; (b) Minimum phase margin of the system with different K_r and L_{arm} variation.

The system dynamic response and stability are mainly determined by the repetitive gain K_r. In order to ensure the system stability at all frequencies, the repetitive control gain K_r has to be yielded as in equation (4.43). Referring to the parameters in Table 4.1, the theoretical range of K_r calculated based on (4.43) is around zero to two, in which the overall control system can be stabilized. Equation (4.47) suggests that the convergence speed of the repetitive controller is proportional to the magnitude of $Q(z) - K_r z^k S(z) H(z)$. Different K_r and L_{arm} are encompassed in convergence and stability analysis since they introduce most

significant influence to the control system. It is obvious in Figure 4.10 that the convergence speed of the repetitive controller at frequencies lower than 1 kHz is highly affected by K_r. As shown in Figure 4.10 (a), a K_r close to one provides relatively fast convergence to harmonics suppression at desired frequencies, and a smaller L_{arm} offers faster convergence speed at frequencies from 10 to 1000 Hz. The minimum phase margin of the repetitive control system is investigated with the consideration of K_r and L_{arm} variation. It can be seen in Figure 4.10 (b) that a larger K_r results in less phase margin, which increases the difficulty in other controller parameters design and might easily lead to system instability when there are disturbances or system parameter variations. The phase margin is to some extent affected by changing the arm inductance from 2 mH to 8 mH. Figure 4.10 (b) shows that the system is robust against L_{arm} variation. Based on the curves in Figure 4.10, $K_r = 0.8$ is selected with the considerations of both convergence speed and system stability. The even harmonic repetitive control system possesses a phase margin of 44 degrees with selected system parameters, as indicated by the black diamond in Figure 4.10 (b). The Nyquist plot of $Q(z) - K_r z^k S(z) H(z)$ depicted in Figure 4.11 (c) indicates that the even-harmonic repetitive control scheme is stable based on the parameters given in this subsection because the stability condition in (4.38) is always satisfied.

4.5.3 Simulation verification

Simulation verification has been conducted on a three-phase MMC with Piecewise Linear Electrical Circuit Simulation (PLECS). The circuit and controller parameters of the three-phase MMC are the same as those of the single-phase MMC listed in Table 4.1, except for the number of phases. The main objective of this

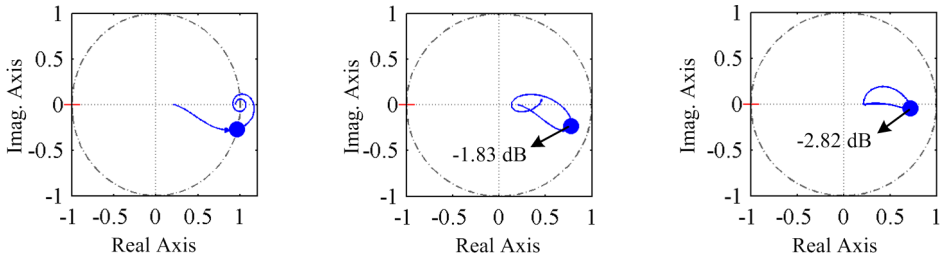


Figure 4.11: Nyquist plots of: (a) $1 - K_r z^k H(z)$; (b) $Q(z) - K_r z^k H(z)$; (c) $Q(z) - K_r z^k S(z) H(z)$.

simulation is to confirm the effectiveness of the even-harmonic repetitive control scheme in circulating current suppression in a three-phase MMC system.

Figure 4.12 shows the inner differential currents in the phase leg regulated by

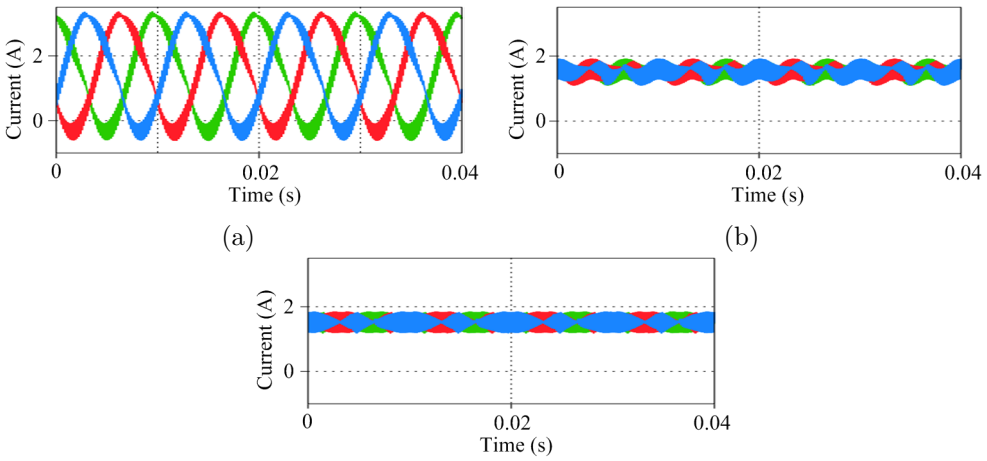


Figure 4.12: Inner differential currents regulated by different controllers in simulation: (a) PI; (b) PI + 2^{nd} R + 4^{th} R; (c) Even-harmonic RC.

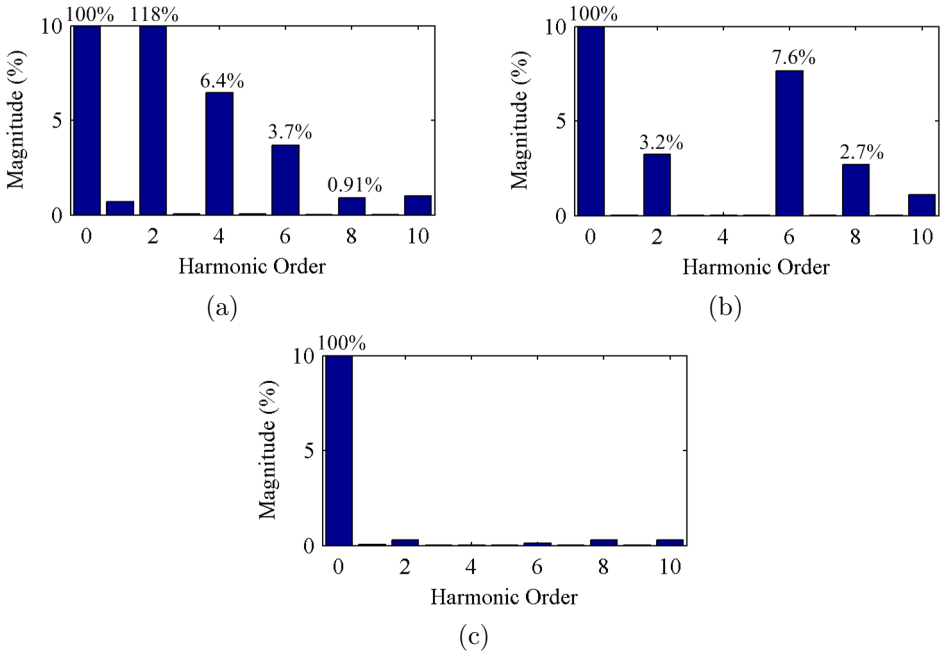


Figure 4.13: Spectra of inner differential currents in phase a regulated by different controllers in simulation: (a) PI; (b) PI + 2^{nd} R + 4^{th} R; (c) Even-harmonic RC.

different controllers, i.e. a PI controller, a PI controller with paralleled 2^{nd} and 4^{th} resonant controllers, and the even-order repetitive controller. The modulation index is set to be 0.833 to generate the output voltage with its peak value of 100 V, and the Root-Mean-Square (RMS) output current is 6.17 A. The harmonic spectra of the differential current in phase a are shown in Figure 4.13. Figure 4.13 (a) indicates that there are considerable even order harmonics in the differential current if only a PI controller is adopted, and there is basically negligible harmonics with frequencies higher than 500Hz, which means that the cutoff frequencies of $Q(z)$ and $S(z)$ are properly designed to cope with current harmonics. The differential current can be less distorted by adding resonant controllers to suppress low order harmonics as shown in Figure 4.12 (b). However, the higher order harmonics, e.g. 6^{th} and 8^{th} harmonics, may be even increased as shown in Figure 4.13 (b). On contrast, the repetitive controller can almost completely eliminate the even harmonics in the circulating current, as shown in Figure 4.12 (c) and Figure 4.13 (c).

The simulated waveforms of the differential currents in a three-phase MMC with unbalanced load conditions are demonstrated in Figure 4.14. The load resistance and inductance of phase c is half of those in other two phases. It can be seen in Figure 4.14 that the even-harmonic repetitive control scheme is effec-

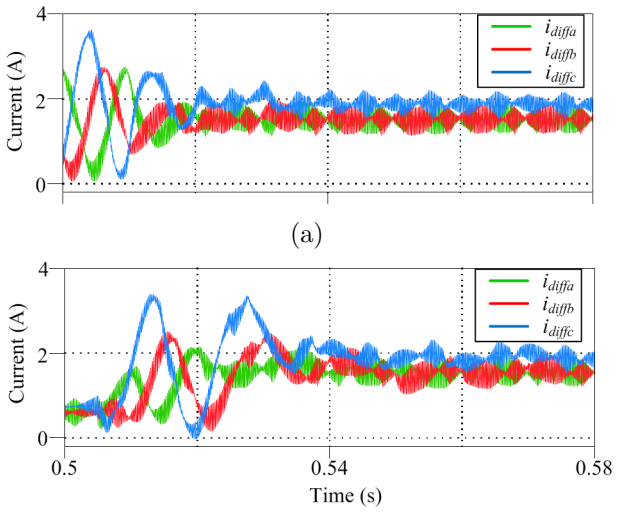


Figure 4.14: Inner differential currents of a three-phase MMC system with unbalanced load condition: (a) Startup; (b) reference step change.

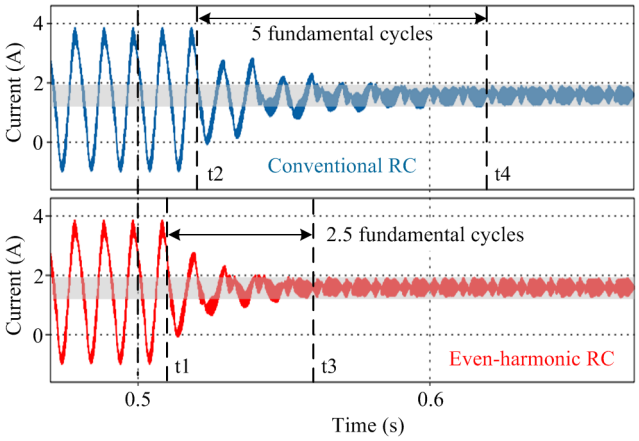


Figure 4.15: Inner differential currents in phase a when the conventional and even-harmonic repetitive controllers are activated.

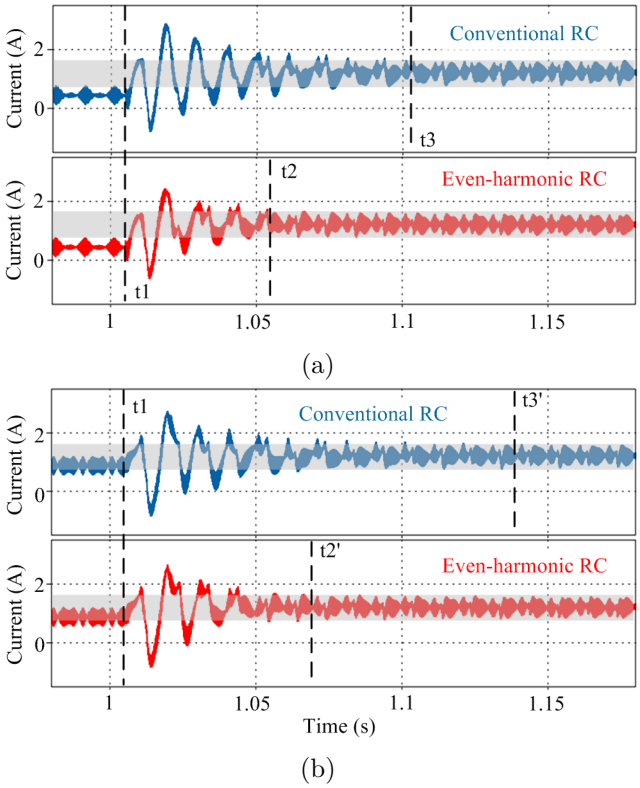


Figure 4.16: Inner differential currents in phase a regulated by conventional and even-harmonic repetitive controllers during: (a) Modulation index step change: 0.5 to 0.833; (b) Load resistor step change: 24 Ω to 12 Ω.

tive to suppress the harmonics in differential currents under both balanced and unbalanced conditions.

The startup process of the even-harmonic and conventional repetitive controllers, when they are enabled at 0.5 s, are illustrated in Figure 4.15. The delay periods of the two controllers are half and one fundamental period respectively. t1 and t2 are the instants at which the repetitive controllers are actually activated and the controllers start to adjust their outputs according to tracking errors. It is obvious that the even-harmonic repetitive controller only requires a half period (2.5 fundamental cycles) to achieve steady state after being activated as compared to that (5 fundamental cycles) of the conventional ones.

The inner differential currents regulated by the conventional and even-harmonic repetitive controllers under reference and load step changes are presented in Figure 4.16. Figure 4.16 (a) illustrates the current waveform when the modulation

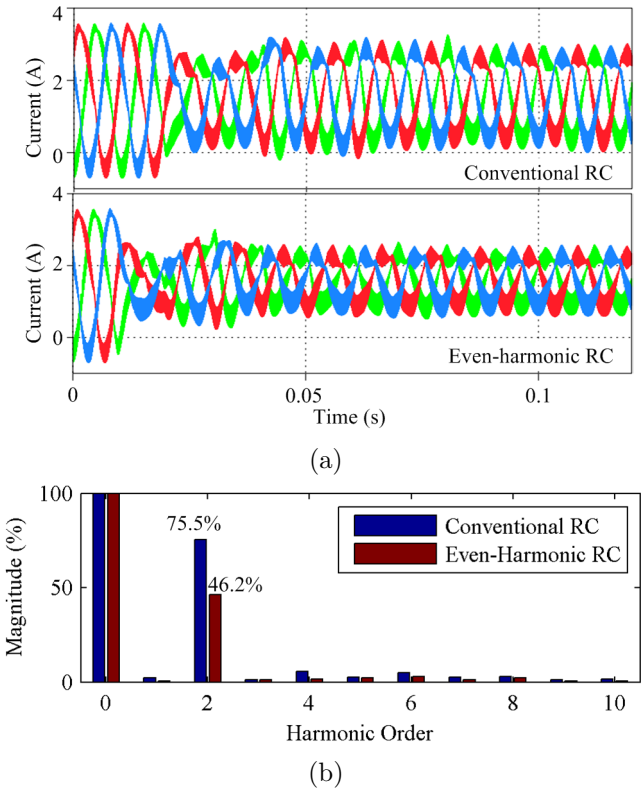


Figure 4.17: Differential currents regulated by the conventional and even-harmonic repetitive controllers at $f_o = 47.5$ Hz in simulation: (a) differential currents; (b) Spectra of the differential currents in phase a.

index changes from 0.5 to 0.833. The current waveforms when the load resistance changes from 24 Ω to 12 Ω are shown in Figure 4.16 (b). It can be seen in Figure 4.16 that i_{diffa} regulated by the even-harmonic repetitive controller is settled down at t2 and t2′, while it is settled down at t3 and t3′ when a conventional repetitive controller is used. The MMC operates stably during reference and load step changes. The halved N_s not only reduces the delay period of the repetitive controller but also speeds up the dynamic response of the system.

The performances of the both repetitive controllers under the condition of 5% frequency variation in the MMC output are shown in Figure 4.17 (a). Figure 4.17 (b) presents the fast Fourier transform (FFT) of the differential currents in phase a. The magnitude of the second order harmonic current, normalized to the DC component of the differential current, is reduced from 75.5% to 46.2% by replacing the conventional repetitive controller with the even-harmonic one.

4.5.4 Experimental verification

The prototype of the single-phase MMC shown in Figure 4.8 has been built in the laboratory. The experimental setup of the MMC platform is shown in Figure 4.18. A dSPACE module DS1006 is adopted to implement the digital control and a DSP TMS320F28335 is used to generate the phase-shifted PWM signals for sub-modules. The parameters of the MMC system are listed in Table 4.1. The equivalent arm resistors representing the losses in arms are not connected in the circuit. The modulation index of the output voltage is set to be 0.833 except for

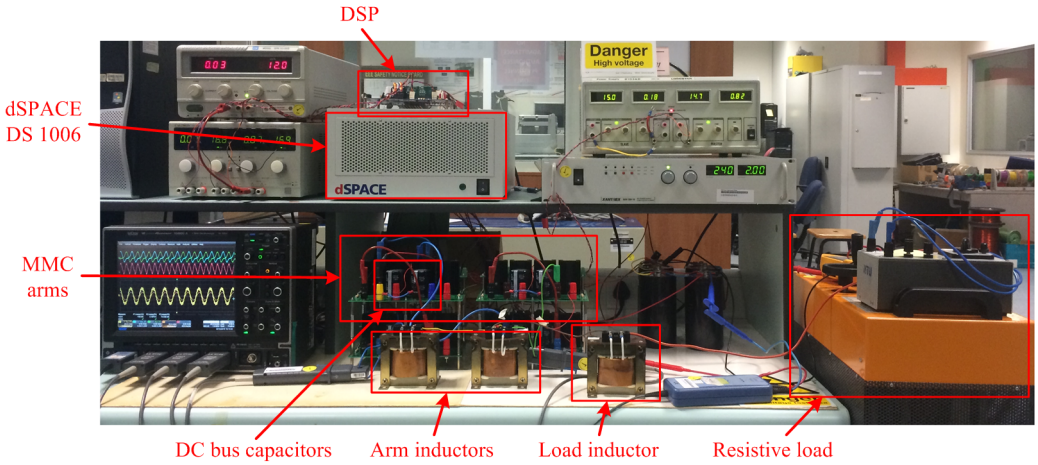


Figure 4.18: Experimental setup of the single-phase MMC.

a set of experiments under reference and load step changes.

Steady-state performance

Figure 4.19 (a) presents the voltage and current waveforms of the MMC with the even-harmonic repetitive control scheme activated at t1. It is obvious that the AC components of the differential current are reduced from 4.4 A to less than 0.8 A. The low-frequency harmonics in the circulating current are almost completely removed in a few fundamental cycles after t1. The high-frequency harmonics after t1 are mainly introduced by the switching of the semiconductor devices. The distortions in the arm currents are also removed, and only the DC and fundamental frequency components are retained as can be seen in Figure 4.19 (a). The output voltage and current are scarcely affected by the differential current even-harmonic repetitive control scheme. The average voltages and voltage ripples across sub-module capacitors are slightly affected after the repetitive controller being activated as shown in Figure 4.19 (b).

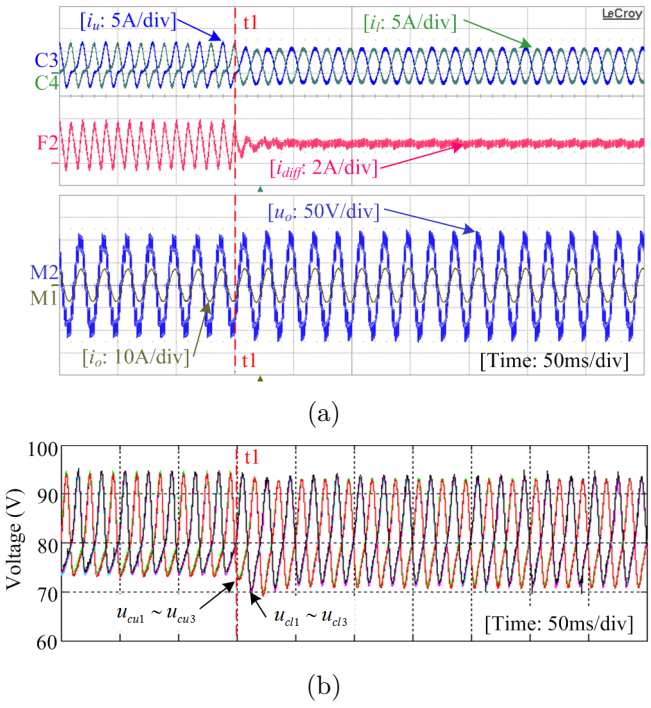


Figure 4.19: Voltage and current waveforms of the MMC when the even-harmonic repetitive controller is activated at t1: (a) arm currents, differential current, output voltage and current; (b) SM capacitor voltages.

The arm currents and inner differential current regulated by different controllers are presented in Figure 4.20 and the spectra of corresponding differential currents are illustrated in Figure 4.21. It can be seen in Figure 4.21 (a) that even order harmonics (dominated by 2^{nd} and 4^{th} harmonics) exist in the differential current if only a conventional PI controller is adopted to regulate the differential current. The differential current controlled by a PI controller with paralleled 2^{nd} and 4^{th} resonant controllers is shown in Figure 4.20 (b), where small low-frequency ripples can still be observed in i_{diff}. Its spectrum in Figure 4.21 (b) shows that the 2^{nd} and 4^{th} harmonics are well suppressed while more 6^{th} harmonics can be

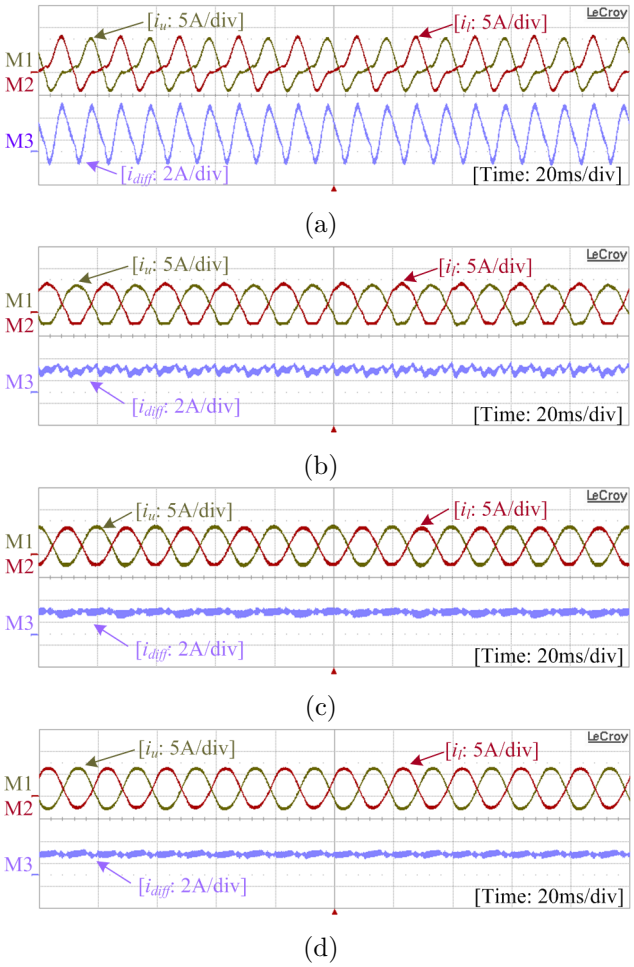


Figure 4.20: Steady state arm currents and inner differential current regulated by different controllers: (a) PI; (b) PI + 2^{nd} R + 4^{th} R; (c) Conventional RC; (d) Even-harmonic RC.

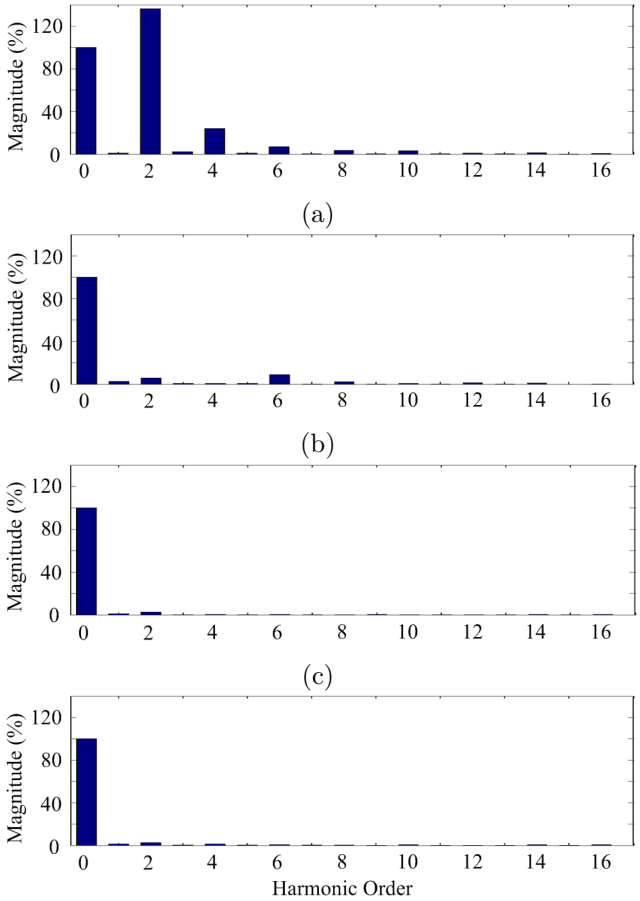


Figure 4.21: Spectra of inner differential currents regulated by different controllers: (a) PI; (b) PI + 2^{nd} R + 4^{th} R; (c) Conventional RC; (d) Even-harmonic RC.

found. The steady state performances of both conventional and even-harmonic repetitive controllers are almost the same and obviously better than those of PI and PR controllers, as shown in Figure 4.20 (c) and (d). The harmonic spectra of these two repetitive controllers presented in Figure 4.21 (c) and (d) are similar as well.

Dynamic response

The dynamic response of the repetitive control system has been investigated in this set of experiments. The transients of the differential current while activating the conventional and even-harmonic repetitive controllers are illustrated in Figure

4.22. After activating the repetitive controller at t = t1, the differential current regulated by the even-harmonic repetitive controller is converged into the shadowed range smoothly by t = t2 (55 ms), while the harmonic contents are removed by the conventional controller by t = t3 (115 ms).

The load inductance is increased to 16.3 mH in the following set of experiments

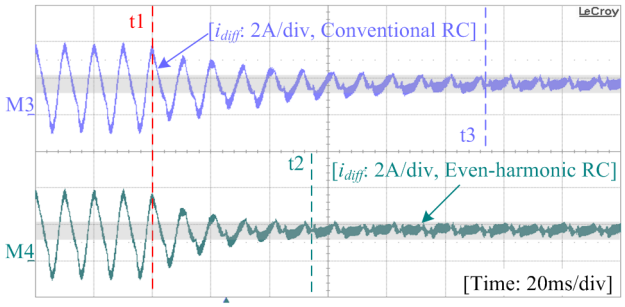


Figure 4.22: Inner differential currents of the MMC when the conventional repetitive controller and even-harmonic repetitive controller are activated.

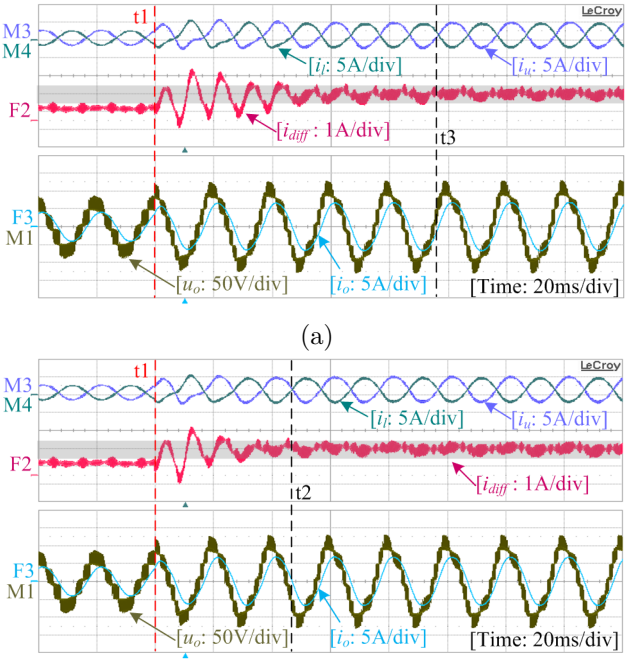


Figure 4.23: Arm currents, differential current, output voltage and current waveforms during reference step change with: (a) conventional repetitive controller; (b) even-harmonic repetitive controller.

in order to clearly show the dynamics of the control scheme under reference and load step changes with resistive-inductive loads. Figure 4.23 presents the voltage and current waveforms of the MMC regulated by the two repetitive controllers when the output voltage reference changes from 0.5 to 0.833 at t1. The dynamic performances of the two controllers when the resistive load changes from 24 Ω to 12 Ω at t1 are shown in Figure 4.24, where the power factor changes from 0.978 to 0.9198 as well. The overall control system is stable during reference and load step changes. It can be seen in both Figure 4.23 and 4.24 that i_{diff} is settled down at t2 when it is controlled by an even-harmonic repetitive controller. On the other hand, i_{diff} is stabilized at t3 if a conventional repetitive controller is adopted.

The results of this set of experiments show that the dynamic response of the even-harmonic repetitive control system is improved without severe transients.

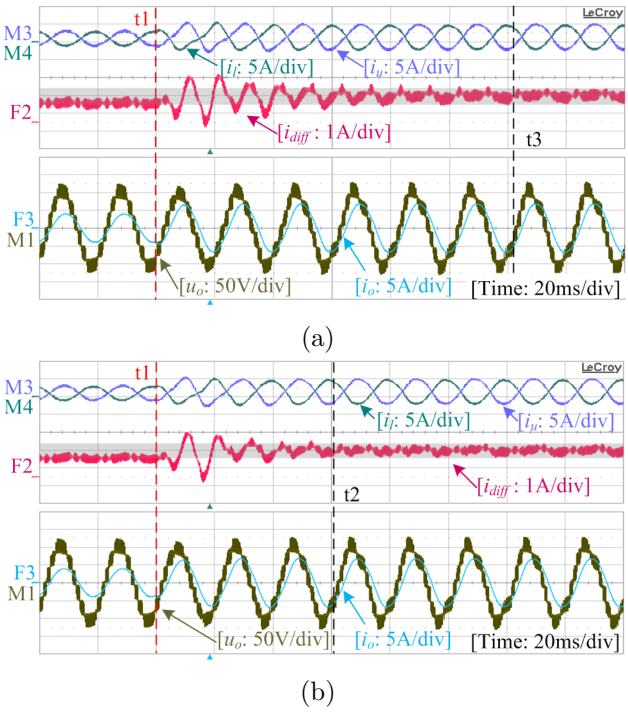


Figure 4.24: Arm currents, differential current, output voltage and current waveforms during load step change with: (a) conventional repetitive controller; (b) even-harmonic repetitive controller.

System convergence and stability

As aforementioned during the repetitive controller design in Section 4.5.2, the repetitive controller gain K_r significantly affects the overall control system convergence speed, dynamic response, and stability. A set of experiments investing the system convergence and stability of the even-harmonic repetitive control system is presented in this subsection. It can be seen in Figure 4.25 (a) that $K_r = 0.8$ offers the relatively proper convergence speed to the differential current after the even-harmonic repetitive controller being activated at t1. The current waveforms of the MMC when K_r is increased to 2.2 is shown in Figure 4.25 (b). It can be seen that the differential current of the MMC starts to oscillate if K_r increases to 2.2, which is in consistence with the system stability analysis.

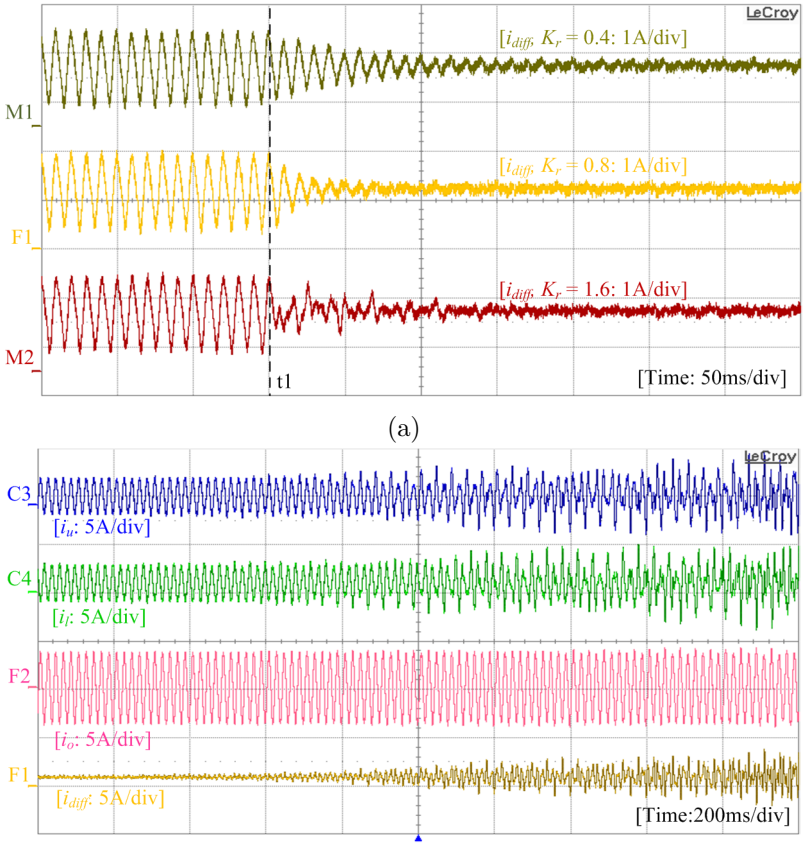


Figure 4.25: Experimental results of: (a) i_{diff} waveforms with different values of K_r; (b) Current waveforms when $K_r = 2.2$.

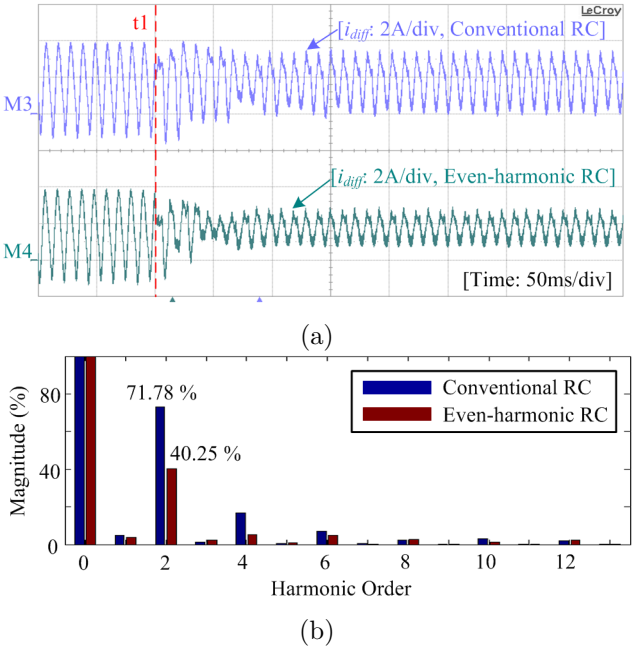


Figure 4.26: Inner differential currents regulated by different repetitive controllers at $f_o = 47.5$ Hz: (a) Waveforms of differential currents; (b) Spectra of differential currents.

Performance under frequency deviation

In Figure 4.26, a frequency deviation of $f_d = -2.5$ Hz (-5%) is intentionally applied to the MMC output voltage reference while the repetitive controller is still designed for $f_o = 50$ Hz. The experimental results suggest that the even-harmonic repetitive controller has better performance in harmonic suppression, reflecting a greater tolerance for system frequency variation than that of the conventional one. As presented in Figure 4.26 (b), the normalized second-order harmonic current is reduced by 31.5% if the conventional repetitive controller is replaced by the even-harmonic one when $f_o = 47.5$ Hz.

4.6 Summary

Circulating harmonics in the inner differential current of MMC systems introduce more power losses and might deteriorate the performance of MMCs. This chapter mainly focus on the suppression of such circulating harmonics. The existing solutions for circulating current suppression are firstly reviewed in Section 4.1. It is

found that repetitive control schemes are effective in circulating current suppression and they can be improved to exclusively cope with even-order harmonics in MMC systems.

Secondly, the contents of circulating current have been analyzed in details in Section 4.2. Some conclusions can be drawn from the analysis, such as there are only even order harmonics in the circulating current, the amplitude of these harmonics decreases with the increasing of harmonic order, and resonant frequencies are associate with those harmonics. Those characteristics of the circulating current can be used to design the even-harmonic repetitive control scheme for harmonics suppression.

Next, the repetitive control widely used in power converters, such as CVCF PWM inverter in uninterruptible power supplies, is introduced in Section 4.3. An analytical and explicit design method for the time advance unit in repetitive controllers is proposed for better control system delay compensation and system stability.

After that, an even-harmonic repetitive control scheme for the circulating current suppression is design in Section 4.4 based on the characteristics of the circulating current. Such even-harmonic repetitive control scheme not only removes the harmonics but also exhibits faster dynamic response and better performance under system frequency variation in comparison to those of conventional repetitive controllers. The frequency characteristics of the even-harmonic repetitive controller show that by reducing the number of error sampling periods, the repetitive controller is improved in terms of less chip memory occupation, shorter controller delay period, faster convergence speed, higher low-frequency gain, higher crossover frequency, and wider control bandwidth at desired frequencies.

Full design processes of the even-harmonic repetitive control scheme for a case study is presented in Section 4.5. The effectiveness and improved performance of the even-harmonic repetitive control scheme is verified in both simulations and experiments. The mathematical analysis, PLECS simulations, and experimental results agree with each other very well. The results show that the harmonics in the differential current are well suppressed. The dynamic response of the differential current control scheme is doubled, and the harmonic suppression performance under frequency variation is improved by more than 30%, compared with that under conventional repetitive controllers.

Chapter 5

Feedback Linearization based Current Control for Modular Multilevel Converters

Modular Multilevel Converters (MMCs) are Multi-Input-Multi-Output (MIMO) nonlinear systems. As introduced in Section 3.4, the control system for MMCs are required to simultaneously achieve multiple control objectives, e.g., output current regulation, sub-module capacitor voltage averaging and balancing, and circulating current suppression. Existing cascaded control strategies for MMCs achieve those control objectives with relatively complex controllers, e.g. multiple resonant controllers and repetitive controller discussed in Chapter 4. The proper controller parameters design is normally difficult and the control performance cannot be guaranteed for such nonlinear systems with coupled states. In view of this, a feedback linearization based current control for MMCs is presented in this chapter, in order to improve the control performance and facilitate the controller design.

5.1 Introduction

Modular Multilevel Converters have a relatively simpler hardware configuration compared with other multilevel topologies in high or medium voltage applications. However, the design complexity of MMC systems has been pushed from the simple topological configuration to the overall control system design, which attracts considerable research interests in recent years.

In addition to controlling the output power, efforts have to be also devoted to the control of MMC internal dynamics [87], i.e. the sub-module capacitor voltages and the inner differential current [73]. Multiple control objectives, such as output voltage or current regulation, sub-module capacitor voltage averaging and balancing, and circulating ripple currents suppression or injection, have to be simultaneously and unconditionally achieved for both load requirements and stable operation of MMC itself [71]. In order to achieve these multiple control objectives, various control strategies have been reported in the literature. The most commonly adopted control schemes are in a cascaded manner as introduced in Section 3.4. This control concept employs multiple control loops with conventional proportional or proportional-integral (PI) controllers combined with a PS-PWM scheme to regulate the MMC output and internal dynamics. However, the ripples in the differential current, which are undesired in most applications from an efficiency point of view, could not be suppressed effectively by the approach introduced in that paper. Reference [171] reveals that using a large proportional gain for suppression of the ripples in the differential current can cause oscillating currents. Therefore, more differential current control methods were proposed recently, such as feedback control in the d-q or rotating frames in [72, 138, 139] for second order harmonic suppression, multiple resonant controllers dealing with harmonics under both symmetric and unbalanced load conditions in [42,140], and plug-in repetitive controllers as proposed in Chapter 4. The design process of the controllers, especially multi-resonant and repetitive controllers, used in those systems may be complicated, and the tuning of controller parameters is difficult in order to achieve both excellent control performance and system stability [166].

As discussed in [171, 172], the control of an MIMO MMC system is a bilinear control problem. Although existing cascaded control schemes are able to achieve those control objectives, the nonlinearities and coupled states of MMCs may inevitably deteriorate the performance of the controllers and more advanced control strategies for MMCs are expected. The Model Predictive Control (MPC) based control methods that are effective and convenient in controlling MIMO systems with nonlinear and discontinuous behaviors are discussed in [74, 75, 78]. However, the computational burden of digital controllers is highly related to the MMC model complexity and the number of sub-modules in the system. The conventional MPC strategies may be not always practical due to the substantial calculation requirements [78], especially in applications where a large number of voltage levels are required. In view of this, efforts are recently devoted to improved

MPC strategies that are suitable for MMC systems with reduced computational burden [78, 80, 173]. A trajectory tracking control method that leads to the decoupling of the controller for the load and MMC internal dynamics is proposed in [174]. The control strategies based on nonlinear control methods have been discussed in [83, 84].

In this chapter, a nonlinear control strategy, where the differential geometry based feedback linearization technique [175–177] is employed, is proposed to regulate the output and inner differential currents of the single-phase MMC system shown in Figure 5.1. A state function model of the MMC system is presented, which shows that the MMC is an MIMO nonlinear system. A nonlinear control theory based strategy is naturally straightforward and theoretically effective to address the control problem of the nonlinear MMC system. Instead of using approximate linearization techniques, such as the small signal modeling adopted in [178], the feedback linearization technique, which has been adopted in power electronics applications [179–183], is applied to the MMC system transforming the MMC nonlinear state-function model to a linear one. The feedback linearization of the MMC system is mathematically developed, followed by the analysis of the system zero-dynamics stability. The output and differential current control loops of the MMC are linearized and decoupled to be simple plants. Easy-to-design controllers, i.e. proportional-resonant (PR) and PI controllers, are applied for the linearized output and differential currents controls respectively. The current controller design process for the linearized model is significantly facilitated in comparison to that of the conventional cascaded control strategies, in which the multiple resonant controllers or repetitive controllers are employed for effective circulating ripple current suppression [42, 140, 144, 145, 184].

To experimentally verify the effectiveness and improved performance of the proposed nonlinear current control, both the feedback linearization control and the conventional cascaded control strategies with plug-in repetitive controller discussed in Subsection 4.3.2 are implemented on the MMC prototype shown in Figure 4.18. The controller parameters in the feedback linearization control strategy are designed according to linear control laws. The proportional and resonant gains adopted in the two control strategies are equivalent with each other, in order to fairly evaluate the steady-state and dynamic performances of those control strategies. The experimental results are presented and compared to show the excellent steady state and dynamic performances of the feedback linearization current control. With the help of the feedback linearization control, the overall

control performance for the MMC is obviously improved. In the steady state, the output current of the MMC tracks its reference more accurately, while almost the same differential current regulation capability can be achieved compared to the conventional cascaded control strategy with a plug-in repetitive controller. The even-order harmonics in the differential current is almost completely suppressed by a simple PI controller designed for differential current regulation in the feedback linearization control. Such control is robust against the system frequency deviation while regulating the differential current. The decoupling of the two current control loops is illustrated by separately injecting harmonics into the output and differential currents. The dynamic responses of both the output and differential currents during reference step changes are significantly improved, as more accurate and faster reference tracking can be obtained with smoother transients. The robustness of the feedback linearization control against the parametric uncertainties is investigated and confirmed.

5.2 State function model of MMCs

The state function model of an MMC is derived according to Figure 5.1, which is slightly modified compared with Figure 4.8. The difference is that the output terminals of the MMC are connected to the load represented by a voltage source u_{load} via an inductor L_o.

Assuming the sub-module capacitor voltages in one arm are perfectly balanced, the average capacitor voltages in the upper and lower arms can be denoted as u_{Cu} and u_{Cl} respectively. According to the equations (2.6), (2.7), and (3.33), the

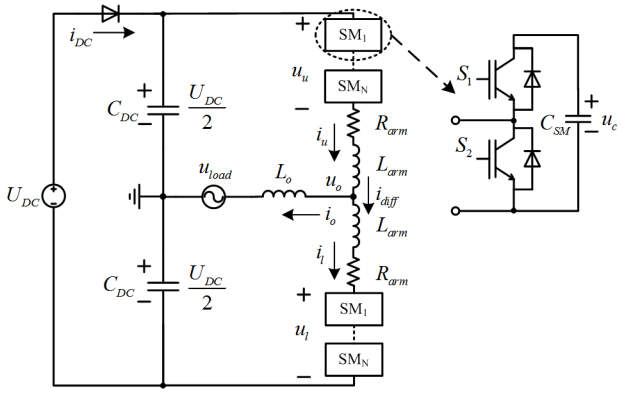


Figure 5.1: Structure of a single-phase MMC based inverter.

voltages and currents in the upper and lower arms can be calculated as

$$\begin{cases} u_u = N u_{Cu} \left[\dfrac{1 - {u_o}^*}{2} - {u_{diff}}^* \right] \\ u_l = N u_{Cl} \left[\dfrac{1 + {u_o}^*}{2} - {u_{diff}}^* \right] \end{cases} \tag{5.1}$$

$$\begin{cases} i_u = i_{diff} + \dfrac{i_o}{2} \\ i_l = i_{diff} - \dfrac{i_o}{2} \end{cases} \tag{5.2}$$

where ${u_o}^*$ and ${u_{diff}}^*$ are the normalized output and differential voltage reference signals. The output voltage of the MMC can be represented as

$$u_o = u_{load} + L_o \frac{di_o}{dt} \tag{5.3}$$

According to (2.9) and (2.10), the voltage and current quantities in the upper and lower arms can be derived as

$$\begin{cases} U_{DC} - 2u_u - 2R_{arm} i_u - 2L_{arm} \dfrac{di_u}{dt} = 2u_o \\ U_{DC} - 2u_l - 2R_{arm} i_l - 2L_{arm} \dfrac{di_l}{dt} = -2u_o \end{cases} \tag{5.4}$$

Substituting (5.2) and (5.3) into (5.4), these equations can be rearranged as

$$\begin{cases} \dfrac{di_o}{dt} = \dfrac{-R_{arm} i_o - u_u + u_l - 2u_{load}}{L_{arm} + 2L_o} \\ \dfrac{di_{diff}}{dt} = \dfrac{-2R_{arm} i_{diff} - u_u - u_l + U_{DC}}{2L_{arm}} \end{cases} \tag{5.5}$$

According to (5.1) and (5.5), it can be seen that i_o and i_{diff} can be eventually controlled by adjusting ${u_o}^*$ and ${u_{diff}}^*$. The sub-module capacitors that are inserted into each arm will be charged or discharged by the arm current and can be calculated according to [71] as

$$\begin{cases} \dfrac{du_{Cu}}{dt} = \dfrac{i_u}{C_{SM}} \left[\dfrac{1 - {u_o}^*}{2} - {u_{diff}}^* \right] \\ \dfrac{du_{Cl}}{dt} = \dfrac{i_l}{C_{SM}} \left[\dfrac{1 + {u_o}^*}{2} - {u_{diff}}^* \right] \end{cases} \tag{5.6}$$

The block diagram of the MMC system is illustrated in Figure 5.2, where

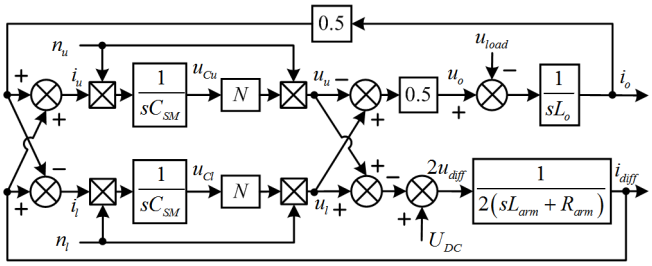


Figure 5.2: Block diagram of the MMC.

$n_u = (1 - {u_o}^*)/2 - {u_{diff}}^*$ and $n_l = (1 + {u_o}^*)/2 - {u_{diff}}^*$ are the actual control inputs of the MMC.

The state functions of the MMC can be obtained by choosing the state variables as $x = [i_o \ i_{diff} \ u_{Cu} \ u_{Cl}]^T$, and system inputs as $u = [{u_o}^* \ {u_{diff}}^*]^T$. The outputs of the MMC system are selected as $y = [i_o \ i_{diff}]^T$. The state functions of the system can then be derived as

$$\begin{cases} \dot{x} = f(x) + g_o(x){u_o}^* + g_{diff}(x){u_{diff}}^* \\ y = h(x) \end{cases} \tag{5.7}$$

where

$$f(x) = \begin{bmatrix} \frac{-2u_{load}}{L_{arm}+2L_o} & \frac{U_{DC}}{2L_{arm}} & 0 & 0 \end{bmatrix}^T + \begin{bmatrix} \frac{-R_{arm}}{L_{arm}+2L_o} & 0 & \frac{-N}{2L_{arm}+4L_o} & \frac{N}{2L_{arm}+4L_o} \\ 0 & -\frac{R_{arm}}{L_{arm}} & \frac{-N}{4L_{arm}} & \frac{-N}{4L_{arm}} \\ \frac{1}{4C_{SM}} & \frac{1}{2C_{SM}} & 0 & 0 \\ \frac{-1}{4C_{SM}} & \frac{1}{2C_{SM}} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_o \\ i_{diff} \\ u_{Cu} \\ u_{Cl} \end{bmatrix} \tag{5.8}$$

$$g_o(x) = \begin{bmatrix} \frac{N(u_{Cu}+u_{Cl})}{2L_{arm}+4L_o} & \frac{N(u_{Cu}-u_{Cl})}{4L_{arm}} & \frac{-2i_{diff}-i_o}{4C_{SM}} & \frac{2i_{diff}-i_o}{4C_{SM}} \end{bmatrix}^T \tag{5.9}$$

$$g_{diff}(x) = \begin{bmatrix} \frac{N(u_{Cu}-u_{Cl})}{L_{arm}+2L_o} & \frac{N(u_{Cu}+u_{Cl})}{2L_{arm}} & \frac{-2i_{diff}-i_o}{2C_{SM}} & \frac{i_o-2i_{diff}}{2C_{SM}} \end{bmatrix}^T \tag{5.10}$$

$$h(x) = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix} x \tag{5.11}$$

It can be seen that the MMC system is nonlinear because of the product of the state variables and the system inputs in (5.7) [185].

5.3 Input-output feedback linearization for MIMO nonlinear systems

Feedback linearization is an approach widely adopted in nonlinear system control. It algebraically transforms nonlinear system dynamics into linear ones [175, 176], so that linear control techniques can be directly applied to these systems. Unlike conventional approximate linearization methods, such as Jacobian linearization, the feedback linearization is achieved by exact state transformation and feedback. Only the basic concepts of the feedback linearization will be introduced in this Section and the detailed explanation of this technique can be found in [175–177, 186].

An MIMO nonlinear system can be described by the state functions as

$$\begin{cases} \dot{x} = f(x) + \sum_{i=1}^{m} g_i(x) u_i \\ y = \begin{bmatrix} h_1(x) & \dots & h_m(x) \end{bmatrix}^T \end{cases} \tag{5.12}$$

where x is an n-dimensional state vector, u and y are m-dimensional input and output vectors, $f(x)$, $g(x)$ are smooth functions on $\mathbb{R}^n$. The Lie derivative of the scalar function $h_i(x)$ with respect to the vector function $f(x)$ is defined as

$$L_f h_i(x) = \nabla h_i f = \frac{\partial h_i(x)}{\partial x} f(x) = \begin{bmatrix} \frac{\partial h_i(x)}{\partial x_1} & \frac{\partial h_i(x)}{\partial x_2} & \dots & \frac{\partial h_i(x)}{\partial x_n} \end{bmatrix} f(x) \tag{5.13}$$

The k^{th} Lie derivative can be defined as

$$L_f^k h_i(x) = L_f \left(L_f^{k-1} h_i(x) \right) \tag{5.14}$$

and

$$L_f^0 h_i(x) = h_i(x) \tag{5.15}$$

Moreover, in the case of another vector field g

$$L_g L_f h_i(x) = \nabla \left(L_f h_i \right) = \frac{\partial L_f h_i(x)}{\partial x} g(x) \tag{5.16}$$

The relative degree of the k^{th} output is said to be r_k at x_0 if

$$\begin{cases} L_{g_i} L_f^{r_k-2} h_k(x) = 0, \text{ for all } i = 1, 2, \ldots, m, \\ \qquad\qquad\qquad\qquad \text{and for all } x \text{ in the neighborhood of } x_0 \\ L_{g_i} L_f^{r_k-1} h_k(x) \neq 0, \text{ for some } i \end{cases} \tag{5.17}$$

With this defined relative degree, the r_k time derivatives of $h_k(x)$ can be described as

$$\begin{cases} h_k^{(l)}(x) = L_f^l h_k(x), \text{ for } l = 1,\ 2,\ \ldots,\ r_k - 1 \\ h_k^{(r_k)}(x) = L_f^{r_k} h_k(x) + \sum_{i=1}^{m} L_{g_i} L_f^{r_k-1} h_k(x) u_i = \gamma_k \end{cases} \tag{5.18}$$

where it can be seen that the input u explicitly appears in the ${r_k}^{th}$ derivative of $h_k(x)$. The map between the newly defined input γ_k and the output $h_k(x)$ is linear for all values of the state x in the neighborhood of x_0. The output $h_k(x)$ can be obtained by directly integrating the input γ_k by r_k times. The k^{th} output y_k is decoupled from input γ_i when $i \neq k$. The vector relative degree of the MIMO nonlinear system is defined as $[r_1, r_2, \ldots, r_m]$ if the equation (5.17) is always satisfied for all $k = 1, 2, \ldots, m$ and the decoupling matrix

$$E(x) = \begin{bmatrix} L_{g_1} L_f^{r_1-1} h_1(x) & \ldots & L_{g_m} L_f^{r_1-1} h_1(x) \\ \vdots & \ldots & \vdots \\ L_{g_1} L_f^{r_m-1} h_m(x) & \ldots & L_{g_m} L_f^{r_m-1} h_m(x) \end{bmatrix} \tag{5.19}$$

is non-singular at x_0. Defining

$$A(x) = \begin{bmatrix} L_f^{r_1} h_1(x) & \ldots & L_f^{r_m} h_m(x) \end{bmatrix}^T \tag{5.20}$$

the state feedback control law can be calculated as

$$u = E^{-1}(x) \left[\gamma - A(x)\right] \tag{5.21}$$

where $\gamma = [\gamma_1, \gamma_2, \ldots, \gamma_m]^T$. Note that equation (5.21) represents the nonlinear feedback transformation that transforms the nonlinear system into a linear one, whose input-output relation is linearized and decoupled [176].

There might be an internal dynamics problem regarding the input-output

feedback linearization. The system dimension or relative degree $r = \sum_{k=1}^{m} r_k$ might be smaller than the dimension of the state n. Therefore, there are $n - r$ internal dynamics that are not observable from the system outputs. The control law (5.21) guarantees the input-output stability. However, this control law not always yields a internally stable closed-loop system. Denoting the first r elements of a z vector as

$$\begin{aligned} &z_1 = L_f^0 h_1(x), \ \ldots, \ z_{r_1} = L_f^{r_1-1} h_1(x), \\ &z_{r_1+1} = L_f^0 h_2(x), \ \ldots, \ z_{r_1+r_2} = L_f^{r_2-1} h_2(x), \\ &\vdots \\ &z_{r-r_m+1} = L_f^0 h_m(x), \ \ldots, \ z_r = L_f^{r_m-1} h_m(x) \end{aligned} \tag{5.22}$$

By selecting a diffeomorphism $\phi(x)$ for each unobservable internal dynamic, the left $n - r$ elements of vector z can be denoted as $z_{r+1} = \phi_1(x), \ \ldots, \ z_n = \phi_{n-r}(x)$. The MIMO system in (5.12) can be rewritten in z coordinate as

$$\begin{aligned} &\dot{z}_1 = z_2 \\ &\dot{z}_2 = z_3 \\ &\vdots \\ &\dot{z}_{r_1} = L_f^{r_1} h_1(x) + \sum_{i=1}^{m} L_{g_i} L_f^{r_1-1} h_1(x) u_i \\ &\vdots \\ &\dot{z}_{r_1+r_2} = L_f^{r_2} h_2(x) + \sum_{i=1}^{m} L_{g_i} L_f^{r_2-1} h_2(x) u_i \\ &\vdots \\ &\dot{z}_r = L_f^{r_m} h_m(x) + \sum_{i=1}^{m} L_{g_i} L_f^{r_m-1} h_m(x) u_i \\ &\dot{z}_{r+1} = L_f \phi_1(x) = q_1(z) \\ &\vdots \\ &\dot{z}_n = L_f \phi_{n-r}(x) = q_{n-r}(z) \\ &y_1 = z_1 \\ &\vdots \\ &y_m = z_m \end{aligned} \tag{5.23}$$

Letting $\eta = [z_1 \ z_2 \ \ldots \ z_r]^T$, $\xi = [z_{r+1} \ \ldots \ z_n]^T$, and setting $\eta = 0$, the zero dynamics of the MIMO system can be defined as

$$\dot{\xi} = q(\eta, \xi) = q(0, \xi) \stackrel{\Delta}{=} q_0(\xi) \tag{5.24}$$

where

$$q(\eta,\xi) \triangleq \left[\begin{array}{ccc} q_1(\eta,\xi) & \cdots & q_{n-r}(\eta,\xi) \end{array}\right]^T \tag{5.25}$$

If the zero dynamics are stable, the nonlinear system is a minimum phase one. The input-output feedback linearization is restricted to minimum phase nonlinear systems, so that the overall nonlinear systems can be stabilized by the control law designed to regulate the system outputs.

5.4 Feedback linearization based current control for the MMC

5.4.1 Conventional cascaded control strategy for the MMC

The structure of the conventional cascaded control system discussed in Section 3.4 for the single-phase MMC is presented in Figure 5.3, which mainly consists of four parts, i.e. output current control, sub-module capacitor voltage control, inner differential current control, and individual sub-module capacitor voltage balancing. These multiple control objectives are achieved by cascaded multiple voltage and current control loops.

The reference of the output current $i_o{}^*$ is either directly given or calculated according to the output active and reactive power commands. In a single-phase system, the output current is normally controlled by G_{i_o}, e.g. a PR controller [187, 188]. Generally, the average and differential voltages in the upper and lower arms are respectively controlled by G_{Ave} and G_{Diff} [87] as shown in Figure 5.3, where $u_C{}^*$ is the reference of the sub-module capacitor voltage. The outputs of the two voltage controllers are employed as parts of the inner differential current

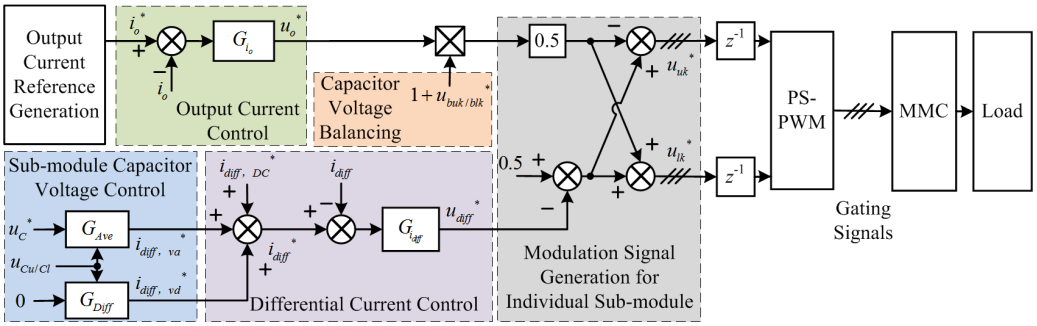


Figure 5.3: Block diagram of the conventional cascaded control system for the single-phase MMC.

reference ${i_{diff}}^*$, i.e. a DC current reference ${i_{diff,va}}^*$ to maintain the sub-module capacitor voltages in the phase leg at the same level and a fundamental frequency current reference ${i_{diff,vd}}^*$ to transfer the energy between the upper and lower arms. A third DC current reference ${i_{diff,DC}}^*$ is employed for the power balancing between the DC and AC sides of the MMC, which can be calculated according to (3.13). Conventionally, the inner differential current can be regulated by $G_{i_{diff}}$, which could be a simple PI controller [85], a PI controller with paralleled multiple resonant controllers [42, 140], or repetitive control schemes as in Chapter 4.

Although it is assumed that the sub-module capacitor voltages are balanced in MMC normal operation, an active sub-module capacitor voltage balancing scheme as introduced in Section 3.4.4 is still needed, where ${u_{buk/blk}}^*$ refer to the voltage balancing reference of the k^{th} sub-module in the upper and lower arms. Note that ${u_{buk/blk}}^*$ is normally negligible, compared to ${u_o}^*$ and ${u_{diff}}^*$, in the MMC modeling and feedback linearization current control design presented later. As illustrated in the modulation signal generation block in Figure 5.3, the reference signal for individual sub-module is generated as

$${u_{uk/lk}}^* = 0.5\left[1 \mp {u_o}^*\left(1 + {u_{buk/blk}}^*\right)\right] - {u_{diff}}^* \tag{5.26}$$

It can be seen in Figure 5.2 and Figure 5.3 that the controller outputs and the states of the MMC are coupled and interacting with each other, which might deteriorate the performance of the controllers. In order to facilitate the controller design process and improve the control performance, a feedback linearization based current control for the MMC is developed and will be discussed in the subsequent sub-sections.

5.4.2 Feedback linearization current control for the MMC

Based on the technique introduced in Section 5.3, a feedback linearization based current control is developed and applied to the MMC system. For the MMC system described by equations (5.7) - (5.11), the first Lie derivative of system output $h(x)$ respect to $f(x)$ and $g(x)$ can be calculated according to equations (5.13) - (5.16) as

$$\begin{aligned} L_{g_o}L_f^0 h_1(x) &= \frac{N(u_{Cu}+u_{Cl})}{2L_{arm}+4L_o}, \quad L_{g_{diff}}L_f^0 h_1(x) = \frac{N(u_{Cu}-u_{Cl})}{L_{arm}+2L_o}, \\ L_{g_o}L_f^0 h_2(x) &= \frac{N(u_{Cu}-u_{Cl})}{4L_{arm}}, \quad L_{g_{diff}}L_f^0 h_2(x) = \frac{N(u_{Cu}+u_{Cl})}{2L_{arm}}. \end{aligned} \tag{5.27}$$

where the first and fourth equations are definitely not equal to zero when the MMC is in normal operation ($u_{Cu} > 0$, $u_{Cl} > 0$). Therefore, the system input ${u_o}^*$ and ${u_{diff}}^*$ explicitly appears in the first Lie derivative. Based on the definition in (5.17), the vector relative degree of the MMC system is $r = [1\ 1]$. The matrices defined in (5.19) and (5.20) can be accordingly derived as

$$A(x) = L_f h(x) = \begin{bmatrix} \dfrac{-2R_{arm}i_o - N(u_{Cu} - u_{Cl}) - 4u_{load}}{2L_{arm} + 4L_o} \\ \dfrac{2U_{DC} - 4R_{arm}i_{diff} - N(u_{Cu} + u_{Cl})}{4L_{arm}} \end{bmatrix} \tag{5.28}$$

$$E(x) = \begin{bmatrix} L_{g_o}L_f^0 h_1(x) & L_{g_{diff}}L_f^0 h_1(x) \\ L_{g_o}L_f^0 h_2(x) & L_{g_{diff}}L_f^0 h_2(x) \end{bmatrix} \tag{5.29}$$

The decoupling matrix $E(x)$ is nonsingular in the whole operating range of the MMC since $u_{Cu} \approx u_{Cl} \approx U_{DC}/N$. The new inputs of the MMC can be selected as $\gamma = [\dot{i}_o\ \dot{i}_{diff}]^T$, which can be regulated by a linear control law. The actual system inputs u used to generate the modulation signals can then be calculated from γ based on (5.21), as

$$\begin{bmatrix} {u_o}^* \\ {u_{diff}}^* \end{bmatrix} = \begin{bmatrix} \dfrac{(u_{Cu} + u_{Cl})(L_{arm} + 2L_o)}{2Nu_{Cu}u_{Cl}} & \dfrac{(u_{Cl} - u_{Cu})L_{arm}}{Nu_{Cu}u_{Cl}} \\ \dfrac{(u_{Cl} - u_{Cu})(L_{arm} + 2L_o)}{4Nu_{Cu}u_{Cl}} & \dfrac{(u_{Cu} + u_{Cl})L_{arm}}{2Nu_{Cu}u_{Cl}} \end{bmatrix} \begin{bmatrix} \gamma_1 - A_1 \\ \gamma_2 - A_2 \end{bmatrix} \tag{5.30}$$

Note that the states feedback (i_o, i_{diff}, u_{Cu} and u_{Cl}) and external voltages (u_{load} and U_{DC}) are employed in (5.30) to calculate the actual system inputs u. Ignoring ${u_{buk/blk}}^*$ as discussed in Section 5.4.1, the block diagram of the proposed MMC control strategy is presented in Figure 5.4. With the help of the feedback

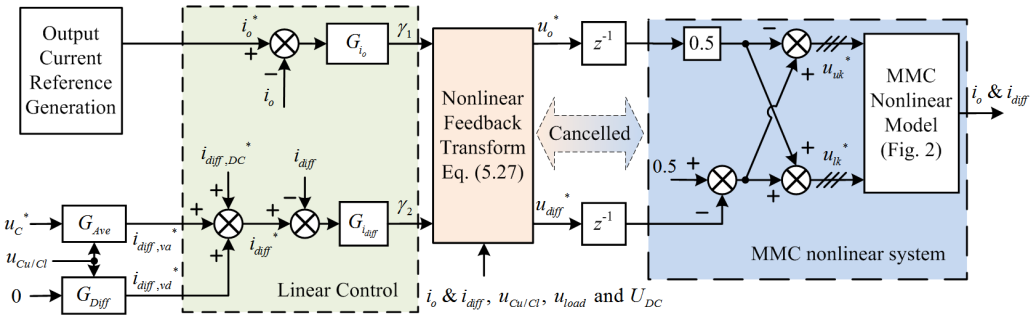


Figure 5.4: Block diagram of the feedback linearization based control.

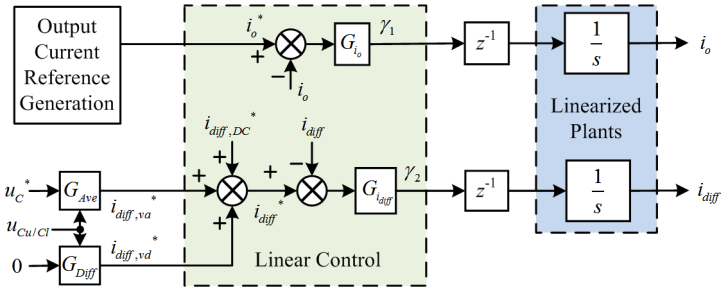


Figure 5.5: Simplified control block diagram of the MMC after feedback linearization.

linearization technique, the nonlinearities and coupled terms in the nonlinear feedback transformation block and the MMC system as the plant of the control system can be canceled and decoupled. Therefore, the plants of the linear controllers in Figure 5.4 can be linearized and significantly simplified, as shown in Figure 5.5. It is clear in Figure 5.5 that the plants of the two linear current controllers are transformed to be two completely decoupled integrators by feedback linearization. The linear current controller design and controller parameter selection can be conveniently achieved based on these simple linearized plants. Although the number of sub-modules in each arm N appears in the matrices $A(x)$ and $E(x)$, it is eventually not present in the linearized MMC shown in Figure 5.5, which implies that the generality of the feedback linearization based current control is theoretically uninfluenced by different values of N.

5.4.3 Zero-dynamics check of the MMC nonlinear system

It is found that the relative degree of the MMC system is $r_1 + r_2 = 2$, which is less than the dimension of the system $n = 4$. There is a $n - r$ dimensional subsystem containing two leftover dynamics (u_{Cu} and u_{Cl}) that are not observable from the outputs. Such unobservable internal dynamics might lead to the overall system instability. In this case, the MMC system can be stabilized by the controllers designed for the input-output dynamics only if the system zero dynamics are stable [176, 177]. Therefore, the zero dynamics stability of the MMC system has to be verified before actually applying the input-output feedback linearization to the MMC system.

The internal dynamics u_{Cu} and u_{Cl} can be described according to (5.2), (5.3),

(5.6), (5.28) and (5.30), as

$$\begin{cases} \dfrac{du_{Cu}}{dt} = -\dfrac{L_{arm}\dot{i}_o + R_{arm}i_o + 2u_o + 2L_{arm}\dot{i}_{diff} + 2R_{arm}i_{diff} - U_{DC}}{4C_{SM}Nu_{Cu}}(2i_{diff}+i_o) \\ \dfrac{du_{Cl}}{dt} = \dfrac{L_{arm}\dot{i}_o + R_{arm}i_o + 2u_o - 2L_{arm}\dot{i}_{diff} - 2R_{arm}i_{diff} + U_{DC}}{4C_{SM}Nu_{Cl}}(2i_{diff} - i_o) \end{cases} \tag{5.31}$$

They are called the zero dynamics if the tracking errors of the system outputs vanish [179]. As the system output tracking errors approaching zero, u_o, i_o, and i_{diff} can be expressed as

$$\begin{cases} u_o = U_o\cos(\omega_o t) \\ i_o = I_o\cos(\omega_o t + \phi_{i_o}) \\ i_{diff} = I_{diff,DC} + I_{diff,vd}\cos(\omega_o t) \end{cases} \tag{5.32}$$

Ignoring the voltage ripples on the sub-module capacitors, the two components of i_{diff} can be written as

$$\begin{cases} I_{diff,DC} = \dfrac{2U_{DC} - N(u_{Cu} + u_{Cl})}{4R_{arm}} \\ I_{diff,vd} = K(u_{Cu} - u_{Cl}) \end{cases} \tag{5.33}$$

where $I_{diff,DC}$ refers to a DC component in i_{diff} that balances the input and output power of the MMC, and $I_{diff,vd}$ is the output of the differential voltage controller that eliminates the voltage difference between the upper and lower arms [71]. Such voltage control loop is necessary to stabilize the capacitor voltage expressed in equation (5.31).

$$\begin{cases} \dfrac{du_{Cu}}{dt} = \dfrac{1}{8C_{SM}Nu_{Cu}}\Big\{2NI_{diff,DC}(u_{Cu} + u_{Cl}) \\ \qquad - 4I_{diff,vd}\left[R_{arm}I_o\cos(\phi_{i_o}) + U_o + R_{arm}I_{diff,vd}\right] \\ \qquad - R_{arm}{I_o}^2 - 2U_oI_o\cos(\phi_{i_o})\Big\} + \text{AC terms} \\ \dfrac{du_{Cl}}{dt} = \dfrac{1}{8C_{SM}Nu_{Cu}}\Big\{2NI_{diff,DC}(u_{Cu} + u_{Cl}) \\ \qquad + 4I_{diff,vd}\left[R_{arm}I_o\cos(\phi_{i_o}) + U_o - R_{arm}I_{diff,vd}\right] \\ \qquad - R_{arm}{I_o}^2 - 2U_oI_o\cos(\phi_{i_o})\Big\} + \text{AC terms} \end{cases} \tag{5.34}$$

A simple proportional controller with a gain K is assumed for the differential voltage control. Substituting (5.32) into (5.31), the zero dynamics can be obtained as in (5.34). Note that the DC components in (5.34) contribute to the shifting of sub-module capacitor voltages, and the AC terms only introduce ripples to the sub-module capacitor voltage. Therefore, only the DC components are taken into account while analyzing the stability of the zero dynamics.

The situation that $u_{Cu} \neq u_{Cl}$ is firstly investigated and the phase trajectories of the zero dynamics are depicted in Figure 5.6. It can be seen that if u_{Cu} and u_{Cl} differ from each other, they will be forced to move towards each other and converge to a new balanced point where $u_{Cu} = u_{Cl}$, with the help of the differential voltage controller. Figure 5.6 also reveals that the condition of $u_{Cu} = u_{Cl}$ can be guaranteed at different operation points.

Thus, it is possible to analyze the zero dynamics considering $u_{Cu} = u_{Cl}$ in the full operation range of the MMC as long as a stable differential voltage controller is adopted. The phase trajectory of the zero dynamics when $u_C = u_{Cu} = u_{Cl}$ is

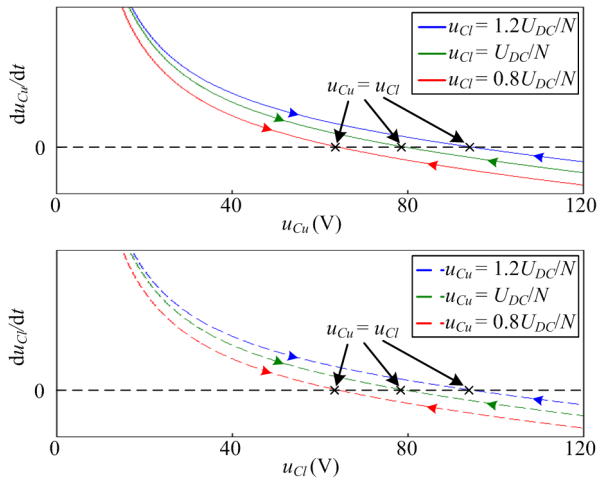


Figure 5.6: Phase trajectory of the zero dynamics when $u_{Cu} \neq u_{Cl}$.

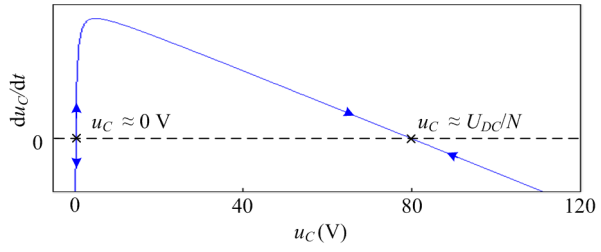


Figure 5.7: Phase trajectory of the zero dynamics considering $u_C = u_{Cu} = u_{Cl}$.

presented in Figure 5.7, where two equilibrium points can be found. The directions of the arrows near the two equilibrium points indicate that the smaller equilibrium point ($u_C \approx 0$ V) is unstable whereas the one close to U_{DC}/N is stable. Note that $u_C \approx 0$ V is generally out of the operation range of an MMC, otherwise the output voltage or current of the MMC is hardly able to track its reference. Hence, the stable equilibrium point suggests that the zero dynamics of the MMC are stable in its normal operation. The zero dynamics stability analysis implies that the MMC can be stabilized by the controllers properly designed for the linearized input-output dynamics [179,186]. It is feasible to apply the input-output feedback linearization technique to the MMC system.

5.5 Overall control system design for the MMC

The MMC prototype is the same as in Figure 4.18 and its parameters are listed in Table 5.1. Three sub-modules are connected in series in each arm. The carrier frequency of each sub-module is 2 kHz. The equivalent switching frequency of the MMC is 12 kHz. The sampling frequency is designed to be $f_s = 12$ kHz and the control system is synchronized with it, having a period of $T_s = 1/f_s$. The arm currents, sub-module capacitor voltages, DC bus voltage, and load voltage are measured for the MMC feedback linearization control strategy implementation. The block diagram of the overall control system including current controllers, voltage controllers, digital control delays, and the MMC model is presented in Figure 5.8.

Table 5.1: Parameters of the single-phase MMC system

Parameter	**Value**
DC bus voltage: U_{DC}	240 V
DC bus capacitance: C_{DC}	4.4 mF
Output inductance: L_o	0.7 mH
Rated output frequency: f_o	50 Hz
No. SM in each arm: N	3
Arm inductance: L_{arm}	5 mH
Arm resistor: R_{arm}	0.025 Ω
SM capacitor: C_{SM}	940 μF
Carrier frequency: f_c	2 kHz

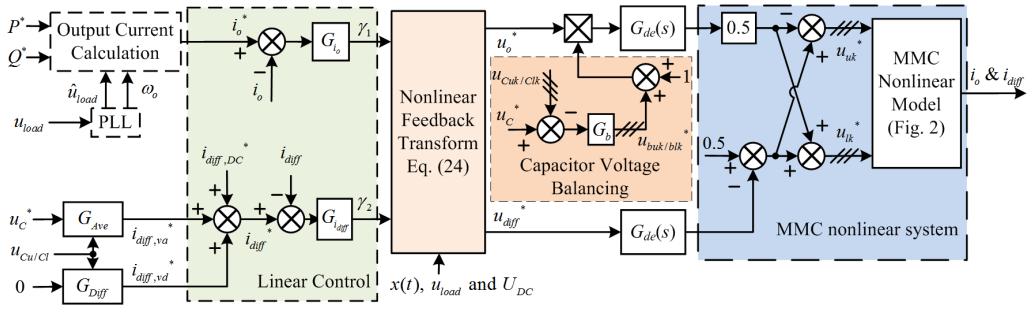


Figure 5.8: Block diagram of the MMC feedback linearization control.

5.5.1 Current controller design for the linearized MMC

For grid-connected applications, the phase-locked-loop (PLL) [189] can be adopted to obtain the phase angle and amplitude of the load voltage. The reference of the output current $i_o{}^*$ can be calculated according to the output power commands. The inner differential current reference $i_{diff}{}^*$ is obtained from the sub-module capacitor voltage control and the active power balancing. The DC current reference for power balancing is set to be $i_{diff,DC}{}^* = U_o I_o \cos(\phi_{i_o})/(2U_{DC})$. According to the linearized and decoupled plants in Figure 5.5, linear controllers for i_o and i_{diff} can be selected.

Since a single-phase MMC is investigated in this chapter, the new input $\gamma_1 = \dot{i}_o$ can be obtained by a PR controller as

$$\dot{i}_o = \left(K_{P1} + \frac{2K_r \omega_{cf} s}{s^2 + 2\omega_{cf} s + {\omega_o}^2} \right) ({i_o}^* - i_o) \tag{5.35}$$

where K_{P1} and K_r are the proportional and resonant gains respectively, and ω_{cf} is the resonant cutoff frequency [170]. The other new input $\gamma_2 = \dot{i}_{diff}$ is generated by a PI controller as

$$\dot{i}_{diff} = \left(K_{P2} + \frac{K_i}{s} \right) ({i_{diff}}^* - i_{diff}) \tag{5.36}$$

where K_{P2} and K_i are the proportional and integral gains respectively.

The inherent computation and PWM delays exist in digital control systems [170]. The voltage and current quantities required by the feedback linearization control are sampled every T_s seconds. The corresponding duty cycle for each submodule are calculated based on these samples in the current sampling interval and then updated in the next sampling instance, which introduces one sampling period

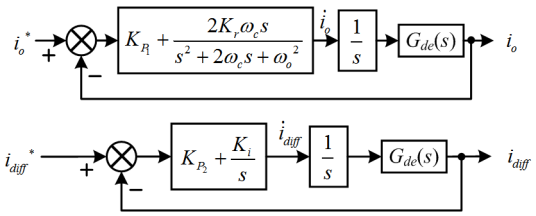


Figure 5.9: Simplified i_o and i_{diff} control loops.

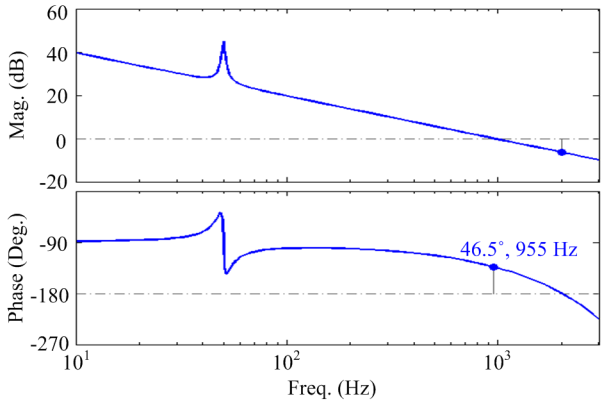


Figure 5.10: Output current control open-loop bode diagram.

computation delay. The PWM modulation is treated as a zero-order-hold (ZOH) block with 0.5 T_s delay [170]. The total delay introduced by the digital control system is 1.5 sampling periods and can be expressed as $G_{de}(s) = e^{-1.5sT_s}$. Such delays may lead to overall system instability and have to be considered during the controller parameter design. The linearized i_o and i_{diff} control loops are shown in Figure 5.9.

The parameters of the current controllers can be designed according to the control loops shown in Figure 5.9. The controller parameters for output current control loop is selected as $K_{P1} = 6000$, $\omega_{cf} = 0.01\omega_o$ and $K_r = 50000$ to ensure the crossover frequency of the control loop is 955 Hz with a phase margin of 46.5°, as indicated in Figure 5.10. Similarly, K_{P2} is selected to be 5000 for a crossover frequency of 796 Hz with a phase margin of 54.2°to effectively regulate i_{diff} and reject the even-order harmonics in the differential current. K_i is selected to be 500 that is far smaller than K_{P2} in order to reduce the current overshoot [177].

For comparison, the conventional cascaded control strategy shown in Figure 5.3 is implemented as the benchmark. The output current is regulated by a PR controller and the differential current is controlled by the plug-in repetitive

Table 5.2: Controller parameters

Feedback Linearization Control	
Proportional Gain for i_o: K_{P1}	6000 s^{-1}
Resonant Gain for i_o: K_r	50000 s^{-1}
Proportional Gain for i_{diff}: K_{P2}	5000 s^{-1}
Integral Gain for i_{diff}: K_i	500 s^{-1}
Conventional Cascaded Control	
Proportional Gain for i_o: K_{P1}	0.16 V/A
Resonant Gain for i_o: K_r	1.35 V/A
Proportional Gain for i_{diff}: K_{P2}	0.1 V/A
Integral Gain for i_{diff}: K_i	0.2 V/(A · s)
Repetitive Control Gain: K_{RC}	0.8 A/A

control scheme as detailed in Chapter 4 due to its excellent performance in suppressing the harmonics of differential current and relatively fast dynamic response. Relatively fair comparisons between the feedback linearization and conventional control strategies can be achieved, since the control system structures and computational burden of the two strategies are similar, and equivalent switching frequency and controller parameters can be adopted. The controller parameters for the traditional cascaded control strategy have to be normalized so that they are equivalent to those used in the feedback linearization control. Substituting $u_{Cu} = u_{Cl} = U_{DC}/N$ into (5.30), the ratio from γ to u can be obtained as

$$\begin{cases} {u_o}^* = \dfrac{L_{arm} + 2L_o}{U_{DC}} (\gamma_1 - A_1) \\ {u_{diff}}^* = \dfrac{L_{arm}}{U_{DC}} (\gamma_2 - A_2) \end{cases} \Rightarrow \begin{cases} \dfrac{{u_o}^*}{\gamma_1} \propto \dfrac{L_{arm} + 2L_o}{U_{DC}} \\ \dfrac{{u_{diff}}^*}{\gamma_2} \propto \dfrac{L_{arm}}{U_{DC}} \end{cases} \tag{5.37}$$

The proportional and resonant gains of the traditional cascaded control strategy approximately equivalent to those of the feedback nonlinear control can be obtained with the help of (5.37). For instance, the proportional and resonant gains of i_o control loop in the conventional control strategy is set to be about $(L_{arm} + 2L_o)/U_{DC}$ times of the ones adopted in the feedback linearization based control. The controller parameters employed for both current control strategies are listed in Table 5.2.

5.5.2 Sub-module capacitor voltage control and balancing

The sub-module capacitor voltages are also controlled for the stable operation.

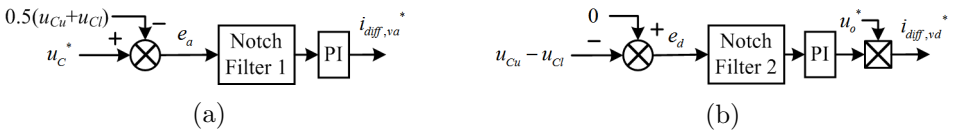


Figure 5.11: Control loops for sub-module capacitor voltages: (a) Average voltage control; (b) Differential voltage control.

The capacitor voltage averaging and differential voltage control are achieved by the voltage controllers G_{Ave} and G_{Diff}, whose detailed block diagrams are given by Figure 5.11. The output of the capacitor voltage averaging PI controller is treated as ${i_{diff,va}}^*$. The output of the differential voltage PI controller, as the amplitude of ${i_{diff,vd}}^*$, is multiplied by ${u_o}^*$ to generate ${i_{diff,vd}}^*$ with the fundamental frequency. According to the capacitor voltage ripples derived in (3.16) and (3.17), there exist second-order ripples in $u_{Cu} + u_{Cl}$ and fundamental ripples in $u_{Cu} - u_{Cl}$. Such voltage ripples introduce extra disturbances to the current references. Therefore, the voltage ripples are removed from the voltage control loops with the help of the notch filters shown in Figure 5.11, whose transfer functions are expressed as

$$\begin{cases} \text{Notch Filter 1} = \dfrac{s^2 + (2\omega_o)^2}{s^2 + 2\omega_o s/Q + (2\omega_o)^2} \\ \text{Notch Filter 2} = \dfrac{s^2 + {\omega_o}^2}{s^2 + \omega_o s/Q + {\omega_o}^2} \end{cases} \tag{5.38}$$

where Q is the quality factor of the notch filters. An individual sub-module capacitor voltage balancing scheme [190] as shown in Figure 5.8 is implemented, where G_b is a PI controller, $u_{Cuk/Clk}$ is the capacitor voltage of the k^{th} sub-module in the upper and lower arms respectively. The sub-module capacitor voltage balancing is achieved by slightly adjusting the output reference of each sub-module, which means that the sub-module with higher capacitor voltage has to provide a little bit more output active power to reduce the voltage across it, and vice versa.

5.5.3 Modulation scheme

The phase-shifted PWM (PS-PWM) modulation scheme introduced in Subsection 3.4.5 is employed to generate corresponding gating signals for each sub-module. The phase displacement of triangular carriers for sub-modules in one arm is $2\pi/N$,

and no phase displacement is required between the upper and lower arm triangular carriers [118, 119]. By doing this, the output voltage level is $2N + 1$ and the equivalent switching frequency is $2Nf_c$.

5.6 Experimental Verification

The single-phase MMC inverter shown in Figure 5.1, whose detailed parameters are listed in Table 5.1, was built in the laboratory. The feedback linearization control is implemented in a dSPACE module DS1006 and PS-PWM signals are generated in a DSP TMS320F28335. Different phase offset values are assigned to the corresponding registers of different PWM channels in TMS320F28335, in order to generate the phase-shifted carriers. The voltage and current quantities required by the feedback linearization control are sampled every T_s seconds to calculate the modulation signals for each sub-module in the dSPACE module. The calculated modulation signals are sent to TMS320F28335 and used to update the PWM duty cycles at the next sampling instance. A resistive load of 7.5 Ω is adopted. The steady state and dynamic performances of the feedback linearization control are experimentally validated and compared with those of the conventional control strategy. The robustness of the control system against parametric uncertainties is tested as well.

5.6.1 Steady-state performance

The steady-state performance of the MMC regulated by the feedback linearization control has been investigated in this set of experiments. The amplitude of the output current is 12 A in the steady-state performance verification experiments.

The steady-state performance of the MMC regulated by the feedback linearization control is illustrated in Figure 5.12. It can be seen that the output and differential currents are well regulated with the help of the nonlinear control method and the MMC operates stably with balanced sub-module capacitor voltages. For comparison, the voltage and current waveforms of the MMC under the control strategy used in Chapter 4 are shown in Figure 5.13.

Figure 5.14 presents the output current tracking errors of the MMC regulated by the traditional cascaded control and feedback linearization control strategies respectively. It is evident that the feedback linearization control is able to achieve better output current tracking accuracy (peak to peak tracking error is less than

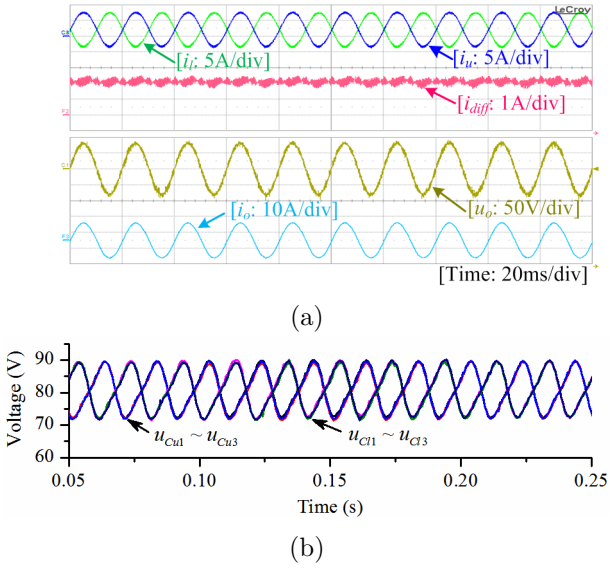


Figure 5.12: Voltage and current waveforms of the MMC regulated by feedback linearization control: (a) Waveforms of arm currents, differential current, output voltage and current; (b) Sub-module capacitor voltages.

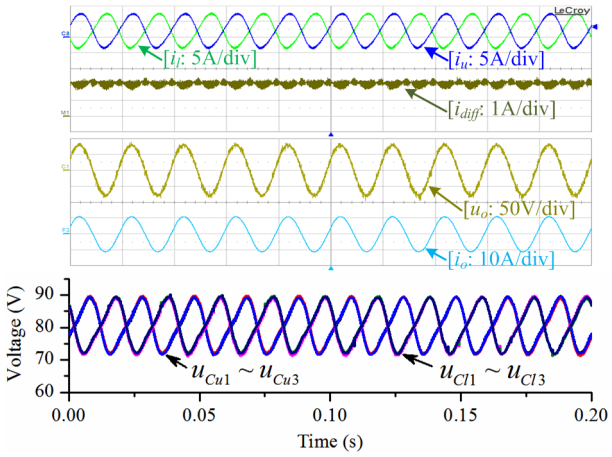


Figure 5.13: Voltage and current waveforms of the MMC regulated by the conventional cascaded control.

0.7 A) than that of the conventional control strategy. The differential currents in the MMC regulated by the conventional and feedback linearization control strategies are shown in Figure 5.15 (a) and the spectra of these differential currents are given in Figure 5.15 (b). It is clear in Figure 5.15 that even-order harmonics can be obviously found in the differential current if it is only regulated by the PI con-

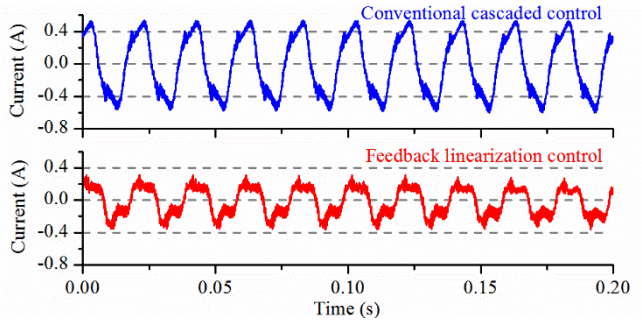


Figure 5.14: Output current i_o tracking error.

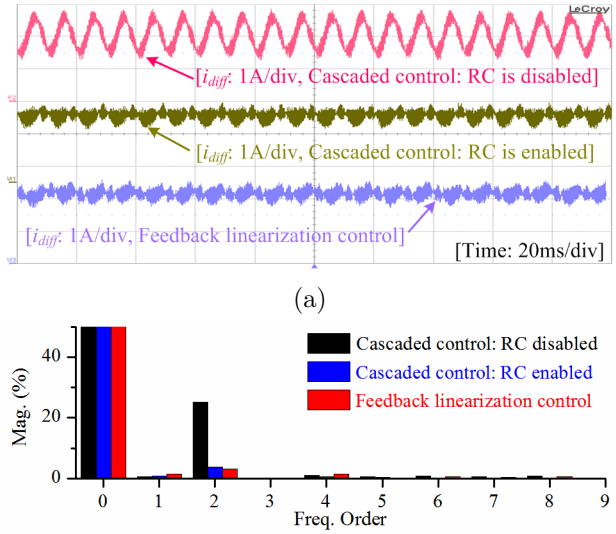


Figure 5.15: Differential currents regulated by different control strategies: (a) Waveforms of the differential currents; (b) Spectra of differential currents.

troller (repetitive controller is disabled) in the existing cascaded control strategy. On the other hand, with the aid of the feedback linearization, the harmonics in the differential current can be significantly reduced from 25% to 3.22% (with respect to the DC component in the differential current) by a simple PI controller with equivalent parameters. The plant of the i_{diff} control loop exhibited in Figure 5.5 is linearized and decoupled as a simple integrator as a result of feedback linearization, and there is no disturbance from the capacitor voltage ripples. Therefore, a properly designed PI controller is sufficient to regulate a DC quantity, i.e. i_{diff}, according to its reference. The feedback linearization control offers similar current harmonics reduction capability with that of the repetitive controller, while

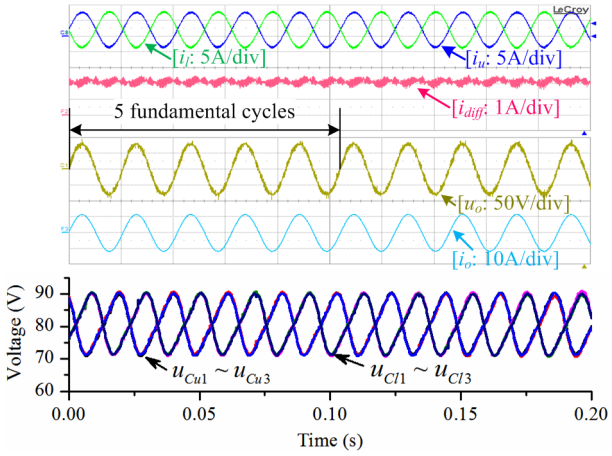
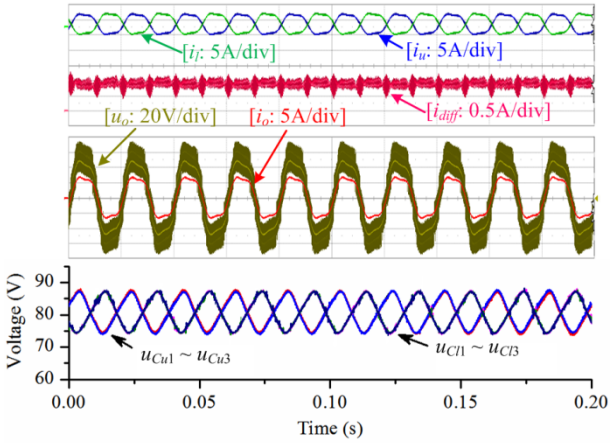


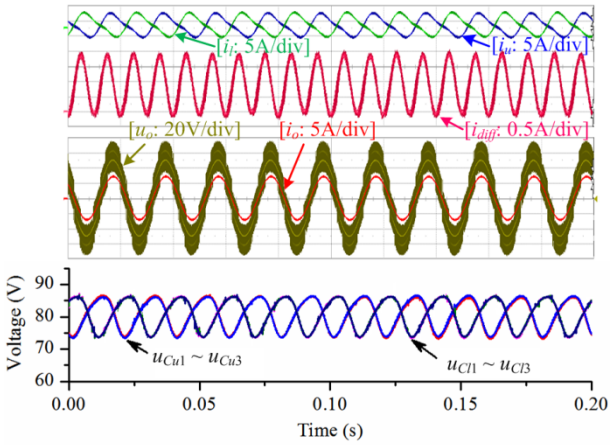
Figure 5.16: Voltage and current waveforms of the MMC regulated by the feedback linearization control when the system frequency is 48 Hz.

the controller design process is greatly facilitated. Unlike the repetitive control scheme discussed in Chapter 4, the inner differential current regulation from the feedback linearization control will not be affected by system frequency variation and deviation. As can be seen in Figure 5.16, the ripples in the differential current are well suppressed when the system fundamental frequency is deviated to be 48 Hz. On the other hand, the multi-resonant controllers or repetitive controller have to be specially designed for applications with small system frequency deviation [42, 157]. Particularly, the design process of repetitive controllers with frequency adaptive capability is quite complex as presented in [157].

The experimental results investigating the decoupling of the output and differential current control loops are presented in Figure 5.17. The amplitude of the fundamental output current is set to be 8 A and the DC component in the differential current is accordingly regulated to compensate the active power of the load. Figure 5.17 (a) shows the voltage and current waveforms when a third order harmonic with an amplitude of 2 A is intentionally injected into the output current. The figure clearly shows that the differential current is scarcely affected and still regulated to be a DC with negligible harmonics even the arm currents and the output current are highly distorted by the injected harmonic. On the other hand, a second order harmonic with an amplitude of 1 A is injected into the differential current, as shown in Figure 5.17 (b). Similarly, the output current is still sinusoidal while the differential and arm currents are distorted by the injected second order harmonic. The experimental results confirm that the output and



(a)

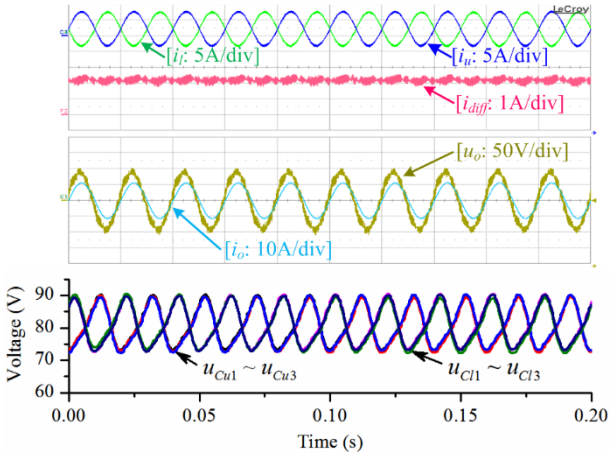


(b)

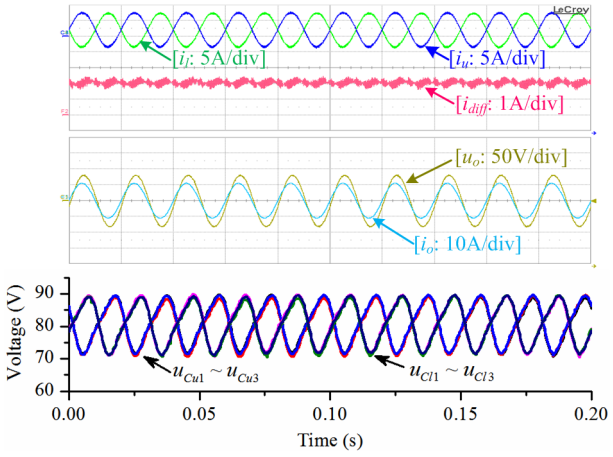
Figure 5.17: Voltage and current waveforms of the MMC regulated by the feedback linearization control with: (a) 3^{rd} order harmonic injected into i_o; (b) 2^{nd} order harmonic injected into i_{diff}.

differential currents can be controlled independently through the two decoupled current control loops.

The effectiveness of the feedback linearization based control under different load characteristics has been verified by the following set of experiments, in which resistive-inductive and resistive-capacitive loads are connected to the MMC while the output current reference is maintained the same. Figure 5.18 (a) depicts the experimental results when a 5 mH inductor is connected in series with the load resistor and Figure 5.18 (b) shows the waveforms of the MMC while a 105 μF capacitor is paralleled with the load resistor. The experimental results presented



(a)



(b)

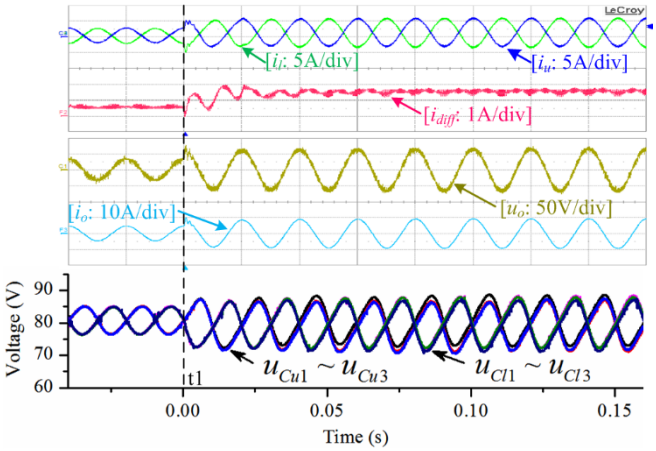
Figure 5.18: Voltage and current waveforms of the MMC regulated by the feedback linearization control with: (a) Resistive-inductive load; (b) Resistive-capacitive load.

in Figure 5.18 confirm that the control strategy can effectively regulate the MMC output and differential currents with different load characteristics.

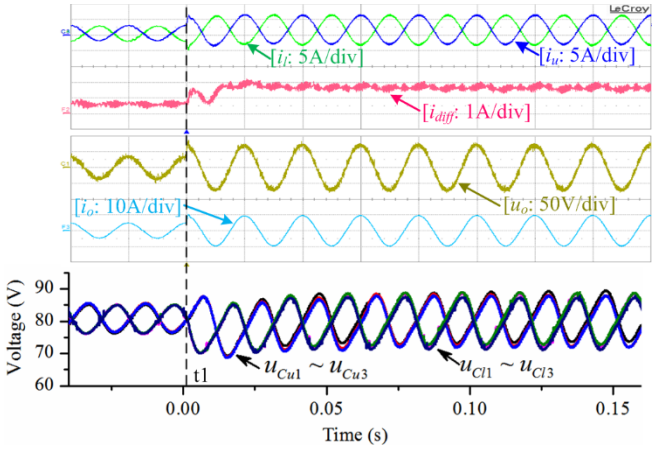
5.6.2 Dynamic response

The dynamic response of the MMC with the feedback linearization control has been evaluated in the following set of experiments, where the amplitude of the output current reference is changed from 5 A to 10 A at the time of t1.

The voltage and current waveforms of the MMC with the feedback lineariza-



(a)



(b)

Figure 5.19: Voltage and current waveforms when the amplitude of $i_o{}^*$ changes from 5 A to 10 A under: (a) Conventional cascaded control; (b) Feedback linearization control.

tion control during the $i_o{}^*$ step change are presented in Figure 5.19 (b), where it can be seen that the MMC system is stable during large operation point step changes and the transients are smooth as well. It takes about one fundamental period before the differential current is settled at the new operation point after the $i_o{}^*$ step change. Note that this apparent slow response of i_{diff} is introduced by the delayed updating of $i_{diff,DC}{}^*$, which is calculated for active power balancing according to u_{load} and i_o. A saturation nonlinearity of ± 0.95 is incorporated in the control system to limit $u_o{}^*$. As can be seen in Figure 5.20, when $i_o{}^*$ is changed at the time of t1, the output of the i_o control loop, i.e. $u_o{}^*$, is saturated

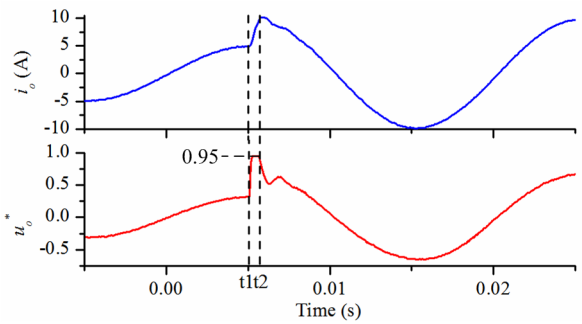
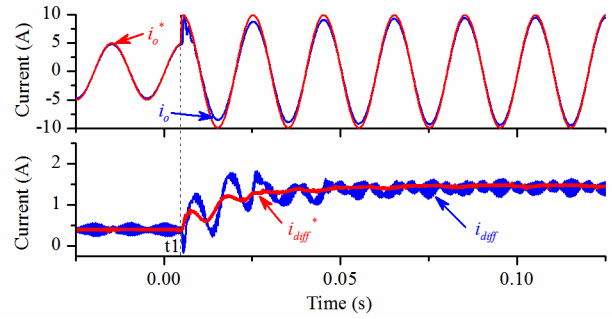
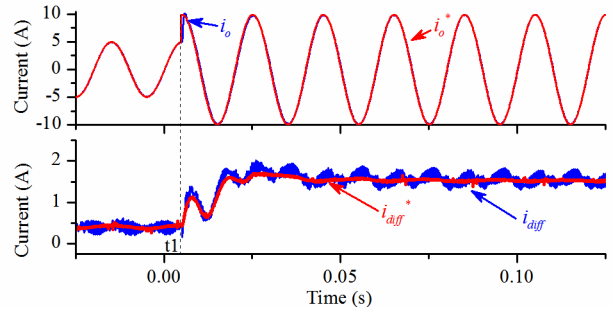


Figure 5.20: Waveforms of i_o and $u_o{}^*$ during $i_o{}^*$ step change with the feedback linearization control.



(a)

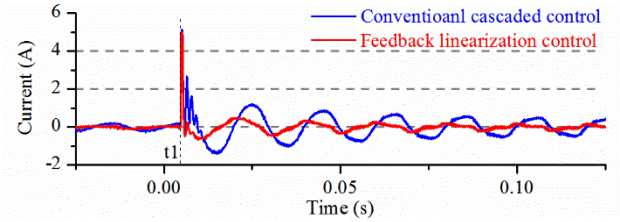


(b)

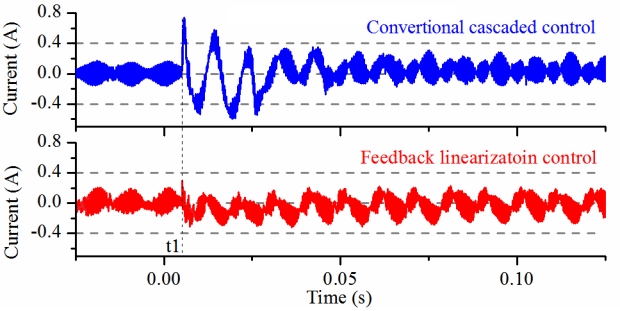
Figure 5.21: Output and differential currents references and waveforms with different control strategies: (a) Conventional cascaded control; (b) Feedback linearization control.

and limited as 0.95 until t2. Such control action saturation limits the raising rate of the output current and slightly slows down the dynamic response of the current controller in tracking the reference step changes.

The dynamic response of the MMC is illustrated in details in Figure 5.21 and Figure 5.22, by comparing the current waveforms with references and the tracking



(a)



(b)

Figure 5.22: Currents tracking errors regulated by different controllers: (a) Output current tracking errors; (b) Differential current tracking errors.

accuracy during reference step changes. The plug-in repetitive controller in the conventional cascaded control strategy is always enabled in these experiments. It is obvious in Figure 5.21 (b) that the differential current regulated by the PI plus repetitive controller is hardly able to track the reference during the dynamic process. Oscillations can be observed as well in the output current regulated by a normal PR controller in the conventional cascaded control strategy when $i_o{}^*$ changes at t1, and the output current tracks the reference accurately after $3-4$ fundamental cycles. In contrast, the output and differential currents regulated by the proposed feedback linearization control with equivalent controller parameters track the references fast and smoothly during the entire dynamic process without observable overshoot and oscillation.

The output current tracking errors shown in Figure 5.22 indicate that, after the reference step change, the i_o tracking error of the feedback linearization control rapidly converges to less than 0.25 A while larger tracking error with longer duration can be found if i_o is regulated by the traditional cascaded control strategy. Figure 5.22 (b) shows that the differential current tracking error of the PI plus repetitive controller in the cascaded control strategy is small at steady state. However, significant tracking errors can be found in dynamic processes. On the

other hand, the differential current tracking error of the feedback linearization based controller is scarcely affected by $i_o{}^*$ step changes and is always within a small range of 0.3 A. The relatively higher tracking error after $i_o{}^*$ being set to 10 A is caused by the larger disturbances introduced by the increased output current.

5.6.3 Robustness against parametric uncertainties

The robustness in the presence of parametric uncertainties of the proposed control strategy has been tested for the case that the arm inductance L_{arm} is perturbed from its nominal value 5 mH, since L_{arm} appears in (5.30) and its variation introduces most significant impact to the proposed control strategy. The variation of another circuit parameter, i.e. L_o, is negligible in comparison to that of L_{arm}. As illustrated in Figure 5.23, L_{arm} is set to be different values while 5 mH is used in the control algorithm to calculate $u_o{}^*$ and $u_{diff}{}^*$. The experimental results show that the output current is scarcely affected when L_{arm} varies from 3 mH to 6.3 mH (60% to 126%). On the other hand, i_{diff} is slightly affected by large L_{arm} variations in terms of current ripples suppression. The experimental results suggest that the control system is robust against the parametric uncertainties at steady states and during step changes.

5.7 Summary

In this chapter, a feedback linearization based current control scheme for the MIMO nonlinear MMC system has been presented, in order to improve the control

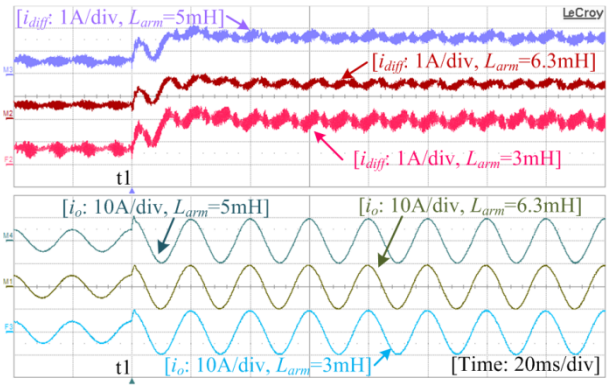


Figure 5.23: Current waveforms during $i_o{}^*$ step change with different arm inductances.

performance while simplifying the control system design process.

The state-function model of the MMC system is firstly presented to show that an MMC is actually an MIMO bilinear system. Therefore, a nonlinear control strategy is a straightforward and effective solution for the control problem of such bilinear system.

The brief principle of input-output feedback linearization technique is presented in Section 5.3. The nonlinear state-function model of the MMC is linearized based on the states feedback and the differential geometry approach in Section 5.4.2. The output and differential currents control loops are linearized and decoupled as two simple integrators. There are two leftover internal dynamics u_{Cu} and u_{Cl} in the linearized system. Therefore, the zero-dynamics stability is discussed and confirmed in Chapter 5.4.3, in order to guarantee the overall system stability while applying the feedback linearization control to the MMC.

Linear controllers, i.e. PR and PI controllers, are designed based on the linearized system to regulate the output and inner differential currents of the MMC system, in Section 5.5. The controller parameters are selected according to classical linear control laws, with the consideration of the control bandwidth and system stability margin. The controller design process for the linearized MMC system is significantly facilitated compared to the design and tuning of multi-resonant controllers or repetitive controllers for effective circulating ripple currents suppression in conventional cascaded control strategies.

The experimental comparisons of the steady-state and dynamic performances between the feedback linearization control and existing cascaded control strategies with equivalent controller parameters are provided in Section 5.6. The results show that the feedback linearization based control offers better tracking accuracy for output current regulation. Although the ripples in the differential current can be well suppressed by both control strategies, the classical PI controller adopted in the feedback linearization control and the PI parameter selection is much simpler than that of the repetitive controller employed in the conventional cascaded control strategy. Unlike resonant and repetitive controllers, the simple PI controller for i_{diff} regulation in the feedback linearization control is not influenced by system frequency deviations. The output and differential currents of the MMC can be independently adjusted since the two current control loops are decoupled. Furthermore, the feedback linearization control features better tracking accuracy, faster dynamic response, and smoother transients for both output and differential currents regulation when there is a reference step change. The robustness with re-

spect to the parameter uncertainty of the feedback linearization control has been experimentally investigated and evaluated.

Chapter 6

Distributed Control for Modular Multilevel Converters

Modularity is one of the most attractive advantages of Modular Multilevel Converters (MMCs). Conventional centralized control architectures, as the ones adopted in Chapter $3-5$, may reduce the flexibility and expandability of an MMC system in terms of firmware implementation. To tackle this issue, this chapter develops a distributed control architecture that is capable of assigning control tasks to distributed local controllers with minimized data exchange through a communication network. The distributed control architecture improves the modularity of an MMC system while achieves all control objectives presented in Chapter 3.

6.1 Introduction

The wide adoption of MMCs in the industry is mainly due to its modularity, flexible expandability, etc. However, most of the MMCs discussed in existing literature are operated with highly centralized control systems for multiple control objectives such as output voltage or current regulation, sub-module capacitor voltage averaging and balancing, and circulating ripple current suppression or injection [71, 73, 87, 184]. Such centralized control systems, whose typical structure is presented in Figure 6.1, limit the modularity and expandability of the overall MMC system in terms of software development. In centralized control structures [85, 145], all the measurements and controls are centralized in a controller (DSP), and the gating signals are generated by FPGA modules. The computational burden is heavy and the execution time might be not sufficient in each

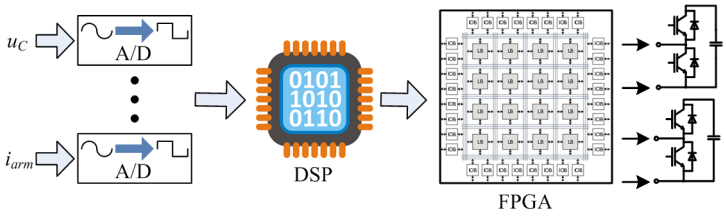


Figure 6.1: Centralized control structure for MMCs.

control cycle if all tasks are centralized into a single digital controller, especially in an MMC with a large number of sub-modules. Therefore, it is beneficial and preferable to investigate distributed control architectures for MMC systems in order to distribute computation burden to different digital controllers and improve the system modularity.

Distributed control structures for MMC systems gradually attract the attention of researchers in recent years. Two different Ethernet-based protocols, distributed PWM generation and voltage balancing control are discussed in [191], where the communication delay, and distributed control loop stability are investigated. A resampled uniform PWM strategy that can be applied in MMC distributed control systems is introduced in [192]. The distributed PWM carrier synchronization technique for local controllers based on EtherCAT distributed clock mechanism is exclusively addressed in [193]. A distributed control method for an MMC based on CAN bus communication is proposed in [194]. However, the proposed control strategy in [194] is only capable for MMCs with a low number of sub-modules. A comprehensive explanation and implementation of a control scheme based on hierarchical control units for different control tasks is reported in [195], which is complex in coordinating different control tasks if a large number of sub-modules are connected in each arm. All of the MMC distributed control architectures discussed in literature so far employ a central controller to process the tasks such as output power control, sub-module capacitor voltage averaging, differential current regulation, and system level protections. Other tasks, e.g. sub-module capacitor voltage measurement, capacitor voltage balancing, PWM generation, and local protections, are distributed into local controllers. Methods similar to the active-control-based capacitor voltage balancing method discussed in Section 3.4.4 are generally adopted in MMC distributed control strategies [191–194, 196]. It should be noted that the sub-module capacitor voltage averaging and balancing are separately implemented in the central and local con-

trollers in existing distributed control strategies. In order to implement the capacitor voltage averaging, the central controller has to be aware of all sub-module capacitor voltages, which requires the voltages measured by local controllers to be sent to the central controller through a communication network. In the case of an MMC system with a considerable number of sub-modules, the communication load is quite high if all the sub-module capacitor voltages are transmitted to the central controller. Therefore, the baud rate of the communication network has to be high enough for fast closed-loop controls. Otherwise, the control bandwidth has to be decreased by increasing the period of control cycle to ensure that all the tasks can be executed within each control cycle [191, 196].

In this chapter, a distributed control architecture for the single-phase MMC system shown in Figure 5.1 is presented in Section 6.2 at first. Such distributed control strategy makes the signals and data transmission required by real-time controls independent of the number of sub-modules in the MMC while all control objectives introduced in Section 3.4 are properly achieved. This control architecture still consists of a central controller and local controllers. Capacitor voltage control loops are completely implemented in local controllers. They are elaborately designed in Section 6.3 so that the individual sub-module capacitor voltage can be properly governed without knowing the capacitor voltages in other sub-modules. Therefore, communication-intensive capacitor voltage transmission in each control cycle is not required and the communication burden of the control system can be significantly reduced. All the control loops are analyzed for controller parameters design. The disturbances introduced by other sub-modules are taken into account while analyzing the stability of the individual average capacitor voltage control loop.

The distributed control strategy is experimentally verified in Section 6.4. The experimental results confirm that the MMC operates properly and stably under the distributed control strategy in the start-up, steady state, and step change operations.

6.2 Distributed control architecture for MMCs

The structure of the distributed control for the MMC is illustrated in Figure 6.2, where the control tasks are assigned to different controllers, i.e. a central controller and local controllers located in sub-modules. The central controller mainly coordinates and manages the overall operation of the MMC, while each

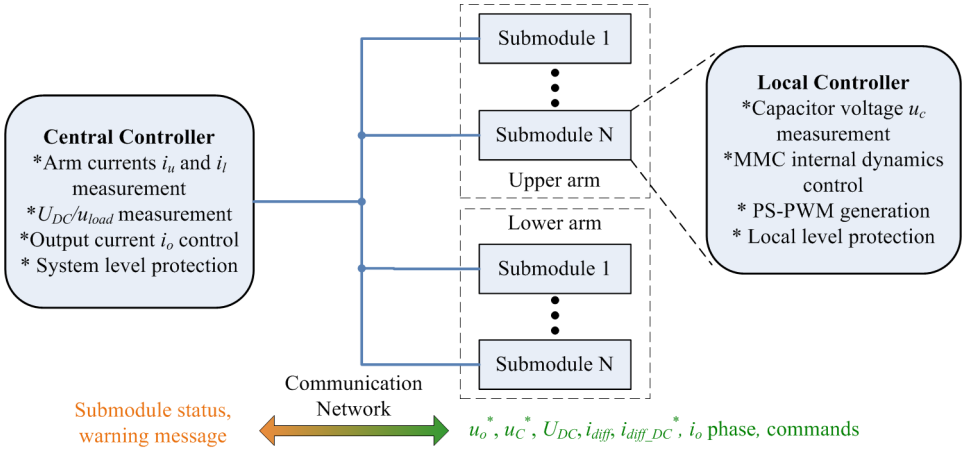


Figure 6.2: Distributed control structure for MMCs.

local controller deals with the internal dynamics and immediate protection of the corresponding sub-module. With the local controllers and distributed control strategy, the MMC sub-modules can be more modularized in terms of software implementation. Significantly reduced information is exchanged between the central and local controllers through the communication network. The complexity of implementing and managing a communication-based distributed control system is reduced, making it convenient to be extended to MMCs with a larger number of sub-modules.

6.2.1 Allocation of control tasks

System level control tasks are assigned to the central controller to coordinate the operation of the MMC at a higher level. The output power and current controls are implemented in the central controller with measured arm currents, DC bus voltage, and load/grid voltage within each control cycle. The capacitor voltage level and the power balance between the DC and AC sides of the MMC are also considered in the central controller. Moreover, system level protections, such as monitoring the sub-module status, are implemented in the central controller as well.

The most significant improvement of the proposed distributed control strategy is that the internal dynamics controls, including capacitor voltage averaging, differential current regulation, and capacitor voltage balancing, are completely distributed into local controllers. They are implemented without knowing the capacitor voltages in other sub-modules that are necessary for conventional con-

trol strategies. Such a distributed control with only local information greatly reduces the communication loads within each control cycle. Each local controller measures the capacitor voltage of the corresponding sub-module at each sampling instance for the distributed voltage control tasks. Sub-module protections, e.g. over-voltage, under-voltage, and fault detection [195], can be implemented in local controllers to protect the sub-modules immediately once abnormal conditions are detected. The gating signals for switching devices in each sub-module are generated by the corresponding local controller.

The comparison of the control tasks allocation and the signals required for real-time controls in the existing and proposed distributed control strategies are visually presented in Figure 6.3, where the sub-modules in the upper and lower arms in the same phase leg are simply labeled as SM_1 to SM_{2N} for convenience. The dashed arrowed lines in Figure 6.3 represent the signals transmitted through the communication network for real-time control. The number of signals for each

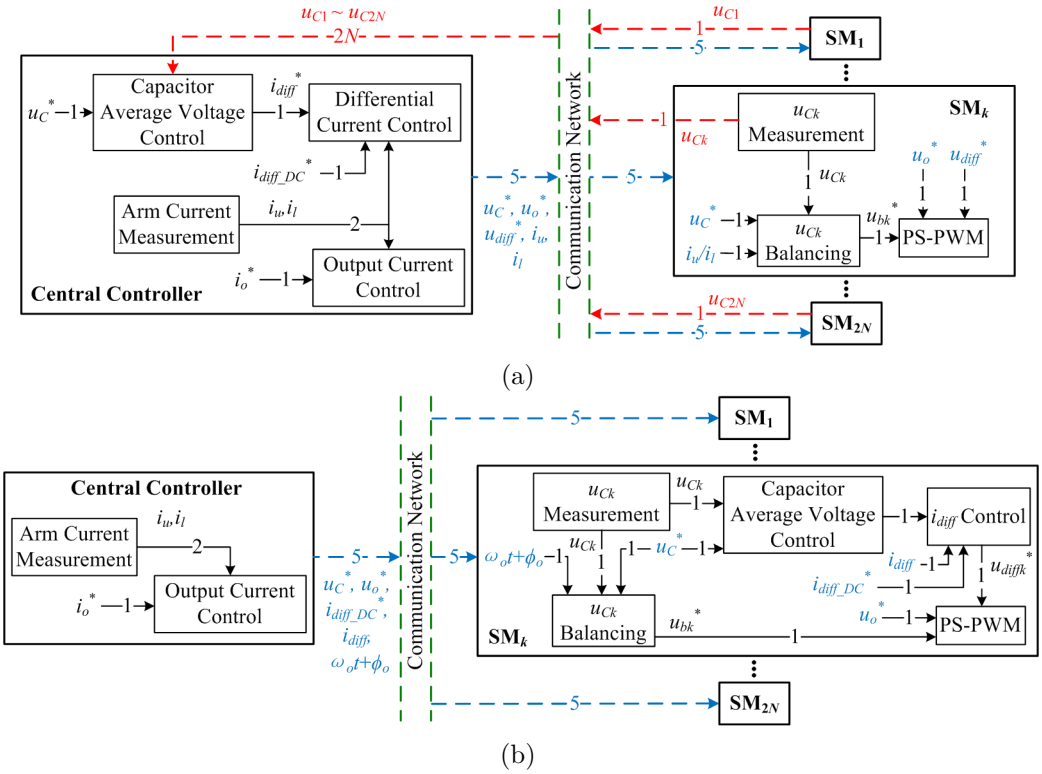


Figure 6.3: Signals required by the MMC real-time controls: (a) Existing distributed control strategy; (b) Proposed distributed control strategy.

arrowed line is directly marked in Figure 6.3. As shown in Figure 6.3 (b), the internal dynamics controls, including capacitor voltage controls and differential current regulation, are completely assigned to local controllers in the proposed strategy. Only two signals are required by the capacitor average voltage control in the local controller in Figure 6.3 (b), while $2N + 1$ signals are needed in existing distributed control strategies. Therefore, the number of signals required by the capacitor average voltage control in the proposed strategy is significantly reduced and no longer depends on the number of sub-modules. The capacitor voltage transmission is not necessary for real-time control, which is beneficial to the control system implementation and the communication network design.

6.2.2 Modulation and synchronization

The phase-shifted PWM (PS-PWM) scheme introduced in Section 3.4.5 is adopted in the distributed control system. A phase-shifted triangular carrier is generated in each local controller. The phase displacements of triangular carriers are calculated based on the number of sub-modules in each arm and assigned to the local controllers when the MMC is initialized after powering up. However, such phase displacements will possibly shift due to the difference of internal oscillators of the local controllers from the manufacturing tolerances, which leads to a distorted output voltage waveform. Therefore, all the local controllers have to be synchronized to the time base of the central controller to generate the desired PS-PWM signals. Since the PWM carrier synchronization is not the main focus of this chapter, a similar method as introduced in [197] can be adopted. A synchronization pulse or command is sent by the central controller every a certain period of time to re-synchronize PWM carriers of local controllers.

6.2.3 Tasks execution sequence and communication

The task execution time sequences of the proposed and existing distributed control strategies are presented in Figure 6.4, where it can be seen that the most significant difference between these two strategies is the capacitor voltage transmission through the communication network. In existing distributed control, the communication bus and the execution time of the central controller would be mostly occupied by the capacitor voltage updating, especially when a large number of sub-modules are employed in the MMC system. In other words, the communication burden is approximately proportional to the number of sub-modules.

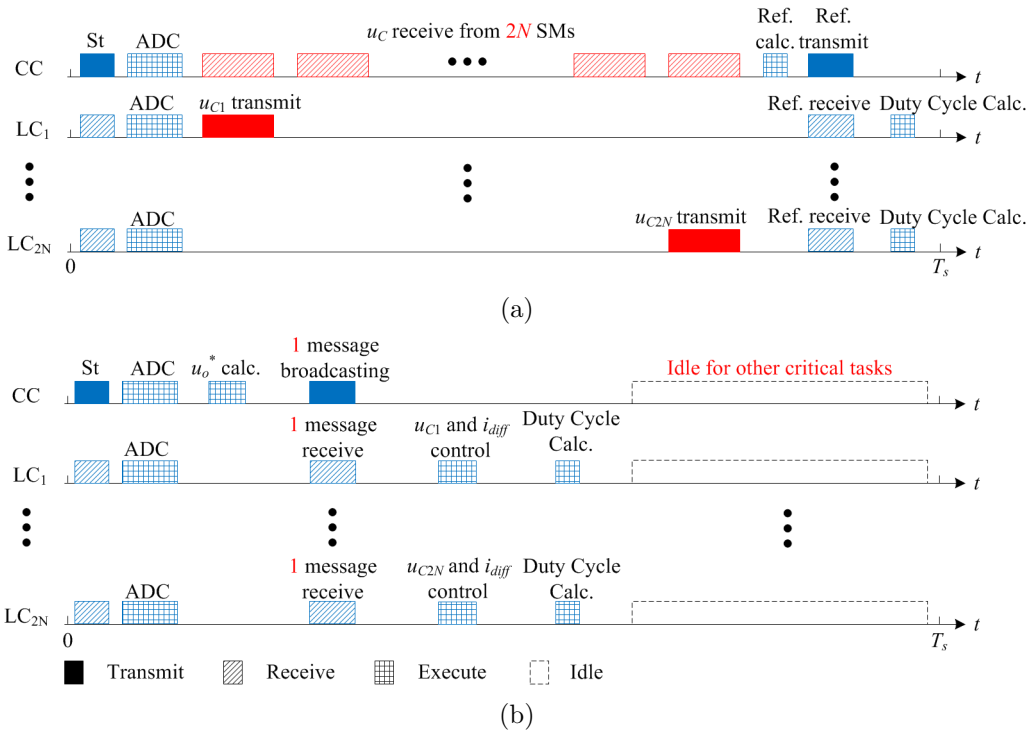


Figure 6.4: Time sequence of tasks in each control cycle of: (a) Existing distributed control; (b) Proposed distributed control.

Consequently, a trade-off between control bandwidth (switching and sampling frequency) and communication baud rate is required due to the large communication load and the delay caused by the communication.

On the other hand, there is no capacitor voltages transmission required in each control cycle for the proposed distributed control strategy, and the execution burden is independent of the number of sub-modules in the MMC. The communication network as well as the controllers are in the idle state in most of the time in each control cycle. They can be used for other tasks such as system status monitoring and protection. At the beginning of each control cycle, a start message (St) is sent by the central controller (CC) to synchronize and trigger the analog-to-digital conversion (ADC) of local controllers (LCs). After the measurements, the central controller calculates the references and sends the information required to local controllers. With received data, the local controllers perform the MMC internal dynamics controls and generate the gating signals for switching devices based on calculated modulation index and PS-PWM scheme.

The communication protocol is selected mainly based on the data rate of the

communication network and the number of messages transmitted per second. In the MMC prototype with a short transmission distance, the Controller Area Network (CAN) protocol having a 1 Mbps data rate with a maximum bus length of 40 meters can be adopted to transmit messages for executing the proposed distributed control in real time. In those cases where more information, higher transmission rate, or longer transmission distance is required, the high-speed Controller Area Network with Flexible Data-Rate (CAN FD) protocol (2 Mbps data rate) or even the Ethernet for Control Automation Technology (EtherCAT) protocol (100 Mbps data rate) can be used in the communication network.

The communication messages are designed accordingly to execute the tasks shown in Figure 6.4 (b) with minimum information exchanging for real-time control with relatively high bandwidth. The output voltage reference $u_o{}^*$, the capacitor voltage reference $u_C{}^*$, differential current reference for power balance $i_{diff,DC}{}^*$, differential current i_{diff}, and output current phase angle ϕ_{i_o} are required in each control cycle and shared by all local controllers in the same phase leg. One message containing those data, which conveys adequate information for the real-time control in local controllers, can be broadcasted by the central controller through the communication network in each control cycle. Besides the message required in each control cycle, some other messages are designed for the overall operation of the MMC. The structure of the message frames are illustrated in Figure 6.5. The controller identifier (ID) field is used to determine the receivers of the message, e.g. all local controllers (broadcasting), controllers in one arm, or a specific local controller. Each sub-module is assigned a sole ID so that it can communicate with the central controller individually as well. The command (CMD) field is designed for local controllers to know the following action according to the request from the central controller, such as synchronization or sub-module status monitoring.

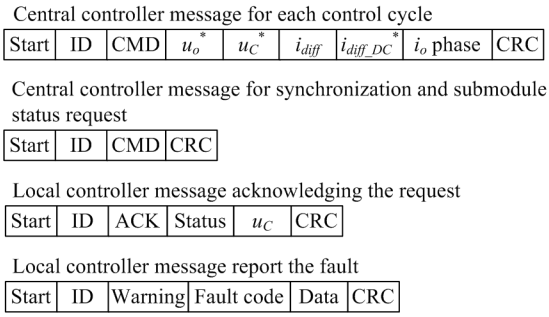


Figure 6.5: Distributed control structure for MMCs.

The synchronization message is broadcasted by the central controller every NT_s seconds, where T_s is the sampling interval. After receiving the synchronization message, local controllers reset their carrier phase angles to the initial values. Each sub-module updates its status and capacitor voltage by request for system monitoring and status display purposes.

If there is any abnormal sub-module status detected by the corresponding local controller, the necessary protection actions can be executed locally, and a warning message with the fault code is immediately sent out to inform the central controller for further decision making. Moreover, if any of the local controllers cannot receive any message from the central controller for a few sampling intervals, the sub-module will cease its operation, being bypassed from the MMC. In contrast, if the central controller cannot receive the acknowledgement for status checking from any local controller for a certain period of time due to the communication failure or the sub-module failure, the central controller will shut down the whole MMC system.

6.3 Distributed control system design and analysis

Assuming the circulating harmonics in the differential current (2.8) have been completely suppressed by the even-harmonic repetitive controller introduced in Chapter 4, the arm currents of the single-phase MMC shown in Figure 5.1 can be written as

$$\begin{cases} i_u = I_{DC} + \dfrac{i_o}{2} \\ i_l = I_{DC} - \dfrac{i_o}{2} \end{cases} \tag{6.1}$$

Without considering the capacitor voltage unbalance and any additional capacitor voltage control, the normalized modulation index of the k^{th} sub-module in the upper and lower arms can be obtained as

$$\begin{cases} n_{uk} = \dfrac{1}{2} - \dfrac{{u_o}^*}{2} - {u_{diff}}^* \\ n_{lk} = \dfrac{1}{2} + \dfrac{{u_o}^*}{2} - {u_{diff}}^* \end{cases} \tag{6.2}$$

and

$$\begin{cases} {u_o}^* = \dfrac{2u_o}{U_{DC}} \\ {u_{diff}}^* = \dfrac{U_{diff,DC} + U_{diff2}\cos(2\omega_o t + \phi_{diff2})}{U_{DC}} \end{cases} \tag{6.3}$$

where $U_{diff,DC}$ is a DC voltage to induce I_{DC}, and $U_{diff2}\cos(2\omega_o t + \phi_{diff2})$ is the voltage utilized to suppress the second-order harmonics in the differential current [136]. According to the analysis in Subsection 3.2.3 , the capacitor voltage of the k^{th} sub-module in the upper and lower arms can be simplified according to (3.14) to (3.17) as

$$\begin{cases} u_{Cuk} = U_C + U_{C1}\sin(\omega_o t + \phi_{C1}) - U_{C2}\sin(2\omega_o t + \phi_{i_o}) \\ u_{Clk} = U_C - U_{C1}\sin(\omega_o t + \phi_{C1}) - U_{C2}\sin(2\omega_o t + \phi_{i_o}) \end{cases} \tag{6.4}$$

where U_C denotes the average voltage across the sub-module capacitor, $U_{C1}\sin(\omega_o t + \phi_{C1})$ and $U_{C2}\sin(2\omega_o t + \phi_{i_o})$ represent the voltage ripples with fundamental and second-order frequencies respectively.

6.3.1 Phase-shifted PWM implementation and control system delay analysis

The PS-PWM scheme for the MMC is implemented in local controllers, whose principle is illustrated in Figure 6.6. Three triangular carriers c_1, c_2 and c_3 are respectively generated in the three local controllers in the same arm. The phase angles of the carriers are shifted by $2\pi/3$ radian from each other. The carriers in the upper and lower arms have the same phase angles to generate $2N+1$ output voltage levels when N is an odd number according to Table 3.1. All the sampling instances are synchronized based on the message sent from the central controller in every control cycle. The duty cycle of each sub-module is updated at the instances that the corresponding carrier reaches the period and zero. Note that the output and differential currents can be adjusted by switching action of any sub-module in the same phase leg. So that the equivalent switching frequency

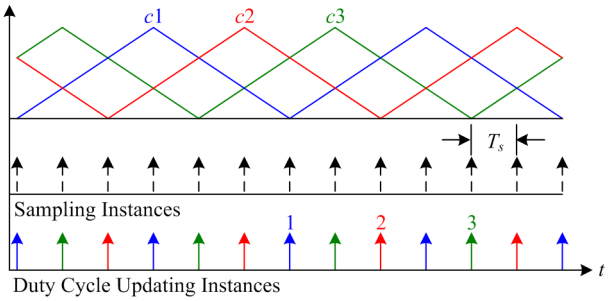


Figure 6.6: Phase-shifted PWM scheme for the distributed control.

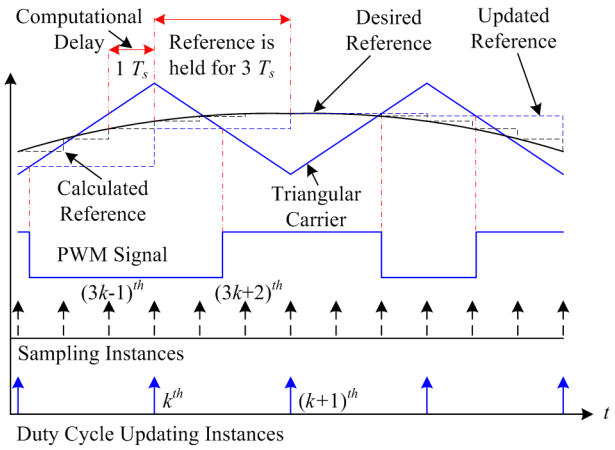


Figure 6.7: Illustration of the digital control delay in voltage control loops.

of the current control loops is correspondingly $f_s = 2Nf_c$. Equivalently, the current measurements are executed at each sampling instance and the calculated duty cycles based on these measurements for current regulation are updated at the next sampling instance, which introduces T_s seconds computational delay. A $0.5T_s$ PWM delay also exists in the current control loops [170]. Therefore, a $1.5T_s$ digital control delay exists in current control loops.

In contrast, the digital control delay in the capacitor voltage control loops is different from that of the current control loops, since the capacitor voltage is adjusted by the local controller and switching devices in individual sub-module. Taking sub-module 1 as an example, the time sequence for the voltage control is illustrated in Figure 6.7. The capacitor voltage is sampled at the $(3k-1)^{th}$ sampling instance and the corresponding reference is calculated in this sampling interval. At the next sampling instance (the k^{th} duty cycle updating instance of sub-module 1 as well), the reference calculated in the last sampling interval is used to update the duty cycle of sub-module 1. The updated duty cycle will be held for the next three sampling intervals ($3T_s$) and an average $1.5T_s$ PWM delay is consequently introduced due to the equivalent ZOH with a sampling period of $3T_s$. Thus, a total $2.5T_s$ digital control delay has to be taken into account while designing the capacitor voltage control loop.

6.3.2 Control loops in the central controller

As illustrated in Figure 6.8, the output current control of the MMC is implemented in the central controller with the given reference $i_o{}^*$. The measured u_{load} and i_o are

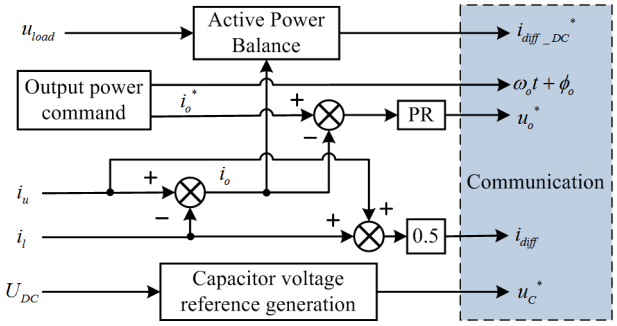


Figure 6.8: Block diagram of the central controller.

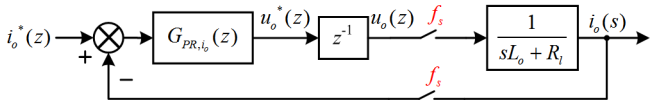


Figure 6.9: Block diagrams of the output current control loop.

used to calculate $i_{diff,DC}{}^*$ for the power balance between the DC and AC sides of the MMC. The reference of the sub-module capacitor voltage $u_C{}^*$ can be obtained according to the DC bus voltage and the operation requirements of the MMC, e.g. in normal operation $u_C{}^* = U_{DC}/N$, during the start-up process, or the average capacitor voltage is intentionally varied in the application discussed in [52]. Since a single-phase MMC system is considered in this chapter, a proportional-resonant (PR) controller is adopted to regulate the output current according to the power demands. The z-domain transfer function of the PR controller is expressed as

$$G_{PR,i_o}(z) = K_{P,i_o} + \frac{2K_{R,i_o}\omega_{cf}T_s\,(z-1)}{z^2 + z\left(\omega_o{}^2T_s{}^2 + 2\omega_o T_s - 2\right) - 2\omega_{cf}T_s + 1} \tag{6.5}$$

where K_{P,i_o} and K_{R,i_o} are the proportional and resonant gains respectively, and ω_{cf} is the resonant cut-off frequency. The output current control loop can be depicted in Figure 6.9, where the sampling frequencies of all samplers are set to be f_s. The open-loop transfer functions of the output current control loop can be derived according to the block diagram in Figure 6.9, as

$$G_{i_o,op}(z) = G_{PR,i_o}(z)z^{-1}Z_{ZOH}(\frac{1}{sL_o + R_l}) \tag{6.6}$$

The outputs of the central controller are passed to local controllers through the communication network.

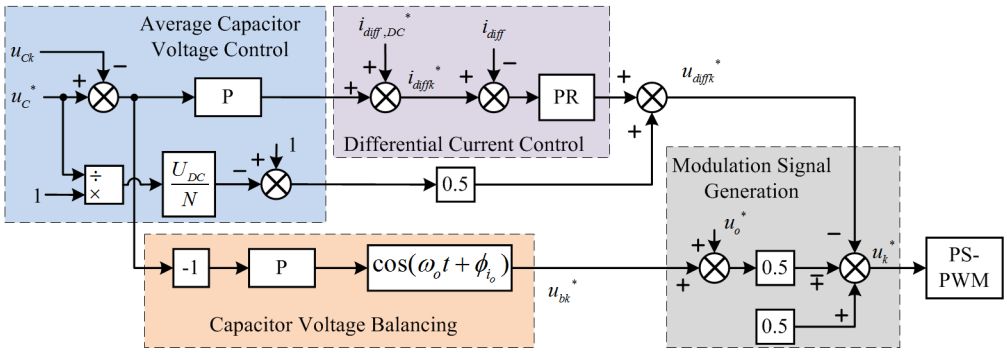


Figure 6.10: Block diagram of the local controller.

6.3.3 Control loops distributed in local controllers

The internal dynamics of the MMC, i.e. the differential current and capacitor voltage are locally controlled in individual sub-module to implement the distributed control strategy in a more modularized manner. The block diagram of the control loops in the k^{th} local controller is shown in Figure 6.10.

Differential current control loop

As shown in Figure 6.10, the reference of the inner differential current $i_{diffk}{}^*$ is mainly obtained from the capacitor voltage control and the active power balancing. The DC side current reference for power balancing is set to be $i_{diff,DC}{}^* = U_o I_o \cos(\phi_{i_o})/(2U_{DC})$. The output of the voltage control loop, which is, ideally, a DC component as well, is regarded as the other part of the differential current reference. A PR controller coping with the signal at the second-order frequency is employed to regulate the circulating ripple current i_{cir} according to its reference. The differential current control loop is presented in Figure 6.11 and the corresponding open-loop transfer function is derived as

$$G_{i_{diff},op}(z) = G_{PR,i_{diff}}(z) z^{-1} Z_{ZOH} \left(\frac{1}{sL_{arm} + R_{arm}} \right) \tag{6.7}$$

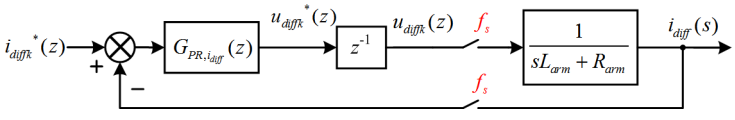


Figure 6.11: Block diagrams of the differential current control loop.

where the s-domain plant is converted to a z-domain transfer function through the ZOH method (Z_{ZOH}).

Sub-module capacitor voltage control

The control of sub-module capacitor voltage of the MMC is an important and unavoidable task that attracts a lot of research interests. As introduced in Subsection 6.2.1, the task of capacitor voltage governing is completely distributed to local controllers with limited information, while the control objectives can still be achieved. Different voltage control loops have to be particularly designed for sub-module capacitor voltage averaging and balancing. Taking the k^{th} sub-module in the upper arm as an example, the power that flows through the capacitor can be calculated according to (5.32), (6.1) - (6.4), as

$$P_{Cuk} = u_{Cuk} n_{uk} i_u = \bar{P}_{Cuk} + \text{AC terms} \tag{6.8}$$

Note that only the average power (DC components) in P_{Cuk} contributes to the capacitor voltage shifting, such average power can be used to adjust the average voltage across sub-module capacitors. The average power of the sub-module capacitor can be obtained as

$$\begin{aligned}\bar{P}_{Cuk} = &\left[U_C\left(\frac{1}{2} - \frac{U_{diff,DC}}{U_{DC}}\right) - \frac{U_o U_{C1}\sin(\phi_{C1})}{2U_{DC}}\right.\\ &\left.+\frac{U_{C2}U_{diff2}}{2U_{DC}}\sin(\phi_{i_o} - \phi_{diff2})\right] I_{DC}\\ &-\left[\frac{U_o U_C \cos(\phi_{i_o})}{U_{DC}} - \left(\frac{1}{2} - \frac{U_{diff,DC}}{U_{DC}}\right) U_{C1}\sin(\phi_{C1} - \phi_{i_o})\right.\\ &\left.+\frac{U_{C1}U_{diff2}\sin(\phi_{C1} + \phi_{i_o} - \phi_{diff2})}{2U_{DC}}\right]\frac{I_o}{4}\end{aligned} \tag{6.9}$$

Average capacitor voltage control loop: The capacitor voltage averaging aims to control the capacitor average voltage in each sub-module according to the capacitor voltage reference $u_C{}^*$. In conventional capacitor voltage averaging strategies [82, 85, 145, 184], the average voltage in one phase leg is controlled with the help of a DC component in the differential current induced by $U_{diff,DC}$ with the awareness of the capacitor voltages in all sub-modules. In the proposed structure, the capacitor voltage might be easily unstable by simply distributing the PI controller used in conventional voltage controls into local controllers, due to the

control conflict among different sub-modules in one phase leg. Therefore, a new voltage control method is designed to maintain the mean value of the capacitor voltage in each sub-module.

As analyzed in [57], the average capacitor voltage is usually selected as $u_C = U_{DC}/N$ in most applications, by simultaneously inserting N sub-modules into one phase leg, for the sake of the capability to generate the maximum output voltage. In fact, such average capacitor voltage in one phase leg can be, ideally, regulated as U_{DC}/N_{eq} by changing the equivalent number of sub-modules inserted into the phase leg N_{eq}. The average voltage control loop is illustrated in Figure 6.10, where the equilibrium average capacitor voltage is U_{DC}/N and a feed-forward path is designed to implement the average voltage control by adjusting N_{eq}. The proposed feed-forward path can be expressed as

$$G_{feedfwd} = \frac{1}{2}(1 - \frac{U_{DC}}{N{u_C}^*}) \tag{6.10}$$

where the coefficient 1/2 is adopted because the equivalent numbers of sub-modules inserted into the phase leg in the upper and lower arms are equally adjusted. According to (6.2) and (6.10), the effectiveness of the proposed feed-forward path in the average capacitor voltage regulation according to ${u_C}^*$ can be verified based on the differential equation of the average capacitor voltage as

$$\frac{dU_C}{dt} = \frac{U_{DC}}{2C_{SM}R_{arm}}\left[1 - \frac{U_C}{{u_C}^*}\right] \tag{6.11}$$

The direction of arrows in Figure 6.12 indicates that the average capacitor voltage will converge to different set points according to its references. In addition,

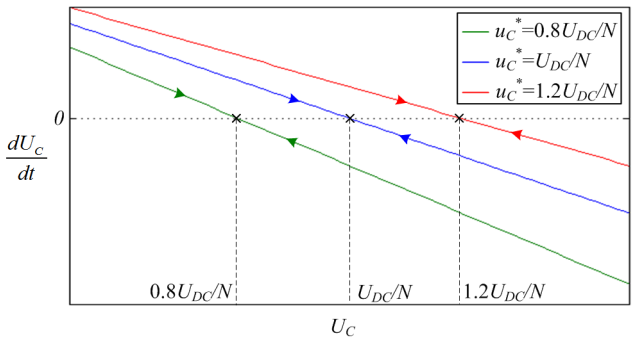


Figure 6.12: Phase trajectory of the average capacitor voltage.

a proportional (P) controller is employed to fine-tune the average capacitor voltage in each individual sub-module. This P controller is used to compensate the control errors introduced by dead-time, parameter difference among sub-modules, and system uncertainties, etc. It is disabled whenever $i_o{}^*$ is zero, and the capacitor average voltage is then only regulated by the feed-forward path in this case.

The average capacitor voltage control block diagram for the k^{th} sub-module, which can be derived according to Figure 6.10, is shown in Figure 6.13 (a). The sampling frequency for voltage and current quantities measurements is f_s, while the sampling frequency of the sampler representing the PWM action is f_c. Note that the references $i_{diffk}{}^*$ and $u_{diffk}{}^*$ of the k^{th} sub-module are different from the ones in other sub-modules because of the individual average capacitor voltage control. The MAF(z) term stands for a moving average filter with a 0.02-second time window, whose z-domain transfer function can be denoted as

$$\text{MAF}(z) = \frac{1 + z^{-1} + \cdots + z^{1-0.02/T_s}}{0.02/T_s} \tag{6.12}$$

Since $u_C{}^*$ and $i_{diff,DC}{}^*$ are generally set to be constant in the steady state operation, the feed-forward path for the average voltage control, as well as the $i_{diff,DC}{}^*$ term, are ignored while designing the proportional controller gain $K_{P,u_{C,ave}}$, as shown in Figure 6.13 (b). $G_{i_{diff},cl}(z)$ refers to the closed-loop transfer function

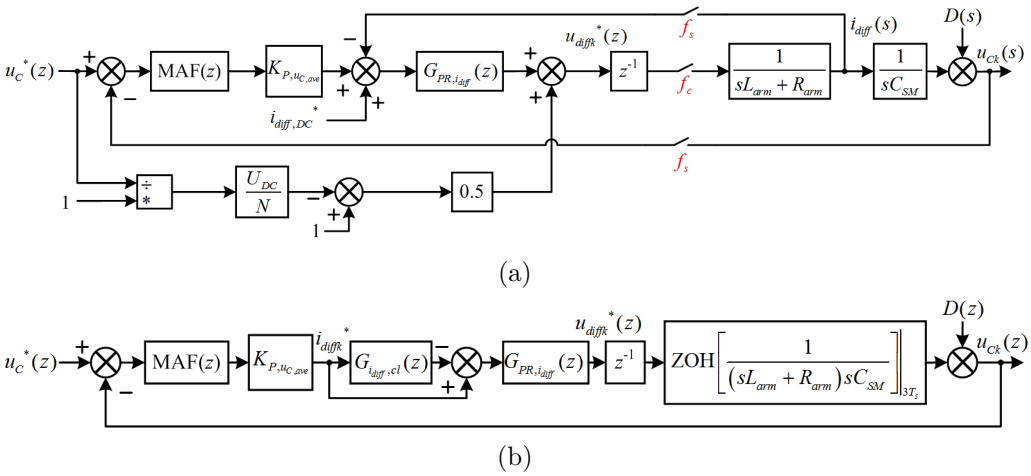


Figure 6.13: Block diagrams for the average voltage control: (a) Actual block diagram; (b) Simplified block diagram in z-domain.

for differential current regulation, which can be written as

$$G_{i_{diff},cl}(z) = \frac{G_{i_{diff},op}(z)}{1 + G_{i_{diff},op}(z)} \tag{6.13}$$

The plant of the average capacitor voltage control loop is discretized by a zero-order-holder (ZOH) with a sampling interval of $3T_s$. As aforementioned, such ZOH will introduce a $1.5T_s$ seconds delay into the voltage control loop.

The open-loop transfer function derived from Figure 6.13 (b) is expressed as

$$\begin{aligned} G_{u_{C,ave},op}(z) =& \text{MAF}(z) K_{P,u_{C,ave}} \left(1 - G_{i_{diff},cl}(z)\right) z^{-1} \\ & \times \text{ZOH} \left[\frac{1}{\left(sL_{arm} + R_{arm}\right) sC_{SM}} \right] \Bigg|_{3T_s} \end{aligned} \tag{6.14}$$

It should be noted that there might be control conflicts among sub-modules, e.g., one sub-module requires higher differential current to increase its capacitor voltage while another sub-module is trying to reduce the current to decrease its own capacitor voltage. Such control conflicts from other sub-modules are modeled as voltage disturbances $D(s)$ to the capacitor voltage of sub-module k, as shown in Figure 6.13 (a). Such control conflict among different sub-modules in the same phase leg has to be taken into account to ensure the overall system stability. The disturbances introduced by control loops in other sub-modules to the capacitor voltage of the k^{th} sub-module can be derived as

$$D_k(z) = \frac{\sum_{i \neq k}^{2N} (u_C{}^* - u_{Ci}) K_{P,u_{C,ave}} K_{P,i_{diff}}}{2N^2} \leq \frac{(N-1) K_{P,u_{C,ave}} K_{P,i_{diff}} \max(|e_{u_{Ci}}|)}{2N^2} \tag{6.15}$$

where $e_{u_{Ci}}$ is the error of the capacitor voltage in the i^{th} sub-module. The closed-loop transfer function from $D_k(z)$ to u_{Ck} can be derived as

$$\frac{u_{Ck}}{D_k(z)} = \frac{1}{1 + G_{u_{C,ave},op}(z)} \tag{6.16}$$

Substituting (6.15) into (6.16)

$$\frac{u_{Ck}}{\max(|e_{u_{Ci}}|)} \leq \frac{(N-1) K_{P,u_{C,ave}} K_{P,i_{diff}}}{2N^2 \left[1 + G_{u_{C,ave},op}(z)\right]} \tag{6.17}$$

The influence of the capacitor average voltage tracking error in other sub-

modules $e_{u_{Ci}}$ to the capacitor voltage in the k^{th} sub-module u_{Ck} can be obtained according to (6.17). The controller gain $K_{P,u_{C,ave}}$ can be accordingly selected with the help of (6.14) and (6.17).

Capacitor voltage balancing: The capacitor average voltage control introduced in the previous subsection cannot guarantee balanced capacitor voltages during the operation of the MMC. Since the DC side current I_{DC} will affect all sub-module capacitor voltages in the phase leg, the AC side active power is utilized to control the individual sub-module capacitor voltage. An AC component with fundamental frequency is intentionally added to the modulation signal of each individual sub-module to generate a controllable active power. The modulation signals are modified as

$$\begin{cases} n_{uk} = \dfrac{1}{2} - \dfrac{u_o^* + {u_{buk}}^*}{2} - u^*_{diffuk} \\ n_{lk} = \dfrac{1}{2} + \dfrac{u_o^* + {u_{blk}}^*}{2} - u^*_{difflk} \end{cases} \tag{6.18}$$

where ${u_{buk}}^*$ and ${u_{blk}}^*$ are the capacitor voltage balancing signals for the k^{th} sub-module in the upper and lower arms respectively. Taking the upper arm as an example, ${u_{buk}}^*$ can be expressed as

$${u_{buk}}^* = {U_{buk}}^* \cos(\omega_o t + \phi_b) \tag{6.19}$$

The average power of the k^{th} sub-module capacitor in the upper arm is

$$\begin{aligned} \bar{P}_{Cuk} = & \left[U_C \left(\frac{1}{2} - \frac{U_{diff,DC}}{U_{DC}} \right) - \frac{U_o U_{C1} \sin(\phi_{C1})}{2U_{DC}} \right. \\ & \left. + \frac{U_{C2} U_{diff2}}{2U_{DC}} \sin(\phi_{i_o} - \phi_{diff2}) \right] I_{DC} \\ & - \left[\frac{U_o U_C \cos(\phi_{i_o})}{U_{DC}} - \left(\frac{1}{2} - \frac{U_{diff,DC}}{U_{DC}} \right) U_{C1} \sin(\phi_{C1} - \phi_{i_o}) \right. \\ & \left. + \frac{U_{C1} U_{diff2} \sin(\phi_{C1} + \phi_{i_o} - \phi_{diff2})}{2U_{DC}} \right] \frac{I_o}{4} \\ & - \left[\frac{U_C I_o \cos(\phi_{i_o} - \phi_b)}{8} + \frac{I_{DC} U_{C1} \sin(\phi_{C1} - \phi_b)}{4} + \frac{I_o U_{C2} \sin(\phi_b)}{16} \right] {U_{buk}}^* \end{aligned} \tag{6.20}$$

where the last three terms on the right-hand side are introduced by the capacitor voltage balancing. Among them, $U_C I_o {U_{buk}}^* \cos(\phi_{i_o} - \phi_b)/8$ is obviously the

most dominant term since the average voltage across the sub-module capacitor is normally much larger compared to the amplitudes of voltage ripples. Therefore, the capacitor voltage balancing loop is most effective if $\phi_b = \phi_{i_o}$ is selected. As illustrated in Figure 6.10, the amplitude of $U_{buk}{}^*$ is generated by a P controller according to the capacitor voltage tracking error. The output of the P controller is multiplied by $\cos(\omega_o t + \phi_{i_o})$ to generate $u_{buk}{}^*$ having the same phase angle as the output current. $u_{buk}{}^* = 0$ if the output current is set to be zero, which is reasonable as the sub-module capacitor voltages are generally stable if there is no power drawn from the MMC by the loads.

Ignoring the voltage ripples across the sub-module capacitor, the block diagram of the k^{th} capacitor voltage balancing loop can be found in Figure 6.14, where the signs of terms containing $\cos(\omega_o t + \phi_{i_o})$ are '$-$' for sub-modules in the upper arm and '$+$' for sub-modules in the lower arm. According to the previous analysis, only the DC components in the capacitor current i_C contribute to the shifting of the capacitor voltage, while the AC terms in i_C introduce voltage ripples across the capacitor. Consequently, the block diagram of the capacitor voltage balancing loop can be simplified as in Figure 6.15, where I_{Ck} and U_{Ck} stand for the DC components of the capacitor current and voltage respectively.

It should be noted that the gain of the capacitor voltage balancing loop is proportional to the amplitude of the output current I_o, and higher I_o leads to less phase margin for the system stability with the same $K_{P,u_{C,bal}}$. Therefore, it is advisable to design the controller gain under the condition that the MMC is operated with its designed maximum output current, i.e. $I_{o,max}$.

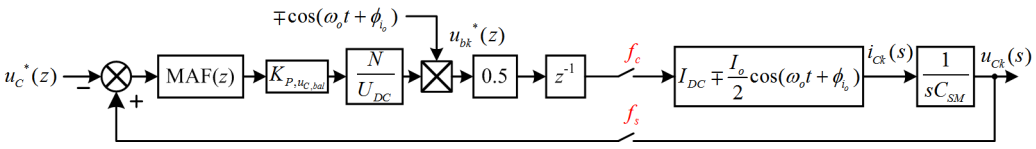


Figure 6.14: Block diagram of capacitor voltage balancing loop.

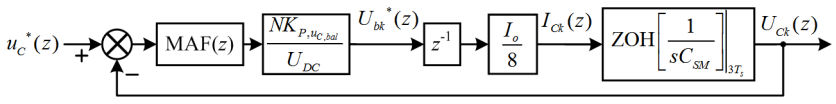
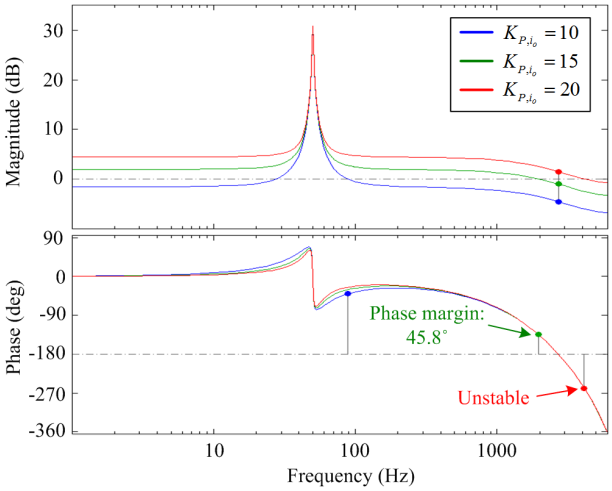


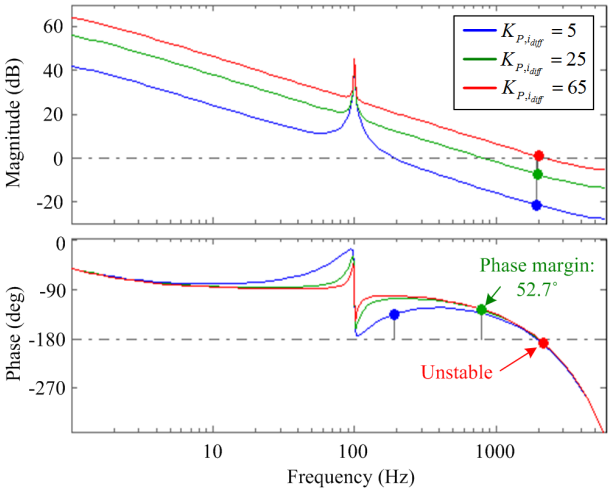
Figure 6.15: Simplified block diagram of capacitor voltage balancing loop.

6.4 Case study and experimental results

The distributed control strategy is implemented on the prototype shown in Figure 4.18, whose parameters are listed in Table 5.1. The equivalent switching frequency of the MMC is $6f_c = 12$ kHz. The sampling frequency of the control system is designed to be $f_s = 12$ kHz and the control cycle period is $T_s = 1/f_s$. As discussed in Subsection 6.3.1, there is a $1.5T_s$ delay and a $2.5T_s$ delay in the current and voltage control loops respectively. Such digital control system delays are taken into



(a)



(b)

Figure 6.16: Bode diagrams of: (a) Output current control loop with different K_{P,i_o}; (b) Differential current control loop with different $K_{P,i_{diff}}$.

account while designing the controllers. The controller parameters are selected according to the control loop analysis in Subsection 6.3.3.

6.4.1 Controller parameters selection

The Bode diagrams of the open-loop transfer function of the output current control loop ($G_{i_o,op}(z)$) in (6.6) is shown in Figure 6.16 (a), which indicate that $K_{P,i_o} = 15$ provides relatively high open-loop controller gain with a phase margin of 45.8°, which guarantees the fast response and the stability of the output current control loop. The resonant gain K_{R,i_o} is set to be 400 to obtain a high magnitude peak at the fundamental frequency 50 Hz, providing satisfactory output current

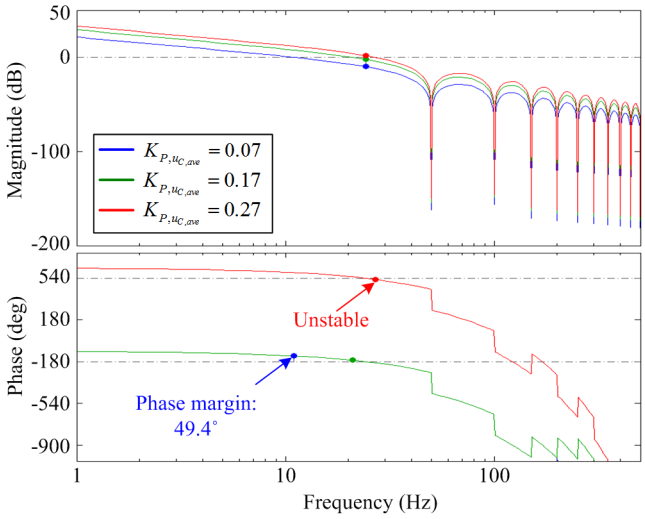


Figure 6.17: Bode diagram of $G_{u_{C,ave},op}(z)$.

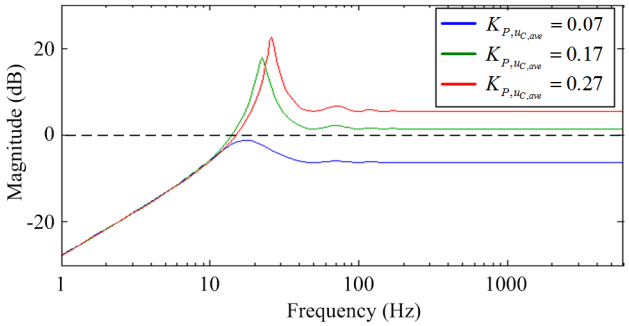


Figure 6.18: Magnitude-frequency characteristics of the right-hand side of inequality (6.17).

regulation. Similarly, based on the Bode diagrams in Figure 6.16 (b), the proportional gain of $G_{i_{diff},op}(z)$ derived in (6.7) can be selected as $K_{P,i_{diff}} = 25$ with the consideration of excellent current regulation and system stability (phase margin 52.7°). The resonant gain is set to be 500 to compensate the second-order harmonics at 100 Hz.

The selection of the proportional gain for the capacitor average control loop has to take both the closed-loop stability and the disturbances from other submodules into consideration. On the one hand, the Bode diagram of the open-loop transfer function of the capacitor average voltage control loop $G_{u_{C,ave},op}(z)$ defined in (6.14) is depicted in Figure 6.17. The proportional gain of the average voltage control loop is selected as $K_{P,u_{C,ave}} = 0.07$ for a phase margin of 49.4°. On the other hand, the bode diagram of the right-hand of inequality (6.17) depicted in Figure 6.18 shows that the disturbances can be well damped if $K_{P,u_{C,ave}} = 0.07$ is selected, since the magnitude characteristics of the right-hand side of (6.17) are always below 0 dB at all frequencies.

According to the control loop design for the capacitor voltage balancing in Subsection 6.3.3, $I_{o,max} = 12$ A is adopted for the controller gain selection. Based on the Bode diagram shown in Figure 6.19, $K_{P,u_{C,bal}} = 4$ is accordingly selected for sufficient phase margin in the entire operation range of the MMC.

The controller parameters for the MMC system under the distributed control

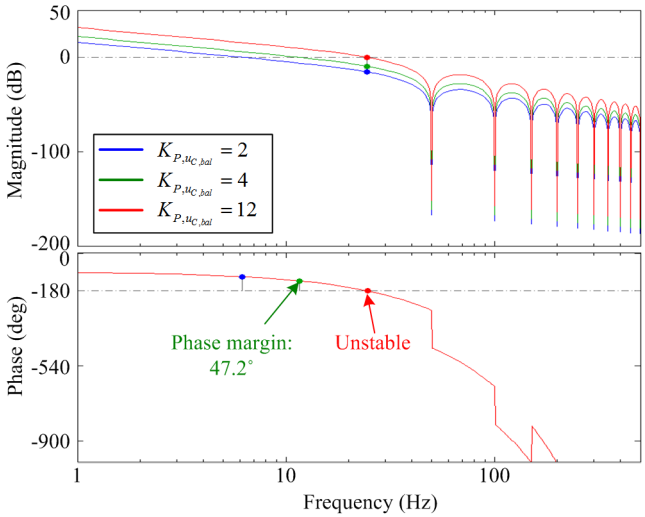


Figure 6.19: Bode diagram of the open-loop transfer function of the capacitor voltage balancing loop.

Table 6.1: Controller parameters

Current Controllers	
Proportional Gain for i_o: K_{P,i_o}	15
Resonant Gain for i_o: K_{r,i_o}	400
Proportional Gain for i_{diff}: $K_{P,i_{diff}}$	25
Resonant Gain for i_{diff}(100Hz): $K_{r,i_{diff}}$	500
Voltage Controllers	
Proportional Gain for voltage averaging: $K_{P,u_{C,ave}}$	0.07
Proportional Gain for voltage balancing: $K_{P,u_{C,bal}}$	4

architecture are listed in Table 6.1.

6.4.2 MMC start-up process and voltage regulation with zero output current

The start-up process of the MMC has been demonstrated in following experiments to verify the effectiveness of the capacitor voltage regulation.

The sub-module capacitor voltage should be automatically charged to, ideally, $U_{DC}/2N$ through the body diode of switching devices if the MMC is connected to the DC bus without any switching action. The sub-module capacitor voltages in the start-up process are depicted in Figure 6.20. After activating the switching devices, the capacitor voltage is initially set to be 50 V and then ramp up to 80 V (U_{DC}/N) with a rate of 40 V/s until t1, which represents the end of the start-up process. It can be seen in the voltage curves in Figure 6.20 that the capacitor voltage is unavoidably unbalanced due to the parameters spread among sub-module capacitors if no voltage balancing control is applied. After the start-up

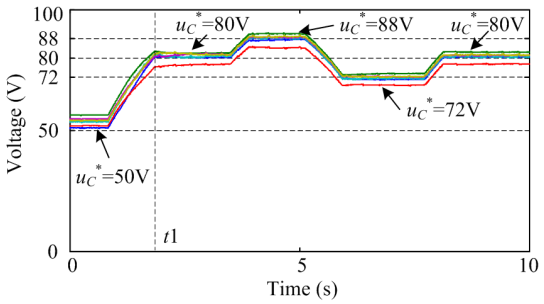


Figure 6.20: Sub-module capacitor voltages during the MMC start-up process with zero output current.

process, the capacitor voltage reference is intentionally set to be 88 V ($1.1U_{DC}/N$) and 72 V ($0.9U_{DC}/N$) respectively to demonstrate that the average capacitor voltage can be regulated according to its references.

6.4.3 Steady-state performance

The steady-state performance of the MMC using the distributed control strategy has been investigated in this set of experiments. Figure 6.21 shows the voltage and current waveforms of the MMC in steady-state operation, where the amplitude of the output current is set to be 9 A. A seven-level output voltage is generated and the output current tracks its reference accurately. The second-order harmonic in i_{diff} is effectively suppressed with the help of the resonant controller, leaving a DC component in the differential current with negligible ripples. Moreover, the sub-module capacitor voltages are well balanced with the proposed voltage control strategy. The overall system works stably under the distributed control in steady-state.

Figure 6.22 presents the voltage and current waveforms of the MMC at different capacitor voltage levels. The amplitude of the output current is set to be 6 A in this set of experiments so that sufficient output voltage can still be provided by the MMC when the average capacitor is set to be 64 V ($0.8U_{DC}/N$). It shows that

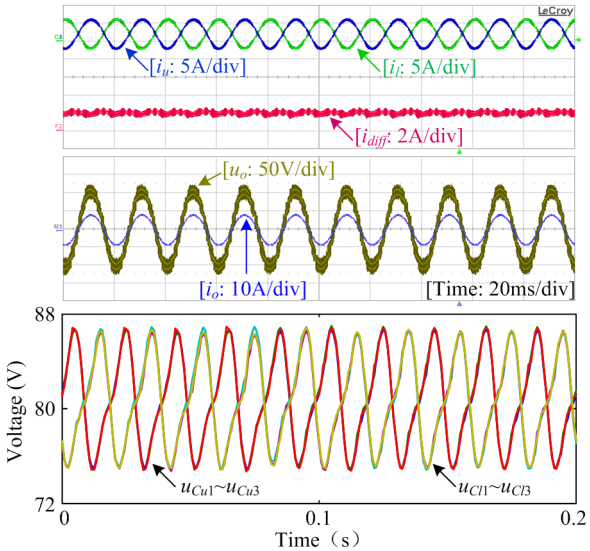


Figure 6.21: Voltage and current waveforms of the MMC during the steady-state operation.

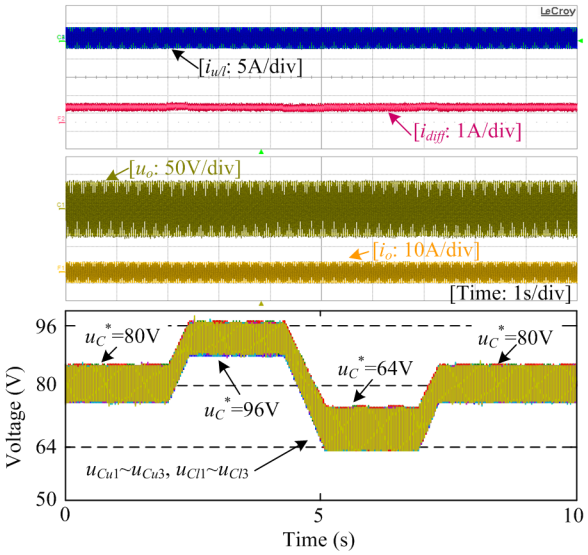


Figure 6.22: Voltage and current waveforms of the MMC at different operation voltage levels.

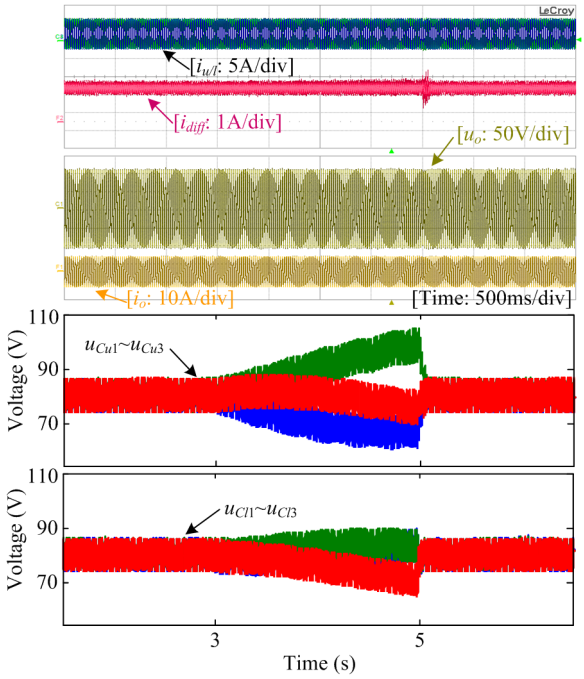


Figure 6.23: Illustration of the effectiveness of the capacitor voltage balancing.

the MMC output voltage and current are scarcely affected by different capacitor voltage levels as long as adequate output voltage can be generated. It is observed

that, with the same output power, the voltage ripples on the capacitor are higher when the average capacitor voltage is lower, and vice versa. The experimental results also show the effectiveness of the proposed average voltage control strategy. The average capacitor voltage is properly adjusted without influencing the system output.

The effectiveness of the voltage balancing control loop has been illustrated in the following set of experiments, whose results are presented in Figure 6.23. After the capacitor voltage balancing controller being disabled at 3 s, the capacitor voltages start to diverge from the set point 80 V. It can be seen that the capacitor voltages of sub-modules in the upper and lower arms are unequally distributed as well. The overall system tends to be unstable because of capacitor voltage divergence without the voltage balancing control. The capacitor voltages converge within about 0.1 s after the voltage balancing is enabled again at 5 s. During the entire process, no severe disturbance introduced by the unbalanced sub-module capacitor voltage is observed in the voltage and current waveforms of the MMC.

6.4.4 Dynamic response

The dynamic response of the MMC during large current reference step changes has been studied in the following experiments.

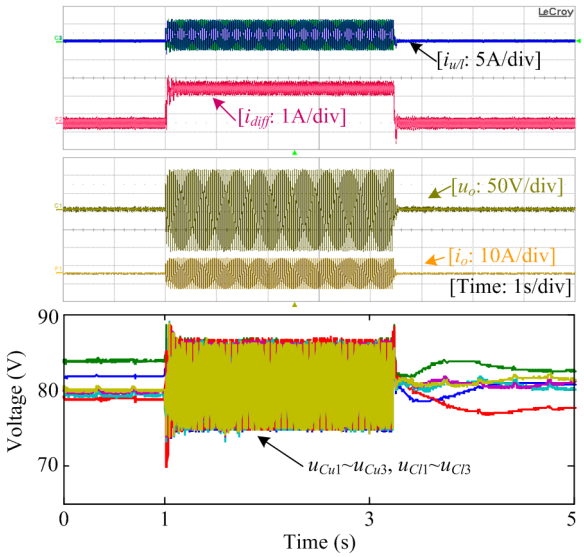
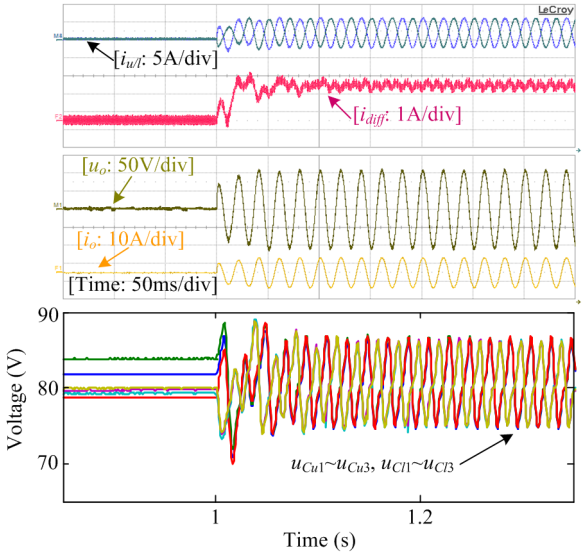
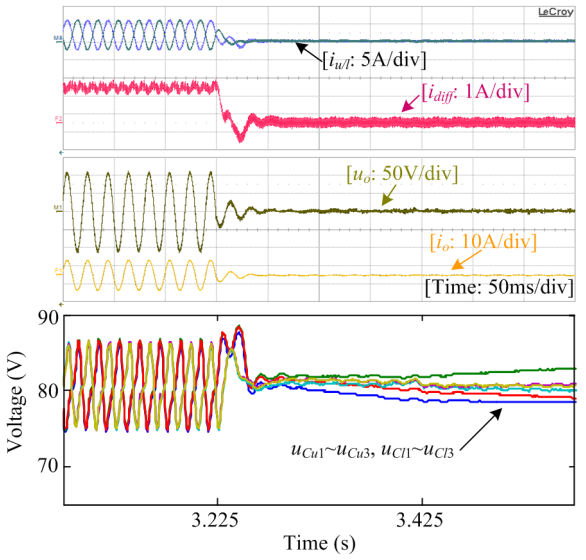


Figure 6.24: Voltage and current waveforms of the MMC during current reference step changes.

The output current is initially set to be zero and then stepped to 9 A at 1 s. After around 2.225 seconds, the output current is set to be zero again. The voltage and current waveforms of the MMC under the distributed control strategy are depicted in Figure 6.24, where it can be seen that the MMC is stable during large operation point step changes even the capacitor voltages are individually



(a)



(b)

Figure 6.25: Zoomed in voltage and current waveforms during current reference step changes: (a) step-up; (b) step-down.

controlled without voltage information in other sub-modules. It is obvious that the capacitor voltages of sub-modules in one phase leg are unequal and cannot be balanced without the output current before 1 s. In contrast, the capacitor voltages converge rapidly when there is an output current from the MMC. After the output current changes to zero again, the capacitor voltages diverge from each other and eventually stabilized at voltage levels around the capacitor voltage set point.

The zoomed in voltage and current waveforms of the MMC in Figure 6.25 present more details during the step changes. The output current tracks its reference within two fundamental cycles without overshoot or oscillation. It takes about 2.5 fundamental periods before the differential current is settled at the new operation point after the $i_o{}^*$ step change. Note that this apparent slow response of i_{diff} is introduced by the delayed updating of $i_{diff,DC}{}^*$, which is calculated for active power balancing according to u_{load} and i_o.

In the other set of experiments, the distributed control strategy has been evaluated when there is a capacitor voltage reference step change. The voltage and current waveforms of the MMC are depicted in Figure 6.26, where the capacitor voltage reference is changed from 70 V to 90 V at 0 s. After the capacitor voltage reference step change, the DC component of the differential current is increased to charge the capacitors according to the capacitor average voltage and differential

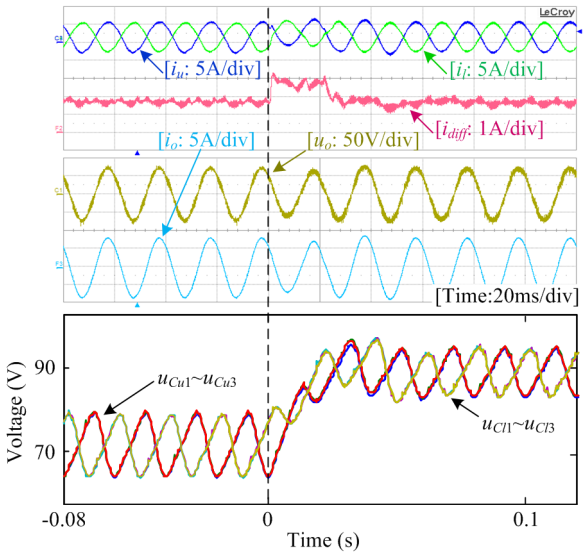


Figure 6.26: Voltage and current waveforms of the MMC during capacitor voltage step change.

current control loops. The capacitor voltages are well-balanced and the average voltage of all capacitors in the phase leg follows the reference within three fundamental periods without severe transients. The experimental results confirm the effectiveness of the distributed control during capacitor voltage step changes.

6.5 Summary

In this chapter, a novel distributed control architecture is presented to improve the modularity of an MMC system.

The existing distributed control strategies for MMCs are reviewed first. It is found that considerable data have to be exchanged in those distributed strategies to ensure the proper operation of MMCs, which introduces high communication burden and makes the design of the control system complicated. A trade-off between the communication network baud rate and the control system bandwidth has been made in existing distributed control strategies.

The distributed control strategy presented in Section 6.2 possesses advantages such as less information exchanging and reduced communication burden. One central controller is used to perform the output current regulation and system-level operations, while the MMC internal dynamics control, PWM signal generation, and local-level protections are distributed into local controllers.

The voltage control loops in each local controller are carefully designed in Section 6.3 to govern the capacitor voltage with only local information. This avoids the capacitor voltage transmission in each control cycle and make the data exchanging independent of number of sub-modules in each arm, which contributes to significantly reduced information exchanging through the communication network and less execution time required. The more modularized control architecture design makes it more flexible and convenient while applying the control strategy for MMCs with different numbers of sub-modules. All control loops for control objectives presented in Chapter 3 are designed and analyzed in Section 6.3.

The controller parameters are selected based on the control loops analysis considering system stability and the disturbances from other sub-modules in Section 6.4. After that, the effectiveness of the distributed control strategy is experimentally verified on the single-phase MMC prototype in the laboratory. The results confirm that the MMC system under the distributed control operates properly and stably in steady-state and during large step changes, with well-regulated and balanced capacitor voltages. All control objectives are achieved with significantly

reduced data exchanging in the distributed control strategy.

Chapter 7

Seamless Fault Tolerant Control for Modular Multilevel Converters

Redundancy in Modular Multilevel Converters (MMCs) greatly increases the system reliability, which is quite important in practical industrial applications. Fault tolerant operation with redundancy sub-modules can be implemented in an MMC, whose precondition is that a fast and accurate fault detection and faulty device localization method has been embedded into the MMC control system. This chapter elaborates a switching device open-circuit fault diagnosis and a fault tolerant operation strategy for a single-phase MMC under the distributed control architecture introduced in Chapter 6. The fault diagnosis is implemented in each individual sub-module without extra hardware circuitry. The fault diagnosis and fault-tolerant control methods improve the reliability of the MMC while maintaining the modularity of its software implementation. Seamless ride-through of switching device open-circuit faults for the MMC is achieved in this chapter.

7.1 Introduction

Modular Multilevel Converters (MMCs) are recently used in high-power applications, such as High-Voltage DC (HVDC) and medium voltage motor drives, in which the reliability is an essential consideration. Although the considerable sub-modules in an MMC are regarded as potential failure points in a part-counting point of view, the redundant sub-modules, as well as fault diagnosis and fault

tolerant techniques, actually increase the reliability of the MMC system [198].

Fault diagnosis is the precondition of the fault tolerant operation for MMCs. A sliding mode observer based fault detection and an assumption-verification process based fault identification are proposed in [199], which locate the faulty switch within 50 ms with relatively high computational burdens. The Kalman filter is adopted to detect open-circuit faults and the faulty sub-module is then localized by comparing the capacitor voltages in the same arm in [200]. The method proposed in [200] can localize different faults occurring in a 50 ms interval. However, the period required to localize the sub-modules ranges from 85ms to more than 250 ms in different scenarios. A state observer based fault detection and capacitor voltage comparison based fault localization are introduced in [201], where only single faulty sub-module can be identified in 50 ms to 150 ms. The above-mentioned fault diagnosis methods employ complicated algorithms with relatively high computational loads to detect the fault based on the MMC states first, and then identify the faulty sub-module according to the MMC internal dynamics, e.g. the circulating current or sub-module capacitor voltages. These methods, either estimating the system states based on the overall MMC model or gathering the sub-module capacitor voltages for fault localization, are suitable to be implemented in a centralized control architecture. Generally, it takes a long time to localize the faulty device in an MMC by aforementioned methods.

The faulty sub-modules identified are generally bypassed and the MMC is required to continuously operate without interruption or significant performance degradation under fault tolerant operation schemes. Hot reserved redundant sub-module schemes [198] are preferred in fault tolerant operation schemes for the sake of excellent transient performance and a higher sub-module utilization ratio. Two control strategies handling redundant sub-modules are introduced in [202]. An MMC control strategy under sub-module fault conditions, which adjusts the capacitor voltage in the faulty arm based on energy balancing of arms with asymmetrical numbers of sub-modules is presented in [198]. Reference [111] proposes two indexes, i.e. dynamic redundancy and sub-module utilization ratio, and synthetically analyzes the MMC operation under fault conditions. An optimized fault tolerant control based on the nearest level modulation scheme is then introduced. An extensive control process for an MMC to ride through a single IGBT open-circuit fault, including fault detection, localization, and system reconfiguration, is detailed in [201]. However, since the faulty IGBT can only be identified after around 50 milliseconds, a fault tolerant method has to be adopted to actively

compensate the voltage disturbances caused by the faulty sub-module before the fault is localized.

In Section 7.2, a switching device open-circuit fault diagnosis method is elaborated and embedded into the distributed control strategy developed in Chapter 6 . The characteristics of the sub-module with switching device in open-circuit faults are analyzed first. A real-time measurement based fault diagnosis is proposed, which can be achieved by simply modifying the measurement points of voltage sensors already equipped in each sub-module. The fault diagnosis method possesses the following distinct features: (a) it is implemented in sub-modules and only requires arm current and locally measured voltage to identify the fault, which can maintain the modularity of the MMC; (b) it is suitable for MMCs with a large number of sub-modules and can be easily extended for applications with different number of sub-modules; (c) it can identify faulty switching devices within a short period before severe malfunction of the MMC or a secondary fault occurs; (d) it can simultaneously localize multiple switching device faults; (e) no extra hardware circuit or sensor is required.

After the fault diagnosis, an effective and easy-to-implement fault tolerant control with hot reserved sub-modules is discussed in Section 7.3. The performance of the MMC after bypassing the faulty sub-modules is investigated in details in Section 7.3.2. The fault tolerant control is accordingly designed so that, even with asymmetrical sub-module operation, the output current, internal dynamics, and switching harmonics cancellation of the MMC can remain the same as those in the normal operation. By properly adjusting the period and phase registers of the PWM modules in the local controller, the fault tolerant control can be achieved. In order to generate a sufficient AC voltage, the capacitor voltages in the faulty arm might be increased according to the number of sub-modules remained in that arm. The control loops in the distributed architecture developed in Chapter 6 are not influenced by the fault diagnosis and fault tolerant control, making the operation transition seamless and reliable.

The fault diagnosis and fault tolerant control are experimentally verified in Section 7.4. The experimental results show that the fault diagnosis can identify faulty switches within 3.5 ms and this method is also immune to system noises and disturbances without triggering faulty alarms. The obtained experimental waveforms under fault tolerant operation are in good agreement with the characteristics analysis of the MMC, implying the effectiveness of the fault tolerant control. Moreover, it is proved that fault identification and system reconfiguration

for fault tolerant operation can be accomplished within 5 ms after the occurrence of switch open-circuit faults in different scenarios. The MMC can operate seamlessly to ride through switching device open-circuit faults without interruptions or catastrophic damages.

7.2 Switching device open-circuit fault diagnosis in local controllers

There are two types of switching device faults, i.e. short-circuit fault and open-circuit fault, should be considered in practical applications. Since the short-circuit fault detection and protection are normally integrated into commercial device drivers [199, 201], only the open-circuit fault of switching devices is discussed in this chapter. Unlike most existing switch open-circuit fault diagnosis methods that the fault detection and fault localization are independently implemented and require a relatively long execution period [199–201], this section develops a real-time measurement based fault diagnosis method that is implemented in the local controller and can identify the faults in one step within a few milliseconds.

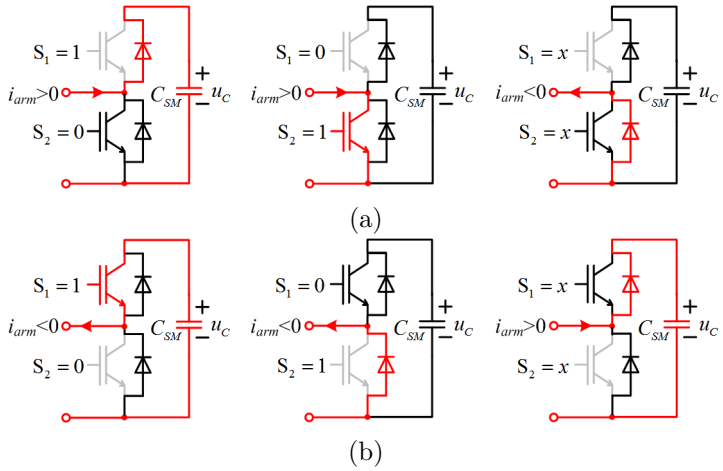


Figure 7.1: Current paths of the sub-module with: (a) S_1 open-circuit fault; (b) S_2 open-circuit fault.

7.2.1 Characteristics of the sub-module with switch open-circuit faults

The sub-module characteristics with switch open-circuit faults are investigated in this subsection. The current paths of the sub-module with open-circuit fault at different devices are illustrated in Figure 7.1. It can be seen in Figure 7.1 (a) that, when S_1 is open-circuit, the current paths are the same as those in the normal condition if $i_{arm} > 0$, and the sub-module is bypassed through the body diode of S_2 if $i_{arm} < 0$ regardless of the gating signals for the switching devices. Such current paths indicate that the sub-module capacitor C_{SM} could not be discharged, which eventually leads to capacitor over-voltage. On the other hand, if S_2 is in open-circuit fault, the sub-module operates normally when $i_{arm} < 0$, and the capacitor is always inserted into the main circuit and continuously charged when $i_{arm} > 0$. In this case, the capacitor voltage will increase as well because the capacitor absorbs more power than that in normal operation. In general, the sub-module with switch open-circuit faults is subject to capacitor over-voltage problems, which might lead to waveform distortions and malfunction of the MMC system. Therefore, the switch open-circuit faults should be detected and localized as soon as possible so that necessary fault-tolerant operation can be seamlessly activated before catastrophic failures occur in the MMC system.

The output voltage of the sub-module, which is the voltage across the two terminals of each sub-module, can be determined by the gating signals and the direction of the arm current in all conditions. As summarized in Table 7.1, the device fault can be detected and located based on the combination of current direction, gating signals, and the sub-module terminal voltage u_{SM}. Specifically, $u_{SM} = 0$ when $i_{arm} < 0$ and $S_1 = 1 \& S_2 = 0$ indicate that S_1 is open-circuit, and $u_{SM} = u_C$ when $i_{arm} > 0$ and $S_1 = 0 \& S_2 = 1$ implies that an open-circuit fault occurs at S_2. Therefore, the sub-module terminal voltage is utilized in the switch open-circuit fault diagnosis in this chapter.

Table 7.1: Sub-module terminal voltage

	$i_{arm} > 0$		$i_{arm} < 0$	
	$S_1 = 1 \& S_2 = 0$	$S_1 = 0 \& S_2 = 1$	$S_1 = 1 \& S_2 = 0$	$S_1 = 0 \& S_2 = 1$
Normal	u_C	0	u_C	0
S_1 fault	u_C	0	0	0
S_2 fault	u_C	u_C	u_C	0

7.2.2 Open-circuit fault diagnosis

The sub-module voltage has to be measured in order to utilize its characteristics to detect the switch open-circuit fault. Normally, adding extra voltage transducers and hardware circuitry into the MMC is undesirable from a cost-effective point of view. It should be noted that there is already one voltage sensor embedded in each sub-module for capacitor voltage control and balancing purposes. Therefore, the measuring points of the existing voltage sensors are reconfigured so that the sub-module terminal voltage can be monitored without affecting the voltage control. As can be seen in Figure 7.2, one of the measurement points is moved to the middle point of the two switching devices to monitor the sub-module terminal voltage.

The voltage measurement instances are associated with the triangular carrier as shown in Figure 7.3, where the terminal voltage u_{SM} is measured at the peaks and valleys of the triangular carrier. According to Figure 7.3 and Table 7.1, in normal operations, u_{SM} is equal to zero when the carrier is at peak values (for example, the k^{th} sampling instance) and $u_{SM} = u_C$ when the carrier reaches zero (the $(k+1)^{th}$ sampling instance). Therefore, $u_{SM} = 0$ and $u_{SM} = u_C$ are alternatively obtained at sampling instances triggered by the ePWM module in the local controller. It is demonstrated in [203] that the capacitor voltage balancing

Figure 7.2: Measurement points of the voltage sensor: (a) conventional; (b) proposed.

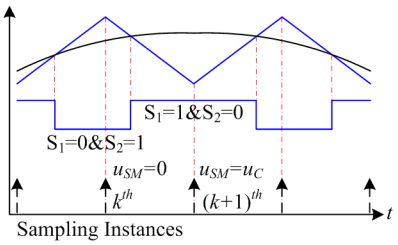


Figure 7.3: Voltage sampling instances associating with the triangular carrier.

control strategy is still effective when the sub-module carrier frequency is around 100 Hz. Therefore, the proposed capacitor voltage measurement are applicable in HVDC applications with a carrier frequency in the range 110 - 130 Hz. Multi-sampling technique [192] can also be employed to measure the terminal voltage much frequently to rapidly identify the open-circuit faults in HVDC applications with low carrier frequency. The capacitor voltages are still conditionally accessible during the MMC start-up pre-charging and the temporary shutdown cases as long as the capacitor is charged through the body diode of the switch S_1 [204].

The implementation of the switch open-circuit fault diagnosis combined with the capacitor voltage measurement in a local controller is illustrated by the flowchart shown in Figure 7.4. Two objectives, i.e. capacitor voltage feedback for control loops and open-circuit fault diagnosis, have to be simultaneously achieved. In the normal operation, the measured voltage at the carrier valleys are directly deemed as the sub-module capacitor voltage and utilized in capacitor voltage control and balancing, as long as the corresponding sub-module is not over-modulated. On the other hand, switch open-circuit faults can be identified by the combination of sampling instances, sub-module terminal voltage, and arm current direction. If $u_{SM} > u_{SM,thr1} = 0.7u_C{}^*$ is obtained at the peak points of the carrier for

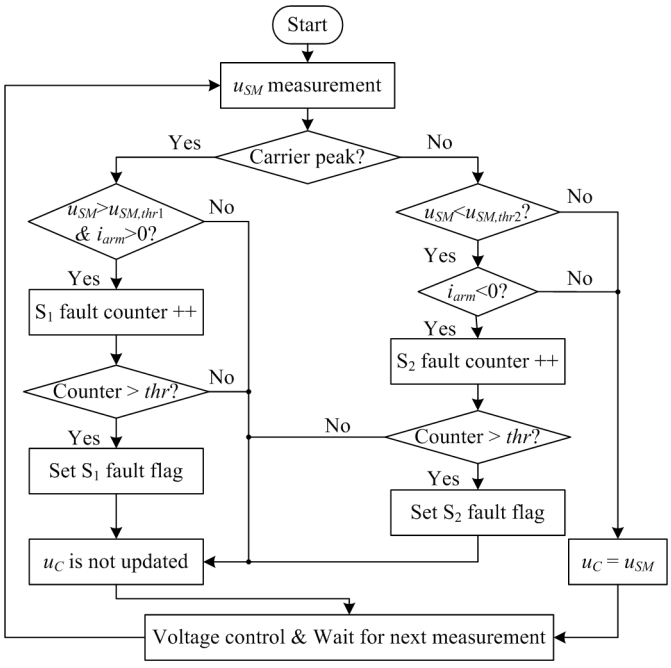


Figure 7.4: Flowchart of the fault diagnosis in the local controller.

$i_{arm} > 0$, an open-circuit fault occurs at S_2; if $u_{SM} < u_{SM,thr2} = 0.3u_C{}^*$ is obtained at the valley points of the carrier for $i_{arm} < 0$, S_1 is open-circuit.

It should be noted that the terminal voltage sampled at carrier valley being less than $u_{SM,thr2}$ might be caused either by the low capacitor voltage or S_2 open-circuit fault. In this case, arm current direction is required in order to determine if the measured terminal voltage can be used as the capacitor voltage. $i_{arm} > 0$ implies that the capacitor voltage is actually quite low so that $u_C = u_{SM}$ is utilized in capacitor voltage control, while u_C is not updated if $i_{arm} < 0$. This mechanism prevents that, when there is an open-circuit fault at S_2, the incorrect voltage is utilized in the closed voltage control loops and consequently leads to rapid divergence or severe oscillation of sub-module capacitor voltages. The fault counters and threshold (thr), as shown in Figure 7.4, are adopted to prevent false alarm introduced by measurement noises or other disturbances. The fault flags are set only if the values of the counters are higher than the threshold, and the counters are cleared if the values are lower than the threshold for one fundamental period. Therefore, a trade-off is made between the speed and accuracy of the fault diagnosis.

Since the fault diagnosis method is directly based on real-time measurements, it is possible to identify the faulty switches within a short time, e.g. a few sampling intervals. Moreover, as the device fault detection is implemented in the local controller with the information of only current direction, sub-module terminal voltage, and sampling instance of the corresponding sub-module, it is able to simultaneously identify multiple device open-circuit faults and can be easily extended to MMCs with a large number of sub-modules. The identified faulty switch information could be helpful for future fault analysis, system maintenance, and components replacement.

7.3 Fault tolerant control for MMCs

In this section, the MMC is assumed to operate with $N + N_r$ sub-modules in each arm, as shown in Figure 7.5. The first N sub-modules are normal ones required to generate the MMC output voltage. The extra N_r sub-modules operate as hot reserved redundant ones to increase the reliability of the overall MMC system [198]. After identifying an open-circuit fault, the local controller immediately bypasses the corresponding sub-module with the faulty switch and send a warning message to the central controller to indicate the bypassed sub-module. The central

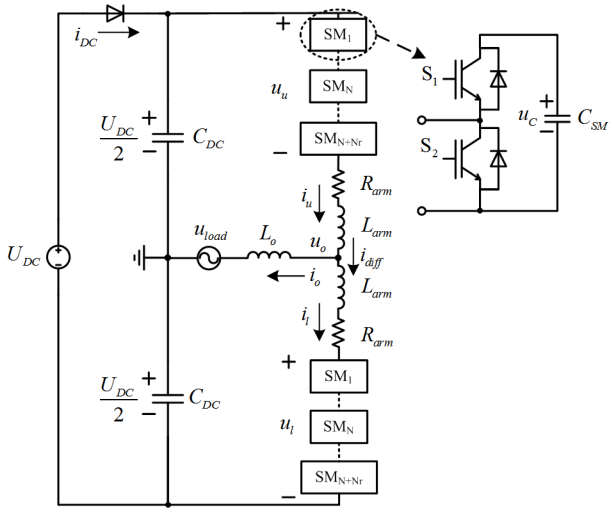


Figure 7.5: Structure of a single phase MMC with redundant sub-modules.

controller adjusts the capacitor voltage references for the remaining sub-modules according to the operation condition of the MMC and broadcasts the information regarding the bypassed sub-module to other sub-modules in the same arm within one or two control cycles. The remaining sub-modules then operate under a fault tolerant control after receiving that information. The interval between the fault occurrence and the fault tolerant operation is short enough so that the MMC works seamlessly during the operation mode transition. The control loops in the central and local controllers are scarcely affected by the fault tolerant operation.

7.3.1 Normal operation of the MMC

The normal operation of the MMC with the distributed control architecture has been explained in details in Section 6.2 and 6.3. The distributed control system in the normal operation of the MMC is depicted in Figure 6.3 (b). The only difference is that N_r redundant sub-modules have to be taken into account while designing the control system. Practically, the rated amplitude of the output voltage in the normal operation can be designed as $0.5U_{DC}N/(N + N_r)$. It is reasonable if a relatively large number of sub-modules are adopted in the MMC and $N \gg N_r$. Therefore, by defining $u_C{}^* = U_{DC}/(N + N_r)$ for all $N + N_r$ sub-modules in each arm, the N normal sub-modules are capable of generating the required output voltage with reduced voltage stress on the sub-module components. The rated working voltage of the sub-module capacitor can be selected as U_{DC}/N while its

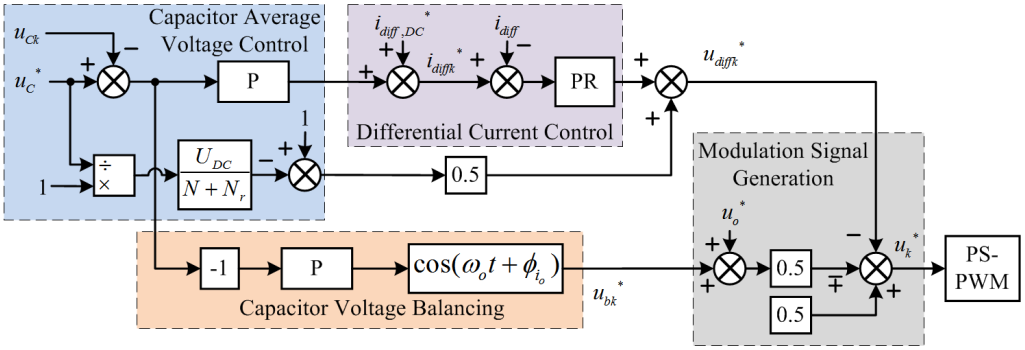


Figure 7.6: Block diagram of the local controller.

voltage limitation is $(1+\varepsilon)U_{DC}/N$, where ε in p.u. is the voltage margin reserved. Note that $u_C{}^*$ is not necessarily sent to local controllers in each control cycle since, ideally, it is unchanged in the normal operation of the MMC.

The detailed control loops in the k^{th} local controller are shown in Figure 7.6. Two resonant (R) controllers coping with the signal at the fundamental and second-order frequencies are paralleled to a proportional (P) controller to regulate i_{diff}. The equilibrium voltage for the capacitor average voltage feed-forward control is modified as $U_{DC}/(N+N_r)$.

7.3.2 MMC operates with sub-modules bypassed

After identifying the switch open-circuit fault, the corresponding sub-module is bypassed and the MMC has to operate with reduced and asymmetrical numbers of sub-modules in arms. Noting that the same output reference $u_o{}^*$ calculated by the central controller has been sent to all sub-modules, a distorted output voltage will be inevitably introduced since the numbers of the sub-modules in the upper and lower arms are different due to the sub-module failure. Assuming N_f sub-modules are bypassed in the upper arm and denoting the well-balanced capacitor voltages in the two arms as u_{Cu} and u_{Cl} respectively, the inserted voltages of the upper and lower arms can be expressed as

$$\begin{cases} u_{u,f} = u_{Cu} n_u (N + N_r - N_f) \\ u_l = u_{Cl} n_l (N + N_r) \end{cases} \tag{7.1}$$

Ignoring the voltage ripples on the sub-module capacitors in (6.4), the capacitor voltages can be denoted as $u_{Cu} = u_{Cl} = U_C = U_{DC}/(N+N_r)$. According

to (5.32), (6.2), (6.3) and (7.1), the output voltage of the MMC under the fault condition can be derived as

$$u_{o,f} = \frac{u_l - u_{u,f}}{2} \approx \left(1 - \frac{0.5N_f}{N + N_r}\right) u_o + \frac{0.25N_f}{N + N_r} U_{DC} \tag{7.2}$$

where the terms containing ${u_{diff}}^*$ are ignored since normally ${u_{diff}}^* \ll {u_o}^*$. It is obvious in (7.2) that the fundamental component of the MMC output voltage is reduced by $0.5u_oN_f/(N + N_r)$ and a DC bias $0.25U_{DC}N_f/(N + N_r)$ exists in the output voltage. The output current regulation in the central controller will try to force the output current to track its reference by adjusting the output voltage reference as ${u_{o,f}}^*$. Letting $u_{o,f} = u_o$, the voltage reference ${u_{o,f}}^*$ under the fault condition can be obtained as

$${u_{o,f}}^* = -\frac{0.5N_f}{N + N_r - 0.5N_f} + \frac{N + N_r}{N + N_r - 0.5N_f} \frac{2U_o \cos(\omega_o t)}{U_{DC}} \tag{7.3}$$

Moreover, the differential voltage applied onto the arm inductors and resistors in the fault condition can be expressed as

$$\begin{aligned} u_{diff,f} &= U_{DC} - u_l - u_{u,f} \\ &= U_C \left[2(N + N_r){u_{diff}}^* + N_f \left(\frac{1}{2} - \frac{{u_{o,f}}^*}{2} - {u_{diff}}^*\right)\right] \\ &= 2U_{DC}{u_{diff}}^* + \frac{0.5N_fU_{DC}}{N + N_r - 0.5N_f} - \frac{N_fU_o \cos(\omega_o t)}{N + N_r - 0.5N_f} - \frac{N_fU_{DC}{u_{diff}}^*}{N + N_r} \end{aligned} \tag{7.4}$$

The first term on the right-hand side of (7.4) is the differential voltage applied in normal conditions. The other three terms will introduce a DC bias and low-frequency components into the differential voltage. Consequently, undesirable capacitor voltage shifting [71] and low frequency circulating current ripples in the phase leg are introduced, which are regarded as disturbances for internal dynamics controls.

Moreover, the switching functions of the i^{th} sub-module in the upper and lower arms generated based on the phase-shifted PWM can be expressed in Fourier series

form equations (3.40) and (3.41) as

$$\begin{cases} s_{ui,f} = \dfrac{1}{2} - \dfrac{{u_{o,f}}^*}{2} + \displaystyle\sum_{k=1}^{\infty}\sum_{n=-\infty}^{\infty} \frac{2}{k\pi}\sin\left[\frac{(k+n)\pi}{2}\right] \times J_n\left(\frac{m_o k\pi}{2}\right) \\ \qquad \times \cos\left[k\left(\omega_c t + \alpha + \beta + (i-1)\dfrac{2\pi}{N+N_r}\right) + n\left(\omega_o t + \pi\right)\right] \\ s_{li,f} = \dfrac{1}{2} + \dfrac{{u_{o,f}}^*}{2} + \displaystyle\sum_{k=1}^{\infty}\sum_{n=-\infty}^{\infty} \frac{2}{k\pi}\sin\left[\frac{(k+n)\pi}{2}\right] \times J_n\left(\frac{m_o k\pi}{2}\right) \\ \qquad \times \cos\left[k\left(\omega_c t + \alpha + (i-1)\dfrac{2\pi}{N+N_r}\right) + n\omega_o t\right] \end{cases} \tag{7.5}$$

Denoting the N_f bypassed sub-modules in the upper arm as $\mathbb{N}_{by} = \{N_{by1},\ \ldots,\ N_{byN_f}\}$, the sums of the switching functions in the upper and lower arms can be expressed as

$$\begin{cases} s_{u,f} = \dfrac{N+N_r-N_f}{2} - \dfrac{(N+N_r-N_f){u_{o,f}}^*}{2} \\ \qquad + \displaystyle\sum_{i=1}^{N+N_r \& i\notin\mathbb{N}_{by}} \sum_{k=1}^{\infty}\sum_{n=-\infty}^{\infty} \frac{2}{k\pi}\sin\left[\frac{(k+n)\pi}{2}\right] \times J_n\left(\frac{m_o k\pi}{2}\right) \\ \qquad \times \cos\left[k\left(\omega_c t + \alpha + \beta + (i-1)\dfrac{2\pi}{N+N_r}\right) + n\left(\omega_o t + \pi\right)\right] \\ s_{l,f} = \dfrac{N+N_r}{2} + \dfrac{(N+N_r){u_{o,f}}^*}{2} + \displaystyle\sum_{i=1}^{N+N_r}\sum_{k=1}^{\infty}\sum_{n=-\infty}^{\infty} \frac{2}{k\pi}\sin\left[\frac{(k+n)\pi}{2}\right] \\ \qquad \times J_n\left(\frac{m_o k\pi}{2}\right) \times \cos\left[k\left(\omega_c t + \alpha + (i-1)\dfrac{2\pi}{N+N_r}\right) + n\omega_o t\right] \end{cases} \tag{7.6}$$

Noting that

$$\begin{cases} \displaystyle\sum_{i=1}^{N+N_r} \cos\left[(i-1)\frac{2k\pi}{N+N_r}\right] = 0,\ k/(N+N_r) \notin \mathbb{N}^+ = \{1,2,3,\cdots\} \\ \displaystyle\sum_{i=1}^{N+N_r} \sum_{k/(N+N_r)\in\mathbb{N}^+} \cos\left[k\left(\omega_c t + \alpha + (i-1)\frac{2\pi}{N+N_r}\right) + n\omega_o t\right] \\ = (N+N_r) \displaystyle\sum_{k/N\in\mathbb{N}^+} \cos\left[k\left(\omega_c t + \alpha\right) + n\omega_o t\right] \end{cases} \tag{7.7}$$

equation (7.6) can be rewritten as

$$\begin{cases} s_{u,f} = \dfrac{N+N_r-N_f}{2} - \dfrac{(N+N_r-N_f){u_{o,f}}^*}{2} \\ \qquad + \displaystyle\sum_{k/(N+N_r)\in\mathbb{N}^+} \sum_{n=-\infty}^{\infty} \frac{2(N+N_r)}{k\pi} \sin\left[\frac{(k+n)\pi}{2}\right] \\ \qquad \times J_n\left(\frac{mk\pi}{2}\right) \times \cos\left[k\left(\omega_c t+\alpha+\beta\right)+n\left(\omega_o t+\pi\right)\right] \\ s_{l,f} = \dfrac{N+N_r}{2} + \dfrac{(N+N_r){u_{o,f}}^*}{2} \\ \qquad + \displaystyle\sum_{k/(N+N_r)\in\mathbb{N}^+} \sum_{n=-\infty}^{\infty} \frac{2(N+N_r)}{k\pi} \sin\left[\frac{(k+n)\pi}{2}\right] \\ \qquad \times J_n\left(\frac{mk\pi}{2}\right) \times \cos\left[k\left(\omega_c t+\alpha\right)+n\omega_o t\right] \end{cases} \tag{7.8}$$

Although α and β are selected according to Table 3.1 to cancel the low order switching harmonics in normal operations, (7.8) suggests that the harmonics and side-bands around carrier frequency ω_c can be found in $s_{u,f}$ due to the asymmetrical switching actions after bypassing N_f sub-modules in the upper arm.

7.3.3 Fault tolerant operation for the MMC

In the fault-tolerant operation, the output and internal dynamics of the MMC should be kept the same as those in the normal operation, with balanced capacitor average voltages in the same arm or phase leg [205]. The DC and fundamental components in the arm currents have to remain unchanged for the same input and output power of the MMC. Equation (7.1) suggests that the inserted voltage in the upper arm is reduced because N_f sub-modules are bypassed. Therefore, the output voltage of each sub-module in the upper arm has to be increased to meet the requirement of the loads, which can be achieved by increasing the amplitude of the fundamental component in n_{uk} or increasing the average capacitor voltage in the faulty arm as long as the capacitors are in the safe operation area. On the other hand, the input DC power of sub-modules in the upper arm has to be accordingly adjusted as well to compensate their output active power, by introducing a DC bias into n_{uk}. The proposed fault tolerant operation scheme can be implemented in two scenarios, according to the number of faulty sub-modules.

Scenario I: $N_r \geq 2N_f$

The maximum symmetrical output voltage of the MMC under the fault condition can be expressed as

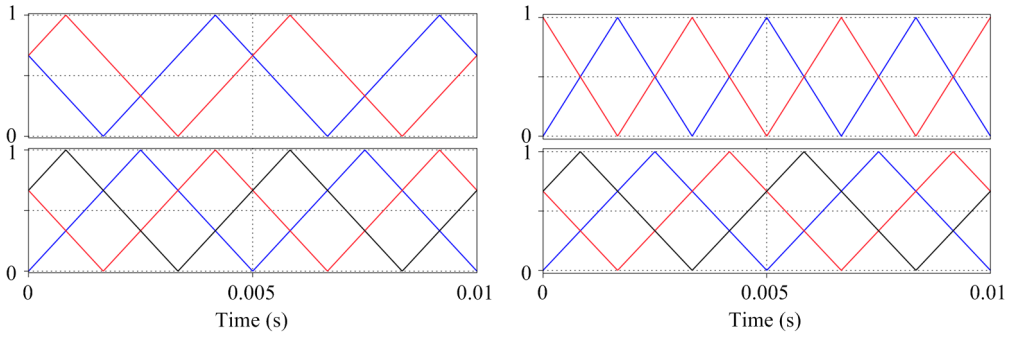
$$\min\left[\left(N+N_r-N_f\right)u_{Cu,f},\left(N+N_r\right)u_{Cl}\right]-\frac{U_{DC}}{2}\geq\frac{N}{N+N_r}\frac{U_{DC}}{2} \tag{7.9}$$

where $u_{Cu,f}$ is the balanced sub-module capacitor voltage in the upper arm with N_f sub-modules bypassed. It should be noted that $u_{Cl}=U_{DC}/(N+N_r)$ always satisfies the inequality (7.9) in this scenario, therefore only the $(N+N_r-N_f)u_{Cu,f}$ term is discussed. The minimum $u_{Cu,f}$ required to generate the desired output voltage can be obtained as

$$u_{Cu,f}=\left(\frac{N+0.5N_r}{N+N_r}\right)\frac{U_{DC}}{(N+N_r-N_f)} \tag{7.10}$$

$$u_{Cu}-u_{Cu,f}=\frac{0.5N_r-N_f}{\left(N+N_r-N_f\right)\left(N+N_r\right)}U_{DC} \tag{7.11}$$

It can be seen in (7.11) that the capacitor average voltage in the normal operation ($u_{Cu}=U_{DC}/(N+N_r)$) is sufficient to generate the required output voltage in the case of $N_r \geq 2N_f$. Therefore, in this scenario, the average capacitor voltage reference for all sub-modules remains unchanged. By re-scaling the modulation signals for the sub-modules in the upper arm by $(N+N_r)/(N+N_r-N_f)$, both the output voltage and the DC bias for active power balancing are increased. Ideally, the voltage inserted into the upper arm is $u_{u,f}=u_{Cu}n_{uk}(N+N_r)$, which is the



(a) (b)

Figure 7.7: Triangular carriers: (a) In normal PS-PWM scheme while one sub-module is bypassed; (b) In modified PS-PWM scheme.

same with that in the normal operation. Consequently, the output and differential voltages remain uninfluenced even N_f sub-modules are bypassed in the upper arm.

Moreover, the carriers in the upper and lower arms are asymmetric because of the N_f bypassed sub-modules as shown in Figure 7.7 (a). The harmonics and sidebands around the frequency ω_c derived in (7.8) significantly increase the current ripples in the upper arm, since the lowest frequency of the switching harmonics in the arm current is reduced from Nf_c to f_c. In order to achieve the same switching harmonics cancellation, the carrier frequency of the sub-modules in the upper arm is increased to $f_c(N+N_r)/(N+N_r-N_f)$ and the phase displacement between adjacent carriers is reset to $2\pi/(N+N_r-N_f)$, in order to obtain the symmetrically distributed triangular carriers in the upper arm, as shown in Figure 7.7 (b). The modified PS-PWM scheme shown in Figure 7.7 (b) also guarantees the same control bandwidth for current control loops.

Applying the aforementioned modulation signal re-scaling, triangular carrier frequency adjusting, and phase angle modification, equation (7.8) can be expressed as

$$\begin{cases} s_{u,f} = \dfrac{N+N_r}{2} - \dfrac{(N+N_r){u_o}^*}{2} \\ \quad + \displaystyle\sum_{k/(N+N_r-N_f)\in\mathbb{N}^+} \sum_{n=-\infty}^{\infty} \frac{2(N+N_r-N_f)}{k\pi} \sin\left[\left(\frac{N+N_r}{N+N_r-N_f}k+n\right)\frac{\pi}{2}\right] \\ \quad \times J_n\left(\dfrac{N+N_r}{N+N_r-N_f}\dfrac{m_o k\pi}{2}\right) \\ \quad \times \cos\left[\dfrac{N+N_r}{N+N_r-N_f}k\left(\omega_c t+\alpha+\beta\right)+n\left(\omega_o t+\pi\right)\right] \\ s_{l,f} = \dfrac{N+N_r}{2} + \dfrac{(N+N_r){u_o}^*}{2} \\ \quad + \displaystyle\sum_{k/(N+N_r)\in\mathbb{N}^+} \sum_{n=-\infty}^{\infty} \frac{2(N+N_r)}{k\pi} \sin\left[\frac{(k+n)\pi}{2}\right] \\ \quad \times J_n\left(\dfrac{mk\pi}{2}\right) \times \cos\left[k\left(\omega_c t+\alpha\right)+n\omega_o t\right] \end{cases} \tag{7.12}$$

Equation (7.12) reveals that the same low-frequency components and switching harmonic cancellation can be achieved as in the normal operation.

Noting that the amplitudes of the voltage ripples U_{C1} and U_{C2} in (6.4) are influenced by the modulation signals [52], the sub-module capacitor voltage in the

upper arm under the fault tolerant operation can be expressed as

$$\begin{cases} u_{Cu,f} = U_C + U_{C1,f}\cos(\omega_o t + \phi_{C1,f}) + U_{C2,f}\sin(2\omega_o t + \phi_{i_o}) \\ U_{C1,f} = \sqrt{\dfrac{\left(\dfrac{N+N_r}{N+N_r-N_f}\right)^4 {m_o}^4\cos^4\phi_{i_o} + 4}{{m_o}^4\cos^4\phi_{i_o} + 4}}U_{C1} \\ U_{C2,f} = \dfrac{N+N_r}{N+N_r-N_f}U_{C2} \end{cases} \tag{7.13}$$

The voltage applied on the arm inductors and resistors can be obtained as

$$\begin{aligned} u_{diff,f} &= U_{DC} - u_{u,f} - u_l \\ &= U_{DC} - \frac{(N+N_r)}{2}\left\{u_{Cu,f}\left[1 - m_o\cos(\omega_o t)\right] + u_{Cl}\left[1 + m_o\cos(\omega_o t)\right]\right\} \\ &= \frac{(N+N_r)}{2}\Bigg[U_{C1}\cos(\omega_o t + \phi_{C1}) - U_{C1,f}\cos(\omega_o t + \phi_{C1,f}) \\ &\quad + \frac{0.5 m_o N_f U_{C2}}{N+N_r-N_f}\sin(\omega_o t + \phi_{i_o}) + \text{otherterms}\Bigg] \end{aligned} \tag{7.14}$$

Fundamental components, which are introduced by the asymmetrical voltage ripples across the capacitors in the upper and lower arms, can be found in (7.14) and eventually induce fundamental circulating current ripples in the phase leg. Such fundamental circulating current can be suppressed by the paralleled resonant controller coping with signals at the fundamental frequency in the differential current controller shown in Figure 7.6.

The fault tolerant control in this scenario can be easily implemented in the distributed control architecture. After receiving the warning message from a particular sub-module N_p, the central controller informs the sub-modules in the same arm that the ${N_p}^{th}$ sub-module is bypassed and these sub-modules should be in fault-tolerant operation mode. By setting ePWM period registers of remaining local controllers in the faulty arm to be $T_c(N+N_r-N_f)/(N+N_r)$, the frequency of the carrier is increased and the amplitude of the triangle is accordingly reduced. The modulation signals for the sub-modules in the corresponding arm are consequently re-scaled. The phase registers of these ePWM modules are updated as well to ensure the phase displacement of $2\pi/(N+N_r-N_f)$ among triangular carriers. Since each sub-module possesses a unique ID, the exact value assigned to the phase register can be decided based on the number of remaining sub-modules and

its ID. To be specific, only the sub-modules having IDs behind the bypassed $N_p{}^{th}$ sub-module need to reset their phase registers according to their new sequence in the faulty arm. The overall process can be completed within a few control cycles.

Scenario II: $2N_f > N_r \geq N_f$

Since the right-hand-side of (7.11) is less than zero in this scenario, the capacitor voltages in the faulty arm should be increased to generate the desired output voltage with reduced sub-modules. All the values assigned to the period and phase registers in the local controllers are the same with those in Scenario I. The only difference is that the new capacitor voltage reference $u_{C,f}{}^*$ is calculated according to the number of the remaining sub-modules in the faulty arm, e.g., $u_{C,f}{}^* = U_{DC}/(N + N_r - N_f)$. In this scenario, the voltage ripples across the capacitors in the upper and lower arms are almost the same since the modulation index m_o for all sub-modules in that phase are almost the same. Therefore, little fundamental circulating current is induced in the phase leg. The current ripples in the faulty arm caused by switching actions have the same frequencies as those in Scenario I.

7.4 Case study and experimental results

The fault diagnosis and fault tolerant control for the MMC are embedded into the prototype developed in Chapter 6, with modified voltage measurement points in all sub-modules. The key parameters of the single-phase MMC system shown in Figure 7.5 are the same with those listed in Table 5.1. The number of sub-modules in each arm is defined as $N + N_r = 3$. The sampling frequency in the central controller is designed to be $f_s = 12$ kHz. On the other hand, the sampling frequency for capacitor voltage measurement in the local controller is $f_c = 2$ kHz. The period for the voltage control cycle is $T_c = 1/f_c$. Therefore, there will be a $1.5T_s$ and $1.5T_c$ digital control delays in the current and capacitor voltage control loops. The controller parameters listed in Table 6.1 are adopted in the verification experiments in this chapter. The fault diagnosis function and the fault tolerant control are enabled in all experiments.

7.4.1 MMC performance in normal operation

The performance of the MMC in the normal operation has been demonstrated in the following experiments.

The capacitor voltage references for all sub-modules are set to be 80 V ($U_{DC}/(N+N_r)$) and the amplitude of the output voltage is 96 V (output current is 6 A). Figure 7.8 shows the voltage and current waveforms of the MMC in the steady-state operation, where a seven-level output voltage and a sinusoidal output current tracking its reference accurately can be observed. The second-order harmonics in i_{diff} is effectively suppressed with the help of the resonant controller. Moreover, the sub-module capacitor voltages are well balanced around their setting point 80 V. The dynamic response of the MMC during large current reference step changes has been evaluated in the experiments, in which the output current is initially set to be 3 A and then stepped to 6 A at t1. The voltage and current waveforms of the MMC are depicted in Figure 7.9, where the MMC system is stable and the transients are smooth during large operation point step changes.

The waveforms of the MMC in the steady state and during step changes imply that the voltage measurement point modification and measured data processing designed in Subsection 7.2.2 will not introduce significant influence to the control loops. All the MMC control objectives, such as output and internal dynamics regulation, are achieved without performance deterioration. Moreover, the fault diagnosis is immune to the noises and disturbances in the steady state and during

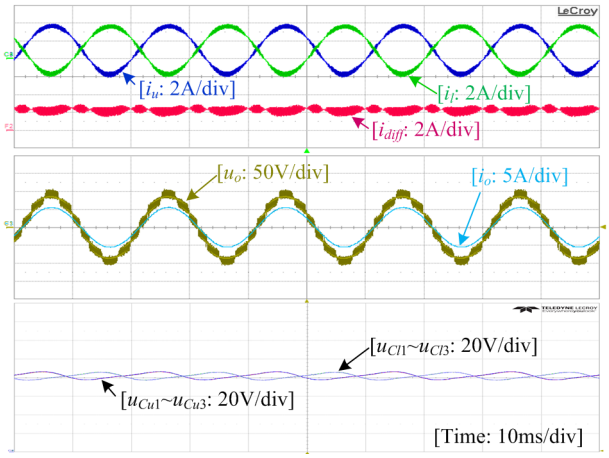


Figure 7.8: Voltage and current waveforms of the MMC in the steady-state operation.

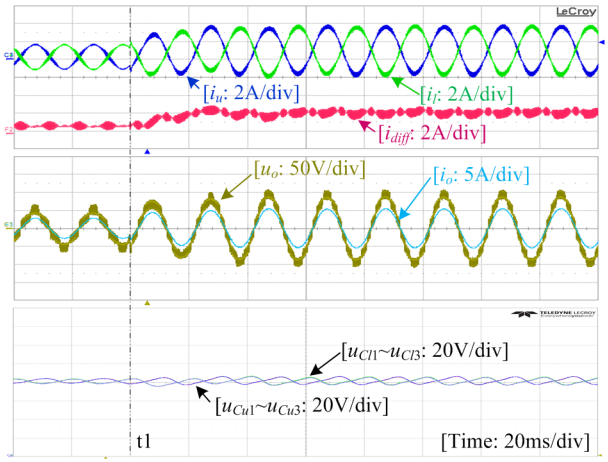


Figure 7.9: Voltage and current waveforms of the MMC during the current reference step change.

large step changes since no false alarm is triggered in the normal operation of the MMC.

7.4.2 MMC performance with switch open-circuit faults

In the following sets of experiments, the MMC performance in fault tolerant operation with one and multiple switch open-circuit faults has been investigated and evaluated. The open circuit fault of the switch is generated by applying a low-level gating signal to the corresponding device. The open-circuit faults at different switches are identified by sub-modules themselves. After identifying the fault, the local controller bypasses the faulty sub-module by assigning a high-level gating signal to the lower switch in that sub-module. The central controller coordinates the operation of the remaining sub-modules as soon as it has received the fault information.

Single switch open-circuit

In this set of experiments, single switch open-circuit fault in the second sub-module in the upper arm (SM_{u2}) is generated.

Fault tolerant operation scenario I: In this scenario, $N = 1$, $N_r = 2$, and $N_f = 1$ are selected and the maximum output voltage of the MMC is 40 V according to the discussion in Subsection 7.3.3. The output current of the MMC

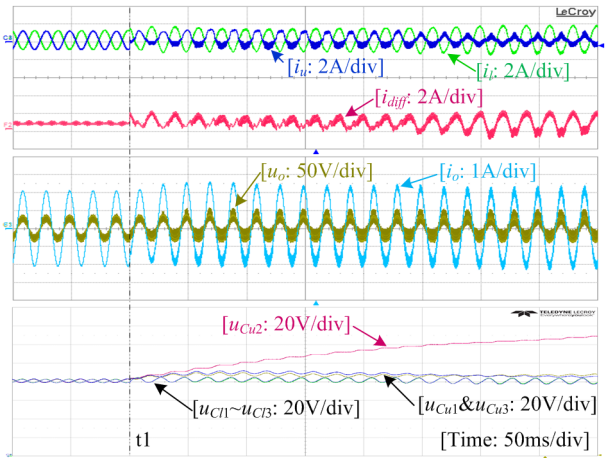
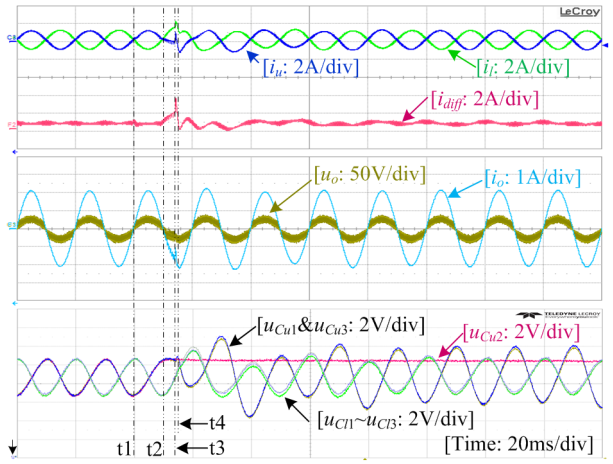


Figure 7.10: Voltage and current waveforms of the MMC with S_1 open-circuit fault in SM_{u2}.

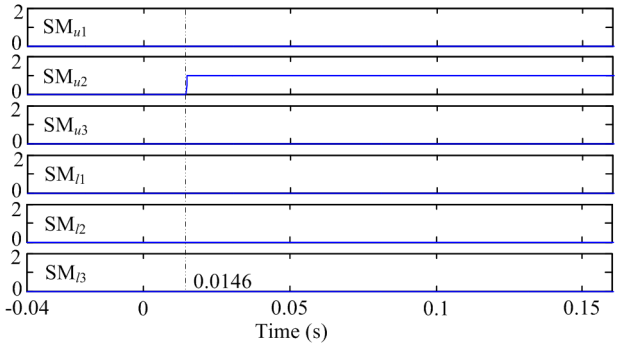
is regulated as 2.3 A so that the amplitude of the MMC output voltage is 37 V. The average capacitor voltage of the sub-modules in the entire phase leg remains unchanged as 80 V.

The voltage and current waveforms of the MMC when the switch S_1 in SM_{u2} is forced to open are presented in Figure 7.10, where no fault diagnosis and fault tolerant operation is applied. It can be seen that the arm currents and differential current are highly distorted. An obvious fundamental component can be observed in the differential current, and high switching current ripples can be found in the arm current as well. The capacitor voltage of SM_{u2} increases to a quite high value and might result in capacitor or other component failure due to over-voltage. Once the switch open-circuit fault occurs, the MMC system without fault diagnosis and fault tolerant control has to shut down to avoid secondary failure.

Figure 7.11 illustrates the waveforms of the MMC with S_1 open-circuit fault in SM_{u2} while the fault diagnosis and fault tolerant control are applied. The open-circuit fault detection results of all sub-modules are presented in Figure 7.11 (b), where the curves indicate the status of the devices in each sub-module. An S_1 open-circuit fault is detected if the status is 1 and an S_2 open-circuit fault is identified if the status is 2. After S_1 being forced to open at t1 = 0 s, the MMC operates normally with slightly distorted current in the upper arm since the arm current is positive and flows as normal through the body diode of S_1, until the upper arm current crosses zero at t2 = 11.8 ms. The fault diagnosis starts to execute from t2 and the S_1 open-circuit fault in SM_{u2} is correctly identified at t3



(a)



(b)

Figure 7.11: Waveforms in fault tolerant operation scenario I with S_1 open-circuit fault in SM_{u2}: (a) current and voltage waveforms; (b) fault detection results for the six sub-modules.

= 14.6 ms, 2.8 ms later after t2, as shown in Figure 7.11 (b). After t3, u_{Cu2} is a straight line since SM_{u2} has been immediately bypassed. The central and local controllers exchanges the necessary fault and operation information, and then the period and phase registers for the PWM generation for sub-modules in the upper arm are accordingly reset, at t4 = 15.3 ms. At t4, the process of fault diagnosis and system reconfiguration is completed within 3.5 ms and the MMC operates under the fault tolerant operation scheme. It is clear in Figure 7.11 (a) that the output voltage and current are almost the same before and after the open-circuit fault occurs. The current ripple and high-frequency harmonics in the arm currents are scarcely affected by bypassing the faulty sub-module, which means that the same equivalent switching frequency and switching harmonics cancellation are achieved

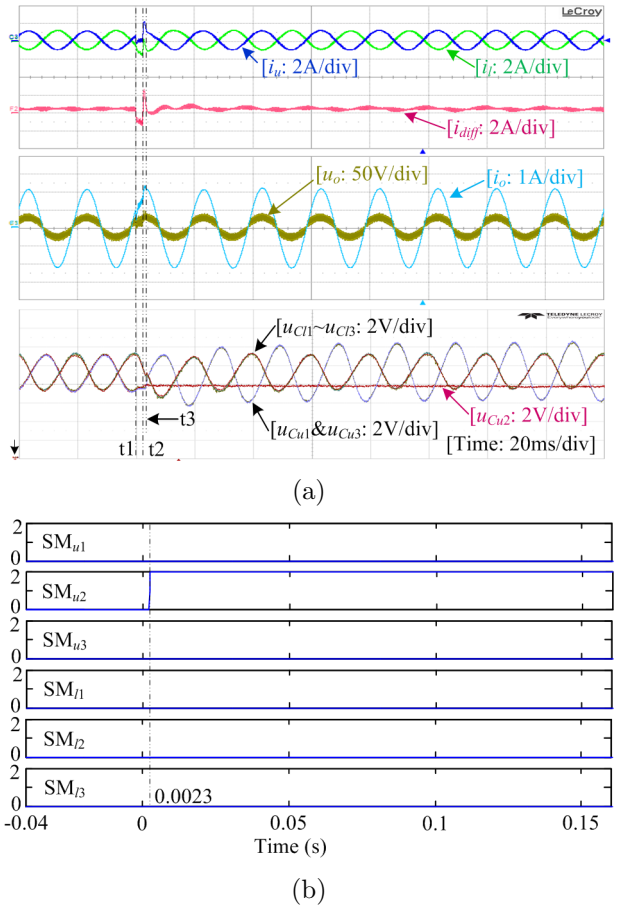
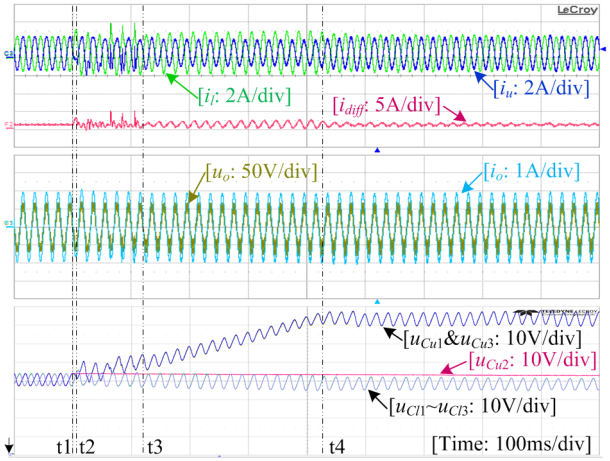


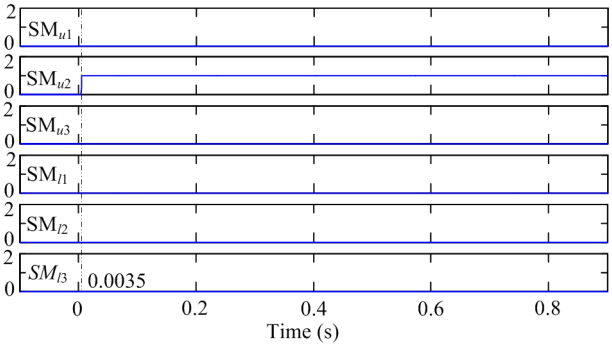
Figure 7.12: Waveforms in fault tolerant operation scenario I with S_2 open-circuit fault in SM_{u2}: (a) current and voltage waveforms; (b) fault detection results for the six sub-modules.

for both the normal and fault tolerant operations. The average capacitor voltages remains as 80 V, and higher voltage ripples across the capacitors in the upper arm could be evidently observed. The fundamental component of the differential current, which is introduced by the asymmetrical capacitor voltage ripples, is negligible owing to the paralleled resonant controller for i_{diff} regulation.

The waveforms of the MMC with S_2 open-circuit fault in SM_{u2} are shown in Figure 7.12, where the switch open-circuit fault occurs at t1 = 0 s. The fault is correctly identified at t2 = 2.3 ms and the fault tolerant operation starts at t3 = 3.6 ms. Other waveforms of the MMC are similar with those in Figure 7.11, which confirms the effectiveness of the fault diagnosis and fault tolerant control in Scenario I when there is a single device open-circuit fault in the MMC.



(a)



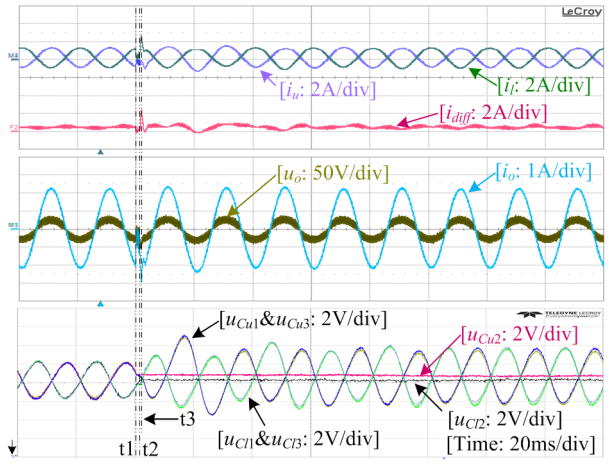
(b)

Figure 7.13: Waveforms in fault tolerant operation scenario II with S_1 open-circuit fault in SM_{u2}: (a) current and voltage waveforms; (b) fault detection results for the six sub-modules.

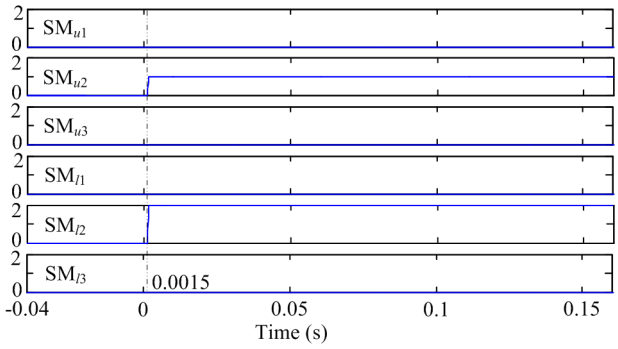
Fault tolerant operation scenario II: In this scenario, $N = 2$, $N_r = 1$, and $N_f = 1$ are selected and the maximum output voltage of the MMC is 80 V according to the discussion in Subsection 7.3.3. The output current of the MMC is regulated as 4 A so that the amplitude of the MMC output voltage is 64 V. The average capacitor voltage of the sub-modules in the entire phase leg is initially set as 80 V, and then the capacitor voltage reference for the sub-modules in the upper arm increases to 115 V after the faulty sub-module in that arm has been bypassed.

The waveforms of the MMC in fault tolerant operation scenario II when S_1 open-circuit fault in SM_{u2} occurs at t1 = 0 s are depicted in Figure 7.13. The open-circuit fault is identified at 3.5 ms and the fault tolerant control takes effect

at t2 = 4.8 ms. After that, the capacitor voltage reference for the sub-modules in the upper arm starts to increase to 115 V with a slope of 100 V/s to clearly show the process. u_{Cu1} and u_{Cu3} try to follow their references as shown in Figure 7.13 (a). It is obvious that the arm currents, differential current, and capacitor voltages in the upper arm are distorted until t3 = 126.5 ms at which the capacitor voltages are higher than 92 V so that the output voltage 64 V can be generated as normal according to (7.9). A fundamental frequency component, which contributes to increasing the capacitor voltages in the upper arm [71], can be found in the differential current from t3 to t4 = 428.8 ms. Consequently, the capacitors of remaining sub-modules in the upper arm are charged to 115 V. After t4, the MMC operates at a new steady state in the fault tolerant operation scenario II.



(a)



(b)

Figure 7.14: Waveforms of the MMC with S_1 open-circuit fault in SM_{u2} and S_2 open-circuit fault in SM_{l2}: (a) current and voltage waveforms; (b) fault detection results for the six sub-modules.

The capacitor voltage ripples in the two arms are almost the same, which coincides with the analysis in Subsection 7.3.3.

7.4.3 Multiple switches open-circuit

In this set of experiments, the performance of the fault diagnosis and fault tolerant control has been investigated while multiple switch open-circuit faults simultaneously occurs. The output current of the MMC is regulated as 2.3 A and the capacitor voltages are maintained as 80 V. Figure 7.14 demonstrates the waveforms of the MMC during fault identification and system reconfiguration, while simultaneous open-circuit faults occur at S_1 in SM_{u2} and S_2 in SM_{l2}. The faults are given to these two switches simultaneously at t1 = 0 s and are identified around t2 = 1.5 ms. All the remaining sub-modules in the upper and lower arms are reconfigured at t3 = 2.6 ms, and the MMC then operates under the fault tolerant control scenario I. The waveforms of the MMC are scarcely affected even two sub-modules have been bypassed, except for the higher voltage ripples across the capacitors of remaining sub-modules in both arms.

7.5 Summary

This chapter presents a seamless fault tolerant control for MMCs with distributed control architecture and hot reserved redundant sub-modules, in order to improve the system reliability.

The characteristics analysis of a half-bridge sub-module with open-circuit fault in different switching devices is performed in Section 7.2. Based on the characteristics, it is concluded that the switching device open-circuit faults in the half-bridge sub-module can be identified according to the sub-module terminal voltage, the arm current, and corresponding gating signals. Accordingly, a fault diagnosis is developed and fully implemented in the local controllers of sub-modules without adding additional hardware circuit or sensors. Single and multiple open-circuit faults can be accurately detected and identified within 3.5 ms, and the diagnosis method is also immune to the noises and disturbances in the system. The fast switching device open-circuit fault diagnosis guarantees that the faulty device can be identified before component catastrophic damage due to over-voltage.

The identified faulty sub-modules are normally bypassed from the MMC system. The MMC performance with asymmetrical are investigated in Section 7.3

in terms of output voltage, phase voltage, circulating current, and switching harmonics in arm currents. In order to achieve the same system output, internal dynamics, and switching harmonics cancellation as in the normal operation, a fault tolerant control is designed in two scenarios, according to the number of faulty sub-modules in the system. The MMC fault tolerant operation can be achieved by properly adjusting the period and phase registers of the PWM modules and the capacitor voltages. The distributed control loops of the MMC developed in Chapter 6 are barely influenced by the fault tolerant operation.

The effectiveness of the fault diagnosis and the fault tolerant control are experimentally confirmed in different scenarios in Section 7.4. Seamless operation of the MMC system under switch open-circuit faults is achieved, and good agreement is attained between theoretical analysis and experimental results. The entire process of fault diagnosis and system reconfiguration for fault tolerant operation can be completed in about 5ms after the occurrence of switch open-circuit faults, making the operation transition seamless and reliable. The MMC can ride through device open-circuit faults before severe malfunction or catastrophic damages occur in the system.

Chapter 8

Conclusions and Future Works

8.1 Conclusions

The promising multilevel topology Modular Multilevel Converter (MMC) has been proposed for more than one decade and attracting considerable research interests. With the advantages like perfect output waveform, modularized structure, flexible scalability, transformer-less configuration, and high reliability, the MMC can be conveniently used in industrial applications with high- or medium-voltage levels. Although the hardware configuration of an MMC is relatively simple compared with other multilevel converters, the difficulty of designing an MMC system actually lies in the control strategies. Multiple control objectives, such as MMC output and internal dynamics, have to be simultaneously met for the stable operation of the MMC, which makes the implementation of the control system complex and hard to be accomplished in a single controller. In consequence, this thesis aims to investigate the control strategies for MMCs.

The thesis starts from the basic principles of a three-phase MMC, including the configuration of sub-modules, arms, and phase legs, as well as the operational principles of the MMC, as presented in Chapter 2. Critical design criteria for main circuit components selection are summarized as well.

The steady state analysis of a general MMC which can be used as either an AC/AC converter or a DC/AC inverter, including sub-module capacitor voltages, output and phase voltages, and harmonics in the inner differential current, has been detailed in Chapter 3. In addition to better understanding of the MMC operation, the analysis also suggests the conditions that ensure the stable operation of the MMC system. Equivalent circuits of the MMC are given based on

the steady state analysis. The control tasks, normally used control strategies, and modulation techniques for the MMC are introduced in Chapter 3 as well.

In order to reduce the power losses introduced by the harmonics in the differential current in phase legs, an even-harmonic repetitive control scheme for circulating current suppression has been discussed in Chapter 4. The characteristics of the circulating current have been analyzed and the even-harmonic repetitive control is designed based on those characteristics. For better overall control system stability, an explicit and analytical design method for the phase-lead filter in repetitive controllers is presented. The even-harmonic repetitive control excellently suppresses the even-order harmonics in the differential current, with advantages over the conventional repetitive control including halved number of error sampling periods, less chip memory occupation, shorter controller delay period, faster convergence speed, higher low-frequency gain, higher crossover frequency, and wider control bandwidth at desired frequencies. The simulation and experimental results confirm the improved performance of the even-harmonic repetitive control.

According to the state-function model presented in Chapter 5, an MMC is a multi-input-multi-output nonlinear system with coupled state variables and system inputs. A nonlinear system control strategy could be a straightforward and effective solution for the control problem of the MMC system. The differential geometry based feedback linearization technique is adopted in Chapter 5 for the output and differential currents regulation. By applying the feedback linearization technique to the nonlinear MMC system, the two current control loops are linearized and decoupled as two simple integrators. Therefore, the controllers for these two current loops can be easily designed according to classic linear control laws. It is concluded that the feedback linearization based current control for the MMC can facilitate the controller design and parameters selection compared to conventional cascaded control strategies. The feedback linearization control also shows better steady state performance and dynamic responses.

The control strategies discussed in Chapter 4 and Chapter 5 are implemented in a centralized manner, which might reduce the modularity and expandability of an MMC system with a large number of sub-modules in each arm. A centralized control architecture is not practical in those applications. In order to address this issue, a distributed control strategy is discussed in Chapter 6. By properly allocating the control tasks into the central and local controllers and elaborately designing the control loops for sub-module capacitor voltage governing, the dis-

tributed control strategy is achieved with minimum data exchanging for real-time control. The data exchanging of the system is no longer proportional to the number of sub-modules in each arm, which significantly reduces the complexity of the control system design. The experimental results show that all the control objectives in conventional MMC control strategies are guaranteed by the distributed control strategy. The overall system operates stably in steady state and during step changes.

To improve the reliability of the overall MMC system, the fault diagnosis and fault tolerant control with hot-reserved redundant sub-modules are embedded into the distributed control system in Chapter 7. A real-time measurement based switching device open-circuit fault diagnosis is implemented in local controllers. The sub-module voltage, arm current, and the corresponding gating signals are used in the fault diagnosis, which is able to identify multiple switching device open-circuit faults within a short period. After the fault diagnosis, a fault tolerant control for MMCs with bypassed faulty sub-modules is designed, so that the same system output, internal dynamics, and switching harmonics cancellation as in the normal operation can be achieved. The experimental results show that the switching device open-circuit faults can be identified in 3.5 ms after the fault occurrence without any false alarm. The entire process of fault diagnosis and system reconfiguration for fault tolerant operation can be completed within 5 ms. Therefore, it is concluded that the MMC is capable of seamlessly riding through switching device open-circuit faults before severe malfunction or catastrophic damages occur in the system.

In all, this thesis provides four control strategies for MMC systems to address the issues related to control performance, efficiency, nonlinearity, modularity, and reliability. All control strategies provide high performances in the MMC system in steady state and during step changes. The effectiveness and improvements of these control strategies have been experimentally confirmed with favorable results.

8.2 Future works

This thesis has to some extent provided sizable materials on the development of control strategies for MMCs. Nevertheless, there are other challenges yet to be solved and improvements can be made to current solutions. Some of them are briefly discussed in this section for future investigations.

The input-output feedback linearization based current control has been dis-

cussed in Chapter 5, where the performance of current controls is improved. However, the capacitor voltages u_{Cu} and u_{Cl} are not included in the feedback linearization control. Since the stability of the overall system also depends on the zero dynamics, the designed feedback linearization current control is not able to sufficiently guarantee the overall system stability, and external controllers for the capacitor voltages are required. A nonlinear control strategy being able to manage all system state variables might be of interest for investigation. The input-state feedback linearization technique based nonlinear control for MMCs, which transfers the nonlinearities between the system inputs and states to linear ones, could be investigated and developed. Such input-state feedback linearization control takes all state variables into the account when designing the control system for the MMC. It should be able to guarantee the control performance of the currents and capacitor voltages, and the system stability as well.

The distributed control strategy has been originally discussed in Chapter 6. Its performance and stability are verified in experiments. However, the stability analysis of the distributed control MMC system is not as straightforward as that in a centralized control system, since the control tasks are implemented in different controllers and interact through a communication network. There are some issues need to be further investigated.

- As long as the data exchanging for real-time control is necessary among different controllers in the distributed control strategy, the delay caused by the communication network should be taken into account while investigating the stability of the overall system. Special cases, such as the delays caused by the communication network blocking because of the high occupation rate of the network, could also be worth to investigate. The communication delays should be modeled and quantified in order to mathematically analyze the system stability. The lack of time-delay model, analysis, and corresponding stability criterion for MMCs on the other hand, also makes difficulties in investigating the time-delay impacts as well as the assessment for system stability margin. MMC models with the consideration of communication delays, such as Padé-approximated based models, can be developed for better stability analysis for the MMC.

- The control conflicts for capacitor voltage control loops among sub-modules in the MMC distributed control system is briefly discussed in Chapter 6. Such or similar control conflicts among controllers in an MMC might make

difficulties in system stability analysis. The control system analysis techniques considering the control conflicts among different controllers could be studied.

- In high power applications, the switching frequency of the semiconductors in an MMC with a large number of sub-modules could be as low as around 100 Hz, in order to minimize the switching losses with acceptable control performance. It is important to select the switching frequency of MMCs with the consideration of system efficiency and stability at the very beginning because it greatly affected the communication network design, control bandwidth, digital control system delays, control performance, and thermal management. Therefore, the power loss estimation and the effectiveness and stability of the distributed control strategy under different switching frequencies should also be investigated.

Although it seems obvious that the reliability of MMCs can be improved with the help of redundant sub-modules, fault diagnosis algorithm, and fault tolerant control as presented in Chapter 7, it is actually difficult to quantify the corresponding reliability improvement brought. Without the quantified reliability, it is hard to evaluate different redundant designs and find a balance between the number of redundant sub-modules and the system cost or complexity, since it is not possible to infinitely add redundant components into a system. The number of redundant sub-modules should be selected to fulfill the expected system reliability or lifetime with the lowest cost. The quantified reliability also makes the comparison of different redundant designs (e.g. cold or hot reserved sub-modules) or fault tolerant operation strategies available in terms of reliability improvement. Hence, reliability assessment models for MMCs and the cost of reliability are expected to describe the cost-effectiveness of redundant designs and fault tolerant control strategies.

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