An In-Pixel Gain Amplifier Based Event-Driven Physical Unclonable Function for CMOS Dynamic Vision Sensors

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***Abstract*—In this paper, a novel in-pixel event-driven physical unclonable function (PUF) is presented for the rapidly developed CMOS dynamic vision sensor (DVS). Different from traditional widely reported PUF implementations with additional dedicated silicon area, power consumption and peripheral circuitries, the proposed implementation extracts PUF based on the original gain amplifier existing in the mainstream DVS pixel, which is necessary to amplify the front-end logarithmic photoreceptor's relatively weak output signal, according to the ratio of the in-pixel capacitor pair. With any ON/OFF event generated and the corresponding DVS pixel fired asynchronously, the DVS pixel's own gain amplifier will be reset in order to capture the next possible event. Due to the inevitable variation of the semiconductor fabrication process, the reset voltages of different DVS pixels' gain amplifiers are slightly different. A bidirectional counter based analog-to-digital converter is customized to digitize the successively fired pixel pair with the sign bit representing the PUF bit (i.e. the reset voltages' difference). Moreover, the proposed implementation is validated using a standard 0.18μm CMOS process in *Cadence*. According to the extensive post-layout simulation results, the uniqueness is calculated to be 49.97%. With the operating temperature varying from -40°C to 120°C and supply voltage varying from 1.7V to 2.1V, the worst-case reliability is reported to be 96.48% and 97.27%, respectively. Meanwhile, its superior randomness is also verified using the NIST test suite.**

I. Introduction

Recent years have witnessed the fast development of CMOS dynamic vision sensor (DVS), which is capable of sensing the target images continuously without the concept of "frame" in traditional CMOS image sensors [1]. As a result, it has shown great promise for a wide range of high-speed machine vision applications, including autonomous driving, reactive surveillance, object tracking, to name a few [2]–[6]. With the explosive increase in the number of image sensing devices for the IoT applications, security related issues have become more and more critical [7]. Traditional software based encryption/decryption algorithms can provide relatively safe communication channels among different image sensing devices. However, for the front-end sensor nodes, they are always assumed to be safe even under the most advanced communication protocols. It is known that without reliable authentication of the image sensing devices, the recorded image or video can be easily tampered with a lot of image processing algorithms, which has been reported in quite a few virtual camera fraud cases [8].

With the development of emerging hardware security technologies, physical unclonable function (PUF) has become a new on-chip security primitive featuring compactness and low power consumption. It can provide an ID for individual sensing chip based on the inevitable variations of the semiconductor fabrication process, which is unique from chip to chip even for dies of the same layout design in the same wafer or same manufacturing lot. A number of PUF implementations have been demonstrated in the previous literatures [9]–[15]. Most of them can be directly replicated on different chips including the image sensor chips, at the expense of additional dedicated silicon area, power consumption and peripheral circuitries. In order to further reduce PUF's design overhead and fully exploit the existing circuit modules of the mainstream CMOS image sensing systems, Cao *et al* present the first pixelated PUF design based on the dark signal non-uniformity (DSNU) of fixed pattern noise (FPN) in traditional CMOS image sensors [16]. It is worthy to mention that this solution can easily extract the PUF with the existing circuitry in the CMOS image sensor's pixel, which completely remove the need of additional silicon area and power consumption for the dedicated PUF design. Moreover, the first event-driven PUF is proposed in [17] using DVS where the random response bits are not only dependent on the device but also the addressed events. The PUF response is generated from a row of pixels through an externally accessible reset switch upon triggered by an address event without stopping address events from being produced by the asynchronous reset of pixels from all other rows.

In this paper, a different in-pixel event-driven PUF design is proposed based on the DVS pixel's gain amplifier, which is an indispensable circuit module for amplifying the very front-end logarithmic photoreceptor's weak output signal. It is known that the DVS pixel's gain amplifier will be pulled back to an initial voltage level, when the pixel encounters a large intensity change (also known as the fired pixel) [1]. Due to the inevitable variations of the semiconductor fabrication process, this gain amplifier's initial voltage level varies from pixel to pixel. This motivates us to read-out this initial voltage immediately after resetting the event-driven DVS pixel, then

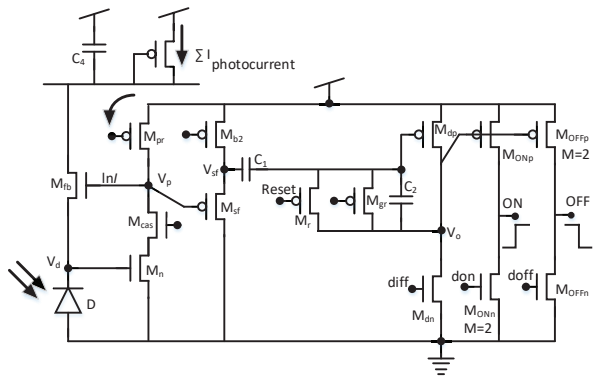

Fig. 1: Pixel structure of the mainstream CMOS dynamic vision sensors [1].

digitizes it with a dedicated bidirectional counter based analog-to-digital conversion (ADC) scheme. With another DVS pixel fired asynchronously, we can have another initial voltage level of the latter DVS pixel's gain amplifier, which is fed to the same ADC circuitry for comparison. Finally, the sign bit of the bidirectional counter, which depends on the initial voltage difference of the pixel pair, is just the generated PUF bit with superior randomness. The rest of this paper is organized as follows. Section II describes the pixel structure of the mainstream DVS system. Section III presents the VLSI implementation of the proposed gain amplifier based in-pixel event-driven PUF. The extensive post-layout simulation results are reported and discussed in Section IV. Finally this paper is concluded by Section V.

II. Pixel Structure of the Mainstream DVS

The mainstream DVS pixel structure is presented in Fig. 1 [1]. The photocurrent is dominated by the saturated NMOS transistor M_{fb}. The pre-amplifier consisting of transistors (M_{pr}, M_{cas}, M_n) is connected as shown in Fig. 1. As a result, the output voltage V_p is proportional to the photocurrent's logarithm. With a source follower (M_{b2} and M_{sf}) isolating the real-time fast transient photosensitive signal from the following stage, the transistors M_{dp} and M_{dn} together with the capacitors C_1 and C_2 form the gain amplifier. When the reset switch is turned on, the input and output of the gain amplifier are shorted together, then we can have the corresponding output V_o denoted as the initial voltage level. When the reset switch is turned off, V_{sf} is amplified to V_0 according to the ratio of C_1 and C_2, and an ON/OFF event is triggered when V_o exceeds the ON/OFF threshold. After the generated event is addressed, the reset transistor M_r will be reactivated to pull the gain amplifier's output voltage V_o back to the initial level. M_{gr} is an additional reset switch that allows external access to initialize selected pixels.

III. Proposed In-Pixel Gain Amplifier Based Event-Driven PUF Implementation

As shown in Fig. 2, transistors M_{dp} and M_{dn} form a common source amplifier that operates at the saturation region. The drain current can be calculated as follows:

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2 \tag{1}$$

where μ, C_{ox}, $\frac{W}{L}$, V_{gs}, V_{th} are the charge carrier mobility, gate oxide capacitance, width to length ratio, gate-source voltage and threshold voltage, respectively. The drain currents flowing through M_{dp} and M_{dn} are same. The gain of the amplifier composed of M_{dp} and M_{dn} can be calculated as follows:

$$A_v = -g_{m,dp}(r_{o,dp}||r_{o,dn}) \tag{2}$$

$$g_{m,dp} = \mu_p C_{ox}(\frac{W}{L})_{dp}(V_{gs,dp} - V_{th,dp}) \tag{3}$$

where $g_{m,dp}$ is the transconductance of M_{dp} and $(r_{o,dp}||r_{o,dn})$ is the output impedance observed at the output node V_o. Then we can have V_o equal to:

$$\frac{\Delta V_o}{\Delta V_{sf}} = -\frac{C_1}{C_2 + \frac{1}{A_v}(C_2 + C_1 + C_{in})} \tag{4}$$

$$\Delta V_o \approx -\frac{C_1}{C_2}(1 - \frac{C_2 + C_1 + C_{in}}{C_2}\frac{1}{A_v})\Delta V_{sf} \tag{5}$$

where C_{in} is the parasitic capacitance of the gain amplifier. It can be observed from the above equations that V_o will be affected by the specific value of A_v even if V_{sf} is the same for all pixels. Meanwhile, the drain currents of M_{dp} and M_{dn} can affect the transconductance $g_{m,dp}$, which in turn change the amplifier's gain A_v and will further affect the value of V_o.

Ideally, without considering the semiconductor fabrication process variation, V_o of each DVS pixel should be the same. However, due to the inevitable process variation, V_o is slightly different from pixel to pixel, which can be exploited to generate a large number of PUF bits with the inherent large number of DVS pixels. In addition, the reset and readout of V_o can be completely driven by external events, which is converted to time domain through the off-pixel ADC having transistor M_{bias} and capacitor C_S. By charging C_S to V_{dd} first then discharging it using M_{bias}, the needed time is proportional to V_o. Then an off-pixel bidirectional counter is shared by the whole pixel array to count the aforesaid discharging time with predetermined period. Specifically, if we have the sequence of the asynchronously fired pixels, we can divide them into a large number of pixel pairs by treating every two successively fired pixels as one pair. In real DVS applications, every pixel pair will be generated sequentially in real time. After the firstly fired pixel's location and time stamp reported to the addressing circuitry, its V_o will be pulled back to the initial level and fed to the above-mentioned off-pixel time-domain ADC. In one pixel pair, the first pixel's V_o is digitized by an up-counter and the second pixel's V_o is digitized by a down-counter over the same counting period. This can be achieved with a bidirectional counter so that the residue stored in the bidirectional counter

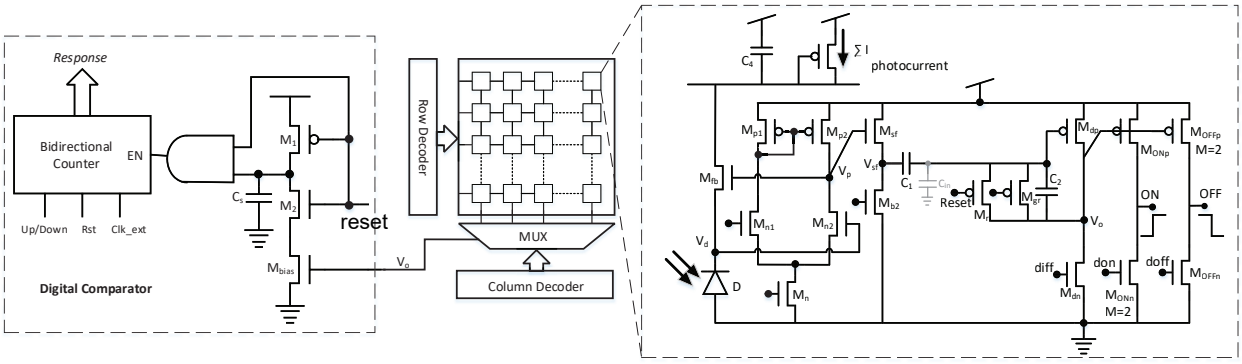

Fig. 2: Block diagram of the proposed in-pixel gain amplifier based PUF for CMOS dynamic vision sensors.

represents the quantized difference of the two pixels' reset voltages, and the sign bit can be used as a PUF bit. As the sequence of the fired pixels is completely determined by the external events, if we can generate the PUF bit stream together with the output DVS image/video, it can be used as a unique authentication of the corresponding image/video.

Furthermore, the generated PUF bits can also be well-optimized based on the aforesaid quantized difference of the pixel pair's reset voltages, which is proportional to the PUF's reliability under various environmental factors. Generally speaking, the larger the quantized difference, the more reliable is the corresponding PUF bit. The generated PUF bit's reliability can be greatly improved by simple thresholding. In order to enable the full access and evaluation of all the DVS pixels, normal binary row/column decoder is adopted to asynchronously and randomly address the whole pixel array. The PUF generated by this method can provide an ID for the device. In real-life applications, the sequence of fired pixels will be completely determined by the external events. The PUF generated by this method can be used as the sequence number of the event recorded by the device, which will be captured using the address encoder and the handshake/arbiter logic.

IV. Simulation Results

The proposed in-pixel PUF design is implemented using a 0.18μm standard CMOS process. Figure 3 presents the overall layout of the in-pixel PUF based DVS and the layout of the single DVS pixel with our proposed PUF. The process variation is introduced by adopting *Monte Carlo* simulation. Then the proposed PUF's performance is evaluated by three most important figures of merit: uniqueness, reliability and randomness.

A. Uniqueness

Uniqueness measures how different the responses of different chips are, with the same input challenge. It is usually evaluated by calculating the inter-die Hamming distance (HD).

$$U = \frac{2}{m(m-1)} \sum_{u=1}^{m-1} \sum_{v=u+1}^{m} \frac{HD(R_u, R_v)}{n} \times 100\% \qquad (6)$$

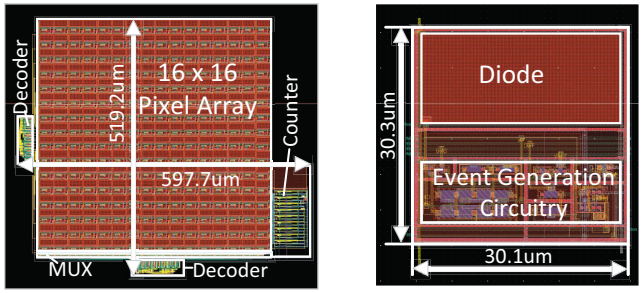

Fig. 3: (a) Overall layout of the proposed in-pixel PUF based DVS design; (b) Layout of the single DVS pixel with gain-amplifier based event-driven PUF.

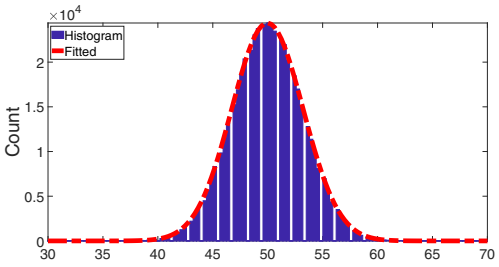

Fig. 4: Distribution of the inter-die Hamming distance (%).

where R_u and R_v are the n-bit responses generated with the same challenge applied to different PUF chips u and v, respectively, m is the total number of PUF instances.

We generated 1000 PUF instances by *Monte Carlo* simulations under standard supply voltage and operating temperature of 1.8V and 27°C. Figure 4 illustrates the distribution of the inter-die Hamming distance. With each PUF instance having 256 response bits, the proposed PUF's uniqueness is calculated to be 49.97%.

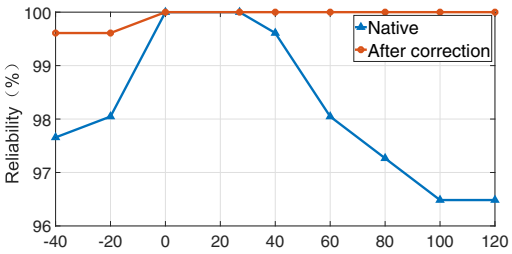

Fig. 5: The calculated reliability with the operating temperature ranging from -40°C to 120°C (the supply voltage is maintained to be 1.8V).

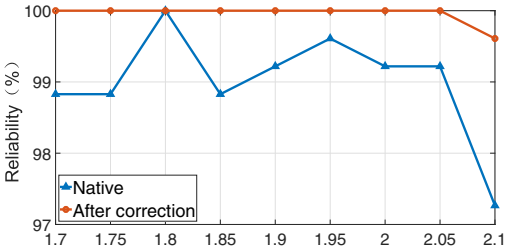

Fig. 6: The calculated reliability with the supply voltage ranging from 1.7V to 2.1V, (the operating temperature is maintained to be 27°C).

B. Reliability

The reliability of a PUF instance measures the consistency of its various CRPs under different operating conditions. The PUF responses generated under non-standard supply voltage or temperature conditions are compared with the response generated under standard voltage and temperature. The reliability of the different responses is evaluated by comparing the intra-die Hamming distance (HD) of the different responses:

$$R = 1 - BER = 1 - \frac{1}{k}\sum_{j=1}^{k}\frac{HD(R_i, R_{i,j})}{n} \times 100\% \quad (7)$$

where BER is the acronym of bit error rate.

Specifically, 1000 256-bit response examples were collected at the standard supply voltage of 1.8V and room temperature of 27°C. The temperature is then changed while the supply voltage is maintained to be 1.8V. As shown in Fig. 5, the worst-case temperature reliability from -40°C to 120°C is observed to be 96.48%. After the thresholding based correction, the worst-case reliability over the same temperature range is increased to 99.61%. Additionally, according to Fig. 6, it is observed that the worst-case reliability under the supply voltage ranging from 1.7V to 2.1V is reported to be 97.27%. After the thresholding based correction, the worst-case reliability over the same supply voltage range is increased to 99.61%.

TABLE I: NIST test results.

STATISTICAL TEST	P VAL	PROP	RESULT
Frequency	0.534146	10/10	Pass
Block Frequency	0.534146	10/10	Pass
Cumulative Sums(forward)	0.350485	10/10	Pass
Cumulative Sums(backward)	0.213309	10/10	Pass
Runs	0.350485	10/10	Pass
Longest Run	0.350485	9/10	Pass
Rank	0.350485	10/10	Pass
Overlapping Template	0.066882	10/10	Pass
Approximate Entropy	0.911413	10/10	Pass
Serial(forward)	0.911413	10/10	Pass
Serial(backward)	0.350485	10/10	Pass
Liner Complexity	0.911413	10/10	Pass

C. Randomness

The randomness of the proposed PUF was evaluated by the NIST test suite [18]. The test data is generated from 10 PUF instances with 10,000 response bits. Due to the limited size of the bit stream, some tests cannot be performed. However, it is worth mentioning that the P values of the listed items in Table I are all greater than 0.01, which validates their excellent randomness.

V. Conclusion

We demonstrate an in-pixel PUF for the rapidly developed CMOS DVS, which is based on the DVS pixel's existing gain amplifier and can be driven by external events. The proposed PUF implementation is completely merged with the gain amplifier circuitry based DVS pixel, which removes the need of additional circuitries dedicated to the PUF design. In addition, the output voltages of the successively fired pixel pair are asynchronously reset to the initial voltage level. Due to the inevitable CMOS process variation, the two slightly different initial voltages are converted to time domain first then digitized using a customized bidirectional counter. With the reverse counting directions for the two reset voltages, the sign and the residue of the counter represent the generated PUF bit and its magnitude. Furthermore, the proposed PUF implementation is validated by our reported extensive post-layout simulation results. The worst-case native reliability is reported to be 96.48% and 97.27% for a wide temperature range of -40°C$\sim$120°C and supply voltage range of 1.7V$\sim$2.1V, respectively. This in-pixel event-driven PUF design can provide a low-cost and low-power solution for authenticating both the DVS devices and the captured DVS images/videos in a wide range of IoT applications.

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