Body-Bootstrapped-Buffer Circuit for CMOS Static Power Reduction

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***Abstract*—In this paper, we present a new CMOS circuit design for increasing the threshold voltages (V_T) of MOSFETS to reduce power consumption. Using a single voltage source V_{DD}, the proposed circuit generates both the high positive and negative voltages, which are connected to the body nodes of MOSFETs to increase the reverse-bias voltage between the source and body in order to raise V_T. Consequentially, static power consumption is reduced. The circuit is integrated into a 256-bit Ripple Carry Adder and a 32-bit Braun multiplier. Simulation results based on Chartered Semiconductor Manufacturing Private Limited's (CHRT) 0.25-µm, 0.18-µm and Berkeley Predictive Technology Model's (BPTM) 90-nm processes showed good trade-offs between power savings and delay.**

***Index Terms*—Static power, threshold voltage, low-power, charge pump.**

I. INTRODUCTION

The concerns for power consumption have become increasingly significant as CMOS technology scales down to the nanometer regime. Over the years, Moore's Law has effectively achieved continuous reduction in the dynamic power. However, the decrease in transistor geometries has exacerbated the static power, raising it to a level comparable to the dynamic power. As the feature sizes shrink below 0.18 µm, the dynamic power per device is expected to decrease. Hence, static power will become increasingly prominent. The ITRS projected that the static power will level out with the dynamic power as technology drops below the 65-nm feature size [1]. Besides facing the classic challenge for dynamic power reduction, it has become inevitable that circuit designers have to face new challenges in static power reduction for future CMOS circuits.

Current methodologies in static power reduction include controlling the dimensions and doping concentration of transistors, scaling the supply voltage, and using dual-V_T technique [2]. The use of dual-V_T technique is getting increasingly popular among integrated circuit designers because of its suitability for burst-mode type integrated circuits where the system is in the idle or sleep mode majority of the time and no computation is taking place [3]. Increasing V_T can achieve an exponential reduction in the subthreshold leakage current, but at the expense of transistor's operating speed. By assigning low V_T (high performance mode) to transistors on the critical paths and high V_T (low performance mode) to those on the non-critical paths, the dual-V_T technique is able to simultaneously achieve both high performance and low power, thus optimizing the power delay product (PDP) for integrated circuits [4].

In applications where generation of multiple voltages is possible, high V_T can be achieved by simply supplying different voltage levels to the body nodes of MOSFETS to raise V_T. However, it is extremely beneficial for portable systems to have the ability to generate all the required voltages from a standard voltage source within an integrated circuit [5].

This paper presents a new CMOS circuit design for raising V_T based on the charge pump approach. By using only one supply voltage, the proposed circuit is capable of generating two voltage levels, one being more positive than V_{DD} and another more negative than ground, to the body of nMOS and pMOS respectively to increase V_T. The proposed circuit has been integrated into an adder and multiplier, and evaluated via extensive NanoSim simulations. The simulation results, based on CHRT's 0.25-µm, 0.18-µm and BPTM's 90-nm processes [6], had achieved a good tradeoff between power consumption and performance.

II. BACKGROUND

Static power dissipation is mainly caused by the subthreshold leakage and gate-oxide leakage of MOSFETS when there is no switching activity. The subthreshold leakage current decreases exponentially with V_T [7]. The gate-oxide leakage is caused by the tunneling of an electron (or hole) from the bulk silicon through the gate-oxide potential barrier into the gate [8]. An equation presented by J. A. Butts and G. S. Sohi [9] shows how static power is related to V_T:

$$P_{static} = N \cdot k_{design} \cdot k_{tech} \cdot 10^{\frac{-V_T}{\beta}} \cdot V_{DD} \qquad (1)$$

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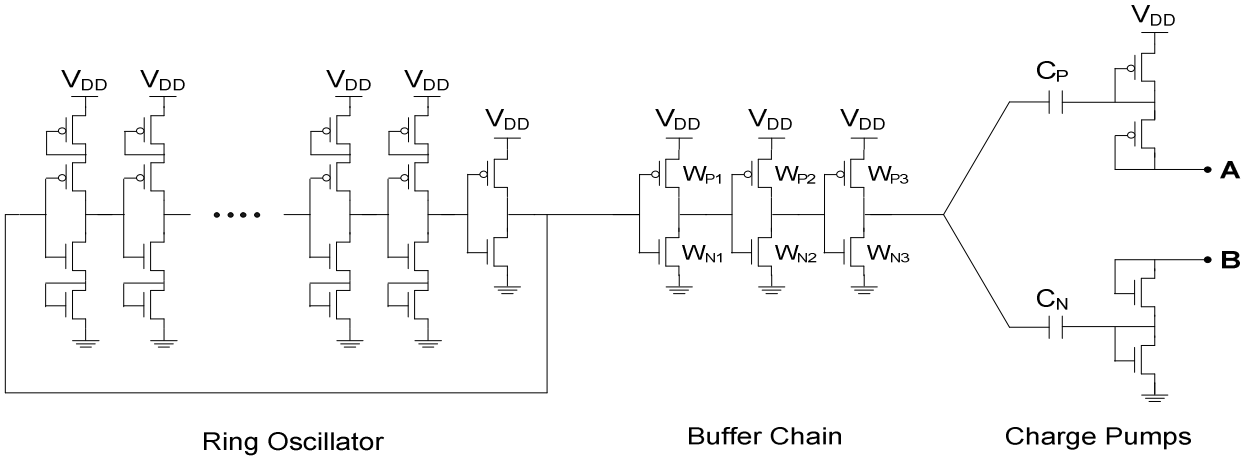

Figure 1. Schematic diagram of the B^3 circuit

where N is the total number of CMOS transistors, k_{design} is a design dependent parameter, k_{tech} and β are technology dependent parameters.

Increasing V_T is able to achieve significant static power reduction. V_T is related to the reverse-bias voltage between the source and body, $|V_{SB}|$, by the following formula [10]:

$$V_T = V_{T0} + \gamma[\sqrt{2\varphi_f + |V_{SB}|} - \sqrt{2\varphi_f}] \qquad (1)$$

where V_{T0} is the zero bias V_T for V_{SB} = 0V, φ_f is a physical parameter and γ is a fabrication-process parameter. Modification of V_T can be achieved by changing $|V_{SB}|$.

III. Proposed Body-Bootstrapped-Buffer Circuit

A new circuit design to provide the enhanced body biasing voltages necessary for raising V_T is discussed in this section. The goal is to increase V_T of MOSFETS in CMOS circuits in order to reduce the power dissipation. The strategy is to supply a voltage level that is more negative than ground to the body of nMOS and another that is more positive than V_{DD} to the body of pMOS of any CMOS circuits. The schematic design of our proposed circuit, which we named Body-Bootstrapped Buffer (B^3) circuit, is depicted in Fig. 1.

A ring oscillator with N (where N is an odd number) stages generates a clock signal for the B^3 circuit. The output of the ring oscillator is connected to three inverters with increasing aspect ratios. These inverters serve as a buffer chain to boost up the charging and discharging speed of C_P and C_N. A positive and negative charge pumps are constructed using p-channel and n-channel bootstrap circuits respectively [11, 12]. While operating at V_{DD}, the B^3 circuit generates and sustains a negative voltage level of $2V_{TN} - V_{DD}$ at node A and a positive voltage level of $2V_{DD} - 2|V_{TP}|$ at node B. Nodes A and B are connected to the body junctions of every nMOS and pMOS in CMOS circuits respectively. This increases the reverse-bias voltage between the source and body junctions of MOSFET, and consequentially raises V_T.

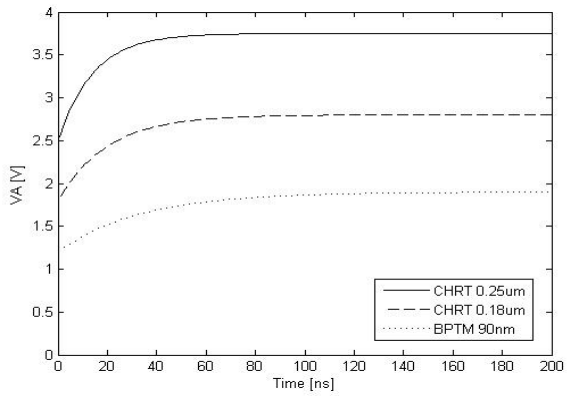

Figure 2. Simulated output voltage (node A) of B^3 circuit

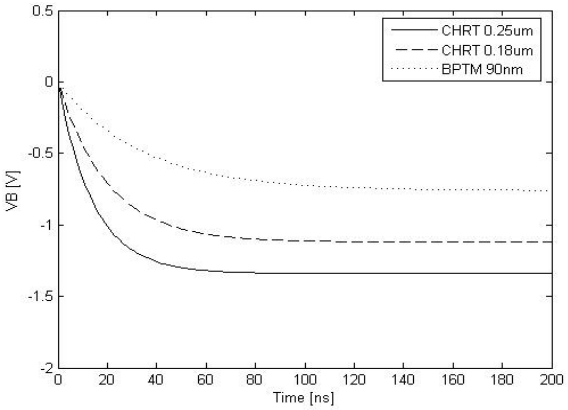

Figure 3. Simulated output voltage (node B) of B3 circuit

TABLE I. Power consumption and setup time of B3 circuit using CHRT's 0.25-micrometer, 0.18 micrometer and BPTM's 90-nanometer processes

CMOS Technology	Overhead Power Consumption (µW)	Setup Time (ns)
CHRT 0.25-µm	33.083	21.601
CHRT 0.18-µm	8.481	26.591
BPTM 90-nm	0.819	74.641

TABLE II. SIMULATION RESULTS OF A 256-BIT CLRCL-BASED RCA USING CHRT'S 0.25-MICROMETER, 0.18-MICROMETER AND BPTM'S 90-NANOMETER PROCESSES

CMOS Technology	256-bit RCA	Power (mW)	Power Saving	Time Delay (ns)	PDP (pJ)	Improvement on PDP
CHRT's 0.25-µm	Without B^3	7.649	-	42.034	321.5	-
	With B^3	5.951*	22.2%	43.099	256.5	20.2%
CHRT's 0.18-µm	Without B^3	3.941	-	35.303	139.1	-
	With B^3	3.141*	20.3%	36.708	115.3	17.1%
BPTM's 90-nm	Without B^3	2.724	-	15.061	41.0	-
	With B^3	2.003*	26.5%	17.259	34.6	15.7%

* Power consumption is inclusive of overhead for B^3 circuit.

The output waveforms of the proposed B^3 circuit for various processes are given in Fig. 2 and 3.

The power consumption overhead of the B^3 circuit is minimized by adding series-connected nMOS and pMOS to the inverters in the ring oscillator to reduce the voltage swing. The size of the ring oscillator is set to 31 inverters. The overhead power consumption and setup time of the B^3 circuit are tabulated in Table I.

IV. INTEGRATION OF B^3 INTO A 256-BIT RIPPLE CARRY ADDER

Adder is a fundamental arithmetic element of all digital computing. Reducing the power consumption of adders can significantly reduce the power consumption of computing intensive applications. In this paper, the proposed B^3 circuit is integrated into a 256-bit ripple carry adder (RCA) built by cascading a 10-transistor full adder design, Complementary and Level Restoring Carry Logic (CLRCL) full adder [13]. The schematic diagram of the CLRCL full adder is shown in Fig. 4.

The CLRCL full adder is chosen because it uses the least number of transistors in literature and yields the lowest power delay product (PDP) among all 10-transistor designs. In spite of the low gate count, the CLRCL full adder inevitably encounters the problem of threshold voltage loss at its outputs common in all other 10-transistor full adders. Both the Sum and Carry outputs suffer from one V_T loss, leading to a drastic increment in the short-circuit power dissipation for the RCA built by cascading CLRCL full adders. Construction of the RCA using small feature sizes of 18 µm and below results in high static power consumption. The resultant 256-bit CLRCL-based RCA is a good representation of future CMOS integrated circuits as the reduction in feature size and the usage of low supply voltage are expected to bring about significant raise to the short-circuit and static power dissipations respectively. It also poses as a good candidate to justify the effectiveness of the proposed B^3 circuit in terms of power savings.

A set of simulations has been performed for the 256-bit CLRCL-based RCA, without the integration of the B^3 circuit, for the purpose of comparison. The B^3 circuit is subsequently integrated into the 256-bit CLRCL-based RCA by connecting nodes A and B (as illustrated in Fig. 1) to the body nodes of every nMOS and pMOS respectively and simulated. Both sets of simulations are performed using various processes and random inputs at a frequency of 10MHz. Comparisons of the results are presented in Table II. Power savings of 22.2%, 20.3%, 26.5% and PDP improvements of 20.2%, 17.1%, 15.7% have been achieved for CHRT's 0.25-µm, 0.18-µm and BPTM's 90-nm processes respectively.

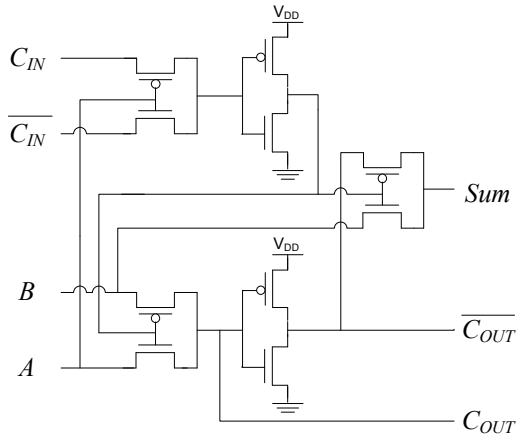

Figure 4. Schematic diagram of the CLRCL full adder

V. INTEGRATION OF B^3 INTO A 32-BIT BRAUN MULTIPLIER

In many VLSI computing intensive applications, the multiplication process constitutes a significant proportion of the overall power consumption. In general, a multiplier consumes a much greater power than an adder. Reducing the power consumption of the multiplier can effectively lower the power consumption at the device level. The proposed B^3 circuit is integrated into a 32-bit array multiplier in the same fashion as the RCA (described in Section IV). The schematic diagram of the 1-bit full adder design, N-12T [14], used in the construction of the 32-bit Braun multiplier [15], is shown in Fig. 5.

Despite the problem of accumulating V_T loss in many low-number-transistor full adder designs which may eventually leads to erroneous output logic when used in a multiplier, the 32-bit Braun multiplier built with the N-12T full adder operates correctly. Simulations are performed

TABLE III. SIMULATION RESULTS OF 32-BIT BRAUN MULTIPLIER BUILT WITH N-12T FULL ADDER USING CHRT'S 0.25-MICROMETER, 0.18-MICROMETER AND BPTM'S 90-NANOMETER PROCESSES

CMOS Technology	32-bit Braun Multiplier	Power (mW)	Power Saving (%)	Time Delay (ns)	PDP (pJ)	Improvement on PDP (%)
CHRT's 0.25-µm	Without B^3	33.691	-	65.541	2208.1	-
	With B^3	24.489*	27.3	68.993	1689.6	23.5
CHRT's 0.18-µm	Without B^3	13.273	-	54.148	718.7	-
	With B^3	9.859*	25.7	57.796	569.8	20.7
BPTM's 90-nm	Without B^3	6.842	-	21.953	150.2	-
	With B^3	4.278*	37.5	28.677	122.7	18.2

* Power consumption is inclusive of the overhead for B^3 circuit.

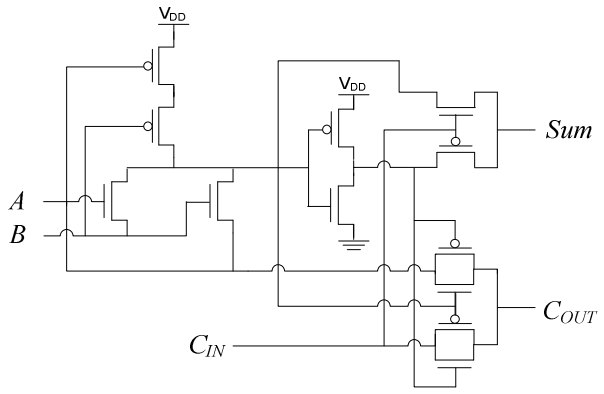

Figure 5. Schematic diagram for N-12T full adder

using random inputs with a frequency of 10 MHz. The results for various processes are tabulated in Table III. Power savings of 27.3%, 25.7%, 37.5% and PDP improvements of 23.5%, 20.7%, 18.2% have been achieved for CHRT's 0.25-µm, 0.18-µm and BPTM's 90-nm technologies respectively.

VI. CONCLUSION

In this paper, a new circuit design for reducing the static power consumption of CMOS circuits is introduced. V_T of MOSFETS is raised by increasing the reverse-bias voltage between the source and body nodes. Integration of this circuit into a 256-bit RCA and a 32-bit Braun multiplier shows a good power-delay tradeoff, with area increments of 12.6% and 3.1% respectively. Simulation results for the 256-bit RCA indicate power savings of 22.2%, 20.3%, 26.5% and improvements of 20.2%, 17.1%, 15.7% on PDP for CHRT's 0.25-µm, 0.18-µm and BPTM's 90-nm technologies respectively. For the 32-bit Braun multiplier, power savings of 27.3%, 25.7%, 37.5% and PDP improvements of 23.5%, 20.7%, 18.2% have been achieved for CHRT's 0.25-µm, 0.18-µm and BPTM's 90-nm technologies respectively. The impact of the power and area overheads introduced by the B^3 circuit can be effectively minimized by sharing it with multiple circuits or integrating it into Very Large Scale Integration (VLSI) systems.

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