STUDY OF ELECTROMIGRATION-INDUCED VOIDING MECHANISMS IN CU INTERCONNECTS

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Abstract

Electromigration has been a very active research topic ever since it was first discovered to be the failure mechanism in integrated circuit (IC) interconnects and has attracted interest of numerous researchers so far, especially due to its direct technological implications. With the advent of new Cu/low-k interconnects and aggressive technology scaling, electromigration has become a major reliability concern for IC interconnects. The subject of the present research is the study of electromigration in Cu dual-damascene interconnects. The objectives of this research are to investigate electromigration behavior of dual-damascene Cu interconnects, identify key electromigration issues and develop in-depth understanding of the electromigration-induced voiding mechanism in Cu dual-damascene interconnects.

Initial part of research work has been conducted using conventional electromigration characterization of via-fed electromigration test structures which represent the dual-damascene architecture. Experiments were performed to study the effect of structure, line-width and length. The results indicated interesting differences in electromigration behavior of via-fed upper and lower-layer dual-damascene test structures. Cu/dielectric-cap interface was found to be the preferred electromigration void nucleation site for upper as well as lower layer dual-damascene structures with the electromigration activation energies in the range of 0.6 to 0.8 eV. The electromigration mean time to failure and activation energy were found to be dependent upon the width in the lower layer test structures while it remained unaffected in the case of upper layer test structure. Similarly, short length upper and lower layer test structures exhibited completely different characteristics. The back stress effect on short lines was evident on both upper and lower layer structures, however, only the upper layer showed two distinct via and line failure mechanisms. The Short length effect was found to be complicated in dual-damascene Cu interconnects, contrary to the direct effect observed in Al and W-plug Cu interconnects. The peculiar electromigration behavior of dual-damascene interconnects could not be completely explained by current understanding of electromigration mechanisms. The observed electromigration behavior can be attributed to Cu/dielectric cap interface acting as vacancy sink and preferable nucleation site. This interface was modified by post-chemical mechanical polishing

surface treatments and its effect on electromigration performance was studied. It was found that although upper and lower layer dual-damascene structures exhibit different electromigration behavior, electromigration performance of both of these structures can be improved by Cu/dielectric interface modification.

In-situ electromigration experiments were carried out to unravel the electromigration-induced voiding mechanism in the upper and lower layer in dual-damascene Cu interconnect structures. The observations revealed electromigration-induced void movement along the Cu/dielectric cap interface. It supports the premise that Cu/ SiN_x interface acts as the dominant electromigration path. However, the observed void nucleation occurs in the Cu/SiN_x interface at locations which are far from the cathode, and void movement along the Cu/SiN_x interface in opposite direction of electron flow eventually causes void agglomeration at the via in the cathode end. The different electromigration behaviors of the upper and lower layer dual-damascene structures can be understood based on this mechanism. These findings, which are contrary to the current understanding of electromigration-induced voiding, have led to a better understanding of real electromigration mechanisms in dual-damascene Cu interconnects. Further i*n-situ* electromigration characterizations were carried out to study electromigration failure mechanism in dual-damascene Cu interconnect tree structures, which are important for reliability assessment as well as design optimizations of on-chip interconnects. Direct evidence of electromigration-induced degradation in interconnect tree structure consisting of void nucleation and void movement in opposite direction to electron flow along the Cu/SiN_x interface was unraveled. This observation is contrary to the current understanding of electromigration mechanism in interconnect tree structures. The peculiar electromigration-induced voiding in Cu interconnect tree structures can be clearly understood based on this mechanism.

Electromigration-induced voiding mechanisms revealed during *in-situ* characterizations could not be explained based on the current understanding of electromigration mechanisms. A simple model is developed, which was implemented using random atomic jumps based on the Monte-Carlo method, to understand electromigration-induced voiding observations revealed during this research work. Only two parameters were considered - electron wind force and bonding energy. The

simulation results indicate that this model can *qualitatively* explain electromigration-induced voiding observed during experimental *in-situ* characterizations as well as in various other reported studies. Differences in the electromigration mechanisms in Cu and Al interconnects and the electromigration behavior of Cu dual-damascene interconnect structures can be understood based on this model.

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List of Abbreviations

IC	Integrated circuit
RC	Resistive-Capacitive
IMD	Inter metald Dielectric
ILD	Inter level dielectric
Cu/low-k	Copper / low-dielectric constant dielectric
CMP	Chemical Mechanical Polishing
RIE	Reactive ion etching
TTF	Time to failure
MTF	Median time to failure
PDF	Probability distribution function
CDF	Cumulative distribution function
PVD	Physical vapor deposition
CVD	Chemical vapor deposition
EM	Electromigration
TDDB	Time dependent dielectric breakdown
MIS	Metal-insulator-silicon
NIST	National Institute of science and technology
USG	Undoped silicate glass
ECP	Electroplating
PECVD	Plasma enhanced chemical vapor deposition
FIB	Focused ion beam
SAM	Self Assembled monolayer

Chapter One

Introduction

1.1 Background

Electromigration has been a very active research topic ever since it was first discovered to be a critical failure mechanism in integrated circuit (IC) interconnects and has attracted interest of numerous researchers so far [1], especially due to its direct technological implications. Typical very-/ultra- large scale integration (VLSI/ULSI) circuit consists of millions of transistors. Interconnects are the "wiring" connecting these devices and are having sub-micron line-widths in current ULSI circuits. These interconnects carry very high current densities ($>10^5 A/cm^2$). Such high current density causes diffusion of metal ions in the direction of electron flow, which is known as electromigration. This causes IC failures due to formation of voids leading to open circuit and hillocks leading to shorts between adjacent interconnect lines.

In order to achieve faster, denser and more functional ICs, device dimensions are continuously shrunk by semiconductor manufacturers. This device scaling appears to obey Moore's law which states that the number of transistors in IC logic circuits is doubled every two years [2,3]. This scaling improves the performance of transistor devices by increasing the speed and reducing power dissipation, but hampers the interconnect performance due to higher Resistive-Capacitive (RC) delays. **Figure 1.1** illustrates this issue, as the technology is scaled down, interconnect delay is becoming higher than the gate delays [4,5]. Thus interconnects have become the bottle-neck for further improvement of IC performance. This is a major hurdle in continuous improvement of ICs. To address this issue, conventional Al or Al-alloy/SiO_2 interconnects are being replaced by Cu/low-*k* interconnects [6]. Cu has lower resistivity than Al leading to lowering of interconnect resistance (R) and Low-k i.e. dielectric materials having lower dielectric constant than SiO_2, lead to lowering of parasitic capacitance(C), causing overall reduction in RC delay. Along with reduction in resistance, Cu is also expected to have better electromigration reliability performance. Fabrication of copper interconnects needs "damascene" process instead of subtractive-etching process used in Al or Al-alloy interconnects

[7]. Use of Cu/low-k interconnects, apart from causing a reduction in delay, also leads to reduced cross talk, power dissipation and reduces required number of metallization levels providing significant cost advantage. Although this technology offers many advantages, there are many integration and reliability issues which need be addressed to meet the future interconnect technology needs [1,8] – electromigration is one of the most important reliability issues.

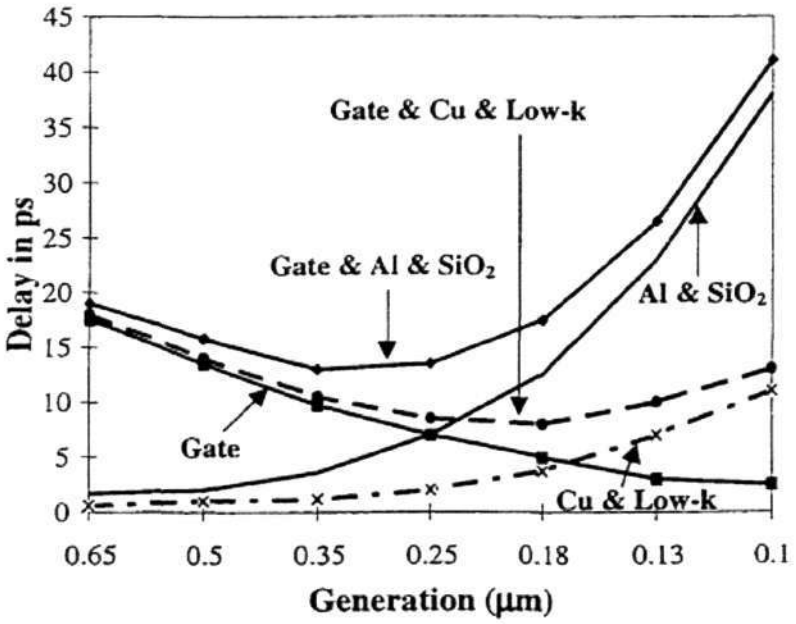


Figure 1.1: Gate and interconnect delay change with technology generation

1.2 Motivation

Electromigration failure that results in an opened and/or a short circuit is a severe reliability concern not only because it causes functional degradation but also, more importantly, causes catastrophic failure ultimately destroying the ICs. Because electromigration is one of the most important factors affecting the long term reliability of ICs, understanding the mechanism of electromigration in interconnects and finding ways to suppress such failures is of utmost importance to face the challenges in the development of future interconnect technologies.

Although considerable amount of research work has been done in past to study electromigration, the electromigration reliability scenario is significantly changing in the current and future interconnect technologies, and there are important issues that need to be addressed:-

- With the reduction of interconnect dimensions with technology generations, the current densities in interconnects are continuously increasing, for example projected worst case current density in interconnect lines in future interconnect technology (for year 2010) is $10^7 A/cm^2$! [9]. Such an extremely high current density will lead to high susceptibility for electromigration. This will be further worsened as the interface to bulk ratio will increase with miniaturization of interconnect dimensions and electromigration in Cu is dominated by interface, especially the Cu/dielectric cap interface [10].
- Al or Al-alloy interconnect is a matured process and electromigration mechanism in these interconnects is well known. Cu damascene technology is relatively new. Electromigration in Cu can be markedly different from that of Al-alloy interconnects [11]. Electromigration mechanisms in Cu and issues with damascene interconnect structures are also being studied but conflicting results are reported and electromigration mechanism in dual-damascene interconnects is not studied in depth [1]. The problem of electromigration is further perplexed by the introduction of new low-k materials having significantly different thermo-mechanical properties than conventional SiO_2 dielectric[12-20]. The fundamental electromigration-induced voiding mechanism in Cu damascene needs to be understood to address these issues.

- In-depth understanding of fundamental electromigration mechanism in Cu damascene interconnect structure needs to be developed to address the above mentioned issues. This research work has made an attempt to do so.

1.3 Objectives

- Investigate electromigration behavior of dual-damascene interconnect structures – effect of structure, width and length.
- Study of interfacial electromigration in Cu damascene interconnect structures and investigate means to improve the electromigration performance by Cu/dielectric cap interface modification.
- Development of in-depth understanding of principle electromigration-induced voiding mechanisms in Cu damascene interconnect structures by *in-situ* characterizations and Monte Carlo simulations.

Chapter two

Literature Review

2.1 Fundamentals of electromigration

2.1.1 Basic Physics of electromigration

Electromigration is a direct diffusion process of ions under an external field. The driving force for electromigration consists of the "electron wind force" ($\overrightarrow{F_{wd}}$) and the direct force ($\overrightarrow{F_d}$). The electron wind force is the effect of moment exchange between the moving electrons and the ionic atoms at the lattice position when an electric current is applied to a conductor. The direct force is due to direct electrostatic force on the moving ion. The net electromigration force ($\overrightarrow{F_{EM}}$) is given by Eq.(2.1).

$$\overrightarrow{F_{EM}} = \overrightarrow{F_{wd}} + \overrightarrow{F_d} \quad \text{.....(2.1)}$$

When the current density, which is proportional to the electron flux density, is high enough, this moment exchange becomes significant and results in a noticeable mass transport of the ions, i.e. electromigration. The ions tend to move in the direction of the applied field since they are positively ionized. The balance of these two forces determines the net movement of the ions. For simplicity, the term "electron wind force", generally refers the net effect of these two electrical forces.

Due to its dominant effect and its importance in electromigration, the driving force resulting from the application of an electric field has been the most extensively studied, both from a theoretical and experimental point of view. It is commonly accepted that this driving force is composed of two contributions. One is due to the direct action of the electrostatic field on the metal ions and the other is derived from the "wind" effect of the moving charge carriers (electrons) on the atomic motion. These effects are explained below in detail based on theoretical model developed by Huntington and Grone [21,22]. Interaction between conduction electrons carrying the electric current and the migrating ion is described by the ballistic model of scattering. It is assumed that the "wind force" on a lattice defect is given by the moment transfer by electrons per unit time as they are scattered by the defect.

During elastic scattering of electron by an ion in a defects site, the system moment is conserved resulting in average change in the electron momentum in the transport

direction equal to $2m_e\langle\upsilon\rangle$, where m_e is the electron mass and $\langle\upsilon\rangle$ is the mean velocity of the electron in the direction of the current flow.

The force on the ion because of this scattering is given by

$$\overrightarrow{F_{wd}} = \frac{2m_e \langle \upsilon \rangle}{\tau_{col}} \quad \text{.....(2.2)}$$

Where τ_{col} is the mean time interval between two successive collisions.

The net moment lost per second per unit volume electrons is then $2m_e\langle\upsilon\rangle / \tau_{col}$, and the force on a single defect ion is therefore equal to

$$\overrightarrow{F_{wd}} = \frac{2nm_e \langle \upsilon \rangle}{\tau_{col} N_d} \quad \text{.....(2.3)}$$

Where, n is the electron density and N_d is density of defects.

The electron current density can be written as

$$j = -n.q.\langle\upsilon\rangle \quad \text{.....(2.4)}$$

Substituting $\langle\upsilon\rangle$ in equation (2.3) from equation (2.4), we get

$$\overrightarrow{F_{wd}} = -\frac{2m_e j}{q\tau_{col} N_d}$$

$$= -\left[\frac{\rho_d}{N_d}\right]\left[\frac{n}{\rho}\right].q.E \quad \text{.....(2.5)}$$

where, $\rho = E/j$ is the total resistivity of a conductor, $\rho_d = m/nq^2\tau_{col}$ is the metal resistivity due to defect and E is the applied electrical field.

Aside from the electron "wind" force, the electric field E will produce a direct force on the defect ion that is given by

$$\overrightarrow{F_d} = Z^*_{el_z}.q\,.\,E. \quad \text{.....(2.6)}$$

Where, Z^*_{el} can be regarded as the nominal valance (Z) of the metal when the dynamical scattering effect around the ion is ignored. So the total force will be

$$\overrightarrow{F_{EM}} = \left[Z^*_{el} - Z\left[\frac{\rho_d}{N_d}\right]\left[\frac{N}{\rho}\right]\right].q.E \quad \text{.....(2.7)}$$

where N is the atomic density of the conductor and n= N.Z is used.

Eq. (2.7) can be written as

$$\overrightarrow{F_{EM}} = Z^*.q.E \quad \text{.....(2.8)}$$

Where,

$$Z^* = \left[Z_{el}^* - Z\left[\frac{\rho_d}{N_d}\right]\left[\frac{N}{\rho}\right] \right] \quad \text{.....(2.9)}$$

Z^* is often called the effective charge number of the ion involved in the electromigration.

Based on the Nerst-Einstien equation ($V_d/F=D/k_BT$) , the electromigration drift velocity $\vec{v}_d$, is related to the electromigration force according to

$$\vec{v}_d = D\frac{\vec{F}_{EM}}{k_B T} \quad \text{.....(2.10)}$$

Where, the atomic diffusion coefficient D is a function of temperature as follows:

$$D = D_o \exp\left(-\frac{E_a}{k_B T}\right)$$

Where, E_a is the activation energy associated with the diffusion mechanism.

Substituting $\overrightarrow{F_{EM}}$,

$$\vec{v}_d = \frac{D_o}{k_B T} q.Z^*.\rho.\exp\left(\frac{E_a}{k_B T}\right).\vec{j} \quad \text{.....(2.11)}$$

Electromigration model based on ballistic scattering of electrons is the first and most simple model of electromigration phenomenon. This and related theories were later found to be controversial [23]. Theoretical understanding is further developed by contributions of numerous researchers to date. In spite of these theoretical developments, the electromigration drift velocity expression (Eq. 2.11) developed by Huntington and Grone is still employed as theoretical basis in most of the experimental studies on electromigration.

It has also been observed that [24,25] the ionic drift ceases as the segment length becomes equal to a critical length, L_c, which decreases with increasing the current density. At L_c, the ionic flux, J_σ, due to electromigration induced stress gradient ("back-stress") is equal to the electromigration induced ionic flux, J_{EM}, such that at steady state [26],

$$J_{EM} + J_\sigma = \frac{C.D.Z^*.q.\rho.j}{k_B T} - \frac{CD}{k_B T} * \frac{\Omega \Delta \sigma}{L_c} = 0 \quad \text{.....(2.12)}$$

Where, Ω is the atomic volume, and at steady state, the stress gradient, $\left(\frac{\Delta\sigma}{L_c}\right)$ is the average gradient of the stress between the anode and cathode, a distance L_c apart. By equating the two fluxes, the critical length-current density product, jL_c, is found to be equal to,

$$jL_c = \frac{\Omega\Delta\sigma}{Z^* e\rho} \quad \text{.....(2.13)}$$

Characterization of the electromigration critical length-current density is important because sub-critical length conductors will not suffer from electromigration damage. The expression for electromigration drift velocity (Eq. 2.11) can be modified to consider this "back-stress" effect as follows.

$$\vec{v}_d = \frac{D_o}{k_B T}.\exp\left(\frac{E_a}{k_B T}\right).\left(e.Z^*.\rho.j - \frac{\Delta\sigma}{\partial x}\Omega\right) \quad \text{.....(2.14)}$$

Where, $\left(\frac{\Delta\sigma}{\partial x}\right)\Omega$ is the steady state back-stress gradient.

2.1.2 Electromigration characterization

2.1.2.1 Electromigration characterization techniques.

Various characterization techniques like low frequency noise measurement[27], ratio of resistance[28], internal friction method[29], temperature-ramp resistance analysis (TRACE) [30-31] as well as wafer-level fast tests like standard wafer-level electromigration accelerated test(SWEAT) [32], breakdown energy of metal (BEM) method [33-34] and wafer-level isothermal joule-heated electromigration test (WIJET) [35] are reported . But the most widely employed electromigration technique is the accelerated life test technique. Drift velocity method is another important technique which was invented by Blech and is very elegant method to study electromigration mass transport.

Lifetime test Method

This is an accelerated life-test. In this method, electromigration test structures are stressed at constant current density and temperature, and their resistance is monitored continuously. The lifetime of each sample i.e. time to failure (TTF) due to open circuit due to voids, or short because of hillocks is noted. In practice, failure

criteria for lifetime are often defined as a certain percentage of resistance increase. Then a cumulative failure probability can be plotted against the failure time. Statistical measurement of lifetime, i.e. median time to failure (MTF), which is the 50% point of the TTF distribution, is used. This method relies on the thermal activation of electromigration, based on Black's empirical equation [37].

$MTF = A\, j^{-n} \exp(E_a / kT)$ .....(2.15)

The electromigration parameters that can be extracted from this test are- Ea activation energy for the electromigration diffusion mechanism and exponent (n) that gives the dependence on current density. E_a is found by stressing at different temperatures keeping the current density constant and exponent (n) by stressing at different current densities keeping the temperature constant. Once the E_a and n are found, the Black's equation can be employed to extrapolate the lifetime data at accelerated life-test to operating conditions.

Drift Velocity Method

The drift velocity of the metal ions under the action of electron wind force provides a direct measure of the electromigration induced mass transport. The test structure, also called as Blech structure, used in this method is as shown in **Figure 2.1.** It consists of metal strip to be tested, deposited over a highly resistive metal strip so that the most of the current flows through the metal strip under test. The mass in the strip will therefore be transported in that direction, resulting in depletion of the metal at the cathode end and accumulation near the anode edge. **Figure 2.2** illustrates a typical result from such structure used by Blech [37]. Au strips on Mo were employed in this study. The average drift velocity is obtained by measuring the depletion at the cathode area and the time for stressing. This test can is used to determine the critical current and length product. Electromigration activation energy can also be measured. The average drift velocity is given by following equation (Eq. 2.14).

$$\vec{v}_d = \frac{D_o}{k_B T} q.Z^*.\rho.\exp\left(\frac{E_a}{k_B T}\right).\vec{j}$$

This equation can be re-written as,

$$\ln\left(\frac{v_d T}{j}\right) = \ln\left(\frac{D_o}{k_B} qZ^*\rho\right) - \frac{E_a}{k_B T}$$

Therefore, the measurement of the drift velocity at different temperature T gives the activation energy (Ea). Also, D_oZ^* product can be found if the drift velocity is measured as a function of the stress current density.

The advantages of this method are, it gives a direct measure of mass transport due to electromigration. Interference due to other factors like current crowding at width transition at line electromigration test structures, influence of via in case of via-line electromigration test structures are isolated in this test structure. Also, joule heating can be minimized by using thicker underlying metal track.

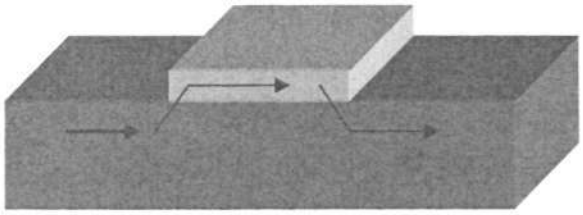


Figure 2.1: Schematic of Blech structure

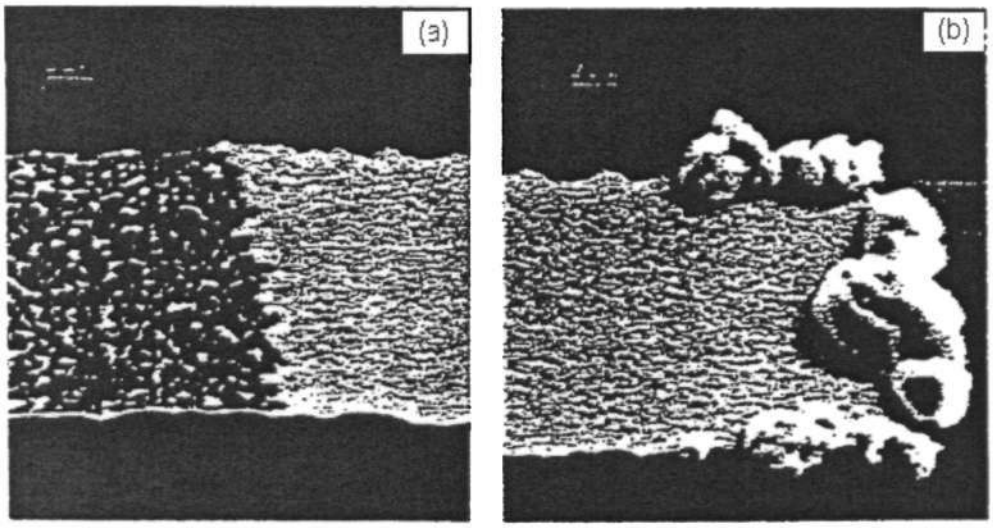


Figure 2.2: SEM micrograph of Au strips on Mo stressed at a current density of $10^6 A/cm^2$ (a) depletion at cathode end (b) accumulation at anode end [37]

2.1.2.2 Electromigration time-to-failure statistics

Generally lognormal distribution is employed for electromigration time-to-failure statistics, although a few reports have suggested other distributions [38]. The lognormal life distribution is a flexible model that can empirically fit many types of failure data. The two parameter form has parameters σ = the shape parameter and t_{50} = the median (a scale parameter). The lognormal probability distribution function (PDF), function is defined as [39-40],

$$f(t)=\frac{1}{t\sigma\sqrt{2\Pi}}\exp\left[-\frac{(\ln t-\mu)^2}{2\sigma^2}\right] \quad \text{.....(2.15)}$$

Comparing lognormal PDF with PDF of normal distribution,

$$f(t)=\frac{1}{\sigma\sqrt{2\Pi}}\exp\left[-\frac{(t-\mu)^2}{2\sigma^2}\right] \quad \text{.....(2.16)}$$

it can be said that the time to failure, t_f, has a lognormal distribution, then the (natural) logarithm of time-to-failure(TTF) has a normal distribution with mean μ = ln t_{50} (t_{50} is the median of time -to-failure of lognormal distribution) and standard deviation (σ). This makes lognormal data convenient to work with using normal distribution of logarithm of failure times. The lognormal cumulative probability (or failure) distribution function (CDF), which gives the cumulative probability of failure prior to t, is as follows.

$$F(t)=\int_0^t\frac{1}{t\sigma\sqrt{2\Pi}}\exp\left[-\frac{(\ln t-\ln t_{50})^2}{2\sigma^2}\right]dt=\phi\left(\frac{\ln t-\ln t_{50}}{\sigma}\right) \quad \text{.....(2.17)}$$

Where, ϕ (z) denotes the standard normal CDF.

If at any instant in time, a degradation process undergoes a small increase in the total amount of degradation that is proportional to the current total amount of degradation, then it is reasonable to expect the time to failure (i.e. reaching a critical amount of degradation) to follow a lognormal distribution. So, lognormal distribution is generally used in case of electromigration as well as other failure mechanisms such as corrosion, diffusion, migration and crack growth.

The TTF failure data is generally analyzed using probability ploting, which is a simple visual method for performing quick and sometimes approximate goodness-of-fit analysis and also obtaining estimates of the mean and standard deviation of the data. It can also be used to identify outliners in the data that do not appear to belong to the distribution. It consists of analyzing reliability data by plotting CDF estimates against time on specially constructed probability paper. The idea behind these probability papers is to model CDF equation and write it in such a way that a function of $F(t)$ is a linear equation of a function of t. This can be explained for lognormal plot as follows,

Lognormal CDF can be re-rewritten as

$$\ln t = \sigma\phi^{-1}\{F(t)\} + \ln t_{50} \quad \text{.....(2.18)}$$

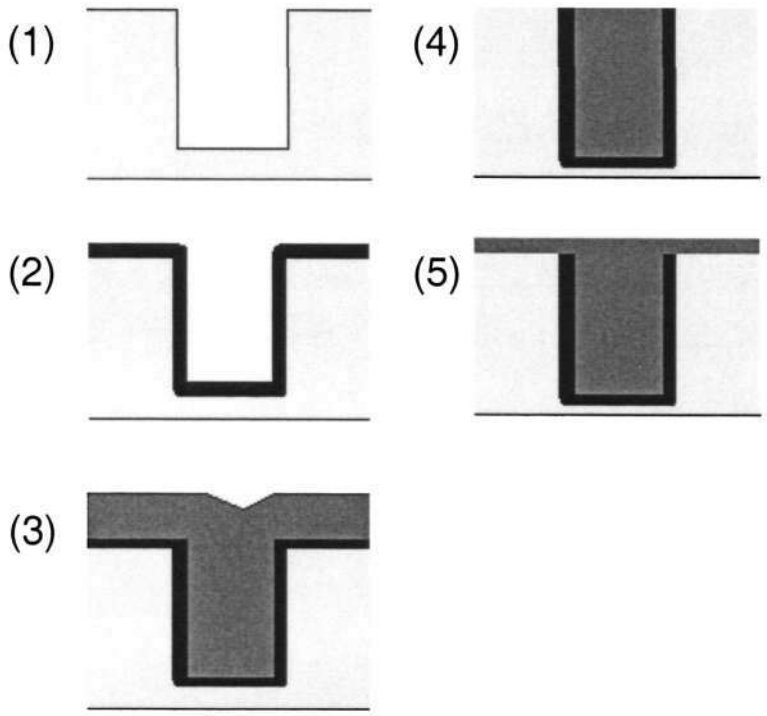
Where ϕ^{-1} denotes the inverse function for the standard normal distribution. If we let $y = t$ and $x = \phi^{-1}\{F(t)\}$, then ln y is linear in x with slope σ and intercept (when $F(t) = 0.5$) of $\ln t_{50}$. If the data are consistent with a lognormal model, the resulting plot will have points that line up roughly on a straight line with slope σ and intercept t_{50} on the y-axis.

2.2 Electromigration in Cu interconnects

2.2.1 Cu damascene interconnects

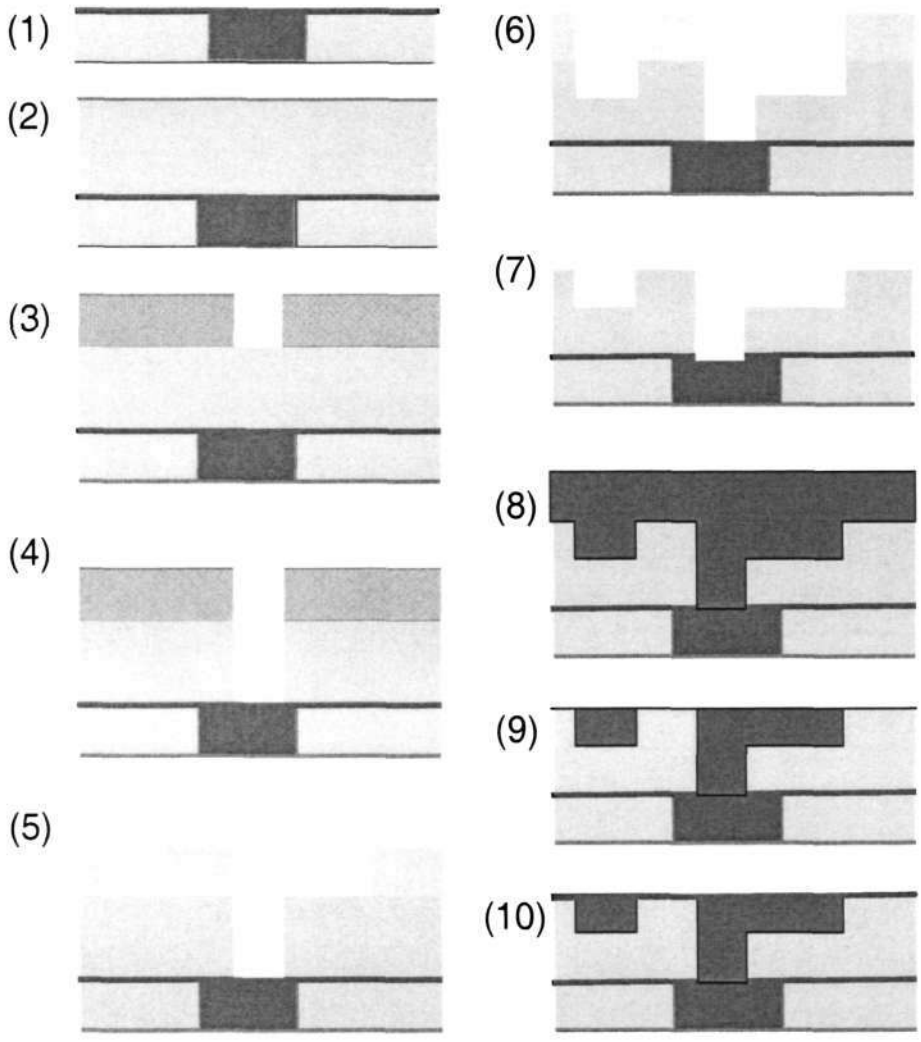
Subtractive etching or liftoff was used as the primary metal-patterning technique in the semiconductor industry for interconnect fabrication. But these techniques had limitations, including non-planarity, difficulties in etching in Cu interconnects, poor metal coverage, and residual metal shorts, which results in inconsistent manufacturability, low yield, and poor reliability and ULSI extendibility. To address these problems a new interconnect technology, called "damascene" process was developed. IBM Corp. was instrumental in the development of this technology and was first to demonstrate use of such technique for ULSI interconnect fabrication [7, 41-45]. The name, damascene, was given because of resemblance to the ancient art of damascene for fabrication of jewelry, wherein, gold is interlaced in grooves made into iron or wood to produce beautiful decorative designs. In the damascene process, interconnects are defined by metal deposition on patterned dielectric trenches and subsequent chemical-mechanical polishing (CMP)[45], as illustrated in **Figure 2.3**. Dielectric layer is deposited first and then trenches are patterned by a reactive ion etching (RIE). Diffusion barrier and Cu is deposited sequentially. Then the excess metal and barrier layers in the filled region are removed by CMP. Finally, a dielectric-cap layer is deposited. The damascene process is very promising because it not only overcomes the poor dry-etchability of Cu, but also achieves global planarization. Since multiple levels of interconnects are required in deep submicron metallization, the global planarization at each interconnect level is critical. It facilitates deep submicron lithography within a small depth-of-focus. A uniform interconnect height at each level simplifies via etching with the same depth. In the multilevel interconnect structures, successive levels of interconnects are connected by vias. The steps in conventional via-first "dual-damascene" process are shown in **Figure 2.4**. Via and interconnect shapes are patterned by reactive ion etching (RIE) by two etching steps. Then Cu deposition and CMP are performed only once. The dual damascene process is promising because it reduces the process steps and reduces overall cost. Lower resistance of Cu via is another advantage over W-plugs. The process shown here is the "via-first" dual

damascene process. "Trench-first" damascene process can also be employed. The via-first approach has been widely adopted for small geometry devices [46,47].



(1)Dielectric deposition and patterning
(2)Barrier layer deposition
(3)Cu deposition
(4) CMP
(5) Dielectric-cap deposition

Figure 2.3: Basic damascene process



(1) Planarized surface
(2) Dielectric deposition
(3) Mask-1 for via
(4) Via etch (stop on buried cap layer), subsequently photoresist strip
(5) Mask-2 for trench
(6) Trench etch, subsequently photoresist strip
(7) Burried cap layer etch
(8) Liner/Cu seed layer deposition followed by Cu electroplating
(9) Chemical mechanical polishing
(10) Dielectric cap deposition

Figure 2.4: Dual-damascene process

2.2.2 Electromigration paths in Cu interconnects

It is important to investigate which is the dominant diffusion path for electromigration in Cu interconnects to understand the electromigration mechanism. The drift due to electromigration, considering different diffusion paths in the conductor can be written as follows based on equation [1,11]

$$\vec{v}_d = .D_{eff}(T) * Z_{eff} \frac{\rho}{k_B T} \vec{j} \quad \text{.....(2.19)}$$

Contribution by different diffusion pathways to (D_{eff} Z^*_{eff}) can be expressed as follows [11].

$$(D_{eff} Z^*_{eff}) = D_B.Z^*_B.F_B + D_P.Z^*_P.F_P + D_I.Z^*_I.F_I + D_S.Z^*_S.F_S + D_{GB}.Z^*_{GB}.F_{GB}$$

$$+ D_{GB}.Z^*_{GB}.F_{GB}$$

The subscripts indicate the diffusion path as follows:

B= bulk, P= pipe, L=lattice, I= interface, S=surface, GB= grain-boundary.

F indicates fraction of atoms at the particular diffusion path. Each pathway is anticipated to have a different Z^* because the wind-force varies according to the local electronic environment surrounding a given atom. [48]. Contribution by the bulk and pipe can be considered as negligible during operating as well as reliability tests conditions (<400°C). The diffusion energies at different paths are tabulated in Table (2.1) as explained in ref [11].

Metal/alloy	Grain boundary (eV)	Interface (TiN) (eV)	Lattice (eV)	Surface (eV)
Al	0.6	?	1.4	NA
Al(Cu)	0.7	0.9-1.0	1.2	NA
Cu	1.2	0.9-1.2	2.1	0.7

Table 2.1: Activation energies for diffusion along the important mass transport paths [11].

Interesting observation is the Cu activation energy for interface may be lower than that for Al alloys. The interfacial activation energy of Cu generally appears to be less than the grain boundary activation energy, in contrast to Al (Cu). It is also important

to note that the tabulated interfacial activation energies are for interface with TiN. Activation energies for interface with dielectric-cap layer can be still lower. With the scaling of interconnect width, the Cu lines are having "bamboo" like grain structure with very few grain boundaries in the direction of electron flow and the electromigration is no longer grain boundary diffusion dominated, rather interface will govern the electromigration performance. This fundamental difference between Cu and Al(Cu) translates that the electromigration performance of Cu may not be as great as anticipated, rather it can be worse![11]. Especially with further scaling of interconnect dimensions this should be considered carefully as the interface to bulk ratio will be increased dramatically.

Many electromigration studies on Cu have indicated surface as the dominant electromigration path. An activation energy of 0.47eV was observed during a in-situ high vacuum study of electromigration in polycrystalline unpassivated Cu film [49]. This result suggested that under clean surface conditions surface diffusion is the primary damage mechanism for electromigration in copper, since the measured energy lies in the range of values obtained theoretically and experimentally for surface diffusion on copper. In another study, electromigration in Cu lines with width 0.25 to 1μ were investigated [50] with a test structure consisting of an upper and lower Ta passivation for the Cu lines. Electromigration activation energy of 0.81eV was observed. A linear relationship between failure lifetime and line-width was found, although the wide lines were polycrystalline and the narrow lines had almost "bamboo" grain structure. These observations were attributed to the fast diffusion along the sidewall surfaces of Cu lines, which were unpassivated. Theoretical model developed by L.M. Klinger et al[51] considered that grain boundary and surface mass transport co-exist. It was proposed that two different modes of damage formation can exist depending on the grain size. For small grains having large curvature, surface diffusion leads to healing of the damages (grooves) at the grain boundaries and thinning of the grains, whereas for large grains with small curvature, it cannot redistribute the material between grain boundaries and grooving results in voids. This healing effect by surface is further supported by research work done to explain unusual behavior of Cu interconnects [52]. Similarly, surface diffusion acting simultaneously along with grain boundary mass diffusion was

proposed to be critical for damage formation in reference [53]. Unpassivated Cu lines with line-widths of 0.15–10 μm were employed for study of electromigration path in Cu interconnects by C. K. Hu and co-workers [54]. For wide polycrystalline lines (line-width >1 μm), the dominant diffusion path was found to be mixture of grain boundary and surface diffusion, while in narrow lines (line-width <1 μm), the dominant path was the surface. Even some recent electromigration studies have indicated surface electromigration as the dominant mechanism [55-56]

But, the test structures employed in these electromigration studies are not similar to the damascene interconnect structure. In actual damascene interconnects there is no Cu surface available, sidewall and bottom surface of Cu is embedded in diffusion barrier like (Ta, TaN, Ti etc) and top surface is passivated by cap dielectric. Thus, these studies may not be directly relevant for electromigration in Cu damascene interconnects. Although studies on surface diffusion may not be directly relevant to EM in damascene interconnects, some of the interesting findings are dependence of surface electromigration on applied electric field [57] and nanometer scale observation of grain structure evolution due to alternating current stressing of Au films [58].

Cu/dielectric-cap interface as the dominant electromigration path.

Few studies have employed test structures which exactly resemble damascene structure. Most of these studies have indicated Cu/dielectric-cap interface as the dominant EM path [10,20-LANE,59-61]. Of particular importance is the research work by Hu and co-workers [10]. In the reference [59] damascene test structures with SiN cap were employed and Cu/dielectric cap layer was identified as the fast diffusion path. Importance of interface electromigration can be further asserted based reference [10]. In this study, electromigration in Cu damascene interconnects with varying cross sectional areas were studied. Cu/ dielectric-cap interface was assumed to be the dominant electromigration path based on previous studies [60]. The MTF was found to linearly decrease with the cross sectional area of the damascene Cu interconnects. This relationship was found to be independent of the Cu deposition processes (PVD, CVD or plating), though the values of activation energy varied considerably 0.7-0.9 to 1eV. Aggravation of electromigration with scaling of Cu damascene interconnect dimensions can be emphasized from this study.

But in this study, it is assumed that the grain structure is always a "bamboo" structure even if the cross sectional area is varied. But this should have been verified by microstructure structure analysis of Cu for lines with different cross sectional areas that were employed in the study. In case of damascene interconnects as the Cu is deposited into trenches made in dielectric, the trench cross sectional area variation can change the microstructure of deposited Cu. But as electroplating was employed in this study, the assumption is valid as it has "super-filling" capability and leads to "bamboo" grain structure in damascene trenches [63]. In another study by Arnauld and co-workers, failure modes of electromigration in Cu damascene interconnects were investigated [64]. In this study, single damascene interconnects were employed and a significant amount of interface diffusion along with grain boundary diffusion was observed.

Decisive evidence of dominance of interfacial electromigration over grain boundary can be confirmed based on study by C. S. Hau-Riege and co-workers [65]. In this study, test structure exactly resembling the damascene structure was employed. Electromigration experiments have been carried out on interconnects with very-long-grained bamboo structures, produced by scanned laser annealing, and interconnects with polygranular structures in which the average grain size is less than the line-width. However, no significant differences in the failure rates were found for Cu interconnects with very large grains. This result clearly shows that in damascene interconnects electromigration is dominated by interfacial diffusion instead of grain boundary diffusion. Although it cannot be inferred from the results obtained in this study whether Cu/dielectric-cap or Cu/diffusion barrier metal interface was the dominant interface, it has clearly isolated the effect of microstructure on electromigration in Cu damascene interconnects. As the activation energy was not calculated in this study it may not provide a conclusive proof, but this interpretation can still be considered as valid because it would be highly unlikely for two different failure modes to exhibit similar lifetime properties under identical EM testing conditions.

Direct evidence of Cu/dielectric interface being the fast electromigration path in multi-level interconnects can be seen in ref [59,66-68]. In ref [66] electromigration in Cu damascene interconnects, with tungsten studs and line-width of 0.28μm was

studied , and has clearly shown that the void grows at Cu/SiN cap-dielectric layer interface as shown in **Figure 2.5**. Sensitivity of electromigration performance on Cu/ dielectric interface is also demonstrated, further supporting that Cu/ dielectric interface is the fast electromigration path. In ref [67,68], Cu dual-damascene interconnects were employed and has similarly indicated void formation at Cu/dielectric-cap interface.

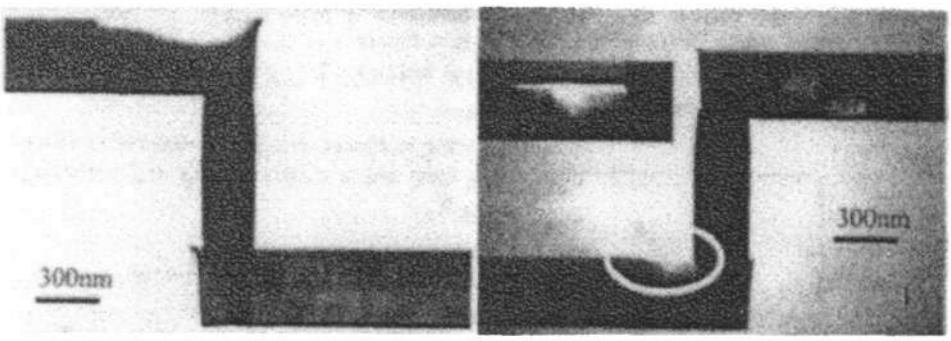


Figure 2.5: Electromigration induced void at Cu/dielectric-cap interface [66].

Thus the Cu/dielectric cap interface plays dominant role in the electromigration performance of Cu-damascene interconnects. Various other parameters like microstructure [63], Cu deposition technique [64], diffusion barrier [69], via reliability [70] and reservoir effects [71] may affect electromigration performance. But the key for better electromigration performance is to improve the Cu/dielectric cap interfacial electromigration and it will become increasingly dominant with scaling for future interconnects. This argument is also supported by a very recent review on electromigration issues in Cu-damascene interconnects by Ogawa and co-workers [1]. Recently extrusion failures are reported in low-k dielectric interconnects [14], which was observed at the IMD/dielectric cap interface. A better IMD/dielectric-cap interface may also help in reducing this failure mode.

In an interesting study in ref [72], a model was developed to simulate the skin effect on current distribution in copper line structure with Ta cladding. Skin effect is a current crowding electromagnetic phenomenon in metal conductor under high frequency. It was found that the current density was maximum at the Cu/Ta interface. Similarly for the critical Cu/dielectric-cap interface, such peak current density will be obtained, for interconnects operating at high frequencies. This effect will become more severe in future technologies, where higher frequency signals will be used.

2.2.3 Electromigration in Cu/low-k interconnects.

New low-dielectric constant (low-k) materials are being investigated as alternatives to SiO_2 for future interconnects to reduce delay, crosstalk and power dissipation [6]. In general, these materials have very different thermo-mechanical properties from SiO_2. There is severe concern over impact of low-k dielectric on electromigration and has developed considerable interest recently. Conflicting results were reported on impact of low-k dielectrics on electromigration performance:-

Degradation in electromigration performance due to low-k dielectrics

Effect of polymer low-k dielectrics on electromigration in Al(Cu) interconnects was studied by Justison and co-workers [73,74]. After compensating for the microstructural differences in Al(Cu) for polymeric low-k and oxide, it was found that there is significant reduction in the back-stress effect in case of interconnects with low-k dielectrics. The reduced back-stress resulted in lack of resistance saturation during EM testing and three times increase in the steady state drift rate. Similar results were found by Lee and co-workers [12-14] for damascene Cu interconnects and failure mode of Cu extrusion at anode at interface between low-k polymer (SiLK^{TM}) and oxide etch stop layer was reported, as shown in **Figure 2.6**. Joule heating is the heating of a conductor as current passes through it. Along with reduction in back-stress and extrusion failures, higher temperature rise due to joule heating because of lower thermal conductivities is also an important concern with low-k dielectrics [75,76]. Similar study on electromigration reliability of Cu/porous low-k interconnects (methylsilsesquioxane MSQ based spin-on organosilicate material) was reported [77]. Reduction in electromigration lifetime and threshold product of current density and line length was found. This observation was attributed to reduction in EM lifetime compared with Cu/oxide interconnect

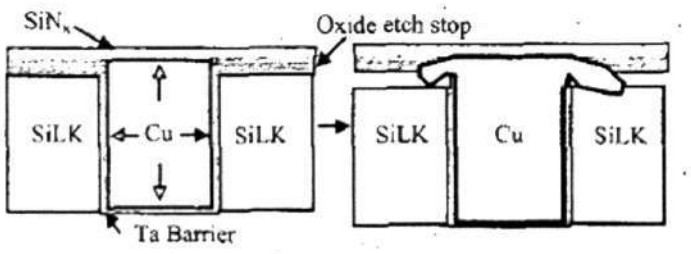


Figure 2.6: Schematic of extrusion failure mode in low-k dielectric interconnects[13]

due to smaller back-stress due to less thermo mechanical confinement of Cu/low k interconnects, similar to previous reports. Lateral Cu extrusion followed by interfacial breakdown at anode was also observed.

Reasons other than reduction in back-stress were attributed for reduction in electromigration lifetime for Cu/FSG interconnects [78]. Formation of void at via bottom instead of at the reservoir due to higher compressive stress was attributed to observed short lifetimes for Cu/FSG interconnects. Attack of fluorine on Ta barrier or Ta/SiN cap interface was thought to be the probable cause of void nucleation.
Impact of low-k dielectrics on electromigration may not be only due to reduction in back-stress. Process issues associated with low-k dielectrics can have significant impact on electromigration performance. Impact of Spin-on-glass^{TM} (SOG) IMD process was reported, in which outgas of SOG at via was found to produce void and correspondingly degradation in electromigration performance [79].

Improvement in electromigration performance due to low-k dielectrics

While some of the reports have shown degradation in EM lifetime due to low-k dielectrics, others have found improvement. S. Foley and co-workers found improvement in electromigration performance of Al(Cu) line with polyimide interlayer dielectric and was attributed to less severe flux divergences at defect locations in case of less rigid polyimide dielectric [80]. In this study, softer dielectric was also shown to be less prone to extrusion failure. Similar improvement in EM lifetime was observed and is explained to be due to elastic deformation of compliant polymer dielectric [15]. This deformation was thought to suppress the tensile stress in interconnect near via and elongate incubation time for void nucleation. In another study by Pei-hua Wang and co-workers [81], improvement in electromigration performance of Al(Cu) was observed, but it is found to be due to micro structural differences in polymer dielectric passivated lines because of high temperature curing process. These differences in impact of low-k dielectrics on electromigration was studied by Doan and co-workers [82] and concluded that low-k dielectrics may improve or degrade EM performance depending on whether EM is void nucleation or void growth dependent. If the electromigration is void growth dominated, then low-k dielectrics will degrade the electromigration performance due to reduced back-stress.

However, if the electromigration is nucleation dominated, low-k dielectrics may improve electromigration performance due to suppression of void nucleation.

Recently, a novel technique to form air gaps in the ILD was disclosed [83]. The interconnects with air gaps were found to have better electromigration performance than conventional interconnects, in spite of reduction in back-stress due to thin passivation layer [84]. Better performance was attributed to reduction in nucleation due to compliant dielectric, similar to previous studies. Reduction in the effective bulk modules by half was estimated, but it has correlated to increase in electromigration lifetime. This is contrary to the model developed by S.P Hau-Riege and co-workers [85], which predicts reduction in electromigration lifetime with decrease in effective modulus.

Despite considerable work on effect of low-k dielectrics on electromigration, there are still many issues, which need to be addressed, like effect of low-k IMDs and ILDs on electromigration in interconnects with different widths and barrier layer thickness. Dominant electromigration mechanism and dominance of interfacial diffusion is dependent on the line width of Cu damascene interconnects. The effect of change in the dielectric on electromigration may be strongly dependent on the width of the line and this effect is evident in the model developed by S.P. Hau-Riege and C.V Thomson [85]. Also, as the barrier thickness is reduced, the change in effective modulus will be significant and may affect EM considerably. But this dependence is not considered in the experimental results reported.

2.2.4 Interfacial electromigration and adhesion

Very recently, a correlation was found to exist between adhesion of Cu to surrounding layers and electromigration [86]. Interfacial adhesion of Cu with various cap layers was measured with four-point bending apparatus. Electromigration tests were performed on Cu damascene test structures with various cap layers to find the void growth rate and activation energy. The interfacial debond energy measured by four-point bending apparatus was found to correlate with the observed void growth rate and activation energies. A linear relationship between electromigration activation energy and work of adhesion was proposed and verified with the experimental results. This study has proved the dominance of Cu-dielectric

interfacial electromigration and has shown interesting correlation of electromigration to interfacial adhesion, i.e. in turn the nature of bonding at the Cu-dielectric interface. Effect of SiC cap layer on electromigration was studied previously [20]. In this study it was observed that SiC cap layer leads to higher MTF as compared to SiN cap during electromigration test and has better adhesion than SiN. This is consistent with the proposed relation between adhesion and electromigration that better adhesion will lead to better electromigration performance. But, if we look at the results closely, it contradicts the proposed model by Lane and co-workers [86] The activation energy was found to be similar for both SiC and SiN cap layers and the observed higher MTF in case of SiC was attributed to change in the pre-exponential factor (D_0) of diffusivity. This is not consistent with the linear relation between electromigration activation energy with interfacial adhesion. Also, adhesion between Cu/SiC is observed to be higher than that of Cu/SiN, which is opposite to observed and predicted adhesion by Lane and co-workers. In these studies only the interfacial adhesion energy of Cu with different cap layers was considered. Stress in the dielectric cap layer may have significant impact on the electromigration drift-velocity due to the "back-stress". Mechanical properties of the film can alter the void nucleation [77] and significantly reduce the incubation time. Stress can also significantly affect adhesion [87]. But, these factors were not considered for the various dielectric cap layers employed in these studies. Despite inconsistency in electromigration parameters, both the studies show improvement in electromigration performance with better adhesion between Cu and dielectric cap layer.

2.2.5 Other important implications of dielectric-cap interface on Cu-damascene interconnect reliability

With the continuous scaling of the interconnect technology, interface to bulk ratio will increase significantly. Thus the interfaces are the key for electromigration reliability of the Cu damascene interconnects. Especially the Cu/dielectric interface is important as it forms the fast electromigration path and will become more severe for future interconnect technologies. This interface is important not only for electromigration reliability, but also for time dependent dielectric breakdown (TDDB) reliability, which is one of the reliability concerns for Cu interconnects.

Recent studies on TDDB of Cu damascene interconnects, using test structures that resemble the actual damascene structure instead of using metal-insulator-Si (MIS) structure, have found that TDDB occurs by a dielectric-cap interface breakdown mode, not by a bulk degradation mode [88]. TDDB mechanism in case of structures without barrier metal was found to be of bulk mode. But in case of structures with barrier metal, which are similar to actual damascene structure, it was found that Cu diffusion is mainly at the Cu-dielectric cap interface as shown in **Figure 2.7** due to CMP damage, also electric field is concentrated at this surface due to shortest distance between the adjacent Cu lines, angular shape of the Cu lines at the corner and higher dielectric constants at this interface due to the cap layer. In case of low-k IMDs, this was found to be further aggravated and interface breakdown mechanism became more dominant. Modification of this Cu-dielectric cap interface was found to have considerable impact on the TDDB performance, which further supports its significance for TDDB reliability [89]. Thus Cu –dielectric interface is the key for both electromigration as well as TDDB reliability, which are the most important reliability concerns in Cu damascene interconnects.

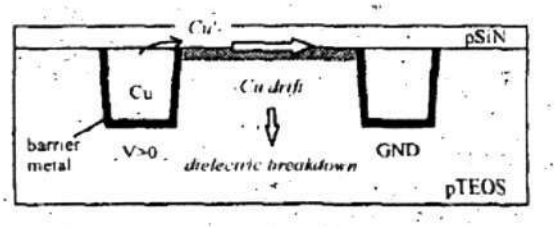


Figure 2.7: Cu/dielectric-cap interface breakdown mode [89]

2.2.6 Methods to improve electromigration performance of Cu damascene interconnects

Doping of Al with Cu was found to retard electromigration in Al [90-91] and Al alloy is widely used later on for better electromigration performance of interconnects. Similarly, various dopants like Mg, Al, Sn, Zr are being investigated for reducing electromigration in Cu interconnects [92]. Some of these dopants are used during Cu seed layer deposition and have shown to improve Cu/diffusion barrier metal interface [93]. But actually not the Cu/diffusion barrier metal interface but Cu/dielectric cap interface is important for electromigration. Various other techniques which attempt to optimize the microstructure are also being tried [63,94].

But with bamboo-like grain structure in sub-micron line-width damascene interconnects and interfaces being the electromigration path, microstructure is not a major concern. As the Cu/dielectric-cap interface is the most dominant electromigration path, especially for sub-micron line-width Cu damascene interconnects with bamboo-like grain structure, this interface should be made more electromigration resistant. A few such attempts have been made so far [95-96]. In reference [95], a technique is reported to suppress the electromigration at Cu/dielectric-cap interface. A thin (10-20nm) electroless metal coating of CoWP, CoSnP, or Pd, was deposited the top surface of Cu damascene lines after CMP, with selectively electroless plating. Dielectric-cap layer is deposited thereafter. A significant reduction in electromigration was observed for the coated samples. Although this is a promising technique to effectively suppress electromigration, selective electroless deposition is hindered with problems such as deposition controllability and film quality [96].

Other method involving Cu surface passivation by Cu silicide passivation was previously reported [97]. In this study higher lifetime was observed for passivated interconnects, but the activation energy was lower. Also, improvement due to NH_3 treatment after CMP is suggested [98]. In reference [99] a novel self-assembled ZrN cap technology to replace dielectric-cap layer is reported. Interesting property of thin (<10nm) ZrN films was observed- these films were found to be metallic when formed on metal under-layer and insulator when formed on dielectric. But similar electromigration activation energies were found for single damascene test structures with and without ZrN cap layer. Also significant improvement in lifetimes was not observed. For early failures (<50% of CDF), lifetimes were almost similar and longer life times were observed only for late failures in case of ZrN capped interconnects.

Alloying of Cu interconnects with Mg can be of particular interest for interfacial electromigration. Recently, integration of Cu-Mg alloys in interconnects was demonstrated [100-101]. Mg doping was used to improve adhesion of Cu with dielectrics. It is important to note from this study that Mg diffuses through Cu to surface and being highly reactive with oxygen, nitrogen and carbon, which are typical constituents of dielectric-cap layer, will form compounds such as MgO or

MgF to alter interface. Formation of such a MgO layer at Cu surface is reported in reference [102]. Thus Mg can improve the adhesion between Cu and the dielectric-cap layer. Better adhesion will lead to reduced electromigration according to recently proposed relationship between adhesion and electromigration activation energy [86]. Similarly, Sn was thought to retard surface electromigration in Cu [103].

2.2.7 Electromigration-induced voiding in Cu dual-damascene interconnect structures

Asymmetric electromigration behavior of upper and lower dual-damascene interconnect structures was reported [61]. The different electromigration behavior between upper and lower layer structures was proposed to be based on the location of maximum tensile stress developed during electromigration at the cathode end via bottom Ta barrier, which acted as the blocking boundary for Cu atom diffusion. The void is assumed to form if the critical stress for void nucleation was reached. It was argued that in the case of M-2 structures the maximum tensile stress was reached at the base of the via where Cu was bounded by Ta on all sides whereas for the M-1 structure, the void nucleation site was thought to be at the Cu/dielectric cap interface near the via bottom due to the peak tensile stress which then grew along this interface. Thus the peculiar behavior of dual-damascene interconnect structures was attributed to the flux divergence at via bottom and ease of void nucleation in Cu/SiNx interface at cathode end. This electromigration-induced voiding mechanism is illustrated in **Figure 2.8.** The short length effect in upper and lower layer structures was studied in reference **[68]** and thought to be attributed to similar mechanism. The condition for electromigration immortality due to the short length effect in lower layer structures has been proposed to be the limit for void nucleation, and in upper layer structures, the proposed condition is when the electron wind force does not exceed the back-stress.

In most of the recently reported studies on similar electromigration in Cu damascene interconnect structures [62,65-68], the electromigration-induced voids were interpreted assuming similar mechanism of void nucleation at the cathode via, which is a flux divergence site.

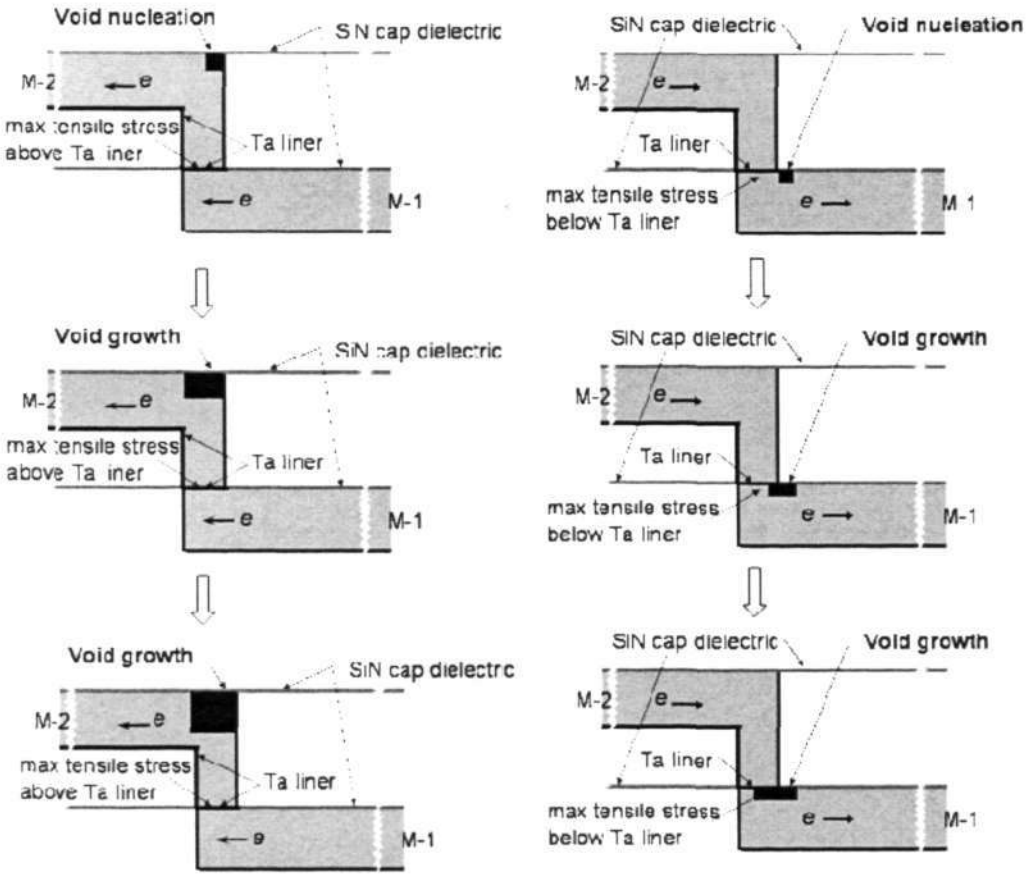


Figure 2.8: Illustration of current understanding of electromigration mechanism in dual-damascene Cu interconnects.

The interconnects in real ICs are much more complex with multiple interconnect line segments connected to vias. Interconnect tree structures are required for realistic electromigration studies which can correctly simulate the conditions in real on-chip interconnects [104]. Electromigration studies on Al interconnect [104, 105] and dual-damascene Cu interconnect [106, 107] tree structures have been reported. Discrepancies in the behavior of Cu damascene interconnect trees as compared to that of Al interconnect trees were observed, and it was found that in the case of Cu damascene interconnect trees, the highest stressed tree segment is not always the least reliable[106, 107]. This peculiar behavior was thought to be probably associated with variation in the architectural schemes of these

interconnect systems- possibility of liner rupture at via bottom and ease of void nucleation at Cu/SiN_x interface in the case of Cu damascene interconnect structures

2.3 Brief summary of electromigration-induced voiding simulation techniques

Many simulation tools have been developed to study evolution of voids and surface of interconnect lines due to electromigration. A majority of these simulation techniques have employed continuum approach to solve the problem of mass transport along the surfaces [108-117]. Each of these approaches have considered a sub-set of three principle modes of atomic migration – mass flux due to electromigration, surface curvature and stress driven mass transport. Simulations for various different scenarios were carried out. These include- simulation of voids in perfect lattice, near an external surface, near other voids leading to coalesce of voids, slit-like void evolution in Al interconnects and simulation of surface evolution along a single crystal and across grain boundary.

Almost all of the electromigration simulation techniques developed so far are formulated as the continuum or mass transport level rather than the atomic level. Very few attempts are made to develop atomic level electromigration simulation technique- an atomistic model of void nucleation and growth was developed by David Frank Richards et al. [118] and a model to simulate void nucleation and evolution was demonstrated by Robert Roy Atkinson et al.[119]. Monte-Carlo methods were employed for simulation of atomic transport in these research works.

Monte-Carlo approach is used in statistical mechanics, which is a tool to study systems that consist of a large number of interacting elements, like the atoms of a crystalline solid. These metals exist in a fixed crystalline lattice which defines the location of atoms. The use of statistical mechanism here is to define the motion of an atom through the lattice. The combination of Monte Carlo selection of atoms and statistical mechanics result in a method to track the motion of atoms in a material under environmental forces resulting from various fields such as electric current, stress gradient, surface tension, grain boundary interface etc. Metropolis algorithm for atomic jumps is generally employed in such Monte-Carlo approach. The Metropolis algorithm states that an atomic movement is successful if there is a reduction in the total energy of the system. However, a movement that raises the total energy of the system is still possible but has a finite probability, as explain below:

$$A(\mu \rightarrow \nu) = \{1..if E_{\mu} - E_{\nu} < 0$$

$$= \begin{cases} \exp\left[\frac{E_\mu - E_\nu}{kT}\right] \ldots if E_\mu - E_\nu > 0 \end{cases}$$

Where, $A(\mu \to \nu)$ is the probability of system change form state μ to state υ and E represents the system energy.

2.4 Gap analysis from the literature review and novelty of this research work

- Cu damascene technology is relatively new and electromigration mechanism in dual-damascene interconnects is not studied in depth. In this work, electromigration mechanism in dual-damascene Cu interconnects is investigated using via-fed test structures which represent the dual-damascene Cu architecture. A detailed characterization of electromigration in upper and lower layer dual-damascene structures with different metal line widths was carried out. A number of investigations on the effect of short length on electromigration have been reported [1,68,120-123]. Short length effect is observed in Cu damascene structures as for Al interconnects. But this effect may be complicated in case of Cu interconnects than in Al interconnects because of the dual-damascene architecture. The complexity can be understood from the different electromigration failure mechanisms in upper and lower layer dual-damascene test structures [61]. It is therefore important to investigate short-length effect for upper and lower layers in dual-damascene structures. This effect was studied using upper and lower layer via-fed test structures with various lengths.

- Initial part of this study suggested that the peculiar electromigration behavior is due to Cu/dielectric cap interface acting as vacancy sink and preferable nucleation site. Effect of modifying Cu/dielectric cap interface on electromigration performance of Cu dual-damascene interconnect structures was investigated.

- Although most of the studies on electromigration in Cu damascene interconnects have shown that the Cu/Si_3N_4 cap interface is the dominant electromigration path [10,59,62,66,68,123], some have reported grain boundary diffusion to be dominant[124-125] and have interpreted electromigration in Cu interconnects by coupling grain boundary and interface diffusion [52]. Others have indicated that the Cu/liner interface is the fast electromigration path [94]. Moreover, contrasting

electromigration behavior of upper and lower layer dual-damascene structure was found[61], and the effect of line width and length on electromigration was determined in the initial part of this study. But the exact details of electromigration mechanism in dual-damascene structure were not completely understood. Due to the technological importance of dual-damascene Cu interconnects, it was necessary to understand the exact electromigration mechanism in these structures. The electromigration mechanism in Cu dual-damascene interconnect structures was unraveled by employing the *in-situ* SEM electromigration characterization technique.

- Numerous studies on electromigration have been reported, however, most of them have employed straight via-to-via test lines or single layer lines directly connected to contacts. The interconnects in real ICs are much more complex with multiple interconnect line segments connected to vias. Interconnect tree structures are required for realistic electromigration studies which can correctly simulate the conditions in real on-chip interconnects[104]. In-depth understanding of electromigration failure mechanism in interconnect tree structures is necessary for optimization of physical and electric design rules. Considering the design rules in future interconnect architectures, optimized on-chip interconnect systems with high immunity to electromigration-induced failures can be designed. Electromigration studies on Al interconnect [104,105] and dual-damascene Cu interconnect [106,107] tree structures have been reported. Discrepancies in the behavior of Cu interconnect trees as compared to that of Al interconnect trees were observed, and it was found that in the case of Cu interconnect trees, the highest stressed tree segment is not always the least reliable[106,107]. This peculiar behavior was thought to be probably associated with variation in the architectural schemes of these interconnect systems and possibility of liner rupture at via bottom in the case of Cu structures. As dual-damascene Cu interconnect technique is currently being employed for on-chip interconnect fabrication, and will continue to be used for next technology generations in the near future due to significant cost advantage, it is of great technological significance to correctly understand the electromigration

mechanism in dual-damascene Cu interconnect tree structures. In this study, electromigration failure mechanism in Cu interconnect tree structures is unraveled by *in-situ* SEM characterizations and a clear understanding of its electromigration behavior is established.

- Electromigration-induced voiding mechanisms revealed during *in-situ* characterizations could not be explained based on the current understanding of electromigration mechanisms. A simple model is developed, which was implemented using random atomic jumps based on the Monte-Carlo method, to understand electromigration-induced voiding observations revealed during this research work. Few similar models were reported previously [118,119]. However, they were not used for extensive investigation of electromigration void evolutions in various Al and Cu interconnect structures, perhaps due to lack of direct and detailed experimental evidence of exact void evolution during electromigration stressing. Now, equipped with *in-situ* SEM observations of electromigration-induced void evolution,an attempt is made to do so in this research work. The electromigration-induced void evolutions in Cu damascene structures revealed during this work as well as experimental results reported by various other researchers can be understood based on this model.

Chapter Three

Experimental Set-up

3.1 Electromigration test structures

Following electromigration test structures were used in this study

3.1.1 Upper layer (M-2) test structure

In this test structure the test line is the upper layer (metal layer-2) trench and it is connected to wide metal layer-1 (M1) trench by a single via at both the ends. This test structure will be referred as M2-test structure. Schematic of cross section and top view of M-2 test structure is as shown in **Figure 3.1(a)**. The wide M-1 trench is connected to the bond pads for external connection. This test structure was used for electromigration characterization of M-2 layer and the electron flow in the via at cathode end is upstream, i.e. from lower (M-1) layer to upper (M-2) test layer.

3.1.2. Lower layer (M-1) test structure

Similar to M-2 test structure, this test structure consists of test line in the lower layer (metal layer-1) trench and it is connected to wide metal layer-2 (M2) trench by a single via at both the ends. This test structure will be referred as M1-test structure. The wide M-2 trench is connected to the bond pads for external connection. This test structure was used for electromigration characterization of M-1 layer and the electron flow in the via at cathode end is downstream, i.e. from wide upper (M-2) layer to lower (M-1) test layer. Schematic of cross section and top view of M-1 test structure is as shown in **Figure 3.1(b)**.

The via diameter is 0.26 μm for both the M-1 and M-2 test structure. Both the structures have top, bottom and side extrusion monitors. M-1 and M-2 test structure dimensions are listed in **Table 3.1**.

3.1.3 Interconnect tree test structure

This test structure was similar to upper layer (M-2) test structure with the test line in upper (M-2) layer. The test line length was 800 μm and width was 0.28 μm. There was an additional via at the center of the test line. Schematic of cross section and top view of interconnect tree test structure is as shown in **Figure 3.2**.

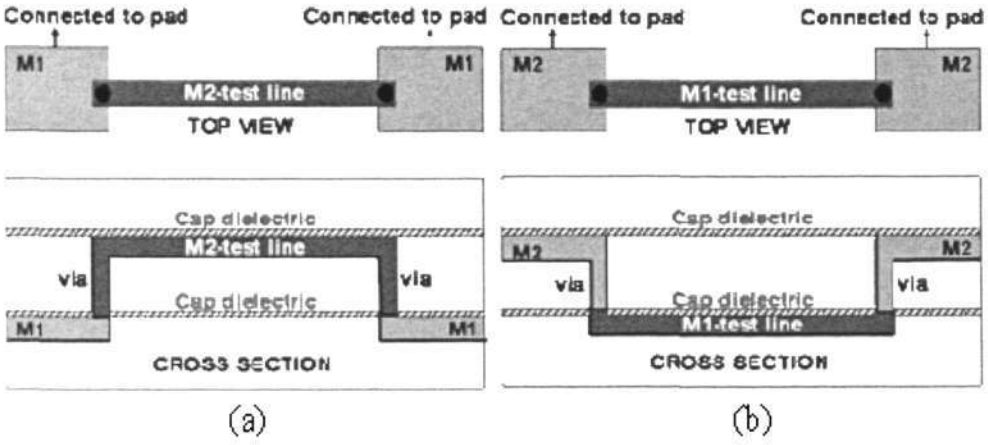


Figure 3.1: Schematic of (a) M-2 test structure and (b) M-1 test structure

Metal level	Length(μm)	Width(μm)
M-1	800, 100,50,20	0.28, 0.70
M-2	800, 100,50,20	0.28, 0.70

Table 3.1: Dimensions of the M-1 and M-2 test structures

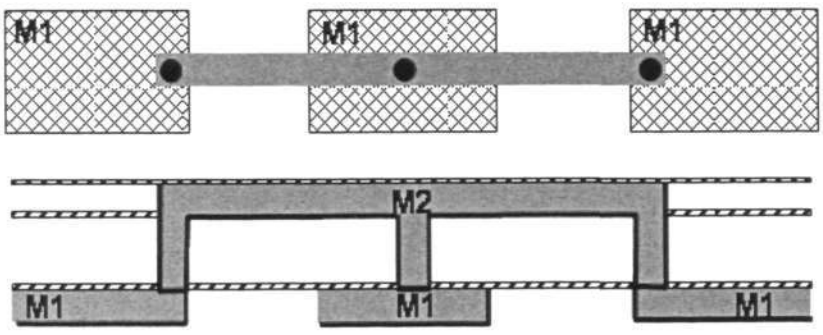


Figure 3.2: Schematic of interconnect tree test structure

3.2 Electromigration test structure fabrication

3.2.1 Test structure fabrication by dual-damascene process

Electromigration test structures were fabricated by advanced 0.18 μm dual damascene process developed *at Institute of Microelectronics (IME), Singapore.* A stack of 500 Å SiN and 5 kÅ Undoped silicate glass (USG) was deposited as the first inter-metal dielectric (IMD1) layer by plasma enhanced chemical vapor deposition (PECVD). Metal 1 (M1) trench was then patterned. The Cu metallization stack consisted of 250 Å Ta barrier layer, 1.5 kÅ Cu seed layer deposited by physical vapor deposition (PVD) and 6 kÅ electroplated (ECP) Cu layer (subsequently CMP). A capping layer of 500 Å (SiN) was deposited after Cu CMP process. Layers of 8 kÅ USG, 500 Å SiN and 5 kÅ USG were then deposited as IMD2. 500Å SiN in IMD2 served as M-2 trench etch stop layer. Metal 2 (M2) trench and via were then formed by a via-first dual damascene process. The M2 metallization stack was the same as M1. The thickness of both M1 and M2 was 0.35 μm and via diameter was 0.26 μm. The details of the 2-metal layer Cu/oxide dual damascene stack is illustrated in **Figure 3.3.** This is the baseline process flow and variations were made to fabricate test structures for studying effect of surface treatment.

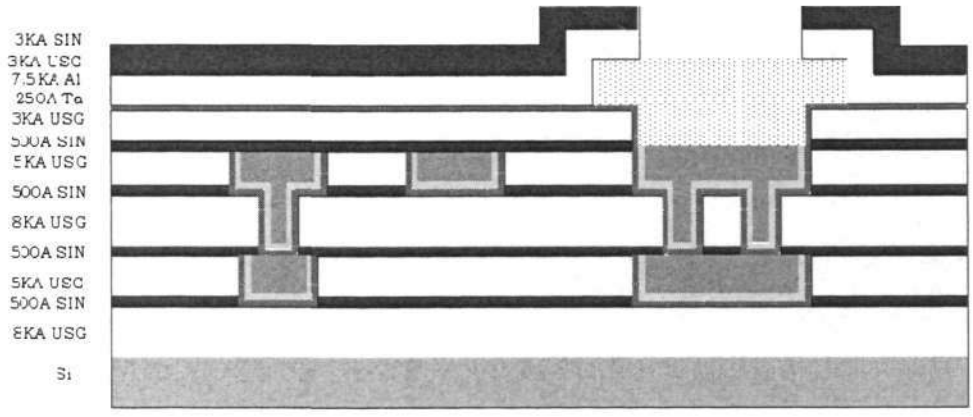


Figure 3.3: Schematic of 2-Metal layer Cu/oxide dual damascene stack

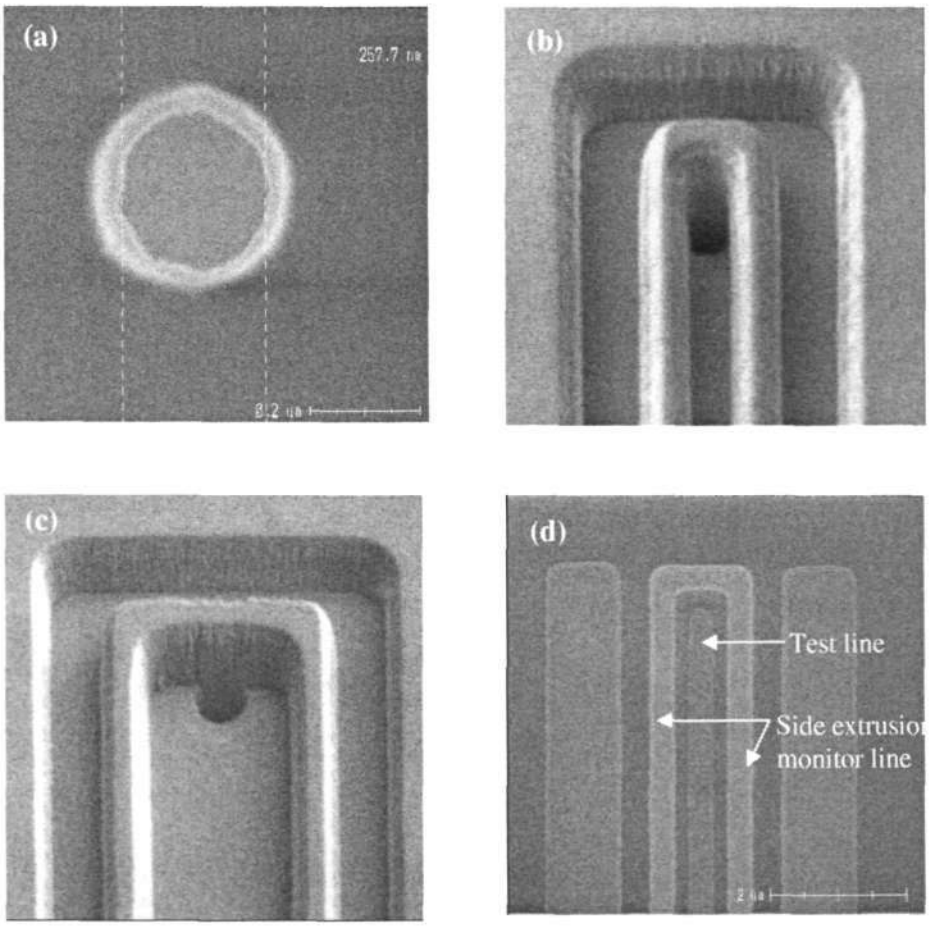


Figure 3.4: Fabrication of test structures

The complete fabrication process was closely monitored using in-line thickness and dimension measurements. M-2 electromigration test structures are shown in **Figures 3.4**. A via (before M-2 trench patterning) connecting the M-2 test line to wide M-1 lines (below) is shown in **Figure 3.4 (a)**. Patterned M-2 test line trenches with width 0.28 μm and 0.7 μm are shown in **Figure 3.4 (b)** and **3.4 (c)** respectively. M-2 test structure with width 0.28 μm after Cu deposition and CMP is shown in **Figure 3.4 (d)**. M-1 test structures have similar structure except the test line was in M-1.

3.2.2 Surface treatments

Dominant role of Cu/dielectric cap interface in electromigration is reported [1,10,59,61,62,66,68,123] and was also observed in our electromigration

characterizations. If this interface is modified so as to make it more resistant to electromigration, the dominant path for electromigration can be retarded leading to better reliability. Cu surface after CMP was exposed to different treatments as explained in **Figure 3.5.** The dielectric cap was deposited subsequently. These experiments also served to confirm that electromigration is interface diffusion dominated and Cu/dielectric interface is the dominant path. Both, M1 and M2 layers were exposed to surface treatments.

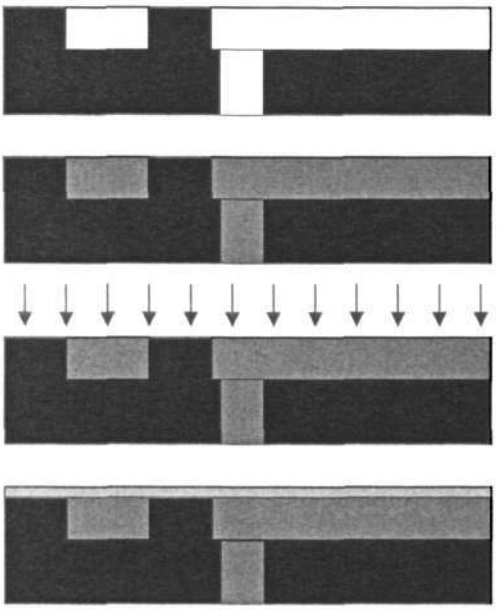


Figure 3.5: Surface treatment

Following surface treatments were carried out:

1. In-situ NH_3 pre-treatment during deposition of silicon nitride dielectric-cap layer by PECVD.
2. In-situ SiH_4 pre-treatment during deposition of silicon nitride dielectric-cap layer by PECVD.
3. Pre-clean treatment – In this treatment a clean process consisting of CF_4 treatment followed by hydrogen treatment by a remote plasma system was carried out.
4. Control samples without any surface treatment

3.3 Electromigration characterization and failure analysis

3.3.1 Electromigration characterization

Electromigration characterization was performed by the life-time test method using package level reliability test system in which 30 test structures were tested at a time. The wafers were diced into dies containing the test structure, followed by die attach to 24-pin ceramic package and wire-bonding for electrical connection to the test structure. The wire-bonding process was established using a 1.2 mil gold wire and the wire-bonding parameters are listed in **Table 3.2**. The package level reliability test system consists of oven which is maintained at a constant temperature and boards with electrical connections in which the packages can be mounted. During electromigration stressing in package level electromigration system, a constant current was forced through each test structure and its resistance was continuously monitored by measuring voltage across the test structure. The electromigration test set-up is illustrated in **Figure 3.6**. Failure time was noted as the resistance increased more than the pre-defined failure criteria and cumulative failure distribution was plotted. A statistical analysis tool was used to plot lognormal distribution and obtain MTF, which was based on Persson and Rootzen method for analysis of lognormal data [126]. Activation energy and current density exponent (n) was determined based on Black's equation. Following experiments were performed on M-1 and M-2 test structures fabricated by base-line process as listed in **Table 3.3 to 3.5.** Electromigration characterization of M-1 and M-2 test structures with different lengths was performed to study the "back-stress" effect. These experiments are summarized in **Table 3.6.** Higher current density was used in order to complete the

Wire	Gold wire (1.2mil)
Temperature	200°C
Impact force	150mN
Bond force	100mN
Time	17msec
Ultrasonic Power	23%

Table 3.2: Wire-bonding parameters

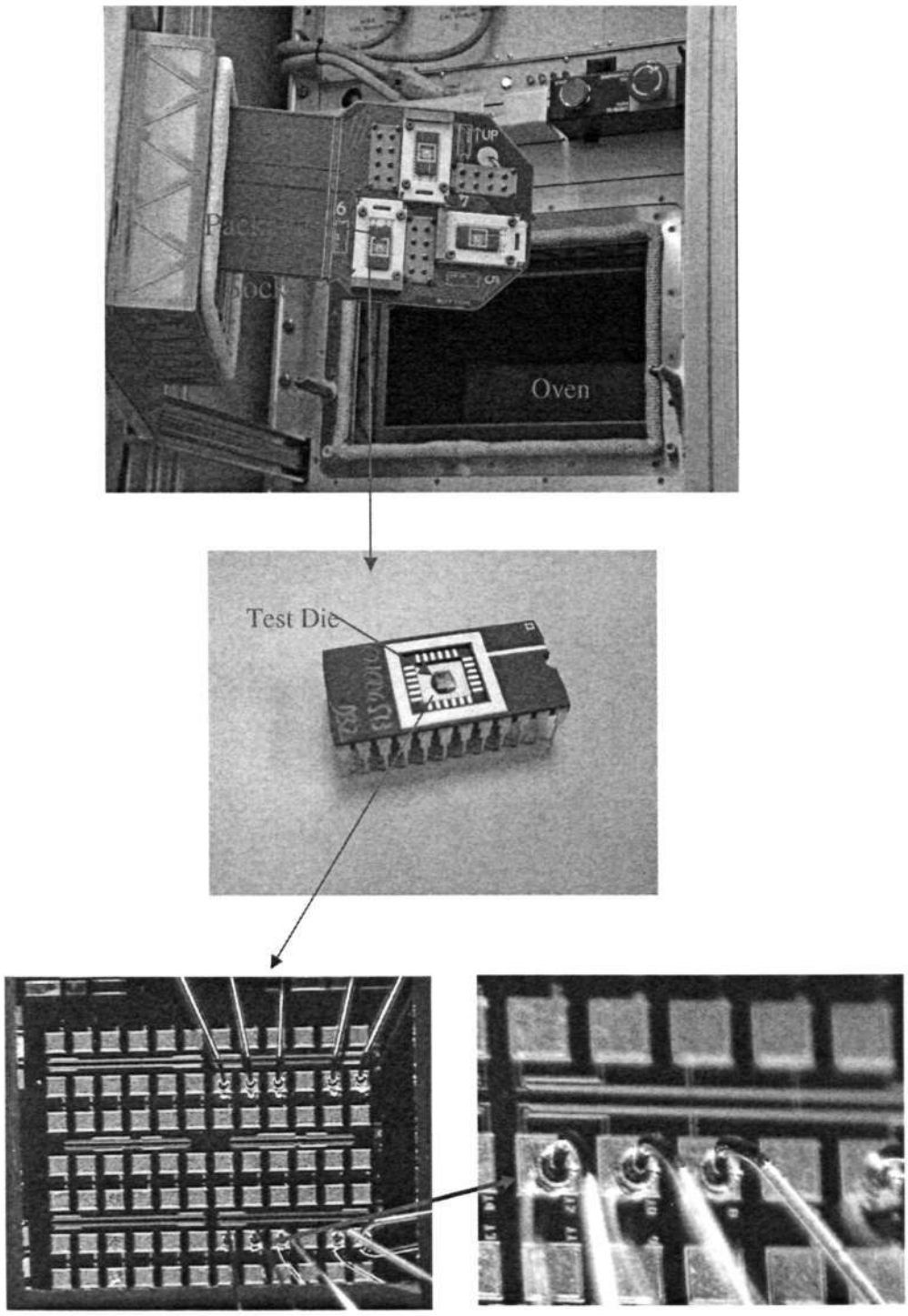


Figure 3.6: Electromigration test set-up

TEST STRUCUTRE			TEST CONDITION	
Metal Level µm	Width µm	Length µm	Temperature °C	Current density(J) MA/cm^2
M-2	0.28	800	300	0.8
M-2	0.28	800	325	0.8
M-2	0.28	800	350	0.8
M-2	0.70	800	300	0.8
M-2	0.70	800	325	0.8
M-2	0.70	800	350	0.8

Table 3.3: Experiments to determine E_a and effect of width in M-2

TEST STRUCUTRE			TEST CONDITION	
Metal Level µm	Width µm	Length µm	Temperature °C	Current density(J) MA/cm^2
M-2	0.28	800	350	0.8
M-2	0.28	800	350	1.2
M-2	0.28	800	350	1.5
M-2	0.70	800	350	0.8
M-2	0.70	800	350	1.2
M-2	0.70	800	350	1.5

Table 3.4: Experiments to determine n

TEST STRUCUTRE			TEST CONDITION	
Metal Level µm	Width µm	Length µm	Temperature °C	Current density(J) MA/cm^2
M-2	0.28	800	300	0.8
M-2	0.28	800	325	0.8
M-2	0.28	800	350	0.8
M-2	0.70	800	300	0.8
M-2	0.70	800	325	0.8
M-2	0.70	800	350	0.8

Table 3.5: Experiments to determine Ea and effect of width in M-1

TEST STRUCUTRE			TEST CONDITION	
Metal Level µm	Width µm	Length µm	Temperature °C	Current density(J) MA/cm^2
M1 and M2	0.28	100	350	2
M1 and M2	0.28	50	350	2
M1 and M2	0.28	20	350	2

Table 3.6: Experiments to study short length effect

TEST STRUCUTRE			TEST CONDITION	
Surface Treatment	Structure	Width µm	Temperature °C	Current density(J) MA/cm^2
NH_3	M1 and M2	0.28	300	1.2
Pre-clean	M1 and M2	0.28	300	1.2
SiH_4	M1 and M2	0.28	300	1.2
Control	M1 and M2	0.28	300	1.2
NH_3	Single layer	0.28	300	1.5
Pre-clean	Single layer	0.28	300	1.5
SiH_4	Single layer	0.28	300	1.5
Control	Single layer	0.28	300	1.5

Table 3.7: Experiments to determine effect of surface treatment

test in reasonable time duration. For studying effect of interface modification, M-1 and M-2 test structures with various surface treatments and control samples were tested (**Table 3.7**). Electromigration performance of single layer NIST test structures with various surface treatments was also tested at 350°C with a current density of 1.5 MA/cm^2.

3.3.2 Failure analysis

Focused ion beam (FIB) was used for failure analysis after electromigration tests. Dual beam FIB has an ion and an electron column. It provides the advantage that the electron beam can be used for imaging therefore limiting the amount of ion damage to the sample. The electron beam can be used to deposit the first 30 - 50 nm of metal. Details of FIB are provided in Appendix 2.

3.3.3 Microstructure analysis

Grain structure was revealed by the ion beam images of the test line during FIB cross-sectioning. Moreover, cross section sample for TEM was prepared by FIB Instead of taking cross section at various sites along the length of a single trench, comb structures with many parallel trenches was used to verify the microstructure at the cross section of the trenches as illustrated in **Figure 3.7**. One cross section at the comb structure can reveal many trench cross sections for characterization of microstructure by TEM.

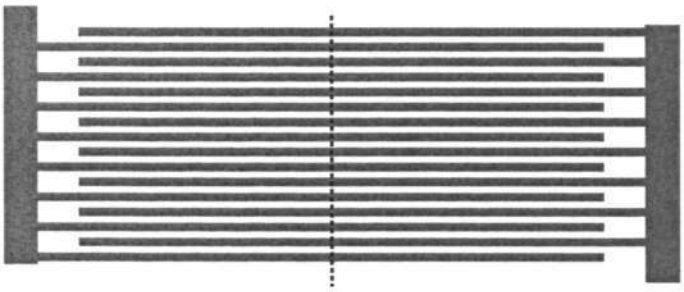


Figure 3.7: Top view schematic of comb structure with many parallel trenches

3.4 *In-situ* SEM characterization

The *in-situ* SEM characterization technique was developed by M. A. Meyer et al.[127] at *AMD (Advanced Micro Devices), Germany*. The key feature of this technique is that a thin layer of passivation was left in front of the cross-section of the line and via under test. Thus, the test structure remains fully passivated, while at the same time it becomes possible to image it with reasonable image quality, during elctromigration stressing.

3.4.1 Sample preparation

Samples were cleaved from the wafer and mounted on 24-pin test chips. The electrical connections were made by wire bonding from the aluminium bond pads to the landing pads of the test chip. Cross-sections were milled at the via site near the cathode end of the line under test using FIB for the in situ investigations. Firstly, a large trench was milled near the cathode end of the line under test **(Figure 3.8 (a) and (b)**). Then, using the fine milling tool, the final cross-section was milled, leaving a thin film of passivation in front of the via / line structure to keep it fully embedded. The most crucial step in this preparation procedure is the final cross-section milling. The milling process was stopped just before the line under test was reached, leaving between 50 and 150 nm of passivation in front of the line and the via. With this procedure, the line and via under test was kept fully embedded. Backscattered electron images of the final cross-section at two different acceleration voltages are shown in **Figure 3.8 (c) and (d)**. The line under test cannot be seen at 5 kV, while it is visible at 15 kV. This prooves that there is thin passivation in front of the line and the via and it is fully embedded.

3.4.2 *In-situ* SEM electromigration test set-up

The stage of a LEO Gemini 1550 SEM system was replaced by a custom-made heating stage as shown in **Figure 3.9.** It consists of a aluminum base plate that can be mounted on the *xy*-stage of the SEM. A vertical glass rod, which holds the sample holder, is fixed to the base plate. An S-shaped thermocoax wire heating element of 10-cm active length runs inside this holder. It is powered by a standard laboratory DC power supply. The power applied to it ranges from 5 to 10 W for

temperatures up to 350°C. This heater block can also be manually tilted to approximately 50–70°, in order to view the samples, which contain FIB-milled cross-sections at the region of interest. A heat shield is mounted just below the sample holder. The glass rod and the heat shield are designed to reduce the thermal load to the stage mechanism during the in situ experiment. A thermocouple is mounted near the sample to monitor the temperature during the experiments.

After the samples were mounted inside the SEM and the sample temperature had been stabilized, the electrical current was applied to the samples and the SEM image capturing was started. The SEM imaging conditions were: 20 kV, 60-μm aperture, SE detector (Everhart-Thornley) at 400 V bias, 20-s frame capture time. Images were recorded automatically using a image recognition and capture software. Upper layer test structures, lower layer test structures and interconnect tree test structures were tested in the *in-situ* SEM system**.** The test structures were stressed at 300-350°C. Upper and lower layer test structures were stressed with a current density of 5-10 MA/cm^2 and the cathode via region was images continuously by the SEM. Resistance of the test structure was also monitored during test. The interconnect tree structures were tested with various current configurations as explained in **Figure 3.10.** Current density and direction in the right segment were kept constant while the left segment was stressed in various configurations. The middle via region was continuously imaged by SEM, and the resistance of the left and the right segments was simultaneously monitored.

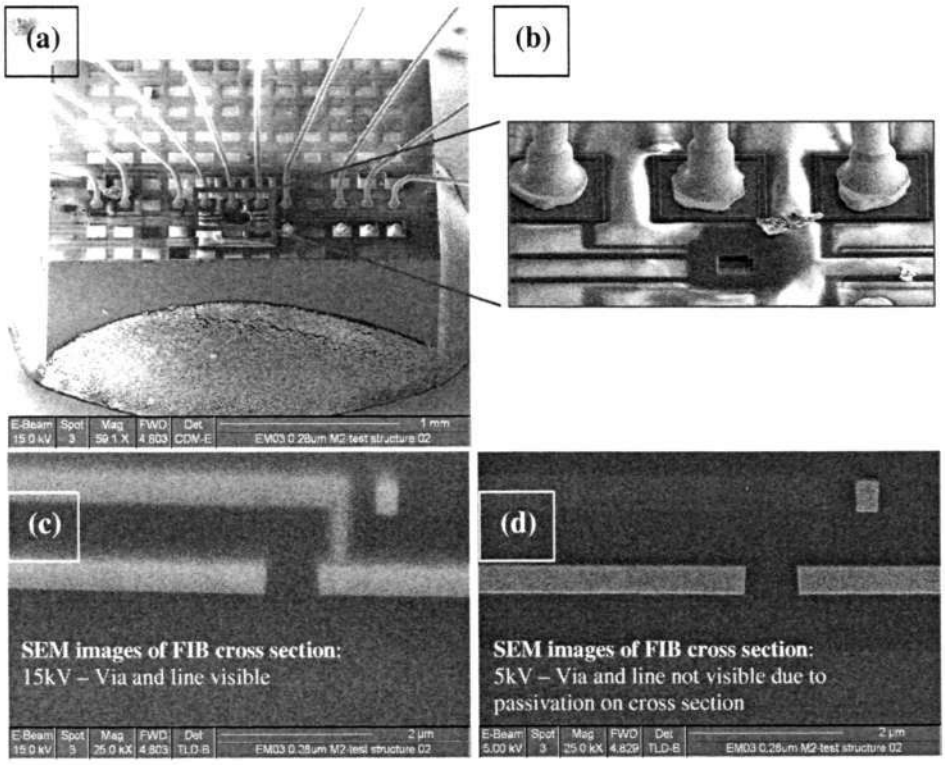


Figure 3.8: Sample preparation for characterization by FIB

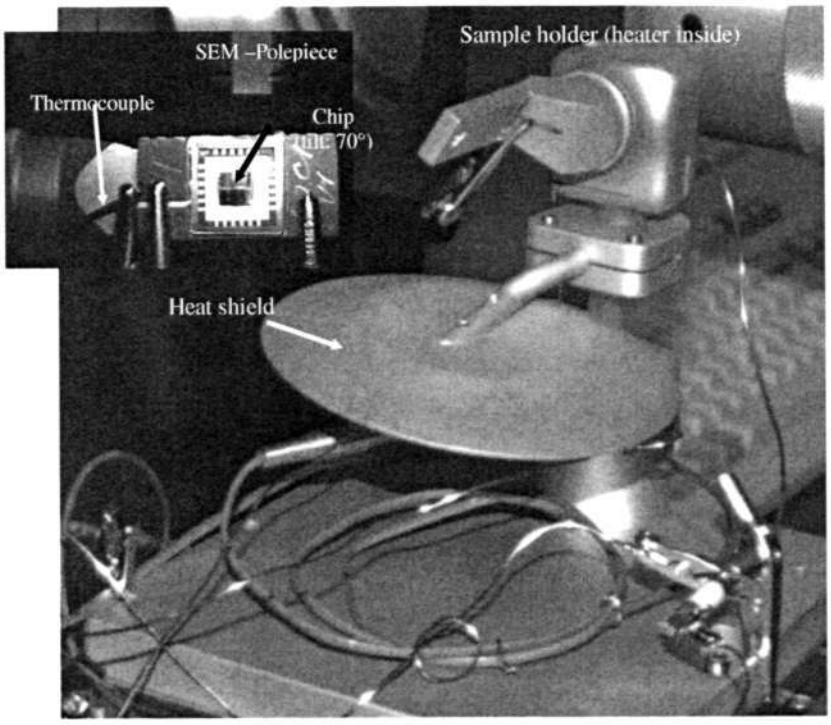


Figure 3.9: *In-situ* SEM test system

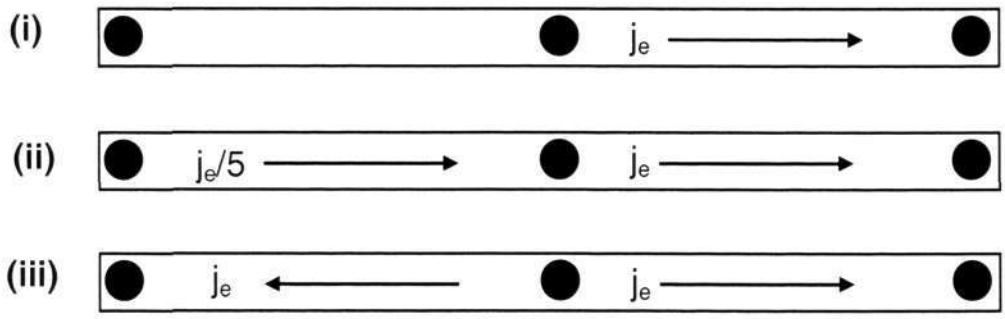


Figure 3.10 Current configurations employed during *in-situ* SEM characterizations of interconnect tree structure (j_e= 5 MA/cm^2 – 10 MA/cm^2 and arrows indicate electron flow direction)

Chapter Four

Results

4.1 Electromigration behavior of dual-damascene interconnects

4.1.1 Electromigration characterizations of upper (M-2) and lower (M-1) layer test structures

Resistance degradation profiles

Typical relative resistance change of the M-1 and M-2 test structures during electromigration test is shown in **Figure 4.1**. Two different types of resistance degradation profiles can be identified. For M-1 test structures, abrupt resistance change profiles were observed, while a gradual resistance change was observed for M-2 test structures. This indicates different failure modes in M-1 and M-2 test structures. Failure analysis was carried out to verify this and revealed different failure modes for M-1 and M-2 test structures. Failure analysis results are presented in subsequent sections.

Activation energy (E_a)

Activation energy was determined from electromigration tests performed at different temperatures keeping same current density. Lognormal cumulative failure distributions at different temperatures are shown in **Figure 4.2a.** MTF values were obtained from the lognormal plot and activation energy was found using the Black's equation [36]. Activation energy was obtained from the slope of line plotted by ln(MTF) versus ln(1/T), where T is the temperature in ^{o}K (**Figure 4.2b**). Calculations for obtaining activation energy are illustrated in **Table 4.1**. Activation energy for other structures was found similarly. For M-2 test structure with line-width of 0.28 μm, activation energy was found to be 0.86 eV. Similar activation energies were observed for 0.7 μm wide M-2 test structures. Activation But for M-1 test structure, lower activation energies- 0.49 eV and 0.60 eV were observed for 0.28 μm wide and 0.7 μm wide structure, respectively.

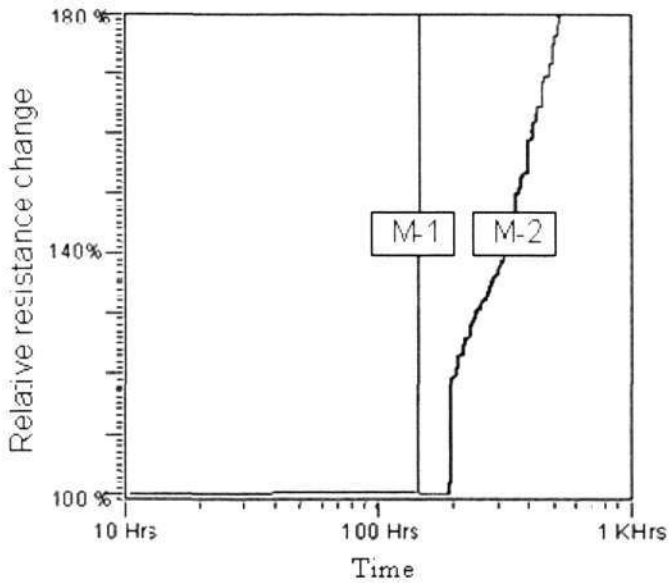


Figure 4.1: Resistance degradation profiles for M1 and M-2 test structures

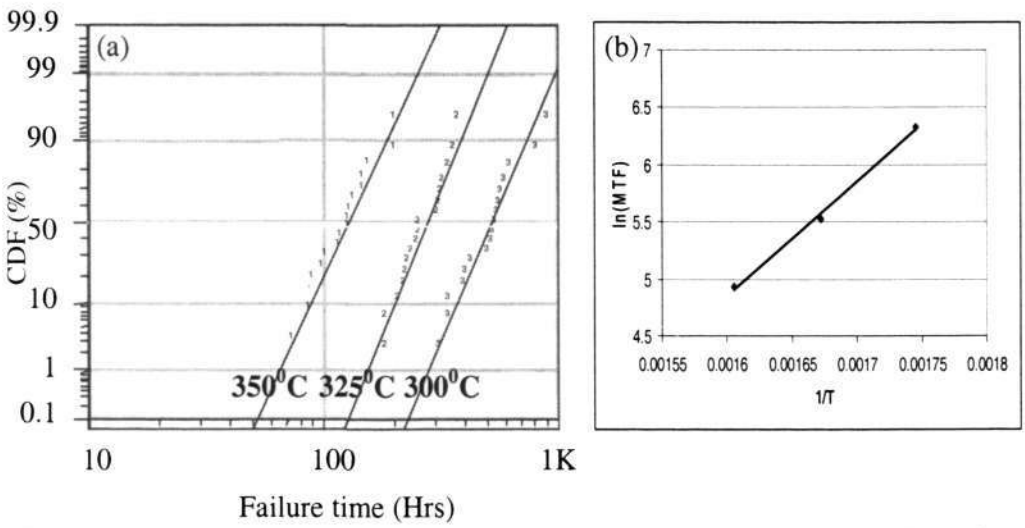


Figure 4.2: a)Lognormal failure distributions at different temperatures b)Plot of ln(MTF) Vs. 1/T for determining E_a

Temperature (t) (°C)	MTF (hrs.)	X= 1/T = (1/t +273) (1/°K)	Y= ln(MTF)	Slope(m)	E_a=m * k_B (eV)
300	561.51	0.001745	6.33063	10023	0.86
325	250.70	0.001672	5.5242		
350	138.23	0.001605	4.9289		

Table 4.1: E_a calculation

Current density exponent (n) for M-2 test structure

Current density exponent (n) was determined for M-2 test structure based on electromigration tests performed with current density of 0.8 MA/cm^2,1.2 MA/cm^2 and 1.5 MA/cm^2 (at a fixed temperature of 350°C). Lognormal cumulative failure distributions at different temperatures are shown in **Figure 4.3a**. MTF values were obtained from the lognormal plot and n was found using the Black's equation [36]. Activation energy was obtained from the slope of line plotted by ln(MTF) versus ln(j), where j is the current density (**Figure 4.3b**). Calculations for obtaining n are illustrated in **Table 4.2**. For other structures n was found similarly. Current density exponent (n) was found to be around 1.21 for both 0.28 μm and 1.28 for 0.7 μm wide test structures.

Effect of width

Although 0.28 μm and 0.7 μm wide structures had different width of the trench, via dimension was the same (0.26 μm), for both M-1 as well as M-2. It was interesting to note that the 0.28 μm and 0.7 μm wide structures in case of M-2 showed similar MTFs, while there was reduction in MTF for wider test structure in case of M-1 as illustrated in **Figure 4.4**.

Failure analysis of M-1 and M-2 test structures

FIB cross-section image of 0.28 μm wide M-2 test structures failed by gradual mode are shown in **Figure 4.5.** Void formed due to electromigration was found to be located at the top portion of the via and trench. It can be seen that void seems to be nucleated at the Cu/dielectric interface above the via and then grow along the Cu/dielectric-cap interface of the trench. Completely different failures were observed in M-1 test structures. FIB images of M-1 test structures failed by abrupt mode are shown in **Figure 4.6.** The void is found to be located just below the via liner and seems to grow along the Cu/dielectric cap interface. But a small void formed below the via causes the via to open and correspondingly sudden resistance increase.

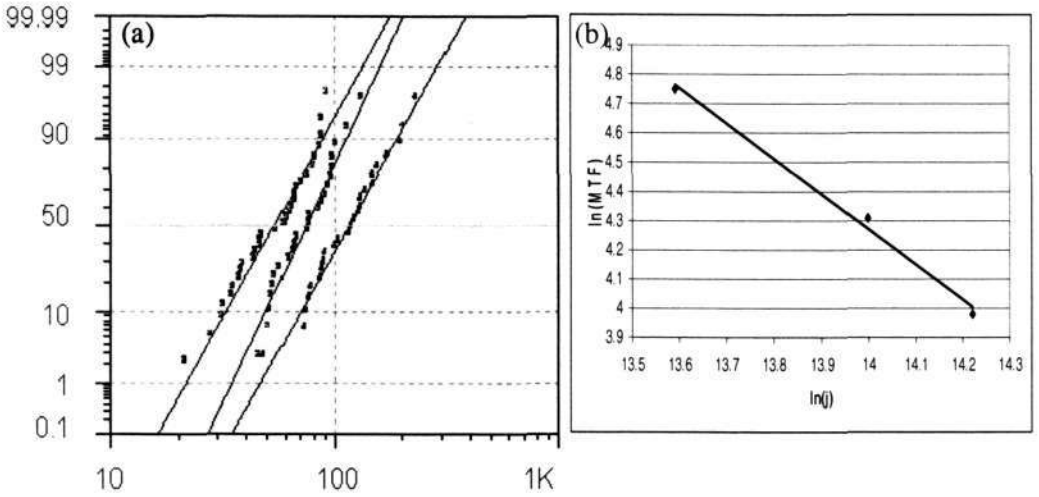


Figure 4.3: a) Lognormal failure distributions at different current densities
b) Plot of ln(MTF) Vs. ln(j) for determining n

Current density (j) (MA/cm^2)	MTF (hrs.)	X= ln(j)	Y= ln(MTF)	Slope(m)	n=-m
0.8	115.78	13.592	4.751	-1.210	1.21
1.2	74.33	13.997	4.308		
1.5	53.56	14.220	3.890		

Table 4.2: n calculation

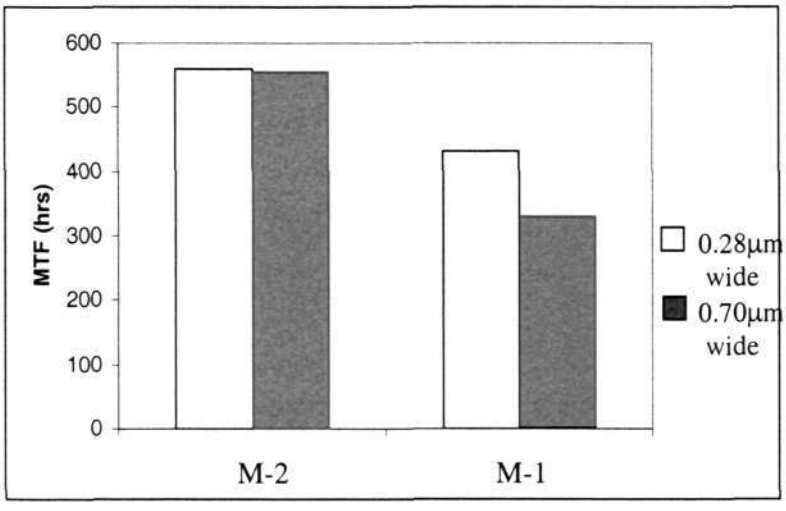


Figure 4.4: Width dependence of MTF in M-1 and M-2 structures

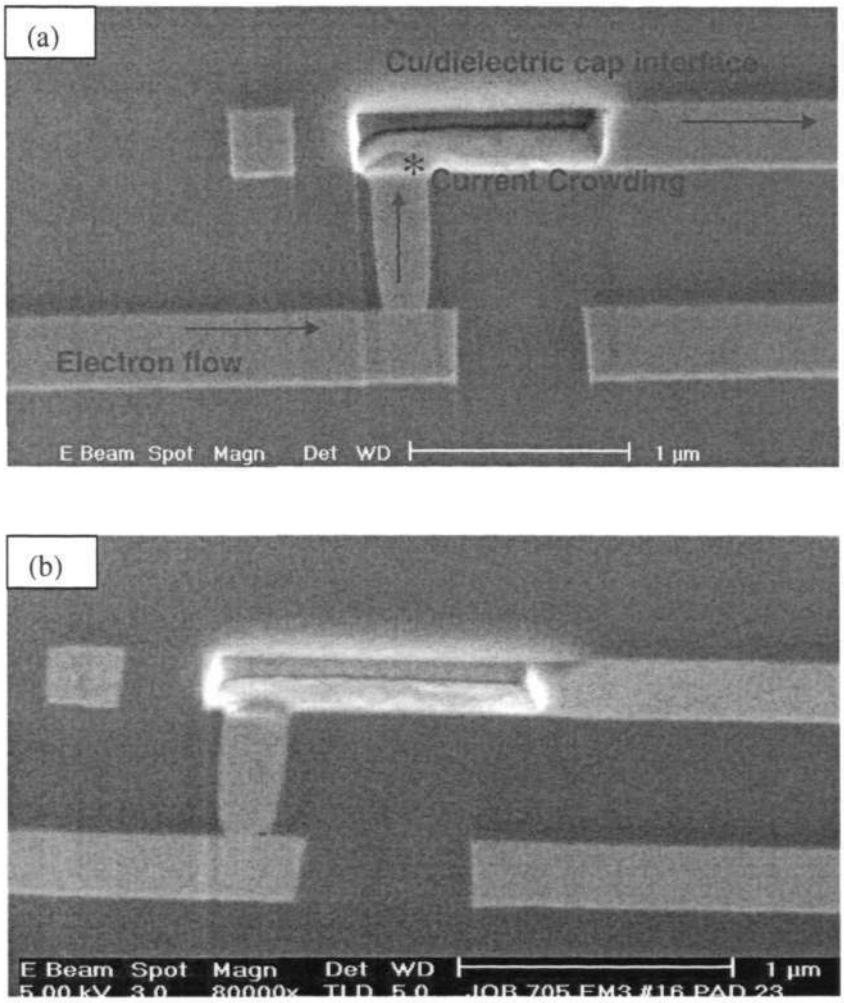


Figure 4.5: FIB cross-section images of M-2 test structures

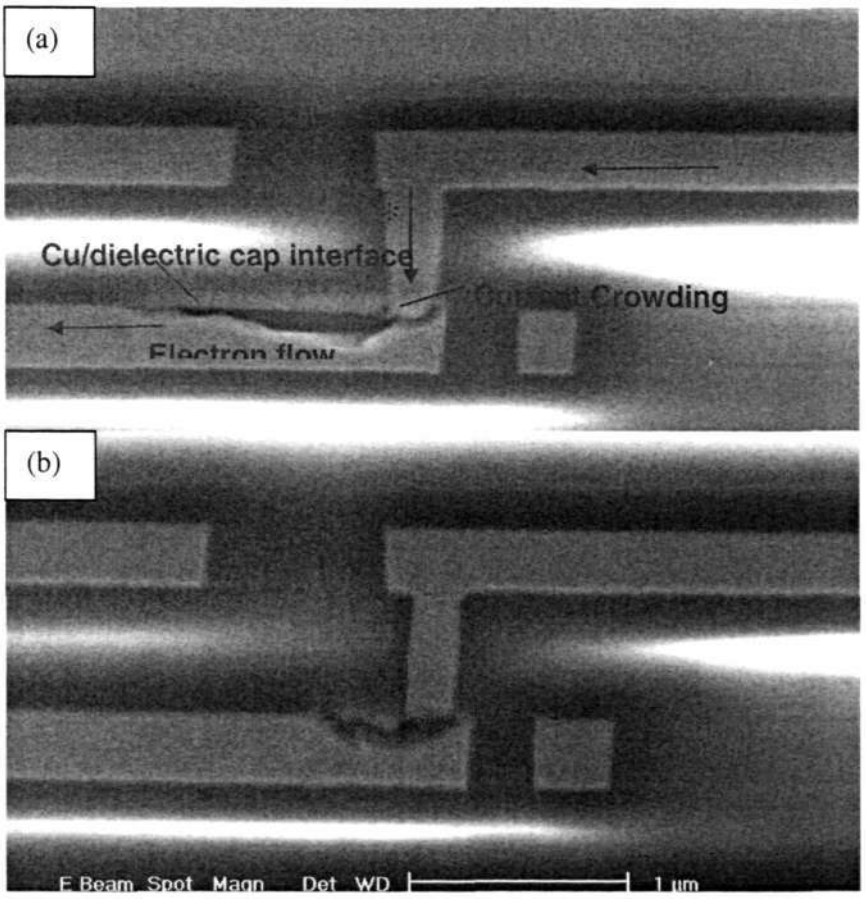


Figure 4.6: FIB cross-section images of M-1 test structures

4.1.2 Short length effect

The log normal probability plot of failure times for M-2 and M-1 test structures with metal lines of different lengths are shown in **Figure 4.7a and b** respectively. As expected, due to back-stress, the shorter length structures showed higher lifetimes. Interestingly M-2 structures showed significantly bi-modal failures with the reduction in length. As the length was reduced from 100 μm to 50 μm, the early failures (<50%) showed only slightly higher failure times, but the late failures (>50%) exhibited much higher failure times. Bi-modal failures were not observed for 20 μm length structures, however, the failure times were significantly longer than for 100 μm and 50 μm length structures and almost 50% of samples did not fail even after 2000 hr. On the other hand, in this case of M-1 structures, slightly higher failure times were observed for 50 μm length structures than for 100 μm length structures, but bimodal failures were not observed. For 20 μm length structures, early failures (<50%) showed significantly higher failure times (increased by an order) and 40% of the samples did not fail. Failure analysis of short length M-2 structures showed that via-bottom and line failure modes were observed as shown in **Figure 4.8** along with the typical via-top failures (**Figure 4.9**). However, mainly the typical voids at Cu/dielectric cap interface near the bottom of the via were observed for short length M-1 structures (**Figure 4.10**).

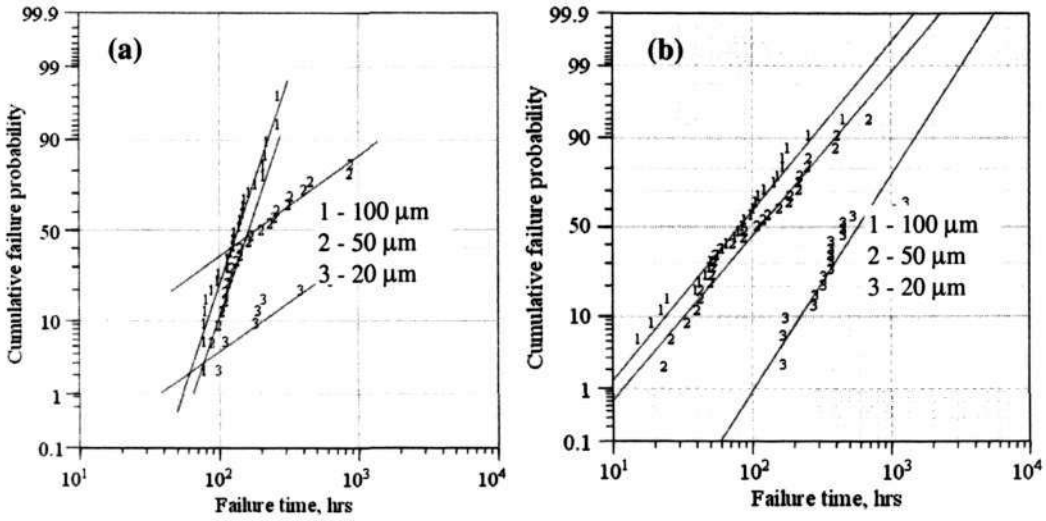


Figure 4.7: Lognormal plot of time to failure for (a) M-2 and (b) M-1 structures with different line lengths

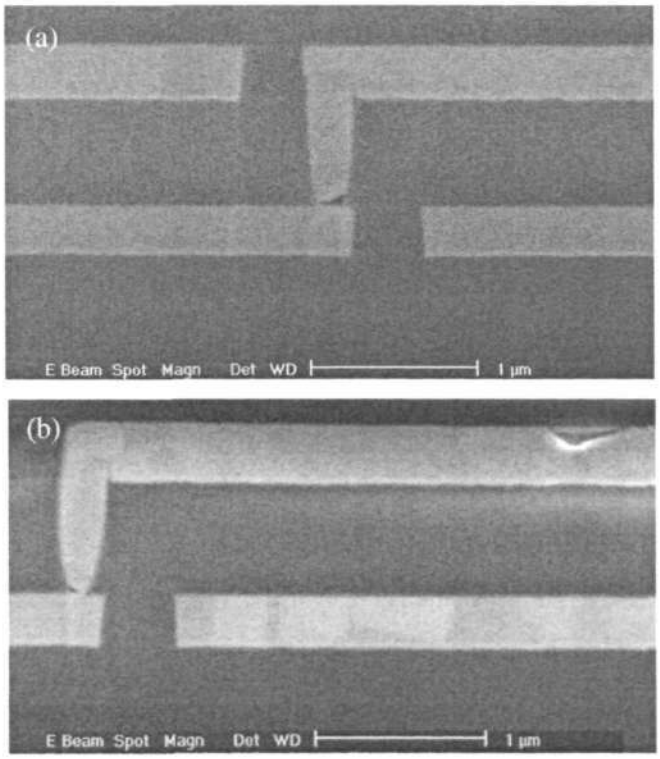


Figure 4.8: Failures in short-length M-2 structures (a) via bottom failures (b) line failures

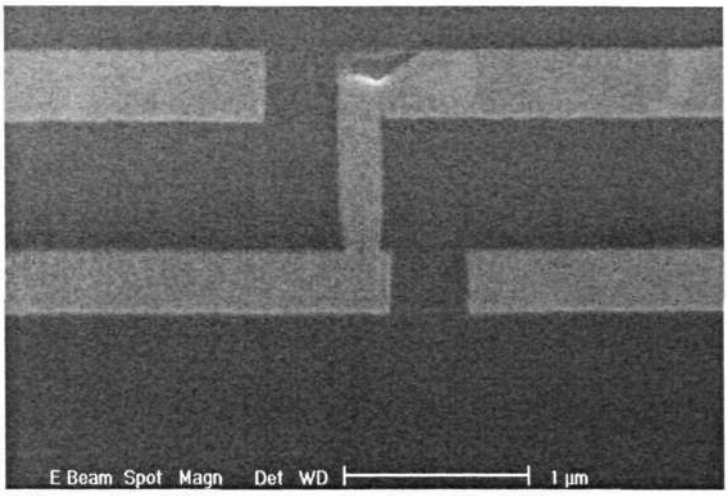


Figure 4.9 : Via-top failure in short-length M-2 structures

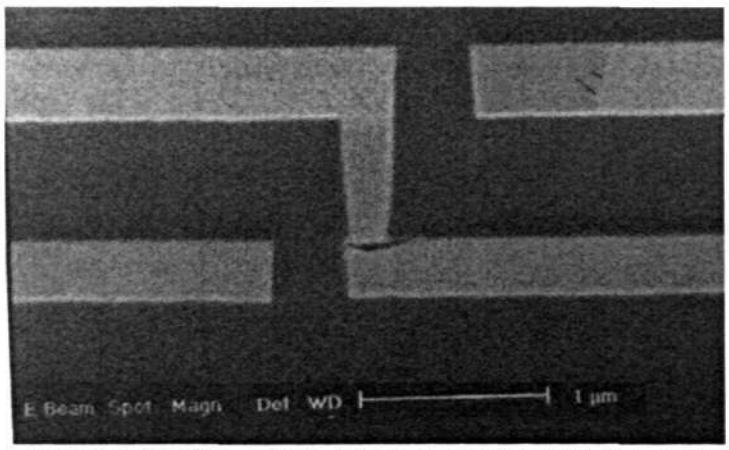


Figure 4.10 : Via-bottom failure in short-length M-1 structures

4.1.3 Microstructure:

Bamboo-like microstructure in the test structure trenches can be verified based on **Figures 4.11**. FIB cross section (along the length of the trench) image revealing bamboo-like grain structure is shown in **Figure 4.11a.** The length of the grains can be seen to be comparable or larger than the line-width. One cross section at the comb structure revealed many trench cross sections as shown in **Figure 4.11b**. Typical TEM micrograph of trench cross section is shown in **Figure 4.11c.** No grain boundary can be seen at the cross section. Most of the trench cross-sections did not show grain boundaries. This suggests the "super-filling" of trenches by electroplating used for Cu deposition [63]. Such a bamboo-like grain structure is ideal for the study of interfacial electromigration. These are preliminary investigations which are sufficient to only re-confirm presence of bamboo-like microstructure in Cu damascene trenches.

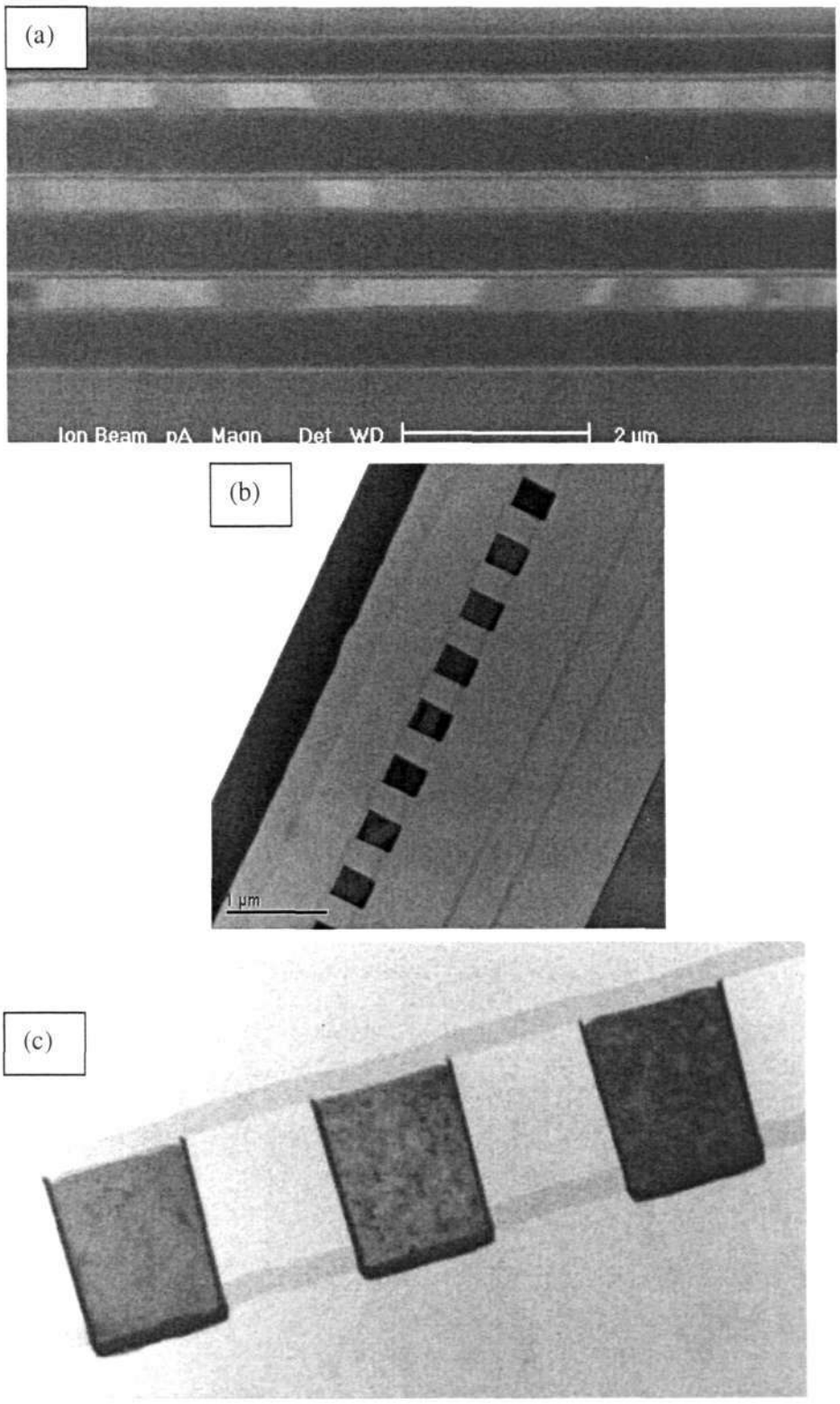


Figure 4.11: Microstructure in trenches -a) FIB cross section image b) and c)TEM cross section

4.1.4 Effect of surface treatment on electromigration

Effect of surface treatment on upper(M-2) and lower(M-1) layer dual-damascene structures.

The lognormal plot of failure times of M-2 layer structures with different surface treatments are shown in **Figure 4.12**. It is clearly observed that the electromigration failure times are improved due to surface treatment. NH_3 treated samples showed slightly higher failure times as compared to control samples with no surface treatment. Significant improvement was observed for hydrogen plasma and silane treatment structures. Similar trend in electromigration performance **(Figure 4.13)** was observed for M-1 layer structures similar to M-2 structures. Hydrogen plasma and silane treatment showed significantly reduced early failures. FIB cross section images of M-2 and M-1 structures after failure are shown in **Figures 4.14** and **4.15** respectively. In both these cases, typical void location along the Cu/dielectric cap interface near cathode via were observed for both M-2 and M-1 structures.

Effect of surface treatment on single layer damascene test structures

The cumulative distribution of failure times of NIST test structures with different surface treatments is shown in **Figure 4.16.** Significant difference in failure times was not observed as in case of M-2 and M-1 dual-damascene structures.

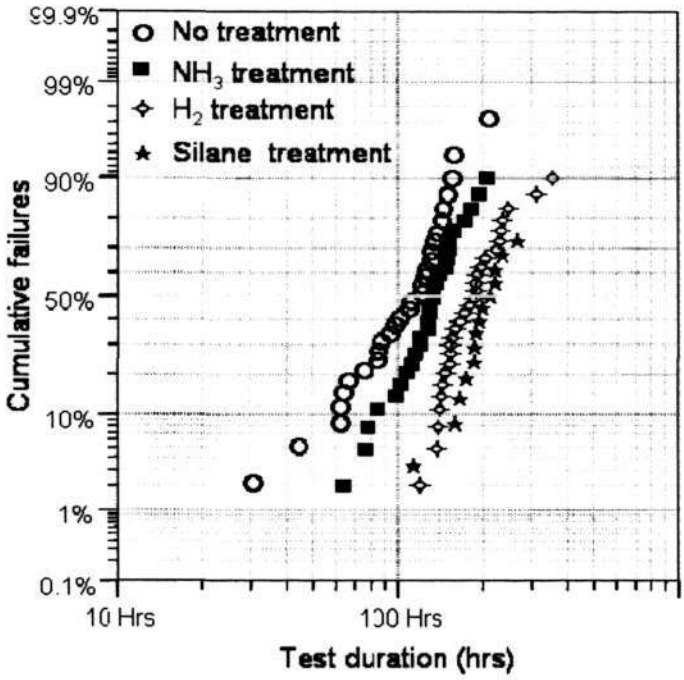


Figure 4.12: Lognormal plot of failure times of upper (M-2) layer test structures with different surface treatments

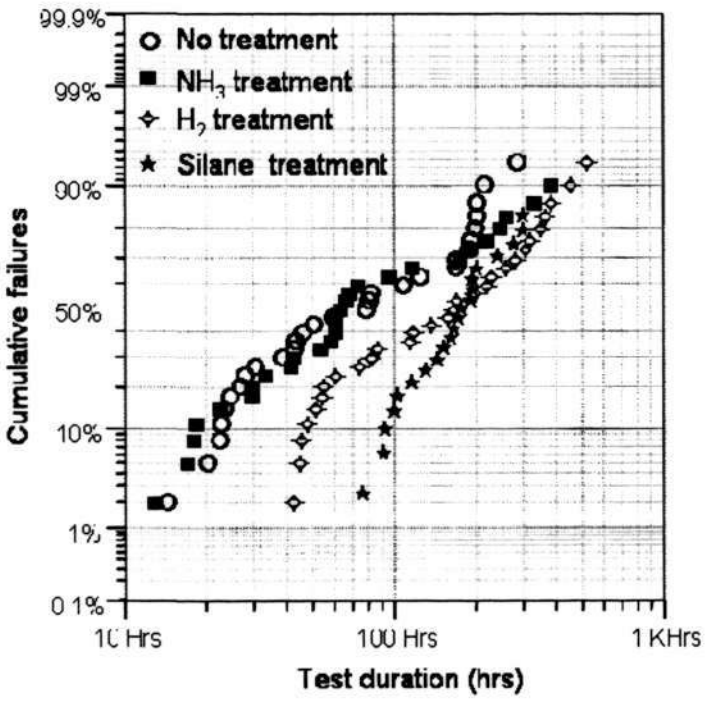


Figure 4.13: Lognormal plot of failure times of lower (M-1) layer test structures with different surface treatments

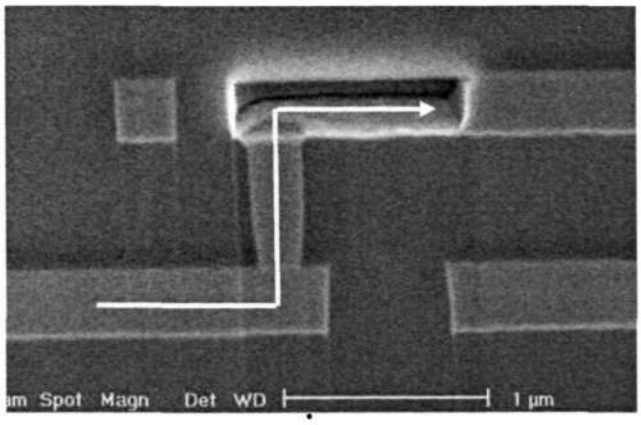


Figure 4.14: FIB cross section image of upper (M-2) layer test structures

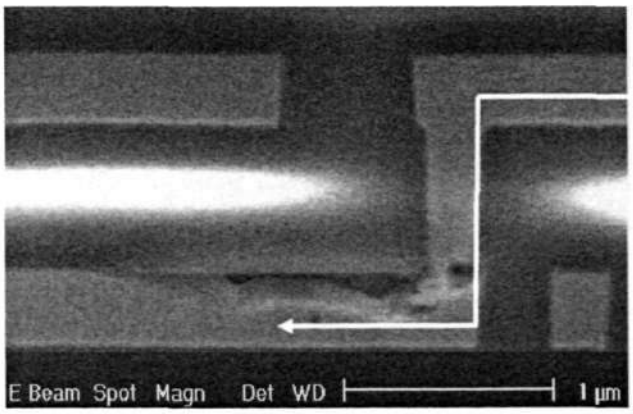


Figure 4.15: FIB cross section image of lower (M-1) layer test structures

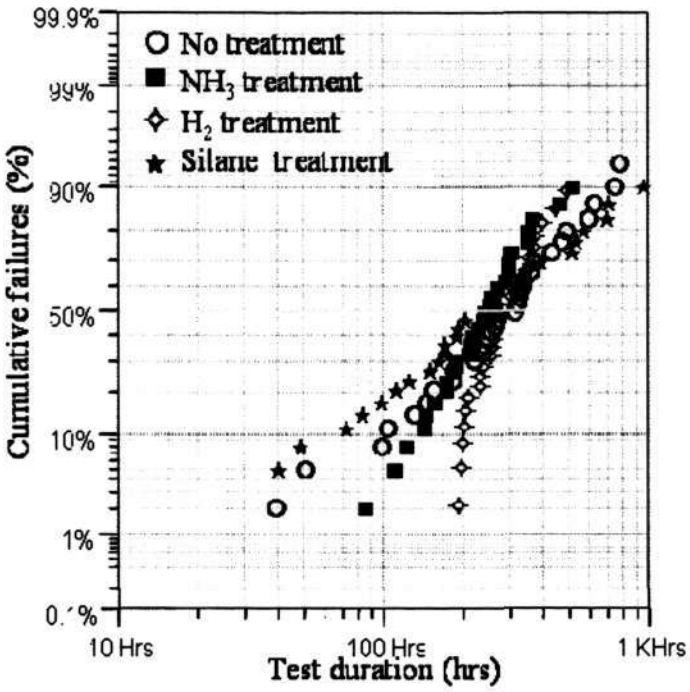


Figure 4.16: Lognormal plot of failure times of single layer test structures with different surface treatments

4.2 *In-situ* characterization of upper (M-2) and lower (M-1) layer dual-damascene structures

Some frames of SEM secondary electron images of one of the M-1 structures at the cathode-via region at various time intervals during electromigration stressing as well as the resistance trace are shown in **Figure 4.17a** and **b**. The void first emerged at the Cu/Si_3N_4 interface at a considerable distance from the cathode via in the M-1 line and moved along this interface towards the cathode end as shown in **Figure 4.17a**. The voids agglomerated near the via bottom along the Cu/Si_3N_4 interface leading to a sudden jump in resistance (as it can directly open the via), and finally grew further to cause opening of the entire via leading to via burn-out. Similarly, in the case of the M-2 structure, the void nucleated at the Cu/Si_3N interface of the M-2 line at some distance from the via corner as shown in **Figure 4.18.** The void agglomerated at the top corner of the M-2 line and its further growth towards the via caused an abrupt resistance increase (**Figure 4.18**). Interestingly, void trapping at the grain boundary during movement along the Cu/dielectric cap interface was observed during *in-situ* characterizations and there seem to be a critical size for the void to be freed from the grain boundary because once trapped at the grain boundary, the void was observed to be moved away from the grain boundary only after coalescence with other voids. An isolated void was observed during in-situ electromigration characterization of one of the test structures as shown in **Figure 4.19,** which indicates mechanisms of void growth, coalescence and trapping.

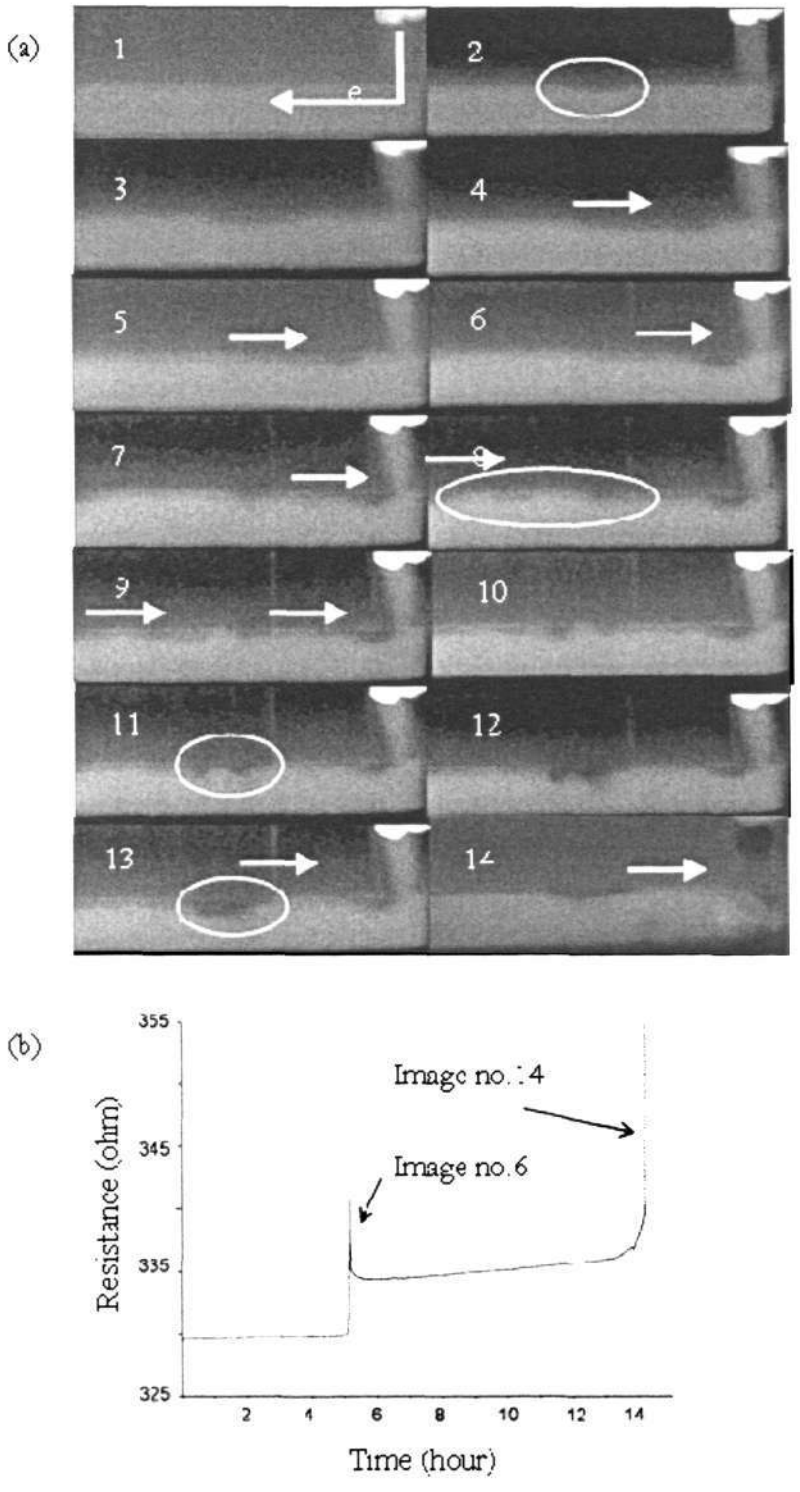


Figure 4.17: (a) SEM of images of the cathode via region of M-1 test structure at various time intervals during *in-situ* electromigration characterization (b): Resistance trace of the M-1 structure shown in Fig.(a)

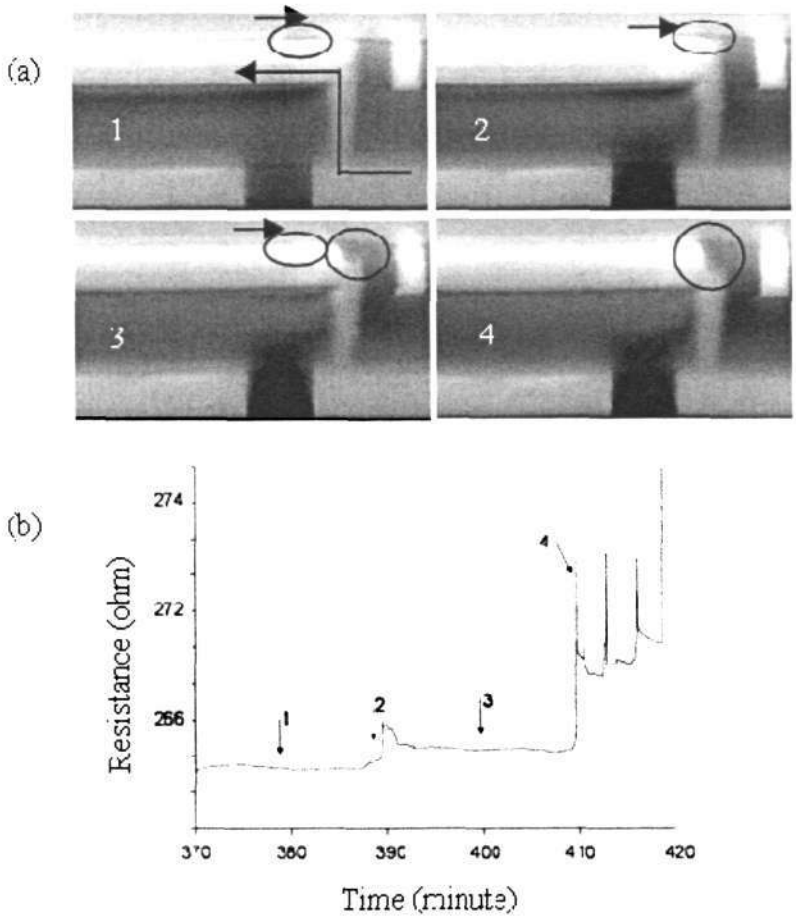


Figure 4.18 (a): SEM of images of the cathode via region of M-2 test structure at various time intervals during *in-situ* electromigration characterization (b): Resistance trace of the M-2 structure shown in Fig.(a)

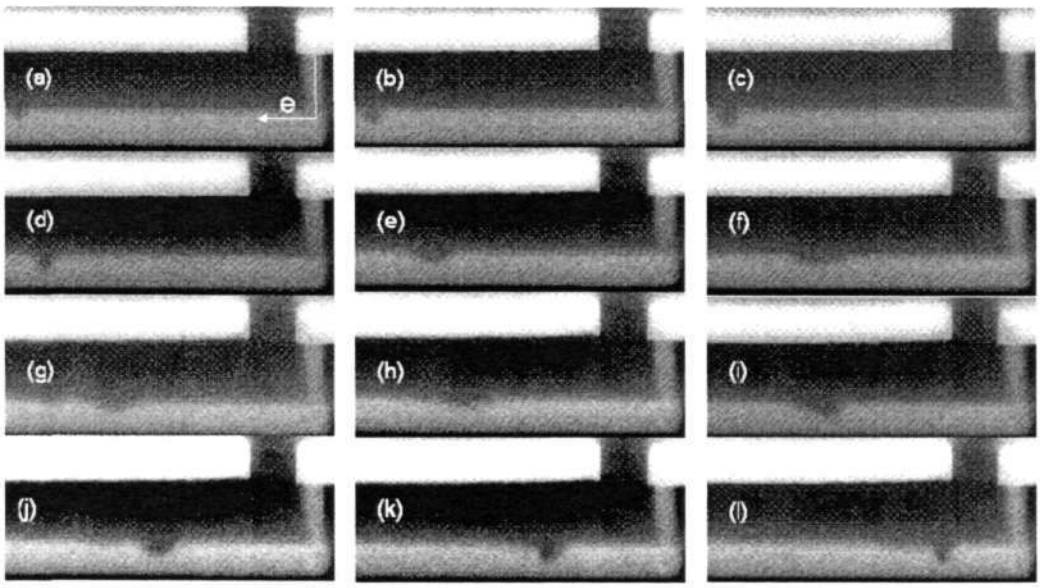


Figure 4.19: An isolated void observed during in-situ electromigration characterization of one of the M-1 test structures: void growth (a)-(c), void movement (d)-(e), void trapping (f), void agglomeration (g)-(i), void movement (j)- (l).

4.3 *In-situ* characterization of dual-damascene interconnect tree structures

Some frames of SEM images of the middle via of an interconnect tree structure stressed in configuration (i) (no current in left segment, refer Figure 3.10) are shown in **Figure 4.20**. The middle via region before starting electromigration stressing is shown in **Figure 4.20a**. Voids were observed to emerge at the Cu/SiN_x interface in the test line away from the via (**Figure 4.20b**) and move towards the via in opposite direction to electron flow. Void movement and agglomeration at the middle via region was observed as shown in **Figure 4.20c-f**. A void was formed at the Cu/SiN_x interface above the middle via and it moved slightly towards the left segment. However, the void neither moved further nor grew continuously. The void size was increased to span the via region only after agglomeration of additional voids moving along the Cu/SiN_x interface leading to failure of the right segment. The left segment of the interconnect tree also showed an open circuit after test.

For the case of configuration (ii), in which the current flowing in the left segment was in the same direction as the right segment (refer Figure 3.10), the void evolution was observed as shown in **Figure 4.21.** The voids which agglomerated at the middle via region of the right segment moved further into the left segment. In this test, the left segment failed earlier than the right segment. Furthermore, as the current in the adjoining left segment was reversed (configuration (iii), refer Figure 3.10), the voids moving along the Cu/SiN_x interface in both the segments converged at the middle via region as shown in **Figure 4.22**. While for some samples, void from only one of the segments agglomerated at the middle via as shown in **Figure 4.23**. Interesting void shape evolution at middle via region was observed for this case as shown in **Figure 4.23**. In this case, the void (agglomerated at middle via region from the left segment) sneaked into the middle via from the left side edge of the via.

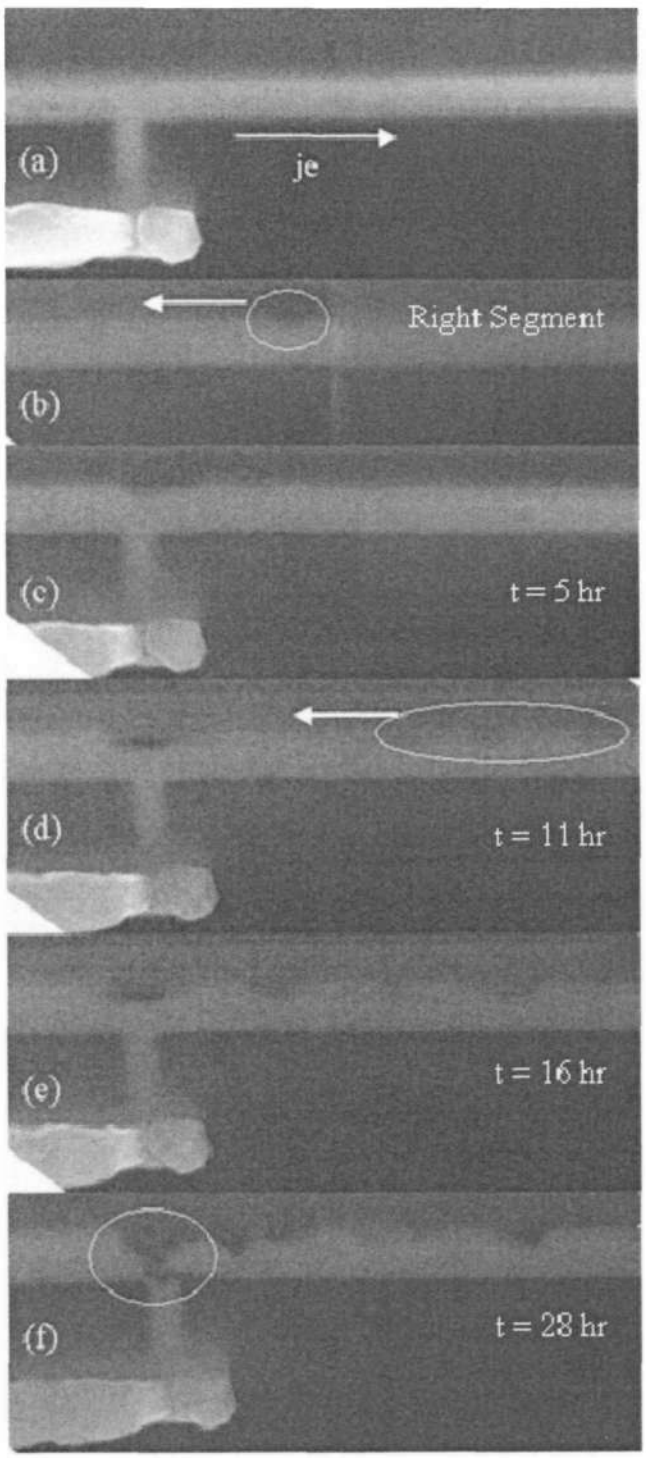


Figure 4.20: SEM images of the middle via region at various time intervals for configuration (i)

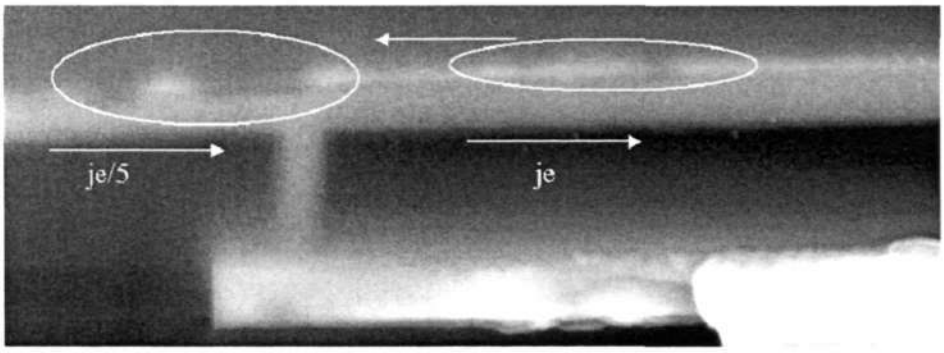


Figure 4.21: SEM image showing void agglomeration at middle via region for configuration (ii)

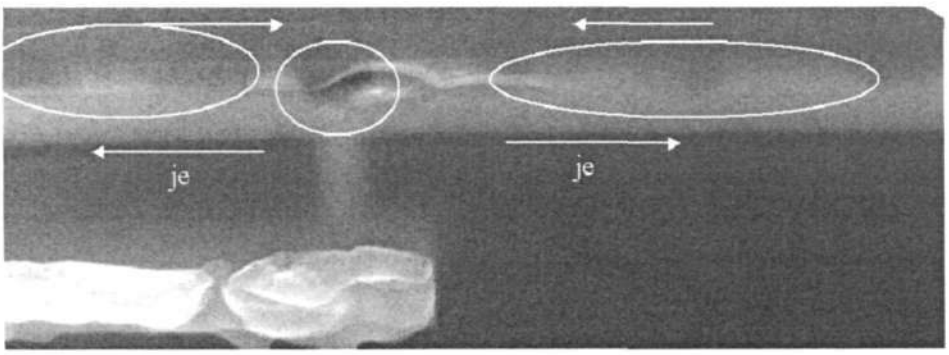


Figure 4.22: SEM image showing void agglomeration at middle via region for configuration (iii)

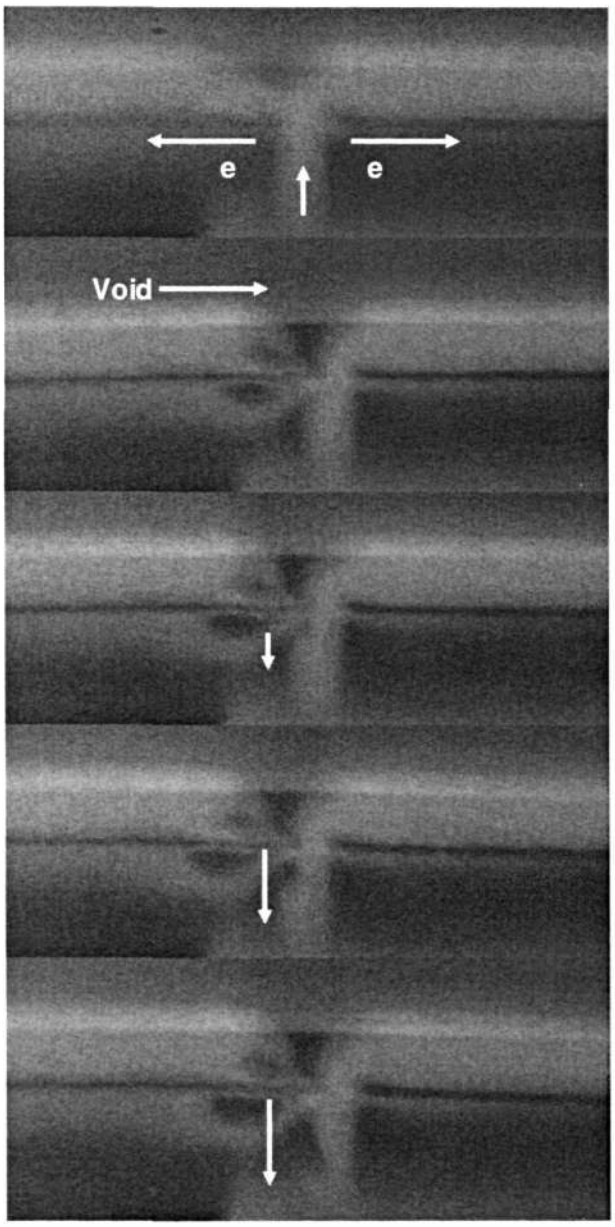


Figure 4.23: SEM images showing void evolution in the middle via region for configuration (iii)

Chapter Five

Discussion

5.1 Electromigration in upper (M-2) and lower(M-1) layer dual-damascene structures

Activation energies & current density exponent:

The activation energies were found to be 0.85 eV and 0.88 eV for the 0.28 μm and 0.7 μm wide M-2 test structures respectively. However, for M-1 test structures, the activation energies were observed to be 0.49 eV and 0.6 eV for 0.28 μm and 0.7 μm wide test structures respectively. The low activation energies (<1.2 eV) indicate interfacial diffusion dominated electromigration [56]. It is interesting to note that the activation energies for both 0.28 and 0.7 μm lines were nearly equal for the M-2 test structure; whereas, the data suggests a line-width influence on activation energies for the M-1 test structures. Observed n values of 1.2 are consistent with the reported values for similar test structures [62, 67].

The observed activation energies in M-2 structure were almost similar and are consistent with the previously reported activation energies for similar structures [20,66,67]. Lower activation energies were found for M-1 test structures. These activation energies are less than the Cu grain boundary activation energy (1.2eV) indicating interface dominated electromigration. Drawing such inference directly, based on only the value of the observed activation energy may not be proper as various activation energies are reported for electromigration in Cu and possibility of coupled grain boundary and interface diffusion can not be denied. But the observed void location and growth along Cu/dielectric interface indicates interface diffusion. The bamboo-like microstructure in the trenches and "super-filling" of trenches observed in TEM cross-section images, further support this argument.

Void location

In the M-2 test structure, voids seem to have nucleated at the Cu/dielectric interface above the vias and then grew along the Cu/dielectric-cap interface of the M2-trench. Similarly for the M-1 test structure, the electromigration induced void was observed at the Cu/dielectric cap interface. This supports the premise that

electromigration is interfacial diffusion dominated; which is also indicated by the observed low activation energies. Grain boundaries as diffusion pathways are likely to have played a negligible role because of the bamboo-like microstructure in damascene trenches.

Asymmetric behavior of upper(M-2) and lower(M-1) layer dual-damascene structures

The Ta liner at the via-bottom is a flux divergence site for both M-1 and M-2 test structures. For the M-2 test structure, voids would be expected to form just above the via-bottom Ta liner at the cathode end where electrons move from a wider M-1 line into the via. These voids near the via-bottom were found in early failures, but these can be eliminated by via process optimization [67]. As voids were not found at the via bottom in our studies, we infer that the via process was robust. Instead voids were found at the Cu/dielectric interface.

The void location can be explained based on the diffusion of atoms due to vacancy wind [59]. The mass transport of Cu along the M-2 surface in the applied electric field by adatom or vacancy mechanisms generates excess vacancies and these excess vacancies easily migrate through Cu. Recently, current crowding was shown to induce vacancy flux from a high current density region to a low current density region [128-130]. If this argument is applied to void formation in the case of M-2 test structures, the vacancies should accumulate at the low current density corner above the via. The observed void location and shape are consistent with this argument. However, if the same argument is applied to the M-1 test structure, the void should be formed at the low current density region at the corner of Cu/ trench bottom-Ta liner interface below the via. But the void location both below the via and along the top dielectric interface and slit-like shape are contrary to the current crowding effect. Reduced peak current due to Ta layer [130] might have led to reduction in current crowding effect in M-1 structures. In addition, the peak current density in the M-1 test structure is at the weak Cu/dielectric cap interface unlike the Cu/Ta interface in the M-2 structure. This coupled with the possibility that the via-bottom area may have an inherent weakness, attributable to potential damage during

the dual-damascene etch and clean steps, may provide an opportune site for void nucleation.

For M-1 test structures with 0.7 μm width (and same line current density) a ~25% reduction in MTF was observed as compared to 0.28μm wide structures. On the other hand, a similar width effect did not exist for the M-2 test structures. As the same via dimension and current density in trench was used, the actual current flowing through the wider line and thus the peak current density due to current crowding was expected to be higher for 0.7 μm-wide test structure. In case of M-1 test structures the peak current density is near the weak Cu/dielectric interface. In case of the wider M-1 structures, peak current densities will be more significant and these higher current densities will cause enhanced nucleation of voids at this location and should lead to reduced MTFs. Yet another explanation of the lower MTFs of wider M-1 lines could be based on a recent literature [131] that investigates stress-induced voiding under vias connected to wide Cu metal lines, and proposes that wider lower layer lines can provide larger supply of vacancies for voiding. If a similar argument is applied for electromigration induced voids in the lower layer M-1 test structures, wider lower layer should be more prone to formation of voids under the via.

Similar to the observations in the M-1 structures, higher current densities must be produced in wider M-2 test structures. However, a width effect on MTF was not observed. This could be because of the peak current densities being located away from the weak Cu/dielectric interface. According to the theory of vacancy flux due to current crowding [128], for the same thickness of lines, with peak current density being higher in 0.7 μm M-2 structure than in 0.28 μm structure, there should be higher driving force due to a larger current density gradient. This should lead to lower MTF for wider M-2 line, but both the lines show similar MTFs. Thus the void location and MTFs cannot be completely explained by vacancy flux due to current crowding. Weak Cu/dielectric-cap interface acting as preferential nucleation site and vacancy sink, can explain these results.

5.1.2 Short length effect in upper(M-2) and lower(M-1) layer structures

As expected, due to back-stress, the shorter length structures showed higher lifetimes. Interestingly they showed significantly bi-modal failures with the reduction in length. As the length was reduced from 100 μm to 50 μm, the early failures (<50%) showed only slightly higher failure times, but the late failures (>50%) exhibited much higher failure times. This indicates that there are two failure mechanisms for 50 μm length test structures. However, for 20 μm length structures, the failure times were significantly longer than for 100 μm and 50 μm length structures and almost 50% of samples did not fail even after 2000hr. The slope of lognormal plot for the late failures in 50 μm length is almost parallel to that of 20 μm length indicating a possibility of similar failure mechanism. The observed failures could be explained by the consideration of the 'back stress' effect and preferential void nucleation sites in M-2 structures. The typical void formation at Cu/dielectric cap interface above the via is effectively suppressed due to the back-stress effect. But in case of M-2 structure, the Ta barrier at via bottom is a flux divergence site and can serve as a void nucleation site when the void formation at Cu/dielectric cap interface is suppressed by back-stress effect. Also, the next point of weakness which could be in the line may cause the line electromigration failure mode to surface. Such via-bottom and line failure modes were observed for short length M-2 structures as shown in **Fig.4.8** along with the typical via-top failures (**Fig. 4.9**). Similar shift in the void location to via bottom was observed when the Cu/dielectric cap interface diffusion was suppressed by surface coating [95]. Thus the interplay of these void nucleation mechanisms in M-2 structures leads to bi-modal failures in response to short length effect.

Completely different short length effect was observed for the M-1 test structures. In this case, slightly higher failure times were observed for 50 μm length structures than for 100 μm length structures, but bimodal failures were not observed. For 20 μm length structures, early failures (<50%) showed significantly higher failure times (increased by an order) and 40% of the samples did not fail. The slope of lognormal plot was almost similar to 50 and 100 μm length structures, indicating similar failure mechanism. This is contrary to electromigration behavior of 20 μm

length **M-2** structure, in which the mechanism indicated by the slope was entirely different from 50 and 100 μm length structures. Failure analysis shows that all failures occurred near the Cu/dielectric cap interface near the bottom of the via (**Fig. 4.10**). The back stress due to the shorter line lengths seemed to be insufficient to overcome the interfacial weakness and thus leading to an insensitivity of failure mechanisms to line lengths when the length was reduced from 100μm to 50μm. But as the length was reduced to 20μm, a significant increase in lifetime was observed and 40% of the samples remained un-failed. This indicates that void formation at Cu/dielectric cap interface below the via in case of lower layer structures can be effectively suppressed by the back-stress effect.

The observed electromigration behavior is due to peculiar dual-damascene architecture and Cu/dielectric cap interface acting as vacancy sink and preferable nucleation site. Short length effect is complicated in dual-damascene Cu interconnects, contrary to the direct effect observed in Al and W-plug Cu interconnects. These observed phenomena are specific to the Cu dual-damascene structures and will continue to have major technological implications for electromigration reliability assessment of dual-damascene interconnects.

5.1.3 Effect of surface treatment on electromigration performance

Effect of surface treatment on upper (M-2) and lower (M-1) layer dual-damascene structures.

In case of M-2 structures, it is clearly observed that the electromigration failure times are improved due to surface treatment. NH_3 treated samples showed slightly higher failure times as compared to control samples with no surface treatment. Significant improvement was observed for hydrogen plasma and silane treatment structures. Contrary to concerns over electromigration behavior of lower layer structures [61,132], it was observed that the surface treatments improved electromigration performance of lower layer structures similar to M-2 structures. Hydrogen plasma and silane treatment showed significantly reduced early failures. In both these cases, the electromigration induced void location bordered the Cu/dielectric cap interface and voids were not observed near the Cu/Ta interfaces.

Electromigration performance has been found to be directly correlated to adhesion between Cu and the dielectric cap layer [86]. We suggest that the surface treatments modify the Cu/dielectric cap interface leading to change in adhesion between Cu and dielectric cap, which in turn influences the Cu/dielectric cap interface dominated electromigration. NH_3 treatment is reported to cause the reduction of copper oxide as well as formation of CuN leading to a better Si_3N_4 interface [133,134]. Hydrogen plasma treatment is known to form hydride on the Cu surface with no change in microstructure [135,136] and to clean the Cu surface [135] providing better adhesion between Cu and subsequently deposited Si_3N_4 dielectric cap layer. Improvement in electromigration performance due to hydrogen has also been attributed to interfacial segregation of hydrogen and the reduction of defects by athermal annealing [137,138]. Thus, the observed improvement in H_2 treated samples may have been contributed by formation of hydrides or reduction of Cu oxide with consequent better adhesion. Improvement due to silane treatment may be attributed to silicide formation on the Cu surface [139]. Microstructural changes arising from surface treatment cannot be completely ruled out, but this change and its effect on electromigration is likely to be less significant since the grain structure was stabilized

due to post-Cu deposition anneal and TEM and FIB images (**Figure 4.11**) suggest bamboo-like grain structure with large grains.

The observed improvement in electromigration performance due to surface treatment supports Cu/dielectric cap interface dominated electromigration mechanism. It is interesting to consider how Cu/dielectric cap interface modification affected electromigration in M-2 and lower layer dual-damascene structures. The different electromigration performance of M-2 and lower structures has been explained to be due to different electromigration mechanism in these structures [8]. It is proposed that the location of maximum stress in case of M-2 structures is at the Cu in the cathode-end via which is surrounded by Ta on all sides, while for lower layer structures is at the Cu/dielectric interface near the cathode-end via bottom where void can be easily nucleated, leading to a shorter lifetime of lower layer structures. However, in our study of electromigration mechanism in M-2 and lower layer structures [23] using in-situ SEM characterization technique [24], the electromigration mechanism in both the M-2 and lower layer structures seems to be similar in that the Cu/dielectric interface facilitates the heterogeneous nucleation of voids and also provides a path for void movement [*This mechanism will be explained in subsequent section*]. In both the structures, voids were found to be nucleated at the Cu/dielectric interface in the line, away from the via, and move along this interface towards the cathode end, where they agglomerate to form a void and cause electrical opening of the via. These observations suggest that the electromigration performance of both M-2 and lower layer structures can be improved by improving Cu/dielectric cap interface. Improved electromigration performance of both M-2 and lower layer structures with modification of Cu/dielectric cap interface due to surface treatments support this mechanism.

Effect of surface treatment on single layer damascene test structures

Different electromigration behavior was observed in case of single layer test structures. Significant difference in failure times was not observed as in case of M-2 and lower layer dual-damascene structures. This different behavior of single layer structures can be explained based on the mechanism of void nucleation and movement along the Cu/dielectric cap interface [*This mechanism will be explained in*

subsequent section]. The void nucleated at Cu/dielectric cap interface in the test line move towards the cathode end along Cu/dielectric cap interface, but unlike via-fed M-2 or lower layer structures, there is no site like the via where the voids can agglomerate at the cathode end. The large pads that are connected to the ends of the test line can serve as sink for the voids. This leads to no significant difference in failure times during electromigration test, although the Cu/dielectric cap interface was modified.

5.2 Electromigration mechanism in standard dual-damascene structures revealed by *in-situ* SEM characterizations

Although most of the studies on electromigration in Cu damascene interconnects have shown that the Cu/Si_3N_4 cap interface is the dominant electromigration path [10,59,62,66,68,123], some have reported grain boundary diffusion to be dominant [124-125] and have interpreted electromigration in Cu interconnects by coupling grain boundary and interface diffusion [52]. Others have indicated that the Cu/liner interface is the fast electromigration path [94]. Moreover, contrasting electromigration behavior of M-2 and M-1 dual-damascene structure was found[61], and the effect of line width and length on electromigration was determined in the initial part of this study **(Sections 4.1 and 5.1)**. But the exact details of electromigration mechanism in dual-damascene structure were not completely understood. Due to the technological importance of dual-damascene Cu interconnects, it was necessary to understand the exact electromigration mechanism in these structures. By employing the *in-situ* SEM electromigration characterization technique, we were able to unravel the electromigration mechanism in Cu dual-damascene interconnect structures.

The electromigration-induced void evolution in M-2 and M-1 structures was revealed by *in-situ* SEM characterization. The observed electromigration behavior supports the premise that the Cu/Si_3N_4 cap interface acts as the fast electromigration path, but it contradicts previously proposed electromigration mechanisms in damascene interconnects[34,61,66,68,123,128]. The different electromigration behavior between M-1 structures and M-2 structures was proposed to be based on the location of maximum tensile stress developed during electromigration at the cathode end via bottom Ta barrier, which acted as the blocking boundary for Cu atom diffusion[61]. The void forms if the critical stress for void nucleation was reached. It was argued that in the case of M-2 structures the maximum tensile stress was reached at the base of the via where Cu was bounded by Ta on all sides whereas for the M-1 structure, the void nucleation site was thought to be at the Cu/dielectric cap interface near the via bottom due to the peak tensile stress which then grew along this interface. But this is contrary to the *in-situ* observation shown in **Fig. 4.17 (a)**, which

shows that the voids nucleated at the Cu/Si_3N_4 interface in the M-1 line, away from the via instead of the Cu/Si_3N_4 interface at the via. Subsequent to nucleation, the voids move along the Cu/Si_3N_4 interface, and agglomerated at the Cu/Si_3N_4 interface near the via bottom. It can be inferred from the *in-situ* observations that the contrasting behavior of M-1 and M-2 structures is because of the structural differences. In both structures voids nucleate at the Cu/Si_3N_4 interface *away from the via* and *move* along the Cu/Si_3N_4 interface *in the direction opposite to electron flow*. But in the case of M-1 structure, the voids agglomerate directly below the via bottom in a high current density region, which can cause an electrical open quickly. It is interesting to note that in some reports[66,68,123,140] voids were observed to be at Cu/Si_3N_4 interface *away from the via* for some of the samples (**Figure 5.1**), but these were ignored and not enough explanation is provided. Actually these voids must be the voids that were nucleated at the Cu/Si_3N_4 interface away from the via and moving towards the cathode end, according to the proposed mechanism in this thesis.

It is interesting to consider here the recently proposed current crowding induced vacancy flux mechanism[128]. It proposed that the vacancy flux induced by electromigration goes from the high current density region to the low current density region. Accordingly, the void should nucleate at the bottom corner of the cathode end of M-1 line and at the top corner of the cathode end of M-2 line for the M-1 and M-2 structures respectively. In our experiment, for the M-1 structure the void location at the Cu/dielectric cap interface is contrary to the expected void location expected by current crowding mechanism. The two possible explanations are that the highly resistive Ta liner has reduced the current crowding at the via interface[129], and also while the proposed current density gradient force is large enough to drive a vacancy from the high to the low current density region, it is too small to drive a void. For M-2 structures although the final void location and shape are consistent with this mechanism, the void nucleation was actually at the Cu/dielectric cap interface at the line away from the cathode and the void aggregation at the top of cathode was due to void movement along this interface towards the cathode end. Owing to heterogeneous nucleation of a void on the Cu/dielectric cap interface, it requires only a small amount of super-saturation of vacancies to nucleate a void on the interface. For example, a triple point of Cu grain boundaries on the interface and the line

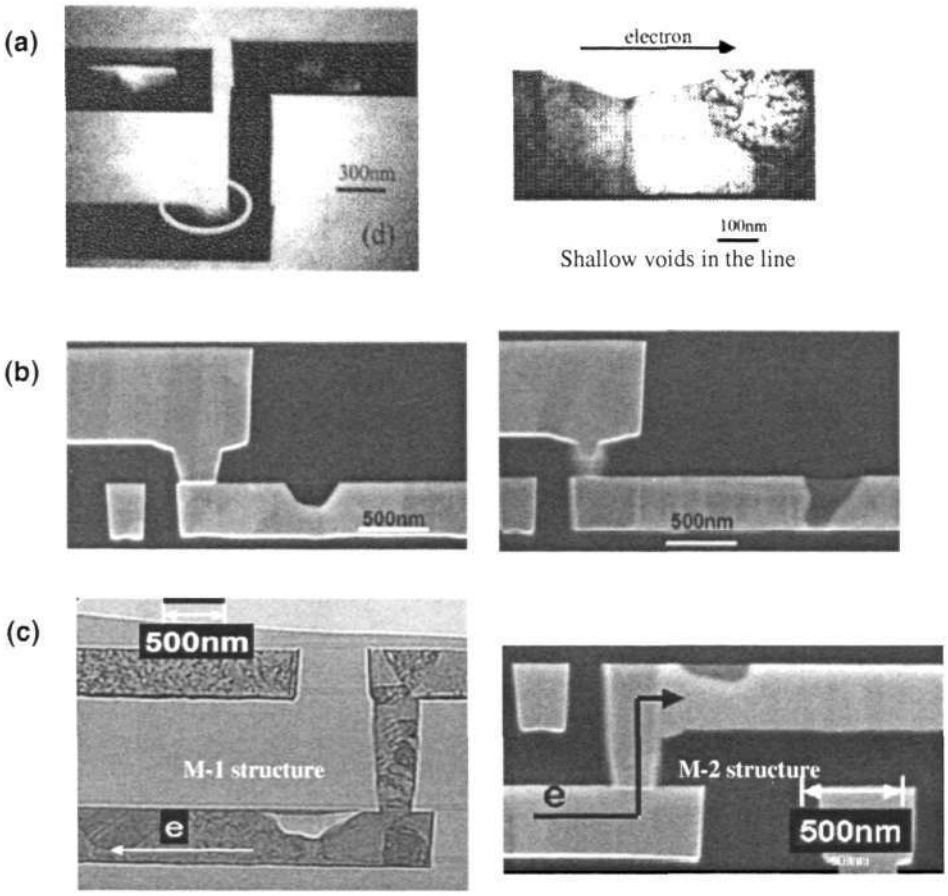


Figure 5.1: Voids observed away from the via (a) in reference 66 (b) in reference 68 (c) in references 123 and 140

intersection, where a Cu grain boundary meets the interface can become a heterogeneous site for void nucleation. So it can occur in the Cu/dielectric cap interface at locations which are away from the cathode in both the M-1 and M-2 structures.

The void movement can be understood based on the Cu atom transport along the periphery of the void, i.e., an inner surface, due to an electron wind force. This causes the void to move along the Cu/dielectric interface in the opposite direction to electron flow. Voids can grow by absorbing more vacancies and also voids can merge to form a larger void. We understand that theoretical studies on mechanism of void drift and coalescence are reported[141,144], but this mechanism is not considered in the studies on electromigration in damascene structures[34,61,66,68,123,128,140].

The condition for electromigration immortality due to the short strip effect in M-1 structures has been proposed to be the limit for void nucleation, and in M-2 structures, the proposed condition is when the electron wind force does not exceed the back-stress[68]. But the condition for M-1 structure may not be true here as it is assumed that the void should nucleate at the Cu/dielectric interface near the via bottom. Rather, the observations here suggest that the immortality condition for M-1 structure should also be similar to M-2 structure because the voids were found to nucleate at the Cu/dielectric cap interface in the line instead of near the via bottom. Overhang or extension above the via was found to improve the electromigration lifetimes[34] as the void formed in these extensions delaying the via-opening. Our observations suggest that this technique may work for the M-2 type of structures, but may not work for the M-1 type of structures.

In summary, electromigration mechanism in dual-damascene Cu interconnect structures was unraveled by *in-situ* SEM characterization. Void formation and migration, in a direction opposite to electron flow, along the Cu/dielectric interfaces are found to the principle electromigration mechanisms in Cu dual-damascene structures. These findings have led to a better understanding of real electromigration mechanisms in dual-damascene Cu interconnects.

5.3 Mechanism of electromigration-induced voiding in interconnect tree structures

Although numerous studies on electromigration have been reported, most of them have employed straight via-to-via test lines or single layer lines directly connected to contacts. The interconnects in real ICs are much more complex with multiple interconnect line segments connected to vias. Interconnect tree structures are required for realistic electromigration studies which can correctly simulate the conditions in real on-chip interconnects[104]. In-depth understanding of electromigration failure mechanism in interconnect tree structures is necessary for optimization of physical and electric design rules. Considering the design rules in future interconnect architectures, optimized on-chip interconnect systems with high immunity to electromigration-induced failures can be designed. As dual-damascene Cu interconnect technique is currently being employed for on-chip interconnect fabrication, and will continue to be used for next technology generations in the near future due to significant cost advantage, it is of great technological significance to correctly understand the electromigration mechanism in dual-damascene Cu interconnect tree structures. In this study, we have unraveled the electromigration-induced voiding mechanisms in Cu interconnect tree structures.

Voids were observed to emerge at the Cu/SiN_x interface in the test line away from the middle via (**Figure 4.20**) and move towards the via in opposite direction to electron flow, consistent with our previous *in-situ* electromigration studies on M-2 and M-1 dual-damascene Cu structures (**Section 5.2**). A void was formed at the Cu/SiN_x interface above the middle via and it moved slightly towards the left segment. However, the void neither moved further nor grew continuously. The void size was increased to span the via region only after agglomeration of additional voids moving along the Cu/SiN_x interface leading to failure of the right segment. The left segment of the interconnect tree also showed an open circuit after test. It is clear from these results why non-current carrying adjacent segments were observed to be open circuited during electromigration tests in other reported studies on Cu interconnect trees[106,107]. It should be noted that in this case there is no Cu/liner interface at the middle via region, which can provide a path for the void to sneak into the via as in case of standard M-2 structures[127,145]. So, the void cannot easily

move into the via as in case of standard M-2 structures without any reservoir segment. The via opening is delayed because the void has to grow to a larger size by agglomeration of additional voids as compared to standard structures. Here, it is interesting to consider the current gradient induced vacancy flux effect[128]. This mechanism is also possible in these structures. However, the observations suggest that this mechanism is unlikely to play a dominant role in these test structures, at least during the initial stage of void evolution at via, because void was not found to be nucleated at low current density region.

The void agglomerated at the middle via region did not move further to the left in the case of configuration (i) (refer Figure 3.10) because there was no current in the left segment to cause atom transport along the void surface, which leads to void movement. However, if there is current flowing in the left segment in the same direction as the right segment, the void is expected to move further from via region into the left segment. Such mechanism was observed for interconnect tree structures with configuration (ii) (refer Figure 3.10) as shown in **Figure 4.21**. The voids which agglomerated at the middle via region of the right segment moved further into the left segment. In this test, the left segment failed earlier than the right segment. This is because the void agglomeration at the middle via region (which is cathode end for the right segment) is averted by further void movement away from middle via into the left segment. It should be noted that the left segment failed earlier although it carried lower current density than the right segment. The previously reported experimental results on Cu interconnect tree suggesting that the highest current carrying segment may not be the least reliable[106,107] can be clearly understood based on the observed mechanism. Furthermore, as the current in the adjoining left segment was reversed (configuration (iii), refer Figure 3.10), the voids moving along the Cu/SiN_x interface in both the segments converged at the middle via region as shown in **Figure 4.22**. While for some samples, void from only one of the segments agglomerated at the middle via as shown in **Figure 4.23**. This is due to statistical variation of time required for void nucleation and agglomeration in each of the segments. Interesting void shape evolution at middle via region was observed for these structures. This observation is different from void evolution in the cathode via for standard M-2 structures and interconnect tree structures, with no current in other

segment. The void sneaked into the via from the left side edge of the via instead of the right side edge (which takes place in standard structures). In this case, the void sneaked into the via from the line segment along the Cu/liner interface which is not at the extreme cathode end of that segment. This void evolution can be attributed to electron flow in the right segment in a opposite direction due to which the void movement (from the left segment) is averted from crossing the middle via region and it moves down the via edge.

The current understanding of electromigration mechanism in similar Cu interconnect tree structures is based on theory of maximum tensile stress developed in the middle via. The void is assumed to be nucleated at the liner in the middle via bottom, and then grow to span the via and interconnect segments[106,107]. The peculiar behavior of Cu interconnect trees leading to the highest stressed segment not being the least reliable, is thought to be associated with possibility of liner rupture at via bottom and ease of void nucleation at Cu/SiN_x interface[106,107]. The mechanism revealed by our *in-situ* characterizations gives a much clearer understanding of the electromigration behavior of Cu interconnect tree structures. The sample size used in these experiments was not statistically significant to determine the relative electromigration performance dependence of the right segment based on current configuration in adjoining left segment. However, it can be easily inferred based on the observed mechanism that the configuration (iii) will have worst performance while the configuration (ii) will have better electromigration performance for the right segment. This inference is consistent with reported electromigration failure data of similar interconnect tree structures[107].

In summary, the peculiar electromigration behavior of dual-damascene Cu interconnect tree structures is due to the electromigration mechanism, which involves void migration along Cu/SiN_x interface in a direction opposite to electron flow. These findings can be useful for an accurate assessment or prediction of circuit level electromigration reliability in complex on-chip interconnect structures.

Chapter Six

Monte Carlo Simulations

6.1 Development of Monte Carlo based electromigration simulation tool

A simple model is employed, which was implemented using random atomic jumps based on the Monte Carlo method, to understand electromigration-induced voiding observations revealed during this research wok. Only two parameters were considered - bonding energy and electron wind force. Monte Carlo scheme is governed by calculation of change of energies for deciding success of an atomic jump between randomly selected neighboring atomic positions. A simplified metropolis Monte Carlo algorithm was employed in which atomic jump was successful only for reduction in energy. Energy consists of sum of pair interaction energies N*Eb (N-number of filled neighboring sites, 0<=N<=8, Eb- binding energy per link) and of effective electric energy due to the electron wind force. We also introduced a special interaction energy at the surface of interconnect line to simulate different interface conditions at this surface. The Monte-Carlo algorithm steps are explained in **Figure 6.1.** Complete code for the simulations was written in MatLab (**Appendix I**). A square lattice is employed for ease in programming and atomic jumps to eight neighboring atomic positions are considered. For random selection of atoms, only an atomic position with at least one neighboring vacancy was considered to save computational time. Pair interaction energies were re-calculated only after atom jump between an atomic location filled with an atom and a location with a vacancy. The force due to electron wind force was simulated by introducing a linear force gradient from one end of the line to another. The interaction energy was considered to be relatively higher than the gradient due to the electromigration wind force.

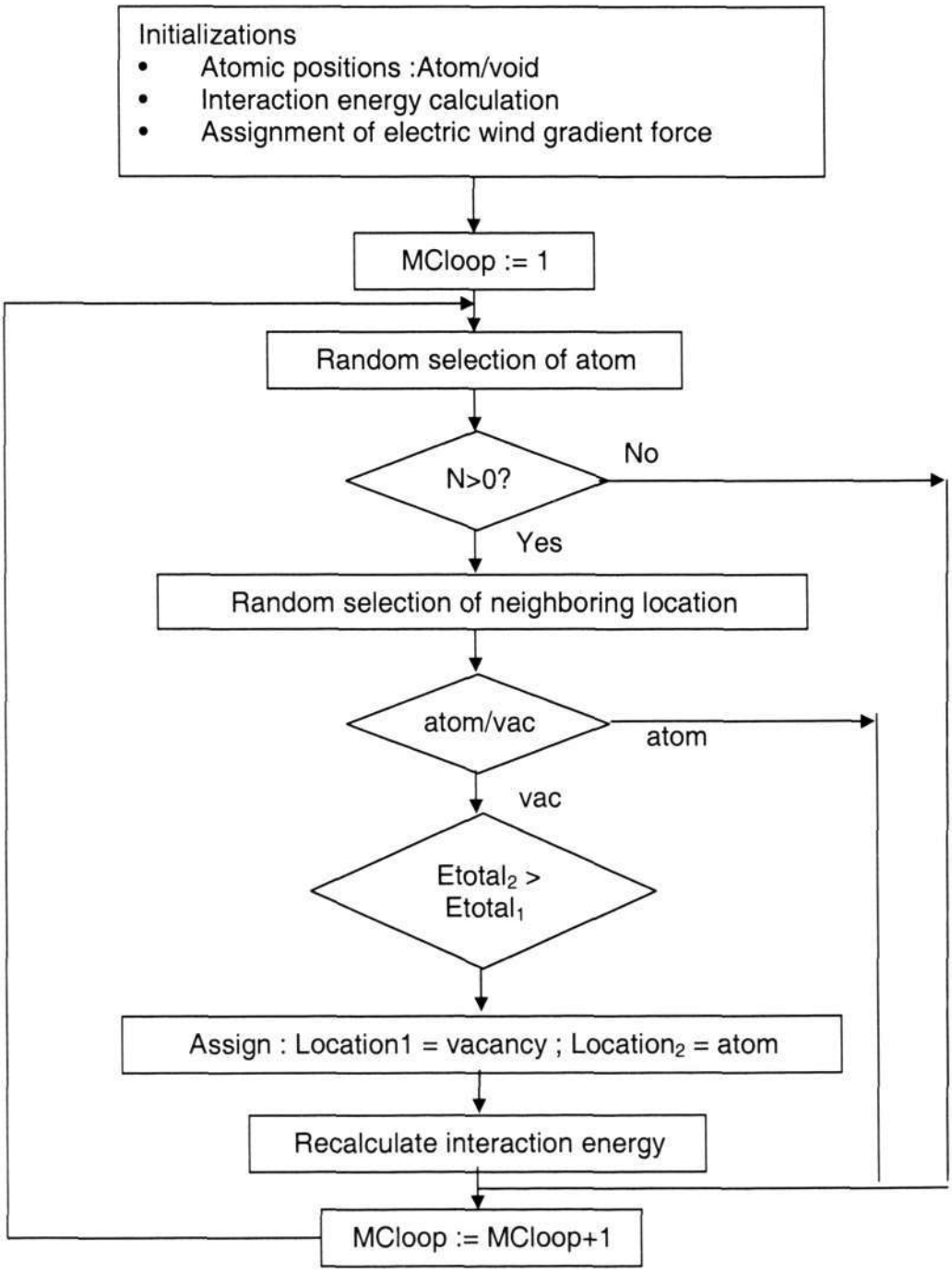


Figure 6.1: Flow chart of Monte-Carlo algorithm

6. 2 Simulations of electromigration-induced voiding

6.2.1 Validation of model

Electromigration in Al and Cu interconnects was simulated with the same initial condition ----(i) same vacancy concentration and (ii) same initial *'vacancy clusters'* at interface (which represent small pre-existing voids at the Cu/dielectric cap interface due to damage during CMP and dielectric cap deposition in Cu interconnects). Low bonding energy was introduced at the interface in the case of simulation of electromigration in Cu interconnects, which represents highly disordered and weak Cu/dielectric cap interface. On the other hand, a higher bonding energy was introduced at the interface for Al simulation, which represent a strong interface in case of Al interconnects. The results indicate that initial vacancy clusters will remain at the Cu/dielectric-cap interface, and vacancies will be captured at this interface in case of Cu interconnects **(Figure 6.2)**. Note that this is a simulation of a region at the interface (roughly a few nanometers), which is only a small section along of the whole interconnect line. However, this phenomenon will occur through out the entire length of the Cu interconnect line. It can be inferred that these vacancies will move along this interface in a direction opposite to electron flow direction leading to void nucleation at the Cu/dielectric-cap interface at the cathode region (possibly at grain boundary / dielectric-cap intersection). This observation is consistent with *in-situ* SEM observations of voids only at the Cu/dielectric cap interface at the cathode end of the line [section 5.2, ref. 145] and *'preferential void nucleation at Cu/dielectric cap interface'* reported in Cu electromigration studies by other researchers[61]. On the contrary, there is no vacancy capture at the interface in case of Al interconnects, and the pre-existing voids will not preferentially remain at the interface and move along this interface **(Figure 6.3)** Based on this result, it can be easily inferred that voids need not always nucleate and move along the interface in Al interconnects. This is exactly in agreement with *in-situ* observations of electromigration in Al interconnects revealing "random" movement of voids [146]. Such electromigration degradation in Al interconnects is well known. This mechanism is completely different from that in damascene Cu interconnects. Thus, it is clear from these results that the peculiar electromigration voiding mechanism in Cu interconnects is due to *Cu/dielectric-cap*

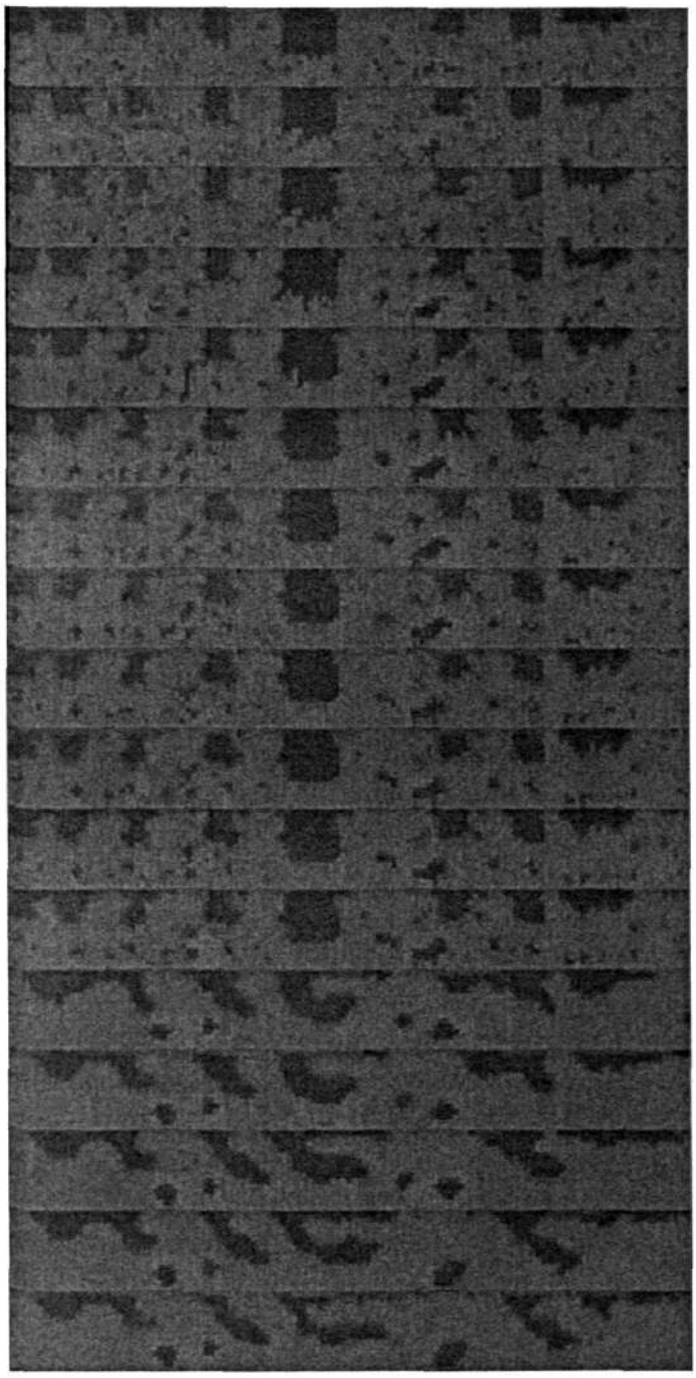


Figure 6.2: Simulation of initial vacancy cluster evolution at Cu interface

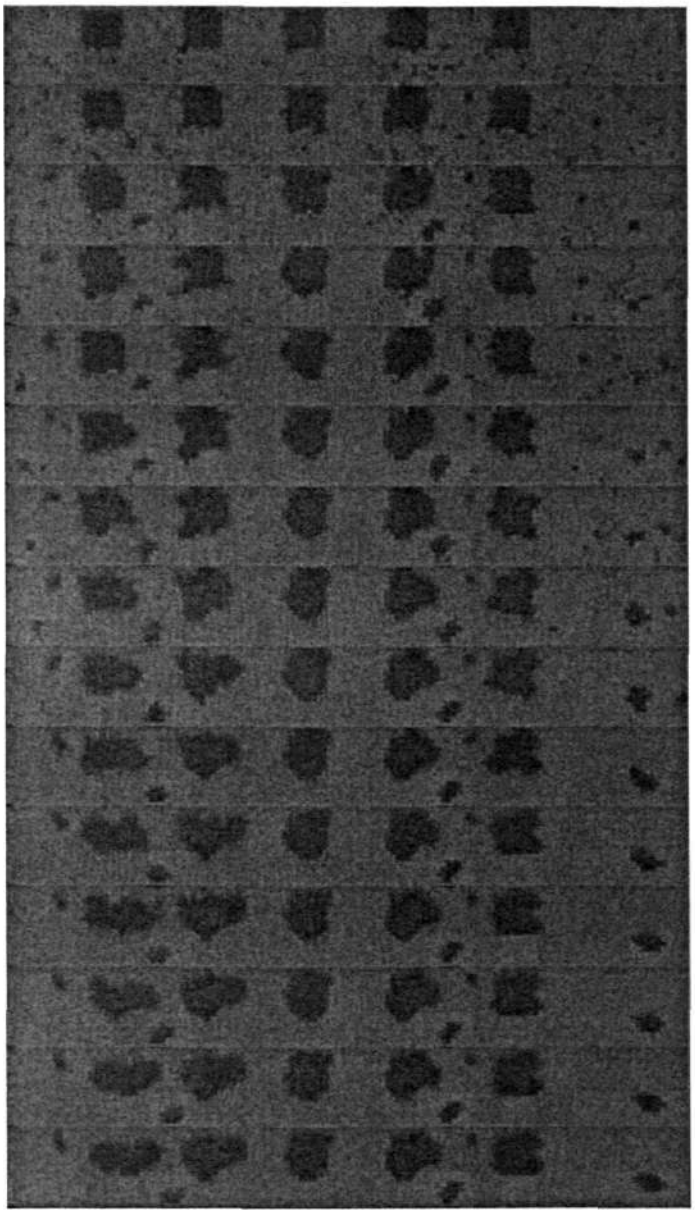


Figure 6.3: Simulation of initial vacancy cluster evolution at Al interface

interface acting as vacancy sink. Moreover, slit-like void evolution in Al interconnects was simulated and it was observed that the voids seem to be slightly tilted (from their original location) in opposite direction to the electron flow during their evolution to slit-like voids. This observation is consistent with other experimental and theoretical studies **[108,117]** suggesting such void behavior in Al interconnects.

Strengthening the Cu/dielectric cap interface by selective electroless plating with CoWP layer was reported **[95]** and a changed electromigration mechanism was observed as compared to Cu/SiN_x interface [section 5.2,145]. Void movement in this was simulated by increasing the bonding energy at Cu/dielectric-cap interface to become equal to the bonding energy at any other location (this rough approximation is based on a TEM investigation of the Cu/CoWP interface). The same initial void condition was used in the simulations of electromigration-induced void movement in Cu/dielectric-cap and Cu/CoWP interface. Significant void movement along the interface is predicted in case of Cu/dielectric-cap (**Figure 6.4**), which is consistent with the *in-situ* SEM observations on interconnect structures with Cu/SiNx interface carried out in this research work [section 5.2,145]. On the other hand, the results suggest that the vacancy clusters seem to be pinned at the interface in case of Cu/CoWP (**Figure 6.5**). This effect should lead to significantly increased time to failure as found in experimental studies [95,146]. As this case is similar to Al, similar failure mechanisms are expected and are really observed. Voiding in the line (same as Al) was found during experimental studies on structures with a Cu/CoWP [95,146] and Cu/Sn interface [149].

The results explained so far are well known and serve to validate the applicability of such a model to investigate the electromigration-induced voiding mechanism, and to explain electromigration degradation and eventually interconnect failure.

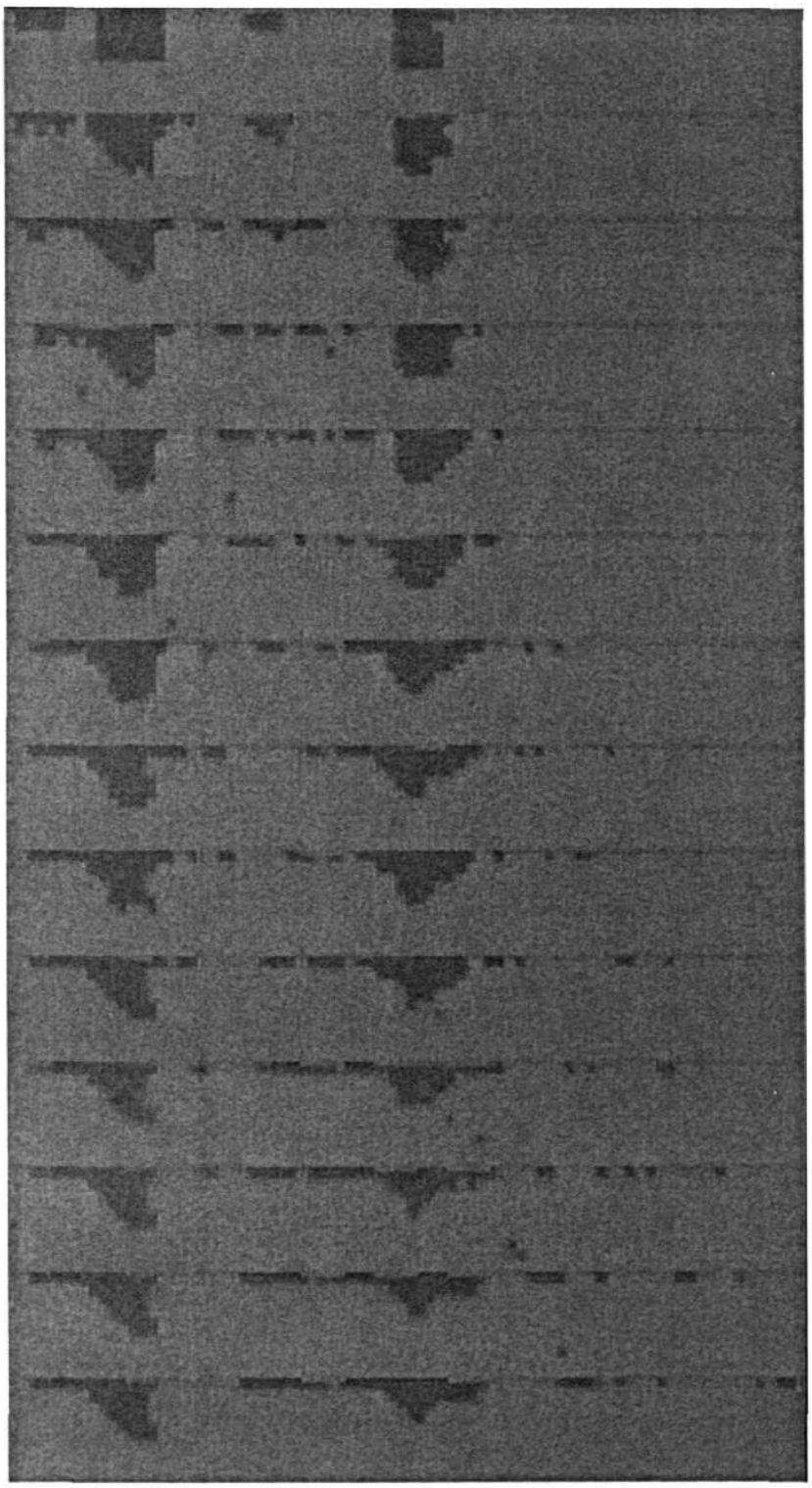


Figure 6.4: Simulation of void evolution for Cu/SiN_x interface

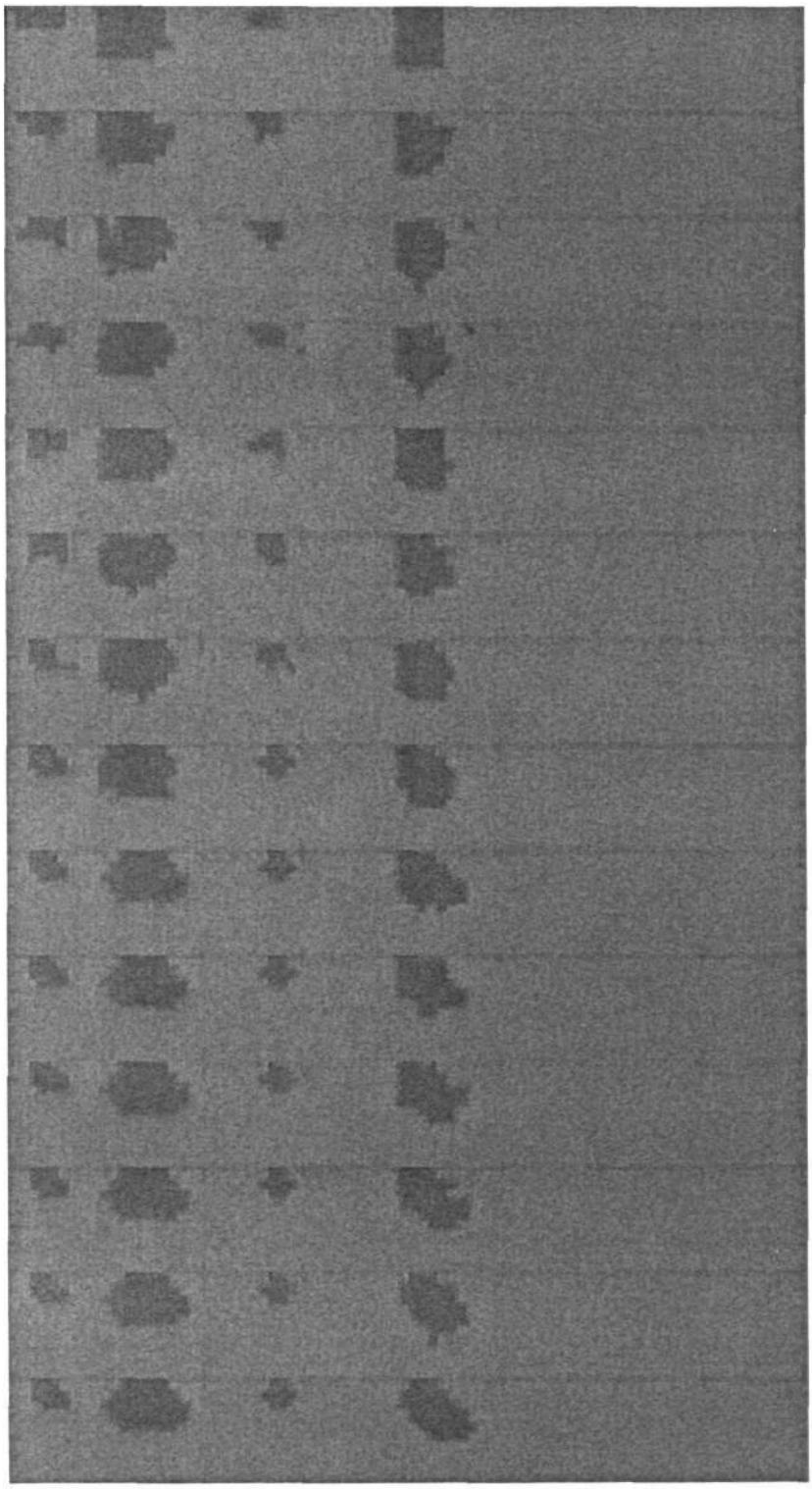


Figure 6.5: Simulation of void evolution for Cu/CoWP interface

6.2.2 Electromigration-induced voiding in Cu damascene structures

Void evolutions in Cu interconnect structures---Upper(M-2)/lower(M-1) layer and interconnect tree structures

From discussion in previous section, it can be inferred that voids will be located at the Cu/dielectric cap interface in the cathode region and that these voids will be flat along this interface, until their size increases due to significant agglomeration. This is consistent with our in-situ observations. Such voids will be assumed in the further studies, and no significant effect of change in current distribution can be approximated. Simulations were carried out for M-2 and M-1 layer dual-damascene test structures (**Figure 6.6**). The void shape and the void location predicted by the results of these simulations are similar to the void evolution observed during the initial stage of electromigration degradation by *in-situ* SEM studies in this research work. These results are also consistent with failure analysis results reported in electromigration studies on similar interconnect structures by other researchers [61,67,68,106,107,140]. The electromigration behavior of Cu interconnect tree structures revealed by *in-situ* SEM characterizations (section 5.3) can be explained based on this model. Simulations to analyze voiding in configuration (i) (refer Figure 3.10) suggest a void location at the Cu/dielectric cap interface on top of the middle via slightly towards the *left segment* (**Figure 6.7a**), similar to the void observed during the initial stage (**Figure 4.20d**). Most interesting is configuration (iii) (refer Figure 3.10) and a situation when a void moves at the middle via region from only one of the segments. The void location suggested by simulating this situation (**Figure 6.7b**) confirms with the experimental *in-situ* SEM observation (**Figure 4.23**). Based on the simulation results, it can be inferred that there is a possibility that the void may sneak into the via from the line segment along the Cu/liner interface which is not at the extreme cathode end of that segment. Indeed, such a void evolution was observed for one of the test samples (**Figure 4.23**). This observation is different from void evolution in the cathode via for standard M-2 structures and interconnect tree structures, with no current in adjacent segment. These peculiar void evolutions could not have been discerned by the conventional theory of maximum tensile stress at cathode flux divergence site.

In summary, this model can *qualitatively* explain electromigration-induced voiding observed during experimental *in-situ* SEM characterizations as well as in various other reported electromigration studies. Based on this model, it can be inferred that peculiar electromigration-induced void evolution in Cu interconnect structures is mainly due to weak interfaces like *Cu/dielectric-cap interface acting as vacancy sink* and due to redistribution of atoms at interface. However, this model is relatively simple with many approximations. Therefore, it can provide only a qualitative explanation of voiding during the initial stage of electromigration. These findings warrant need to re-investigate electromigration mechanisms by developing rigorous models based on similar concepts, considering other important parameters such as microstructure, current density distribution, stress and temperature gradients, and introducing diffusivities for different atomic transport paths using kinetic Monte-Carlo and finite-element methods. Such approaches will provide quantitative information and further in-depth understating of electromigraion-induced voiding in damascene Cu interconnect structures.

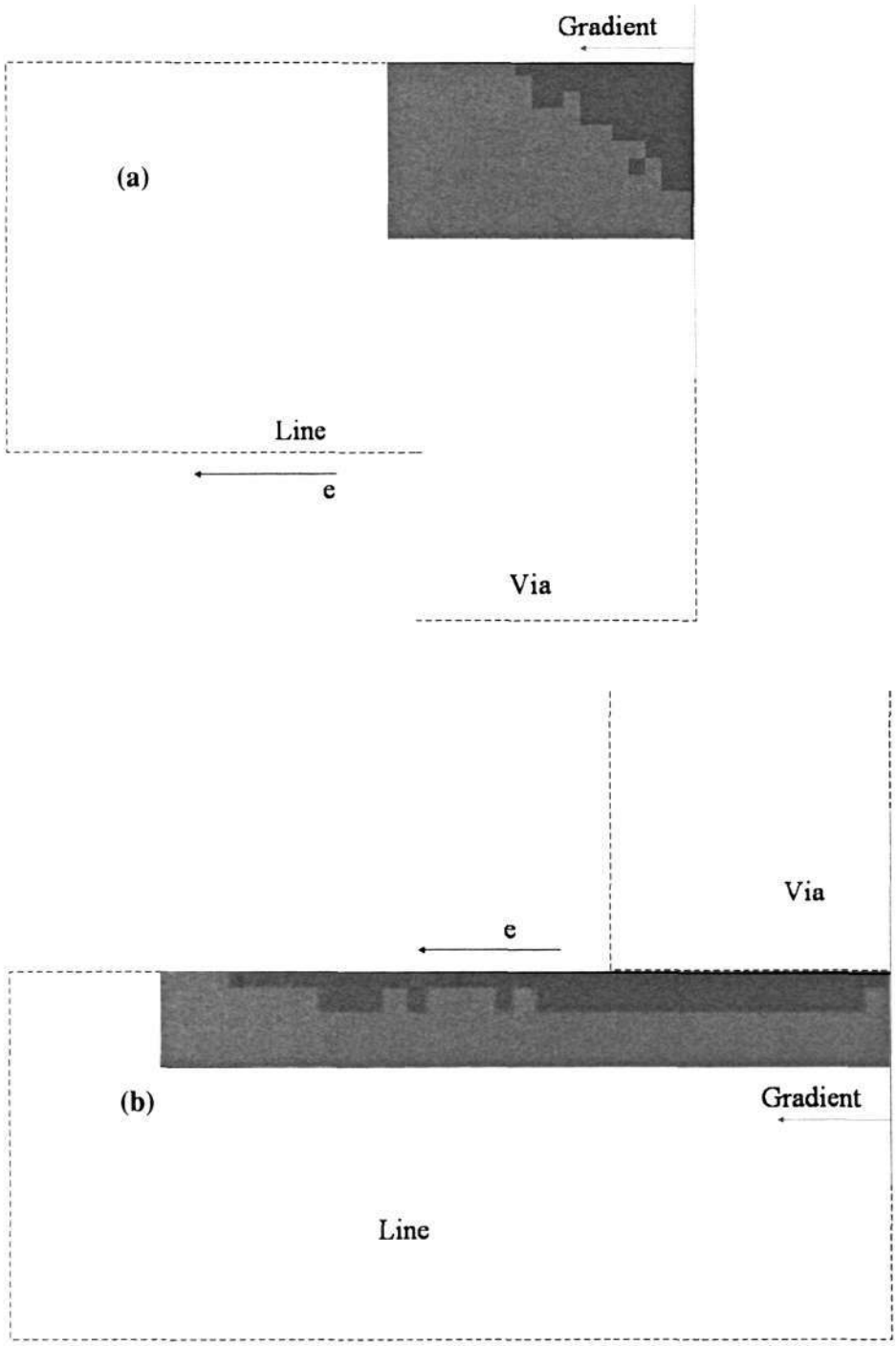


Figure 6.6: Simulation of electromigration-induced voiding in (a) upper layer (M-2) and (b) lower layer (M-1) structures

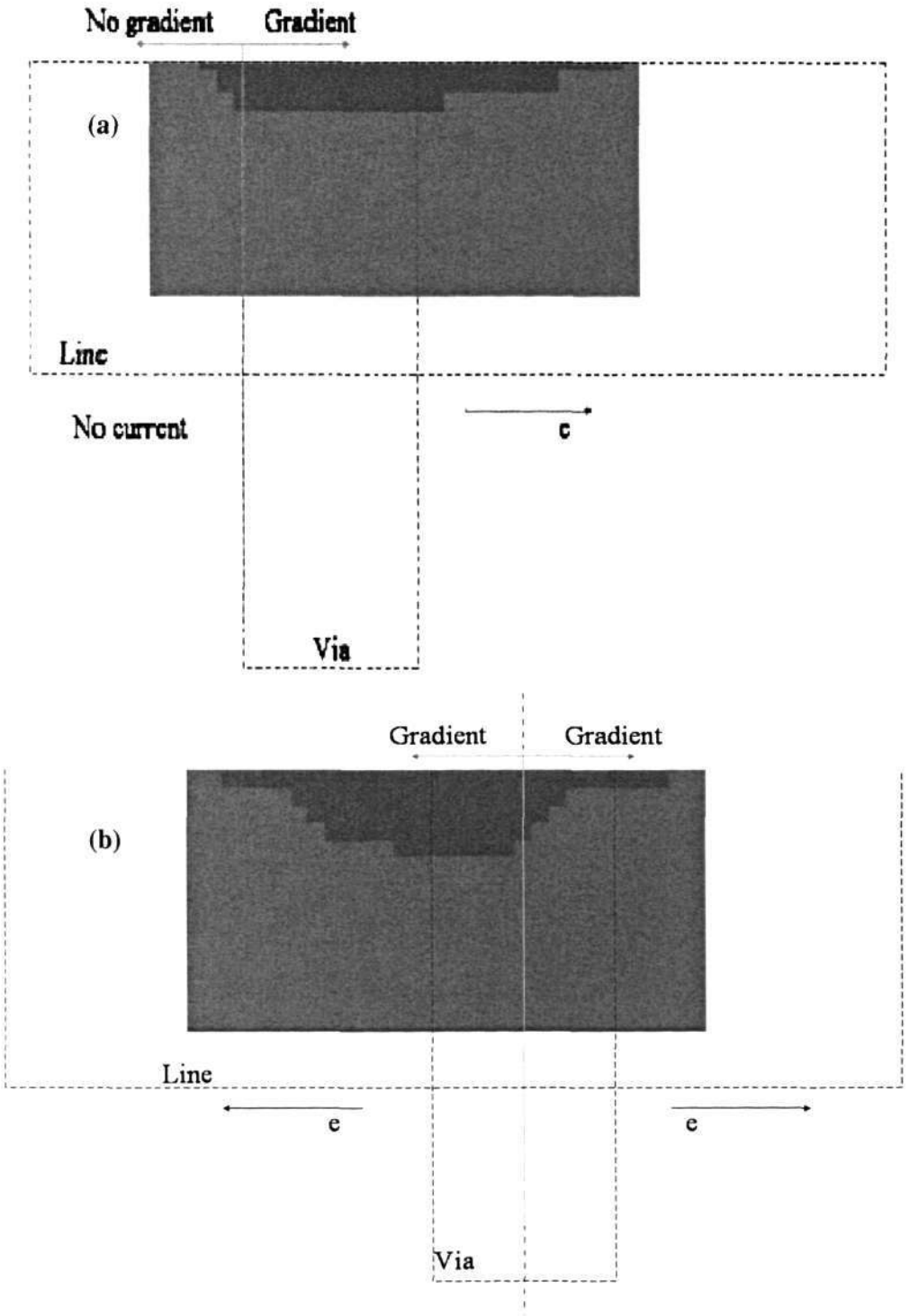


Figure 6.7: Simulation of electromigration-induced voiding in (a) interconnect tree stressed in configuration (i) and (b) interconnect tree stressed in configuration (iii)

Chapter Seven

Conclusions and future work

7.1 Conclusions

- **Investigation of electromigration behavior of dual-damascene interconnects**
  1. Dual-damascene Cu interconnects exhibit interesting asymmetric electromigration behavior. Cu/dielectric-cap interface is the preferred electromigration void nucleation site for M-2 as well as M-1 dual-damascene structures with the activation energies in the range of 0.6 to 0.8 eV. Contrasting effect of line-width on electromigration in M-2 and M-1 layer dual-damascene structures cannot be completely explained by conventional theory of maximum tensile stress at cathode flux divergence site and current gradient induced vacancy flux.
  2. Short length effect is complicated in dual-damascene Cu interconnects, contrary to the direct effect observed in Al and W-plug Cu interconnects. M-2 structures show two distinct, via and line, electromigration failures whereas, the M-1 test structures only show the Cu/dielectric cap voiding failures.
  3. The observed electromigration behavior can be attributed to Cu/dielectric cap interface acting as vacancy sink and preferable nucleation site.
  4. These differences again could be comprehended by taking into account the back stress effect and the possible weakness in the via-bottom and Cu/ dielectric cap areas. These observed phenomena are specific to the Cu dual-damascene structures and will continue to have major technological implications for electromigration reliability assessment for future interconnects.

- **Effect of Cu surface treatment**
  1. Although M-2 and M-1 dual-damascene structures have different electromigration behavior, both of these can be altered similarly due to

surface treatment. The observed effect supports the Cu/dielectric cap interface dominated electromigration mechanism in dual-damascene interconnects.

2. Hydrogen plasma and silane treatments were found to cause better electromigration performance with improvement in MTF by approximately 200%. Surface treatment process optimization can be pursued to achieve further improvement. Surface treatment can be effectively used to improve overall electromigration reliability of dual-damascene Cu interconnects and it is more compatible to conventional damascene process than other techniques.
3. Single layer damascene test structures show different electromigration behavior for surface treatments and cannot be directly used for assessing effect of surface treatment on electromigration reliability of dual-damascene structures.

- **Electromigration mechanism in Cu dual-damascene structures**
  1. *In-situ* characterizations revealed electromigration-induced void evolution in dual-damascene structures.
  2. Based on *in-situ* observations a phenomenological model of EM mechanism can be proposed: heterogeneous void nucleation at Cu/dielectric cap interface, movement along Cu/dielectric interface in a direction opposite to electron flow and eventually agglomeration at cathode via leading to failure.
  3. Mechanism in both M-2 and M-1 structures is the same, only difference is the site of agglomeration, due to peculiar dual-damascene architecture.
  4. This mechanism is contrary to current understanding of void nucleation at max tensile stress location (which is the Cu/liner interface at cathode bottom) and current gradient induced vacancy flux theory
  5. Void movement is along Cu/dielectric cap interface in a direction opposite to electron flow. This void movement can be understood based on the Cu atom transport along the periphery of the void, i.e., an inner

surface, due to an electron wind force. This causes the void to move along the Cu/dielectric interface in the opposite direction to electron flow.

6. Void movement rate was found to be 0.5 μm/hr and it is of the same order of analytically derived values.
7. Void growth, coalescence and trapping at grain boundary were also observed.
8. Such mechanism consisting of void nucleation and movement along Cu/dielectric cap interface in a direction opposite to electron flow is an important finding in this research field. These findings have led to a better understanding of real electromigration mechanism in dual-damascene Cu interconnects and its peculiar electromigration behavior.
9. M-1 and M-2 test structures are conventionally used for electromigration reliability assessment. The mechanism proposed in this thesis can be used for better understanding of electromigration test results and utilizing the test data for reliability estimation.

- **Electromigration-induced voiding in Cu interconnect tree structures**

1. EM-induced void evolution in Cu interconnect tree structures was unraveled by *in-situ* characterizations.
2. Mechanism consisting of void movement along Cu/dielectric cap interface in a direction opposite to electron flow was found to be the cause of peculiar behavior Cu interconnect tree structures.
3. Effect of reservoir and stressing condition in adjacent segment in an interconnect tree on EM-induced void evolution can be understood and predicted according to the proposed mechanism.
4. Electromigration behavior of Cu interconnect structures and discrepancies as compared to Al interconnect trees can be clearly understood.
5. Electromigration performance can be inferred based on the proposed mechanism and is in agreement with reported experimental data on similar structures.
6. Electromigration-induced voiding mechanism in the interconnect tree test structures, which realistically represent the complex interconnect

structures in real ICs, is clearly understood from the present study. These findings can be useful for an accurate assessment or prediction of circuit level electromigration reliability in complex on-chip interconnects. The present electromigration reliability estimation/verification IC design tools mainly consider the current density distribution and the back-stress effect in interconnect structures. However, the void-evolution mechanism based on the movement along Cu/dielectric cap interface in opposite direction to electron flow needs to be considered by incorporating appropriate estimation of void/vacancy cluster volume migration to a critical site such as extreme cathode via or a via connected to various high current density carrying line segments.

- **Monte carlo simulations**

1. Electromigration-induced void evolution in various interconnect structures were simulated by a simple model, which was implemented using random atomic jumps based on Monte-Carlo method. Only two parameters were considered - electron wind force and maximization of bonding energy. Results indicate that this model can *qualitatively* explain electromigration-induced voiding observed during our experimental *in-situ* characterizations as well as various other reported studies.
2. Simulations of EM-induced voiding in Al and Cu interconnects match with well-known mechanisms.
3. Differences in electromigration mechanisms in Cu and Al interconnects and electromigration behavior of Cu interconnect structures can be understood by this model.
4. Based on this model, peculiar voiding in M-2/M-1 layer and interconnect tree Cu dual-damascene structures can be clearly understood. These peculiar void evolutions could not have been completely explained by conventional theory of maximum tensile stress at cathode via bottom and current gradient induced vacancy flux.

5. This model can *qualitatively* explain electromigration-induced voiding observed during experimental *in-situ* SEM characterizations as well as in various other reported electromigration studies.
6. Based on this model, it can be inferred that peculiar electromigration-induced void evolution in Cu interconnect structures is mainly due to weak interfaces like *Cu/dielectric-cap interface acting as vacancy sink* and due to redistribution of atoms at interface.
7. However, this model is relatively simple with many approximations. Therefore, it can provide only a qualitative explanation of voiding during the initial stage of electromigration.
8. These findings warrant need to re-investigate electromigration mechanisms by developing rigorous models based on similar concepts, considering other important parameters. Such approaches will provide quantitative information and further in-depth understating of electromigraion-induced voiding in damascene Cu interconnect structures.
9. Strategies for electromigration reliability improvement can be suggested based on the proposed mechanism. The electromigration-induced voiding can be suppressed by reducing the initial vacancy cluster volume and/or retarding the void evolution due to vacancy cluster movement along the Cu/dielectric cap interface. The initial vacancy cluster volume may be reduced by various methods such as improved Cu CMP process, reducing damage during dielectric cap deposition and controlling the ECP Cu deposition process. Void evolution due to vacancy cluster movement may be retarded by improving Cu/dielectric cap adhesion by surface treatments or introducing stronger bonding at Cu surface by new selective cap deposition methods such as selective CoWP cap. Moreover, interconnect design strategies may also be employed to improve circuit level electromigration reliability by developing reliability tools which incorporate the void movement and agglomeration mechanisms.

7.2 Future work

- **Monte Carlo Simulations :**

The Monte-Carlo based model implemented in this research work can be further improved by developing rigorous model based on similar concepts, considering other important parameters such as microstructure, current density distribution, stress and temperature gradients, and introducing diffusivities for different atomic transport paths. Finite-element methods can be introduced in the Monte-Carlo loop to determine important parameters such as distribution of current density, stress and temperature. Kinetic Monte-Carlo methods can be employed to keep track of time during simulations. Such approaches will provide *quantitative* information and further in-depth understating of electromigration-induced voiding in damascene Cu interconnect structures. This rigorous model can also be particularly important to simulate void evolution during *the last* stage of electromigration-induced void evolution when the voids agglomerate at the cathode via region eventually leading to failure. By introducing strain energy parameter during atomic jump simulation in a Monte-Carlo loop, stress-induced voiding can be simulated using the same model. Moreover, combined effect of stress-induced and electromigration-induced voiding can be studied. Another important electromigration mechanism that can be studied with this model is the short length effect. This effect is understood based on increase in back-stress effect with reduction in length of the interconnect line which balances the electromigration wind force. Investigations can be pursued using the Monte-Carlo simulations to determine whether this effect is possibly due to reduction of available *initial vacancy cluster volume* in a short length interconnect line.

- **Investigation of novel Cu/cap interfaces for future interconnect technologies**

A diffusion barrier is required for Cu interconnects as Cu as easily diffuse into the dielectrics. As the critical feature size in microelectronic devices continues to decrease below 100 nm, barrier materials of < 5 nm thickness are required. Recently it was shown that self-assembled monolayers (SAMs) can be attractive candidates for this purpose [150]. SAMs are shortchained organic molecules of the type X-$(CH_2)_n$-

Y, or their variants, where X and Y are either organic or certain inorganic moieties. SAMs are typically tethered to a substrate on one end by moieties such as a thiol (–SH) or a silane (–SiZ_3 where Z is typically a halogen or an alkoxy group). The molecules of SAM are composed of three parts: terminal functional group, alkyl chain and the anchor group as shown in **Figure 7.1** [151].

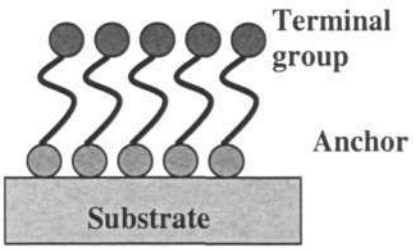


Figure 7.1: Schematic of SAM molecule structure.

The anchor group makes the SAM attach to the substrate and the terminal group is the moiety standing out of the surface. The alkyl chain helps the molecules to interconnect to each other through the Van der Waals force. The number of alkyl groups determine the length of the molecule. Long molecules provide stronger Van der Waals inter-chain strength, so that molecules pack together well. But at the same time, since the Van der Waals force is not strong enough, long molecule chain will tilt more than short chain, which will possibly randomize the structures

SAMs have been shown to act as diffusion barrier for Cu and their "near zero" thickness make an attractive candidate as a barrier for future interconnect technologies [150]. Also, it has been recently shown that SAMs can improve adhesion between Cu and dielectrics [151,152]. In reference [152], it is interesting to note that XPS measurements showed that Cu-pyridine and Cu-amine interactions have a factor-of-four higher binding energy than that of Cu-N bonds at Cu/SiN interfaces.

Recent electromigration studies on effect of dielectric cap-layer have considered silicon nitride or low-k dielectric cap layers that will be employed in near future interconnects. But, according to knowledge of author, there are no reported studies on the effect of SAMs on interfacial electromigration. Although this may not be relevant to current or near-future interconnect technologies, it will be important for next generation interconnects where SAMs will be the likely candidates as barriers. The current research work can be extended to study effect of SAMs on

interfacial electromigration. Electromigration test structures with SAM layer as cap layer, instead of conventional dielectric cap layers, can be fabricated as shown in **Figure 7.2.**

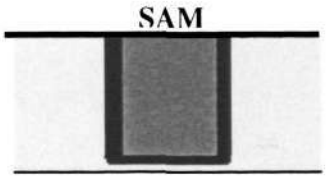


Figure 7.2: Test structure with SAM as a cap layer.

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Appendix 1
Monte Carlo simulation tool code developed in MatLab

```
%using muldimentional arrays -1 is atom/void 2 is Ep(bond) and 3 is Ee (EM)
%dimension is the row and column dimension
rdimension=15
cdimension=150
%intializing array 1 to 1 at each location ie atom, if 0 means void

%ADDING vacancies

vac_per=0.1
for r=1:1:rdimension
   for c=1:1:cdimension
      vac=rand(1,1)
      if vac < vac_per
intial_structure(r,c,1)=0
else
   intial_structure(r,c,1)=1
end
end
end

%ADDING vacancies



I = intial_structure (:,:,1)
image(I,'CDataMapping','scaled')
axis image

%axis([0 10 0 30])
pause(2);

%FUNCTION FOR VOID ASSIGNMENT
% assigning 0 to void locations semicircle with centre at cdimension/2
% Radius is the radius of the void NOTE:Raduis should be even number
Radius=4
%decide colums using R*cos(theta)
%separate function can be used for circular
for c=2:1:6

   for r=1:1:5
   intial_structure(r,c,1)=0
end
end
```

```
%void 2

for c=10:1:16

   for r=1:1:5
   intial_structure(r,c,1)=0
end
end

for c=25:1:28

   for r=1:1:5
   intial_structure(r,c,1)=0
end
end


for c=40:1:44

   for r=1:1:6
   intial_structure(r,c,1)=0
end
end


for c=55:1:65

   for r=1:1:9
   intial_structure(r,c,1)=0
end
end

for c=85:1:90

   for r=1:1:5
   intial_structure(r,c,1)=0
end
end


for c=100:1:105

   for r=1:1:5
   intial_structure(r,c,1)=0
end
end

for c=110:1:122
```

```
   for r=1:1:3
   intial_structure(r,c,1)=0
end
end


for c=100:1:105

   for r=1:1:5
   intial_structure(r,c,1)=0
end
end

I = intial_structure (:,:,1)
image(I,'CDataMapping','scaled')
axis image

axis image
%axis([0 10 0 30])
pause(35);

%void assignment completed



%FUNCTION FOR EE ASSIGNMENT
%ee assignment in plane2
%ee_constant is for Fee=ee_constant*J
%J_normal is current density
ee_constant= 50
J_normal=1
ee_normal=ee_constant*J_normal


for r=1:1:rdimension
   for c=1:1:cdimension

%adding a gradient here

intial_structure(r,c,2)=ee_normal+0.5*ee_normal*(c/cdimension)

end
end

I2 = intial_structure (:,:,2)
image(I2,'CDataMapping','scaled')
axis image
```

```
%axis([0 10 0 30])
pause(32);

%FUNCTION FOR PP ASSIGNMENT
%pp assignment in plane3
%calculating no. of neighbours at each location-limited locations
%Box defines this box for calculating no. of neighbours

Box=4
%dding 5for Al make it strongest NOTHING FOR cu
%first defining seperately for row 1 only
temp_neigh_r=1
for temp_neigh_c=(2:1:cdimension-1)

neigh_count(temp_neigh_r,temp_neigh_c)=intial_structure(temp_neigh_r,temp_neig
h_c-1,1) ...
      +intial_structure(temp_neigh_r,temp_neigh_c+1,1)...
      +intial_structure(temp_neigh_r+1,temp_neigh_c-1,1) ...
      +intial_structure(temp_neigh_r+1,temp_neigh_c,1) ...
      +intial_structure(temp_neigh_r+1,temp_neigh_c+1,1)
end


% Now for rows 2 onwards
for temp_neigh_c=(2:1:cdimension-1)
   for temp_neigh_r=(2:1:rdimension-1)
      neigh_count(temp_neigh_r,temp_neigh_c)=(intial_structure(temp_neigh_r-
1,temp_neigh_c-1,1)...
      +intial_structure(temp_neigh_r-1,temp_neigh_c,1) ...
      +intial_structure(temp_neigh_r-1,temp_neigh_c+1,1)...
      +intial_structure(temp_neigh_r,temp_neigh_c-1,1) ...
      +intial_structure(temp_neigh_r,temp_neigh_c+1,1)...
      +intial_structure(temp_neigh_r+1,temp_neigh_c-1,1) ...
      +intial_structure(temp_neigh_r+1,temp_neigh_c,1) ...
      +intial_structure(temp_neigh_r+1,temp_neigh_c+1,1))
   end
end


%for column 1 and cdimension
temp_neigh_c=1
for temp_neigh_r=(2:1:rdimension)
   neigh_count(temp_neigh_r,temp_neigh_c)=8
end

temp_neigh_c=cdimension
for temp_neigh_r=(2:1:rdimension)
```

```
   neigh_count(temp_neigh_r,temp_neigh_c)=8
end

%for rdimension
temp_neigh_r=rdimension
for temp_neigh_c=(2:1:cdimension)
   neigh_count(temp_neigh_r,temp_neigh_c)=8
end

intial_structure(:,:,3)= neigh_count (:,:)
image(intial_structure(:,:,3),'CDataMapping','scaled')
axis image

axis image
%axis([0 10 0 30])
pause(25);


%defining Ep and Ee
%bond_pair_potential

%NOTE use higher to make bond energy dominanant
bond_pair_pt=2000
Ep(:,:)=bond_pair_pt*intial_structure(:,:,3)

%EM_constant_Zep
EM_const=2
Ee(:,:)=EM_const*intial_structure (:,:,2)
% Gradiant can be added later on


% for capturing void evolution in a video
aviobj = avifile('Cu add8 AND vac8.avi','fps',5);


%MONTE CARLO LOOP

for mcloop=1:1:100000000000
 %selection of random location
 [sizer,sizec]=size(Ep)
%random selection of element in matrix Ep
temp_rand_r=rand(1,1)*sizer
temp_rand_c=rand(1,1)*sizec
%note : random number is noramlized to select element ONLY from Ep
for rand_r=1:1:sizer
   if (rand_r-1)<=temp_rand_r & temp_rand_r<=rand_r
      rnd_r=rand_r
   else
```

```
   end
end

for rand_c=1:1:sizec
   if (rand_c-1)<=temp_rand_c & temp_rand_c<=rand_c
       rnd_c=rand_c
    else
    end
end
%selection of random location completed --rnd_r, rnd_c

%checking whether it is a bulk or void location-if yes reject and EXIT
COMPLETELY from mc loop
if ~( neigh_count (rnd_r,rnd_c)==8 | intial_structure(rnd_r,rnd_c,1)==0 | (rnd_r==1
& neigh_count (rnd_r,rnd_c)==5)|rnd_r==rdimension |rnd_c==1
|rnd_c==cdimension  )

%selecting a neighbouring void location
if 2<=rnd_r & rnd_r<=rdimension-1
   temp_rand_r2=rand(1,1)*8
   for rand_r2=1:1:8
   if (rand_r2-1)<=temp_rand_r2 & temp_rand_r2<=rand_r2
      rnd_ex=rand_r2
   else
   end
   end

   if rnd_ex==1
   ex_r=rnd_r
   ex_c=rnd_c-1

   elseif rnd_ex==2
   ex_r=rnd_r+1
   ex_c=rnd_c-1

   elseif rnd_ex==3
   ex_r=rnd_r-1
   ex_c=rnd_c-1

   elseif rnd_ex==4
   ex_r=rnd_r+1
   ex_c=rnd_c

   elseif rnd_ex==5
   ex_r=rnd_r-1
   ex_c=rnd_c

   elseif rnd_ex==6
```

```
   ex_r=rnd_r
   ex_c=rnd_c+1

   elseif rnd_ex==7
   ex_r=rnd_r+1
   ex_c=rnd_c+1

   elseif rnd_ex==8
   ex_r=rnd_r-1
   ex_c=rnd_c+1

   else
   end

elseif rnd_r==1
   temp_rand_r2=rand(1,1)*5

   for rand_r2=1:1:5
   if (rand_r2-1)<=temp_rand_r2 & temp_rand_r2<=rand_r2
      rnd_ex=rand_r2
   else
   end
   end


   if rnd_ex==1
   ex_r=rnd_r
   ex_c=rnd_c-1

   elseif rnd_ex==2
   ex_r=rnd_r+1
   ex_c=rnd_c-1

   elseif rnd_ex==3
   ex_r=rnd_r+1
   ex_c=rnd_c

   elseif rnd_ex==4
   ex_r=rnd_r
   ex_c=rnd_c+1

   elseif rnd_ex==5
   ex_r=rnd_r+1
   ex_c=rnd_c+1

   else
   end
```

```
end

temp_state1=intial_structure(rnd_r,rnd_c,1)
temp_state2=intial_structure(ex_r,ex_c,1)

%cheching change in system energy
deltaE= -Ep(ex_r,ex_c)+Ep(rnd_r,rnd_c)-Ee(rnd_r,rnd_c)+Ee(ex_r,ex_c)

if deltaE<0 & temp_state2==0 &  ~(intial_structure(ex_r,ex_c,3)==1)

intial_structure(rnd_r,rnd_c,1)=temp_state2
intial_structure(ex_r,ex_c,1)=temp_state1

%Revaluate Ep
%calculating no. of neighbours at each location-limited locations
%Box defines this box for  calculating no. of neighbours

Box=4
%first defining seperately for row 1 only
%using ONLY box recal

for temp_neigh_r=(ex_r-Box):1:(ex_r+Box)

for temp_neigh_c=(ex_c-Box):1:(ex_c+Box)

if temp_neigh_r==1 & 2<=temp_neigh_c & temp_neigh_c<cdimension

neigh_count(temp_neigh_r,temp_neigh_c)=intial_structure(temp_neigh_r,temp_neig
h_c-1,1) ...
      +intial_structure(temp_neigh_r,temp_neigh_c+1,1)...
      +intial_structure(temp_neigh_r+1,temp_neigh_c-1,1) ...
      +intial_structure(temp_neigh_r+1,temp_neigh_c,1) ...
      +intial_structure(temp_neigh_r+1,temp_neigh_c+1,1)

% Now for rows 2 onwards

elseif 2<=temp_neigh_r & temp_neigh_r<rdimension & 2<=temp_neigh_c  &
temp_neigh_c<cdimension
      neigh_count(temp_neigh_r,temp_neigh_c)=(intial_structure(temp_neigh_r-
1,temp_neigh_c-1,1)...
      +intial_structure(temp_neigh_r-1,temp_neigh_c,1) ...
      +intial_structure(temp_neigh_r-1,temp_neigh_c+1,1)...
      +intial_structure(temp_neigh_r,temp_neigh_c-1,1) ...
      +intial_structure(temp_neigh_r,temp_neigh_c+1,1)...
      +intial_structure(temp_neigh_r+1,temp_neigh_c-1,1) ...
      +intial_structure(temp_neigh_r+1,temp_neigh_c,1) ...
      +intial_structure(temp_neigh_r+1,temp_neigh_c+1,1))
```

```
else
end

end
end

%for column 1 and cdimension
temp_neigh_c=1
for temp_neigh_r=(2:1:rdimension)
   neigh_count(temp_neigh_r,temp_neigh_c)=8
end

temp_neigh_c=cdimension
for temp_neigh_r=(2:1:rdimension)
   neigh_count(temp_neigh_r,temp_neigh_c)=8
end

%for rdimension
temp_neigh_r=rdimension
for temp_neigh_c=(2:1:cdimension)
   neigh_count(temp_neigh_r,temp_neigh_c)=8
end


%intial_structure(:,:,3)= neigh_count (:,:)
%defining Ep and Ee
%bond_pair_potential
bond_pair_pt=2000
Ep(:,:)=bond_pair_pt*neigh_count (:,:)

image(intial_structure(:,:,1),'CDataMapping','scaled')
axis image

axis image

pause(0.5);

frame = getframe;
aviobj = addframe(aviobj,frame);

else
end

else
end
end
```

Appendix 2
Focused ion beam system

Focused ion beam (FIB) systems are similar to scanning electron microscopes in that they involve rastering a beam of focused ions (rather than electrons) over a sample. The ions are field extracted from a liquid metal ion source that consists of a tungsten needle with a radius of curvature of 1 μm that is wetted by a liquid metal. The application of an electric field ($>10^8$ cm/V) to the wetted tip results in the formation of a Taylor's cone with a radius of curvature of 10 nm from which the ions are field extracted. The most commonly used liquid metal is Ga since it is liquid almost at room temperature. Other metals, which have been used, include In, while alloy sources such as Co/Nd, Au/Si or Pd/As/B have also been used in conjunction with a mass separator in the ion column. The extracted ions are accelerated, collimated and focused by a series of apertures and electrostatic lenses. Typically the accelerating voltage used ranges from 5 to 30 keV and, depending on the size of the aperture and the strength of the lenses, beam currents from 1 pA to 20 nA with corresponding spot sizes of approximately 10 nm to 500 nm are possible. On penetrating a solid an accelerated ion transfers energy to the solid which can result in the formation of collision cascades and, for events close to the surface of the solid, the emission of ions, atoms and electrons. The emitted electrons or ions can be collected to form an image, as the ion beam is rastered over the surface of the solid. Depending on the material being imaged and the spot size of the beam the resolution of a typical system for the electron or secondary ion imaging modes can be 10 nm and 100 nm, respectively.

The position of the ion beam can be controlled by electrostatic deflector plates and depending on the dwell time, i.e. the dose, at each pixel a system can be used to either implant or sputter away material in user defined areas. Capability of removing material in user defined areas make FIB very useful for failure analysis. A FIB system can also be used to deposit metals or insulators in user defined areas. Typically a gas precursor, such as an organo-organic metallic compound, is bled into the chamber of the system, usually via a fine needle inserted to within 100 μm of the position of the ion beam, and this is broken down by the ion beam to deposit the metal or the insulator with the volatile products being pumped away. Commonly

deposited metals are platinum and tungsten while a commonly deposited insulator is SiO_2. In addition, gases such as iodine or xenon difluoride can be bled into the chamber to chemically assist the milling of metals and insulators.

List of publications that were made in course of this work

Publications in journal

1. A.V.Vairagar, S. G. Mhaisalkar, E. Zschech, A. M. Gusak "A simple model to understand electromigration-induced voiding in dual in-laid Cu interconnect structures," *submitted to Applied Physics Letters.*

2. A.V.Vairagar, Z. H. Gan, S. G. Mhaisalkar, Ahila Krishnamoorthy, K. N. Tu "Effect of surface treatment on reliability of sub-micron Cu dual-damascene interconnect structures", *to be submitted*

3. M. Y. Yan, K. N. Tu, A.V.Vairagar, S. G. Mhaisalkar, Ahila Krishnamoorthy, "Void confinement in Cu interconnect structure by embedded Ta layer," *accepted in Applied Physics Letters.*

4. M. Y. Yan, K. N. Tu, A.V.Vairagar, S. G. Mhaisalkar, Ahila Krishnamoorthy, "A direct measurement of electromigration induced drift velocity in Cu Dual Damascene Interconnects," *accepted in J. Microelectronics Reliability.*

5. M. Y. Yan, O. Suh, F. Ren, K. N. Tu, A.V.Vairagar, S. G. Mhaisalkar, Ahila Krishnamoorthy, "Effect of Cu_3Sn coatings on electromigration lifetime improvement of Cu dual-damascene interconnects," *Applied Physics Letters, Nov. 2005, in press.*

6. A.V.Vairagar, S. G. Mhaisalkar, Ahila Krishnamoorthy, M. A. Meyer, E. Zschech, K.N. Tu, A. M. Gusak, "Direct evidence of electromigration-induced failure mechanism in Cu interconnect tree structures," *Applied Physics Letters, Aug. 2005, in press.*

7. E. Zschech, M. A. Meyer, S. G. Mhaisalkar A.V.Vairagar, A. Krishnamoorthy, H.J. Engelmann and V. Sukharev "Effect of interface modification on EM-induced mechanisms in Cu interconnects, *Thin Solid Films, Oct. 2005, in press.*

8. A.V.Vairagar, S. G. Mhaisalkar, Ahila Krishnamoorthy, M. A. Meyer, E. Zschech, "Reservoir effect in dual-damascene Cu interconnect tree structures", *Microelectronic Engineering, Vol. 82, 2005, p.675.*

9. E. Zschech, H-J Engelmann, M. A. Meyer, V. Kahlert, A.V.Vairagar, S. G. Mhaisalkar, Ahila Krishnamoorthy, M. Y. Yan, K. N. Tu and V. Sukharev, "Effect of interface strength on electromigration-induced inlaid copper interconnect degradation: Experiment and simulation," *Z. Metallkunde, International journal of materials research, Vol. 69, 2005, p. 96.*

10. C. Tan, Arijit R, A.V.Vairagar, Ahila Krishnamoorthy, S. G. Mhaisalkar, "Effect of current crowding on copper dual damascene via bottom failure for ULSI applications", *IEEE Trans. Dev. Mat. Rel, Vol. 5, 2005, p.198.*

11. Wei Shao, A.V.Vairagar, Chih-Hang Tung, Ze-Liang Xie, Ahila Krishnamoorthy and S.G. Mhaisalkar, "Electromigration in copper damascene interconnects: reservoir effects and failure analysis", *Surface and Coatings Technology, Vol. 198, 2005, p. 257.*

12. A.V.Vairagar, S. G. Mhaisalkar, Ahila Krishnamoorthy, K.N. Tu, A. M. Gusak, Moritz Andreas Meyer, Ehrenfried Zschech, "In-situ observation of electromigration induced void migration in dual-damascene Cu interconnect structures," *Applied Physics Letters, Vol. 85, 2004, p.2502*

13. A.V.Vairagar, S. G. Mhaisalkar and Ahila Krishnamoorthy, "Effect of surface treatment on electromigration in sub-micron Cu damascene interconnects", *Thin Solid Films, Vol. 462-463, 2004, p.325.*

14. A.V.Vairagar, S. G. Mhaisalkar and Ahila Krishnamoorthy, "Electromigration behavior of dual-damascene Cu interconnects - Structure, width, and length dependences," *J. Microelectronics Reliability Vol. 44, 2004, p. 747.*

Invited talk in international conference

1. S.G. Mhaisalkar et al. "Understanding the impact of surface engineering, structure, and design on electromigration through Monte Carlo simulation and in-situ SEM studies", *Invited talk, 8th International Stress Workshop on Stress-Induced Phenomena in Metallization, 2005, Germany, in press.*

2. E. Zschech, M. A. Meyer, S. G. Mhaisalkar A.V.Vairagar, A. Krishnamoorthy, H.J. Engelmann and V. Sukharev "Effect of interface modification on EM-induced mechanisms in Cu interconnects," *Invited talk, International Conference on Materials for Advanced Technologies 2005, Singapore.*

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