An Ultra Low-Power Successive Approximation ADC Using an Offset-Biased Auto-Zero Comparator

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Abstract – **This paper presents a new offset-biased auto-zero comparator for the design of an ultra low-power charge redistribution Successive Approximation Analog-to-Digital Converter (SA-ADC) dedicated to biomedical applications. The circuits are realized in CSM 0.18μm CMOS technology. The simulated results have shown that the power consumption of the 10-bit ADC is only 6.2μW at a single supply of 1.8V whilst sampling at a frequency of 64kHz, with conversion time of 187.5μs. The energy per quantization level is less than 0.1pJ/level.**

I. INTRODUCTION

An advancement of portable biomedical devices has pushed integrated circuits towards very low power consumption in order to extend operation time of battery. Hence, power, resolution and speed become the important performance parameters in the specifications for nowadays biomedical-based ADCs. Of the available ADC topologies, the SA-ADCs are well known for low-power operation and they can deliver 8-10 bits resolution [1]. Among the designs, the comparator plays a critical role in affecting overall power consumption. In this paper, the circuit techniques for the design a new offset-biased auto-zero comparator are proposed to further reduce the power consumption whilst yet offering reasonable good conversion time, contributing a good power-speed SA-ADC in comparison with state-of-art works.

II. SYSTEM DESIGN

The architecture of unipolar charge redistribution SA-ADC [2] together with split-capacitor array [1] for area efficiency is presented in Fig. 1 whilst the new comparator with respective building blocks is shown in Fig. 3, Fig. 4 and Fig. 5. The key advantage of the architecture is that it eliminates a dedicated sample-and-hold circuit to conserve power [3], which is favorable in biomedical applications.

The operation of ADC starts by charging the capacitors to input voltage, V_{in} while the comparator is being reset by switch S1, and at this juncture the sample-and-hold function is being performed by the capacitor array by connecting switches S2 and S3 to V_{in}, in conjunction with the amplifier. The next step is to hold the input voltage on the capacitor array, which is done by turning the comparator out of reset first and then switching the bottom plates of the capacitors to ground potential. Finally, the switch S2 is switched to reference voltage, V_{ref} so that the successive approximation bit cycling can be performed on each bit, at this point switch S3 is connected to ground potential. The binary search is then conducted. First by assuming the MSB is logic 1, the bottom plate of the largest capacitor is connected to V_{ref}. When V_{DAC} is negative, it is confirmed that the MSB is logic 1. On the contrary, when V_{DAC} is positive, the MSB is logic 0. The similar procedure repeats 10 times to obtain the complete digital output logic. The voltage at the upper plates of the capacitor array is given as follows:

$$V_{DAC} = -V_{in} + V_{ref} \cdot \sum_{k=0}^{N-1} bit_k \cdot 2^{-(k+1)} \qquad (1)$$

where, bit_k is the digital output logic generated at the ADC output at each bit cycling process. At the end of the conversion, V_{DAC} can be approximated equal to zero.

III. COMPARATOR DESIGN

A. Comparator

For ADC architecture, the comparator is often regarded as the critical performance limiting block, which in general determines the major performance of data converters, including the maximum sampling rate, bit resolution and power consumption [3]. A commonly-used topology for realizing a high-speed, high-resolution comparator consists of a preamplifier employing offset storage followed by a regenerative latch [4]. Of particular interest is the fact that it is also a useful circuit topology for ultra low-power comparator design in biomedical circuit. Fig. 2 shows the basic comparator topology employing a preamplifier followed by a track-and-latch circuit. A track-and-latch circuit provides rail-to-rail output voltage swing but it may have a large input offset. Hence, a high-gain preamplifier at the expense of decreasing speed is needed to reduce the latch input offset. For preamplifier offset, two most common offset cancellation methods are considered. They are input offset storage (IOS) and output offset storage (OOS) [4]. IOS is preferable because of large input common-mode range, which is favorable for low voltage operation in the biomedical circuit. The implementation of IOS is shown in Fig. 1 whereas the analysis of the residual input-referred offset in the blocks of IOS comparator in Fig. 2 shows that

$$V_{OS} = \frac{V_{OSP}}{1 + A_o} + \frac{\Delta Q}{C} + \frac{V_{OSL}}{A_o} \qquad (2)$$

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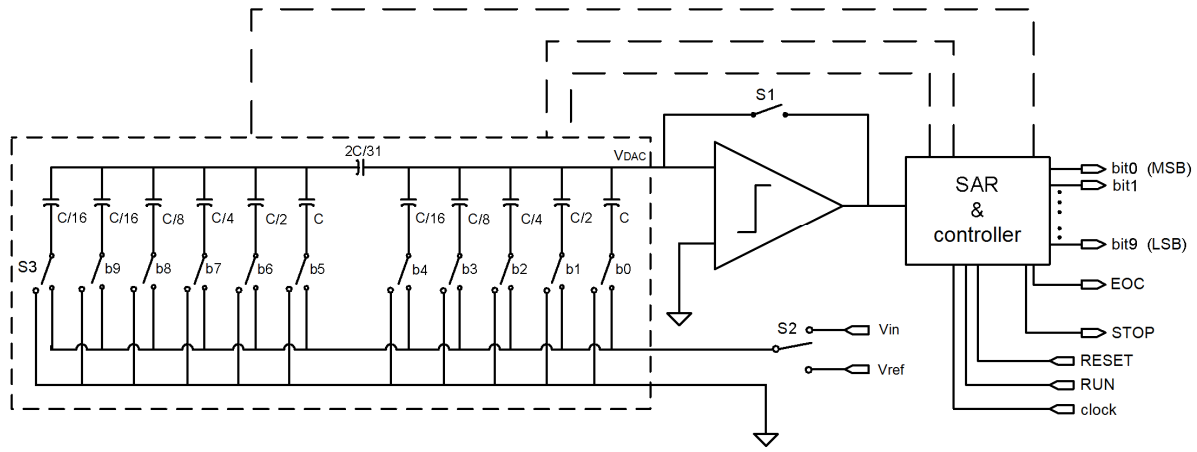


Figure 1. Successive approximation ADC architecture using the proposed ground-reference auto-zero comparator

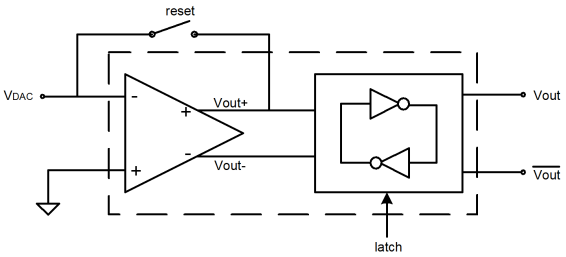


Figure 2. Auto-zero comparator circuit topology using preamplifier and track-and-latch

where V_{OSP} and A_o are the input offset and gain of preamplifier, respectively, ΔQ is the residual charge injection from switch S1 onto the capacitor, and V_{OSL} is the latch offset. As can be seen in the first term in (2), it is favorable to have high open-loop gain of preamplifier to suppress the offset arising from the gain error of pre-amplifier. Although the multistage amplifier for comparator design [5] can offer high-speed low-power operation, it may cause potential gain error because of finite open-loop gain. It can be significant if the gain is small. For instance, a 10mV preamplifier offset in a gain of 5 leads to a gain error of 2mV offset being stored in the capacitor, thus jeopardizing the resolution significantly if the design were not properly addressed the issue.

B. *Offset-Biased Auto-Zero Preamplifier*

The proposed offset-biased auto-zero preamplifier is presented in Fig. 3. It is formed by an offset-biased source follower stage together with a cascode single differential stage. The current sources are designed using micropower approach [6]. The techniques to reduce the power are to minimize the number of references and to bias transistors in weak inversion. A ground-reference comparator benefits from stated advantage but it causes the transistors out of desired active region during reset because the output node as well as input nodes of the comparator is forced close to ground potential, dropping the gain of amplifier. To alleviate the problem, an intentional dc offset biased at the input of amplifier permits the transistors operating in proper region through adding an offset-biased source follower formed by M1, M3 and I_B and another standard source follower formed by M2 and I_B. Despite the intentional one-diode offset may lead to gain error, the gain A_o of preamplifier is dedicatedly designed to be 60dB or above in order to adequately suppress the gain-induced offset error to about 0.4mV. Herewith, high gain is achieved by employing composite transistors [7] M4-M6, M5-M7, M8-M10 and M9-M11 in the single-pole differential stage. As a result, based on (2), the first term is reduced significantly whereas the second term can be reduced via suitable dummy switch compensation. Finally, the third term becomes negligible even for case of large-offset (typically from 75 mV to 300 mV) dynamic comparators [8]. Besides using cascode structure to achieve fast settling, the speed of the comparator is further improved through clamping the output swing of preamplifier. M12 is added to limit the maximum output swing to about 0.8V. This yields the output swing of about +/- 0.4V at quiescent dc operating point of about 0.4V.

C. *Track-and-Latch Circuit*

The track-and-latch circuit [2] depicted in Fig. 4 amplifies preamplifier output signal during track phase and amplifies it again during latch phase when positive feedback is enabled. The positive feedback regenerated the analog signal into a full-scale digital signal. The input voltages that trigger track-and-latch are obtained from the outputs of preamplifier. The preamplifier output, V_{out+} is connected to V_{in+} input of track-and-latch, while the other input is triggered by V_{out-} from preamplifier, which has a value close to the threshold voltage of track-and-latch input transistor. The track-and-latch circuit is controlled by a latch signal. When the latch signal is low, the internal associated nodes are forced to either V_{DD} or ground so as to ensure that no hysteresis is transferred from one decision cycle to the next. Unfortunately for case of low-frequency clock, when the latch signal is high, there is a significant amount of power dissipated in the circuit due to the turning on of associated devices which establishes a dissipating current path from supply to ground under long duration of the half clock signal. This problem can be solved by adding a narrow pulse latch clock generator as shown in Fig. 5, which aims to reduce power drain by clocking the circuit for a short period only in latch mode. As illustrated in Fig 6, the original 32 kHz clock turns latch mode on for 15.625 µs, while the modified clock turns latch mode on for only 18.162 ns in the design. As a consequence, the narrow pulse latch clock generator doubles the original 32 kHz clock frequency to a sampling frequency of 64 kHz. The reduction of power is significant, especially for low clock frequencies.

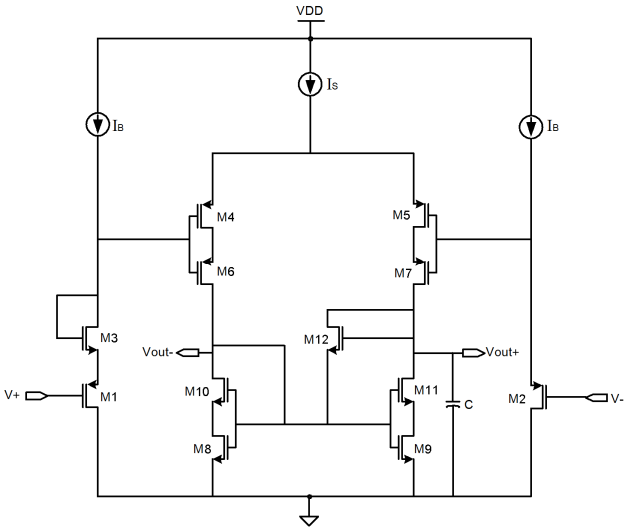


Figure 3. Offset-biased preamplifier for auto-zero comparator

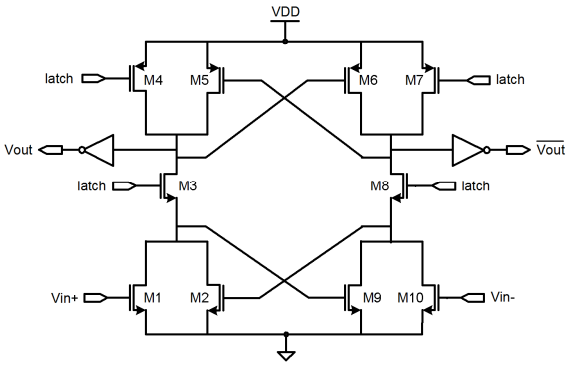


Figure 4. Track-and-latch for auto-zero comparator

IV. RESULTS AND DISCUSSIONS

The transistor-level simulations for the ADC were conducted using realistic BSIM3 models for CSM 0.18µm CMOS technology. Fig. 7 shows the outputs of ADC under an exemplary input signal of 0.75 V_{ref}. The bit outputs 1100000000, respective clock signal and output End-of-Conversion (EOC) signal confirm the operation of the ADC. Table I and Table II have summarized the performance parameters for comparator and ADC at ultra low-power condition. Comparing the two-stage design in comparator, the response time of comparator is dominated by the preamplifier stage since the track-and-latch stage is fast in general. Fig. 8 shows the response time of preamplifier. Besides, the Figure-of-Merit (FOM) used for assessing ADC performance is

$$FOM = \frac{P_{tot}}{2^{bit} \cdot F_s} \quad (3)$$

where P_{tot} is the total power dissipation, *bit* is the ADC bit resolution and F_s is the sampling frequency. The lower the FOM, the better the energy efficiency is. As can be seen in Table III, the SA-ADC incorporating a new offset-biased auto-zero comparator has achieved significantly optimal good results in terms of resolution, power consumption and speed when compared to other previously published ADC works [9]-[10]. It further confirms that the proposed ultra low-power ADC has achieved better efficiency in energy per quantization level.

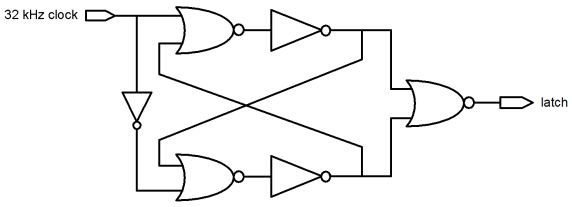


Figure 5. Narrow pulse latch clock generator

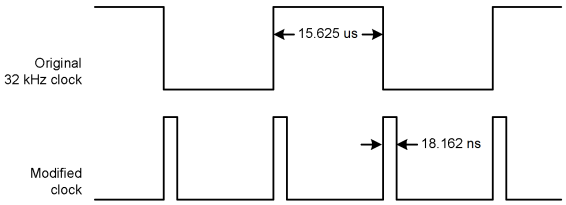


Figure 6. Input and output waveforms of Figure 5

Table I. Simulated comparator performance

Input voltage range		0 – 1 V
Offset voltage		0.78 mV
Response time of pre-amp.	Low-to-High	1.69 µs
	High-to-Low	0.26 µs
Output voltage range		0 – 1.8 V
Open loop gain		60.88 dB
Unity gain bandwidth of pre-amp. at load C=50 fF		3.1 MHz
Power at 1.8V supply		6.2 µW
Total static supply current (including biasing circuit)		3.45 µA

Table II. Simulated SA-ADC performance

Power at 1.8V supply (without voltage reference)	6.2 µW
Total drain current (without voltage reference)	3.45 µA
Input voltage range	0 – 1.26 V
DNL	0.625 LSB
INL	1.115 LSB
Sampling rate	64 kHz
Conversion time	187.5µs

Table III. Performance comparison with reported ADC works

Parameters	Ref. [9]	Ref. [10]	This work
Technology	BiCMOS 0.8 µm	CMOS 0.18 µm	CMOS 0.18 µm
Supply voltage (V)	2.8	1	1.8
Sampling rate (kHz)	32	150	64
Resolution (bit)	10	9	10
Power (µW)	17.9	30	6.2
FOM (pJ/level)	0.55	0.39	0.095

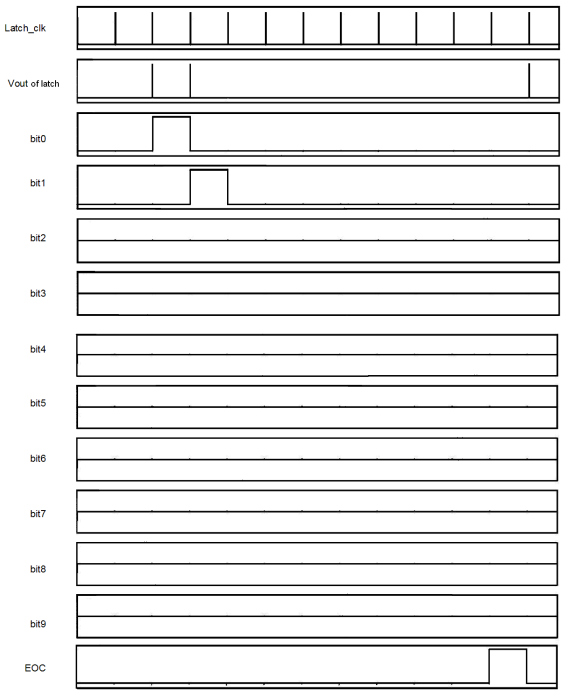
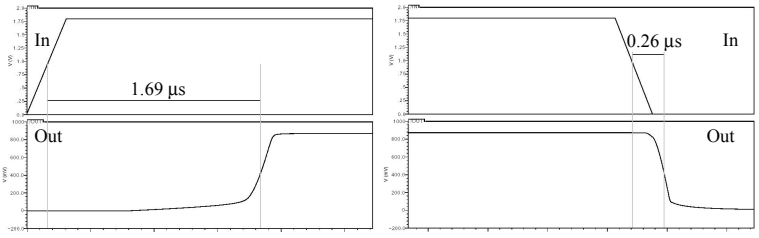


Figure 7. Output waveforms of SA-ADC for V_{in}=0.75 V_{ref}

V. CONCLUSION

A new ultra low-power op-amp based comparator is proposed. Combining this dedicated building block for the design of charge redistribution SA-ADC, it displays very low energy per quantization level in comparison to prior-art works. It is particularly useful for biomedical data acquisition applications that require higher sampling rate while yet meeting the power demand in micropower level.



(a) (b)

Figure 8. Preamplifier response time:
(a) Low-to-high output (b) High-to-low output

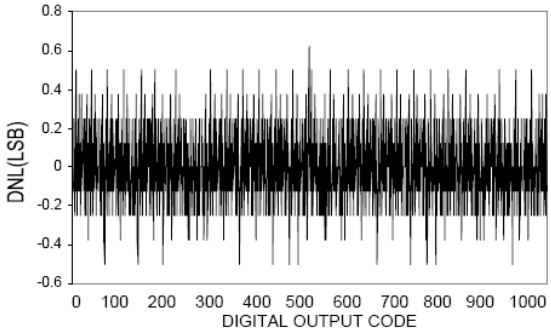


Figure 9. Differential nonlinearity vs. digital output code

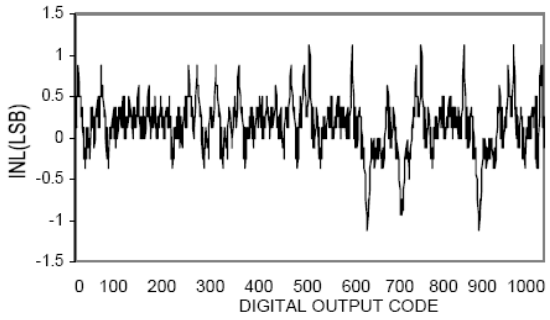


Figure 10. Integral nonlinearity vs. digital output code

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