A Low-Jitter and Low-Reference-Spur 320 GHz Signal Source With an 80 GHz Integer-*N* Phase-Locked Loop Using a Quadrature XOR Technique

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***Abstract*—This paper reports a 320 GHz low-jitter and low-reference-spur signal source consisting of an 80 GHz integer-*N* phase-locked loop (PLL) and a 320 GHz frequency quadrupler. The 80 GHz PLL features a novel dual-path quadrature exclusive-OR (QXOR) technique to cancel the spurs at the reference frequency and its harmonics, enabling low-spur and low-noise phase locking. The proposed PD also enables frequency detection and lock detection, rendering the band-searching to be decoupled from the loop components. Implemented in a 0.13-µm SiGe BiCMOS technology, the proposed signal source shows a −73.1 dBc reference spur, –113.7 dB/Hz phase noise at 1-MHz offset at 40.96 GHz, and –90.3 dB/Hz phase noise at 1-MHz offset at 311.8 GHz. It achieves an integrated jitter of 66.9 fs_{rms} at 40.96 GHz, and 122 fs_{rms} (both integrated from 10 k to 100 MHz) beyond 300 GHz, with a total division ratio of 512. The lock detection time is at the microsecond level. The maximum output power is –3.24 dBm, and the power consumption is 372 mW.**

***Index Terms*—BiCMOS, exclusive-OR gate, frequency detector, harmonic cancellation, lock detector, phase detector, phase-locked loop, jitter, terahertz, phase noise.**

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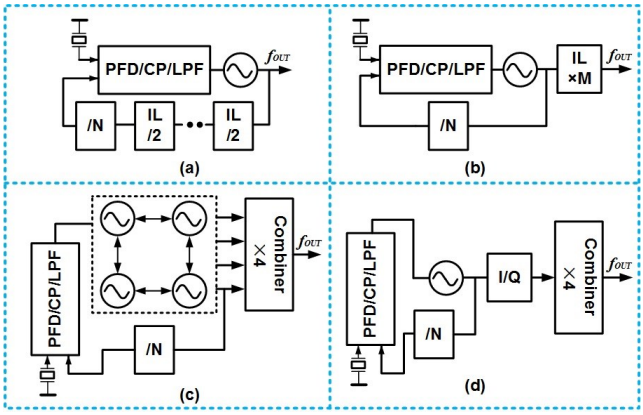

Fig. 1. THz signal source based on: (a) fundamental VCO [15]–[17], (b) injection-locked frequency multiplier [18], [19], (c) coupled oscillator network [21], and (d) proposed I/Q hybrid.

I. Introduction

The recent efforts on integrated circuits and systems operating toward terahertz (THz) frequency range have unlocked various useful and emerging applications, such as 240-/300-GHz short-range high-speed wireless interconnects [1], [2], and THz rotational spectroscopy imaging [3], [4]. In these systems, a wideband, low-spurious-tone, low-phase-noise, and high-output-power signal source is critical to increase their data rate to tens of Gb/s, or to enhance detection sensitivity to −100 dBm or below [5], [6]. For these purposes, a stabilized signal source, such as a phase-locked loop (PLL) is highly favored over a free-running voltage-controlled oscillator (VCO) owing to its precise frequency control, signal integrity, and low integrated root-mean-square (RMS) jitter. This has led to the growing need for signal sources incorporating with PLLs to operate toward hundreds of gigahertz. Although THz signal sources were traditionally implemented by expensive and power-hungry compound semiconductors [7], silicon technologies including CMOS and SiGe BiCMOS are deemed to be the ultimate low-cost, low-power yet high-integration solutions. The SiGe BiCMOS technology is preferred for this frequency range due to its higher f_T/f_{max} and the higher breakdown voltage of the heterojunction bipolar transistor (HBT).

Recently, several stabilized THz signal sources have been reported in silicon [8]–[12]. A 283-GHz PLL employing a triple-push VCO was reported in [8], but the in-band phase noise was −53.5 dBc/Hz at 100 kHz offset. A 300-GHz frequency synthesizer incorporating a triple-push VCO

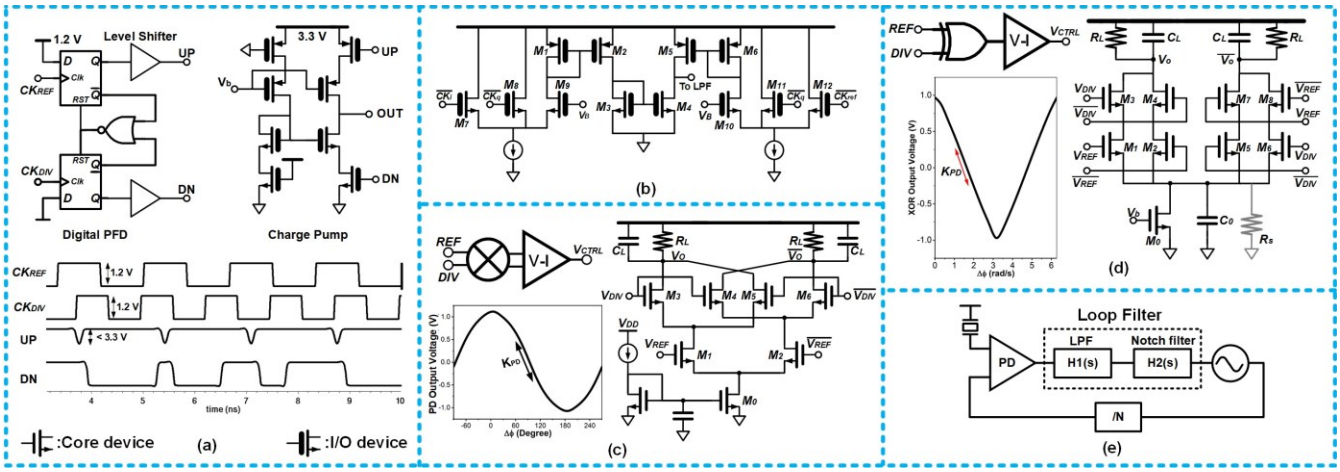

Fig. 2. Phase detectors: (a) digital phase frequency detector (PFD), charge pump (CP) [23], and waveform of PFD, (b) analog phase detector [24] built with I/O devices, (c) Gilbert-cell mixer phase detector [7], [25] and its output characteristic, (d) XOR gate phase detector and its output characteristic, and (e) a PLL with a notch filter after the PD [28].

achieved a wide locking range of 7.9% [9], but it generated only −14 dBm output power with 0.01% peak DC-to-RF efficiency. A 560-GHz frequency synthesizer was demonstrated in [10] with an operation range of 21 GHz, but two triple-push Colpitts oscillators were used to isolate the parasitic loading. A mixing-based frequency synthesizer was proposed in [11] to lock a transmitter at 208–255 GHz, but it consumed 1.4 W power. A dividerless quadruple-push signal source employing an on-chip frequency-stabilization feedback loop without a reference clock was realized from 302 to 332 GHz in [12]. However, the stabilized tuning range was limited by the bandwidth of the filter. Moreover, using a variable input current for reference, its output frequency could not be precisely controlled.

This paper aims to develop a low jitter, low reference spurs, and high output power 320 GHz signal source in a 0.13-μm SiGe BiCMOS technology. Motivated by the recent development of low-jitter PLLs operating at the multi-gigahertz frequencies, a plausible approach to lower the N^2 in-band noise multiplication is to raise the reference frequency [13]. This calls for a high-speed phase detector (PD) capable of responding to the high-frequency reference yet generating desired noise level with minimal reference spurs. A dual-path quadrature exclusive-OR (QXOR) gate technique is proposed for serving these purposes by extending the fundamental principle of the traditional single-path XOR-gate PD. The operation of QXOR also enables fast-locking frequency detection (FD) and lock detection (LD). A 320 GHz frequency quadrupler based on a two-stage passive *RC* polyphase shifter is introduced.

In this manuscript, we extend our recent conference presentation in [14] with the following key additions:

1. Design consideration for the THz source architecture with comparisons with conventional arts. (Section II)
2. Detailed analysis of the fundamental trade-offs in conventional PDs, conceptualizes and elaborates the proposed dual-path QXOR PD. (Section III)
3. Extensive performance comparison between the proposed QXOR PD and conventional PDs, followed by the description of PLL loop dynamics. (Section IV)
4. Detailed description of the dual-path QXOR-based FD and LD, and the THz circuits. (Section V).
5. Update the measurement results and comparison tables for both 80 GHz PLL and 320 GHz signal source; more testing results are provided and compared. (Section VI)

Finally, this paper is concluded in Section VII.

II. THz Signal Sources Architecture

The systematic architectures of THz signal sources can be categorized into four versions as summarized in Fig. 1. The most direct way is to implement a PLL operating at the desired frequency [15]–[17], as depicted in Fig. 1(a). This approach has a worsened phase noise due to the use of a fundamental VCO in which the tank quality factor is severely degraded by the varactor. Using high-frequency dividers such as the injection-locked frequency dividers (ILFD) suffers from narrow locking ranges, necessitating cumbersome tuning. In contrast, the topology sketched in Fig. 1(b) utilizes a low-frequency PLL followed by multi-stage injection-locked frequency multipliers (ILFMs) [18], [19]. Using a low-frequency VCO, this method improves the phase noise of the system and omits the need for ILFDs. However, it raises similar locking-range issues at ILFM as ILFD, introducing large spurs at the output. ILFM realized by using the quadrature injection locked oscillator (QILO) has the benefit of low in-band phase noise and small power consumption [20], yet it may cause the misalignment between the PLL output frequency and the QILO natural oscillation frequency, potentially demanding both amplitude and frequency calibration with extra circuit complexity. The topology depicted in Fig. 1(c) utilizes a coupled-oscillator-network operating at a moderate frequency with *N*-phase-coupled oscillator units, generating the output frequency *N* times of the PLL output frequency through phase combining. This approach has the benefit of *N* times noise reduction by self-synchronizing each oscillator unit-cell in a loop [21]. However, the coupled-oscillator-network consumes *N* times more power than a single oscillator unit-cell. Moreover, the routing in the practical layout makes the symmetry difficult, degrading the noise and introduces phase error between each oscillator core. The harmonic frequency can also be extracted directly from the VCO tank [22]. However, as the drain current's waveform is nearly square-wave for a typical *LC* oscillator operating in the

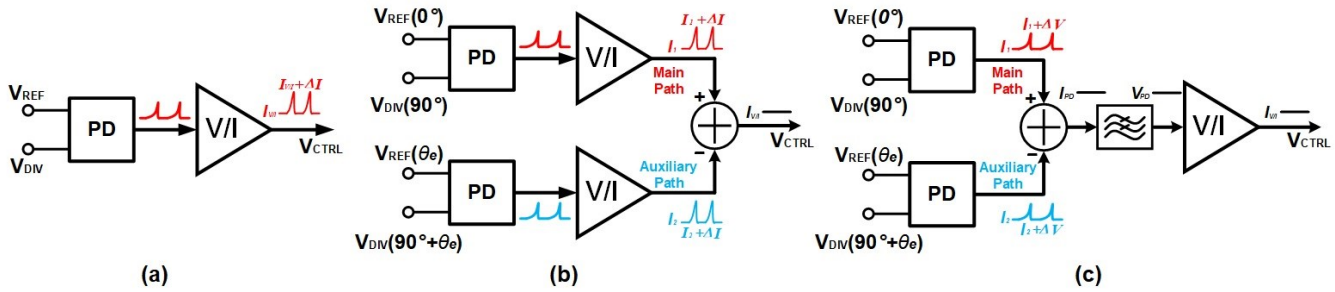

Fig. 3 (a) Block diagram of conventional single-path PD, (b) proposed dual-path PD with spur cancelling, and (c) simplified version of (b).

current-limited region, the ratio of the 3rd harmonic current to the 1st harmonic current is limited to 33%. Moreover, depending on the transformer coupling coefficient k, a tradeoff exists between the fundamental and third-harmonic equivalent parallel tank resistances R_{D1} and R_{D3}. A larger k leads to a larger R_{D1} yet a smaller R_{D3}, demanding more power to sustain a higher third-harmonic oscillation.

Considering the above tradeoffs, this work proposes a THz signal source architecture to balance phase noise, reference spurs, power consumption, and operating bandwidth. As shown in Fig. 1(d), the proposed topology obviates the need for narrow-band injection-locking techniques by utilizing a PLL operating at a moderate frequency of 80 GHz, followed by a frequency quadrupler. The frequency quadrupler is featured by an I/Q hybrid which generates a quadrature-phase, and two stages of frequency doubler. Since only one VCO is used, full symmetry is guaranteed, and the power consumption is smaller than the counterpart in Fig. 1(c). Moreover, since no calibration circuitry or band tuning is required at the prescaler or the frequency multipliers, the system complexity is much simpler than the topologies shown in Fig. 1(a) and (b).

Choosing the proposed architecture in Fig. 1(d) raises several concerns. Since a high frequency of 600-MHz is chosen for the reference in this work, the noise and spurs generated by PD become critical, which will be discussed in the next Section. Besides, the quadrature-phase error of the I/Q hybrid should be carefully examined. This part will be addressed in Section V-C.

III. Dual-path QXOR Phase Detector

The proposed THz source architecture in Fig. 1(d) brings us four design goals for the 80 GHz PLL: 1) high supply voltage is used to drive the VCO, 2) wide loop bandwidth (f_{BW}), 3) small reference spurs, and 4) low phase noise. In detail, 1) effectively reduces the VCO gain (K_{VCO}), yet maintaining the desired frequency tuning range, 2) aims to suppress more VCO noise, while 3) and 4) are mandatory for high-performance PLLs.

A. Design Considerations for PD

The above four design goals are highly related to the design choice and performance of PD. The topologies of traditional PDs including digital phase frequency detector (PFD) [23], analog PD [24], Gilbert-cell mixer PD [7], and XOR-gate PD, are summarized in Fig. 2(a)–(d). In general, a PD needs to sense the input phase error (ϕ_e) and generates proportional error information at the output to drive the subsequent V/I converter. This aspect leads to the first design goal. In recent SiGe PLL designs, the supply voltage of the V/I converter is raised much higher than the normal voltage applicable to core transistors [25]. In Fig. 2, both the digital PFD and analog PD need to generate narrow pulses, demanding a power-hungry voltage level shifter, whereas mixer PD and XOR PD converts ϕ_e into output voltage error without pulse generation. Using thick-oxide I/O transistors for digital PFD and analog PD suffer from power penalty in exchange for speed. By contrast, the mixer or XOR PD can be designed by core transistors, while the V/I converter uses I/O devices. From this aspect, mixer PD and XOR PD are preferred to serve the design goal 1).

Due to the absence of high-quality passives in a high-frequency integrated PLL, the VCO phase noise, which is high-pass filtered in the PLL, will significantly degrade the PLL jitter performance, suggesting the need to increase f_{BW} for sufficient attenuation of the VCO noise. Yet, extending the PLL frequency roll-off to a higher frequency makes the PLL less effective to suppress the reference spur. Therefore, our design goals 2) and 3) fundamentally contradict each other. Although digital PFD/charge pump (CP) topology can introduce a negative feedback loop in the CP to reduce the skew between the pull-up and pull-down network [26], or translates the reference spurs to higher frequencies [27], these two methods still adopt small f_{BW} (< 500 kHz) for achieving <–60 dBc reference spurs. The channel length modulation of the pull-up network in analog PD causes the control-line ripple, posing a tradeoff between the PD noise and reference feedthrough [24]. For mixer PD and XOR PD, large damping capacitors are required at the PD output for spur suppression, but the level of spur rejection is marginal. With a wide f_{BW} of 47-MHz, the mixer PD incurs a –37 dBc reference spur [25]. An alternative approach, as shown in Fig. 2(e), is to add a passive notch filter after the PD to create a resonance path at f_{ref} [28]. However, the spur rejection level is limited to 7-14 dB at f_{ref}, and the filter inevitably introduces poles to the loop, degrading the loop stability and introduces more noise to the loop. This approach achieves the reference spur of –63.7 dBc in the best case, but a small loop bandwidth of less than 100 kHz is adopted.

In summary, none of the above PDs can simultaneously cope with our design goals 1) to 3).

B. Dual-path PD and Proposed QXOR PD

As depicted in Fig. 3(a), instantaneous glitches are generated at the PD output upon the edge of each clock transition, modulating the VCO control line voltage (V_{ctrl}) and translating to reference spurs. Intuitively, if such a path for phase detection is duplicated once to an auxiliary path, and their output currents are subtracted, one may perfectly cancel out the glitch if the two PD paths generate the in-phase glitches.

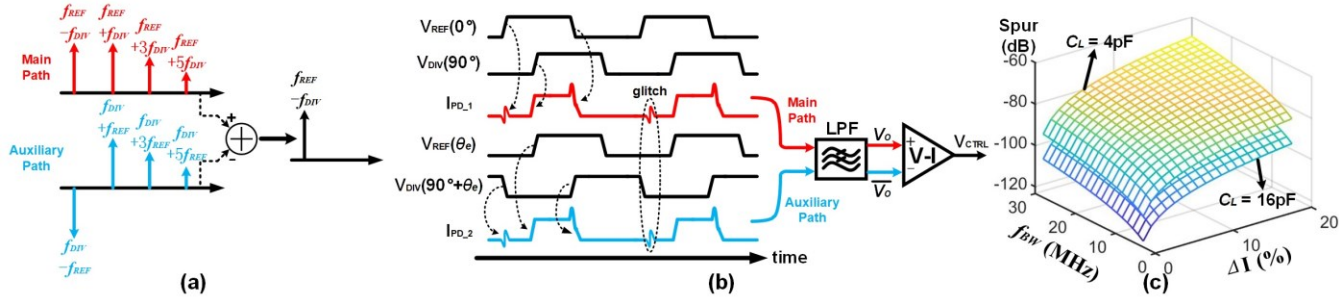

Fig. 4 (a) phasor diagram of the proposed dual-path PD, (b) its timing diagram at phase-locked, (c) reference spur against ΔI, f_{BW}, and C_L.

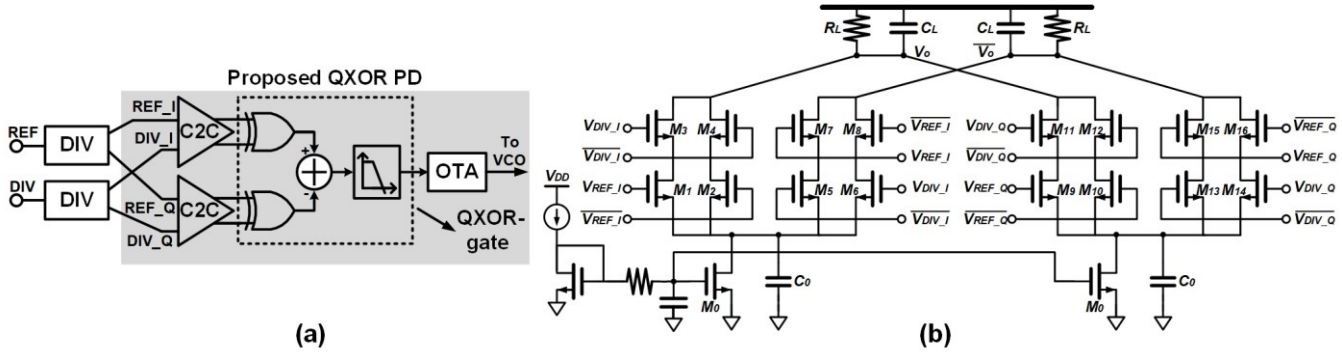

Fig. 5 (a) Block diagram of phase detection by the proposed QXOR PD, and (b) schematic of the proposed QXOR gate.

This idea is conceptualized in Fig. 3(b), where the main path is duplicated once to an auxiliary path, and each path generates the output DC current proportional to their respective input phase error, i.e. I_1 and I_2. There is a constant phase shift θ_e for the inputs between the two paths. As shown, θ_e is chosen such that the two paths generate instantaneous glitches in the same phase. The V/I circuit then converts the voltage into current, i.e., $I_1 + \Delta I$ and $I_2 + \Delta I$, respectively, for the main path and the auxiliary path, where ΔI is due to the glitches. The net current will be $I_{V/I} = I_1 - I_2$ and is free of ΔI in the absence of current mismatches.

Using such a dual-path PD provides several merits. First, it omits the need for the negative feedback loop with an operational amplifier as in digital PFD/CP, and is thus suitable for a wide range of V_{ctrl} to maintain the full effectiveness of spur cancellation. Second, the level of spur cancellation does not depend on the poles at the PD output, removing the need for a notch filter or large capacitors at the load. More importantly, the level of spur rejection now becomes decoupled from f_{BW} ($\propto I_{V/I}$). As a result, this approach breaks the tradeoff between the reference spur and f_{BW}.

The block diagram in Fig. 3(b) can be simplified to Fig. 3(c), where the two V/I converters are merged, and the spur cancellation takes place at the PD's output. Similarly, the glitch current generated by one PD will perfectly cancel out the counterpart generated by the other PD. The net current I_{PD} is then converted to a near-DC voltage V_{PD} by the subsequent low-pass filter (LPF). In that sense, mixer PD and XOR PD are feasible for such a dual-path PD concept.

The choice of θ_e can be determined by regarding the PD as a single-switch sampler. By applying two square pulses to the sampler, the output frequency components are expressed by the phasor diagram as shown in Fig. 4(a). Intuitively, except for the first term, each term expressed by sin(•) can be perfectly canceled by subtracting another counterpart in which the sampler is driven by two quadrature inputs. The resulting phasor diagram is shown in Fig. 4(a) as well. At the locked state, f_{REF} and f_{DIV}, which denotes the reference frequency and the divider output frequency, must be equal. The net effect is the mutual canceling of all frequency components, leaving only the near-DC term. Therefore, this configuration does not affect the normal operation of PD for frequency tracking or phase realignment, i.e., when $f_{REF} \neq f_{DIV}$. For these reasons, 90º is chosen for θ_e in such a dual-path PD.

The timing diagram for the dual-path PD is illustrated in Fig. 4(b). Upon the rising edge of clocks, the instantaneous glitch generated in the main path cancels out the in-phase glitch introduced by the auxiliary path. The PLL output spur can be quantized against ΔV_{ctrl} as follows, where ΔV_{ctrl} is the voltage disturbance on the VCO control line [28].

$$\mathrm{Spur}_{\mathrm{PLL}} = 20\log\left(\frac{K_{VCO}\times\Delta V_{ctrl}}{2\pi\times f_{REF}}\right) \quad (1)$$

For example, the closed-loop results in Section IV-A show only 42-μV ΔV_{ctrl} disturbed by the fourth harmonics of f_{REF}, translating to –85.5 dBc reference spur at the fundamental frequency (i.e., 80 GHz) for f_{BW} = ~5 MHz, while the spurs at f_{REF} to $3f_{REF}$ are fully canceled. The spur level at $4f_{REF}$ degrades slightly when f_{BW} expands to 10 MHz, while the spur from f_{REF} to $3f_{REF}$ remain being canceled. As a result, the spur cancellation is not affected by f_{BW}. In the presence of a current mismatch between the two paths, the unbalanced current ΔI degrades the reference spur, as illustrated in Fig. 4(c). While a smaller f_{BW} attenuates the spur due to the current mismatch, using a larger capacitance C_L at the load of PD also helps to reduce the reference spur with a negligible impact to f_{BW}.

All the above observations guide the circuit design of the dual-path PD. Using both square pulses for complete switching,

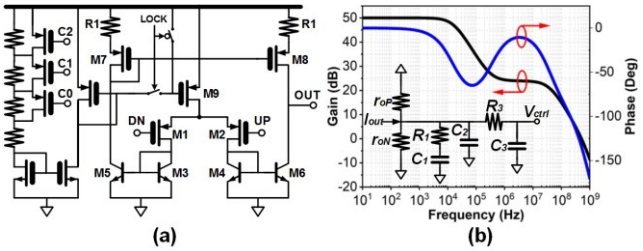

Fig. 6. (a) Operational transconductance amplifier (OTA) built with I/O devices, and (b) gain/phase plot of OTA+LPF (inset).

TABLE I

PERFORMANCE SUMMARY OF PDS

PD Type	PD Gain (V/rad)	PD+ V/I Gain K_{PD} (mA/rad)	PD Current (mA)	V/I Current (mA)
PFD_LV	$V_{DD}/2\pi$	0.47	Total: 32 mW	
PFD_HV	$V_{DD}/2\pi$	0.41	Total: 24 mW	
Analog PD	$V_{DD}/2\pi$	0.34	Total: 7.2 (3.3 V)	
Mixer	$\alpha A_1 A_2/2$	1.6	6 (1.2 V)	5 (3.3 V)
XOR	$2V_{DD}/\pi$	5.2	6 (1.2 V)	5 (3.3 V)
QXOR	$2V_{DD}/\pi$	5.0	6 (1.2 V)	5 (3.3 V)

the single XOR PD is chosen and extended to a dual-path XOR PD, forming a QXOR PD. The block diagram is provided in Fig. 5(a). It consists of two CML-to-CMOS (C2C) converters, dual XOR-gates loaded with one LPF, and one subsequent operational transconductance amplifier (OTA). Fig. 5(b) shows the differential QXOR PD circuit using core transistors, which combines two XOR-gate outputs in the current domain. The combined current then converts to a differential voltage V_{PD} by the output RC load. The quadrature signal is extracted from a static divider. Since the output swing of the static divider is relatively small (< 600 mV), and the flicker noise of the switched transistors in the QXOR PD are highly related to the input voltage swing, the C2C circuit ensures a rail-to-rail output swing and completely switches on/off the QXOR PD. A loading capacitor C_L can be utilized not only to suppress the glitches caused by any circuit asymmetry but also to reduce the PD high-frequency noise. Noise decomposition suggests that the tail current source M_0 contributes ~58% integrated noise from 1 kHz to 30 MHz. Instead, using a tail resistor for both paths reduces the integrated noise by 51%.

C. Noise Consideration and OTA

The proposed QXOR PD fulfills our design goal 1)−3). However, adding another path inevitably introduces 3 dB more noise at the output, thereby bringing us to the fourth design goal: low phase noise. The design target is to make the intrinsic noise of the QXOR PD fall below the reference input clock noise level. Once QXOR PD noise becomes negligible, the PLL in-band noise becomes dominated by reference clock noise. Meanwhile, as stated above, the PLL out-of-band noise, which is dominated by the VCO noise level, is suppressed by widening f_{BW} without affecting the level of spur rejection.

Random jitter (RJ) contributed by the PD is described by

$$\text{Noise}_{\text{OTA}} = 20\log\left(\frac{2\cdot\pi\cdot I_N\cdot N}{K_{PD}}\right) \quad (2)$$

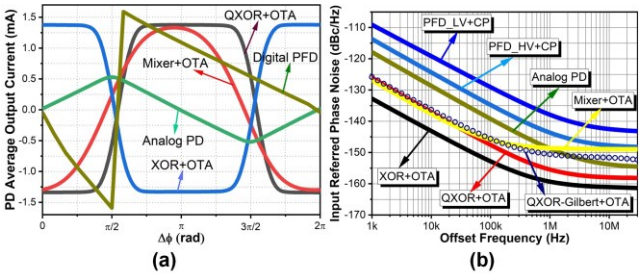

Fig. 7. (a) Simulated output characteristics of PDs, and (b) simulated input-referred phase noises (IRPN) of PDs.

where I_N represents current noise from the OTA in amperes. The PD+OTA in-band noise can be significantly reduced by increasing K_{PD} and adopting a higher reference frequency, where K_{PD} is enlarged by increasing the OTA output current. Moreover, the OTA intrinsically serves as a voltage level shifter and also decouples the VCO control line from the PD.

Since the QXOR PD is built using 1.2-V core transistors, the OTA, which operates under a 3.3 V power supply, should employ PMOS transistors as the input stage, as shown in Fig. 6(a). The LF gain can be digitally set by a 3-bit tuning (C0 − C2). OTA is disabled by the LOCK signal during band searching to prevent fighting between the PD and the frequency tracking loop (FTL). The current mirror is constructed using HBT M3−M6 and PMOS M7 and M8, where the flicker noise of M7 and M8 are attenuated by 40% through the source degeneration resistor R1. The flicker noise of the OTA is further reduced by 7 dB by taking the advantage of the low-flicker-noise feature of HBT M3−M6 compared with using NMOS transistors. Since OTA responds to a near-DC signal, the sizing of each device in QXOR PD and OTA becomes independent, both toward achieving the desired noise level, while maintaining low power operation. According to (2), the PLL division ratio N plays an important role in reducing the OTA in-band noise level. Noise analysis suggests that the in-band noise contributed from the QXOR PD + OTA is −115 dBc/Hz. This value is 7 dB lower than the reference clock noise plus 20log$N$, i.e., −108 dBc/Hz, satisfying our design goal 4) by choosing N = 128.

Noted that the XOR-gate in the proposed QXOR PD can be built using the Gilbert cell topology [Fig. 2(c)] as well. QXOR PD using the Gilbert cell as XOR-gate worsens the LF noise by 17% at 1 kHz offset, mainly due to the relatively small impedance at the source of the switching quad, which exacerbates the flicker noise up-conversion [29].

The simulated gain/phase of OTA+LPF is given in Fig. 6(b). r_{oP} and r_{oN} denote the equivalent small-signal output resistance of transistors M_8 and M_6, respectively. The OTA provides a small-signal gain of ~50 dB, which is adequate to raise the PD output voltage to the full swing, and therefore covers the whole tuning-voltage range of the VCO. The high near-DC gain makes the OTA output current becomes saturated easily even for a small input phase error, boosting the PD gain. The first pole is determined by $(r_{oP} \parallel r_{oN})\times C_1$, while $R_1\times C_2$ dominates the second pole. The serial combination of R_1 and C_1 provides a zero at $R_1\times C_1$ to compensate for the phase drop, stabilizing the loop. The third pole, determined by $R_3\times C_3$, is located at a higher frequency for further attenuation of the reference spurs.

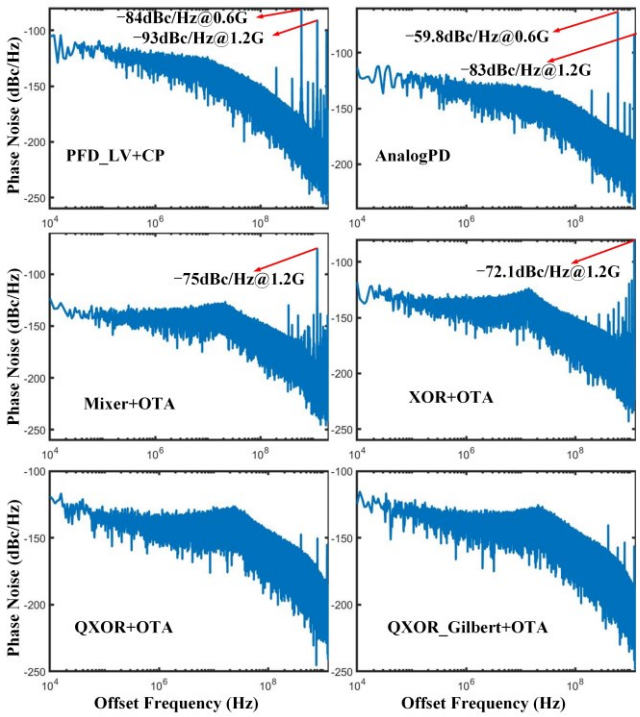

Fig. 8. Simulated phase noise and reference spur of PDs.

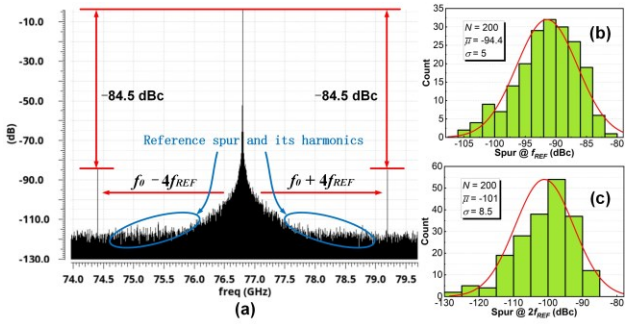

Fig. 9. (a) Simulated spectrum of the 80 GHz PLL output; simulated reference spurs (b) at f_{REF}, and (c) at $2f_{REF}$ over process spread.

The Monte-Carlo statistics of quadrature generation by the static divider show a small standard deviation of only 0.022° phase error. The dual-path PD, including the two static dividers, two C2C circuits, QXOR PD, OTA, and LPF generates a mean of 23 fs jitter with a standard deviation of 0.4 fs.

IV. Comparison of PDs and PLL Loop Dynamics

A. PD Performance Comparison

The analog PD in Fig. 2(b) is built with I/O devices and consumes a DC power of 23.7 mW from a 3.3 V power supply, driven by large signals (3.3 V voltage swing). Mixer PD, XOR PD, and the proposed QXOR PD all consume 6 mA currents from a 1.2 V power supply and drive a subsequent OTA, which consumes 5 mA from a 3.3 V supply. In mixer PD [Fig. 2(c)], the switching quad M3−M6 is driven by large square inputs, whereas the gain stage M1 and M2 receive a −15 dBm differential sinusoidal signal [25]. The QXOR PD is composed of two static dividers (1.2 mW), two C2C circuits (2 mW), and one QXOR gate [2.8 mW, Fig. 5(b)]. QXOR-Gilbert denotes the QXOR PD using the topology in Fig. 2(c), but all transistors

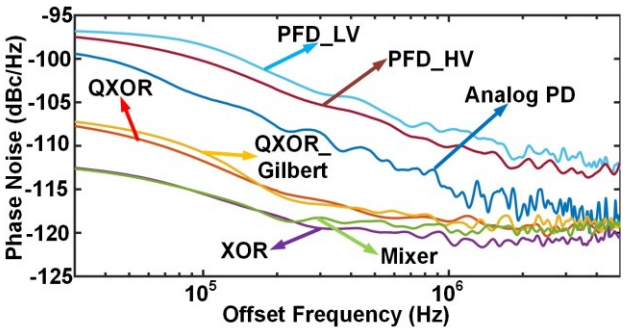

Fig. 10. Extracted phase noise from Fig. 8.

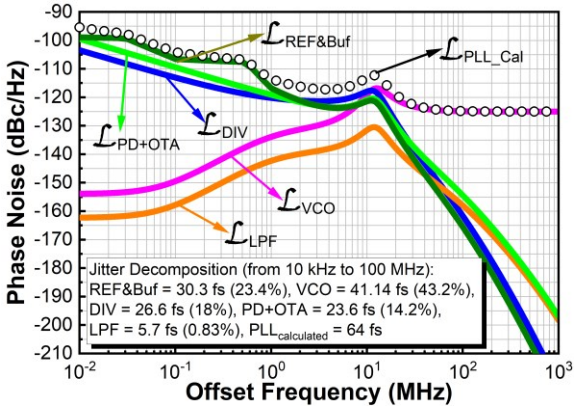

Fig. 11. MATLAB-simulated phase noise decomposition.

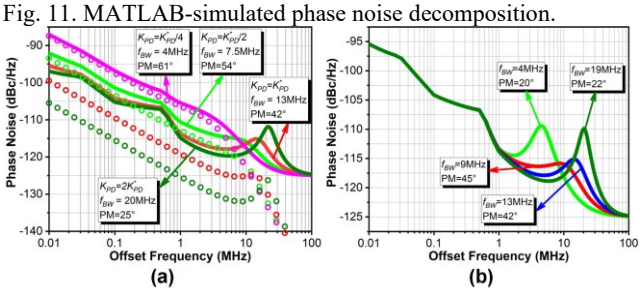

Fig. 12. Simulated PLL phase noise against (a) K_{PD} (inset dots: PD phase noise with the same color as its PLL noise), and (b) f_{BW}.

are driven by large signals. The transistor sizes of the mixer PD and XOR PD are two times of both QXOR PD topologies. A loading capacitor of 6 pF is added at the output of XOR, mixer, and the two QXOR PDs. Since level shifter and inverter buffers are necessary to boost the voltage and to fully drive the CP, PFD_LV, which denotes the PFD designed with core transistors, has to consume higher power than the other PDs. PFD_HV denotes the PFD/CP all designed with the I/O transistor.

Fig. 7(a) illustrates the output characteristic of PDs. As expected, the digital PFD and the analog PD exhibits a gain of $I_{cp}/2\pi$ near $\phi_e = 0$. The mixer PD presents a sinusoidal-like gain curve whose amplitude is proportional to its input voltage. Owing to the high near-DC gain of OTA, XOR and the QXOR PDs feature a near square-like gain curve against ϕ_e, indicating higher PD gains. The performance of PDs are summarized in Table I. The input-referred phase noise (IRPN) of PDs (dBc/Hz) is obtained from the output noise PSD (dBA/Hz) subtracted by the PD gain (in decibel). Shown in Fig. 7(b), the XOR PD exhibits ~9 dB smaller IRPN than analog PD, whereas the mixer and the two QXOR PDs are in between. The two QXOR PD topologies exhibit the same PD gain. In mixer PD, the

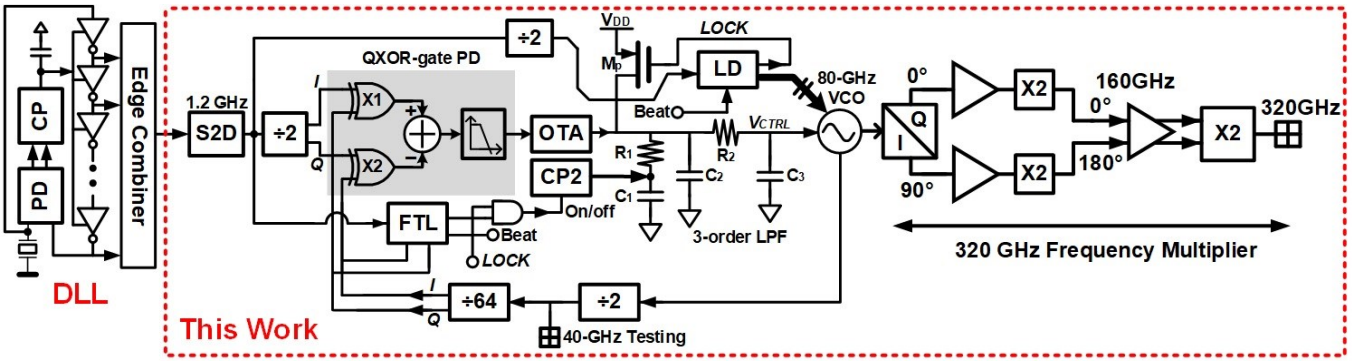

Fig. 13. Proposed 320 GHz signal source involving an 80 GHz integer-*N* PLL and a 320 GHz frequency quadrupler.

thermal noise of the gain stage (M1 and M2) dominates the high-frequency noise.

An ideal 2.4 GHz PLL synchronized by a constant f_{ref} = 600 MHz reference is built to investigate the PD in-band noise and reference feedthroughs transferring to the VCO output, where only the PDs and the V/I converters are using the transistor model. Other components, including VCO, divider, and LPF, are behavior models and therefore noiseless [30]. The respective LPF is tuned to ensure loop stability and a loop bandwidth of around 10 MHz. Fig. 8 summarizes the phase noise extracted from the closed-loop transient results in the steady state. The digital PFD generates spurs at f_{ref} and $2f_{ref}$, whereas the analog PD generates a higher spur level at f_{ref} and $2f_{ref}$. The mixer PD and XOR PD both introduce large spur at $2f_{ref}$, with a similar amplitude. By contrast, both QXOR PDs eliminate spur at f_{ref} and $2f_{ref}$. Fig. 9(a) shows the simulated spectrum at the 80 GHz PLL output using the proposed QXOR PD [Fig. 5(b)]. The spurs from f_{ref} to $3f_{ref}$ are buried in the noise floor, leaving only the $4f_{ref}$ term, indicating the spur cancellation decoupled from the loop bandwidth. Such a spur cancellation is inevitably degraded by process variation. As summarized in the histograms (collected from the PLL spectrum) in Fig. 9(b) and (c), the spur level at f_{ref} in the worst case is still at least 20 dB smaller than the PFD/CP adopting mismatch compensation [26] and analog PD. Similarly, the worst-case at $2f_{ref}$ is at least 38 dB lower than that of the single-path mixer [25] and XOR PD.

The phase noise of each loop is extracted from Fig. 8 by averaging the result. These fitting results are summarized in Fig. 10. All curves are summed by a factor of 24 dB to accommodate an additional division ratio of 16. As observed, the XOR PD and mixer PD both exhibit similar yet the smallest phase noise. The phase noises of QXOR PDs are in between, which are ~4 dB worse than the XOR or mixer PD. From the noise decomposition, doubling the width of each NMOS in the QXOR PD will reduce the phase noise by ~2 dB. Although conventional mixer and XOR PD have better noise performance, they show large spurs at $2f_{ref}$. In fact, the overall phase noise of QXOR PD + OTA becomes less important since their total intrinsic noise already falls below the reference noise level.

Since the QXOR PD using the proposed topology in Fig. 5(b) shows smaller phase noise with a similar spur level compared with the topology using Gilbert cell, it was chosen in this work. This topology also facilitates the layout for symmetry.

B. PLL Loop Simulation

The PLL open-loop gain is expressed by

$$H_{open} = \frac{K_{QXOR}}{R_L} \times \frac{R_L}{1+sR_LC_L} \times g_m(r_o \,||\, Z_{LF}) \times \frac{K_{VCO}}{N \times s} = \frac{K_{QXOR}}{1+s/\omega_{PD}} \times g_m(r_o \,||\, Z_{LF}) \times \frac{K_{VCO}}{N \times s} \quad (3)$$

Where K_{QXOR} is the gain (V/rad) of the QXOR PD, Z_{LF} is the transfer function of the loop filter. Adding C_L at the QXOR PD output degrades the phase margin (PM) since ω_{PD} is reduced, posing a limit to the spur reduction and the OTA's input transistor sizing. The open-loop gain transfer function presents five poles, respectively at the origin, 5.4×10^9, 7.4×10^8, 7.7×10^7, and 4.6×10^5 rad/s, whereas the zeros cancel out the other two poles at 5.5×10^9 and 6.8×10^8 rad/s at the same locations. The remaining zero is at 6.3×10^6 rad/s, between the two dominant poles. C_L is set to ~10 pF in this work to compromise spur, noise, and loop stability. This results in a loop bandwidth of ~12.9 MHz and the worst-case phase margin of 42º.

The MATLAB-simulated phase noise decomposition is plotted in Fig. 11, where the phase noises of input reference and VCO are obtained from the testing data (Section VI). The overall noise of QXOR PD + OTA is smaller than that of the input reference, and is thus no longer the main constraint to the PLL in-band noise. Phase noise against K_{PD} (K_{PD}^* denotes the PD gain chosen in this work) is summarized in Fig. 12(a). Reducing K_{PD} by decreasing the OTA output current can reduce the loop bandwidth, but doing so degrades the noise of the PD in-band noise according to (2), thereby increasing the PLL in-band noise level. When the reference noise is dominating the in-band noise, further increasing K_{PD} brings less noise improvement yet incurs peaking. Phase noise against f_{BW} tuned by the loop resistor is summarized in Fig, 12(b). Choosing a 9 MHz f_{BW} improves the phase margin to 50º, but the level of rejection to the VCO noise is reduced. Further decreasing the loop resistor incurs a peaking near the loop bandwidth since the remaining zero becomes larger and not sufficiently compensates for the first main pole.

The noise of the other loop components, such as the VCO, should be carefully examined and described in the next Section.

V. 320 GHz Signal Source and THz Circuits

A. 320 GHz Signal Source Architecture

Based on the topology illustrated in Fig. 1(d), the 320 GHz signal source is realized by cascading an 80 GHz PLL with a frequency quadrupler (×4) using an I/Q generator, as detailed in

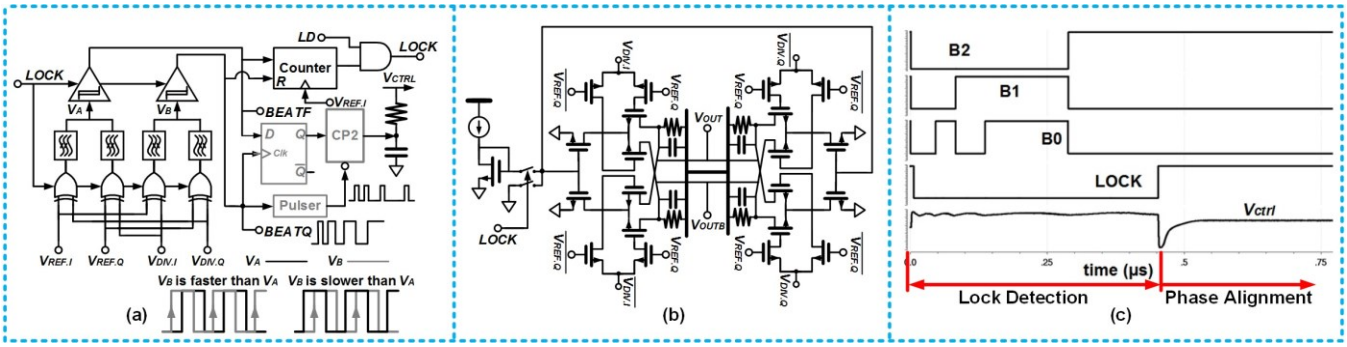

Fig. 14. (a) FD using two pairs of low-power QXOR gates, (b) low-power QXOR gate, and (c) PLL band-searching and locking process.

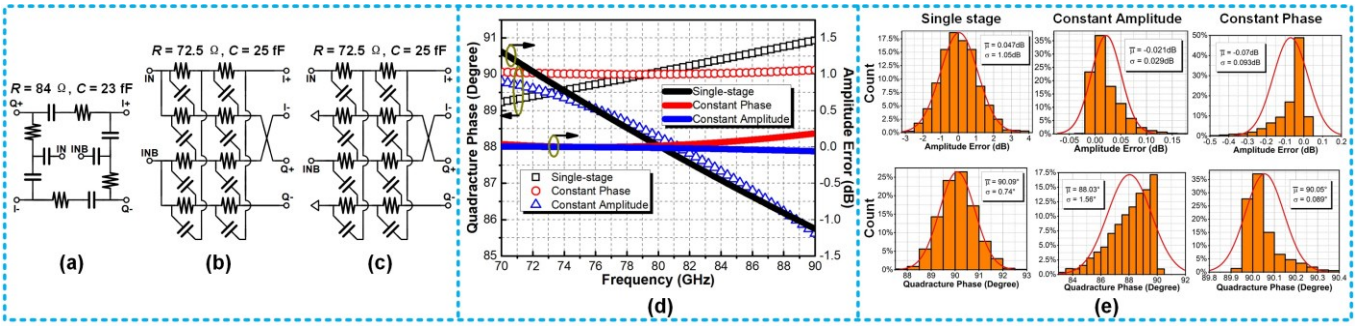

Fig. 15. (a) *RC* polyphase shifters: (a) single stage, (b) two stages and constant amplitude, and (c) two stage and constant phase; (d) simulated quadrature phase error and amplitude error for *RC* polyphase shifters, and (e) their Monte-Carlo statistics (sample $N = 2000$).

Fig. 13. The first frequency doubler generates an out-of-phase signal by doubling the frequency, which further drives a subsequent doubler for an overall frequency multiplication factor of 4. This approach mitigates the multi-stage lossy transformers in the multiplier chain and omits the need for injection locking. The design, therefore, becomes more flexible to overcome the process-voltage-temperature (PVT) variations, mismatches, and other nonidealities. The 600-MHz quadrature reference signal can be extracted from the other low-frequency PLL or a delay-locked loop in the future prototype.

B. Proposed FD and LD

The proposed dual-path PD has a limited capture range that is proportional to $K_{VCO} \cdot K_{PD}$, necessitating an FD. Conventional band-searching using dual comparators to measure V_{ctrl} consumes a long time since this searching process couples with loop components [31], motivating a new design. A practical approach to decouple the VCO band-searching from the loop components is realized by counting the $\Delta f = |f_{REF} - f_{DIV}|$. Fortunately, this function is enabled by the QXOR since all higher-order terms are canceled, leaving only Δf. In detail, the QXOR distills the frequency error in the form of $V_A = \sin(2\pi\Delta f t)$ in the main path, while a quadrature version of $V_B = \cos(2\pi\Delta f t)$ is generated by the auxiliary path. Whether the reference signal is leading or lagging can be examined by using V_B to continuously sample V_A, operating similarly to the bang-bang FD [22]. The proposed FD is shown in Fig. 14(a). Two digital Schmitt triggers convert V_A and V_B to digital format *BEATF* and *BEATQ*, respectively. CP2 is triggered by a pulser since Δf is small upon frequency locked. A low-power QXOR gate, which is used for frequency extraction, is depicted in Fig. 14(b).

The LD is made by using *BEATF* to continuously sample *BEATQ*, and the sampling result contributes to the decision of whether the band register switches to a higher band. In detail,

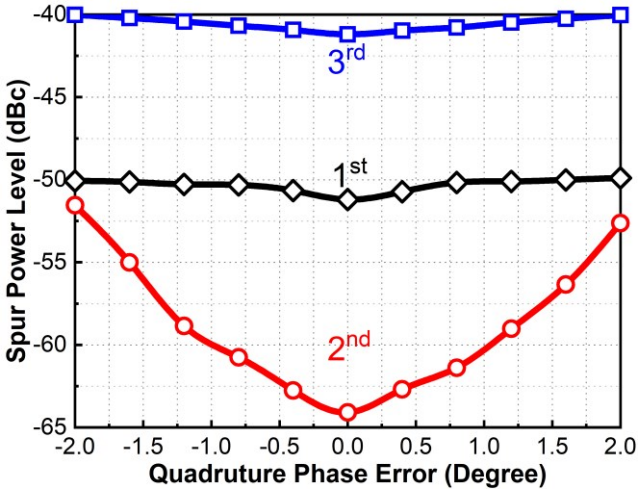

Fig. 16. Simulated subharmonic spur level (dBc) at 320 GHz (4th harmonic) against the quadrature phase error.

once the *BEATF* samples a "1"—which means the reference frequency is still high—the LD switches to a higher VCO band, and the VCO then operates in a higher frequency. This process continues until the *BEATF* samples a "0". Then, a "lock" signal *LD* is asserted. Thus, the time required for the VCO band searching is at least T_{LD}, which is quantized as below:

$$T_{LD} = T_{d1} + \sum_{i=1}^{k \le M} \left(\frac{1}{\left| f_{ref} - \frac{f_{VCO,i}}{N} \right|} + T_{d2} \right) + T_c \Bigg|_{\substack{f_{ref} - \frac{f_{VCO,k-1}}{N} > 0 \\ f_{ref} - \frac{f_{VCO,k}}{N} < 0}} \tag{4}$$

Where T_{d1} accounts for the VCO start-up time and signal propagation time in the divider chain. N is the PLL division

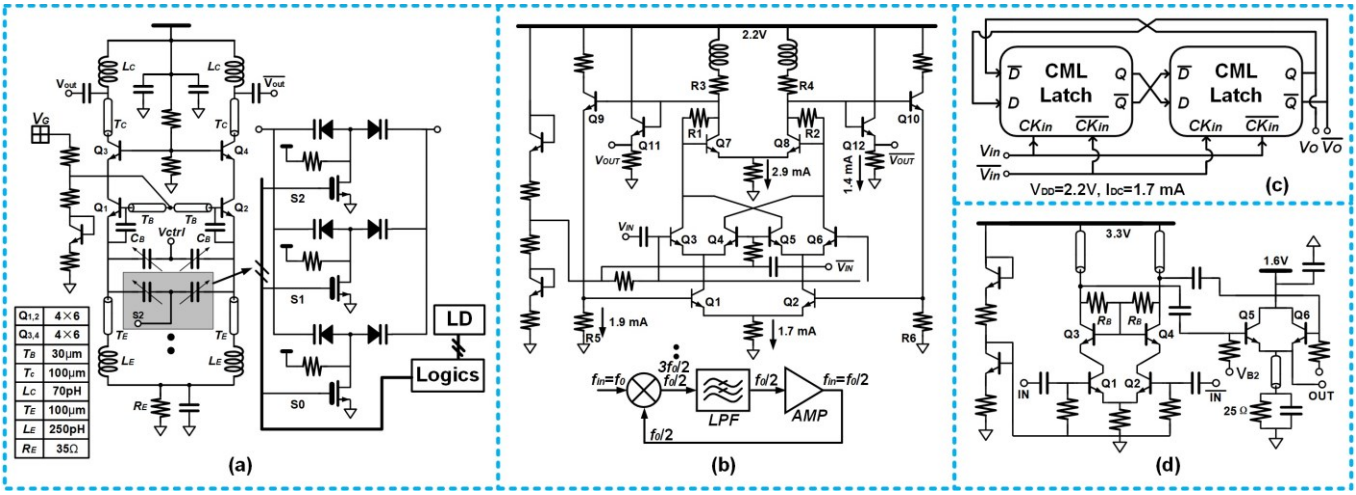

Fig. 17. (a) 80 GHz SiGe Colpitts VCO, (b) 80 GHz Miller divider, (c) static divider, and (d) 320 GHz frequency doubler and its pre-amplifier.

ratio. T_{d2} represents the delay of band-switching logic. T_c is the duration of time required for a counter to overflow. $k \in [1, M]$ implies the *BEATF* samples a "0" at the k^{th} band, and M is the number of VCO bands. T_{LD} accumulates till $\Delta f = f_{ref} - f_{VCO,k}/N < 0$. Clearly, T_{LD} is not dependent on loop components, but rather on Δf, k, and M. As a numerical example, the required time of band searching for Δf reduced from 50 to 2 MHz is ~ 540 ns and $k = 5$ in this case. The simulated transistor-level locking process is illustrated in Fig. 14(c), where it takes ~450 ns for lock detection and another ~100 ns for phase alignment.

C. 80 GHz I/Q Generation

An *RC* polyphase shifter is chosen for its compact size, wideband, and relaxed requirement on impedance matching.

Fig. 15(a)–(c) depicts three versions of *RC* polyphase shifters. The single-stage method can work with single or differential input, whereas the other two approaches, namely the two-stage constant amplitude and two-stage constant phase, require differential input [32]. Fig. 15(d) summarizes the performance: the third configuration maintains a phase difference of 90° for a wider bandwidth, with minor amplitude mismatch at high frequencies compared to the second method. In the third configuration, 72.5 Ω poly resistors with a size of 6 µm × 30 µm, and 25 fF MOM capacitors with a size of 4.3 µm × 4.3 µm, are used. Minor changes of these values are expected for each component according to the layout parasitic. Statistics results are summarized in Fig. 15(e). The third configuration exhibits better robustness in terms of maintaining the quadrature-phase, with < 0.4 dB amplitude error. Consequently, the two-stage constant-phase *RC* polyphase network is chosen.

The simulated power levels of the subharmonic spurs (including the fundamental, 2nd and the 3rd subharmonics) against the quadrature error are summarized in Fig. 16. With ±2º quadrature error, the spur power at the 1st and the 3rd harmonic exhibits around 1.3 dB and 1.2 dB variation, respectively, whereas the spur power at the 2nd harmonic is at least 10 dB smaller than that at the 3rd harmonics. The process variation of the poly-resistors is addressed by designing them with a large size. A layer called "pWellBlock" has been used to cover the entire resistor so as to remove the highly doped Pwell region beneath the poly-resistor, and thus reduces its parasitic capacitance and therefore, its resistance variation and loss at high frequencies. An individual testing of a poly-resistor, whose size is W = 15 µm and L = 30 µm (2.5X area of our design), shows a ~1% reduction on the resistance at 50 GHz. Yet, a standard poly-resistor (without the pWellBlock) shows a ~43% resistance variation.

D. 80 GHz VCO, Divider, and THz Circuits

The 80 GHz VCO is illustrated in Fig. 17(a), with crucial parameters listed in the table. The Colpitts oscillator is chosen for its low phase noise and wide tuning range. For low phase noise, it is essential to minimize the base inductance L_B, while sustaining the oscillation. L_B is chosen as ~20 pH using a 30 µm long, 3.4 µm thick top aluminum transmission line (TL), whose width is selected as 12 µm and providing a reasonably high quality-factor ($Q \approx 13$). The tank Q is thereby dominated by the accumulation-mode MOS varactor.

The 80 GHz Miller divider is shown in Fig. 17(b). The wideband and high gain of the transimpedance amplifier (TIA) allows the DC supply to be reduced from 3.3 to 2.2 V, and the minimum operating frequency of 135 GHz is found at 125˚C [14], which is feasible for frequency division at 80 GHz considering PVT. The 40 GHz and the subsequent frequency dividers are static dividers [Fig. 17(c)], with their DC powers scaled down across each stage.

The 320 GHz frequency doubler is depicted in Fig. 17(d). The NPN Q_1–Q_4 and the loading TL form a cascode topology of the pre-amplifier, and $Q_{5,6}$ establish the push-push doubler. Resistor R_B provides DC biasing for the cascode NPN $Q_{3,4}$ and stabilizes the pre-amplifier. The pre-amplifier is necessary for isolating the preceding stage while providing a large voltage swing to fully drive the doubler. The operation region of the doubler is strongly dependent on the bias voltage V_B. To obtain a strong 2nd harmonic power at 320 GHz, the V_B is assigned to ensure the doubler operates at the boundary between the ON and OFF states. The V_B is provided externally in this work. The TL at the emitter forms a resonance with parasitic capacitance from the HBT emitter and the pad. Load pull simulation is performed for maximizing the output power at 320 GHz.

VI. Measurement Results

The proposed 320 GHz PLL was fabricated in IHP 0.13 µm SiGe BiCMOS process with a featured HBT f_T/f_{max} = 300

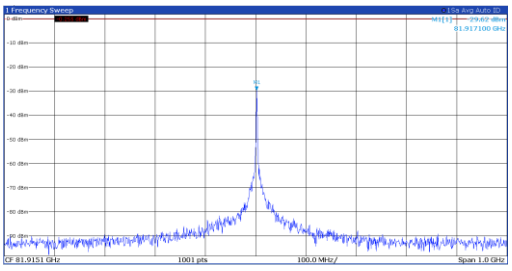

Fig. 18. Measured VCO spectrum at 81.9 GHz.

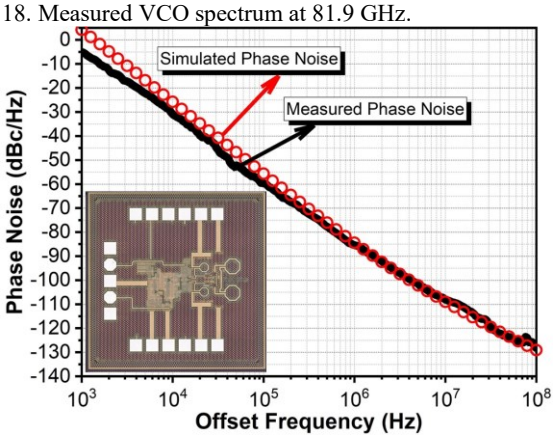

Fig. 19. VCO die photo and measure phase noise at 81.9 GHz.

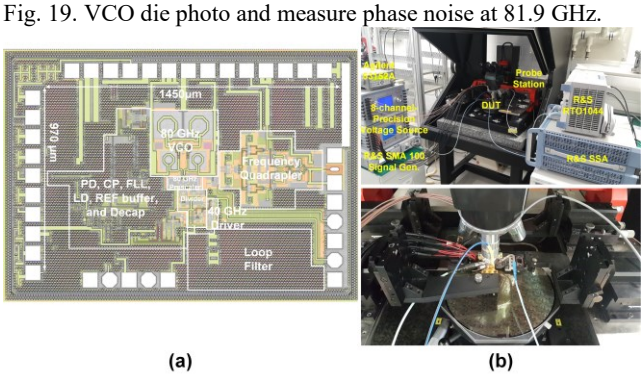

Fig. 20. (a) Die photo of the 320 GHz signal source, and (b) on-wafer measurement setup.

GHz/500 GHz [33]. The minimum channel length of the thin-oxide core MOS transistor was 130 nm, while it was 450 nm for the thick-oxide I/O MOS transistor.

A. VCO

The measured VCO spectrum is provided in Fig. 18, and the measured phase noise is provided in Fig. 19, together with the die photo. The VCO core occupies an area of 0.11 mm^2. When assigning V_G = 2.1 V, the measured phase noise at 81.9 GHz is −85 dBc/Hz at 1 MHz offset, and −108 dBc/Hz at 10 MHz offset. The measured phase noise at 1 MHz offset was ~5 dB worse than that of the simulation result. Noise decomposition reveals that such a discrepancy may come from the transistor layout stack, which contributes to the base resistance and has not been accurately captured by the *RC* extraction. The VCO drew 24.2 mA current from a 3.3 V power supply.

B. Reference Spur

The die photo of the proposed 320 GHz signal source is shown in Fig. 20(a). The design occupies an area of 1.4 mm^2. The on-wafer testing is shown in Fig. 20(b). The spectrum and phase noise were measured using the R&S spectrum analyzer

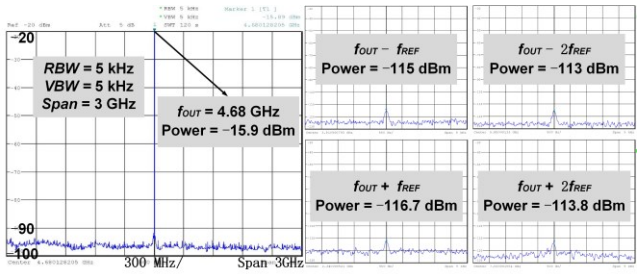

Fig. 21. Measure PLL spectrum and reference spurs at 4.68 GHz.

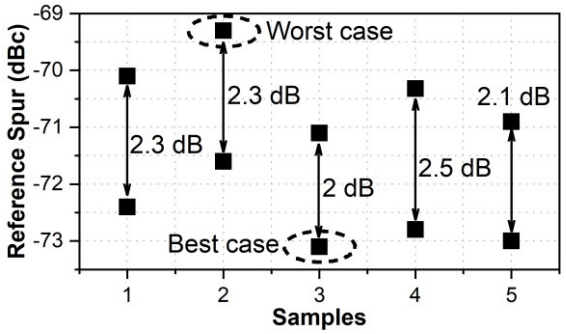

Fig. 22. Measured reference spurs across frequency and samples.

Fig. 23. Measured PLL phase noise at 40.96 GHz.

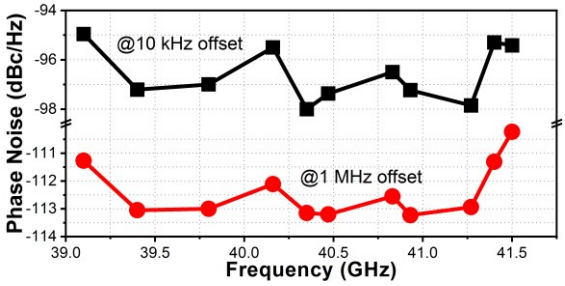

Fig. 24. Measured phase noise over the entire operation frequencies.

(R&S FSW 67), with an embedded frequency extender to 325 GHz. The reference signal was provided by R&S SMA 100.

Fig. 21 shows the measured spectrum at the 5-GHz divider output. The output power at 4.68 GHz is −15.9 dBm, and the power of spurs up to $2f_{REF}$ are summarized in Fig. 21 as well. The highest power of spurs appears at $f_{OUT} - 2f_{REF}$, which is −113 dBm. Thus, the maximum reference spur is −97.1 dBc, which is normalized to 80 GHz by adding 20log(16) = 24 dB, translating to −73.1 dBc at the fundamental frequency. The reference spurs at $\pm 4f_{REF}$ were below –80 dBc. The spurs at f_{REF} and $2f_{REF}$ may possibly come from circuit mismatches, the crosstalk among wires, substrate coupling, and the leakage

TABLE II

W-BAND INTEGER-*N* SILICON PLL PERFORMANCE SUMMARY AND COMPARISON

	ISSCC'09 [16]	*JSSC*'11 [15]	*TMTT*'12 [25]	*TMTT*'12 [19]	*RFIC*'13 [34]	*TMTT*'14 [17]	*TMTT*'19 [31]	*JSSC*'20 [18]	**This work**
Technology	65 nm CMOS	130 nm SiGe	0.8 µm SiGe	180 nm SiGe	130 nm SiGe	130 nm SiGe	65 nm CMOS	65 nm CMOS	**130 nm SiGe**
f_{ref} (GHz)	0.375	3	1.5	0.125	0.333	3	0.1	0.1	**0.6**
f_{out} (GHz)	96	80–100	64–84	92.8–98.1	73.9–83.5	92.7–100.2	93.4–104.8	61.2–100.8	**78.4–83**
PN @100 kHz	/	−93	−102	−85	−88.5	−92.5	/	−81.85	**−97.4***
PN@1MHz	−75.2	−100	−106	−92	−91	−102.0	−85.8	−93	**−107.7***
$\mathcal{L}_{norm}$ (dBc/Hz^2)	–209 @1 MHz	–225 @ 1 MHz	–234 @1 MHz	–231 @1 MHz	–224 @1 MHz	–227 @1 MHz	–226 @1 MHz	–235 @1 MHz	**–238 @1 MHz**
Spur (dBc)	−52.7	/	−37	−52	−67	−60	−43.8	−35.7/−48.7	**−73.1**
f_{BW} (MHz)	2	0.5–1.9	47	1	1	20	3	1	**12.9**
Integrated jitter (fs_{rms})	2220	166 [1 MHz−1 GHz]	161 [10 kHz−100 MHz]	167 [10 kHz −10 MHz]	120 [10 kHz −100 MHz]	78.5 [10 kHz−100 MHz]	607.3 [10 kHz −300 MHz]	124 [10 kHz −100 MHz]	**66.9 [10 kHz−100 MHz]**
Power(mW)	43.7	1150	517	140	510	469.3	57	23.6	**147.2**#
Area (mm^2)	0.7	1.87	1.1	1.8	2.46	0.93	0.87	0.58	**1.1**
FoM (dB)	−217	−225	−229	−234	−231	−235	−227	−244.4	**−242**#
$FoM_{JIT,N}$(dB)	−241	−240	−247	−263	−255	−250	−257	−273	**−263**#

*: 6 dB is added to the result in Fig. 22.

#: excluding the power consumption of mm-wave output test buffers at 40 GHz and 80 GHz.

current through the varactors. Fig. 22 summarized the reference spurs measured for the entire operating frequency over 5 samples. The worst case is –69.3 dBc, with ~2.3 dB variation for the entire operating range.

C. Phase Noise and PLL Performance Comparison

By turning off the frequency quadrupler, the minimum phase noise was found at 40.96 GHz, measured at the prescaler's output as shown in Fig. 23. The minimum PN was –97.2 dBc/Hz at 1 kHz offset and –113.7 dBc/Hz at 1 MHz offset. The resulting integrated $jitter_{rms}$ (from 10 kHz to 100 MHz) was 66.9 fs_{rms}. Fig. 24 summarizes the phase noise over the entire frequency range. PN smaller than –110 dBc/Hz at 1 MHz offset was achieved for the whole operation frequencies.

The standard metrics for PLL performance quality are $\mathcal{L}_{norm}$ [35], FoM [15], and $FoM_{JIT,N}$ [36], as described below

$$L_{norm} = L_{in-band} - 20\log(N) - 10\log(f_{REF}) \tag{5}$$

$$\mathrm{FoM} = 10\log\left[\left(\frac{\mathrm{RMS\_Jitter}}{1\,s}\right)^2\left(\frac{\mathrm{Power}}{1\,\mathrm{mW}}\right)\right] \tag{6}$$

$$\mathrm{FoM_{JIT,N}} = 10\log\left[\left(\frac{\mathrm{RMS\_Jitter}}{1\,s}\right)^2\left(\frac{\mathrm{Power}}{1\,\mathrm{mW}}\right)\Big/\left(\frac{f_{out}}{f_{REF}}\right)\right] \tag{7}$$

Table II summarizes silicon-based PLLs operating in *W*-band. The proposed PLL achieves the lowest phase noise at 1 MHz offset, and the lowest integrated $jitter_{rms}$, smallest $\mathcal{L}_{norm}$, with competitive FoM and $FoM_{JIT,N}$ among state-of-the-art. The measured reference spur is at least 6 dB smaller than the other works in Table II, albeit a wide f_{BW} of 12.9 MHz is adopted.

Fig. 25 at the next page shows the THz source spectrum and phase noise measured at the frequency quadrupler's output. The THz source can lock from 306. 9 to 321 GHz. The measured phase noise performance of the device-under-test (DUT) was compared with a reference phase noise measurement performed using a low phase noise signal generator (instead of the DUT). The reference measurement shows a much lower phase noise, and thus it can be concluded that the noise contribution of the measurement equipment is negligible compared to the noise contribution of the DUT. The minimum phase noise of the DUT was found at 311.8 GHz, with –62.9 dBc/Hz noise at 10 kHz offset, and –90.3 dBc/Hz at 1 MHz offset. The resulting integrated jitter was 122 fs_{rms} (10 kHz to 100 MHz). The input base resistors of the frequency quadrupler couple with the VCO core and hence reduces its oscillation frequencies. Such a coupling also adds noise to the VCO tank and degrades the VCO phase noise. This suggests that a chain of buffers between the VCO and frequency quadrupler may be necessary for future prototypes, though it comes at the cost of higher power consumption and area.

D. Settling Behavior

Fig. 26 shows the measured PLL settling behavior upon the switching of the reference frequency in the same VCO band (with FD and LD turned off). With FD and LD turned on, Fig. 27 demonstrates the operation of VCO band-searching. A "reset" signal was provided as a triggering signal, such that the LD started the band-searching from the lowest frequency band, and then switched the VCO band upward gradually toward the desired frequency. As shown, the PLL's overall convergence time was at the microsecond level.

E. THz Source Power Measurement

An Erickson PM5 power meter was used for power measurement, and the full setup is depicted in Fig. 28. Fig. 29 summarizes the measured output power P_{sat} over all the operating frequencies. The optimal biasing voltage $V_{B2.opt}$ (biased through current mirrors with emitter degeneration) for the push-push frequency doubler was ~1.15 V, and the doubler drew 10.3 mA from a 1.6 V power supply. Choosing such a $V_{B2.opt}$ made the base-emitter voltage $V_{BE} \approx 874$ mV to be close

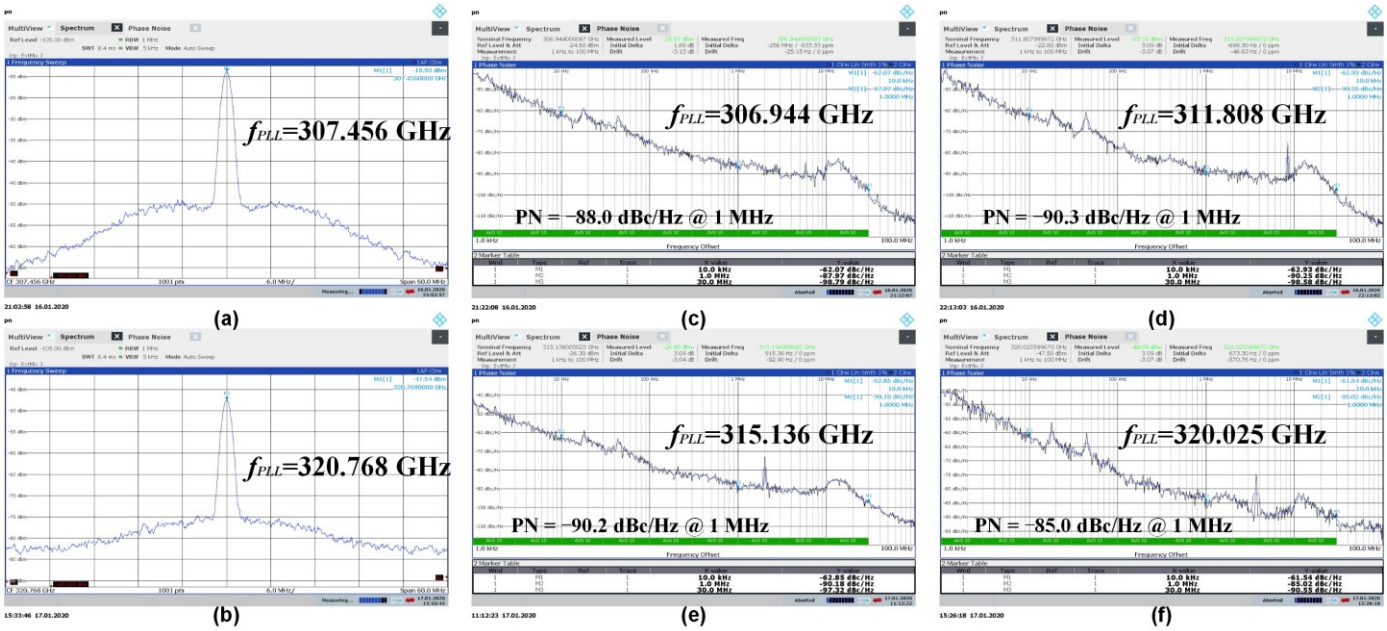

Fig. 25. Measure 320 GHz SiGe BiCMOS signal source spectrum at (a) 307.456 GHz, and (b) 320.768 GHz; Measured phase noise at (c) 306.944 GHz, (d) 311.808 GHz, (e) 315.136 GHz, and (f) 320.025 GHz.

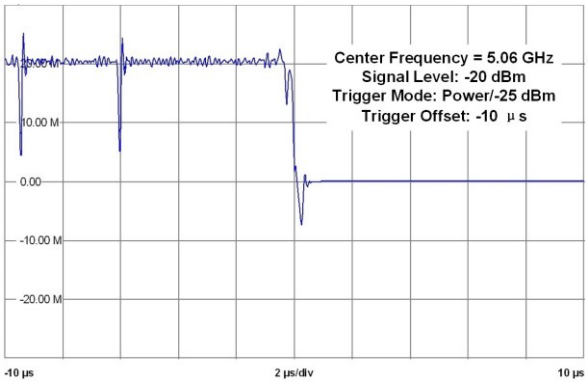

Fig. 26. Measure PLL settling behavior by switching frequency.

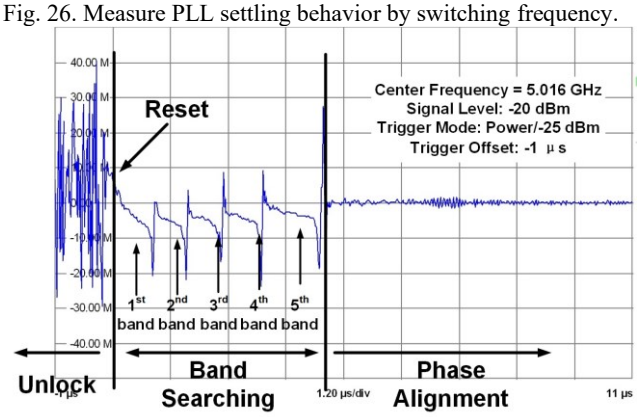

Fig. 27. Measure PLL settling behavior with lock detection.

to the turn-on point of the transistor. The maximum output power is shown in Fig. 29, which was 116.37 µW (–9.34 dBm) before calibration. The value for the loss of the I-325 GSG probe was delivered by the vendor, and the insertion loss of the waveguide component has been verified by S-parameter measurements in the past. After calibration, the highest output power was –3.3 dBm, which was 5 dB smaller than the simulation result with the same bias voltages. The reasons for such a discrepancy include 1) tank quality-factor degradation

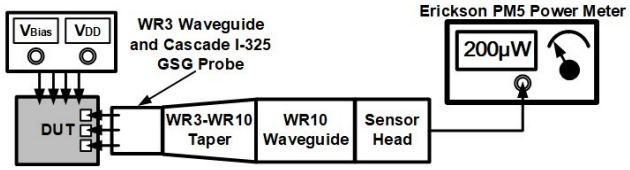

Fig. 28. 320 GHz power measurement setup.

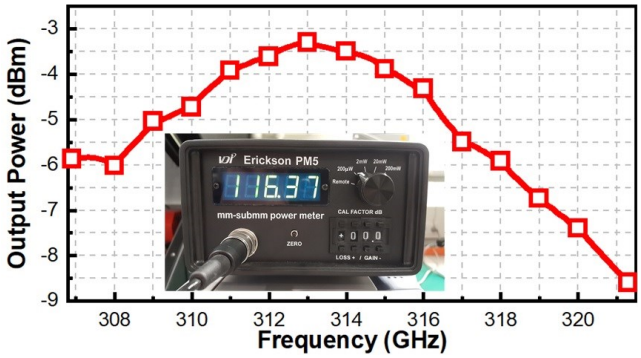

Fig. 29. Measured output power of the frequency quadrupler after calibration over the entire operating frequency. Inset: the largest achievable output power before the power calibration.

and hence output voltage-swing drop of the VCO, 2) underestimate of the resistance of vias connecting the TLs to the power plane, and 3) EM extraction error. Fig. 30 summarizes the measured subharmonic spurious tone rejection (dBc). The fundamental tone was measured by the Agilent N5260-60003 (67–110 GHz Wave Guide T/R Module), and the second harmonic was measured by PNA-X Keysight N5247A with the VDI VNAX extender module. The testing setup of the third harmonic was identical to that of the desired output signal (4^{th} harmonic). The spurious tone rejection was better than 35 dB, which is ~13 dB higher than that in [37] for the operating frequency higher than 300 GHz.

The signal source consumed a DC power of 372 mW from 1.2/2.2/3.3-V power supplies.

TABLE III

THz Signal Source Performance Summary and Comparison

	ISSCC'14 [9]	*ISSCC*'15 [38]	*ISSCC*'16 [10]	*VLSIC*'16 [11]	*Proc. IEEE*'17 [7]	*TTHz*'18 [8]	*ISSCC*'18 [12]	**This work**
Technology	90 nm SiGe	130 nm SiGe	65 nm CMOS	65 nm CMOS	130 nm InP	65 nm CMOS	130 nm SiGe	**130 nm SiGe**
f_{ref} (GHz)	0.273~0.296	0.31	0.1~0.11	0.125	30	0.0057	N/A	**0.6**
f_{out} (GHz)	280~303 (7.9%)	317.44	539~560 (3.8 %)	208~255 (20.3%)	300.7~301.1 (0.14%)	282.3~283.7 (0.49%)	302~332 (9.5%)	**306.9~321.3 (4.44%)**
Multi. ratio N	1024	1024	5390	1664~2040	10	16384	N/A	**512**
PN@100 kHz	−77.8	N/A	−71	N/A	−78	−53.5	−77.5	**−78**
PN@1 MHz	−82.5	−79	−74	−80	−85	−53.5$^{\Delta}$	−78.5	**−90.3**
Normalized PN $\mathcal{L}_{norm}$ (dBc/Hz^2)	–227 @1 MHz	–224 @1 MHz	–229 @1 MHz	–227 @1 MHz	–210 @1 MHz	–205 @1 MHz	N/A	**–232 @1 MHz**
Integrated jitter (fs_{rms}) [Integ. range]	737$^{\Delta}$ [10 kHz –100 MHz]	N/A	286$^{\Delta}$ [30 kHz –30 MHz]	N/A	171$^{\Delta}$ [10 kHz –10 MHz]	2430$^{\Delta}$ [10 kHz –100 MHz]	192$^{\Delta}$ [10 kHz –100 MHz]	**122$^{\Delta}$ [10 kHz –100 MHz]**
DC Power (mW)	376	610	172	1400	301.6	114	51.7	**372**
Probed P_{sat}(mW)	−14	−6.8	−27$^{\#}$	−11	−23	−22.5	−13.9	**−3.3**
Peak DC-to-RF Effi. η (%)	0.01	0.54	0.001	0.006	0.002	0.005	0.079	**0.12**
Area (mm^2)	2.56	2.08	2.79	5.6	0.84	0.48	0.85	**1.4**
FoM (dB)	−217	N/A	−229	N/A	−231	−212	−237	**−233**
$FoM_{JIT,N}$ (dB)	−247	N/A	−266	N/A	−241	−254	N/A	**−260**
FoM_P (dB)	−223	N/A	−221	N/A	−228	−233	−245	**−249**

Δ: Estimated from figure

#: Radiated power

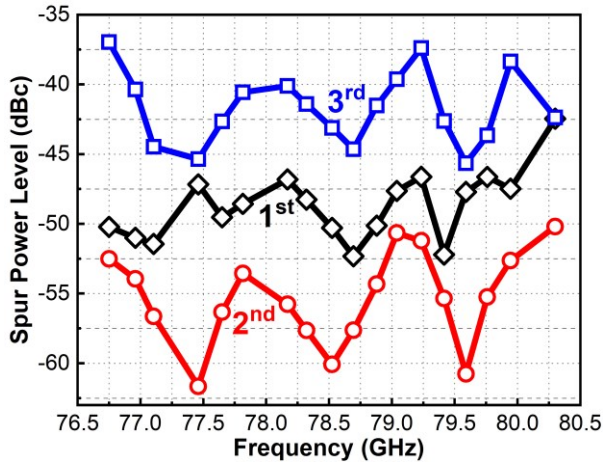

Fig. 30. Measured power levels of subharmonic spurious tones.

F. THz Source Performance Comparison

State-of-the-art signal sources operating at the THz range are summarized in Table III. Power consumptions of the test buffer at 40 GHz and 80 GHz have been excluded. The proposed 320 GHz signal achieves 1) the lowest PN at 1 MHz offset, 2) the smallest $\mathcal{L}_{norm}$, 3) highest probed output power P_{sat}, and 4) the lowest integrated $jitter_{rms}$, thanks mainly to the benefit of using a higher reference frequency with the proposed QXOR PD. Both the FoM of –233 dB and the $FoM_{JIT,N}$ of –260 dB compare favorably with the state-of-the-art. Given that a significant portion of the DC power is spent to boost the output power at the THz range, it is also meaningful to incorporate the P_{sat} into FoM, which is FoM_P as expressed as follows [23]:

$$\mathrm{FoM_p} = \mathrm{FoM} - 10\log\left(\frac{\mathrm{P_{sat}}}{1\ \mathrm{mW}}\right) \tag{8}$$

The proposed 320 GHz signal source attains the smallest FoM_P of –249 dB among state-of-the-art. Future work should reduce the phase noise of the VCO.

VII. Conclusion

A 320 GHz fully integrated SiGe signal source incorporating an 80 GHz PLL and a 320 GHz frequency quadrupler is reported. The 80 GHz PLL involves a novel dual-path phase detector based on the proposed QXOR technique. The QXOR PD is analyzed and compared with the traditional PDs, showing the ability to cancel out the reference spurs, with competitive speed and noise performance. The frequency tracking and lock detection both benefit from the QXOR technique as well. The lock detection time is decoupled from the loop components. Fabricated in a 130 nm SiGe BiCMOS technology, the proposed THz signal source demonstrates low spurious tones, low noise, small integrated jitter, and high output power among state-of-the-art. Therefore, the proposed signal source has the potential to be employed for recent emerging low-cost applications in the THz region.

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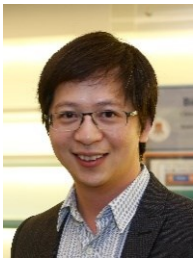

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