

A Time-Multiplexed Switched-Capacitor CDS Equalizer With Reduced Crosstalk Layout

K. A. Ng and P. K. Chan

Abstract—A new time-multiplexed switched-capacitor (TM-SC) equalizer is designed on the basis of the previously reported correlated double-sampling integrator and the crosstalk reduction layout approach, which aims at improving the performance aspects on crosstalk, gain loss, $1/f$ noise and offset. The equalizer, which operates at a single 3-V supply and has a filter bank with 4 TM channels, has been fabricated to confirm the effectiveness of the structure using a standard 0.8- μm CMOS process.

Index Terms—Crosstalk, equalizers, integrated circuit, layout, switched-capacitor (SC) circuit, time-multiplexed (TM) circuit.

I. INTRODUCTION

DESIGNING an independent analog integrated circuit in a multi-channel system has the advantage of low crosstalk and it is easy to integrate due to the process of duplication in the channel electronic circuit. However, it is most often at the cost of increased silicon area and power consumption. Time-multiplexed (TM) tasks are suitable for switched-capacitor (SC) circuits. Multiplexed SC filters or equalizers are popular application examples. Although TM-SC techniques [1], [4], [9] or architectures [1]–[9] have been reported successfully in relaxing certain shortcomings from the independent channel design approach, there still exist many challenging problems such as crosstalk interference signal, gain loss, dc offset, and coupling noise that limit the circuit performance. Among these imperfect factors, the inter-channel crosstalk most often outweighs the achievable signal-to-noise (S/N) ratio and causes the accuracy issue in terms of gain loss in the TM integrated systems. For example, a 60-dB S/N ratio circuit will be swamped by a -30 -dB crosstalk signal. For the noise issue, the $1/f$ noise appears as one of the dominant fundamental noise sources, which deteriorates the dynamic range of CMOS circuits, but it is possible to reduce the noise by a proper circuit design technique. Thus, crosstalk reduction becomes one of the most difficult problems when dealing with a large number of time-sharing channels being integrated in the silicon environment while concerning the area utilization tradeoff. In addition, dependent upon the applications, the potential large dc offset or mismatched dc components among different channels may

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K. A. Ng was with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798. He is now with Chartered Semiconductor Manufacturing, Singapore 738406 (e-mail: ngkianann@charteredsemi.com).

P. K. Chan is with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798 (e-mail: epkchan@ntu.edu.sg).

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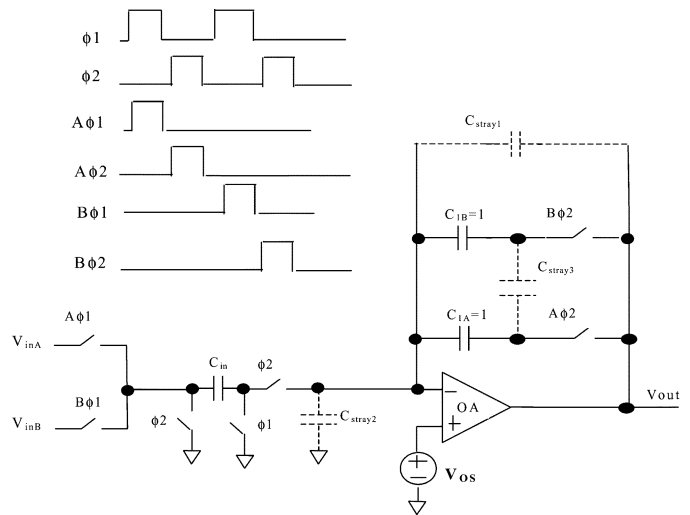


Fig. 1. Classical TM-SC integrator.

cause a harmful effect in the multi-channel system. Therefore, the objective of this paper is to study the key limitations and to present the design of a correlated double-sampling (CDS)-SC equalizer using the previously reported CDS-TM-SC integrator [9] that addresses the issues from circuit design perspective and layout perspective in order to reduce three types of crosstalk effects as well as both circuit dc offset and $1/f$ noise simultaneously. The experimental results are given to validate the proposed method.

Section II, is concerned with the review of the conventional TM integrators. The nonideal effects that greatly limit the integrator performance are described. A CDS-TM-SC integrator, taking into account all major crosstalk issues, is proposed for improving the current TM-SC circuits. In Section III, the operation principle of the equalizer architecture is explained together with the specifications. The layout plan that allows further reduction of crosstalk from system considerations is also presented. In Section IV, the application of the CDS-TM-SC integrator to implement a new CDS-TM-SC equalizer is discussed. In Section V, the experimental results together with the implications are discussed. This is then followed by the concluding remarks in Section VI.

II. TM INTEGRATORS

A TM integrator is the fundamental building block in TM filter design. Fig. 1 shows the classical two-channel TM-SC integrator. There is one SC input resistor and two storage capacitors responsible for individual channel memory in the feedback path of the op-amp. The integrator is run with the biphasic clock

together with two channel control clock signals. Turning on the channel selection switch would activate the channel. There are three relevant sources of parasitic capacitances in this circuit. C_{stray1} is the stray capacitance between the output of the integrator and the op-amp inverting terminal [1]. C_{stray2} is the stray capacitance between the op-amp inverting terminal and ground [2]. C_{stray3} is the coupling capacitance between the integrating capacitors. These undesirable capacitances are the principal contributors of inter-channel crosstalk in TM-SC filters or circuits.

Regarding C_{stray1} , it would couple a small-signal charge of an active channel to the next channel via charge sharing in the integrating capacitor, C_I , of the next active channel, thus contributing parasitic crosstalk of $(C_{\text{stray1}})/(C_{\text{stray1}} + C_I)$. The C_{stray1} depends upon the layout routing of integrating capacitors and the associated switches.

Regarding C_{stray2} , it represents the total lumped parasitic capacitors associated at the inverting terminal of the op-amp. It comprises the total top-plate capacitance of all the integrating capacitors, the parasitic input capacitance of the op-amp and the capacitance of the associated input switch. For the op-amp with finite gain A , the gain-limited crosstalk is of the amount $(C_{\text{stray2}})/(AC_I)$. Although this crosstalk is negligible for op-amp having gain more than 60 dB [2], C_{stray2} has the possibility of introducing extra noise and offset gain if the lumped top plate capacitance becomes significant in a case of a large number of multiplexing channels. This places constraints on the low-power op-amp because the closed-loop bandwidth (BW) as well as the settling time is therefore reduced. These drawbacks can be overcome by adding extra channel switches [1] for isolation of integrating capacitor to the virtual ground of the op-amp but this leads to additional charge injection in a form of dc offset at the output of the integrator. In addition, the structure is subject to significant output dc offset if C_{stray2} is not properly controlled or high input dc offset, V_{os} , in the CMOS op-amp.

Regarding C_{stray3} , it is formed via the electrical fringing field between two adjacent integrating capacitors. Therefore, it provides undesirable coupling mechanism between two channels. Assuming each integrator capacitor is C_I , the amount of coupling crosstalk to the next channel is $(C_{\text{stray3}}/C_I)/(C_I + C_{\text{stray3}}/C_I)$. In another case, if adjacent channel is in idle state, the sampling noise from the idle channel could be coupled to the active channel via C_{stray3} . This cannot be easily solved through the circuit design technique.

Fig. 2 shows the exemplary first-order low-pass filter with inclusion of two key crosstalk capacitances, C_{stray1} and C_{stray3} . Assuming ideal op-amp, ideal switches and grounded Channel B input, when the input signal is only applied in Channel A, the simulated crosstalk output in Channel B is illustrated in Fig. 3. It can be seen that the crosstalk effect is a function of frequency. For different values of stray capacitances, different crosstalk frequency responses are observed. It is also apparent that in signal frequency band, the crosstalk from C_{stray3} has contributed at least few dB with reference to the standalone crosstalk from C_{stray1} in this first-order filter implementation. Thus, for higher-order filter design, the crosstalk effect is much pronounced. This investigation of alternative structure or tech-

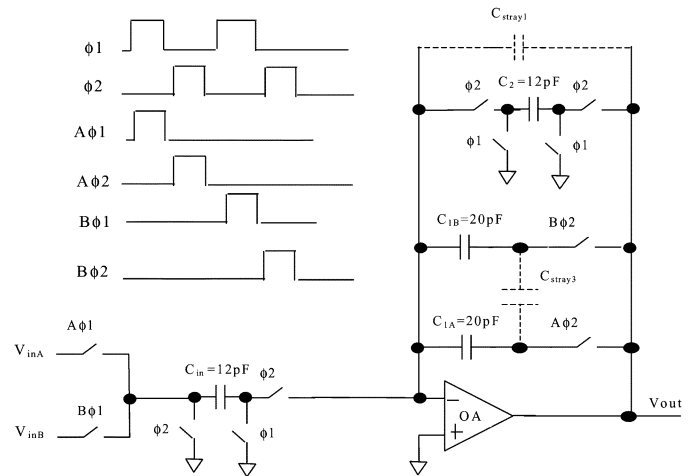


Fig. 2. Example of two-channel TM-SC first-order low-pass filter for crosstalk simulation.

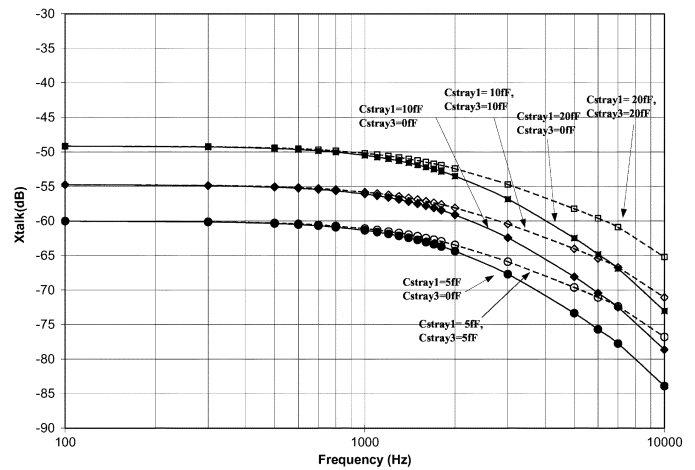


Fig. 3. Crosstalk performance for the two-channel TM-SC first-order low-pass filter.

nique for suppression of the two critical crosstalk parasitic capacitances is needed.

Fig. 4 shows the evolutionary structure of Fig. 1. The effect of C_{stray1} can be reduced by turning on a clamp switch [1], [4], [9] during the inactive channel periods (ϕ_1). This effectively prevents it from sharing any channel charges to the next active channel integrating capacitor. Alternatively, the use of neutralization capacitors to compensate C_{stray1} is possible but restricting to differential topology [3]. It is difficult to obtain the exact neutralization value from estimation. Hence, the clamping switch method is preferred because it supports either single-ended or fully differential TM-SC structures. In general, using the channel reset switch, it can be observed that the typical coupling crosstalk, from adjacent channels to far apart passbands channels, ranges from -27 dB to -50 dB [1], [4], [9] based on the measured results of different circuit architectures. To further improve the crosstalk range, the remaining crosstalk problem arising from C_{stray3} needs to be resolved. It is mainly because C_{stray3} contributes significant coupling effect in terms of adjacent channel crosstalk as well as far apart passbands channel crosstalk through layout structures.

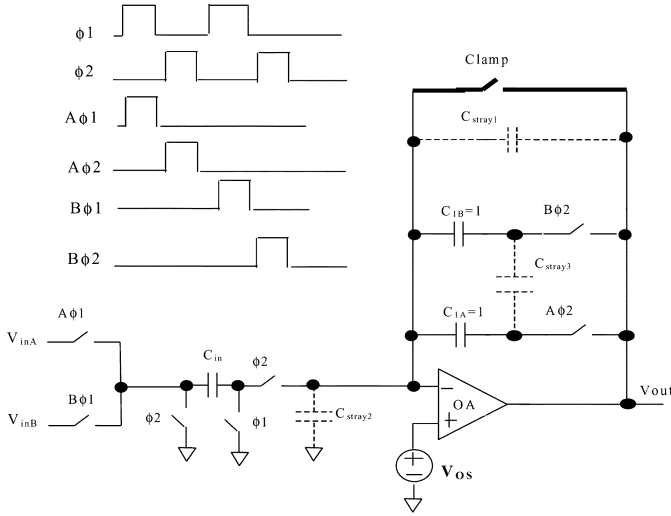


Fig. 4. TM SC integrator with a channel reset switch.

Another problem is that the output dc offset in TM-SC circuits mainly comes from op-amp offset and MOS switch charge injection along critical signal paths. For higher-order filter implementation, a cascade configuration will further worsen the dc offset performance. Although it is well known that if each channel implements the same signal path, the output offset of each channel will track with each other, it does not guarantee that each channel would exhibit low offset since the amplifier dc offset in conjunction with charge injection effect would cause variation in offset values at different parasitic gain functions. Another well-known method to reduce the op-amp offset and the switch charge injection is based on fully differential SC implementation incorporating high pass function [8]. Alternatively, further effective method to reduce the offsets is through CDS technique [4], [9] combined with minimum switch size whenever meeting the worst case speed in specification. As a matter of fact, not only does the CDS structure benefit the reduction of the $1/f$ noise, it is also a natural extension for the TM-SC circuits with reset feature. It is therefore the first objective of this paper is to utilize the CDS structure as a means to relax the shortcomings as described.

Fig. 5 shows the fundamental integrator [9] together with associated clock waveforms. It is based on adding CDS feature to form CDS-SC integrator. Using usual nodal analysis, the discrete equations are established as follows:

$$C_1 [V_{\text{out}}^e(n)T - V_{\text{out}}^e(n-1)T + V_{\text{OS}}(n-1)T - V_{\text{OS}}(n)T] = C_{\text{in}} \left[V_{\text{in}}^o \left(\frac{n-1}{2} \right) T + V_{\text{OS}}(n)T - V_{\text{OS}} \left(\frac{n-1}{2} \right) T \right] \quad (1)$$

$$[V_{\text{out}}^e(n)T - V_{\text{out}}^e(n-1)T + V_{\text{OS}}(n-1)T - V_{\text{OS}}(n)T] = \frac{C_{\text{in}}}{C_1} \left[V_{\text{in}}^o \left(\frac{n-1}{2} \right) T + V_{\text{OS}}(n)T - V_{\text{OS}} \left(\frac{n-1}{2} \right) T \right]. \quad (2)$$

If $V_{\text{OS}}(n-1)T$ is approximately equal to $V_{\text{OS}}(n)T$ and $V_{\text{OS}}(n)T$ is approximately equal to $V_{\text{OS}}(n-1/2)T$, the offset

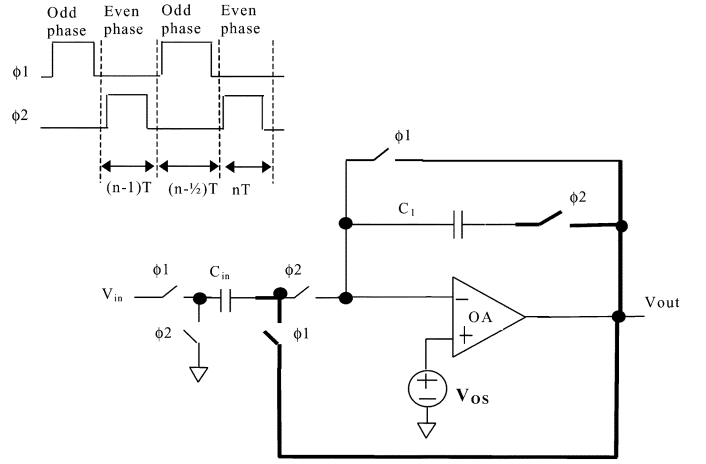
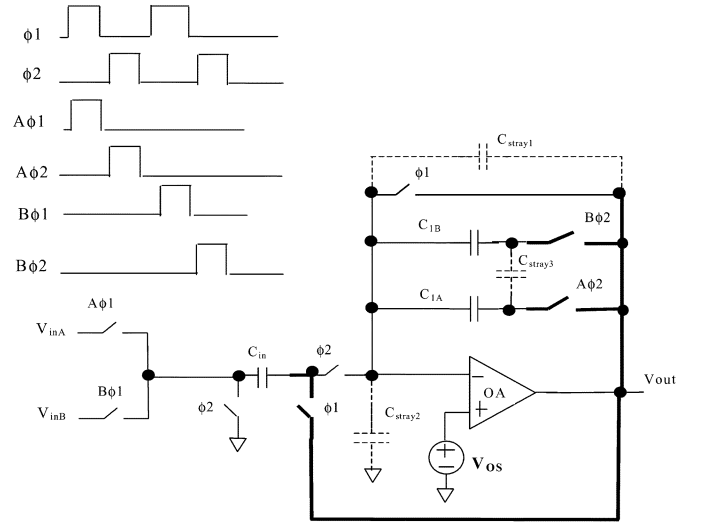


Fig. 5. Previously reported CDS-SC integrator with a channel reset switch [9].


 Fig. 6. Proposed CDS-TM-SC integrator with minimized C_{stray3} via layout technique.

terms within (2) are cancelled and hence, the z -domain transfer function is obtained as

$$\frac{V_{\text{out}}^e(z)}{V_{\text{in}}^o(z)} = \frac{C_{\text{in}}}{C_1} \left[\frac{z^{-\frac{1}{2}}}{1 - z^{-1}} \right]. \quad (3)$$

This is regarded as a lossy discrete integrator (LDI) noninverting integrator with offset cancellation. Extension of this offset-free integrator to the multiplex integrator [9] is illustrated in Fig. 6. The associated controlled clock signals are depicted in Fig. 7. This alternative structure utilizes: 1) the CDS technique [10] to minimize parasitic crosstalk arising from C_{stray1} and circuit dc offset arising from amplifier offset V_{OS} in TM integrator; 2) the high gain op-amp to minimize the gain-limited crosstalk through suppressing C_{stray2} and 3) the crosstalk reduction layout (Section III) to minimize C_{stray3} , which is identified as the main contributor of the coupling crosstalk that has not been reported from the prior research works [1]–[9]. Of particular importance, the crosstalk mechanism, in general, is identified as the main error source [8]. Therefore, the second objective of this paper is to devise a layout methodology, which aims at improving the crosstalk range in the design of TM-SC circuits and systems.

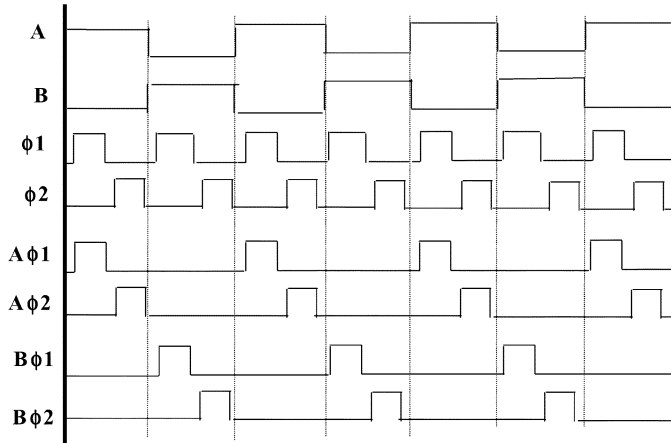


Fig. 7. Controlled clocks for two-Channel CDS-TM-SC integrator.

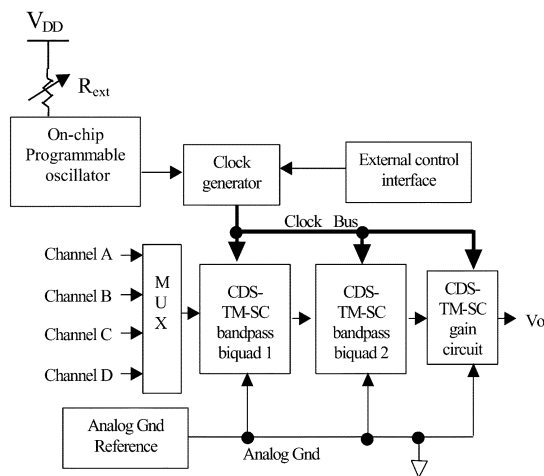


Fig. 8. System architecture of the CDS-TM-SC equalizer.

III. TM EQUALIZER

A. System Considerations

The equalizer comprises a 4-channel multiplexer, two identical TM-SC bandpass biquads being arranged in cascade architecture, a TM-SC gain circuit, an oscillator, a clock generator and an analog ground voltage reference as depicted in Fig. 8. The system is targeted for a 3-V supply. It is operated with a master clock frequency of 256 kHz, which is generated by an on-chip programmable oscillator [11] that drives the clock generator to derive all the necessary control clock signals to the respective circuit blocks. Hence, each channel has a 2- μ s processing time such that the settling time for each amplifier should be no more than 1 μ s on the basis of half a clock period in each allocated channel period. At this juncture, the current work does not place emphasis on low-power op-amp implementation or low-power optimization. The op-amp, which is implemented using a standard folded-gain stage in cascade with rail-to-rail push-pull output stage in Fig. 9, is applied for the SC filters, the SC gain circuit and the voltage reference. Each SC bandpass filter, designed with the programmable functions, has the specifications as follows:

- 1) centre frequencies (CFs): 300 Hz, 1.5 kHz, 3.5 kHz, and 6 kHz;
- 2) BW: 550 Hz, 850 Hz, and 1.5 kHz;
- 3) gain: -12 dB, -6 dB, 0 dB, +6 dB, and +12 dB.

The SC gain circuit provides gain as well as external drive capability for testing purpose. It outputs the signals of all channels in TM manner on a single output pin.

B. Crosstalk Reduction Layout

Despite C_{stray1} and C_{stray2} are suppressed through circuit design techniques, C_{stray3} becomes the key contributor for inter-channel residual crosstalk. The amount of this coupling effect depends on several layout issues. They are: 1) separation between adjacent channels; 2) length of the parallel edge along the integrating capacitors; 3) topological placement of channel integrating capacitors; 4) area utilization tradeoff and 5) the size of integrating capacitor which is determined by the sampling frequency and the capacitance ratio.

Fig. 10 shows the exemplary layout for placement of two channel integrating capacitors, where an electrostatic shield is established between CA and CB . Electric field coupling between CA and CB is reduced, thus contributing smaller C_{stray3} . Of particular interest, CA and CB are placed in separate wells to avoid electric field coupling through the same well. In addition, an intermediate n-well, which is added to surround the shield line, further minimizes inter n-well electric field coupling.

Besides the shielding technique, the crosstalk can be further reduced via the use of diagonal layout topology, where the structure is not sensitive to the parallel fringing field. Fig. 11(a) shows a 4-channel compact layout with two diagonal channel pairs (A and C , B , and D) together with the associated shield lines as described before. The use of compact layout aims at reducing the silicon area. If the space is sufficient, it is possible to place the integrating capacitors in entire diagonal configuration, as illustrated in Fig. 11(b), but at a cost of approximately doubling the area of integrating capacitors. However, this ensures that coupling crosstalk is maintained low for every channel. In a case of the channel numbers exceeding four, the topological placement can be extended to the arrangement as shown in Fig. 11(c) for an 8-channel diagonal layout example.

For new deep submicrometer processes in advanced integrated circuit manufacturing technologies, metal-insulator-metal (MIM) capacitor has emerged as an attractive integrated element for mixed-signal IC applications on the basis of high dielectric constant, good matching, high- Q factor, low deposition temperature (400 °C) and ease of integration at the expense of higher masking cost. Due to relative thicker dielectric, it usually exhibits smaller capacitance per unit area than double-poly capacitor for comparison to same technology but MIM capacitor can be wired in parallel on two or more levels so as to yield an equivalent multiple increase in unit capacitance, hence saving the silicon area, and which also benefits SC design in terms of matching and area-efficiency. Although it is well known that frequency-dependence performance of nitride-based MIM capacitor is not as good as double-poly capacitor, the baseband mixed-signal IC application like the implementation proposed herewith, does not cause any significant deviation of circuit performance. More importantly, MIM capacitor can be manufactured with low parasitics, which gives greater possibility for improving the performance of multiplexed SC circuit designs.

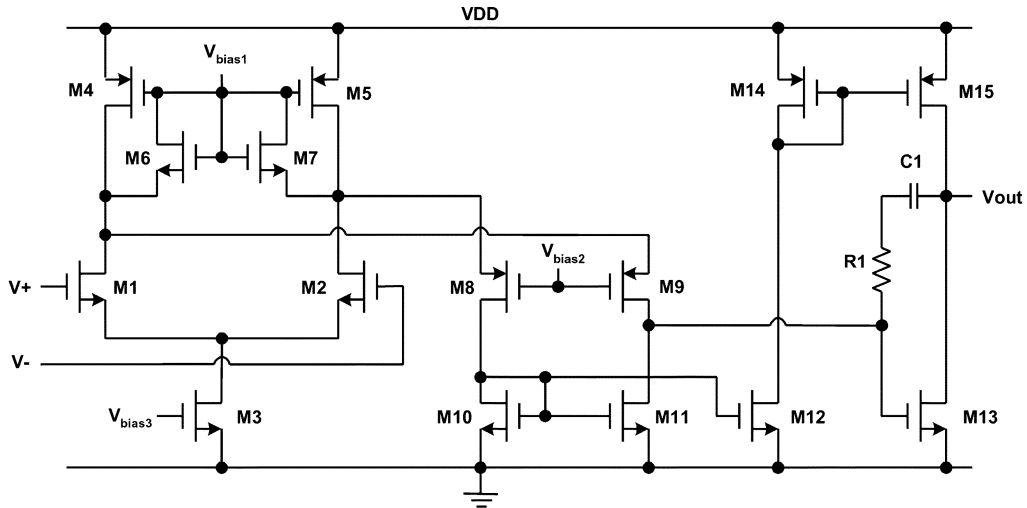


Fig. 9. Conventional folded-gain op-amp with rail-to-rail push-pull output stage.

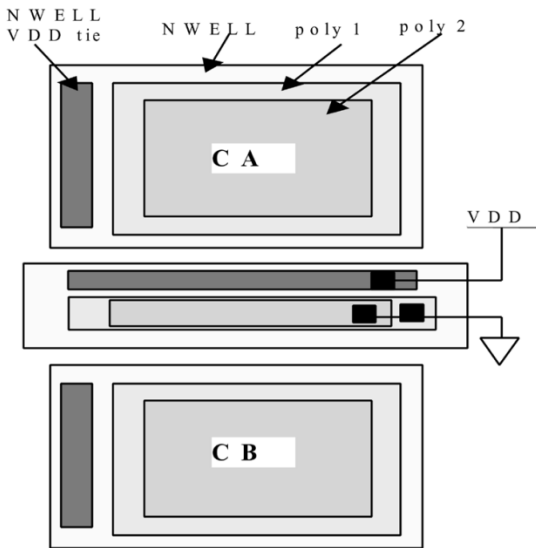


Fig. 10. Crosstalk reduction between adjacent capacitors via electrostatic shielding.

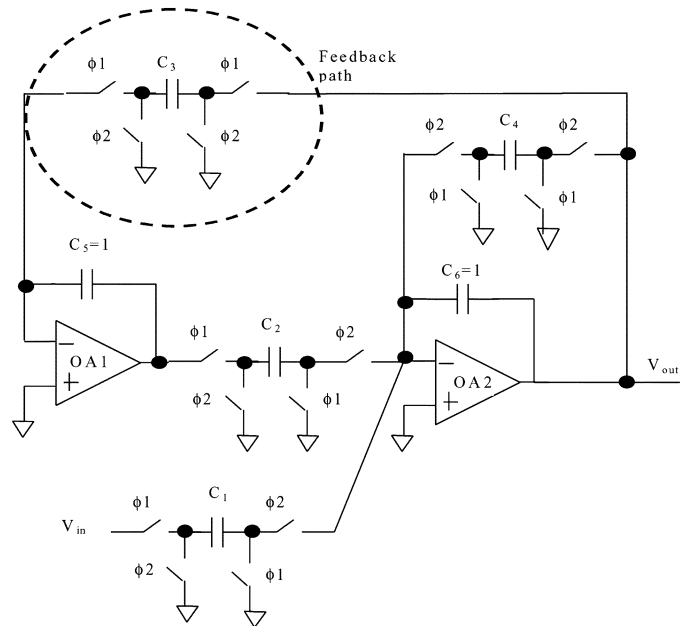


Fig. 12. Low- Q bandpass SC biquad foundation circuit.

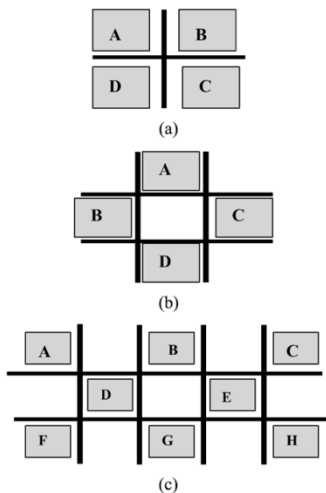


Fig. 11. Coupling crosstalk reduction using shield and diagonal layouts. (bold lines indicate electrostatic shielding). (a) 4-channel compact layout with two diagonal pairs and shield. (b) 4-channel with entire diagonal layout and shield. (c) Multi-channel with entire diagonal layout and shield.

IV. IMPLEMENTATION OF TM EQUALIZER

The TM-SC equalizer is constructed from the cascade of two low- Q bandpass SC biquad circuits. Fig. 12 shows the foundation circuit of the low- Q bandpass SC biquad circuit, which is modified from a general biquad [10]. However, it is not straightforward to implement multiplex function directly since the sampling capacitor C_3 is reset for every ϕ_2 clock phase. To overcome this drawback, a 4-channel TM CDS biquad is proposed in Fig. 13. Note that similar to Fig. 7, clocks A, B, C, and D are the individual channel active time control signals, whose duration covers both ϕ_1 and ϕ_2 . The transfer function of each TM channel can be derived as

$$\begin{aligned}
 H_i(z) &= \left. \frac{V_{outi}(z)}{V_{ini}(z)} \right|_{i=A,B,C,D} \\
 &= \frac{k_{1i}(z-1)}{(1+k_{4i})z^2 + (k_{2i}k_{3i} - k_{4i} - 2)z + 1} \quad (4)
 \end{aligned}$$

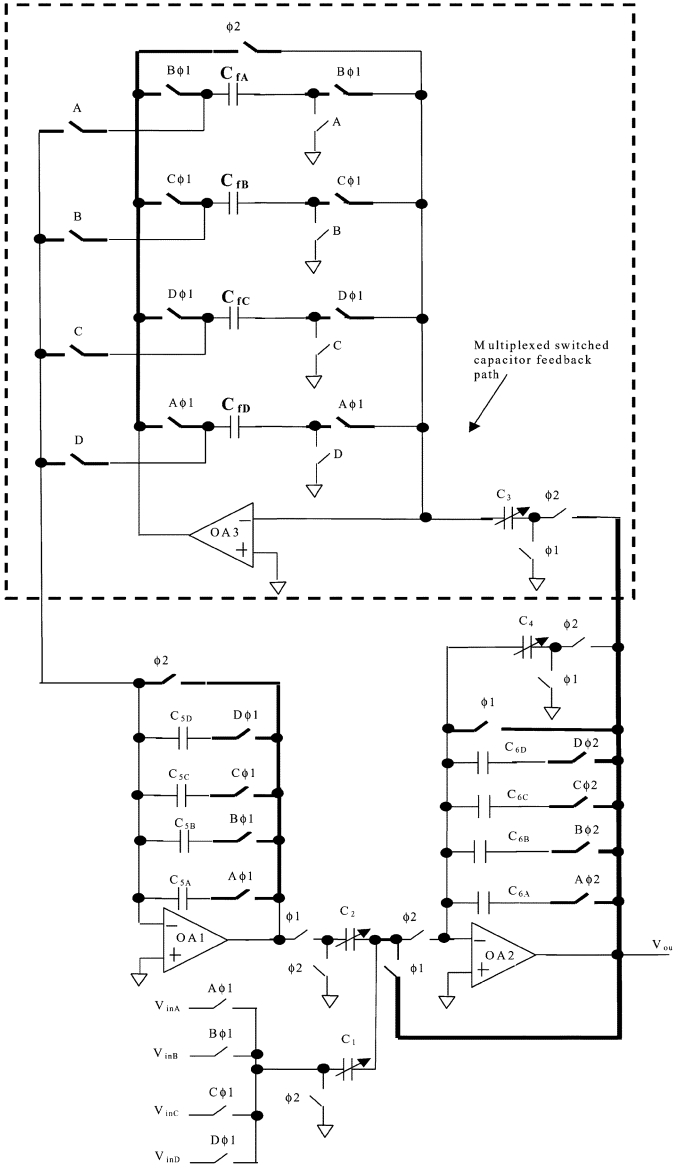


Fig. 13. TM bandpass SC biquad with CDS and reset action within two clock phases.

where i suffix ($i = A, B, C, D$) denotes the channel designation, $C_{5i} = C_{6i}$, $k_{1i} = C_1/C_{5i} = C_1/C_{6i}$, $k_{2i} = C_2/C_{5i} = C_2/C_{6i}$, $k_{3i} = C_3/C_{5i} = C_3/C_{6i}$, and $k_{4i} = C_4/C_{5i} = C_4/C_{6i}$.

It is also noted that for pipelined and multi-channel operation, the SC noninverting resistor feedback path formed by C_3 and associated switches in Fig. 12 is replaced with a multi-channel noninverting sample-and-hold circuit (dotted line) in Fig. 13. The sample-and-hold network in association with the integrating capacitors C_{5A} , C_{5B} , C_{5C} , and C_{5D} has the following relationship:

$$\left. \frac{C_3}{C_{5i}} \right|_{i=A,B,C,D} = \left(\frac{C_3}{C_{fi}} \right) \times \left(\frac{-C_{fi}}{C_{5i}} \right). \quad (5)$$

The term C_3/C_{5i} determines one of the coefficients in the biquad transfer function according to (4). The first gain factor (C_3/C_{fi}) quantifies the charge transfer between the sampling C_3 and the feedback capacitor C_{fi} whereas the second gain factor

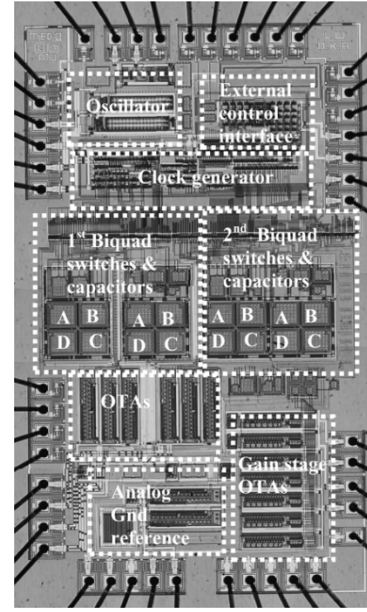


Fig. 14. Microphotograph of the CDS-TM-SC equalizer.

($-C_{fi}/C_{5i}$) quantifies the charge transfer between the feedback capacitor C_{fi} and the integrating capacitor C_{5i} . It is also of interest to observe that C_{fi} does not affect the transfer function in (5). However, the value of C_{fi} should not be too small due to switch charge injection consideration.

In [9] and the present biquad circuit, the CDS technique was implemented with a channel reset switch within a 2-phase nonoverlapping clock scheme. The CDS technique can be seen as a natural extension of the channel reset feature found in [1], [4]. When used together, it improves the crosstalk performance, lowers the output offset as well as the system $1/f$ noise.

The present single-ended biquad circuit can be implemented in a fully differential structure whereby the critical problems associated with the clock feedthrough, switch charge injection and substrate noise or environmental noise can be further suppressed, but at the expense of increased silicon area and circuit components.

V. RESULTS AND DISCUSSION

The microphotograph of the complete 4-channel TM-SC CDS equalizer is depicted in Fig. 14. Fabricated by a standard $0.8\text{-}\mu\text{m}$ CMOS technology, the total active analog area on chip is $2 \times 2.6 \text{ mm}^2$ (excluding house keeping circuitries such as oscillator, external control interface, clock generator and IO pads). As can be observed, the crosstalk reduction layout has been implemented using the compact layout with shielding scheme as described in Section III on the basis of Fig. 11(a).

A. Frequency Responses

The programmable functions for CF, BW, and gain have been exercised to verify the functionality of the IC. With the programmable clock frequency tuned to 256 kHz through the external resistor [11] as depicted in the system block diagram of Fig. 8, the measured results on the Channel A of the filter bank are illustrated in Figs. 15–17, respectively. Table I summarizes

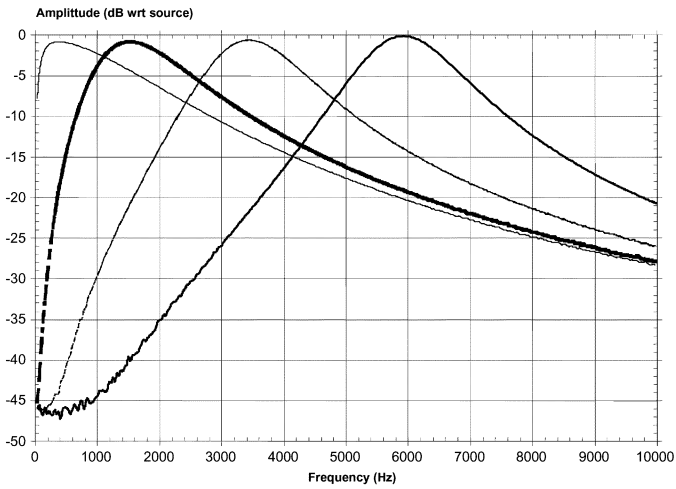


Fig. 15. Programmable CF of 300 Hz, 1.5 kHz, 3.5 kHz, and 6 kHz at BW of 1.5 kHz.

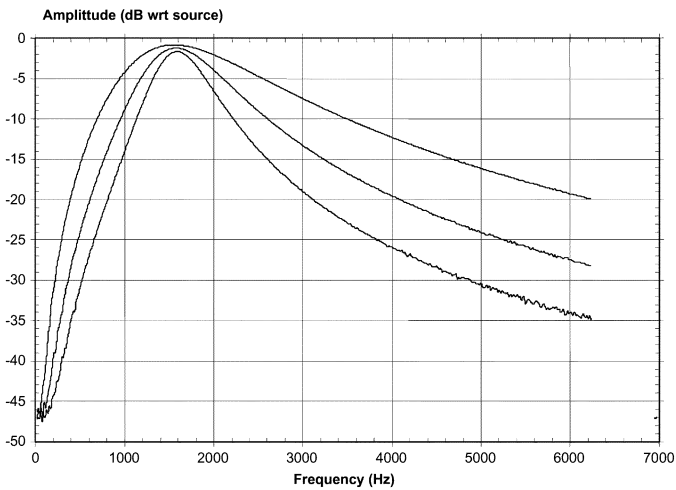


Fig. 16. Programmable BW of 550 Hz, 850 Hz, and 1.5 kHz at CF of 1.5 kHz.

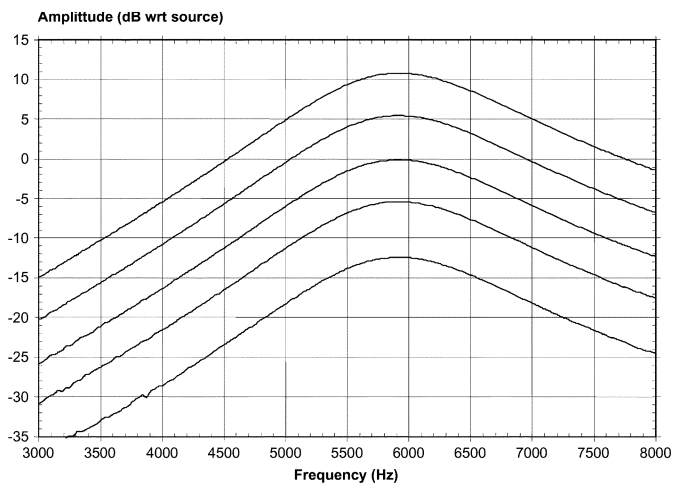


Fig. 17. Programmable gain of 0 dB, ± 6 dB and ± 12 dB at CF of 6 kHz.

the comparison of the measured accuracy of Channel A with respect to ideal CFs and the relative matching between adjacent Channel B. Except at CF of 300 Hz, all the other frequency responses are close to the design values. The relative higher devia-

TABLE I
CF ACCURACY FOR CHANNEL A AND ITS MATCHING WITH ADJACENT CHANNEL B

Ideal center frequency (Hz)	Measured channel A center frequency (Hz)	Channel A accuracy with respect to ideal frequency (%)	Channel B matching with respect to channel A (%)
300	325	8.33	-0.30
1500	1522	1.47	-0.54
3500	3460	-1.14	-0.45
6000	5940	-1.00	-0.50

TABLE II
ADJACENT CHANNEL CROSSTALK WITH REFERENCE TO CHANNEL A AT IDENTICAL PASSBAND FOR ALL CHANNELS

Adjacent channel crosstalk Source at channel A			
CF (Hz)	Xtalk at B (dB)	Xtalk at C (dB)	Xtalk at D (dB)
300	-41	-70	-47
1500	-42	-69	-49
3500	-50	-65	-49
6000	-40	-64	-55

TABLE III
ADJACENT CHANNEL CROSSTALK WITH REFERENCE TO CHANNEL B AT IDENTICAL PASSBAND FOR ALL CHANNELS

Adjacent channel crosstalk Source at channel B			
CF (Hz)	Xtalk at C (dB)	Xtalk at D (dB)	Xtalk at A (dB)
300	-41	-70	-54
1500	-41	-70	-51
3500	-49	-69	-51
6000	-40	-63	-53

TABLE IV
FAR APART PASSBANDS CHANNEL CROSSTALK WITH REFERENCE TO CHANNEL D AT DIFFERENT PASSBANDS FOR ALL CHANNELS

Far apart passbands channel crosstalk Source at channel D, CF = 300 Hz			
Channel	A CF=6k	B CF=3.5k	C CF=1.5k
Xtalk (dB)	-50	-65	-63

tion at 300 Hz is due to larger mismatching error of the capacitor ratio under large time constant implementation in SC filter circuit. However, the gain loss at different CFs is in the range of -0.1 to -0.8 dB as indicated by the normal frequency responses in Fig. 15. Fig. 16 depicts the tuning of BW at CF of 1.5 kHz, with maximum BW error of $+7.3\%$ and additional gain drop of about -1 dB for maximum Q setting. For gain tuning, the gain variation at different gain settings is about $+1$ dB/ -0.5 dB at maximum gain of ± 12 dB in Fig. 17. Besides, the adjacent channel matching performance is reasonably good.

B. Crosstalk Results

The measured crosstalk figures are given in Tables II–IV, respectively. Refer to Table II, there is significant reduction of crosstalk between Channels A and C when compared to that of Channel A to the rest of the channels (B or D). Up to -70 dB crosstalk is attainable. This is because the integrating capacitors of Channels A and C are placed diagonally in Fig. 11(a). Similar results are also obtained between Channels B and D

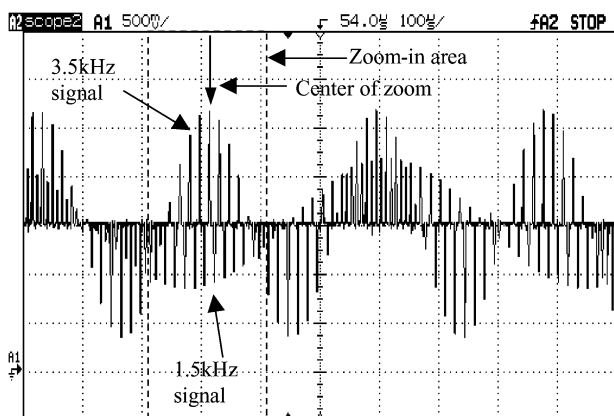


Fig. 18. TM output of Channel A and Channel C.

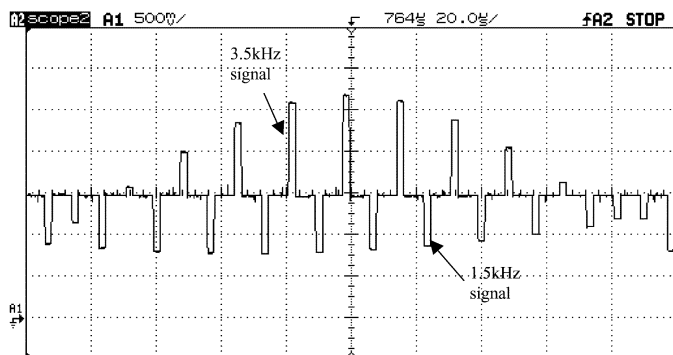


Fig. 19. Zoomed in view of TM output of Channel A and Channel C.

in Table III. The asymmetrical crosstalk values, measured from Channel B with reference to Channel A and vice versa as an example, are accounted for unequal metal routings from the output of op-amp to the respective switch that is connected to channel integration capacitor. Improving the routing layout will make further balance in the channel crosstalk performance. Nevertheless, the electrostatic shield for nondiagonal channels in compact layout together with the clamping switch at least maintains comparable results, of the order -40 dB, with that of the layout style [2] (without clamping switch but having far separation between channel integration capacitors) and exhibits improved results when referring to other approaches [1], [8] (with clamping switch but absence of shielding technique). It will be expected that further lower adjacent crosstalk is possible when employing entire diagonal layout style as depicted in Fig. 11(b) at the expense of increased silicon area. When considering the crosstalk for far apart passbands, the measured values, listed in Table IV, indicate the range from -50 to -65 dB. This also validates the effectiveness of the layout plan.

C. Other Performance Parameters

The time-domain response of the filter to 2 separate inputs in Channels A and C is illustrated in Fig. 18. The input to Channel A was a 3.5-kHz 2.3-Vpp sinusoid. The input to Channel C was a 1.5-kHz 1.4-Vpp sinusoid. It can be seen that the outputs of both channels are displayed in TM form at the output. Both output waveforms are symmetrical with reference to the midpoint potential of 1.5 V. The zoom in view shown in Fig. 19 has confirmed that the op-amp can settle down within half a clock

TABLE V
INPUT-REFERRED DC OFFSETS IN CHANNEL A

Input-referred DC offset (mV): Setting: channel A Bandwidth = 1.5 kHz, Gain = 0dB			
CF = 300Hz	CF = 1.5kHz	CF = 3.5kHz	CF = 6kHz
$C_2 = 0.65\text{pF}$ $C_3 = 0.65\text{pF}$	$C_2 = 3\text{pF}$ $C_3 = 3\text{pF}$	$C_2 = 7\text{pF}$ $C_3 = 7\text{pF}$	$C_2 = 12\text{pF}$ $C_3 = 12\text{pF}$
V_{in_offset} = -15.3 mV	V_{in_offset} = -3.3 mV	V_{in_offset} = -1.3 mV	V_{in_offset} = -1.3 mV

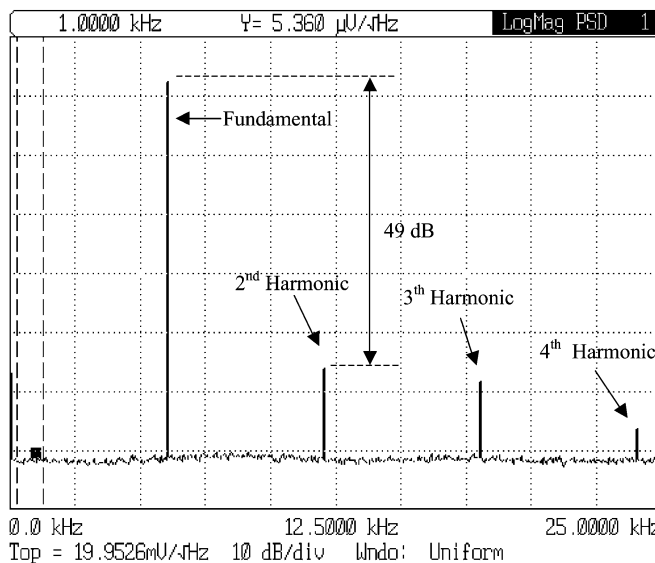


Fig. 20. Measured output noise floor of the equalizer with 6 kHz, 0.5 Vp output signal.

period, which is due to the use of rail-to-rail push-pull output stage in conjunction with slew-rate enhancement transistors in the op-amp circuit design.

Table V summarizes the measured input-referred offsets for Channel A in the fourth-order bandpass filter bank. The offsets are contributed by several sources as mentioned in Section II. It can be seen that for sampling capacitors $C_2 = C_3 > 3$ pF, the measured absolute offset is < 3.3 mV for most of the center frequencies. This also implies that the employment of CDS technique helps the reduction of offset arising from CMOS op-amps in the cascaded filter structure. The residual offset is mainly contributed by charge injection effect of CMOS switches. Such the effect will be pronounced when smaller values of C_2 and C_3 (0.65 pF) are selected for the center frequency $CF = 300$ Hz. However, the typical dc offset values are, in general, lower than that of previously reported structures [1], [8]. It can be confirmed that the system dc offset component is dominated by the switch channel charge injection.

The offset performance of other channels is the same as that of reported in Table V since each channel shares the same op-amps in time multiplexed manner. Regarding the noise aspects, for $CF = 6$ kHz, $BW = 1.5$ kHz and $Gain = 0$ dB in Channel A, the measured output noise root spectral density is $5.36 \mu\text{V}/\sqrt{\text{Hz}}$ as shown in Fig. 20. There is no observable $1/f$ noise in the output spectrum. For 1 Vpp, the total harmonic distortion (THD) is about 0.5%. When Channel A input is applied with a 3.5-kHz 0.3-Vp sinusoid and Channel B input is applied with

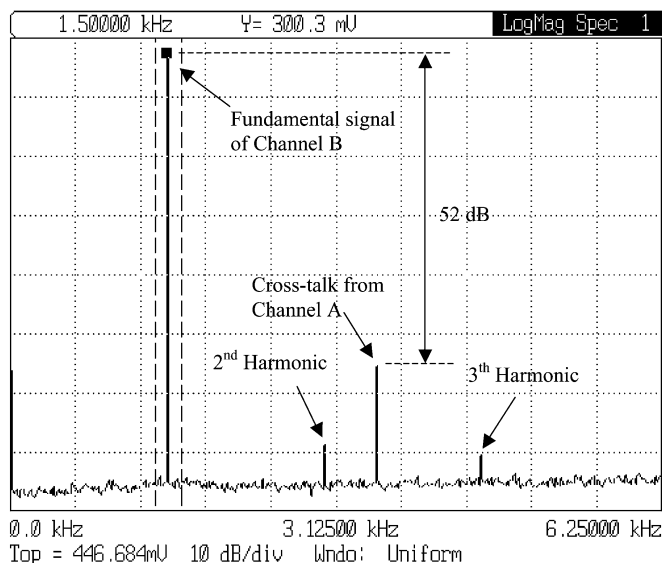


Fig. 21. Measured crosstalk effect from Channel A to Channel B.

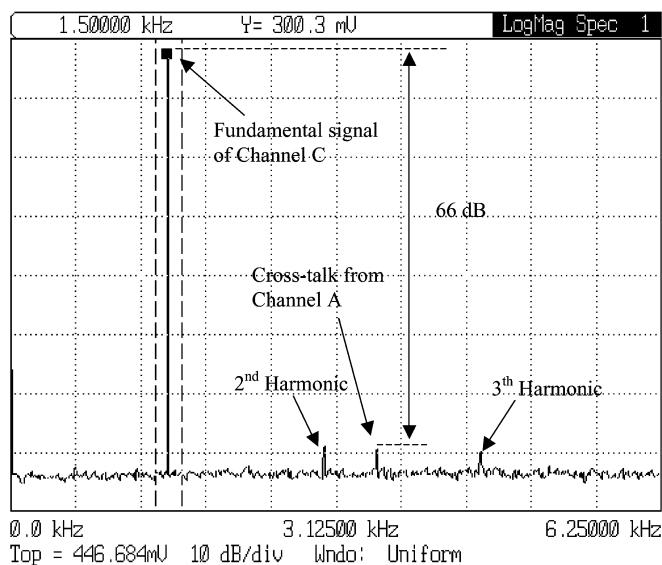


Fig. 22. Measured crosstalk effects from Channel A to Channel C.

a 1.5-kHz 0.3-V_p sinusoid simultaneously, it can be inspected from Fig. 21 that the de-multiplexed Channel B output has displayed the fundamental signal frequency of 1.5 kHz together with the harmonics and the crosstalk tone of 3.5 kHz being suppressed to -52 dB. For a similar setup condition for Channel A and Channel C, the crosstalk tone coupled from Channel A to Channel C is -66 dB as shown in Fig. 22. This confirms that the diagonal placement and shielding does improve the crosstalk performance. Regarding power-supply rejection ratio (PSRR) in a single supply, the measured PSRR₊ is -54 dB at 1 kHz and -18 dB at 15 kHz at identical setting with that of noise measurement setup in Channel A.

D. Comparison With Other TM-SC Filters

The performance of the proposed CDS equalizer is compared with other previous works in Table VI. As can be seen, the general crosstalk performance is better than the prior-art works. Adding shielding technique does reduce the crosstalk figure.

TABLE VI
PERFORMANCE COMPARISON WITH OTHER TM FILTERS

Parameter	Ref. [1]	Ref. [2]	Ref. [4]	Ref. [8]	Ref. [9]	This Work
Technology	5 μm NMOS	7.5 μm NMOS	6 μm CMOS	1.2 μm CMOS	0.8 μm CMOS	0.8 μm CMOS
Supply (V)	+15/-5	—	3	3	3	3
Multiplex Channel No	20	2	8	1	2	4
F _{sample} per Channel (kHz)	20	100	16 for 4 ch. 32 for 4 ch.	50	128	64
Filter Order	2	5	2	4 (N=2)	2	4
Filter Type	BPF	LPF	BPF	HP +BPF	LPF	BPF
Filter Topology	Single-Ended	Single-Ended	Single-Ended	Fully Diff.	Single-Ended	Single-Ended
Clamp Switch	Yes	No	Yes	No	Yes	Yes
Crosstalk Range (dB)	-50	-40	-27 to -40	—	-32 to -42	-40 to -70
Maximum Gain Loss (dB)	-5	-1	-2	-2	-1.38	-0.8
Normal Response	—	—	—	—	—	—
Input-referred DC Offset (mV)	200 to 300	—	—	—	10.0 to 13.5	-1.3 to -15.3

With introducing diagonal layout structure, the crosstalk is further minimized. When considering precision issue, owing to the reduction of the crosstalk, the gain loss (-0.1 dB to -0.8 dB) being translated from the results of frequency response curves, is also reduced when compared with the previous reported measurement results [1], [2], [4], [8], [9]. Incorporating CDS technique permits to suppress the offsets arising from the op-amps or parasitic circuit gain effect but it is subject to charge injection effect. The obtained dc offsets are acceptable. Through combination of CDS technique and shielding layout style, the 1/f noise becomes insignificant whereas the shielding guard lines also reduce the sampling noise coupling from idle channels. Hence, the overall S/N ratio is good.

VI. CONCLUSION

A new equalizer using the previous reported TM integrator is presented. Through the use of CDS technique and crosstalk reduction layout technique, the equalizer has achieved improved crosstalk range and offsets, low gain loss and good S/N ratio in a single 3-V supply. The proposed techniques would be useful for SC signal processing circuits.

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K. A. Ng was born in Singapore. He received the B.E. degree in electrical and electronic engineering and M.E. degree in integrated circuit design from Nanyang Technological University, Singapore, in 2000 and 2005, respectively.

From 2000 to 2004, he was with Asia Pacific Design Center of STMicroelectronics, Singapore, working on smartcard radio frequency identification circuits (RFID) and analog intellectual property (IP) design. Currently, he has joined Chartered Semiconductor Manufacturing, Singapore, working on

high performance analog IP development. His main research interest includes precision analog circuits, switched-capacitor circuits, and RFID.



P. K. Chan was born in Hong Kong. He received the B.Sc. (Hons.) degree from the University of Essex, Colchester, U.K., the M.Sc. degree from the University of Manchester, Institute of Science and Technology (U.M.I.S.T.), Manchester, U.K., and the Ph.D. degree from the University of Plymouth, Plymouth, U.K. in 1987, 1988, and 1992, respectively.

From 1989 to 1992, he was a Research Assistant with the University of Plymouth, working in the area of MOS continuous-time filters. In 1993, he joined the Institute of Microelectronics (IME) as a Member

Technical Staff, where he designed CMOS sensor interfaces for industrial applications. In 1996, he was a Staff Engineer with Motorola, Singapore, where he developed the magnetic write channel for Motorola 1st generation hard-disk preamplifier. He joined Nanyang Technological University (NTU), Singapore, in 1997, where he is currently an Associate Professor in the School of Electrical and Electronic Engineering and Program Director [analog/mixed-signal integrated circuit (IC) and applications] for the Center for Integrated Circuits and Systems (CICS). He holds four patents and is an IC Design Consultant to local and multi-national companies in Singapore. He has also conducted numerous IC design short courses to the industrial companies and design centers. His research interests include circuit theory, amplifier frequency compensation techniques, sensing interfaces for integrated sensors, biomedical circuits and systems, integrated filters and data converters.