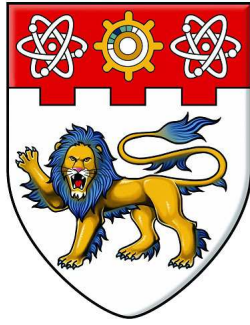


DESIGN ISSUES IN SILICON CARBIDE POWER CONVERTERS YIN SHAN 2016



**NANYANG
TECHNOLOGICAL
UNIVERSITY**

**DESIGN ISSUES IN SILICON CARBIDE
POWER CONVERTERS**

YIN SHAN

School of Electrical and Electronic Engineering

2016

**DESIGN ISSUES IN SILICON CARBIDE
POWER CONVERTERS**

YIN SHAN

School of Electrical and Electronic Engineering

A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
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Abstract

The trend towards more electric aircraft (MEA) requires replacement of the existing non-propulsive powers including hydraulic, pneumatic and mechanical systems by the electric power. Due to the strict demands on space and weight for lower fuel consumption in aircraft, a high power density converter (HPDC) is needed. The conventional Si power converter has difficulty meeting all these requirements due to the switching frequency limitation. In addition, the trend to directly mount the electric generator/starter with power converter on the shaft of gas turbine engine will subject the power converter to high ambient temperatures above 200 °C, which makes Si totally unacceptable for this application. The wide bandgap (WBG) material silicon carbide (SiC) is regarded as the next-generation semiconductor for the high power density and harsh environment applications.

In this thesis, the key technologies related to the development of SiC-based HPDC for MEA application are investigated. Basically, there are two strategies to push the power density envelope. From the electrical point of view, the power converter needs to operate at high switching frequency to reduce the size of passive components, like the DC-link capacitor and output filter. From the thermal point of view, the heat sink size needs to be minimized by use of advanced cooling method. Hence, the issues encountered when applying these two strategies are addressed in this work.

By maximizing the switching frequency of SiC power converter, this tends to deteriorate the electromagnetic interference (EMI) issue and dv/dt , di/dt effects. Hence, the circuit simulation models for the SiC power devices are developed to assist the gate driver and converter design firstly. Then the gate driver is optimized and a novel gate assisted circuit is proposed to resolve the shoot-through issue in the classical half bridge configuration. In addition, a novel high-speed short-circuit protection scheme based on gate charge detection is proposed. The stray inductances for both gate driver and converter are minimized during layout

design. To reach the optimized converter design, the switching characterizations for various SiC power devices are conducted based on the universal double pulse testing setup. Furthermore, an integrated micro-channel heat sink is proposed for the SiC power module. Hence, the size of heat sink can be minimized while the cooling efficiency is maximized. Finally, the 1st generation prototype of liquid-cooled SiC-based HPDC based on three-phase two-level voltage source inverter is developed and tested with 50 kW output power, ± 375 Vdc input voltage, 230 Vac out voltage, 60 kHz switching frequency, 98% efficiency, and 32 kW/L power density.

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Nomenclature

List of Abbreviations

ABM	Analog Behavioral Modeling
AGVC	Active Gate Voltage Control
AlN	Aluminum Nitride
APU	Auxiliary Power Unit
BJT	Bipolar Junction Transistor
CFD	Computational Fluid Dynamics
CMRR	Common Mode Rejection Ratio
CSD	Current Source Driver
CT	Current Transformer
CTE	Coefficient of Thermal Expansion
DBC	Direct Bond Copper
DOS	Density Of State
DPT	Double Pulse Testing
DSP	Digital Signal Processor
DUT	Device Under Test
ECS	Environmental Control System
EMI	Electromagnetic Interference
EPC	Equivalent Parallel Capacitance
ESL	Equivalent Series Inductance
FFT	Fast Fourier Transform
FUL	Fault Under Load
FWD	Freewheeling Diode
GAC	Gate Assisted Circuit
GaN	Gallium Nitride
HEV	Hybrid Electric Vehicle
HPDC	High Power Density Converter
HS	High Side
HSF	Hard Switching Fault
IC	Integrated Circuits
ICE	Internal Combustion Engine
IDG	Integrated Drive Generator

NOMENCLATURE

IGBT	Insulated-Gate Bipolar Transistor
IPEM	Integrated Power Electronics Module
IPS	Ice Protection System
JBS	Junction Barrier Schottky
JFET	Junction Field-Effect Transistor
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LPF	Low Pass Filter
LS	Low Side
MCHS	Micro-Channel Heat Sink
MEA	More Electric Aircraft
MLCC	Multi-Layer Ceramic Capacitor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPS	Merged PiN/Schottky
NO	Nitric Oxide
NPC	Neutral Point Clamping
NSC	Network Side Converter
PCB	Printed Circuit Board
PEBB	Power Electronics Building Block
PWM	Pulse Width Modulation
RAT	Ram Air Turbine
RGD	Resonant Gate Driver
rms	root mean square
SCE	Short-Channel Effect
S/G	Starter/Generator
Si	Silicon
SiC	Silicon Carbide
SiO ₂	Silicon Oxide
SMPS	Switching-Mode Power Supply
SR	Synchronous Rectification
TCAD	Technology Computer-Aided Design
TIM	Thermal Interface Material
TRU	Transformer Rectifier Unit
TVS	Transient Voltage Suppression
VCCS	Voltage Controlled Current Source
VSD	Voltage Source Driver
VSI	Voltage Source Inverter
WBG	Wide Band Gap

NOMENCLATURE

List of Acronyms

A	Area
BV	Breakdown voltage
BW	Bandwidth
C	Capacitance
c_p	Specific heat
D	Diameter Duty cycle
E_c	Critical electric field
E	Energy
f	Frequency
Gz	Graetz number
g_m	Transconductance
H	Height
h	Heat transfer coefficient
I, i	Current
k	Boltzmann's constant Thermal conductivity
L	Inductance Length
M	Mutual-inductance
m	Mass
m_a	Modulation index
N	Doping concentration Number
n_i	Intrinsic carrier concentration
Nu	Nusselt number
P	Power Pressure
Q	Charge
q	Elementary charge
\dot{q}	Heat flux
R	Resistance Thermal resistance
Re	Reynolds number
T	Temperature
t	Thickness Time
V, v	Voltage
W	Width

NOMENCLATURE

ε	Dielectric constant
η	Efficiency
λ	Channel modulation index
μ	Carrier mobility Fluid viscosity
ξ	Damping factor
ρ	Density
τ	Time constant
ϕ	Potential Phase angle

Chapter 1

Introduction

1.1 Background

The conventional architecture for aircraft power system is a combination of pneumatic, mechanical, hydraulic and electrical hybrid subsystems, as Figure 1.1 shows [1]. The fuel is converted into propulsive power by the main engine, which is the dominant factor of total power consumption. Then the rest of power is converted into the four main forms of non-propulsive power as aforementioned. However, with the increasing complexity of each subsystem, the interactions between them tend to reduce the system efficiency and reliability.

The trend in moving towards more electric aircraft (MEA) is to replace the traditional non-electrical power subsystems by increasing use of electric power. The mechanically driven engine accessories, oil pump, fuel pump, hydraulic pump and generators are replaced by the electrically driven machines and generators. The concept of MEA had been considered for fighter planes since World War II [2]. However, the lack of electrical power generation capability made it unpractical at that time. The advancements in electric machines and solid-state power electronics have enable the demonstration of MEA. It significantly improves the reliability and reduces the maintenance cost, fuel consumption and overall weight/volume of aircraft.

As Figure 1.2 shows, the requirement of electrical power in aircraft is increasing year by year. And more and more non-electrical subsystems including pneumatic, mechanical and hydraulic power are partially or fully replaced by electrically powered systems. Several examples of electrification in the existing MEA Boeing 787 are introduced in the following section [3, 4].

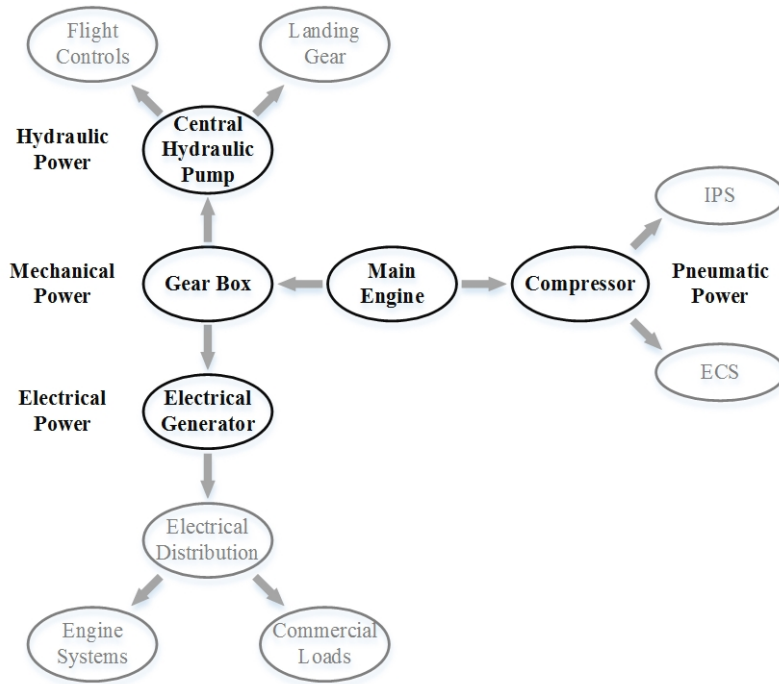


Figure 1.1: Conventional aircraft power distribution system.

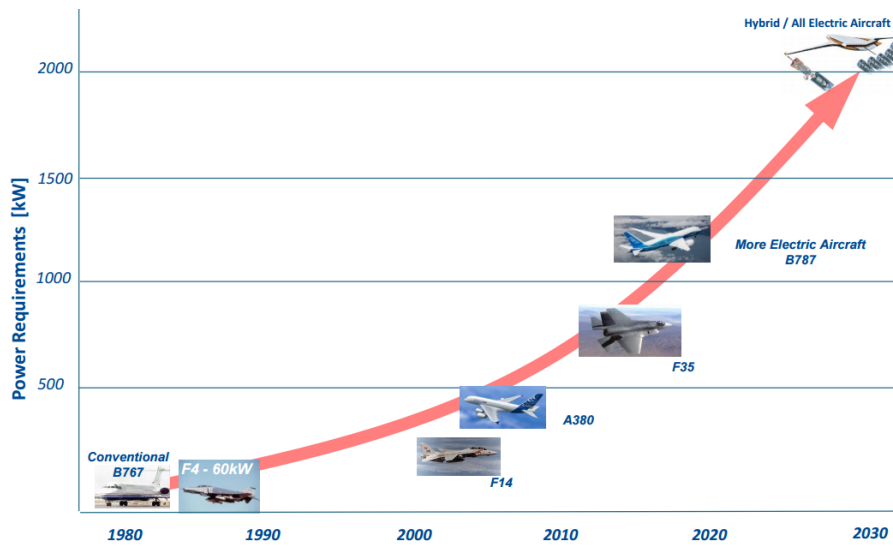


Figure 1.2: Progression of aircraft electrical power requirements (Courtesy of Rolls-Royce).

A. Environmental Control System

The environmental control system (ECS) is used to regulate the cabin pressure and temperature. In the traditional architecture of aircraft, it uses the bleed air obtained from the compressor of main engine. In the no-bleed architecture of Boeing 787, the electrically driven compressor is used to regulated the pressure and temperature. Hence, it significantly improves the fuel consumption efficiency as it avoids excessive energy extraction from engine.

B. Ice Protection System

In the traditional architecture of wing ice protection system (IPS), the hot bleed air from bleed system is distributed through the areas of wing leading edge. The flow of bleed air is controlled by a valve and the heat is evenly distributed along the protected areas by a duct. The Boeing 787 adopts an electro-thermal IPS with the heating blanket bonded to the leading edge. Similarly, this approach is more efficient than the traditional system since no excessive energy is exhausted.

C. Auxiliary Power Unit

Traditional auxiliary power unit (APU), which is a gas turbine engine, provides both pneumatic and electric power to the aircraft. While on the ground, the compressed air is provided by APU to start the main engines. While in the air, it can be used under emergency conditions. With the electrically driven motor, it is now practical to eliminate the pneumatic function from APU [5]. This simpler electric-only APU results in a significant improvement in reliability and maintenance.

D. Stater/Generator

The Boeing 787 employs 4 main engine generators (2 per engine). And each of them has a power rating of 250 kVA. Additionally, it employs another 2 APU generators and each of them has a power rating of 225 kVA. In this new architecture, the main engine generator can also operate as motor to start the engine,

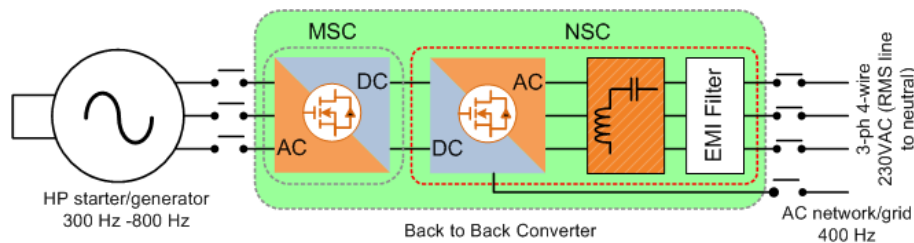


Figure 1.3: Diagram of back-to-back power converter for S/G application.

hence it is called as starter/generator (S/G). While on the ground, the AC power from APU generator is converted to DC power and then back to AC power to achieve the variable voltage and frequency control of S/G, and therefore it works as starter. While in the air, it will work as generator and operate at a variable frequency proportional to engine speed. Hence, a back-to-back power converter is needed for S/G application, as Figure 1.3 shows. Considering the weight and space constraints in aircraft, high power density is required. In addition, the advancement in power converter and electrical machine have permitted the possibility to directly mount the S/G on the shaft of gas turbine engine, leading to a direct exposure of power converter to the high ambient temperature of 200~250 °C. Hence, it brings a new challenge in the power converter design for high power density and harsh environment applications.

Over the past half century, replacement of the bulky vacuum tubes by the compact Si-based solid-state devices and integrated circuits (IC) has given rise to a revolutionary change on avionics systems. With the ever increasing demand on high power density and high temperature of avionics systems, the conventional Si power converters become hard to maintain high performance for this application. To increase the power density, the power converter needs to work at high switching frequency to reduce the filter size. However, the switching frequency of most commonly used Si power device IGBT is normally restricted below 20 kHz, and the further increase of switching frequency seems unpractical. In addition, the junction temperature of Si devices and ICs is currently within the MIL-STD temperature range of -55~125 °C, which is unacceptable for the embedded S/G in MEA. Currently, one solution in the hybrid electric vehicle (HEV) of Toyota is to adopt two separate cooling loops [6], in which the temperatures of coolant for power converter and engine are 65 °C and 105 °C, respectively. However, this complicated cooling system design is apparently unfavorable in aerospace converter.

Recently, the wide band gap (WBG) semiconductor material silicon carbide (SiC) has become a promising candidate for aerospace power converter [7]. The SiC power devices permit high switching frequency up to 100 kHz and high junction temperature theoretically up to 600 °C. A comparison of physical properties between Si, SiC and other WBG semiconductor materials is summarized in Table 1.1 [8].

For the unipolar power devices, the specific on-resistance is the dominant factor for conduction loss, which is the product of on-resistance and active area

Table 1.1: Physical properties of Si, 4H-SiC, GaN and diamond.

Property	Si	4H-SiC	GaN	Diamond
Critical electric field (MV/cm)	0.25	2.2	2	10
Electron saturation velocity (10^7 m/s)	1	2	2.2	2.7
Band gap (eV)	1.12	3.26	3.45	5.45
Relative dielectric constant	11.7	10	9	5.5
Thermal conductivity at 300 K (W/mK)	150	370	130	2200

of device. And the relationship with breakdown voltage is given by

$$R_{on,sp} = \frac{4BV^2}{\varepsilon\mu_n E_c^3} \quad (1.1)$$

where ε is the dielectric constant, μ_n is the electron mobility and E_c is the critical electric field. And the denominator $\varepsilon\mu_n E_c^3$ is commonly referred as *Baliga's Figure of Merit* for Power Devices [9], which indicates the impact of semiconductor material on specific on-resistance. Since the critical electric field of SiC is around one order of magnitude higher than that of Si, it is practical to fabricate high voltage and low specific on-resistance SiC unipolar power devices, which means a smaller conduction loss. In addition, the active area of SiC dies can also be reduced for the same current rating as Si counterpart. Hence, the parasitic capacitances can be smaller, leading to a higher switching speed and lower switching loss.

The intrinsic carrier concentration of semiconductor material is determined by the thermal generation of electron-hole pairs across the band gap

$$n_i = \sqrt{N_C N_V} \exp\left(\frac{-E_G}{2kT}\right) \quad (1.2)$$

where N_C and N_V are the density of states in the conduction band and valence band respectively, E_G is the energy band gap, k is Boltzmann's constant and T is the temperature. According to the Shockley equation, the leakage current of the classical PN junction in semiconductor device is proportional to the square of intrinsic carrier concentration [10]. For Si, n_i is close to the typical doping concentration $1 \times 10^{15} \text{ cm}^{-3}$ at 250 °C. Hence, the Si power devices can no longer operate in a normal way due to the tremendous leakage current at high temperature. As the band gap of SiC is around 3 times larger than that of Si, n_i is far below $1 \times 10^{15} \text{ cm}^{-3}$ even when the temperature rises up to 600 °C. This fundamental semiconductor physics theory explains why SiC is capable of high temperature

operation.

Among the three types of WBG materials, diamond shows the most promising performance with largest bandgap. However, the processing issue is still unsolved and only a few results were available on diamond diode [11]. Due to the lack of native oxide, it is difficult to obtain GaN MOSFET. In addition, the poor thermal conductivity of GaN makes it less favorable in high temperature applications compared with SiC. Hence, GaN is preferred for opto-electronics and radio frequency (RF) applications [8].

1.2 Motivation and Objective

This work is devoted to investigation and development of the key technologies related to the SiC high power density converter (HPDC) for aerospace applications. To increase the power density, a typical strategy is to increase the switching frequency so as to reduce the size of passive components, like the DC-link capacitor and output filter. Hence, the SiC power converter needs to operate at high-speed switching to reach the maximum switching frequency, which leads to a lot of new challenges.

- The higher dv/dt at turn-on increases the risk of shoot-through in the half bridge configuration, which leads to higher switching loss and overstress on device. In addition, the conventional gate driver relies on the optocoupler as the isolator, which has a typical common mode rejection ratio (CMRR) up to $40 \text{ kV}/\mu\text{s}$ [12]. The high dv/dt may exceed the CMRR of optocoupler.
- The higher di/dt at turn-on means a rapid current rise, which increases the risk of device failure when subjected to any short-circuit fault. In addition, the higher di/dt at turn-off leads to an overshoot voltage of Ldi/dt , especially in the situation of fast turn-off of over-current. It tends to increase the device switching loss or even leads to avalanche breakdown once it exceeds the blocking voltage of device.
- The voltage and current ringings during switching transitions lead to serious EMI issues.

In addition, the power density can also be increased from the point of view of thermal design. The weight and volume of conventional heat sink keeps increasing with the thermal resistance decreasing. It tends to offset the effort to reduce

the passive components size by increasing switching frequency. Since SiC power devices permit a theoretical junction temperature of 600 °C, the demand for the high performance cooling system can be reduced. However, the high temperature (> 200 °C) packaging for the commercial SiC power module is still lacking. The issue of miniaturized cooling system design still exists.

1.3 Major Contributions

In this work, the issues resulted from the high frequency and high-speed switching of SiC power converter in MEA application are to be resolved. And the major contributions of this dissertation are summarized as below.

- Review the up-to-date status and key issues in developing SiC power converter from the aspects of device technology, gate driver and protection schemes, packaging technology, converter design and MEA requirements.
- Develop the accurate circuit simulation models for SiC power devices including SiC Schottky diode, SiC MOSFET and SiC power module, which are implemented in the circuit simulator PSpice and show a good agreement with experiment.
- Demonstrate the design and optimization guidelines of high-speed gate driver for SiC MOSFET.
- Propose a novel gate assisted circuit for SiC power module to eliminate Cdv/dt effect in the half bridge configuration, enhance the turn-off speed and reduce switching loss.
- Propose a short-circuit protection scheme for SiC MOSFET based on gate charge detection, which shows a response time of less than 200 ns.
- Design and optimize the integrated micro-channel heat sink for power module, and also compare the cooling performances between single-side and double-side cooling, which show a junction-to-ambient thermal resistance of 0.128 and 0.058 K/W, respectively.
- Conduct a completed switching characterization for SiC power devices including SiC Schottky diode, SiC MOSFET and SiC power module. The power module is tested up to 750 V and 120 A with an optimized gate resistance, which is a tradeoff between switching frequency and EMI issues.

- Develop an accurate analytical model for power loss and efficiency estimation of three-phase voltage source inverter.
- Develop a 7 kW three-phase voltage source inverter using synchronous rectification. It shows a 98% efficiency when operating at a switching frequency of 40 kHz.
- Develop the prototype of 1st generation SiC HPDC and test up to 50 kW input power with a power density of 32 kW/L. It achieves a high efficiency up to 97.77% at 60 kHz switching frequency.

1.4 Thesis Organization

This thesis is divided into the following 8 chapters.

Chapter 1 presents the background and motivation of this work.

Chapter 2 reviews the related issues of SiC power converters, including the material properties, SiC devices, gate driver and protection circuits, packaging technology, high power density converter and power converter requirements in MEA.

Chapter 3 develops the comprehensive circuit simulation models for the commercial SiC Schottky diode, SiC MOSFET and SiC power module.

Chapter 4 presents the design of high-speed gate driver and short-circuit protection scheme for SiC MOSFET.

Chapter 5 presents the design and optimization of the integrated micro-channel heat sink used in future SiC power module.

Chapter 6 conducts the comprehensive switching characterization on SiC Schottky diode, SiC MOSFET and SiC power module.

Chapter 7 presents the development, prototyping and testing of SiC high power density converter.

Chapter 8 summarizes the completed work, and some future works are recommended.

Chapter 2

Literature Review

In this chapter, the up-to-date status and key issues in developing SiC power converter from the aspects of device technology, gate driver and protection schemes, packaging technology, high power density converter design and requirements in MEA are reviewed.

2.1 Physical Properties of 4H-SiC

Among the three most important SiC polytypes including 4H-, 6H- and 3C-SiC, 4H-SiC has the largest low field mobility [13], relatively small mobility anisotropy [14] and largest energy bandgap [15], which makes it especially attractive for power electronics applications. The major physical properties of 4H-SiC are reviewed firstly, which is also crucial for the development of circuit simulation model in the following work.

A. Energy Bandgap

The bandgap is sum of temperature-dependent exciton bandgap and constant binding energy. For 4H-SiC, the exciton bandgap is 3.265 eV and binding energy is 20 meV at low temperature (< 5 K) [15]. The temperature-dependent bandgap is given by [16]

$$E_G(T) = 3.825 - 3.3 \times 10^{-2} \frac{T^2}{T + 10^5} \text{ eV} \quad (2.1)$$

The doping-dependent bandgap is the result of bandgap narrowing effect in the heavily doped regions and given by [17]

$$\Delta E_G = A \left(\frac{N_{tot}}{10^{18}} \right)^{1/3} + B \left(\frac{N_{tot}}{10^{18}} \right)^{1/4} + C \left(\frac{N_{tot}}{10^{18}} \right)^{1/2} \text{ eV} \quad (2.2)$$

Table 2.1: Fitting parameters for bandgap narrowing effect of 4H-SiC.

Parameter	Unit	n-type	p-type
A		17.91	-35.07
B	meV	28.23	73.11
C		8.44	7.81

where A , B and C are the fitting parameters, N_{tot} is the total doping concentration. The fitting parameters for the bandgap narrowing effect is given in Table 2.1.

B. Effective Density of State

The electron effective mass is the geometric mean of the mass tensors. And the hole effective mass is related with the three uppermost valence bands. The expressions are given by

$$m_{de} = \sqrt[3]{m_{M\Gamma}m_{MK}m_{ML}} \quad (2.3)$$

$$m_{dh} = m_{dh1}^{3/2} + m_{dh2}^{3/2} \exp\left(-\frac{\Delta_{so}}{kT}\right) + m_{dh3}^{3/2} \exp\left(-\frac{\Delta_{cf}}{kT}\right) \quad (2.4)$$

where the detailed parameters can be found in [18]. At room temperature, the effective mass of electron and hole is $0.37m_0$ and $1.20m_0$ respectively, where m_0 is the static electron mass. Hence the effective density of state (DOS) is given by [10]

$$N_C = 2M_C \frac{(2\pi m_{de} kT)^{3/2}}{h^3}, \quad N_V = 2 \frac{(2\pi m_{dh} kT)^{3/2}}{h^3} \quad (2.5)$$

where M_C is the number of equivalent minima for the conduction band with the value of 3, and h is Planck's constant. At room temperature, the effective DOS can be calculated: $N_C(300) = 1.69 \times 10^{19} \text{ cm}^{-3}$, $N_V(300) = 3.30 \times 10^{19} \text{ cm}^{-3}$. The intrinsic carrier concentration is given by Eq.(1.2). And at room temperature, the intrinsic carrier concentration is as small as $1.21 \times 10^{-8} \text{ cm}^{-3}$. By comparison, the intrinsic carrier concentration of Si at room temperature is $1.4 \times 10^{10} \text{ cm}^{-3}$.

C. Effective Richardson Constant

With (0001) as the emitting face in Schottky contact, effective mass for single conduction band minimum is $\sqrt{m_{M\Gamma}m_{MK}}$. After considering M_C , effective Richardson constant is given by

$$A^* = AM_C \frac{\sqrt{m_{M\Gamma}m_{MK}}}{m_0} = 144 \text{ A/cm}^2\text{k}^2 \quad (2.6)$$

where A is Richardson constant of free electron with the theoretical value of $120 \text{ A/cm}^2\text{k}^2$.

D. Incomplete Ionization

Due to the relatively high impurity ionization energy in 4H-SiC, incomplete ionization effect needs to be considered

$$N_D^+ = n, \quad N_A^- = p \quad (2.7)$$

$$N_D^+ = \frac{N_D}{1 + g_D \frac{n}{N_C} \exp\left(\frac{\Delta E_D}{kT}\right)}, \quad N_A^- = \frac{N_A}{1 + g_A \frac{p}{N_V} \exp\left(\frac{\Delta E_A}{kT}\right)} \quad (2.8)$$

where g_D (g_A) is the donor/acceptor degeneracy factor, and ΔE_D (ΔE_A) is the donor (acceptor) activation energy. Currently, nitrogen is most widely used as donor dopant with aluminum as the typical acceptor dopant. The activation energy decreases with total doping level increasing [19]

$$\Delta E = \Delta E_0 - \alpha N_{tot}^{1/3} \quad (2.9)$$

where ΔE_0 is the activation energy for low doping level and α is the fitting parameter. Considering the charge neutrality conditions $N_D^+ = n$ and $N_A^- = p$ in the n-type and p-type semiconductors respectively, the ionized donor and acceptor concentration can be derived as

$$N_D^+ = \frac{-1 + \sqrt{1 + 4g_D(N_D/N_C)\exp(\Delta E_D/kT)}}{2g_D \exp(\Delta E_D/kT)/N_C} \quad (2.10)$$

$$N_A^- = \frac{-1 + \sqrt{1 + 4g_A(N_A/N_V)\exp(\Delta E_A/kT)}}{2g_A \exp(\Delta E_A/kT)/N_V} \quad (2.11)$$

The fitting parameters for the incomplete ionization is given in Table 2.2.

Table 2.2: Fitting parameters for incomplete ionization of 4H-SiC.

Parameter	Unit	n-type	p-type
g	1	2	4
ΔE_0	eV	0.105	0.265
α	eV·cm	4.26×10^{-8}	3.60×10^{-8}

E. Mobility

The anisotropic mobility of 4H-SiC is due to anisotropic effective mass and

Table 2.3: Fitting parameters for mobility model of 4H-SiC.

Parameter	Unit	n-type	p-type
μ_{min}	cm^2/Vs	0	15.9
μ_{max}	cm^2/Vs	947	124
N_{ref}	cm^{-3}	1.97×10^{17}	1.76×10^{19}
α_d	1	-2.15	-2.15
γ	1	0.61	0.34

given by [20]

$$\mu_{n,\parallel} = 1.20\mu_{n,\perp}, \quad \mu_{p,\parallel} = 0.87\mu_{p,\perp} \quad (2.12)$$

where $\mu_{n(p),\parallel}$ and $\mu_{n(p),\perp}$ are electron (hole) mobility parallel and perpendicular to c-axis respectively. As illustrated in [10], the low field mobility is a function of total doping concentration, instead of ionized impurity concentration. The low field mobility perpendicular to c-axis is given by the Cauchy-Thomas correlation [21]

$$\mu_{\perp} = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + (N_{tot}/N_{ref})^{\gamma}} \left(\frac{T}{300} \right)^{\alpha_d} \quad (2.13)$$

where μ_{min} and μ_{max} are the minimum and maximum mobility respectively, α_d , N_{ref} and γ are the fitting parameters. For higher breakdown voltage, the SiC-based power devices are normally fabricated on (0001) wafer with 8° off-axis. Hence the moving direction of carriers for vertical devices is parallel to c-axis. The fitting parameters for the mobility model are given in Table 2.3.

2.2 SiC Power Devices and Modules

In terms of the device function in power converter, various power semiconductor devices can be categorized into two types: rectifier and switch, corresponding to diode and transistor respectively.

2.2.1 SiC Power Diodes

Various kinds of power diodes can be categorized into the following two types:

Schottky diode: As the unipolar device, it offers extremely high switching speed but suffers from high leakage current and large on-resistance.

PiN diode: As the bipolar device, it offers low on-resistance due to the conductivity modulation in the drift region, but suffers from low switching speed,

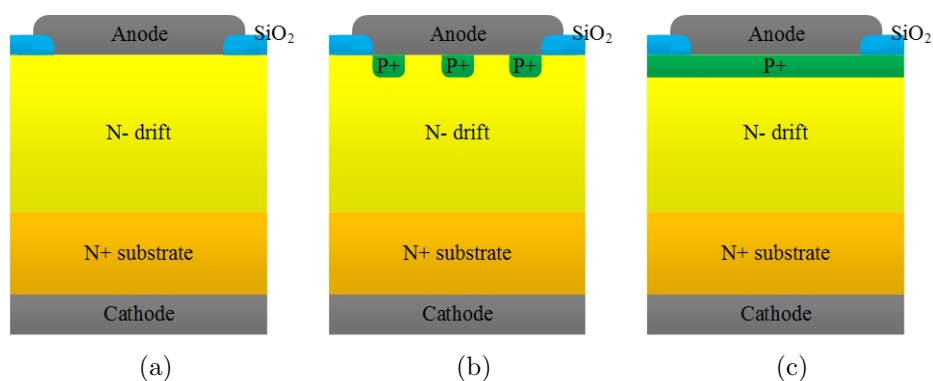


Figure 2.1: Cross-sections of SiC power diodes: (a) Schottky diode, (b) JBS diode, (c) PiN diode.

which is opposite to the Schottky diode.

As Figure 2.1(a) shows, the Schottky diode consists of a metal-semiconductor contact. The low barrier height of metal-Si contact (typically 0.7 eV) leads to a high leakage current. Hence, the Si Schottky diode is normally restricted to the application below 100 V [9]. With the emerging WBG material SiC, the Schottky diode may easily expand to the application above 1.2 kV. The first 4H-SiC Schottky diode was fabricated in 1995, with a breakdown voltage up to 1 kV, a specific on-resistance of $2 \text{ m}\Omega\cdot\text{cm}^2$ and a forward voltage drop of 1.06 V at a current density of $100 \text{ A}/\text{cm}^2$ [22]. A 3 kV 4H-SiC Schottky diode was demonstrated in [23] with a specific on-resistance of $34 \text{ m}\Omega\cdot\text{cm}^2$. To further reduce the electric field in the Schottky barrier and lower the leakage current during reverse blocking, the junction barrier Schottky (JBS) structure is inherited from Si counterpart, as Figure 2.1(b) shows. In [24], a JBS diode was fabricated in 4H-SiC with a blocking voltage up to 3.9 kV, and then a 10 kV JBS diode was reported in [25]. The first commercial SiC Schottky diode was released by Infineon in 2001. To date, various SiC Schottky diodes with 600~1700 V voltage rating and 1~50 A current rating are commercially available, supplied by several vendors including Cree, Rohm, Infineon, GeneSiC, STMicroelectronics and others.

On the other hand, the PiN diode consists of an intrinsic layer between the conventional PN junction, as Figure 2.1(c) shows. Under forward conduction, the holes injected into the intrinsic layer reduces the on-resistance, which is known as conductivity modulation. For the ultra-high ($> 10 \text{ kV}$) voltage application, SiC bipolar device is superior to unipolar device due to the existence of conductivity modulation. To date, SiC PiN diode has the largest blocking capability up to 15

kV [26,27], which is attractive for power distribution and transmission system.

2.2.2 SiC Power Transistors

Similarly, the power transistor can be categorized into unipolar and bipolar devices. Among the most commonly seen power transistors, the unipolar transistors mainly include MOSFET and JFET, while the bipolar transistors include BJT and IGBT.

The power MOSFET evolves from the traditional CMOS technology, but differs from that by incorporation of a low-doped and thick drift region into the drain structure, as Figure 2.2(a) shows. In addition, unlike the Si vertical double-diffusion MOSFET (VDMOS), the diffusion coefficient in SiC is extremely low and the ion implantation must be used instead. The first SiC MOSFET was fabricated using 6H-SiC in 1997, with a blocking voltage up to 760 V and a specific on-resistance of $66 \text{ m}\Omega\cdot\text{cm}^2$ when the gate-source voltage is 30 V [28]. Then a $27 \text{ m}\Omega\cdot\text{cm}^2$, 1.6 kV 4H-SiC MOSFET was reported in [29] with a channel mobility of $22 \text{ m}\Omega\cdot\text{cm}^2$. This low channel mobility is the result of high density of electron traps at SiC/SiO₂ interface. The gate oxide is normally annealed in nitric oxide (NO) ambient to reduce the interface traps [30]. A $1.8 \text{ m}\Omega\cdot\text{cm}^2$ SiC MOSFET with a blocking voltage of 660 V was reported in [31], and a channel mobility of $90 \text{ m}\Omega\cdot\text{cm}^2$ was achieved. Hence, the on-resistance of SiC MOSFET is no longer limited by the channel resistance currently. The first commercial SiC MOSFET was released by Cree in 2011. And Rohm further released the SiC MOSFET with trench structure instead of traditional planar structure. Nowadays, off-the-shelf

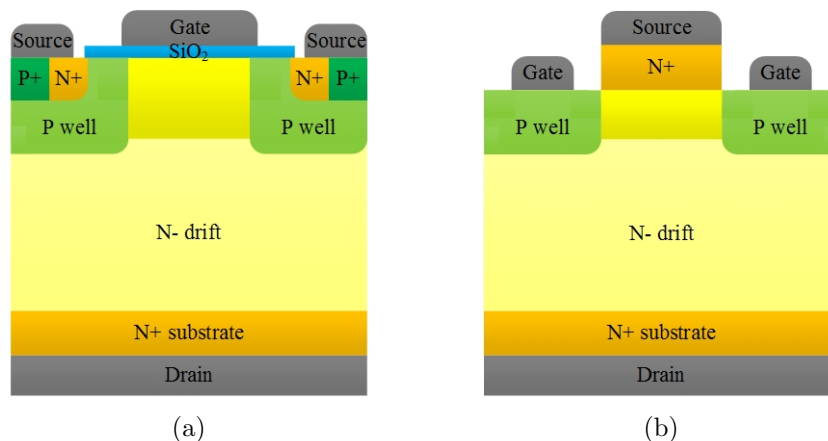


Figure 2.2: Cross-sections of SiC power transistors: (a) MOSFET, (b) JFET.

SiC MOSFETs with 400~1700 V voltage rating and 3~60 A current rating are commercially available and provided by Cree, Rohm, Microsemi, STMicroelectronics and others.

In the past, the poor SiC/SiO₂ interface quality motivated intensive investigations on the junction FET (JFET) structure. As Figure 2.2(b) shows, the JFET relies on two PN junctions to pinch off the channel during reverse blocking state. Due to the disappearance of MOS interface, the issue of low channel mobility in SiC MOSFET can be totally eliminated in SiC JFET [32]. However, the drawback of SiC JFET is that it is a normally-on device, leading to significant complexity in the gate driver design. The normally-on SiC JFET is mostly limited in applications like solid-state circuit breakers (SSCB), in which the system reliability can be increased without providing gate bias to maintain the rated conduction [33, 34]. To make the SiC JFET adaptable in the conventional power converter, the normally-off device is developed [35]. However, the threshold voltage is low and the on-resistance is high due to the pinched off region. At present, off-the-shelf SiC JFETs with 1.2 kV voltage rating and 26~35 A current rating are commercially available and provided by Infineon and others.

Among the bipolar devices, power BJT has the lowest on-resistance and highest current capability due to the presence of conductivity modulation. Due to the complexity of base driver design, it is rarely used in power converter. At present, the off-the-shelf SiC BJTs with 1.2~1.7 kV voltage rating and 3~100 A current rating are commercially available and provided by GeneSiC, Fairchild and others. The SiC IGBT is more competitive than SiC MOSFET in ultra-high voltage applications due to its lower conduction loss. The 13 kV n-channel SiC IGBT has been successfully fabricated by Cree [36]. The 15 kV SiC IGBT for the 60 Hz solid state transformer (SST) in smart grid application is under developing [37].

2.2.3 SiC Power Modules

To fully utilize the advantages of SiC power devices, the SiC power module is of interest for higher power density due to the small stray inductance and low thermal resistance. Two kinds of modules, hybrid Si/SiC and all-SiC, are reviewed herein.

The conventional Si IGBT power module normally employs the anti-parallel Si PiN diode. The high reverse recovery current of PiN diode leads to a high current overshoot during turn-on transition, and therefore a high switching loss is imposed on IGBT. Since the first release of commercial SiC Schottky diode,

it has become popular to replace the Si PiN diode in the hybrid IGBT power module due to the negligible reverse recovery current. It has been proven in [38–40] by merely replacing Si PiN diode with SiC Schottky diode, the converter loss can be reduced significantly. At present, off-the-shelf hybrid Si/SiC modules with 600~1700 V voltage rating and 20~1200 A current rating are commercially available and provided by Powerex, Semikron, Fuji Electric and others.

Recent advancement in SiC MOSFET has prompted the appearance of all-SiC power module. In 2009, the 1.2 kV and 100 A all-SiC power module was fabricated and characterized for DC-DC boost converter by U.S. Army Research Lab, with the 50 A SiC MOSFET developed by Cree [41, 42]. And the 400 A and 800 A modules with half bridge configuration are developed in the following works [43, 44]. The industry’s first reliable 1.2 kV and 100 A all-SiC power module was launched by Cree in 2013. At present, off-the-shelf all-SiC modules with 1200~1700 V voltage rating and 20~1200 A current rating are commercially available and provided by Cree, Rohm, Powerex, Vincotech and others.

2.3 Gate Driving Mechanism of Power MOSFET

The power BJT was developed to replace thyristor for higher switching frequency up to 50 kHz, with current capability of hundreds of amperes and blocking voltage of 600 V [45]. It differs from the small signal BJT by incorporation of a low-doped and thick drift region into the collector structure. The most attractive feature of power BJT is the relatively high current density due to the high level injection effect. However, the high level injection effect leads to degradation of current gain. As a current-controlled device, a continuous base current is required to maintain the power BJT’s steady on-state or off-state, which means a high power dissipation on base driver. Considering the low current gain, a high current capacity is required for the base driver. Hence, these factors add to the complexity in base driver design.

Due to the limited performance of power BJT, the power MOSFET was developed in the 1970s [45]. Instead of a continuous gate current, a gate bias voltage is required to maintain power MOSFET during on-state. The gate current only appears during switching transitions for charging and discharging of gate capacitor. The high input impedance of power MOSFET significantly simplifies the gate driver design. Currently, the power Si MOSFET is dominant in the market for application below 100 V. With the release of CoolMOS, the application field

of power Si MOSFET expands to 600 V. And the SiC MOSFET further expands beyond 1.2 kV application and starts to compete with the Si IGBT.

The high-speed switching SiC MOSFET introduces a new challenge to the high-speed gate driver design. In this section, the gate driver topology is reviewed firstly to choose the most suitable gate driver for this work. The switching mechanism of MOSFET is further discussed so as to optimize the gate driver design.

2.3.1 Gate Driver Topology: Voltage Source or Resonant

Various kinds of gate driver topologies can be categorized into the following two types [46]:

Voltage source gate driver (VSD): the gate capacitor is charged/discharged as in a RC network with all the power delivered from the voltage source. To date, the VSD is the dominant topology with a wide range of gate driver ICs off-the-shelf.

Resonant gate driver (RGD): the gate capacitor is charged/discharged as in a RLC network with the power delivered from the voltage source as well as the resonant inductor. RGD can be classified into the following two types. Type 1 RGD has a zero initial inductor current during switching transition [47], while type 2 RGD has a nonzero initial inductor current [48], hence it is also named as current source gate driver (CSD). Some literatures regard CSD as a third type of gate driver.

The conventional VSD can be modeled by an input capacitor C_{iss} in series with a gate resistor R_G and a pulse voltage source, as Figure 2.3 shows. The gate resistance consists of on-resistance of M_H or M_L of totem-pole stage, external gate resistance and internal gate resistance of power transistor. Even though the parasitic inductances from PCB trace as well as packaging will make the charging/discharging circuit behaves like an RLC second-order system, the gate voltage ringing is always unwanted and a large enough gate resistance is normally used to eliminate rings. Hence this circuit can be simplified as a first-order RC system. The power loss on VSD due to charging and discharging of gate capacitor is given by

$$P_{GD} = Q_G(V_{CC} - V_{EE})f_s \quad (2.14)$$

where Q_G is the gate charge of main transistor and f_s is the switching frequency. In each switching cycle, all the power loss is dissipated on the driver IC and gate

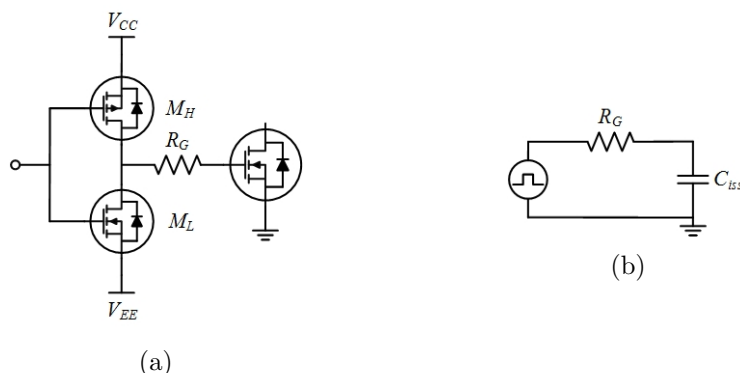


Figure 2.3: Voltage source gate driver: (a) typical schematic, (b) equivalent circuit.

resistor, the latter of which is the dominant part. As P_{GD} is independent of gate resistor, P_{GD} cannot be reduced with smaller gate resistance.

Three factors limit VSD in high frequency application beyond 1 MHz. Firstly, the conventional VSD is constrained by the power loss, which is proportional to switching frequency. Secondly, switching speed is limited due to the time-consuming charging/discharging of RC circuit. Last but not least, the parasitic inductor leads to gate voltage ringing and slows down the switching speed. In order to minimize the gate loop inductance, the VSD needs to be put as close as possible to the main transistor.

An advanced resonant gate driver topology is proposed based on VSD for lower gate driver loss and higher switching frequency above 1 MHz. Compared with VSD, a resonant inductor is introduced in RGD, hence the driver circuit turns into an RLC second-order system, as Figure 2.4 shows. During charging/discharging of C_{iss} , the energy from the power supply is partially stored in the inductor instead of dissipating all of it. If the damping resistor is eliminated, the driver circuit turns into an ideal LC resonant circuit with zero power loss. In addition, RGD is non-sensitive to the parasitic inductance due to the existence of a much larger external inductor. Unlike VSD, it is unnecessary to put RGD as

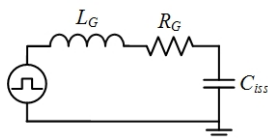


Figure 2.4: Equivalent circuit of resonant gate driver.

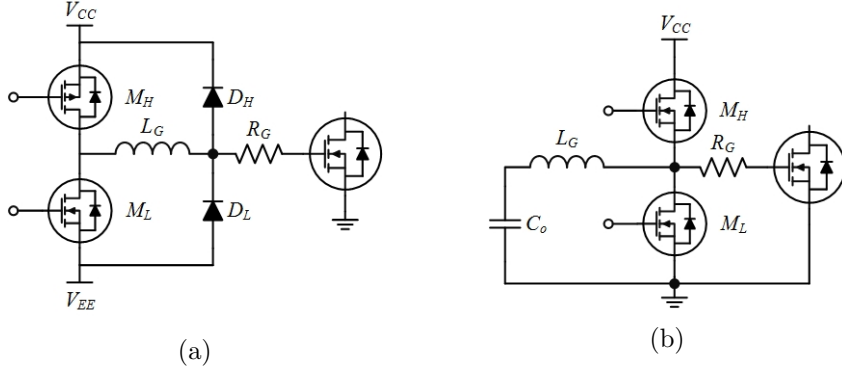


Figure 2.5: Schematics of resonant gate driver: (a) type 1, (b) type 2.

close as possible to the main transistor. Hence RGD becomes a possible candidate for high temperature application, as it can be put far from hash environment without degrading its performance.

RGD has been proposed with the appearance of resonant power converter. The basic idea for different RGD topologies is to control the resonant circuit so that C_{iss} is charged/discharged to the desired voltage. As the inductor current cannot change abruptly, freewheeling circuit needs to be provided after the inductor is disconnected from C_{iss} . Lots of work has been done on RGD topologies, and two classical RGD topologies of type 1 and type 2 are briefly introduced.

The proposed RGD in [47] consists of a totem-pole circuit inherited from conventional VSD, an inductor and two diodes, which clamps output voltage and freewheels the inductor current, as Figure 2.5(a) shows. During turn-on transition, an inverse trigger pulse is applied on M_H , then the charging current flows through M_H , L_G , R_G and starts to charge C_{iss} . After C_{iss} is charged to V_{CC} , D_H is forward biased and V_{GS} is clamped. Then M_H is turned off and the inductor current flows through the body diode of M_L , L_G , D_H and then back to the power supply. The turn-off process behaves in a similar way. The output voltage is clamped between V_{EE} and V_{CC} . It is also possible to apply a continuous PWM signal on the totem-pole circuit. Although power loss will increase as the inductor is always conducting, a simpler control strategy can be achieved. In addition, the discrete totem-pole circuit can be replaced by driver IC for higher switching speed [49].

The proposed RGD in [48] can also be regarded as CSD, as Figure 2.5(b) shows. The switching transition between on and off is controlled by M_H and M_L with a dead time zone. The inductor provides a current pulse to charge/discharge

C_{iss} . A large enough capacitor C_o is used to remove the DC voltage component from the inductor. And C_o can also be directly connected with power supply [50]. The switching process is illustrated as follows. After C_{iss} is completely charged to V_{CC} by the inductor current source, M_H is turned on and then the inductor current flows back to the power supply via the body diode of M_H . This current decreases linearly to a negative peak current until M_H is turned off. After C_{iss} is completely discharged, M_L is turned on and then the inductor current flows to C_o via the body diode of M_L . This current will increase linearly to a positive peak current until M_L is turned off.

2.3.2 Switching Mechanism of Power MOSFET

The switching mechanism of power MOSFET is discussed herein for a better understanding of the procedure to design and optimize gate driver. The typical switching test circuit for MOSFET is shown in Figure 2.6 [51]. And the switching waveforms are shown in Figure 2.7.

A. Turn-on Transition

Subinterval $t_0 \sim t_1$ (turn-on delay time $t_{d,on}$): The input capacitance including C_{GS} and C_{GD} (at $v_{DS} = V_{DC}$) starts to get charged via the gate resistor R_G . And v_{GS} rises exponentially with a time constant $\tau_1 = R_G[C_{GS} + C_{GD}(V_{DC})]$, as Eq.(2.15) illustrates. This time interval ends until v_{GS} reaches the threshold voltage V_{th} . Since v_{GS} is below V_{th} , no drain current flows via MOSFET and v_{DS} remains at V_{DC} . The expressions of v_{GS} , i_G , and $t_{d,on}$ are given by

$$v_{GS}(t) = V_G \left(1 - e^{-t/\tau_1}\right) \quad (2.15)$$

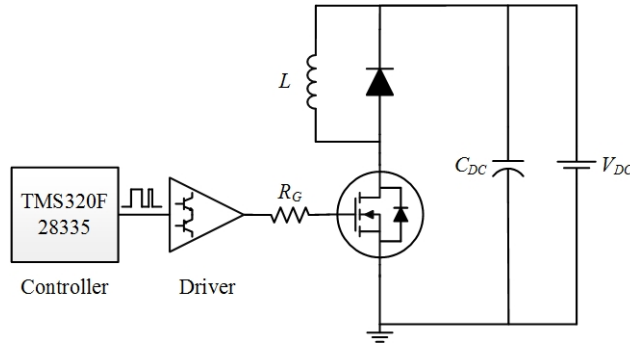


Figure 2.6: Typical switching test circuit for MOSFET and freewheeling diode.

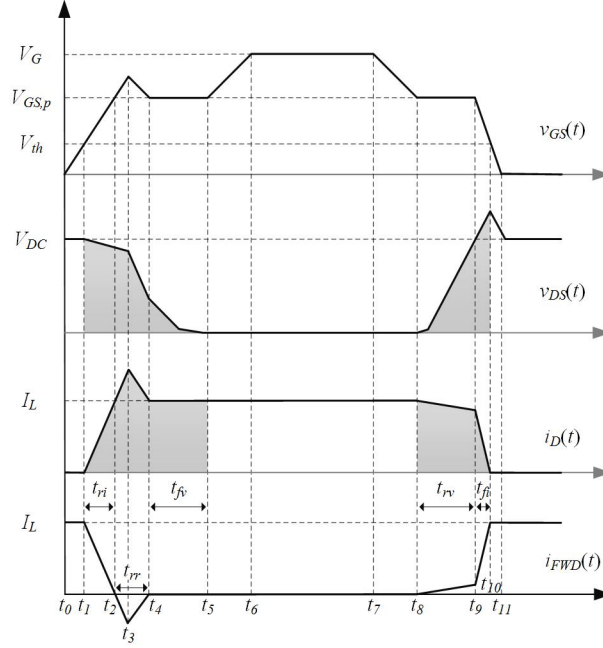


Figure 2.7: Switching waveforms: gate-source voltage, drain-source voltage, drain current, freewheeling diode current.

$$i_G(t) = \frac{V_G - v_{GS}(t)}{R_G} = \frac{V_G}{R_G} e^{-t/\tau_1} \quad (2.16)$$

$$t_{d,on} = \tau_1 \ln \left(\frac{V_G}{V_G - V_{th}} \right) \quad (2.17)$$

Subinterval $t_1 \sim t_2$ (current rise time t_{ri}): The input capacitance continues to be charged and v_{GS} rises exponentially beyond V_{th} with the time constant τ_1 . Since v_{GS} is above V_{th} , i_D starts to rise until it reaches the load current I_L , at which time v_{GS} reaches Miller plateau voltage $V_{GS,p}$

$$i_D(t) = g_m [v_{GS}(t) - V_{th}] \quad (2.18)$$

$$V_{GS,p} = \frac{I_L}{g_m} + V_{th} \quad (2.19)$$

where g_m is the transconductance. And the slew rate of i_D is given by

$$\frac{di_D(t)}{dt} = \frac{g_m V_G}{\tau_1} e^{-t/\tau_1} \quad (2.20)$$

Hence, di/dt at turn-on is dominated by the gate driver, including driving

voltage and gate resistance. And it is independent of load current. Combing Eq.(2.15)~(2.19), the current rise time t_{ri} can be derived

$$t_{ri} = \tau_1 \ln \left(\frac{V_G - V_{th}}{V_G - V_{GS,p}} \right) \quad (2.21)$$

During this time, v_{DS} should remain constant theoretically since the FWD cannot block reverser voltage before all the inductor current is transferred to MOSFET. However, in real situation v_{DS} will be reduced by the amount of $L_S di/dt$ due to the effect of stray inductance.

Subinterval $t_2 \sim t_4$ (reverse recovery time t_{rr}): C_{GS} ceases to be charged while the charging current to C_{GD} continues. The MOSFET starts to carry the full inductor current and the diode enters the reverse recovery process. Due to the reverse recovery current I_{rr} , i_D rises from I_L to $I_L + I_{rr}$, and v_{GS} rises beyond $V_{GS,p}$ according to Eq.(2.15). When the diode current starts to recover towards 0 at t_3 , it starts to enter reverse blocking mode, and v_{DS} starts to fall. The reverse recovery process can be described by

$$I_{rr} = \frac{di}{dt} \frac{t_{rr}}{S + 1} \quad (2.22)$$

$$Q_{rr} = I_{rr} t_{rr} / 2 = C_d V_{DC} \quad (2.23)$$

where di/dt is given by I_L/t_{ri} , S is the snappiness factor and $S < 1$ for most diodes [51], Q_{rr} is the reverse recovery charge, and C_d is the depletion capacitor of Schottky diode. Combing Eq.(2.22) and (2.23), the reverse recovery time can be derived

$$t_{rr} = \sqrt{\frac{2(S+1)C_d V_{DC}}{di/dt}} < 2\sqrt{\frac{C_d V_{DC}}{di/dt}} \quad (2.24)$$

Subinterval $t_4 \sim t_5$ (voltage fall time t_{fv}): With the continuing charging current to C_{GD} , v_{DS} continues to fall towards the on-state voltage drop of MOSFET. As $i_D = I_L$, v_{GS} is temporarily clamped at $V_{GS,p}$, and the gate charging current is given by

$$I_{G,p} = \frac{V_G - V_{GS,p}}{R_G} \quad (2.25)$$

The slew rate of v_{DS} can be derived

$$\frac{dv_{DS}(t)}{dt} = \frac{d[v_{DG}(t) + v_{GS}(t)]}{dt} = -\frac{dv_{GD}(t)}{dt} = -\frac{I_{G,p}}{C_{GD}(v_{DS})} \quad (2.26)$$

Hence, dv/dt is proportional to the gate current, while inversely proportional to C_{GD} . As C_{GD} is bias-dependent, dv/dt under high bias is much larger than that under low bias. Substituting Eq.(2.19) and (2.25) into Eq.(2.26),

$$\frac{dv_{DS}(t)}{dt} = -\frac{V_G - (V_{th} + I_L/g_m)}{R_G C_{GD}(v_{DS})} \quad (2.27)$$

It can be further conclude that dv/dt is strongly dominated by the gate driving voltage. Due to the low transconductance of SiC MOSFET, using of higher driving voltage is even more important. In addition, dv/dt will slightly decrease with I_L increasing, which means a longer voltage fall time.

Subinterval $t_5 \sim t_6$: After the MOSFET enters the full conduction mode, the input capacitance including C_{GS} and C_{GD} (at $v_{DS} = V_{DS,on}$) is further charged via R_G . And v_{GS} rises exponentially with a time constant $\tau_2 = R_G[C_{GS} + C_{GD}(V_{DS,on})]$ until it reaches the positive power supply voltage of gate driver. As this time interval has no substantive effect on switching loss, it is not analyzed in details.

B. Turn-off Transition

The turn-off transition analysis can be performed in a similar way to the turn-on transition, but in an inverse sequence.

Subinterval $t_7 \sim t_8$ (turn-off delay time $t_{d,off}$): The input capacitance starts to get discharged via R_G , and v_{GS} falls exponentially with a time constant τ_2 . Within this time, there is no change for both v_{DS} and i_D until v_{GS} reaches $V_{GS,p}$.

Subinterval $t_8 \sim t_9$ (voltage rise time t_{rv}): C_{GD} continues to be discharged while the charge on C_{GS} maintains, and v_{DS} rises towards V_{DC} . As $i_D = I_L$, v_{GS} is temporarily clamped at $V_{GS,p}$, and the gate discharging current is given by $I_{G,p} = V_{GS,p}/R_G$.

Subinterval $t_9 \sim t_{10}$ (current fall time t_{fi}): The input capacitance starts to get discharged again, v_{GS} falls exponentially towards V_{th} with a time constant τ_1 and i_D falls towards 0. In addition, due to the stray inductance, v_{DS} will have an overshoot voltage of $L_S di/dt$ during the current fall time. During the turn-off transition, both dv/dt and di/dt are strongly influenced by I_L . It is because the turn-off speed of MOSFET is dominated by the turn-on speed of FWD. A smaller load current leads to a slower charging process of junction capacitor of FWD.

Subinterval $t_{10} \sim t_{11}$: The input capacitance is further discharged, and v_{GS} continues to fall exponentially towards 0 with a time constant τ_1 .

2.4 Protection Circuit Design

The high-speed switching of SiC MOSFET also introduces a new challenge to the protection circuit design. The high di/dt at turn-on means the current may rise more rapidly when subjected to a short-circuit fault, which requires a short-circuit protection scheme with faster response. In addition, the high di/dt at turn-off introduces a more serious voltage overshoot of Ldi/dt , which may lead to the over-voltage issue, especially at the abrupt turn-off of short-circuit current.

2.4.1 Short-circuit Protection

Due to the different physical properties of SiC compared with that of Si counterpart, application issues like the short-circuit or over-current protection schemes are incompletely investigated at this time. However, the power converters can be easily subjected to short-circuit fault conditions. From the controller side, the controller misfiring or improper dead time may simultaneously turn on both high side (HS) and low side (LS) transistors in a half-bridge configuration and short the DC-bus. From the converter itself, the destruction of transistor or diode in the converter may lead to arm shoot-through. From the load end (e.g. motor), a wiring misconnection or dielectric breakdown may short the output terminals of converter. Generally, the fault conditions can be categorized into the following two types: hard switching fault (HSF) and fault under load (FUL) [52]. HSF is defined as the short-circuit fault while the transistor is in the turn-on transition. As Figure 2.8(a) shows, the transistor is turned on with the DC bus voltage directly supported across the device. FUL is defined as the short-circuit fault while the transistor is in the steady on-state. As Figure 2.8(b) shows, the LS transis-

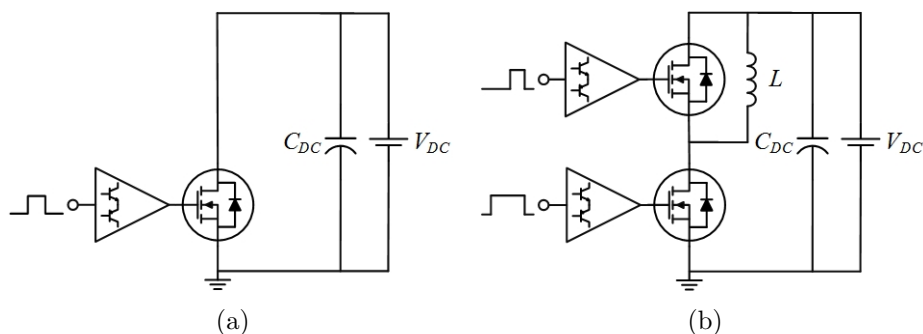


Figure 2.8: Short-circuit fault conditions: (a) HSF and (b) FUL.

tor is initially in normal on-state and then subjected to FUL by turning on the complementary HS transistor, hence resulting in arm shoot-through.

The device manufacturers normally specify a short-circuit withstand capability for power transistor in terms of time, which is from the start of short-circuit current until the transistor is completely destroyed. For Si IGBT, the typical short-circuit withstand capability is around 10 μ s. SiC MOSFET tends to have smaller short-circuit withstand capability due to its smaller die size and higher current density [53]. Due to the excessive power dissipation during short-circuit conditions, the junction temperature of die may easily exceed the limit and lead to a permanent thermal runaway. Even the transistor survives during short-circuit fault, the abrupt turn-off may lead to a new problem of voltage overshoot.

The short-circuit protection issue has received lots of attention in Si IGBT protection design during the last two decades. SiC MOSFET is regarded as an attractive replacement of Si IGBT for applications ranging from 1.2~10 kV. However, very few works can be found on the short-circuit protection scheme for the newly emerging SiC MOSFET. Just recently, there is one work on short-circuit protection for SiC MOSFET [53]. Due to the unique characteristics of SiC MOSFET, the traditional short-circuit protection scheme for Si IGBT cannot be directly used for SiC MOSFET. The recommended gate-source voltage of SiC MOSFET is typically 20 V [54] to mitigate the effect of low transconductance, which is attributed to the high density of electron traps at SiC/SiO₂ interface. However, a higher gate voltage tends to degrade the short-circuit withstand capability due to the increased short-circuit current. In addition, due to the smaller die size and higher current density of SiC MOSFET, its junction capacitance is smaller than that of Si IGBT. Hence to maximize the advantages of SiC MOSFET, it is normally driven at high-speed, which leads to high dv/dt and di/dt . The high switching noise introduces a new challenge for the high-speed protection scheme design. The conventional protection schemes include detection of collector/drain current [52, 55], collector-emitter/drain-source voltage (or desaturation technique) [56–59], current rising rate (di/dt) [53, 60, 61] and gate voltage [62–66], as Figure 2.9 shows.

The collector/drain current detection scheme is the most straightforward solution with a current sensor like the shunt resistor or current transformer [52]. The shunt resistor introduces extra parasitic inductance into the main power circuit. In addition, as the main current is flowing through the shunt resistor, the conduction loss on the current-sensing resistor is considerable, which is unacceptable for

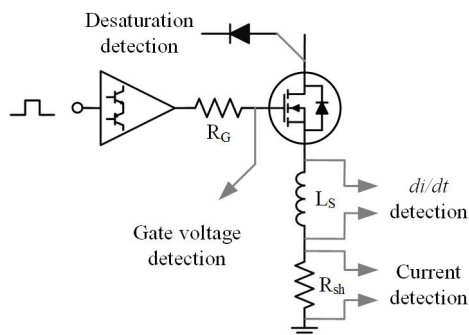


Figure 2.9: Short-circuit protection schemes.

applications where high efficiency is the main aim. The current transformer can avoid such drawbacks of shunt resistor since it is totally isolated from the main power circuit. However, the limitation of bandwidth makes it hard to capture the fast current rising rate. An integrated scaled-down current-sensing transistor parallel with the main transistor provides the best solution based on collector/drain current detection scheme [55]. However, it requires a special design on the device level.

The desaturation technique is the most widely used solution with a voltage-sensing diode connected with the collector/drain terminal. And lots of gate driver ICs with integration of desaturation detection block are off-the-shelf [56]. It will not insert any resistive or inductive component into the main power circuit, which is the most attractive benefit. However, a blanking time around $1\sim 5\ \mu\text{s}$ is required during turn-on transition to wait until V_{CE} or V_{DS} falls to the predefined threshold voltage, so as to avoid fault triggering. Hence the fault current will rise to a huge value and lead to excessive power dissipation.

The di/dt detection makes use of the stray inductance between the Kelvin emitter/source and power emitter/source by detecting the Ldi/dt voltage drop. The gate voltage detection makes use of the difference of gate voltage under fault and normal conditions, since the abnormal collector/drain voltage will feedback to the gate side via Miller capacitor. Similar to desaturation technique, no extra component is inserted into the main power circuit. And due to elimination of blanking time, both of them promise faster response time. However, the former requires extraction of the small inductance by measurement, which adds to the design complexity. And the latter is very sensitive to the gate voltage noise, which is induced by the parasitic inductance of gate driver loop.

2.4.2 Over-voltage Protection

The over-voltage issue mainly originates from the overshoot voltage of Ldi/dt during turn-off transition, especially in the situation of fast turn-off of over-current. Hence, considering the amount of overshoot voltage, selection of power devices with higher rating than the DC-link voltage becomes a normal procedure, which tends to increase the system cost. The simplest strategy to mitigate the voltage overshoot is to use a snubber circuit [51]. However, the bulky snubber circuit increases the power loss, weight, volume and cost of system.

The MOS-gate-controlled switches including power MOSFET and IGBT have prompted development of snubberless smart gate driver. The active clamp connected between the gate-drain terminals of MOSFET can effectively mitigate voltage overshoot [67], as Figure 2.10 shows. Several transient voltage suppression (TVS) diodes are connected in series to meet the clamping voltage. And the Schottky diode is to block the current flowing from gate to drain. When there is a voltage spike exceeding the rated voltage of TVS diode, its impedance will decrease sharply within several picoseconds and V_{DS} is clamped at a safe value. The current from TVS diode flows into the switch to charge the gate capacitor and therefore V_{GS} rises. Hence the turn-off speed is slowed down and voltage overshoot is suppressed.

A more advanced strategy is using active gate voltage control (AGVC) to actively control the turn-off speed so as to mitigate voltage overshoot. A novel gate driver IC with two-level turn-off was proposed in [68], in which an intermediate voltage is introduced below the normal positive gate voltage. An improved AGVC with three-step turn-off was proposed in [69], which differs from the two-level strategy by introducing another gate charge extraction time. Hence, the turn-off delay time ($t_6 \sim t_7$ shown in Figure 2.7) is shortened. The AGVC is especially attractive when the transistor is subjected to over-current or short-circuit conditions. However, the AGVC will operate during every switching cycle, no matter whether the over-current or short-circuit happens or not. It resolves the voltage overshoot

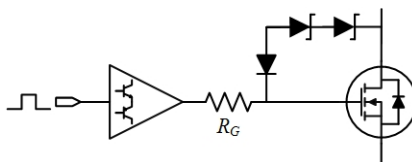


Figure 2.10: Schematic of active clamp.

issue at the expense of slowing down the turn-off speed, hence the switching loss increases. Even if the AGVC is adopted in gate driver, the implementation of an active clamp circuit is still advisable as an additional safety consideration [67].

2.5 Power Electronics Packaging Technology

The ever increasing demand for high power density has motivated the modularization and integration of power electronic systems. Hence, power electronics packaging technology has become a more and more crucial issue for modern power converter design. Compared with the discrete power devices, the power module has lower stray inductance, which makes the high-speed switching and low switching loss practical. In addition, it also facilitates the thermal design due to the use of high thermal conductive substrate. To maximize the power density of the newly emerging SiC power converter, the packaging stray inductance needs to be further reduced and an improved thermal design is required.

2.5.1 Low Stray Inductance Packaging Technology

The commercial Si IGBT power module has a typical loop stray inductance of 15~50 nH, which is measured from the positive to negative power terminals [70]. The stray inductance of the 1st generation commercial SiC half bridge module CAS100H12AM1 from Cree is as high as 20 nH [71]. The high stray inductance leads to voltage overshoot at turn-off and EMI issues including voltage and current oscillations. It has become the bottleneck for high-speed switching of SiC power module.

Much work has been carried out to reduce the stray inductance of SiC power module. In [72, 73], the wirebonding layout was rearranged and optimized so as to minimize the current commutation loop, and a loop stray inductance around 10 nH was obtained. A more promising and advanced packaging structure was proposed

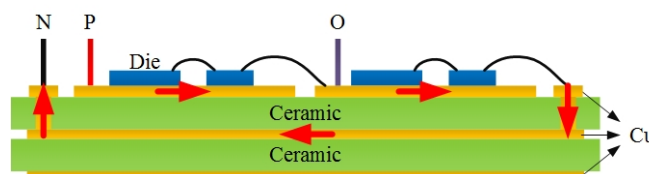


Figure 2.11: Cross-section of packaging structure of SiC power module with triple-conductor and double-ceramic layered substrate.

by [70, 74], in which a compact phase-leg SiC power module with 4.5 nH stray inductance was demonstrated, as Figure 2.11 shows. Instead of the conventional direct bond copper (DBC) structure, it adopts a triple-conductor and double-ceramic layered substrate. The bottom pads of power devices are soldered on the top conductor and the top pads are connected by wirebonding. The middle conductor plays a key role in reducing the stray inductance. It is because the current directions between the top and middle conductors are opposite, resulting in a strong mutual inductance. The drawback of this five-layer substrate is the potential to increase the thermal resistance.

2.5.2 3D Packaging Technology

The wirebonding technology, which was initially inherited from the conventional IC packaging, has also been widely used in power electronics packaging due to the low-cost, maturity and simplicity. The thick aluminum wires (0.25~0.5 mm) inside the power module will be subjected to high current and thermal cycles. Hence, the wirebonding becomes the one of the weakest points of the whole module. Currently, one of the major failure mechanism in IGBT module is the wirebonding lift-off, which is due to the coefficient of thermal expansion (CTE) mismatch between aluminum wires and dies [75]. In addition, the high parasitic inductance and proximity effect result in non-uniform current distribution among the wires and parallel dies [76]. As a consequence, these reliability issues have prompted the elimination of wirebonding in power electronic packaging.

The flip-chip technology is widely used in IC packaging to replace wirebonding by using the solder bump interconnection, which can provide the high current capability required in power electronics packaging. In addition, the low-profile solder bump only introduces negligible stray inductance. The 3D packaging technology with flip-chip was firstly applied to power electronics packaging in [76, 77], as Figure 2.12 shows. The power devices are sandwiched between the DBC substrate

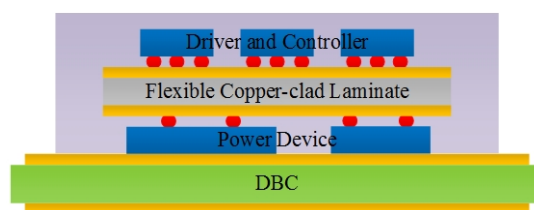


Figure 2.12: Cross section of 3D packaging with flip-chip technology.

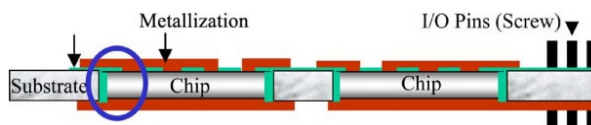


Figure 2.13: Cross section of embedded power module.

and flexible copper-clad laminate. And the gate driver and controller ICs can be built on top of the flex circuitry. Then a similar work was conducted in [78]. With the 3D packaging technology, the concept of integrated power electronics module (IPEM) becomes practical to further increase the power density.

The use of flip-chip technology requires the top pads of power devices to be solderable. However, the surface metallization of current SiC power devices is initially designed for the conventional wirebonding technology. For example, only the backside (drain) metallization of the commercial SiC MOSFET die CPM2-1200-0080B is made of the solderable material Ni/Ag, while the frontside (source and gate) metallization is just aluminum, which can be easily bonded with the aluminum wires [79]. Hence, the solderable top pads are unavailable without special treatment like silver sputtering. As a compromise of wirebonding and 3D flip-chip technologies, a hybrid packaging structure was proposed in [80, 81]. It keeps the high power density advantage of 3D packaging technology. In addition, it also adopts wirebonding to simplify fabrication.

The embedded power (EP) is another promising solution for 3D power electronics packaging technology [82, 83]. As Figure 2.13 shows, multiple power devices are buried in the ceramic frame and covered by the dielectric layer with the vias on top of electrode pads. Then a deposition of planar metallization pattern is followed to form the interconnection. The ceramic frame serves as the substrate as well as extra thermal path due to the high thermal conductivity.

The flexible circuitry shown in Figure 2.12 can be replaced by another DBC substrate. Hence, the power devices become sandwiched by two thermal conductive DBC substrates, which also make double-sided cooling practical to ultimately improve the cooling efficiency [84, 85].

2.5.3 Integrated Micro-channel Cooling Technology

The further increasing high power density may require system integration of heat sink inside the IPEM, which introduces a tremendous challenge to the thermal design. The conventional cooling systems like natural convection and forced con-

vection become difficult to meet the rigorous demands. In addition, the bulky heat sink becomes a limiting factor for the power density. A contradictory requirement for the cooling system is made with small size and high cooling efficiency.

Some early works on the integrated power electronics packaging and cooling include: double side cooling with heat pipes [86] or liquid impingement cooling [84], replacement of thermal interface material (TIM) with solder between DBC and heat sink [87]. Although these works are capable of dissipating heat flux of 100 W/cm^2 , there is still enough room to further improve the cooling efficiency. The past few decades have witnessed extensive investigations on micro-channel heat sink (MCHS) since the first fabrication in 1981, which cooled a heat flux of 790 W/cm^2 with a temperature rise of $71 \text{ }^\circ\text{C}$ [88]. This landmark result has activated great interests in application of MCHS for power electronics cooling. In [89], a new packaging technique was developed by mounting the very large-scale integrated (VLSI) chips on the multi-layered alumina substrate with micro-channels ($400 \mu\text{m} \times 800 \mu\text{m}$) fabricated inside. The allowable power dissipation was 400 W at a flow rate of 1.0 L/min . In [90], the $400 \mu\text{m} \times 1000 \mu\text{m}$ micro-channels were integrated in the FR4 printed circuit board (PCB). Heat removal capability of this cooling system was 20 W per channel. In [91], the application of MCHS for flip chip ball grid array packages (FCBGA) was investigated, in which the Al-based MCHS ($2 \text{ mm} \times 0.21 \text{ mm}$) was assembled to the chip by TIM.

The DBC with a sandwich structure of Cu-ceramic-Cu plays a key role in the modularization and integration of power electronic systems. It serves as the mechanical support, electrical isolation and heat removal path for the power module. As the thick top Cu-layer allows large current capability, circuit diagram can be patterned in this layer. Currently, Al_2O_3 is most widely used as the ceramic material of DBC due to the low cost and mature mass production. However, due to the low thermal conductivity, Al_2O_3 is limited to low and middle power applications. AlN (aluminum nitride) has been regarded as the most promising candidate for the ceramic material due to high thermal conductivity and high mechanical strength. Besides, it is especially attractive for application in SiC power electronics packaging, as its CTE is very close to that of SiC.

In the early works, the MCHS was soldered to DBC [92], or fabricated in the back Cu-layer of DBC [93,94], or fabricated in the AlN-layer of DBC [95,96]. With integration of MCHS in DBC, the cooling performance is ultimately improved by minimizing heat conduction path and eliminating TIM. In addition, the ultra-light weight and compact volume make it attractive for aerospace applications.

2.6 SiC High Power Density Converter

The SiC-based HPDC becomes more and more attractive in the applications with space restriction. In addition, implementation of SiC power converter allows a simpler topology with similar efficiency and power density compared with Si power converter [97], which also tends to reduce the complexity of controller design. Hence, most of the early works focused on the basic converter topologies.

A summary of the early works on SiC HPDC is given in Table 2.4. The power density can be measured by power per volume and power per weight. In this work, the volumetric power density is adopted for comparison. And a maximum power density of 50 kW/L was achieved in [98], which consists of SiC power module, gate driver, DC-link capacitor and heat sink, as Figure 2.14 shows. However, these values were evaluated under different conditions. For example, for the same topology of three-phase two-level voltage source inverter, an EMI filter was also included in [99–101].

These early works mainly focused on telecommunication and automotive applications, like the high voltage DC (HVDC) distribution system in data server [102, 103], motor drive inverter [98–101, 104–107] and on-board battery charger [110, 111] in HEV. However, research in application of SiC HPDC in MEA is still lacked. Since the automotive application has the most similar situations as aerospace, like the high temperature environment and limited space, the automotive application is reviewed in the following section.

The typical diagram of automotive power converter is shown in Figure 2.15. It

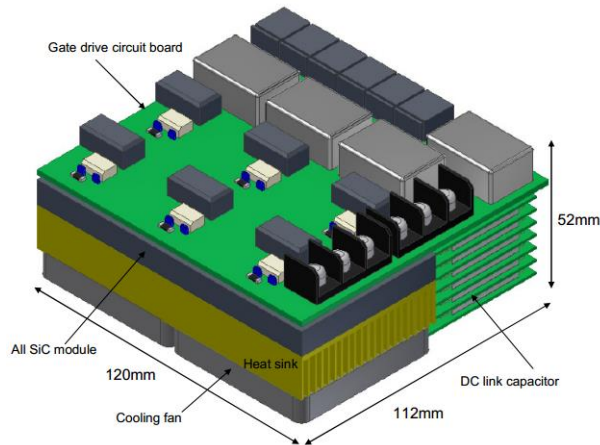


Figure 2.14: Prototype of high power density three-phase inverter.

Table 2.4: Summary of early works on SiC high power density converter.

Reference	Component	Topology	Power (kW)	Density (kW/L)
[102,103]	Si CoolMOS, SiC Schottky diode	Isolated full bridge DC/DC converter	5	10
[98]	SiC MOSFET, SiC Schottky diode	3-phase 2-level inverter	30	50
[104]	SiC JFET, SiC Schottky diode	3-phase 2-level inverter	20	25
[105]	SiC JFET, SiC Schottky diode	3-phase 2-level inverter	10	20
[99]	SiC JFET, SiC Schottky diode	3-phase 2-level inverter	10	27
[106]	SiC JFET, SiC Schottky diode	3-phase 2-level inverter	15	40
[100,101]	SiC JFET, SiC Schottky diode	3-phase 2-level inverter	30	8.35
[107]	SiC JFET, SiC Schottky diode	3-phase 2-level inverter	10	8
[108]	SiC JFET	3-phase 2-level rectifier with interleaving	15	6.3
[109]	SiC JFET, SiC Schottky diode	3-level Vienna rectifier (1st stage) and 3-phase 2-level inverter (2nd stage)	10	3
[110]	SiC MOSFET, SiC Schottky diode	Bridgeless boost rectifier	6	11.1
[111]	SiC MOSFET, SiC Schottky diode	Bridgeless boost rectifier (1st stage) and isolated full-bridge DC/DC converter (2nd stage)	6.1	5
[112]	SiC MOSFET, SiC Schottky diode	Indirect matrix converter	15	13
[113]	SiC JFET	Matrix converter	20	20
[114]	SiC MOSFET, SiC Schottky diode	Bidirectional DC/DC converter with interleaving	60	20

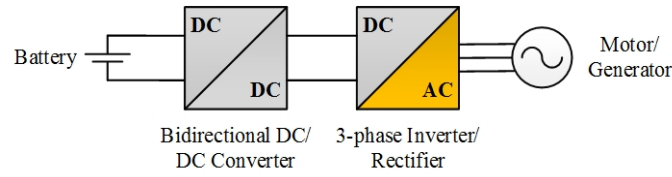


Figure 2.15: Diagram of automotive power converter.

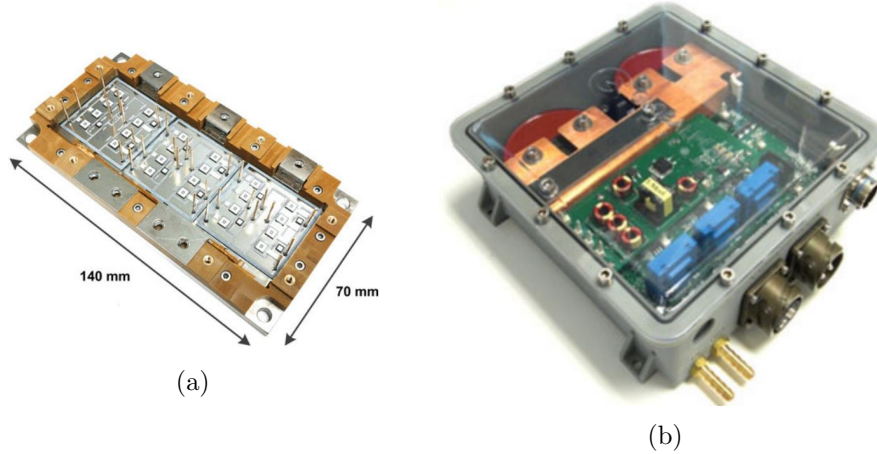


Figure 2.16: (a) Six-pack SiC JFET-based power module; (b) Prototype of high power density three-phase inverter.

consists of a battery bank, a bidirectional DC/DC converter and a three-phase inverter/rectifier, which is connected to the motor/generator. And the bidirectional DC/DC converter acts as a boost converter when the battery is discharging, while as a buck converter when the battery is charging.

The propulsion system of HEV is a combination of internal combustion engines (ICE) and electrical motor. The power converter is directly subjected to the high temperature environment resulted from ICE. Although two separate cooling systems are adopted in current HEV, the solution of single cooling system is promising to reduce the cost, weight and system complexity. Thus, the HPDC prototypes that are capable of operating at high temperature were developed in several early works. In [100, 101], a fully integrated six-pack power module with SiC JFET was developed, as Figure 2.16 shows. And the inverter prototype was successfully tested with liquid coolant temperature up to 95 °C. In [107], an automotive inverter system with discrete SiC JFET was developed. It was directly cooled with ambient air of up to 120 °C to avoid the complex and costly liquid cooling system, and active cooling was adopted for the control electronics.

2.7 Power Converter Requirements in More Electric Aircraft

Due to the lack of research in SiC HPDC for MEA application, the requirements for MEA need to be discussed and defined firstly before converter design.

Conventionally, the majority of civil aircraft uses an AC power system with a line-to-neutral voltage of 115 V and a line frequency of 400 Hz [115], as Figure 2.17 shows. In this architecture, the integrated drive generator (IDG) is connected with the main engine to adjust the variable speed of engine to a constant speed by mechanical means. Hence, it provides a constant voltage constant frequency (CVCF) AC power to electrical bus of aircraft. This electrical power is mainly used by the fans that circulating air in aircraft, hotel, lighting and galley loads. The 28 V DC power is converted from the 115 V/ 400 Hz AC power by the transformer rectifier unit (TRU). And it is mainly used by the avionics electronics like microprocessors and other ICs. The APU acts as an additional power source when the aircraft is on the ground or in certain emergency situations. Besides, the ram air turbine (RAT) is used to provide electrical and hydraulic power in

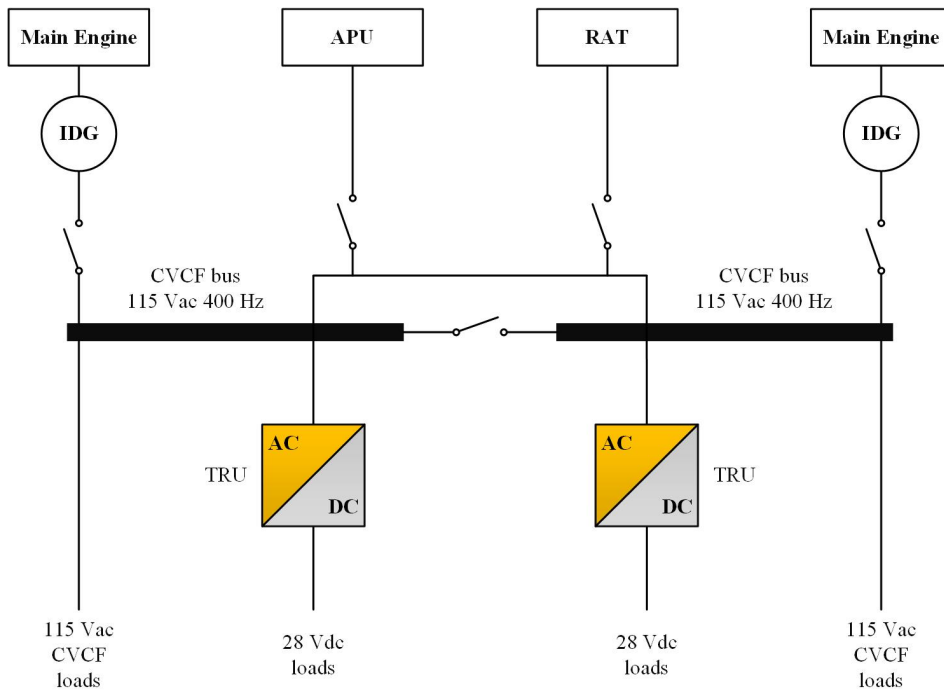


Figure 2.17: Architecture of power distribution system in traditional aircraft.

emergency situations.

Nowadays, MEA like Boeing 787 has moved from the 115 V/ 400 Hz AC system to a combined 115 V, 235 V AC system with a variable frequency of 360~800 Hz, as Figure 2.18 shows. And the 235 V AC power is further rectified to a ± 270 V DC power by TRU. The traditional 28 V DC system is also included. In this new architecture, the S/G is adopted and directly connected to the main engine gear box instead of IDG, which produces a variable frequency proportional to the engine speed. As a consequence, it provides a constant voltage variable frequency (CVVVF) AC power to electrical bus of aircraft. Elimination of conventional IDG in MEA improves reliability and also reduces maintenance cost. However, the traditional AC loads in aircraft still require a constant 400 Hz AC power. The back-to-back AC-AC power converter has to be used to convert the variable frequency to a constant frequency. This back-to-back converter shown in Figure 1.3 is one of the key technologies to further motivate the electrification of MEA.

For the power distribution system in next generation MEA shown in Figure 2.19, insted of the standard DC distribution system of ± 270 V in current MEA, a new ± 375 V DC system is adopted, which is regarded as the potential standard

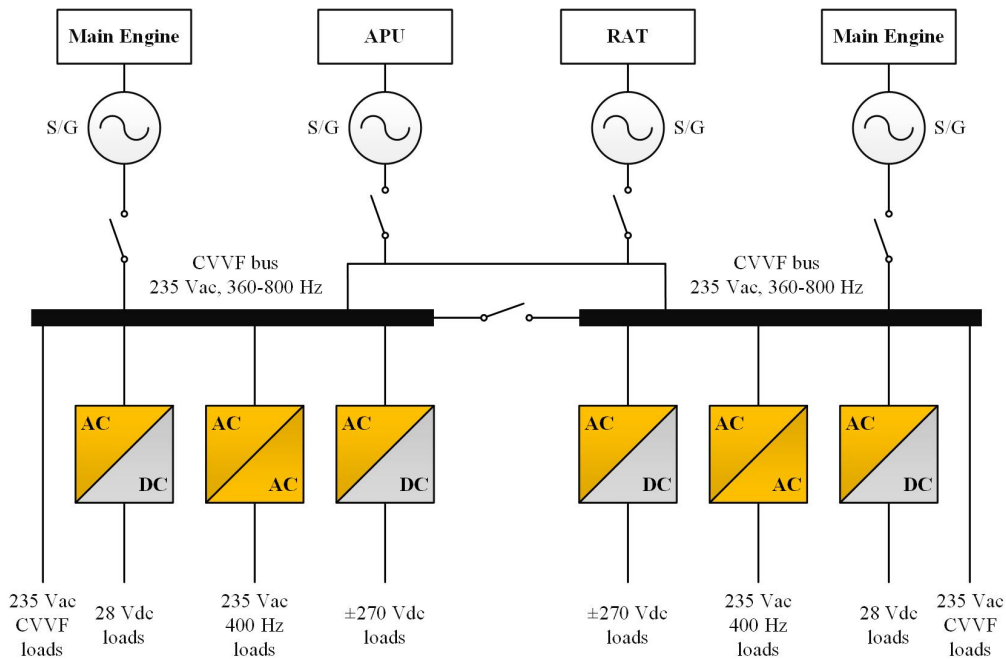


Figure 2.18: Architecture of power distribution system in more electrical aircraft Boeing 787.

for future MEA [116]. It allows to eliminate the transformer from power converter, thus to reduce the weight of the on-board power electronics system. The requirements of power converter conducted in this work are summarized in Table 2.5.

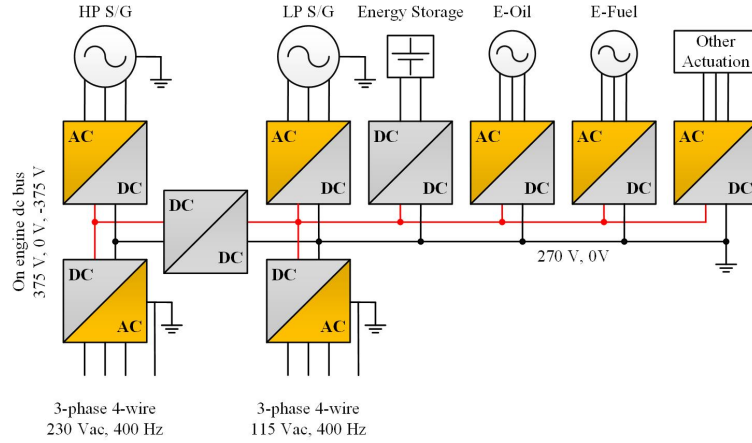


Figure 2.19: Architecture of power distribution system in next generation MEA.

Table 2.5: Requirements of power converter in next generation more electric aircraft.

Operation mode	Starting and generating
Power flow	Bidirectional
Input voltage	± 375 Vdc with neutral point
Input frequency	0 Hz
Output voltage	230 Vac (line-to-neutral) 3-phase 4-wire
Output frequency	400 Hz
DC-bus voltage variation	$\pm 10\%$
AC-bus voltage variation	$\pm 10\%$
Input/output earthing	Aircraft chassis
Switching frequency	> 20 kHz
Efficiency	$> 95\%$
Power density	> 4 kW/L > 4 kW/kg

2.8 Conclusion

The conclusions of this chapter are summarized below.

Firstly, the power devices are selected based on the commercial SiC power devices and power converter requirements in MEA. The normally-off SiC JFET is not selected due to the limited supply chain. In order to have a better understanding on device characteristics, the circuit simulation models for SiC power devices will be discussed in Chapter 3, which can also be used to assist converter design in the following work.

Secondly, the conventional VSD is adopted as the gate driver topology, since the maximum switching frequency of power converter designed in this work is expected to be 100 kHz. To maximize the high-speed switching advantage of SiC MOSFET, the gate driver and protection circuit design becomes to be a challenge due to the increasing dv/dt and di/dt , and they will be discussed in Chapter 4.

Thirdly, the advanced cooling technology needs to be investigated to further improve the power density and cooling efficiency. Hence, the integrated micro-channel cooling for power module will be discussed in Chapter 5 as a part of packaging technology. Although the low stray inductance packaging is not investigated in this work, the stray inductances of packaging as well as PCB layout still need to be investigated, which will be discussed in Chapter 6.

Finally, the relative lack of in-depth research on the HPDC for MEA applications has motivated this work. To optimize the performance of HPDC, the switching characterization for SiC power devices plays as the key role, which is a combination of device, gate driver, packaging and converter design. And it will be discussed in Chapter 6. Then the converter prototyping and testing will be presented in Chapter 7.

Chapter 3

Development of Circuit Simulation Model for SiC Power Devices

The accurate circuit simulation model of power device is of great significance to reduce the design cost and period in power electronics. Although some vendors will provide device model implemented in circuit simulator like Spice to the designer, it is incomplete and fails to cover all the products. In addition, most models are based on purely analytical curve fitting and it is difficult for the circuit designer to revise and make a new model based on it. In this chapter, the circuit simulation models for commercial SiC Schottky diode, SiC MOSFET and SiC power module are developed.

3.1 Introduction

Much work has been conducted in the development of circuit simulation models for SiC power devices. The physical model with FEM-based (finite element method) TCAD (technology computer-aided design) software offers the most accurate prediction but the longest simulation time [117]. In addition, it requires the device parameters including the geometry and physical models, which are normally restricted to the circuit designer. Hence, the TCAD model is still limited in device and process simulation. The circuit simulators, like PSpice [118] and Saber [119], offer the best trade-off between simulation accuracy and time. The semiconductor vendors provide the circuit simulation models of devices and

ICs to the circuit designer for function verification before prototyping. Most of the models provided by vendors are behavioral, which are based on purely mathematical equations and curve fitting with the measurement results. The behavioral models lack physical meaning. Hence, much work has been performed to integrate the equations and models of semiconductor physics into the behavioral models to improve the modeling accuracy.

The work in [120] proposed a physics-based, temperature-dependent circuit simulation model for SiC PiN diode and was implemented in PSpice. In addition, a simple parameter extraction strategy for the device geometry was proposed. The works in [121, 122] proposed comprehensive models that were implemented in Saber for all the three types of SiC power diodes, including Schottky, PiN and merged PiN/Schottky (MPS) diodes. Instead of extracting the geometry parameters, the device parameters like the saturation current and series resistance are extracted. The leakage current model of JBS diode is further considered in [123]. The work in [124] demonstrated a datasheet-oriented parameter extraction procedure of the geometry parameters for several types of commercial SiC Schottky diodes. However, some crucial physical mechanisms in SiC, like the incomplete ionization and Schottky contact, are still not fully addressed in these physics-based circuit simulation models.

Compared with SiC Schottky diode, the device structure of SiC MOSFET is much more complicated. Hence it is difficult to rebuild the geometry based on the limited information provided by the datasheet and most of the early works are behavior-based. The work in [125] was based on the Hefner IGBT model [126], in which the channel current consists of two portions: conduction at the corners at low current level and conduction by the main cells at high current level. Then the work in [127] further improved the model by defining a transition parameter to describe the gradual transition of SiC MOSFET from the linear region to the saturation region. Some early works introduced the n th-power law model presented by [128] to describe the transition region [129–131]. The work in [132] still adopted the standard level 1 Spice model of MOSFET, and it modeled the nonlinear Miller capacitance by the switch model, which accounts for the different doping concentrations in JFET and drift regions. Then in [133], the low temperature characteristics (25 °C) of SiC MOSFET was further modeled. In these works, the nonlinear Miller capacitance was still not well modeled especially at low bias.

The circuit simulation model for the emerging SiC power module is rather

limited. In [134], the SiC MOSFET/JBS power module was investigated, in which the MOSFET model was based on the Hefner IGBT model. And the packaging stray inductance was extracted by Ansys Q3D.

In this chapter, the off-the-shelf SiC power devices, including SiC Schottky diode, SiC MOSFET and SiC MOSFET module, are investigated. Their circuit simulation models are developed to address the issues in current models with two different approaches. The physics-based approach is adopted for SiC Schottky diode due to the relatively simple geometry. On the other hand, the behavior-based approach is adopted for both SiC MOSFET and SiC power module.

3.2 Physics-based Circuit Simulation Model of SiC Schottky Diode

A physics-based and datasheet-oriented parameter extraction strategy is proposed for three kinds of commercial SiC Schottky diode samples C4D20120 (1200 V/20 A), C4D10120 (1200 V/10 A), C4D05120 (1200 V/5 A) from Cree. Figure 3.1 shows the cross section and equivalent circuit of SiC Schottky diode. The typical fabrication process is described as follow. Firstly, a low doped n-type epitaxial layer is grown on the heavily doped n-type substrate. The Schottky contact is then formed on top of epitaxial layer after oxidation. Finally, the ohmic contacts are formed by aluminum and nickel depositions. The physical models as well as device parameters are necessary for the physics-based modeling. Unfortunately,

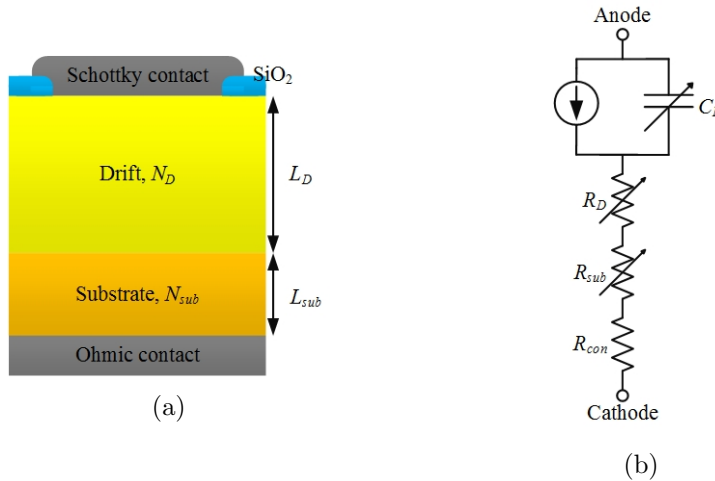


Figure 3.1: SiC Schottky diode: (a) cross section,(b) equivalent circuit.

the device parameters like geometry details and doping profiles are rarely provided by manufacturers. The key parameters can be extracted from the limited information in datasheet.

3.2.1 Model Description

Figure 3.2 shows the forward $I - V$ characteristics of C4D20120, which is used as the example for parameter extraction process. The current transport mechanism across Schottky contact is dominated by thermionic emission theory

$$I_F = I_S \left[\exp \left(\frac{qV_D}{kT} \right) - 1 \right] \quad (3.1)$$

where I_S is the saturation current, q is the elementary charge and V_D is the voltage drop across Schottky contact. The expression of I_S is given by

$$I_S = AA^*T^2 \exp \left(-\frac{q\phi_b}{kT} \right) \quad (3.2)$$

where A is the active area and ϕ_b is the Schottky barrier height. Then the forward voltage drop across Schottky diode is sum of voltage drops across the Schottky contact and series resistance

$$V_F = V_D + I_F R_S, \quad R_S = R_{con} + R_D + R_{sub} \quad (3.3)$$

where R_{con} , R_D and R_{sub} are the resistances of contact, drift and substrate respectively. As the specific contact resistance (normally $10^{-7} \sim 10^{-4} \text{ m}\Omega \cdot \text{cm}^2$) plays an insignificant role in overall series resistance, R_{con} is neglected. The overall series

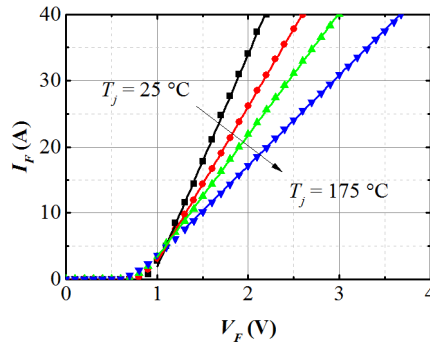


Figure 3.2: $I - V$ characteristics of C4D20120.

resistance is the reciprocal of slope of on-state $I - V$ curve

$$\frac{dV_F}{dI_F} = \frac{L_D}{q\mu_D N_D^+ A} + \frac{L_{sub}}{q\mu_{sub} N_{sub}^+ A} \quad (3.4)$$

where L_D , μ_D and N_D^+ are the thickness, electron mobility and ionized donors of drift region, L_{sub} , μ_{sub} and N_{sub}^+ are the thickness, electron mobility and ionized donors of substrate. The doping concentration in resistance expression is replaced by ionized dopants due to incomplete ionization effect. A typical substrate with $350 \mu\text{m}$ thickness and $1 \times 10^{19} \text{ cm}^{-3}$ doping is assumed. The electron mobility is obtained from Eq.(2.12) and (2.13).

The switching characteristics of Schottky diode is dominated by the depletion capacitance, which is almost temperature-independent

$$C = A \sqrt{\frac{q\epsilon N_D^+}{2(\phi_{bi} - V)}} \quad (3.5)$$

$$\phi_{bi} = \phi_b - \phi_n, \quad \phi_n = \frac{kT}{q} \ln \left(\frac{N_C}{N_D^+} \right) \quad (3.6)$$

where ϕ_{bi} is the contact potential, ϕ_n is the energy difference between conduction band and Fermi level [10], and V should be negative when reverse biased. The $C - V$ characteristics of C4D20120 is shown in Figure 3.3(a). From Eq.(3.5), the linear relationship between $1/C^2$ and reverse voltage V_R can be derived, as Figure

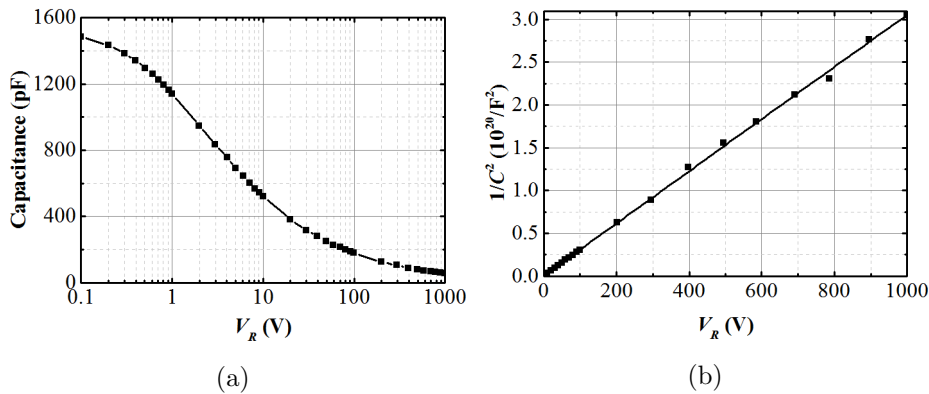


Figure 3.3: $C - V$ characteristics of C4D20120: (a) capacitance versus V_R , (b) $1/C^2$ versus V_R .

3.3 (b) shows.

$$\frac{d(1/C^2)}{dV_R} = \frac{2}{qN_D^+A^2} \quad (3.7)$$

The limitation of junction termination technology degrades the breakdown voltage compared with the ideal parallel planar junction. Hence the correlations which predict ideal breakdown voltage with respect to doping cannot be used for parameter extraction. The drift thickness can be estimated from the depletion length at breakdown voltage

$$L_D = \sqrt{\frac{2\varepsilon BV}{qN_D^+}} \quad (3.8)$$

The Schottky barrier height is determined by the metal work function and the metal-semiconductor interface states, the latter of which strongly relies on process. Hence, the parameter extraction for Schottky barrier height is needed even if the metal work function is known. Supposing $V_D \gg kT/q$, the Schottky barrier height can be derived from Eq.(3.1)~(3.3) as

$$\phi_b = \frac{kT}{q} \ln \left(\frac{AA^*T^2}{I_F} \right) + V_F - I_F R_s \quad (3.9)$$

3.2.2 Parameter Extraction

Combining Eq.(3.4) and (3.7)~(3.9), the four variables N_D^+ , L_D , A and ϕ_b can be extracted. N_D^+ , L_D and A are coupled with each other, while ϕ_b is only dependent on A . The relationship between N_D^+ and drift doping N_D is described by incomplete ionization, as Eq.(2.10) illustrates. Thus N_D , L_D and A are firstly extracted, then ϕ_b is calculated based on A . Since there are several groups of $I-V$

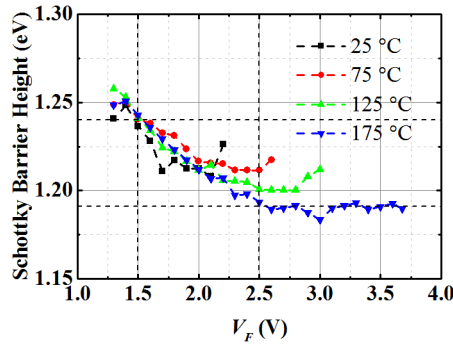


Figure 3.4: Parameter extraction results for Schottky barrier height.

Table 3.1: Parameter extraction results for C4D10120 at different temperatures.

Temperature	N_D (cm^{-3})	L_D (μm)	A (m^2)
25	3.76×10^{15}	19	0.1122
75	3.73×10^{15}	19	0.1119
125	3.92×10^{15}	18	0.109
175	3.66×10^{15}	19	0.1127
Tolerance	6.6%	5.3%	3.3%

Table 3.2: Parameter extraction results for SiC Schottky diodes.

Part no.	N_D (cm^{-3})	L_D (μm)	A (m^2)	ϕ_b (eV)
C4D20120	3.76×10^{15}	19	0.1122	1.224
C4D10120	3.86×10^{15}	19	0.0613	1.223
C4D05120	4.18×10^{15}	18	0.0311	1.218

data at different junction temperatures, any group can be used for parameter extraction and similar results should be obtained. As Table 3.1 shows, parameter extraction results for N_D , L_D and A at different junction temperatures coincide well with each other. Substituting A , I_F and V_F at different temperatures into Eq.(3.9), the extracted value of ϕ_b varies between 1.19~1.26 eV (5.6% tolerance), as Figure 3.4 shows. And in the main operating region ($V_F = 1.5\sim 2.5$ V), ϕ_b varies between 1.19~1.24 eV (4% tolerance). In present work, the extraction results of the first group (25 °C) are adopted, and for ϕ_b the mean value is used. In addition, ϕ_{bi} is obtained by substituting ϕ_b and N_D into Eq.(3.6).

Similar parameter extraction algorithm is implemented on the other two samples, and the results are given in Table 3.2. The values drift doping and thickness, Schottky barrier height of the three diode samples are close to each other. On the other hand, the active area shows a difference of times in correspondence to the device current rating.

3.2.3 Model Implementation

The physics-based SiC Schottky diode model is implemented in PSpice for circuit simulation, using the equivalent subcircuit model shown in Figure 3.1(b). The default diode model can be directly incorporated to model the current transport

mechanism. The temperature-dependent saturation current is given by [135]

$$IS(T) = IS\left(\frac{T}{T_0}\right)^{XTI/N} \exp\left[\frac{qEG}{Nk}\left(\frac{1}{T_0} - \frac{1}{T}\right)\right] \quad (3.10)$$

where IS is the saturation current at 300 K, XTI is the temperature coefficient with the value of 2, N is the emission coefficient with the value of 1, and EG is the Schottky barrier height.

As it is difficult to incorporate the junction capacitance of SiC Schottky diode into default diode model, the junction capacitance at zero bias (CJO) in the diode model is assumed to be 0 and an external parallel capacitor is defined. The analog behavioral modeling (ABM) module provides the feasibility to model the nonlinear capacitance. A voltage controlled current source (VCCS) can be used to model the depletion capacitance

$$I = A\sqrt{\frac{q\varepsilon N_D}{2(\phi_{bi} - V)}} \frac{dV}{dt} \quad (3.11)$$

The temperature-dependence of resistor can only be modeled by polynomial with temperature coefficients in PSpice. The global temperature parameter in simulation settings cannot be used in the default resistor model. Hence, the resistance is replaced by a VCCS, in which global temperature parameter can be incorporated. The VCCS is defined by the voltage drop across the resistance. Since external resistors are introduced to model R_D and R_{sub} , the parasitic resistance RS in the default diode model is also assumed to be 0.

The physics-based model is coded and packaged in PSpice. The extracted

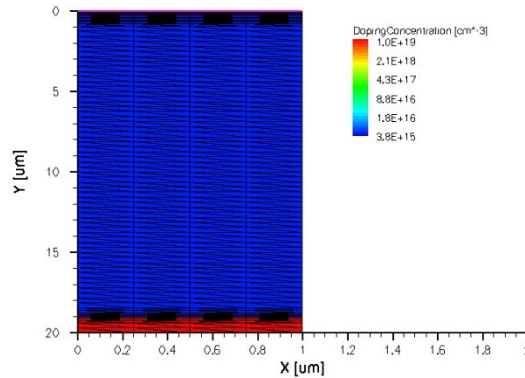


Figure 3.5: TCAD simulation model of SiC Schottky diode.

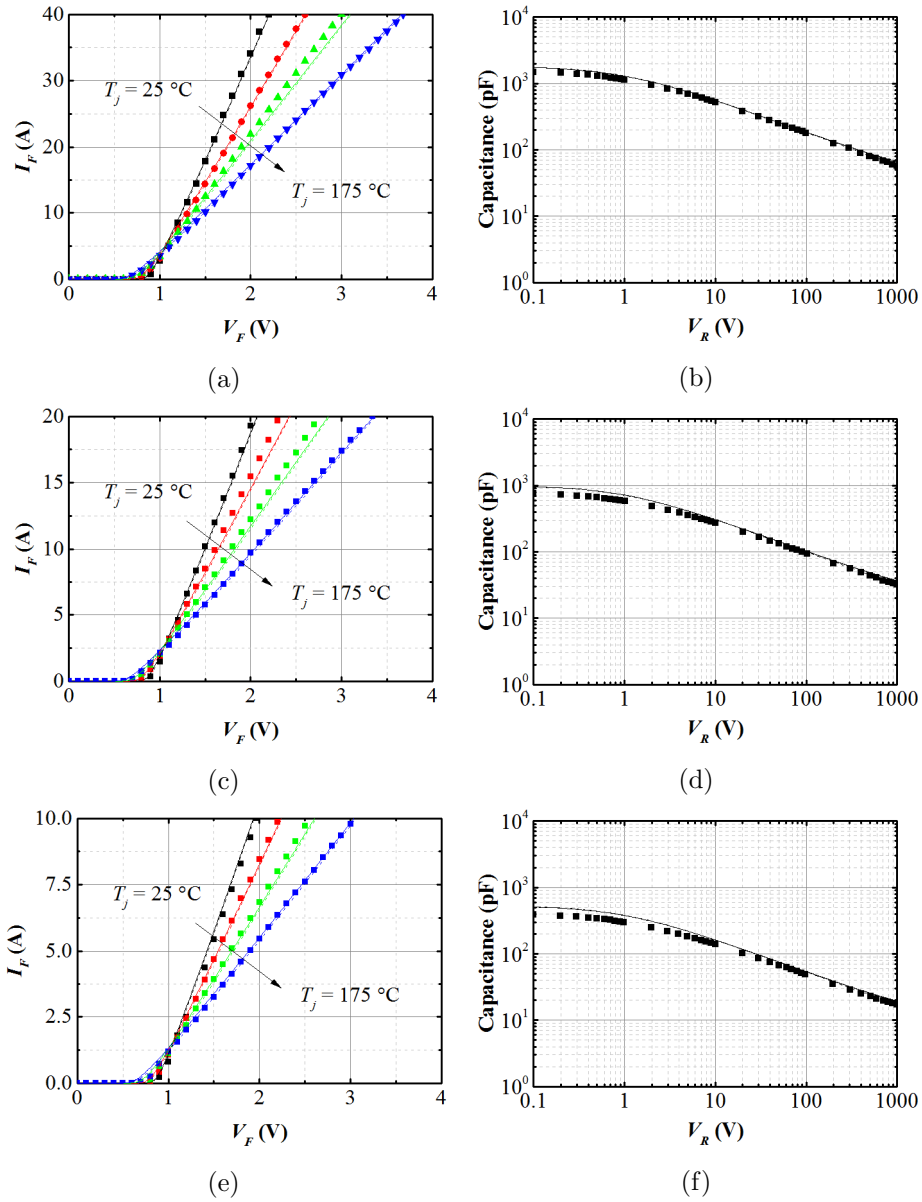


Figure 3.6: $I - V$ (a) and $C - V$ (b) characteristics of C4D20120; $I - V$ (c) and $C - V$ (d) characteristics of C4D10120; $I - V$ (e) and $C - V$ (f) characteristics of C4D05120.

device parameters are also incorporated in Synopsys TCAD Sentaurus for further verification, with the physical models discussed in the previous section. The doping profile with mesh definition in TCAD Sentaurus is shown in Figure 3.5. To speed up the numerical simulation, the heavily doped substrate is laminated to $1\ \mu\text{m}$ and modeled by an external contact resistance. The comparison between datasheet and simulation results is shown in Figure 3.6. In these figures, the dots are from datasheet, solid lines are PSpice simulation results and dashed lines are Sentaurus simulation results. It is found that both simulation results show a good agreement with datasheet. Only at low reverse bias ($V_R < 1$), the simulation results of $C - V$ characteristics cannot match datasheet perfectly. Nevertheless, this region is unimportant for the switching characteristics of SiC Schottky diode.

3.3 Behavior-based Circuit Simulation Model of SiC MOSFET

A behavioral and datasheet-oriented parameter extraction strategy is proposed for two commercial SiC MOSFET samples CMF20120 (1200 V/20 A) and C2M0080120 (1200 V/30 A) from Cree. Figure 3.7 shows the cross section and equivalent circuit of SiC MOSFET. The typical fabrication process is described in the following. Firstly, a low doped n-type epitaxial layer is grown on the heavily doped n-type substrate. Then the P well and N+ source regions are formed by a double implantation process, and the channel length is determined by the difference of implantation depth. The JFET region is formed by a selective n-type ion implan-

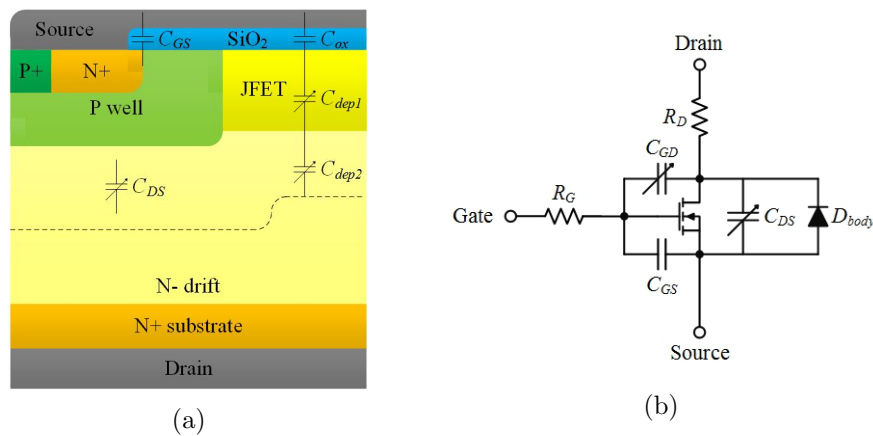


Figure 3.7: SiC MOSFET: (a) cross section, (b) equivalent circuit.

tation process. After rapid thermal annealing (RTA) to activate the implanted ions, a thin layer of gate oxide is grown by wet oxidation. Finally, the ohmic contacts are formed by aluminum and nickel depositions.

3.3.1 Model Description

The output characteristics of SiC MOSFET is based on standard MOSFET level 1 SPICE model [135]. When the gate-source voltage V_{GS} is below the threshold voltage V_{th} , the channel is cut off and no current flows between drain and source, hence the MOSFET operates in the cut-off region at this time.

$$I_D = 0, \text{ when } V_{GS} < V_{th} \quad (3.12)$$

A subthreshold current may exist when V_{GS} increases but is still below V_{th} , and the semiconductor-oxide interface is in weak inversion. Considering the much lower current in subthreshold region than the current in full conduction region, it is normally neglected in power MOSFET modeling.

Once V_{GS} is above V_{th} , the semiconductor-oxide interface is in strong inversion, which acts as a current conducting channel between drain and source. With a bias applied to the channel, the electrons start to move from source to drain via the inversion layer. A saturation voltage is defined by the expression $V_{DS,sat} = V_{GS} - V_{th}$. When the channel voltage drop V_{ch} is below $V_{DS,sat}$, the MOSFET operates in the linear region (also called as triode region). The MOSFET behaves like a resistor, which is controlled by the gate voltage. The drain current exhibits an approximately linear relationship with V_{ch} . When V_{ch} further increases and exceeds $V_{DS,sat}$, the MOSFET operates in the saturation region. The channel is pinched off near the drain area and ideally the drain current remains the same regardless of drain bias. However, when the shortened channel length is a substantial fraction of the total length, the short-channel effect (SCE) needs to be taken into account in the device modeling. And the drain current is weakly dependent on the drain bias in reality. It has been found that SCE is an important consideration when modeling the SiC MOSFET [54]. The expressions of the drain current in both the linear and saturation regions are given by

$$I_D = \beta \left(V_{DS,sat} - \frac{V_{ch}}{2} \right) V_{ch} (1 + \lambda V_{ch}), \text{ when } V_{GS} \geq V_{th} \text{ and } V_{ch} < V_{DS,sat} \quad (3.13)$$

$$I_D = \beta \frac{V_{DS,sat}^2}{2} (1 + \lambda V_{ch}), \text{ when } V_{GS} \geq V_{th} \text{ and } V_{ch} \geq V_{DS,sat} \quad (3.14)$$

$$V_{th} = V_{th0} + \gamma \left(\sqrt{2\phi_p - V_{sb}} - \sqrt{2\phi_p} \right) \quad (3.15)$$

$$\beta = \mu_{ch} C_{ox} \frac{W}{L} \quad (3.16)$$

where V_{th0} is the zero bias threshold voltage, γ it the body effect coefficient, ϕ_p is the surface potential, V_{sb} is the substrate bias voltage, β is the transconductance coefficient, λ is the channel modulation index, μ_{ch} is the channel electron mobility, C_{ox} is the capacitance of gate oxide, W and L are the channel width and length respectively. Due to the effect of inversion layer charge in SiC MOSFET, μ_{ch} shows a linear relationship with gate bias [136]. Hence β is given by

$$\beta = [\beta_0 + VC_1 (V_{GS} - V_{GS,nom})] \quad (3.17)$$

where VC_1 is the voltage coefficient. As the voltage coefficient of β cannot be fitted into the MOSFET level 1 model, a VCCS is introduced to model the channel current. And the transition between current conduction mode is modeled by two embedded IF() function blocks.

The on-resistance of MOSFET is a sum of the resistors including contact, N+ source, accumulation layer, JFET region, drift and N+ substrate. In order to simplify analysis, only the drift resistance R_D is considered. Hence the overall drain-source voltage drop V_{DS} is given by

$$V_{DS} = V_{ch} + I_D R_D \quad (3.18)$$

Due to the wide bandgap of SiC, the built-in potential of P-N junction is also higher, as given by

$$\phi_{bi} = \frac{kT}{q} \ln \left(\frac{N_D N_A}{n_i^2} \right) \quad (3.19)$$

where the typical doping concentrations of drift region and P-well region are $1 \times 10^{15} \text{ cm}^{-3}$ and $1 \times 10^{17} \text{ cm}^{-3}$ respectively. Substituting the intrinsic carrier concentration calculated by Eq.(1.2), the built-in potential is estimated to be 2.85 V. The high built-in potential is one disadvantage of SiC P-N junction [9]. Therefore, the body diode of SiC MOSFET cannot be used as the freewheeling diode. The external SiC Schottky diode is necessary to bypass the freewheeling current. Or the SiC MOSFET can work in the 3rd-quadrant region as a syn-

chronous rectifier. The current transport mechanism across the P-N junction is given by the Shockley equation.

$$I_F = I_S \left[\exp \left(\frac{qV_D}{kT} \right) - 1 \right] \quad (3.20)$$

The Shockley equation for ideal diode with P-N junction is similar to the expression for Schottky contact. However, the saturation current is defined as

$$I_S = Aqn_i^2 \left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A} \right) \quad (3.21)$$

where D_n/D_p is the electron/hole diffusion coefficient, which is given by the Einstein relation, L_n/L_p is the electron/hole diffusion length. The relationships are given by

$$D_n = \frac{kT}{q} \mu_n, \quad D_p = \frac{kT}{q} \mu_p \quad (3.22)$$

$$L_n = \sqrt{D_n \tau_n}, \quad L_p = \sqrt{D_p \tau_p} \quad (3.23)$$

For the abrupt junction, the saturation current is dominated by the low doped drift region. Hence, Eq.(3.21) can be simplified as

$$I_S = Aqn_i^2 \frac{D_p}{L_p N_D} \quad (3.24)$$

The forward voltage drop across the body diode is a sum of voltage drops on P-N junction and series resistance

$$V_{SD} = V_D + I_F R_S \quad (3.25)$$

Here V_{SD} and I_F are used instead of V_{DS} and I_D in Eq.(3.18), since the current flows from source to drain. V_D is also defined as knee voltage. The body diode can be directly modeled by the default diode model in PSpice. The saturation current I_S and series resistance R_S need to be extracted during the modeling procedure.

The absence of minority carriers makes the MOSFET inherently suitable for high frequency operation. The dynamic characteristics of MOSFET are dominated by charging and discharging of internal parasitic capacitors, including gate-source (C_{GS}), drain-source (C_{DS}) and gate-drain (C_{GD}) capacitors. C_{GS} is mainly due to overlap of gate metalization over source and P well regions, and it is modeled by a constant capacitor. C_{DS} is a bias-dependent depletion capacitor of P

well / N- drift junction, which is modeled by the junction capacitance in default diode model

$$C_{DS} = C_{DS0} \left(\frac{V_{bi}}{V_{DS} + V_{bi}} \right)^{M_{CDS}} \quad (3.26)$$

where V_{bi} is the build-in potential, and M_{CDS} is the fitting parameter.

The Miller capacitor C_{GD} is the most important and complicated parasitic capacitor, as it provides the feedback loop between output and input. C_{GD} is due to the overlap of gate metalization over drift region. And it consists of a constant gate oxide capacitor C_{ox} in series with a bias-dependent depletion capacitor C_{dep} beneath the gate oxide, as Figure 3.8 shows. During on-state with $V_{GD} > 0$, the depletion region shrinks, C_{ox} is much smaller than C_{dep} and becomes the dominant factor of C_{GD} . During off-state with $V_{DG} > 0$, the depletion region gradually expands. Due to the different doping concentration in JFET and drift regions, two different depletion capacitors C_{dep1} and C_{dep2} exist. From the $C - V$ curve, two different slopes can be observed and a transition voltage V_{DGT} is defined. When V_{DG} is below V_{DGT} , only C_{dep1} exists and C_{GD} is given by series of C_{ox} and C_{dep1} . When V_{DG} exceeds V_{DGT} , the drift region begins to be depleted, and C_{GD} is given by series of C_{ox} , C_{dep1} and C_{dep2} . The definition of C_{GD} is given by

$$C_{GD} = \begin{cases} C_{ox}, & \text{when } V_{DG} < 0 \\ C_{ox} \parallel C_{dep1}, & \text{when } 0 < V_{DG} < V_{DGT} \\ C_{ox} \parallel C_{dep1}(V_{DGT}) \parallel C_{dep2}, & \text{when } V_{DG} > V_{DGT} \end{cases} \quad (3.27)$$

$$C_{dep1} = \left(\frac{\epsilon q N_{JFET}}{2V_{DG}} \right)^{M_{CDEP1}} A = \frac{C_1}{V_{DG}^{M_{CDEP1}}} \quad (3.28)$$

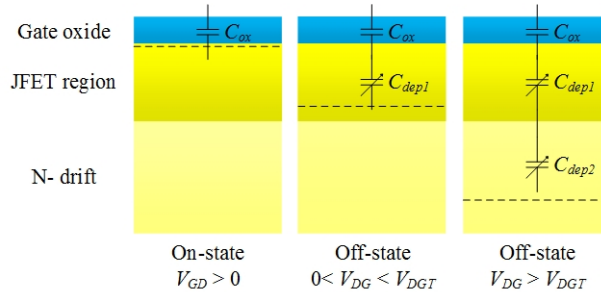


Figure 3.8: Miller capacitor model.

$$C_{dep2} = \left[\frac{\epsilon q N_D}{2(V_{DG} - V_{DGT})} \right]^{M_{CDEP2}} A = \frac{C_2}{(V_{DG} - V_{DGT})^{M_{CDEP2}}} \quad (3.29)$$

where N_{JFET} and N_D are the doping concentrations of JFET and drift region respectively, C_1 is the unit depletion capacitance of JFET region at $V_{DG} = 1$ V, C_2 is the unit depletion capacitance of drift region at $V_{DG} - V_{DGT} = 1$ V, and M_{CDEP1} , M_{CDEP2} are the fitting parameters. The circuit behavior is also controlled by two embedded IF() function blocks.

3.3.2 Parameter Extraction

The parameter extraction is demonstrated in the following process:

A. Threshold Voltage

As there is no general criterion for V_{th} , which defines V_{GS} at I_D like 1 mA, 5 mA, 50 mA, et al., V_{th} within an acceptable range needs to be extracted even though it is provided by the datasheet. In the saturation region, V_{ch} is the dominant factor of V_{DS} as the channel is pinched-off. A simplification of Eq.(3.14) can be made with replacement of V_{ch} by $V_{DS} = 20$ V. From the transfer characteristics, a 2nd order polynomial fitting for $I_D - V_{GS}$ is made using the curve fitting tool in Matlab.

B. Transconductance Coefficient

At low gate bias ($V_{GS} < 12$ V), R_{ch} is the dominant factor of R_{on} . Hence a similar simplification for Eq. (3.13) can be made with replacement of V_{ch} by V_{DS} in the linear region. In addition, the SCE is also neglected. After considering the voltage-dependent property of β , the simplified $I_D - V_{DS}$ relationship is given by

$$I_D = [\beta_0 + VC_1 (V_{GS} - 10)] \left(V_{GS} - V_{th} - \frac{V_{DS}}{2} \right) V_{DS} \quad (3.30)$$

Two sets of $I_D - V_{DS}$ data in linear region at $V_{GS} = 10$ V (nominal voltage) and 12 V are used to extract β_0 and VC_1 .

C. Drift resistance and Channel Modulation Index

When the gate bias is as high as 20 V, R_{ch} will be reduced significantly and become comparable with R_D . In order to extract R_{ch} , an assumption is made with $R_D = 0 \Omega$ and $\lambda = 0$ during simulation. And therefore it is the reciprocal of slope of $I_D - V_{DS}$ curve. Then R_D can be derived by

$$R_D = R_{on} - R_{ch} = R_{on} - \frac{dV_{DS}}{dI_D} \quad (3.31)$$

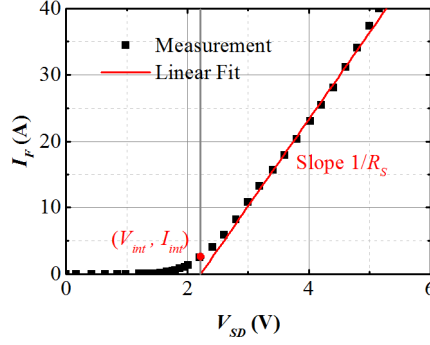


Figure 3.9: Body diode characteristics of CMF20120.

where R_{on} is the typical on-resistance in the datasheet. Finally, a channel modulation index of 0.01 is set after adjusting the simulated curves to fit the measurement.

D. Body Diode

The body diode characteristics are measured by the Tektronix high power curve tracer 371A. As Figure 3.9 shows, R_S is the reciprocal of slope of $I_F - V_{SD}$ curve, which can be derived by linear fit. And V_D is extracted by subtracting the voltage drop on R_S from V_{int} (intercept of $I_F - V_{SD}$ curve at V -axis)

$$V_D = V_{int} - I_{int}R_S \quad (3.32)$$

The knee voltage is defined at the forward current of 100 mA. Then I_S is calculated by the following equation. Finally I_S is slightly adjusted in PSpice to make the simulated curve match the measurement.

$$I_S = 0.1 \times \exp\left(-\frac{V_D}{0.026}\right) \text{ A} \quad (3.33)$$

E. Parasitic Capacitance

Typically, three kinds of capacitor are provided by the datasheet: input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances. And the parasitic capacitors can be derived from

$$C_{GS} = C_{iss} - C_{rss}, \quad C_{DS} = C_{oss} - C_{rss}, \quad C_{GD} = C_{rss} \quad (3.34)$$

Firstly, C_{GS} is extracted by subtracting C_{rss} from C_{iss} , and a constant value

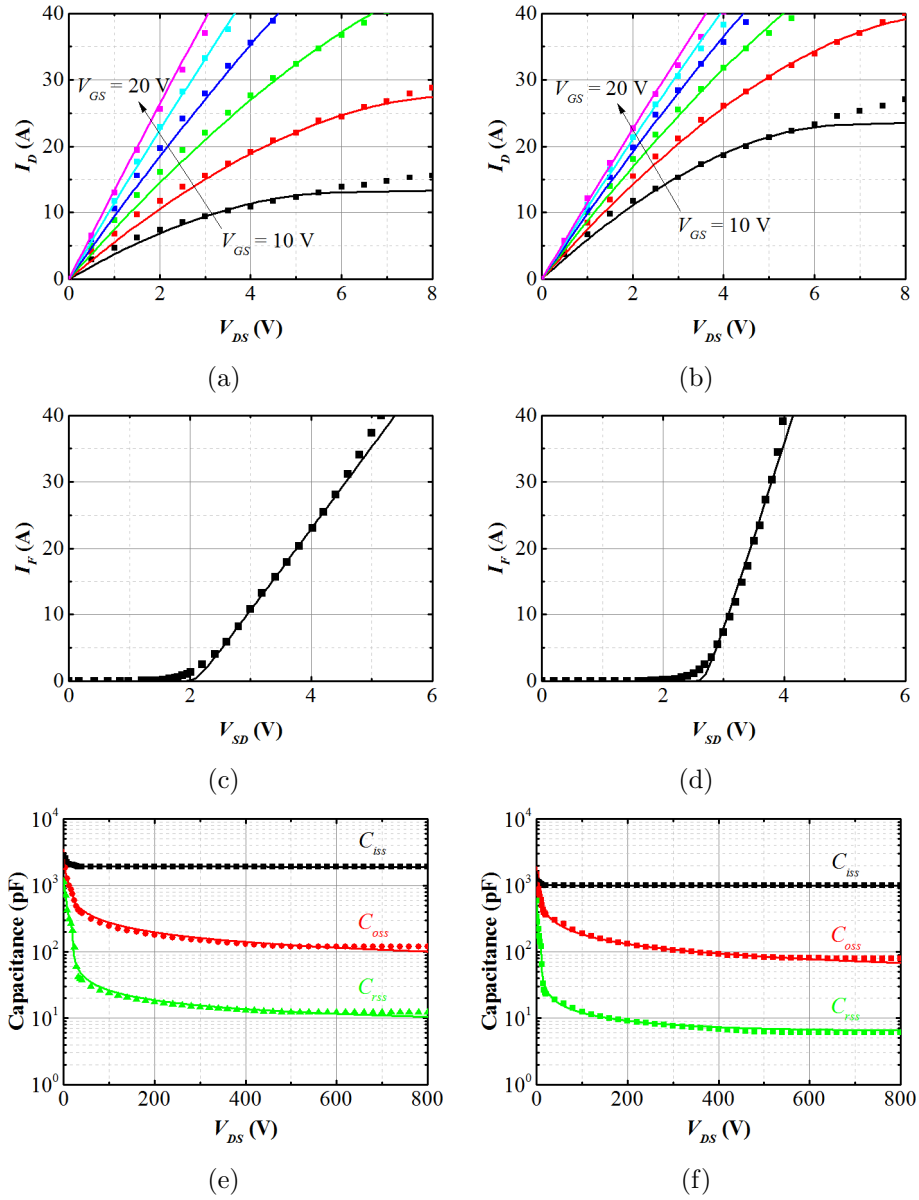


Figure 3.10: $I - V$ characteristics of CMF20120 (a) and C2M0080120 (b); Body diode of CMF20120 (c) and C2M0080120 (d); $C - V$ characteristics of CMF20120 (e) and C2M0080120 (f).

is obtained. The bias-dependent C_{DS} can be derived in a similar way. And the fitting parameters for C_{DS} are extracted by curve fitting of $C_{DS} - V$ relationship with Eq.(3.26). C_{ox} is extracted from C_{rss} at zero bias. V_{DGT} can be easily extracted from the $C_{rss} - V$ curve due to the two remarkably different slopes. Then the fitting parameters for C_{dep1} and C_{dep2} are piecewise extracted by curve fitting of $C_{rss} - V$ relationship with Eq.(3.28) and (3.29).

3.3.3 Model Implementation

The behavior-based models for the two commercial SiC MOSFET samples are implemented in PSpice. And the simulated output, body diode and $C - V$ characteristics from PSpice match well with that from datasheet for the two kinds of SiC MOSFET samples CMF20120 and C2M0080120, as shown in Figure 3.10. In these figures, dots are from datasheet while solid lines are simulation results. In addition, the simulated $C_{rss} - V$ characteristics in Figure 3.10(c) shows a very good agreement with the datasheet. Hence, the nonlinear model for Miller capacitance developed in this work provides an accurate curve fitting result and also a good description on its physical behavior.

3.4 Behavior-based Circuit Simulation Model of SiC Power Module

The SiC power modules CAS100H12AM1 (1.2 kV, 100 A) and CAS120M12BM2 (1.2 kV, 120 A) from Cree are investigated in present work, with the half bridge configuration shown in Figure 3.11. The CAS100H12AM1 consists of five parallel Cree 1st generation SiC MOSFETs, and five anti-parallel SiC Schottky diodes. An internal 1.25Ω resistance is in series with the gate electrode of each MOSFET die. The CAS120M12BM2 consists of 6 parallel Cree 2nd generation SiC MOSFETs, and 12 anti-parallel SiC Schottky diodes. Similarly, an internal 1.8Ω resistance is used. And the Kelvin source is adopted to separate the gate driver loop from the power loop for both modules.

A behavioral and datasheet-oriented subcircuit model is proposed for SiC power module. In [134], each SiC MOSFET die was modeled separately, which tends to increase the simulation time. To simplify the model, the parallel SiC MOSFETs are equivalent to be a single MOSFET, and the parallel SiC Schottky diodes are equivalent to be a single diode as well. The equivalent circuits for both

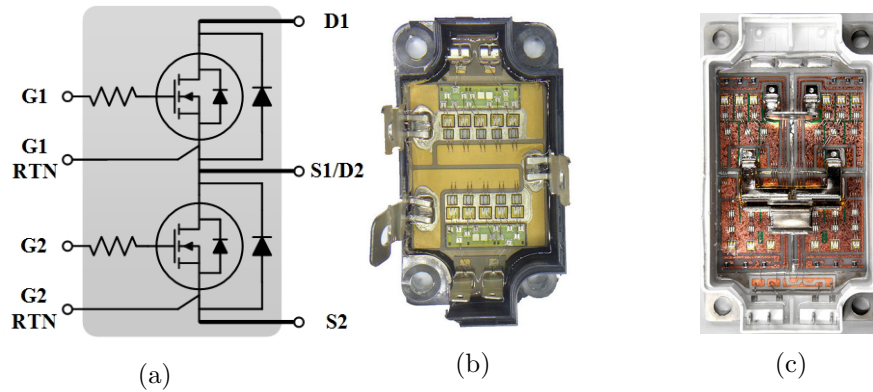


Figure 3.11: SiC half bridge module: (a) schematic, (b) CAS100H12AM1, (c) CAS120M12BM2.

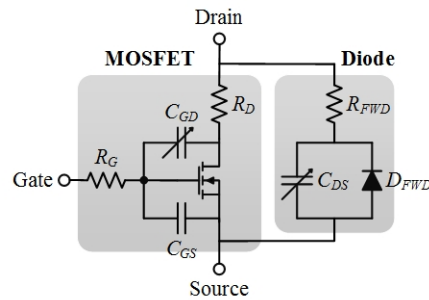


Figure 3.12: Equivalent circuit of SiC power module.

the high side and low side of module are identical, as shown in Figure 3.12. Due to the high knee voltage of body diode of SiC MOSFET, it will never conduct when parallel with the external SiC Schottky diode. Hence, the body diode can be neglected in the model. In addition, the drain-source capacitance of MOSFET is absorbed by the anti-parallel diode. The output, freewheeling diode and $C - V$ characteristics of SiC MOSFET module can be modeled in a similar procedure as in the previous section, as Figure 3.13 shows. A good agreement is achieved between the model and datasheet.

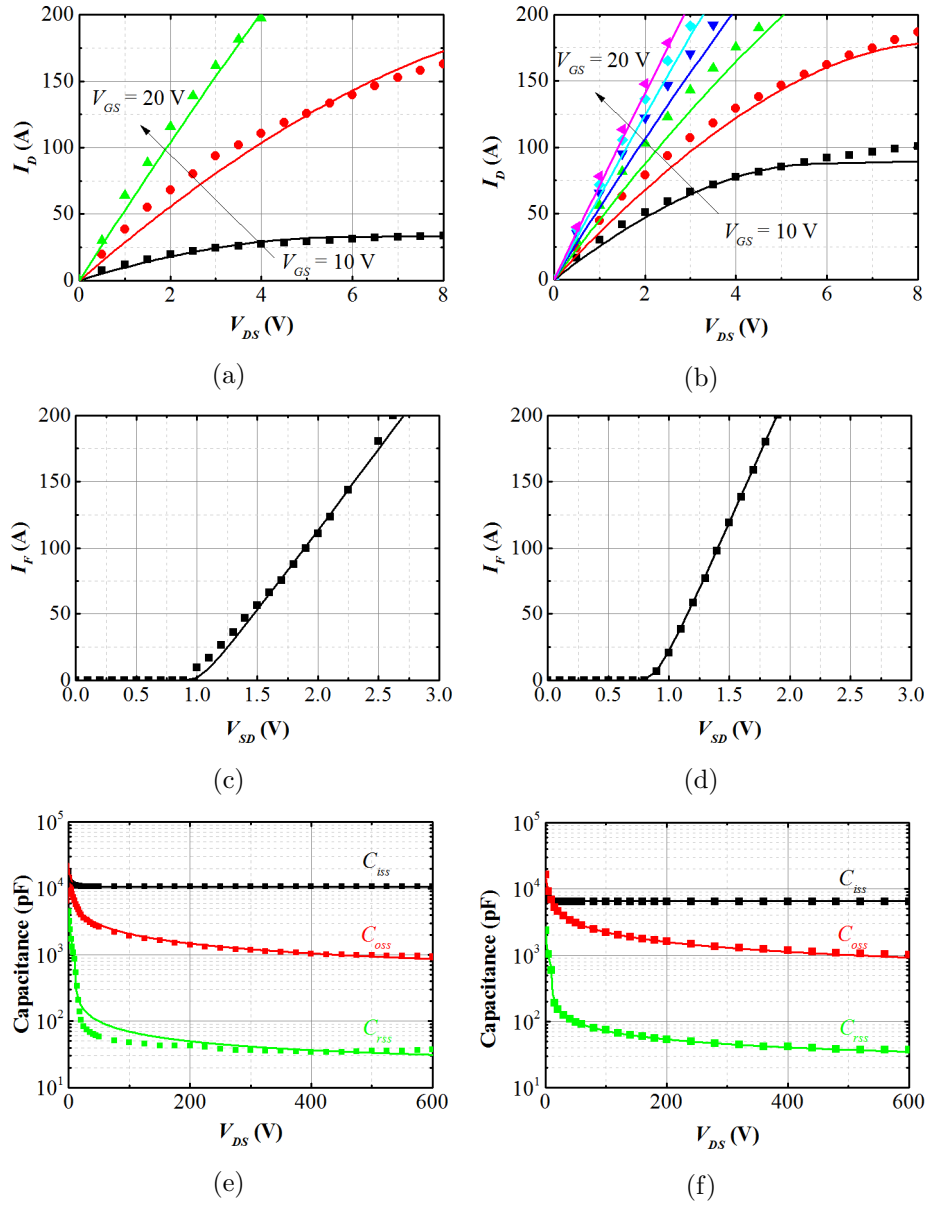


Figure 3.13: $I - V$ characteristics of CAS100H12AM1 (a) and CAS120M12BM2 (b); Freewheeling diode of CAS100H12AM1 (c) and CAS120M12BM2 (d); $C - V$ characteristics of CAS100H12AM1 (e) and CAS120M12BM2 (f).

3.5 Experimental Verification

In this section, the switching characteristics of circuit simulation models are verified by the double pulse testing experiment. The details of experiment will be demonstrated in Chapter 6. The Cree 2nd generation SiC power module CAS120M12BM2 is investigated.

The schematic in PSpice simulation is shown in Figure 3.14. To make the simulated curve fit with the experimental, the external gate resistance $R_{G,ext}$ and external stray inductance $L_{S,ext}$ needs to be extracted from the experiment. And $R_{G,ext}$ is extracted based on the measured RC constant of gate driver loop

$$R_{G,ext} = \frac{\tau}{C_{iss}} - R_{G,int} \quad (3.35)$$

where $R_{G,int}$ is the internal gate resistance of power module. $L_{S,ext}$ is extracted based on the resonant frequency of power converter loop

$$L_{S,ext} = \frac{1}{(2\pi f)^2 C_{oss}} - L_{S,int} \quad (3.36)$$

where $L_{S,int}$ is the internal stray inductance of power module, C_{oss} is the output capacitance of power module at a certain bias voltage. The power module is tested at 750 V DC-bus voltage. Comparison between the experimental and simulated switching waveforms under the load current of 50 A and 100 A is shown in Figure 3.15. The simulated results show a good agreement with the experimental results.

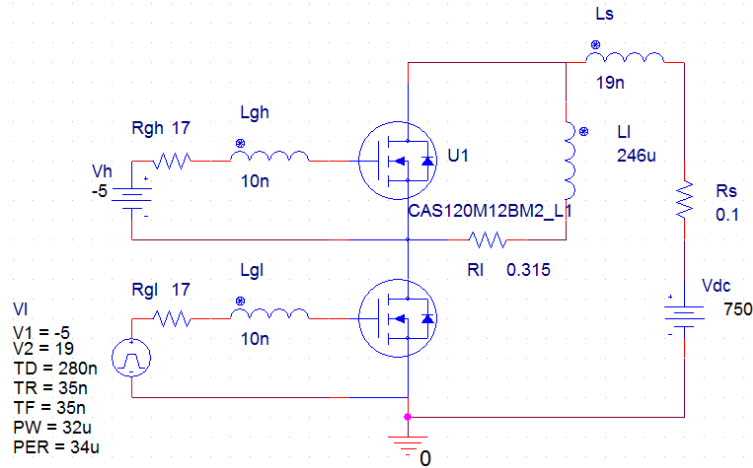
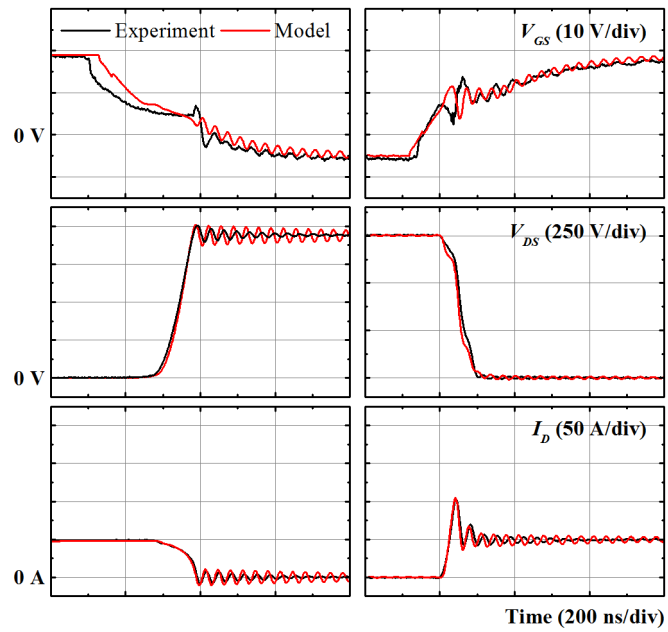
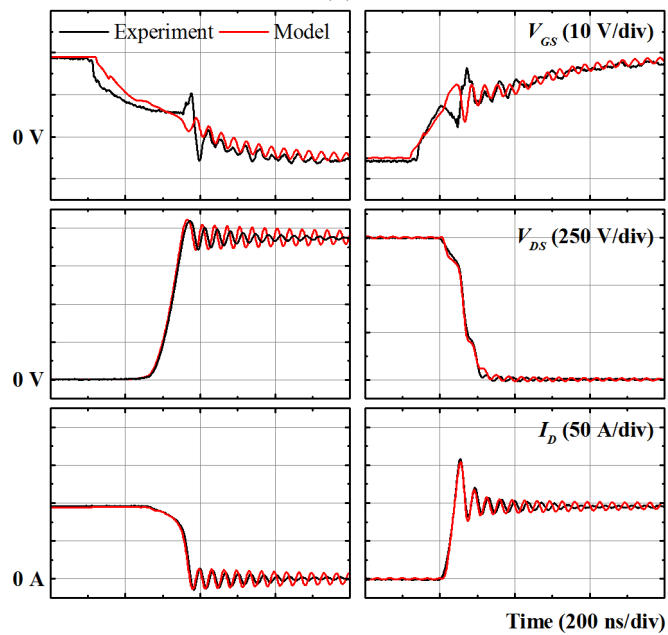


Figure 3.14: PSpice simulation schematic of double pulse testing.



(a)



(b)

Figure 3.15: Comparison of switching waveforms between experiment and simulation: (a) 50 A, (b) 100 A.

3.6 Conclusion

The conclusions of this chapter are summarized below.

Firstly, a physics-based and temperature-dependent circuit simulation model for the commercial SiC Schottky diode has been presented and implemented in PSpice. Based on the datasheet, a parameter extraction procedure is conducted for the device physical parameters, including drift concentration and thickness, active area and Schottky barrier height. The device parameters as well as the detailed physical models of SiC are also incorporated in TCAD Sentaurus. A good match between the PSpice and TCAD simulations are attained over a wide range of temperature.

Secondly, a behavior-based circuit simulation model for the commercial SiC MOSFET has been presented and implemented in PSpice. Based on the datasheet, a parameter extraction procedure is conducted for the device parameters, like the transconductance, series resistance and threshold voltage. An accurate model for the nonlinear Miller capacitance is presented, which accounts for the different doping concentrations in the JFET and drift regions.

Finally, a behavior-based circuit simulation model for the commercial SiC power module has been presented and implemented in PSpice. The parameter extraction process can be directly inherited from that of SiC MOSFET. Instead of modeling each die separately, the parallel SiC MOSFETs are equivalent to be a single MOSFET, and also similar to the SiC Schottky diodes. With this simplification strategy, the simulation time and convergence issue can be improved significantly. And a good agreement between simulation model and double pulse testing experiment is achieved.

CHAPTER 3. DEVELOPMENT OF CIRCUIT SIMULATION MODEL FOR
SIC POWER DEVICES

Chapter 4

Design of High-speed Gate Driver for SiC MOSFET

In this chapter, the high-speed gate drivers for discrete SiC MOSFET and SiC power module are designed. The impact of parasitic parameters on gate driver is analyzed and modeled. A novel gate assisted circuit is proposed to further mitigate the dv/dt effect. And a novel short-circuit protection scheme using gate charge detection is proposed for SiC MOSFET.

4.1 Introduction

In power electronics system, the gate driver serves as the interface between the controller and power devices to provide the gate driving signal at the desired voltage and current levels. The power supply of controller is only 3.3 V or 5 V, while the bus voltage of power converter may reach up to thousands of volts. Hence, it also provides electrical isolation between controller and power converter. In addition, some protection strategies implemented via the gate driver including over-voltage and short-circuit are necessary for power converter.

Design of compact and high-speed gate driver for Si IGBT has become very mature during the past decades with the rapid advancement of semiconductor industry. Recent emergence of SiC MOSFET breaks through the frequency limitation of Si IGBT. It is regarded as an attractive alternative of Si IGBT for high power density applications. As both devices have similar MOS-gated structure, the gate driver of SiC MOSFET can inherit from that of Si IGBT. However, considering the inherent difference in device physics shown in Table 4.1, some special

CHAPTER 4. DESIGN OF HIGH-SPEED GATE DRIVER FOR SiC
MOSFET

Table 4.1: Comparison between SiC MOSFET C2M0080120D and Si IGBTs IKW15N120H3 and STGW15M120DF3.

Parameters	SiC MOSFET	Si IGBT	
	C2M0080120D	IKW15N120H3	STGW15M120DF3
Manufacturer	Cree	Infineon	ST
Breakdown voltage	1.2 kV	1.2 kV	1.2 kV
Continuous current	30 A	30 A	30 A
Gate voltage	-5/20 V	±20 V	±20 V
Threshold voltage	3.2 V	5.8 V	6 V
C_{rss}/C_{iss} at 25 V	0.02	0.051	0.038
Gate charge	49.2 nC	75 nC	53 nC

attentions need to be paid during the gate driver development. In addition, the SiC MOSFET needs to be driven at high speed to allow high operating frequency, which tends to aggravate the EMI issues.

From the device output characteristics discussed in previous chapter, the transition from linear region to saturation region of SiC MOSFET is not as clear as that of Si counterpart. Due to the modest transconductance, the transition is spread over a wider range of drain current. As Eq.(4.1) illustrates, the modest transconductance is the result of low inversion channel mobility, which is attributed to the high density of electron traps at the SiC/SiO₂ interface [9].

$$g_m = \frac{\mu_n C_{OX} W}{2L} (V_{GS} - V_T) \quad (4.1)$$

To improve inversion channel mobility by reducing interface traps, the gate oxide is normally annealed in NO ambient [30]. However, the side effect of NO annealing is lower threshold voltage [137]. With the increasing temperature, the decreasing interface traps will further reduce the threshold voltage [138]. From the circuit design point of view, a higher gate voltage is required to improve the transconductance. Normally a +20 V gate voltage is recommended for Cree SiC MOSFET [54]. Although the negative gate voltage is unnecessary for complete turn-off of enhancement-mode FET, it is recommended for better noise immunity due to the lower threshold voltage of SiC MOSFET. As the maximum negative gate bias is only -5 V, an asymmetric gate driving signal is required, unlike the ±15 V typically used in IGBT. Hence for SiC MOSFET, it is not so effective to improve noise immunity by simply using the negative gate bias. In addition, since the threshold voltage shows a negative temperature coefficient, the noise issue will

become more serious at elevated temperature.

The high-speed switching of SiC MOSFET tends to aggravate dv/dt and di/dt effects due to the impact of parasitic parameters, resulting in shoot-through and high device stress in the half bridge configuration. To mitigate the shoot-through issue, an optimized gate driver design is required with the trade-off between the switching speed and switching loss. In this chapter, two kinds of isolated gate drivers for the discrete SiC MOSFET and half bridge SiC power module are developed. Then the impact of various parasitic parameters on gate driver is analyzed and modeled. A novel gate assisted circuit is proposed and experimentally demonstrated to eliminate the parasitic effect and also improve the turn-off speed.

The use of high gate driving voltage and fast rise time in gate driver design results in a rapid current rise at turn-on, which tends to aggravate the short-circuit fault. The existing short-circuit protection strategies include detection of drain current, drain-source voltage (or desaturation detection), current slew rate and gate voltage. However, these schemes suffer from need of extra current sensor, long response time, sensitivity to parasitic inductance or gate voltage noise, respectively. Hence, a novel short-circuit protection scheme for SiC MOSFET is proposed, which is based on gate charge detection. The fundamental analysis for the gate charge of SiC MOSFET under normal and fault conditions is conducted for the first time. By using the proposed circuit simulation model of SiC MOSFET with accurate nonlinear Miller capacitance model, a simulation study is used to verify the function of protection circuit.

4.2 Design of Isolated High-speed Gate Driver

4.2.1 Gate Driver for Single SiC MOSFET

The gate driver for single SiC MOSFET is based on the classical totem-pole configuration, as Figure 4.1 shows. The gate driver IC offers the advantages of lower parasitic inductance and higher density compared with that implemented by discrete devices. In this work, the Avago gate drive optocoupler ACPL-P343 with 35 V wide operating voltage and 4 A peak current is used. It is capable of blocking a continuous peak voltage 891 V (maximum working insulation voltage V_{IORM} according to IEC60747-5-2). The creepage distance is 8 mm and CMRR is 35 kV/ μ s. Since it only has single output terminal, the turn-off diode D_{off} (typically Schottky diode) is used in order to separate the charging/discharging path of

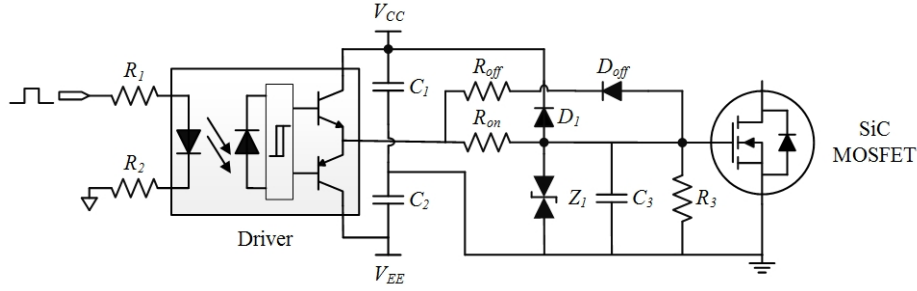


Figure 4.1: Schematic of gate driver for single SiC MOSFET.

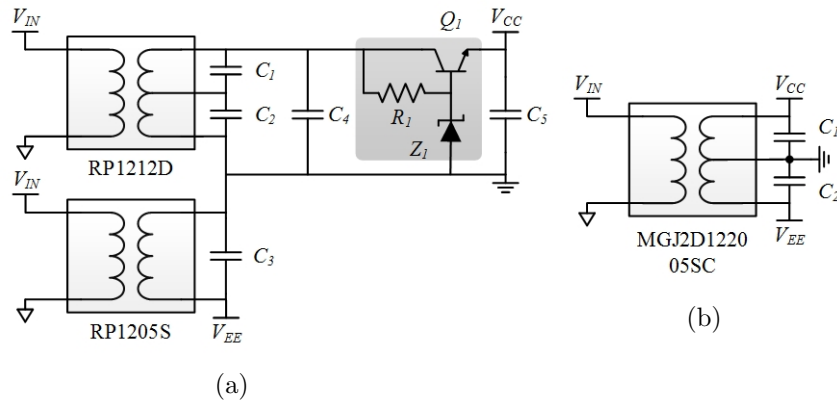


Figure 4.2: Schematic of isolated power supply: (a) Cree gate driver, (b) this work.

gate capacitance. The operating current of the photonic diode in optocoupler is set by the two current limiting resistors R_1 and R_2 . A $10\text{ k}\Omega$ resistor R_3 is recommended to be connected as close as possible between gate and source terminals of transistor. It serves as a pull-down resistor before the power-on of driver board. In addition, an auxiliary gate-source capacitor C_3 is optional in gate driver board. The gate voltage is clamped by Schottky diode D_1 and Zener diode Z_1 to prevent gate oxide breakdown. For a faster response to the voltage overshoot, TVS diode with picosecond response time can be used to replace Zener diode. In order to suppress the EMI issues in high-speed PCB, the bypass capacitors C_1 and C_2 should be put as close as possible to the power pins of IC.

For applications below 600 V , the level shifter with bootstrap power supply is the most commonly used for cost consideration. For higher voltage, individual gate driver with galvanically isolated power supply is preferred for consideration of reliability and switching frequency [139]. The SiC MOSFET gate driver developed

CHAPTER 4. DESIGN OF HIGH-SPEED GATE DRIVER FOR SiC MOSFET

by Cree adopts two magnetically isolated DC/DC converters RP1212D (1 W, 12 V to ± 12 V) and RP1205S (1 W, 12 V to 5 V) from Recom [140], as Figure 4.2(a) shows. The negative output terminal of RP1212D and positive output terminal of RP1205S are connected as the common ground terminal. In order to convert the rail-to-rail ± 12 V from RP1212D to the recommended gate voltage, the Zener regulator with an emitter follower is used as the linear voltage regulator. Since the recommended gate voltage of Cree SiC MOSFET is 20 V [54], a 20 V Zener diode is used. In this work, the complicated isolated power supply aforementioned is replaced by a single isolated DC/DC converter MGJ2D122005SC (2 W, 12 V to 20/-5 V) from Murata, as Figure 4.2(b) shows. It simplifies power supply design, reduces cost and also increases system reliability significantly.

The high dv/dt noise resulted from the fast switching of SiC MOSFET will introduce perturbation to the logic circuits via Miller capacitor and parasitic coupling capacitor, the latter of which is contributed by optocoupler, DC/DC converter and PCB layout. Hence in the layout design, a maximum creepage distance is required to minimize the coupling capacitance. In addition, the parasitic inductance of gate driver output stage should be minimized to reduce the gate voltage ringing. Hence, the gate driver should be put as close as possible to the MOSFET. The laminated layout is further adopted to enhance the coupling effect between

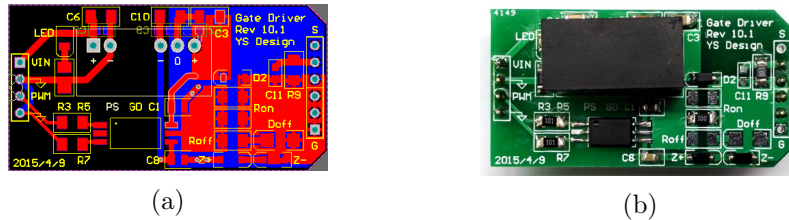


Figure 4.3: Gate driver for single SiC MOSFET: (a) PCB layout, (b) prototype.

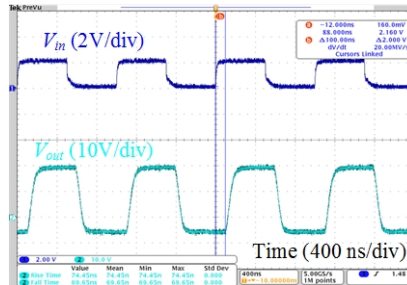


Figure 4.4: Input and output waveforms of gate driver for single SiC MOSFET.

the positive and negative planes so as to reduce the gate stray inductance. The PCB layout and prototype of gate driver for single SiC MOSFET is shown in Figure 4.3. The details for gate inductance extraction will be discussed in Chapter 5.

The dynamic performance of gate driver is tested by subjecting to a 1 MHz, 3.3 V square wave input. The gate driver is connected with a discrete SiC MOSFET C2M0080120, the external gate resistance is 10 Ω . The input and output switching waveforms are shown in Figure 4.4. And the rise time, fall time and propagation delay time are measured to be 74 ns, 70 ns and 100 ns respectively.

4.2.2 Gate Driver for SiC Half Bridge Module

The half bridge gate driver consists of non-isolated/isolated power supply units, logic control unit, signal isolation unit and gate driver unit, as Figure 4.5 shows.

The driver unit can directly inherit its design from the single gate driver unit due to the use of isolated power supply. For a higher driving current capability, the individual IXYS gate driver IC IXD609 with 35 V operating voltage and 9 A peak current is adopted. And the Avago optocoupler ACPL-P484 is used as signal isolation instead of a gate drive optocoupler. Some advanced digital control functions are further introduced in the half bridge gate driver, as Figure 4.6 shows.

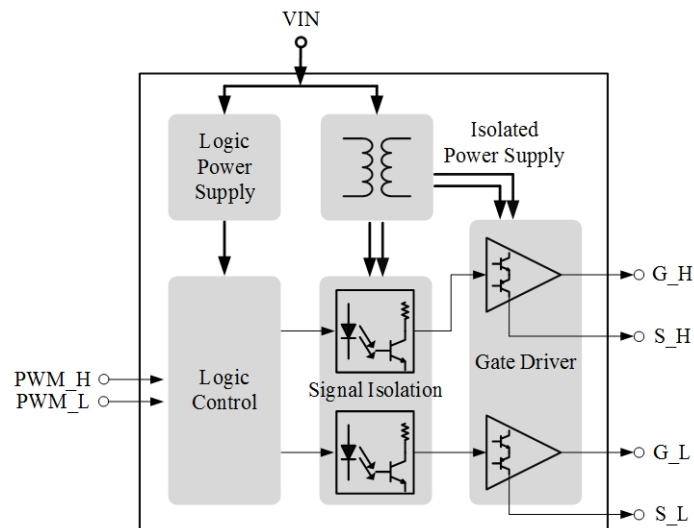


Figure 4.5: Diagram of gate driver for SiC power module.

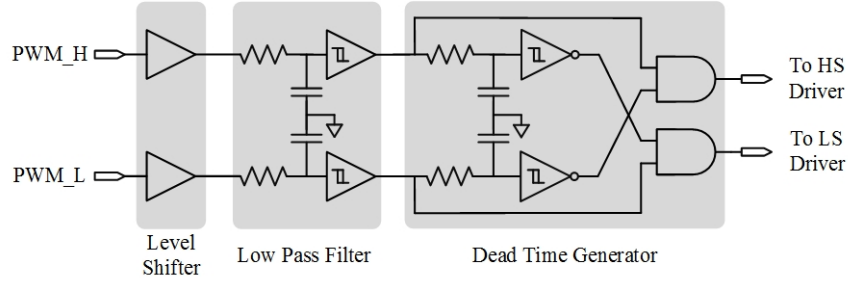


Figure 4.6: Schematic of digital control unit.

Level Shifter: A dual level shifter is firstly adopted as the input stage of half bridge gate driver, which converts the logic 3.3 V from DSP to logic 5 V.

Filter: The low pass filter (LPF) consists of an RC 1st order filter and a dual non-inverting Schmitt trigger. It can suppress the high frequency noise and also limit the maximum operating frequency of gate driver. In this work, the RC constant of LPF is designed to be $1 \mu\text{s}$ ($R = 10 \text{ k}\Omega$ and $C = 100 \text{ pF}$) to suppress any pulse with width below $0.5 \mu\text{s}$.

Dead Time Generator: Since the HS and LS transistors in half bridge can never conduct at the same time, a dead time zone is required for the two complementary gate driver signals. Conventionally, the dead time zone is generated by the microcontroller for cost and space consideration to avoid an extra dead time generation circuit. However, the controller fault or improper dead time design may turn on both HS and LS transistors at the same time, then result in a short-circuit fault. The hardware-based dead time generator completely eliminates the

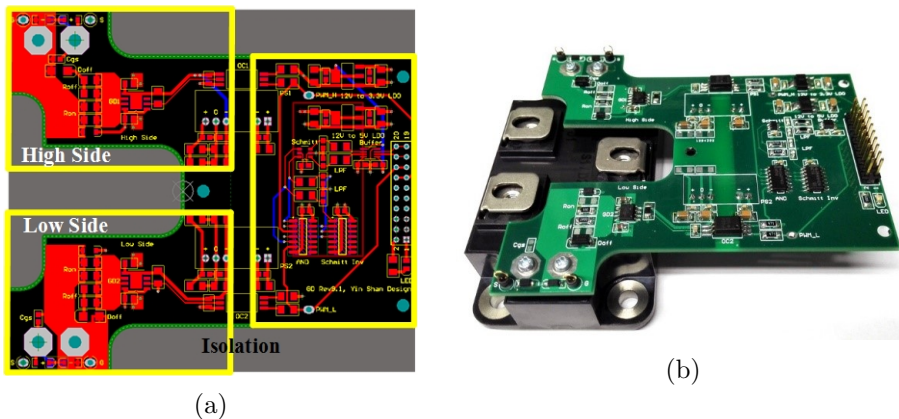


Figure 4.7: Gate driver for SiC power module: (a) PCB layout, (b) prototype.

potential of arm short-circuit, and therefore increases the system reliability. The dead time can still be controlled by microcontroller if it is larger than the RC constant of dead time generator. Hence, the proposed dead time generator is to guarantee a minimum dead time zone and also allows the system flexibility.

To minimize the stray inductance of gate driver loop, a 4-layer PCB of proposed half bridge gate driver is designed to exactly fit the Cree SiC half bridge module CAS100H12AM1. And it is mounted on module by screws, as Figure 4.7 shows.

Two complementary square wave signals with 200 kHz frequency and zero dead time are used to test the dead time function, as Figure 4.8 shows. The RC constant of the dead time generator circuit is designed to be 470 ns ($R = 4.7 \text{ k}\Omega$ and $C = 100 \text{ pF}$). And the experimental waveforms show a dead time of 508 ns.

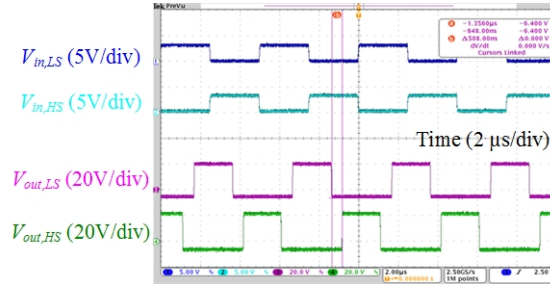


Figure 4.8: Waveforms of dead time generator of gate driver for SiC power module.

The LPF function is verified by subjecting to a pulse signal. The HS driver is clamped off and only the LS driver is tested due to the circuit symmetry. The pulse duration is set to be 500 ns. As Figure 4.9 shows, any pulse within a width of 500 ns from the controller can be completely suppressed.

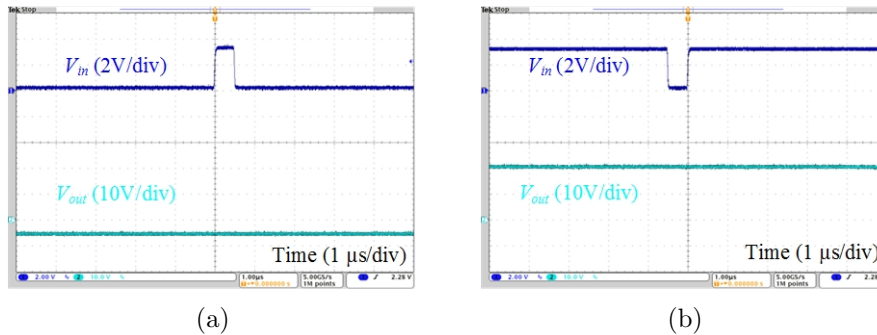


Figure 4.9: Waveforms of low pass filter of gate driver for SiC power module: (a) positive pulse, (b) negative pulse.

The dynamic performance of gate driver is tested by subjecting to a 200 kHz, 3.3 V square wave input. The gate driver is connected with the SiC power module CAS100H12AM1, and the external turn-on and turn-off resistances are 4.3Ω and 10Ω respectively. The input and output switching waveforms are shown in Figure 4.10. And the rise time, fall time and propagation delay time are measured to be 186 ns, 337 ns and 884 ns respectively.

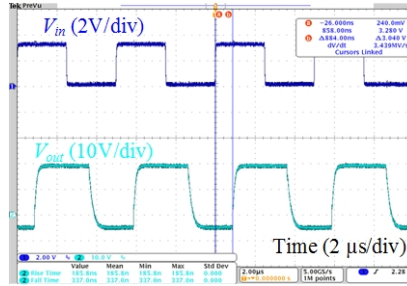


Figure 4.10: Input and output waveforms of gate driver for SiC power module.

4.3 Investigation of Parasitic Parameters on Gate Driver Design

As a unipolar device, SiC MOSFET shows a higher switching speed compared with the bipolar counterpart Si IGBT. However, the increasing dv/dt and di/dt tend to aggravate the switching noise in gate driver due to the effect of parasitic parameters. Considering the lower threshold voltage of SiC MOSFET (2.5 V typically), it is more susceptible to the switching noise. Hence, a new challenge is brought in the high-speed gate driver design to eliminate the parasitic effects without compromise on the high-speed switching advantage of SiC MOSFET.

In half-bridge configuration, the high dv/dt and di/dt during the switching transition of one transistor will affect the complimentary transistor via the Miller capacitance C_{GD} and common source inductance L_{CSI} . C_{GD} is due to the overlap of gate metallization over drift region, while L_{CSI} is the lead shared by gate driver loop and power loop in the packaging. To analyze the effect of these parasitic parameters on switching characteristics, the operation mode of current commutation in the half bridge configuration is discussed firstly, as Figure 4.11 shows.

During the turn-on transition of LS transistor M_L , a voltage ramp occurs across the drain-gate terminals of HS transistor M_H . Then a Cdv/dt current

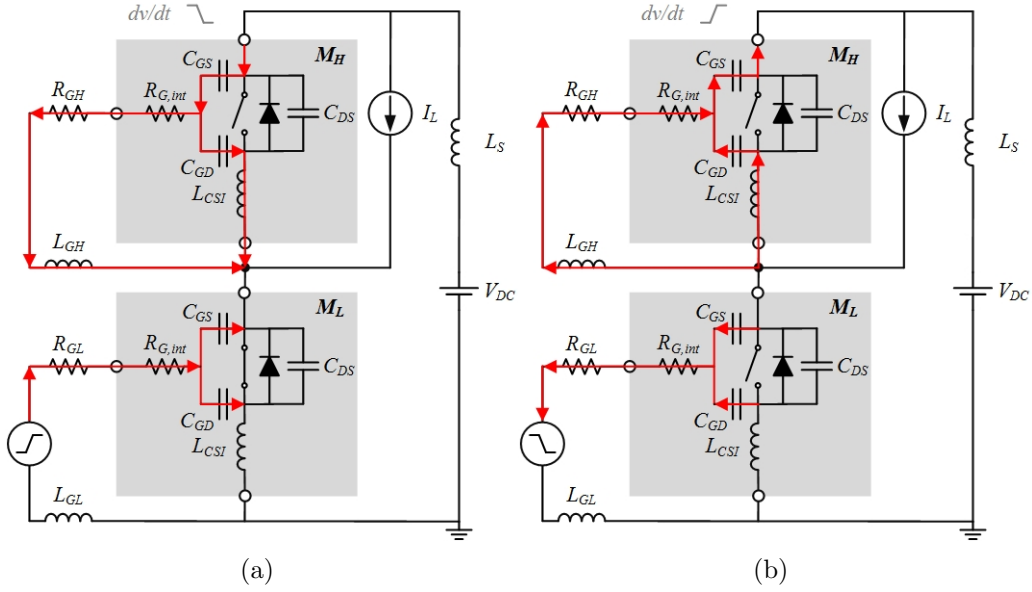


Figure 4.11: Operation mode of the half bridge configuration: (a) turn-on, (b) turn-off.

flows via C_{GD} and gate resistor, resulting a positive voltage drop across gate-source terminals of M_H . In addition, the voltage spike is further aggravated by L_{CSI} . M_H may be faultily turned on if it exceeds the threshold voltage, leading to a momentary arm shoot-through (typically 10~100 ns). It results in an increasing switching loss or even device destruction. Similarly, during the turn-off transition of M_L , a Cdv/dt current is induced by C_{GD} , but in an opposite direction. Hence a negative voltage drop across gate-source terminals of M_H is observed, which brings no adverse side-effect to the switching transition but tends to stress the gate oxide.

A mathematical model for shoot-through analysis in half bridge configuration is developed firstly. During turn-on transition of M_L , the simplified equivalent circuit with consideration of stray inductance is shown by Figure 4.12. Applying KVL, the following equations can be derived

$$v_{DC}(t) = v_{DS}(t) + i_D(t)R_S + L_S \frac{di_D(t)}{dt} + L_{CSI} \frac{di_S(t)}{dt} \quad (4.2)$$

$$v_{DS}(t) = v_{DG}(t) + v_{GS}(t) \quad (4.3)$$

$$i_G(t)R_G + L_G \frac{di_G(t)}{dt} = v_{GS}(t) + L_{CSI} \frac{di_S(t)}{dt} \quad (4.4)$$

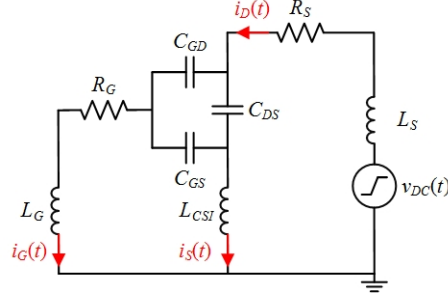


Figure 4.12: Equivalent circuit of half bridge configuration at turn-on.

where R_S is a sum of on-resistance of M_L and the parasitic resistance of converter loop, R_G is a sum of internal and external gate resistances. A constant slew rate of voltage source is assumed, hence $v_{DC}(t)$ is given by

$$v_{DC}(t) = kt \quad (4.5)$$

where k is the dv/dt ratio. In addition, the following equations can be derived after applying KCL

$$i_D(t) = C_{GD} \frac{dv_{DG}(t)}{dt} + C_{DS} \frac{dv_{DS}(t)}{dt} \quad (4.6)$$

$$i_S(t) = C_{GS} \frac{dv_{GS}(t)}{dt} + C_{DS} \frac{dv_{DS}(t)}{dt} \quad (4.7)$$

$$i_G(t) = C_{GD} \frac{dv_{DG}(t)}{dt} - C_{GS} \frac{dv_{GS}(t)}{dt} \quad (4.8)$$

In order to derive the close form expression of $v_{GS}(t)$, some approximation needs to be made. Since the nonlinear C_{GD} will decrease significantly when subjected to high reverse bias, it is reasonable to assume a constant C_{GD} and $C_{GD} \ll C_{DS}$. In addition, after considering $v_{GS}(t) \ll v_{DS}(t)$, Eq.(4.6) and (4.7) can be simplified as

$$i_D(t) \approx i_S(t) \approx C_{DS} \frac{dv_{DS}(t)}{dt} \quad (4.9)$$

Combining Eq.(4.2) and (4.9) after applying Laplace transform, $v_{DS}(s)$ at the frequency-domain can be derived

$$v_{DS}(s) = \frac{1}{s^2(L_S + L_{CSI})C_{DS} + sR_S C_{DS} + 1} v_{DC}(s) \quad (4.10)$$

CHAPTER 4. DESIGN OF HIGH-SPEED GATE DRIVER FOR SIC
MOSFET

The converter loop is an RLC second order system with the resonant frequency given by

$$f = \frac{1}{2\pi\sqrt{(L_S + L_{CSI})C_{DS}}} \quad (4.11)$$

Combining Eq.(4.4), (4.8) and (4.9) after applying Laplace transform, $v_{GS}(s)$ at the frequency-domain can be derived

$$v_{GS}(s) = \frac{s^2(L_G C_{GD} - L_{CSI} C_{DS}) + s R_G C_{GD}}{s^2 L_G (C_{GS} + C_{GD}) + s R_G (C_{GS} + C_{GD}) + 1} v_{DS}(s) \quad (4.12)$$

The damping factor of the driver loop is given by

$$\xi = \frac{R_G}{2} \sqrt{\frac{C_{GS} + C_{GD}}{L_G}} \quad (4.13)$$

As a rule of thumb in gate driver design, the gate inductance should be minimized and a large enough gate resistance is normally selected to damp the ringing.

Table 4.2: Parameters for evaluation of gate-source voltage spike.

Parameter	Value
C_{GS}	6.263 nF
C_{GD}	37 pF
C_{DS}	843 pF
R_G	11.8 Ω
L_{CSI}	2 nH
L_S	20 nH
R_S	0.1 Ω

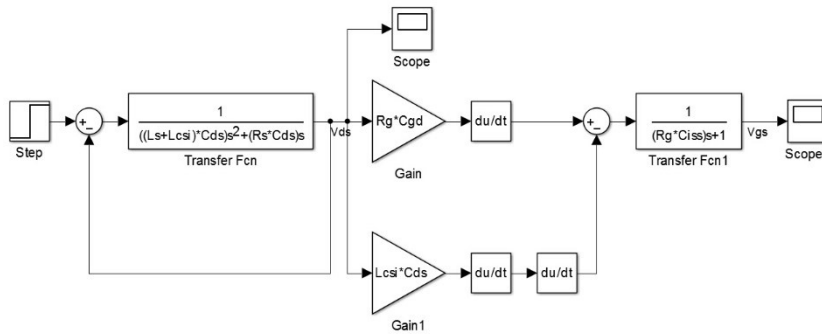


Figure 4.13: Transfer function block.

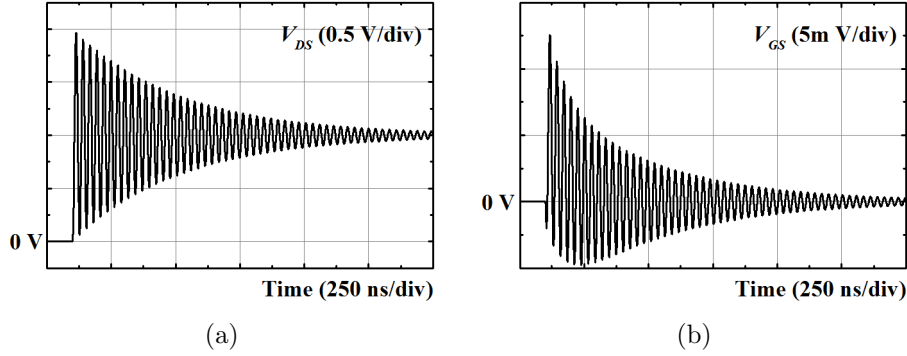


Figure 4.14: Output waveforms of transfer function block: (a) drain-source voltage, (b) gate-source voltage.

Hence, the effect of L_G can be neglected and Eq.(4.12) can be simplified as

$$v_{GS}(s) = \frac{-s^2 L_{CSI} C_{DS} + s R_G C_{GD}}{s R_G (C_{GS} + C_{GD}) + 1} v_{DS}(s) \quad (4.14)$$

The transfer function block of Eq.(4.10) and (4.14) is built in Simulink with a step function stimulus, as Figure 4.13 shows. The parasitic capacitances are taken from the datasheet at 1 kV, and an external gate resistor 10Ω is used with an internal gate resistor 1.8Ω . The list of parasitic parameters is given by Table 4.2. From the output waveforms shown by Figure 4.14, the voltage spike and ringing are observed across the gate-source terminals of M_H . Applying fast Fourier transform (FFT) to both waveforms, the resonant frequency of driver loop is 37 MHz, which is identical as that of converter loop, as Eq.(4.11) illustrates.

To further evaluate the effect of stray inductance, an AC sweep simulation is conducted in PSpice, as Figure 4.15 shows. A pulse function with a constant dv/dt of 15 V/ns at turn-on is used as the stimulus. Meanwhile, the converter loop inductance maintains at a constant value of 22 nH regardless of variation of L_{CSI} . From the simulation results in both frequency and time domains shown by Figure 4.16, the resonant frequency and magnitude of ringing are dominated by L_{CSI} . By comparison, L_G has a rather insignificant influence on the ringing [141]. Substituting $R_G = 11.8 \Omega$ and $L_G = 20$ nH into Eq.(4.13), ξ is equal to 3.3 and the driver loop is over-damping obviously. However, ringing of gate voltage and current can still be observed regardless of the damping factor. Hence, it is concluded that the ringing of driver loop is due to the feedback effect of L_{CSI} . It is crucial to reduce the length of sharing trace between converter loop and driver

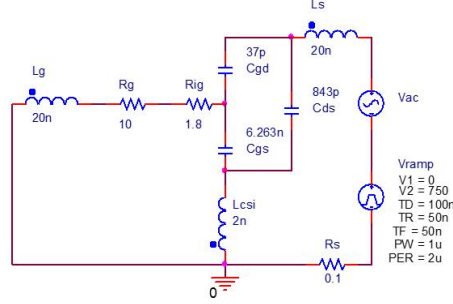


Figure 4.15: Schematic of AC sweep simulation in PSpice.

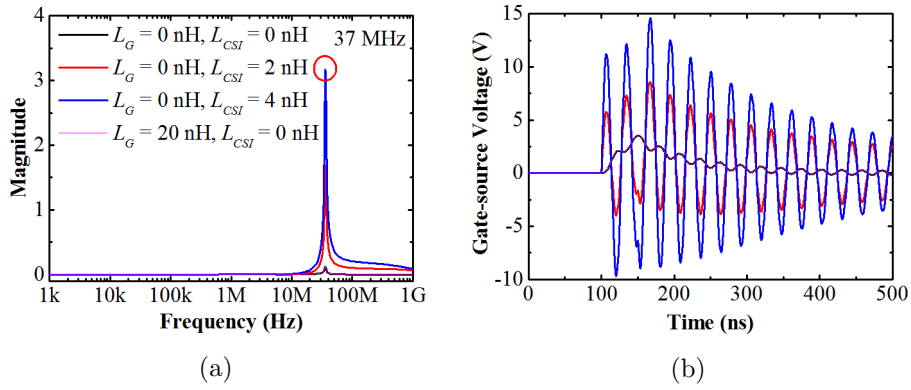


Figure 4.16: Response of gate-source voltage of HS transistor to dv/dt : (a) frequency domain, (b) time domain.

loop by using of Kelvin source inside the package.

Neglecting all the stray inductances and combining Eq.(4.5) after applying Laplace transform, $v_{GS}(s)$ can be further simplified as

$$v_{GS}(s) = \frac{k \frac{C_{GD}}{(C_{GS} + C_{GD})}}{s \left[s + \frac{1}{R_G(C_{GS} + C_{GD})} \right]} = \frac{k \frac{C_{rss}}{C_{iss}}}{s \left(s + \frac{1}{R_G C_{iss}} \right)} \quad (4.15)$$

Applying inverse Laplace transform, the time-domain relationship is given by

$$v_{GS}(t) = k R_G C_{rss} \left[1 - \exp \left(-\frac{t}{R_G C_{iss}} \right) \right] \quad (4.16)$$

The gate-source voltage spike ΔV_{GS} is obtained at the end of drain voltage ramp

$$\Delta V_{GS} = k R_G C_{rss} \left[1 - \exp \left(-\frac{V_{DC}}{k R_G C_{iss}} \right) \right] \quad (4.17)$$

For the ideal situation, R_G becomes 0, and shoot-through is non-existing. For the worst situation, R_G becomes infinity and ΔV_{GS} can be approximated by

$$\lim_{R_G \rightarrow \infty} \Delta V_{GS} = \frac{C_{rss}}{C_{iss}} V_{DC} \quad (4.18)$$

For the complementary situation of turn-off transition, ΔV_{GS} is negative of Eq.(4.18). Based on the discussions above, the shoot-through issue can be mitigated by smaller gate resistance, smaller C_{rss}/C_{iss} ratio or negative bias.

4.4 A Novel Gate Assisted Circuit to Reduce Switching Loss and Eliminate Cdv/dt Effect

To eliminate Cdv/dt Effect in the half bridge configuration, from the aspect of device design, the Miller capacitance can be reduced by using smaller polysilicon gate width [142]. From the aspect of circuit design, there are four commonly used solutions: 1) negative power supply, 2) auxiliary gate-source capacitor, 3) turn-off diode, 4) active Miller clamp [140, 143–148].

By using of the negative power supply, the off-state gate-source voltage is directly shifted by a negative value to create a wide margin between the off-state and threshold voltages. It is most effective but costly, since the cost of isolated power supply is considerable. Hence, the AC-coupled gate driver with RCD (resistor-capacitor-diode) components was proposed to replace the use of negative power supply [148]. However, the maximum negative gate voltage of SiC MOSFET is only -5 V due to the limitation of gate oxide reliability [54]. Hence, the negative bias cannot exceed -5 V and the outcome is limited.

The auxiliary capacitor is parallel with the gate-source terminals of transistor. It increases the effective input capacitance so as to suppress the gate voltage spike. However, it slows down the switching speed and increases the switching loss.

The turn-off diode is a simple strategy to achieve shoot-through mitigation as well as turn-off speed enhancement. However, both the turn-off current and Cdv/dt current still need to flow through the output impedance of gate driver [149]. Hence, for the gate driver IC with high output impedance, the outcome of turn-off diode is limited.

The active Miller clamp introduces a local low impedance path for the Cdv/dt current. It is initially proposed to eliminate the need of negative power supply. It can be integrated inside the gate driver IC [68] and is available in lots of

commercial off-the-shelf products [150]. However, due to the internal gate resistor inside the package of SiC power MOSFET and module, the active Miller clamp is no longer suitable for this application. Hence, the improved active Miller clamp circuits were proposed by early works.

In [144], a gate assisted circuit (GAC) was proposed for quick and stable driving of SiC JFET in a three-phase inverter, which utilized a PNP transistor and an auxiliary capacitor. And this circuit is active only when the main transistor is off, so as to avoid the influence on the normal turn-on process. However, as the reverse breakdown voltage of base-emitter junction of PNP transistor is normally below 10 V, it cannot be directly used in SiC MOSFET, whose recommended gate-source voltage reaches up to 20 V. Replacement of PNP with NMOS makes this kind of circuit practical for use in SiC MOSFET [146], since the maximum gate-source voltage of NMOS can be as high as 25 V. However, the gate driver with complementary outputs are required, since the logic of auxiliary NMOS is inverse to the main transistor.

A novel GAC to mitigate shoot-through in SiC half bridge module is proposed, which solve the issues in [144] and [146]. As Figure 4.17(a) shows, it consists of an auxiliary PMOS transistor M_A , an auxiliary capacitor C_A , a gate resistor R_{AG} and a diode D_A . The gate resistor damps the gate signal oscillation of auxiliary transistor. The Schottky diode paralleling with the auxiliary capacitor is optional, which clamps the capacitor voltage. It also makes the GAC adaptable to gate driver without negative power supply. Due to the use of PMOS transistor, the auxiliary transistor can share the same gate driving voltage with the main transistor, which simplifies the gate driver circuit significantly. The 30 V, 8.8 A, 20 m Ω P-channel trench MOSFET FDS4435BZ from Fairchild Semiconductor is used as the auxiliary transistor. The peak value of V_{GS} is ± 25 V, which has enough

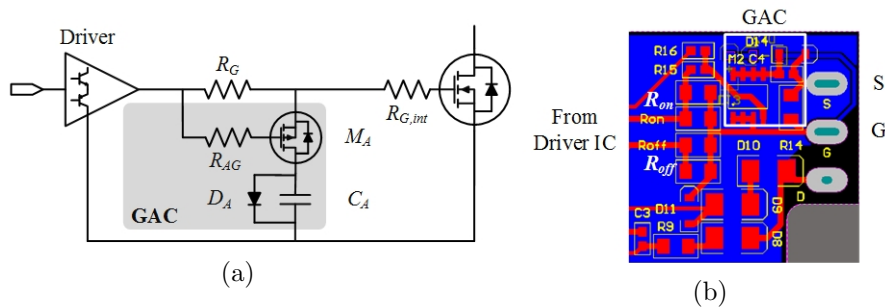


Figure 4.17: Gate assisted circuit: (a) schematic, (b) PCB layout.

margin for application in SiC MOSFET. In addition, inside the SO-8 package, a pair of Zener diodes is internally parallel with the PMOS die to prevent breakdown of gate oxide. During hardware implement, the GAC should be put as close as possible to the main transistor to minimize the loop inductance, as Figure 4.17(b) shows.

Neglecting the stray inductances, the equivalent circuit with the proposed GAC is shown by Figure 4.18. A constant slew rate of drain-source voltage across M_H is assumed. Similar to the previous discussion, the following equations can be derived after applying KVL

$$v_{DS}(t) = v_{DG}(t) + v_{GS}(t) = kt \quad (4.19)$$

$$v_{GS}(t) = v_A(t) + R_G C_A \frac{dv_A(t)}{dt} \quad (4.20)$$

where $v_A(t)$ is the voltage drop across C_A . And the following equations can be derived after applying KCL

$$C_{GD} \frac{dv_{DG}(t)}{dt} = C_A \frac{dv_A(t)}{dt} + C_{GS} \frac{dv_{GS}(t)}{dt} \quad (4.21)$$

Applying Laplace transform to Eq.(4.19)~(4.21), $v_{GS}(s)$ at the frequency-domain can be derived

$$v_{GS}(s) = \frac{k \frac{C_{rss}}{C_{iss}} \left(s + \frac{1}{R_G C_A} \right)}{s^2 \left(s + \frac{C_{iss} + C_A}{R_G C_{iss} C_A} \right)} \quad (4.22)$$

Applying inverse Laplace transform, the time-domain relationship is derived

$$v_{GS}(t) = \frac{k C_{rss}}{C_{iss} + C_A} t + \frac{k R_G C_{rss} C_A^2}{(C_{iss} + C_A)^2} \left[1 - \exp \left(-\frac{C_{iss} + C_A}{R_G C_{iss} C_A} t \right) \right] \quad (4.23)$$

The peak gate-source voltage is also obtained at the end of drain voltage ramp.

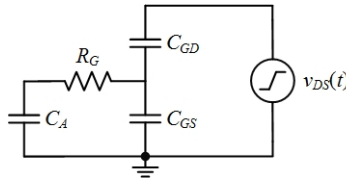


Figure 4.18: Equivalent circuit with proposed gate assisted circuit.

After considering the initial voltage V_{EE} on C_A , it is given by

$$V_{GS,pk} = V_{EE} \pm \frac{C_{rss}}{C_{iss} + C_A} V_{DC} \pm \frac{kRC_{rss}C_A^2}{(C_{iss} + C_A)^2} \left[1 - \exp\left(-\frac{C_{iss} + C_A}{kRC_{iss}C_A} V_{DC}\right) \right] \quad (4.24)$$

where the +/- symbol is for turn-on/off transition.

4.4.1 Operating Principle of Proposed Gate Assisted Circuit

The operation principle of GAC is discussed by Figure 4.19. It is assumed only M_L is active, which means M_H is always off and M_{AH} is always on. For the complementary situation when M_H is active, it behaves in a similar way. The stray inductance of PCB layout and packaging is neglected. The switching time of auxiliary transistors are neglected, as C_{iss} of auxiliary transistor is much smaller than that of main transistor. The switching waveforms of the gate-source voltage of main transistor, auxiliary capacitor voltage and current are shown by Figure 4.20.

Subinterval $t_0 \sim t_1$: M_L is turned on and M_{AL} is off, which has no influence on the normal turn-on process of M_L . The common terminal between M_H and M_L is now pulled down to ground. Then a sudden voltage ramp occurs across the drain-source terminals of M_H . M_{AH} provides a low impedance path for the Cdv/dt current induced by Miller capacitance. Since the initial voltage on C_{AH} (V_{CAH} in Figure 4.20) is negative, C_{AH} is discharged and the potential increases. Then $V_{GS,HS}$ is a sum of voltage drops across $R_{G,int}$, M_{AH} on-resistance $R_{DS,on}$ and C_{AH} . The small positive voltage drop across M_{AH} and the negative potential on C_{AH} help to mitigate shoot-through. The auxiliary Schottky diode is optional for the extreme situation when the potential on C_{AH} rises beyond zero, hence C_{AH} is clamped to avoid a floating positive potential. This period lasts until $V_{GS,LS}$ is fully pulled up to V_{CC} and M_L is fully turned on.

From Eq.(4.24), the voltage spike of $V_{GS,HS}$ can be mitigate by a large auxiliary capacitance. To reach the optimized design, the relationship between the voltage spike and auxiliary capacitance needs to be derived. Due to the nonlinear property of Miller capacitance, two extreme situations are assumed with small capacitance at high bias (0.037 nF at 750 V) and large capacitance at low bias (600 pF at 10 V) to simplify the analytical model. A high dv/dt of 750 V/50 ns is assumed. And other parameters are given by Table 4.2. From the computational results shown by Figure 4.21, $V_{GS,pk}$ is far below the threshold voltage of SiC

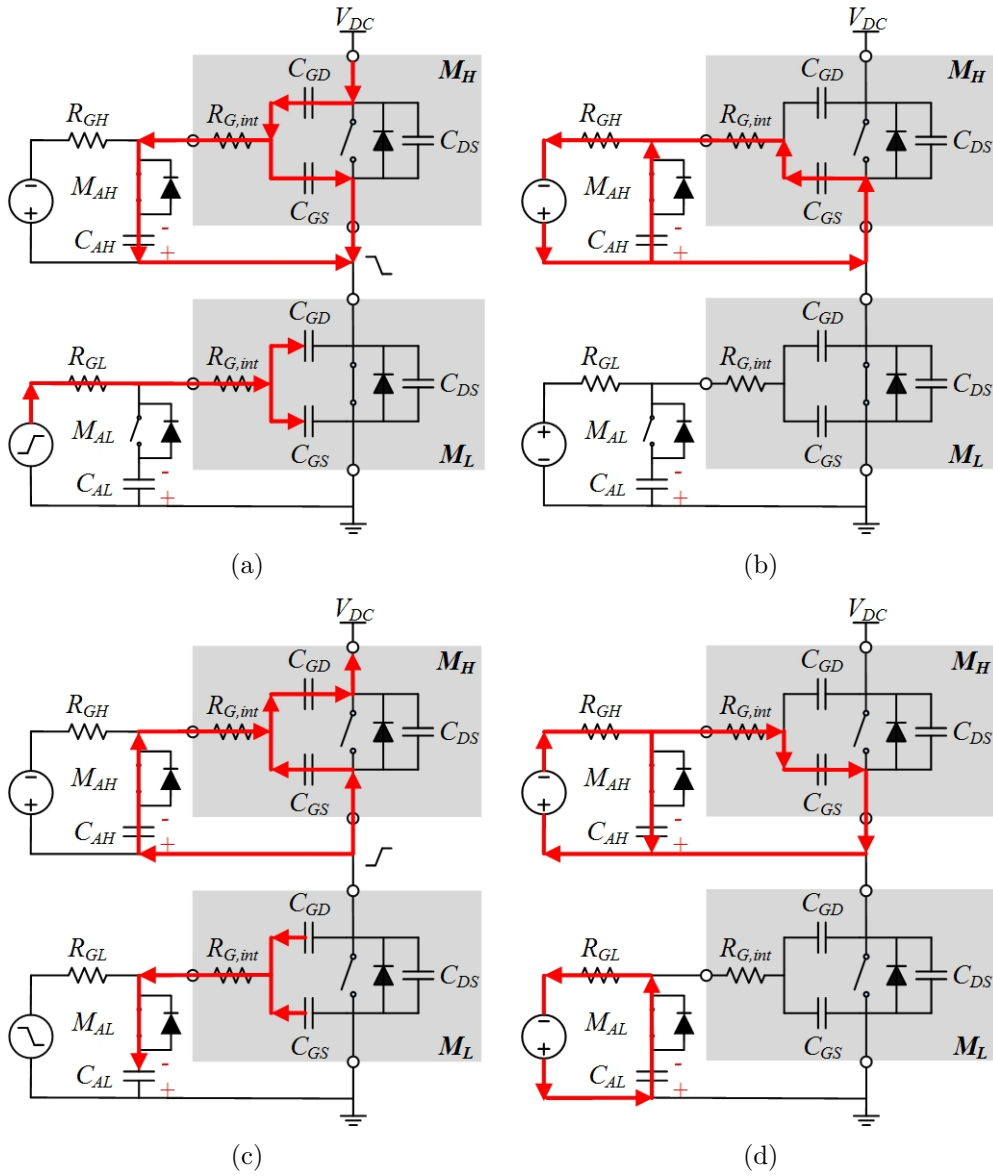


Figure 4.19: Operation principle of GAC, (a) subinterval $t_0 \sim t_1$, (b) subinterval $t_1 \sim t_2$, (c) subinterval $t_2 \sim t_3$, (d) subinterval $t_3 \sim t_4$.

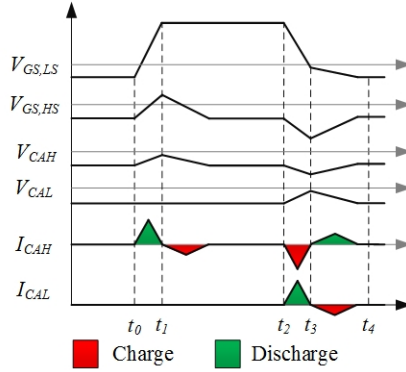


Figure 4.20: Switching waveforms of gate-source voltage, auxiliary capacitor voltage and current.

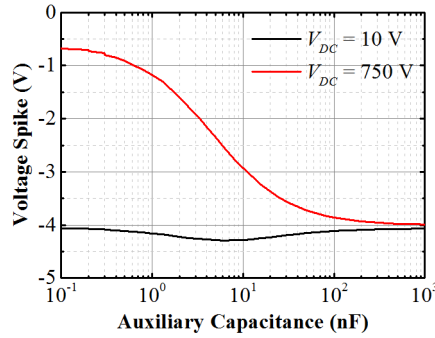


Figure 4.21: Impact of auxiliary capacitance on gate-source peak voltage.

MOSFET with the proposed GAC. For high bias assumption, the voltage spike can be significantly reduced when the auxiliary capacitance is large enough. And the decreasing tendency will become insignificant when the auxiliary capacitance is above 100 nF. For low bias assumption, there will be an optimized value for the auxiliary capacitance, which is close to the input capacitance. And this voltage spike is much lower than the assumption of high bias.

Subinterval $t_1 \sim t_2$: M_L is in on and M_{AL} is still off. The negative power supply starts to charge C_{AH} via R_{GH} and channel of M_{AH} until it is completely charged to V_{EE} . Meanwhile, C_{GS} of M_H is also charged via R_{GH} . This period lasts until M_L is turned off.

Subinterval $t_2 \sim t_3$: M_L is turned off while M_{AL} is on. A low impedance path is provided for the discharging current of M_L and the turn-off speed is improved. C_{AL} is discharged and the potential increases (V_{CAL} in Figure 4.20). Meanwhile, a Cdv/dt current is induced by Miller capacitance similar to subinterval $t_0 \sim t_1$,

but in an opposite direction. Hence, C_{AH} is charged and the potential further decreases. To estimate the value of C_{AL} , an ideal assumption is made that all the positive charge on C_{iss} of M_L is neutralized by the negative charge on C_{AL} . Hence C_{AL} should hold enough negative charge to make sure the potential always below zero during this period. According to the charge balance equation

$$C_{AL}V_{EE} + C_{iss}V_{CC} < 0 \quad (4.25)$$

Considering $V_{EE} = -5$ V and $V_{CC} = 20$ V, C_{AL} should be at least 4 times of C_{iss} . C_{AH} is same as C_{AL} due to the circuit symmetry. Considering the effect of C_{AH} on the voltage spike, a 100 nF, 50 V ceramic capacitor is selected as the auxiliary capacitor, which has enough capability for shoot-through mitigation as well as turn-off enhancement. During this period, M_{AL} mainly acts as a speed-enhancement device. Considering the threshold voltage of PMOS, it becomes less effective as $V_{GS,LS}$ gradually approaches V_{EE} . And the discharging current starts to flow through R_{GL} . This transition only occurs after $V_{GS,LS}$ is already below zero, hence the turn-off speed is unaffected actually. This period lasts until $V_{GS,LS}$ is fully pulled down to V_{EE} and M_L is fully turned off.

Subinterval $t_3 \sim t_4$: both M_H and M_L are off, which is the dead zone for half-bridge configuration. Meanwhile, both M_{AH} and M_{AL} are on. As the potential on C_{AH} is below V_{EE} after the previous subinterval, it is discharged via R_{GH} and M_{AH} . And $C_{GS,HS}$ is charged by the negative power supply via R_{GL} and M_{AL} .

4.4.2 Experimental Verification

A double pulse testing (DPT) experiment is set up to test the performance of GAC. More details for the experimental setup of DPT will be discussed in Chapter 6. The comparison between the conventional gate driver with $R_{on} = R_{off} = 10 \Omega$ and proposed gate driver with GAC is shown in Figure 4.22. The turn-off speed of M_L is significantly improved with GAC. As Figure 4.23 shows, the turn-off loss of proposed gate driver with GAC almost keeps constant with load current increasing. By comparison, the turn-off loss of conventional gate driver increases significantly. For the normal turn-on process, it is totally unaffected, since M_{AL} is off during this period. And it allows a 34% reduction of total switching loss at 100 A, as Table 4.3 illustrates.

The dv/dt and di/dt ratios for both conventional and proposed gate drivers

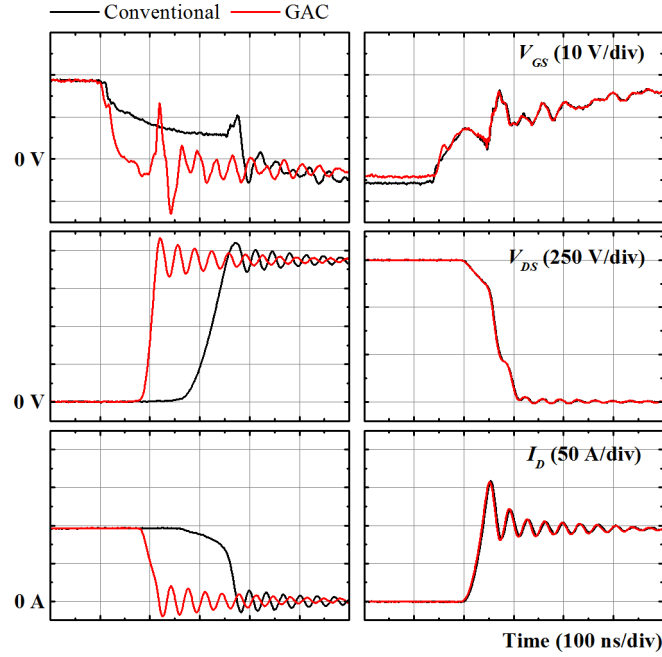


Figure 4.22: Switching characterizations of conventional gate driver and proposed gate driver with gate assisted circuit.

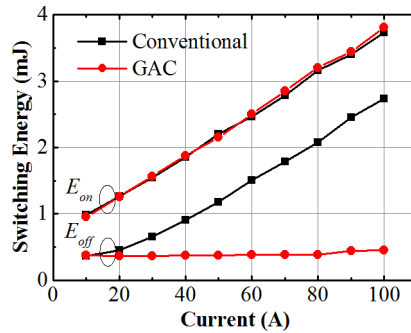


Figure 4.23: Switching loss versus load current at 750 V with conventional and proposed gate drivers.

are summarized in Table 4.4. The increasing di/dt with GAC introduces an increasing voltage overshoot (115 V) compared with the conventional (90 V). And the voltage overshoot will be reduced significantly to 75 V if removing the CT. Hence, the proposed GAC permits the maximum turn-off speed with acceptable voltage overshoot issue.

The EMI spectra (500 kHz~1 GHz) is obtained by applying FFT on the

CHAPTER 4. DESIGN OF HIGH-SPEED GATE DRIVER FOR SIC
MOSFET

Table 4.3: Switching loss at 750 V and 100 A with conventional and proposed gate drivers.

Parameter	Unit	Conventional	GAC
E_{off}		2.73	0.45
E_{on}	mJ	3.73	3.81
E_{tot}		6.46	4.26

Table 4.4: dv/dt and di/dt at 750 V and 100 A with conventional and proposed gate drivers.

Parameter	Unit	Conventional		GAC	
		Turn-on	Turn-off	Turn-on	Turn-off
dv/dt	V/ns	20	11	20	31
di/dt	A/ns	4.2	3.6	4.2	4.2

experimental waveforms, as Figure 4.24 shows. The higher dv/dt and di/dt ratios with GAC at turn-off leads to a slightly increased EMI effect. In addition, it is found that the gate driver loop shows the same resonant frequency of 29 MHz as power converter loop. It is because the voltage ringing of converter loop can be coupled into driver loop via L_{CSI} as aforementioned.

The waveforms of LS and HS gate voltage are measured to evaluate the shoot-through possibility. The CT is removed since the current measurement is unnecessary in this step. And the complementary gate signals are applied to LS and HS transistors. As Figure 4.25 shows, during the turn-off transition of LS transistor, the gate voltage across LS transistor shows more serious ringing due to the extremely fast turn-off speed. However, it brings no side-effect of shoot-through due to the dead time. During the turn-on transition of LS transistor, an obvious gate voltage spike across HS transistor is observed for the conventional gate driver, which already exceeds the threshold voltage. By comparison, the gate voltage spike with proposed GAC is far below threshold voltage. Hence, the shoot-through issue can be completely eliminated.

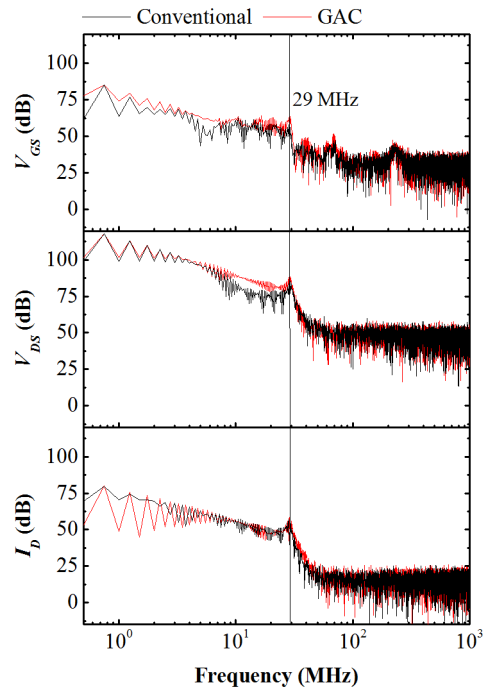


Figure 4.24: EMI spectra of switching waveforms with conventional and proposed gate drivers.

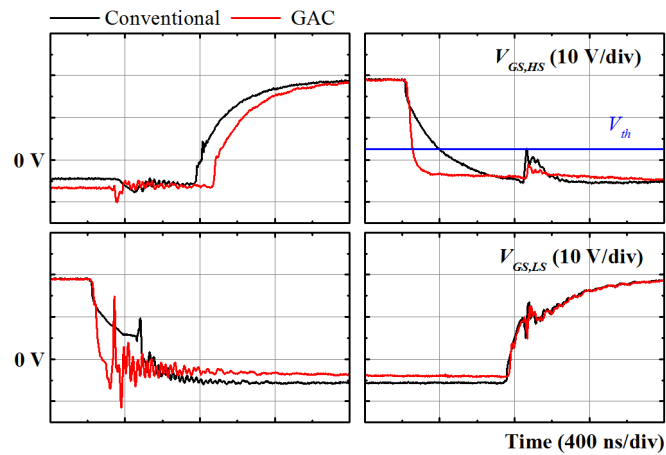


Figure 4.25: Effect of gate assisted circuit on shoot-through mitigation.

4.5 Short-circuit Protection Circuit with Gate Charge Detection

In this section, a novel short-circuit protection scheme based on gate charge detection is proposed. Under short-circuit conditions, the drain-source voltage drop is larger than that under normal operation, and the Miller capacitor becomes smaller due to the expansion of depletion layer beneath the gate oxide. Hence the gate charge also decreases. As a consequence, it is theoretically practical to detect the short-circuit fault by means of gate charge.

The protection circuits in [151, 152] introduces a current mirror integrated inside gate driver IC to detect the gate current, which is accumulated by a capacitor to get the gate charge. It requires a specially designed driver IC and is hard to implement by discrete components. The circuit in [153] uses the gate resistor as current sensor. The voltage across the resistor is detected by a differential amplifier, then followed by an integrator to get the gate charge. It is later experimentally verified in [154, 155] for both HSF and FUL conditions. Even though implemented by discrete components, it is also practical to be integrated in the driver IC. All the early works focused on short-circuit protection for Si IGBT, and have shown a fastest response time within 1 μ s. It is attractive to investigate the use of gate charge detection in SiC MOSFET protection.

4.5.1 Fundamentals of Gate Charge Detection

A. Normal Condition

A detailed discussion of normal turn-on condition has been conducted in Chapter 2. Generally, the total gate charge Q_G required to turn on the MOSFET during normal operation will result in the voltage drop across C_{GS} rising from V_{EE} to V_{CC} , and the voltage drop across C_{GD} rising from $V_{EE} - V_{DC}$ to V_{CC} (the on-state drain-source voltage drop $V_{DS,on}$ is neglected). Hence, the gate charge can be derived by the initial and final states of gate capacitors.

$$Q_{GS} = C_{GS} (V_{CC} - V_{EE}) \quad (4.26)$$

$$Q_{GD} = C_{ox} V_{CC} + \int_0^{V_{DC}-V_{EE}} C_{GD} (v_{DS}) dv_{DS} \quad (4.27)$$

B. HSF Condition

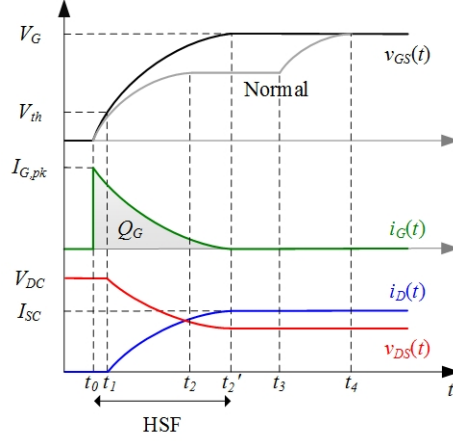


Figure 4.26: Switching waveforms under normal and HSF conditions.

The transistor is subjected to HSF condition with the DC-bus voltage directly across the device. Under HSF condition, the turn-on transition analysis is much more straightforward due to disappearance of Miller plateau. As Figure 4.26 shows, v_{GS} rises exponentially until finally reaching V_G , and i_G falls towards 0 with the same time constant. Once v_{GS} exceeds V_{th} , i_D starts to rise towards the short-circuit current I_{SC} . Meanwhile, v_{DS} falls slightly due to the voltage drop on the parasitic resistive components. Hence, after considering the asymmetric positive/negative power supply V_{CC}/V_{EE} of gate driver, the voltage drop across C_{GS} rises from V_{EE} to V_{CC} , and the voltage drop across C_{GD} rises from $V_{EE} - V_{DC}$ to $V_{CC} - V_{DS,on}$ (here $V_{DS,on}$ becomes no longer negligible). Q_{GS} is still same as that of normal condition, but Q_{GD} decreases, as given by

$$Q_{GD,HSF} = \int_{V_{DS,on} - V_{CC}}^{V_{DC} - V_{EE}} C_{GD}(v_{DS}) dv_{DS} \quad (4.28)$$

C. FUL Condition

As Figure 4.27 shows, before the occurrence of FUL condition, the converter operates normally. Once subjected to FUL condition at t_5 , v_{DS} starts to rise rapidly. Due to the voltage ramp across the LS transistor, a Cdv/dt current will flow via the Miller capacitor and gate resistor, leading to the gate voltage overshoot. The extra gate voltage plus V_G results in a higher surge current than that of HSF condition. As the direction of Cdv/dt current is opposite to the gate charging current, it will discharge the gate capacitor and reduce the gate charge.

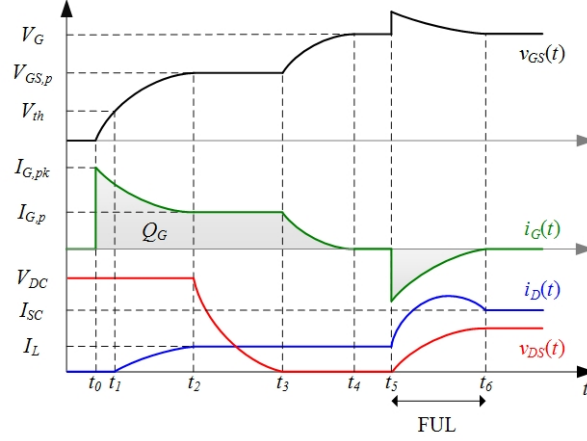


Figure 4.27: Switching waveforms under FUL condition.

Finally v_{DS} will reach a voltage slightly below V_{DC} due to the voltage drop on the parasitic resistive components, and i_D restores to I_{SC} . Since the final state of FUL condition is same as that of HSF condition, the gate charge under HSF and FUL conditions should have the same value.

$$Q_{GD,FUL} = Q_{GD,HSF} \quad (4.29)$$

4.5.2 Operating Principle of Protection Circuit

The proposed short-circuit protection circuit can be divided into the following three fundamental circuit blocks: gate charge detection, fault decision and turn-off circuit, as Figure 4.28 shows.

The gate charge detection block consists of a differential amplifier, an integrator and a comparator. The voltage drop across R_{G2} is detected by the differential amplifier. Due to the high impedance of OPAMP, the normal operation of gate driver is unaffected.

$$v_b - v_a = i_G(t) R_{G2} \quad (4.30)$$

The integration of differential voltage with time is calculated by the following integrator, with the output voltage V_{QG} given by

$$V_{QG} = \frac{R_{G2}}{R_5 C_1} \int i_G(t) dt = \frac{R_{G2}}{R_5 C_1} Q_G \quad (4.31)$$

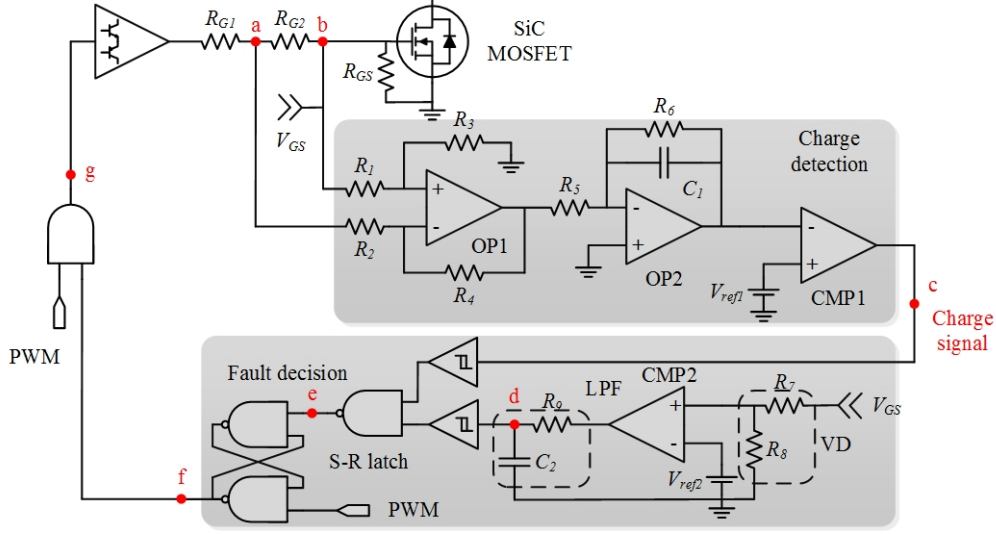


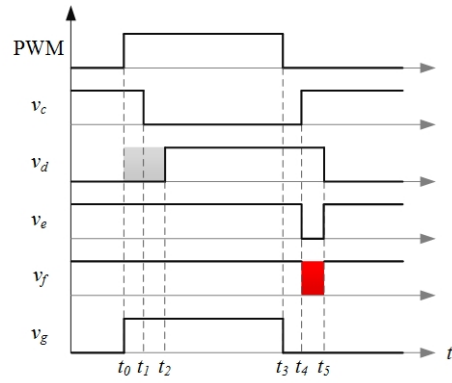
Figure 4.28: Schematic of proposed short-circuit protection circuit.

Here an additional resistor R_6 is parallel with the integrator capacitor to offset the gate leakage current, which is induced by the gate-source pull-down resistor R_{GS} and protection circuit. Or else the integrator output voltage will keep increasing slightly with time and finally lead to fault triggering.

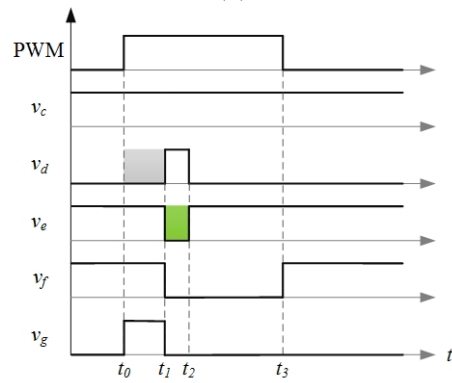
The charge signal v_c after CMP1 cannot be directly used to decide short-circuit fault, since it is also logic 1 when the MOSFET is in turn-on transition, turn-off transition and off-state. Fortunately, the protection circuit has no influence on normal turn-off transition and off-state. Hence, a fault decision circuit is to ensure the protection circuit will only perform during on-state, in which the gate voltage is used as reference signal.

A voltage divider (VD) is first used to scale down the gate voltage to within 5 V. Since the gate voltage is as high as 20 V, a scale-down gate voltage allows a lower reference voltage and a simplified power supply design. A reference voltage $V_{ref2} = 4.5$ V is set, so that only when the scale-down gate voltage is above V_{ref2} the MOSFET is treated as full on-state. The gate voltage rings induced by the high switching speed of SiC MOSFET may cause fault triggering of protection circuit. The noise during turn-on transition is suppressed by a RC LPF. With the pre-processing circuit for reference signal, the stability and noise immunity of the fault detection circuit can be significantly improved.

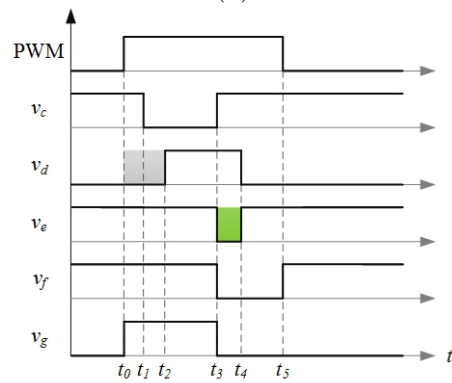
The operating principle of the digital control unit of short-circuit protection circuit is discussed by the sequence diagrams shown in Figure 4.29. And the delay



(a)



(b)



(c)

Figure 4.29: Sequence diagrams of digital control unit: (a) normal condition, (b) HSF condition, (c) FUL condition.

time introduced by the digital components is neglected.

During normal condition, V_{QG} is higher than V_{ref1} and v_c becomes logic 0 at t_1 . v_d can be treated as delay of the PWM control signal. The grey shadowed area between t_0 and t_2 is the blanking time to avoid fault triggering of protection circuit during turn-on transition. The NAND gate output v_e remains at logic 1 and the gate driver signal is enabled. Hence, the normal turn-on process is unaffected. Although there is a period ($t_4 \sim t_5$) when the output of S-R latch is in unstable state, it has no influence on the normal operation of gate driver since it is already off.

During HSF condition, V_{QG} is lower than V_{ref1} and v_c is always logic 1. Then v_e becomes logic 0 immediately after the on-state signal of MOSFET is read from v_d at t_1 . Then gate voltage of MOSFET starts to decrease to shut down the short-circuit current. And the green shadowed area ($t_1 \sim t_2$) shown in Figure 4.29(b) is the response time of protection circuit. The MOSFET is held off by the S-R latch after the scaled-down gate voltage falls below V_{ref2} .

During FUL condition, initially the converter works in the normal state and v_c is logic 0. Then v_c abruptly becomes logic 1 after detecting the fault at t_3 . As v_d is already logic 1 (on-state), v_e becomes logic 0 immediately and the MOSFET starts to shut down the short-circuit current similar to the HSF condition.

4.5.3 Simulation Verification

The Cree SiC MOSFET C2M0080120 (1200 V/30 A) is used as the sample for short-circuit protection circuit design with the PSpice model developed in Chapter 3. First of all, the gate charge values under normal, HSF and FUL conditions

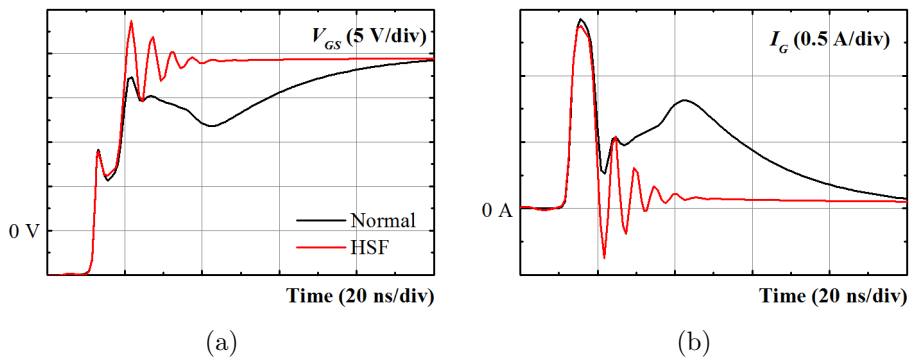


Figure 4.30: Simulation waveforms under normal and HSF conditions: (a) gate-source voltage, (b) gate current.

Table 4.5: Calculation and simulation results of gate charges under normal and fault conditions.

	Charge	Normal (nC)	Fault (nC)
Calculation	Q_{GS}	23.6	23.6
	Q_{GD}	20.3	4.1
	Q_G	43.9	27.6
Simulation	Q_G	42.3	26.7

have to be derived. Since the HSF and FUL have the same gate charge, only HSF condition is discussed in the gate charge calculation. Under HSF condition, it is assumed that short-circuit fault occurs across the inductive load, hence the DC-bus voltage is directly supported by the MOSFET and a small stray resistor, which is assume to be 1Ω . Under normal condition, a 30Ω resistive load instead of the inductive load is used to simplify simulation. The DC-bus voltage is 600 V, and the driver output voltage is +20/-5 V with 2 gate resistances ($R_{G1} = R_{G2} = 5 \Omega$) in series. From the simulation results shown in Figure 4.30, v_{GS} rises towards V_{CC} rapidly without Miller plateau under HSF condition, which results in a smaller gate charge than that under normal condition.

The gate charge can also be calculated based on Eq.(4.27) and (4.28) by substituting $C_{GS} = 944 \text{ pF}$ and $C_{ox} = 618 \text{ pF}$. The integral term in the equations can be calculated by the area under C_{GD} - v_{DS} curve. And $V_{DS,on}$ during short-circuit is assumed to be 100 V. The calculated and simulated gate charge values under normal and fault conditions are summarized in Table 4.5, which show good match with each other.

Based on the simulation results, the gate charge under fault condition is around

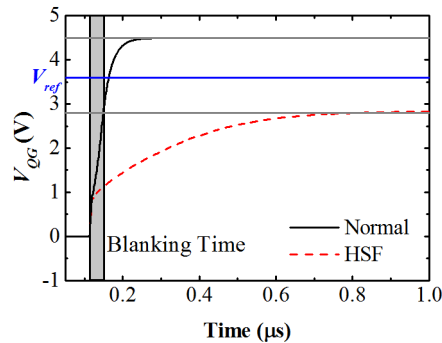


Figure 4.31: Simulation waveforms of integrator output voltage.

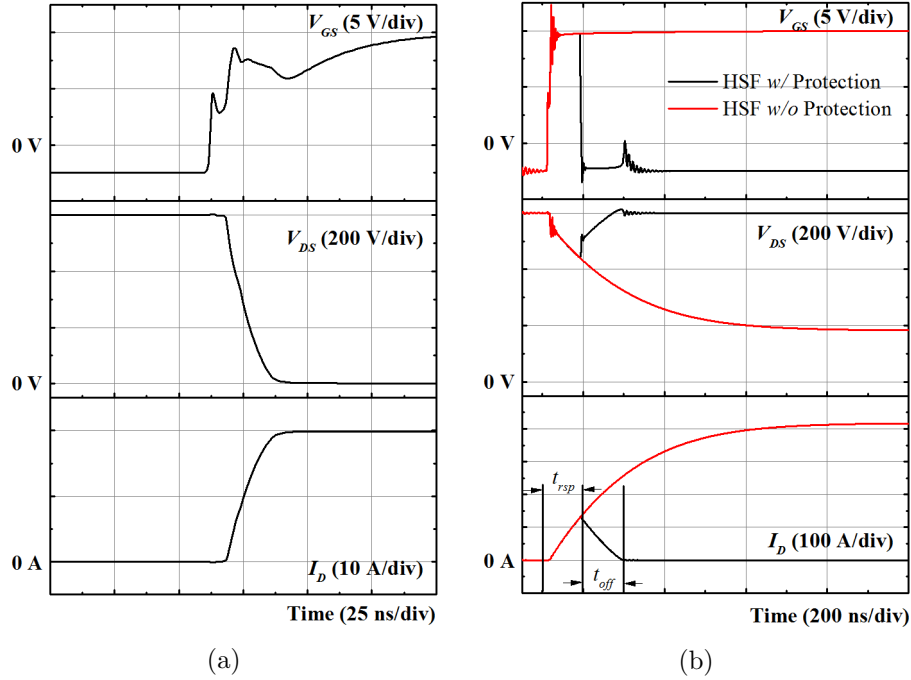


Figure 4.32: Simulation waveforms: (a) normal condition, (b) HSF condition.

63% of normal condition. According to Eq.(4.31), $R_5 = 10 \Omega$ and $C_1 = 4.7 \text{ nF}$ are selected so that V_{QG} is 4.5 V and 2.84 V at normal and fault conditions respectively. The reference voltage is set to 3.6 V with a detection window around ± 0.8 V, as Figure 4.31 shows. The shadowed area is time for gate charge accumulation, hence it needs to be blanked to avoid fault triggering during normal condition.

As Figure 4.32(a) shows, the normal operation of power converter is totally unaffected by the protection circuit. As Figure 4.32(b) shows, when subjected to HSF, the protection circuit will take effect immediately after detecting the fault signal. The MOSFET will be turned off before the drain current rises to the peak short-circuit current. Meanwhile, the drain-source voltage returns back to the DC-bus voltage. The response time t_{rsp} of protection circuit under HSF condition is 76 ns, which is measured from the start to the end of current rise time. The turn-off time t_{off} of short-circuit current is 103 ns, which is measured from the start to the end of current fall time.

The protection circuit is also verified in the FUL condition. As Figure 4.33 shows, the LS transistor carries a load current of 20 A and the HS transistor is off initially. Then the HS transistor is turned on, leading to the arm short-circuit. Without protection, the current via LS transistor rises to the peak short-circuit

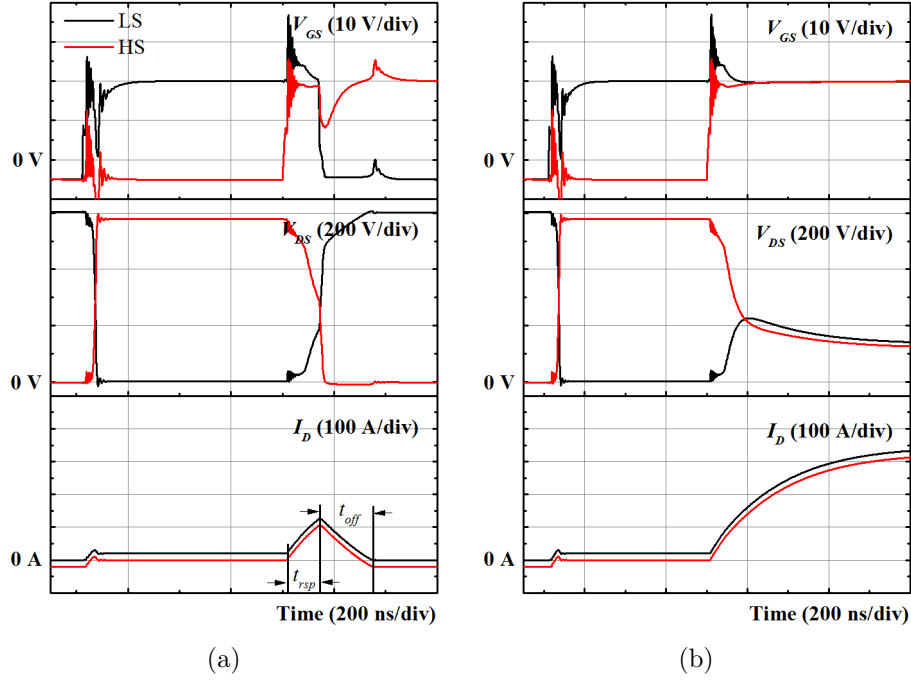


Figure 4.33: Simulation waveforms under FUL condition: (a) with protection, (b) without protection.

current 330 A, which is smaller than that under HSF condition (420 A). It is because both the LS and HS transistor are supporting the DC-bus voltage under FUL condition. By comparison, there is only one transistor supporting the DC-bus voltage under HSF condition. In addition, the LS transistor carries a higher current than the HS transistor, which is contributed by the load current.

Similar to the HSF condition, two parameters t_{rsp} and t_{off} are defined, which are measured to be 63 ns and 105 ns, respectively. Due to the faster response speed, the peak short-circuit current under FUL condition (126 A) is smaller than that under HSF condition (131 A). Theoretically, the higher V_{GS} under FUL condition will result in a higher short-circuit current than that under HSF condition. With the proposed protection circuit, this situation is opposite. It is because the response time under HSF condition is given by the blanking time and delay time. The blanking time is deliberately introduced by CMP2 and LPF to avoid fault triggering of protection circuit during normal turn-on process. The intrinsic delay time is due to the transmission delay in circuits. By comparison, the response time under FUL condition only relies on the delay time. Since at this time the gate voltage is on, there is no such issue of fault triggering.

4.6 Conclusion

The conclusions of this chapter are summarized below.

Firstly, the isolated high-speed gate driver for single SiC MOSFET is developed. The optocoupler gate drive IC with fast rise/fall time and small propagation delay time are selected. The laminated layout is adopted to reduce the stray inductance of driver loop. The half bridge gate driver is based on the single driver unit. In addition, the level shifter, LPF and dead time generator are further included in the logic unit. Both gate drivers show fast rise/fall time from the testing results.

Secondly, the impact of parasitic parameter on gate driver is analyzed and modeled. The high dv/dt and di/dt during the switching transition of one transistor will affect the complimentary transistor via C_{GD} and L_{CSI} . And it is found that L_{CSI} is the dominant factor for gate voltage ringing instead of L_G . The voltage ringing of converter loop can be coupled into driver loop via L_{CSI} .

Thirdly, a novel gate assisted circuit is proposed. A local low impedance path is provided for the discharging current as well as the Cdv/dt current. Hence, it also improves the turn-off speed as well as reduces the turn-off loss. It has been experimentally demonstrated with a switching test up to 750 V and 100 A. The proposed gate assisted circuit can drive the SiC MOSFET module with the maximum switching speed, but without such issues like shoot-through and over-voltage.

Finally, a novel high-speed short-circuit protection circuit for SiC MOSFET is designed. By monitoring the gate charge, the proposed circuit shows fast response time as well as reduced peak current. The proposed protection circuit has been verified by a simulation study and subjected to both HSF and FUL conditions. It shows a response time less than 200 ns to shut down the short-circuit current.

Chapter 5

Micro-channel Cooling Technology for Power Module

In this chapter, the integrated micro-channel heat sink is designed and optimized for power module, and the effects of single-side cooling and double-side cooling are also compared.

5.1 Introduction

As Figure 5.1 shows, the conventional power electronics packaging structure normally consists of multiple thermally resistive layers. Firstly, the top Cu foil of the electrically isolated DBC substrate is pre-patterned to form the interconnection. Then the bottom pads of MOSFET and diode dies are directly soldered on top of substrate. The substrate needs to be mounted on a base plate with high thermal conductivity and mechanical strength. Finally, the base plate is mounted on the heat sink by TIM. The heat dissipated by the power devices has to go through

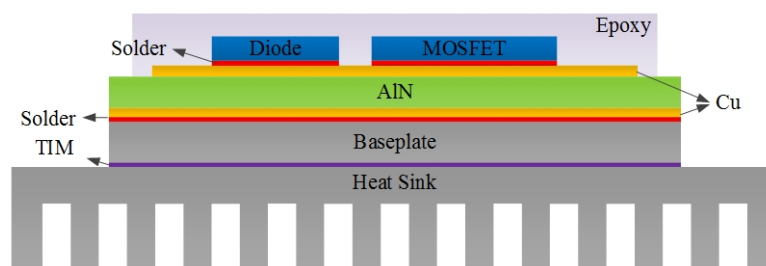


Figure 5.1: Conventional packaging structure of power module.

a long heat conduction path before finally being removed by the heat sink. The long heat conduction path consists of 9 layers and 8 interfaces [84]. The typical thermal conductivity of TIM is 1~3 W/mK, which tends to degrade the cooling performance significantly.



In addition, the conventional cooling technologies, including natural convection and forced convection, show difficulty in cooling the high heat flux (≥ 100 W/cm²) in high power applications. The thermal resistance of heat sink can be derived by the following equation

$$R_{th,hs} = \frac{T_j - T_a}{P_{loss}} - R_{th,M} - R_{th,TIM} \quad (5.1)$$

where T_j and T_a are the junction and ambient temperatures respectively, P_{loss} is the power dissipated by the converter, $R_{th,M}$ is the thermal resistance from junction to case for the module, $R_{th,TIM}$ is the thermal resistance of TIM. For the SiC half bridge module CAS100H12AM1 used in this work, $R_{th,M}$ is 0.22 K/W [71]. Even though SiC can operate at 600 °C theoretically, the junction temperature specified in the datasheet is only 150 °C due to the limitation of packaging technology. Assuming the thermal conductivity of TIM is 2 W/mK, the thickness of 50 μ m, and the area is same as the module (9 cm \times 5 cm), then $R_{th,TIM}$ is estimated to be 0.022 K/W. Assuming the output power of converter is 25 kW with 98% efficiency, so P_{loss} is 500 W. Finally $R_{th,hs}$ is estimated to be 0.008 K/W.

Two types of off-the-shelf heat sinks with the lowest thermal resistance are listed in Table 5.1. The use of natural convection is totally unacceptable in this

Table 5.1: Parameters of off-the-shelf heat sinks with natural convection and liquid cooling.

	Natural convection	Liquid cooling
		
Thermal resistance	0.3 K/W	0.005 K/W
Material	Al	Al, Cu
Volume	30 cm \times 20 cm \times 4 cm	38 cm \times 13 cm \times 1.7 cm

work, and therefore liquid cooling must be adopted. However, the bulky heat sink constitutes a significant volume and weight of power converter, which is undesirable for aerospace applications due to the space and weight constraints.

In this chapter, the integrated MCHS is proposed for the power electronics packaging technology. In addition to the excellent cooling performance, the volume and weight of heat sink can be reduced significantly, which is especially attractive for HPDC applications. The analytical model for MCHS is developed for geometry optimization, and it is also compared with computational fluid dynamics (CFD) simulation. An integrated MCHS inside DBC substrate is designed and optimized, and the cooling performance can be further improved by double-side micro-channel cooling.

5.2 Heat Transfer and Fluid Dynamics Theories of Micro-Channel Cooling

5.2.1 Numerical Modeling

During the last two centuries, heat transfer and fluid dynamics in macro-channel heat sink has been extensively studied with well-established theories and analytical correlations. However, as the heat sink shrinks to micro-size, scaling effects that used to be neglected for the macro-channel case need to be considered now, including temperature-dependent fluid properties, entrance effect, viscous dissipation and conjugate heat transfer. After accounting for these scaling effects, detailed 3D numerical computation must be introduced to analyse the complicated heat transfer mechanism in MCHS. The fluid flow and heat transfer mechanisms in micro-channel are governed by the incompressible, steady Navier-Stokes equations, with conservations of mass, momentum and energy.

Mass

$$\nabla \cdot (\rho \mathbf{U}) = 0 \quad (5.2)$$

Momentum

$$\begin{aligned} \nabla \cdot (\rho u \mathbf{U}) = & -\frac{\partial P}{\partial x} + \frac{\partial}{\partial x} \left[2\mu \frac{\partial u}{\partial x} + \lambda \nabla \cdot \mathbf{U} \right] + \frac{\partial}{\partial y} \left[\mu \left(\frac{\partial u}{\partial y} + \frac{\partial v}{\partial x} \right) \right] \\ & + \frac{\partial}{\partial z} \left[\mu \left(\frac{\partial u}{\partial z} + \frac{\partial w}{\partial x} \right) \right] \end{aligned} \quad (5.3)$$

$$\begin{aligned} \nabla \cdot (\rho v \mathbf{U}) = & -\frac{\partial P}{\partial y} + \frac{\partial}{\partial x} \left[\mu \left(\frac{\partial u}{\partial y} + \frac{\partial v}{\partial x} \right) \right] + \frac{\partial}{\partial y} \left[2\mu \frac{\partial v}{\partial y} + \lambda \nabla \cdot \mathbf{U} \right] \\ & + \frac{\partial}{\partial z} \left[\mu \left(\frac{\partial v}{\partial z} + \frac{\partial w}{\partial y} \right) \right] \end{aligned} \quad (5.4)$$

$$\begin{aligned} \nabla \cdot (\rho w \mathbf{U}) = & -\frac{\partial P}{\partial z} + \frac{\partial}{\partial x} \left[\mu \left(\frac{\partial u}{\partial z} + \frac{\partial w}{\partial x} \right) \right] + \frac{\partial}{\partial y} \left[\mu \left(\frac{\partial v}{\partial z} + \frac{\partial w}{\partial y} \right) \right] \\ & + \frac{\partial}{\partial z} \left[2\mu \frac{\partial w}{\partial z} + \lambda \nabla \cdot \mathbf{U} \right] \end{aligned} \quad (5.5)$$

Energy

$$\nabla \cdot (\rho c_p T \mathbf{U}) = -\nabla \cdot (P \mathbf{U}) + \nabla \cdot (k_f \nabla T) + \Phi, \text{ fluid region} \quad (5.6)$$

$$0 = \nabla \cdot (k_s \nabla T), \text{ solid region} \quad (5.7)$$

$$\begin{aligned} \Phi = & \mu \left\{ 2 \left[\left(\frac{\partial u}{\partial x} \right)^2 + \left(\frac{\partial v}{\partial y} \right)^2 + \left(\frac{\partial w}{\partial z} \right)^2 \right] + \left(\frac{\partial u}{\partial y} + \frac{\partial v}{\partial x} \right)^2 + \left(\frac{\partial v}{\partial z} + \frac{\partial w}{\partial y} \right)^2 \right. \\ & \left. + \left(\frac{\partial w}{\partial x} + \frac{\partial u}{\partial z} \right)^2 \right\} + \lambda (\nabla \cdot \mathbf{U})^2 \end{aligned} \quad (5.8)$$

The commercial CFD solver Ansys Fluent is based on finite volume method. In present work, the Navier-Stokes equations are discretized with second-order upwind scheme and standard pressure interpolation scheme. Semi-implicit method for pressure-linked equations (SIMPLE) algorithm is used to solve the pressure-velocity coupling equations and double precision solver is used.

5.2.2 Analytical Model of Macro-channel Heat Sink

The primary objective of analytical study is to achieve the minimum thermal resistance at a fixed pressure drop by geometry optimization, and therefore to provide guidelines for experiment design. The pressure drop between the inlet and outlet of MCHS is much larger than that of macro-channel counterpart, which is one of the main impediments for its wide-spread application. To enhance the heat transfer efficiency, the fluid needs to pass through the channel with high velocity, hence it demands a large pumping power.

$$P_{pump} = N u_{av} H_{ch} W_{ch} \Delta P \quad (5.9)$$

where N is the number of channels.

Hence, a trade-off between the pressure drop and thermal resistance exists. As it is impractical to achieve a high fluid rate at the expense of an ultra-high pumping power, the turbulence flow is rare for micro-channel. The well-established relationship between the velocity and pressure drop for the macro-channel model is presented as follows. Thermophysical properties of fluid at the average temperature of inlet and outlet are used ($T_{av} = (T_i + T_o)/2$). For fully developed laminar flow, the dimensionless Fanning friction factor, which accounts for the pressure drop due to friction, is given by

$$f = \frac{D_h}{2\rho_{av}u_{av}^2} \frac{\Delta P}{L_x} \quad (5.10)$$

where D_h is the hydraulic diameter defined by $D_h = 2H_{ch}W_{ch}/(H_{ch} + W_{ch})$.

The Poiseuille number (product of Fanning friction factor and Reynolds number) for the fully developed laminar flow is given by [156], which increases with aspect ratio and finally reaches a saturation value of 24

$$Re f_{\infty} = 24 \left(1 - \frac{1.3553}{\alpha} + \frac{1.9467}{\alpha^2} - \frac{1.7012}{\alpha^3} + \frac{0.9564}{\alpha^4} - \frac{0.2537}{\alpha^5} \right) \quad (5.11)$$

where α is the channel aspect ratio with the expression $\alpha = H_{ch}/W_{ch}$. Another important geometry parameter is channel width ratio β and given by $\beta = W_{ch}/W_{pitch}$. Consequently, the relationship between pressure drop and average velocity is given by

$$\Delta P = \frac{2\mu_{av}L_x Re f_{\infty}}{D_h^2} u_{av} \quad (5.12)$$

As Figure 5.2 shows, the thermal resistance network of MCHS is defined by $R_{hs} = (T_j - T_i)/\dot{q}A_{hs}$ (\dot{q} is the heat flux) and consists of the following 3 parts.

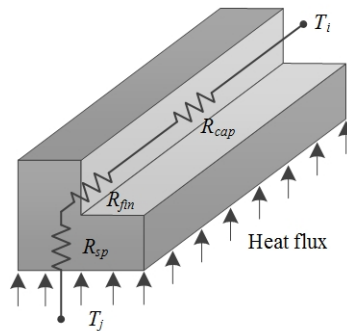


Figure 5.2: Thermal resistance network.

The spreading thermal resistance is related to the heat transfer within the base of heat sink. In present work, the power module is assumed to have the same size as the heat sink. Hence, the expression of spreading thermal resistance is similar to that of conductive thermal resistance

$$R_{sp} = \frac{t_s}{k_s A_s} \quad (5.13)$$

where t_s and A_s are the thickness and area of solid respectively.

The convective thermal resistance is due to the heat transfer from the fins to the working fluid and given by

$$R_{fin} = \frac{1}{\eta_0 h_{av} A_{eff}} \quad (5.14)$$

where η_0 is the total efficiency of micro-fins, h_{av} is the average heat convection coefficient and A_{eff} is the effective area of heat convection with the expression $A_{eff} = N(W_{ch} + 2H_{ch})L_x$. The expression of η_0 is given by

$$\eta_0 = \frac{A_{base} + \eta_{fin} A_{fin}}{A_{eff}} \quad (5.15)$$

where A_{base} is the area of channels base with the expression $A_{base} = NL_x W_{ch}$, A_{fin} is the surface area of fins with the expression $A_{fin} = 2NH_{ch}L_x$, and η_{fin} is the efficiency of single rectangular fin. Compared with the heat removed by the fluid, the natural convection as well as radiation of the baseplate can be neglected. Hence the thin fins can be approximated as adiabatic tips and with the efficiency given by

$$\eta_{fin} = \frac{\tanh(mH_{ch})}{mH_{ch}} \quad (5.16)$$

where m is given by

$$m = \sqrt{\frac{2h_{av}(L_x + W_{fin})}{k_s L_x W_{fin}}} \approx \sqrt{\frac{2h_{av}}{k_s W_{fin}}} \quad (5.17)$$

The average heat convection coefficient h_{av} is given by

$$h_{av} = \frac{k_{f,av} Nu}{D_h} \quad (5.18)$$

where the Nusselt number for the fully developed laminar flow with four sides

heated is from [156], which keeps increasing with aspect ratio and finally reaches a saturation value of 8.235

$$Nu_{\infty} = 8.235 \left(1 - \frac{2.0421}{\alpha} + \frac{3.0853}{\alpha^2} - \frac{2.4765}{\alpha^3} + \frac{1.0578}{\alpha^4} - \frac{0.1861}{\alpha^5} \right) \quad (5.19)$$

The capacitive thermal resistance is related to the amount of heat absorbed by the fluid which leads to the increase of fluid temperature

$$R_{cap} = \frac{1}{\rho_{av} c_{p,av} u_{av} A_{ch}} \quad (5.20)$$

where A_{ch} is the total cross-section area of channels with the expression $A_{ch} = NH_{ch}W_{ch}$.

5.2.3 Analytical Model of Micro-channel Heat Sink

These analytical models are based on classic fluid dynamics theories with simplified assumptions, such as constant fluid properties, fully developed flow, no viscous dissipation, and idealized boundary conditions. For micro-channels, the so-called scaling effects make these assumptions no longer correct. In [157], an optimization method was developed for rectangular micro-channels with both laminar and turbulent flow. A revised analytical model accounting for hydrodynamically and thermally developing laminar flow was developed by [158]. Based on these two works, an analytical model was presented in [159] for geometry optimization of single-phase, laminar flow, rectangular and liquid cooled MCHS. And the effects of various geometry parameters on thermal resistance and pressure drop were evaluated.

The dimensionless Graetz number is defined as a criterion for entrance effect, as Eq.(5.21) shows. It was concluded that entrance effect should be considered when $Gz > 10$ [160]

$$Gz = \frac{RePrD_h}{L_x} \quad (5.21)$$

where Re is the Reynolds number defined by $Re = \rho\mu_{av}D_h/\mu$, Pr is the Prandtl number defined by $Pr = c_p\mu/k_f$, H_{ch} , W_{ch} and L_x are the depth, width and length of the channels respectively.

The Brinkmann number is defined as the ratio between average rate of viscous dissipation and average rate of solid-fluid heat transfer, as Eq.(5.22) shows. In [161], the criterion to predict the limit of significant viscous dissipation effect was

proposed, as Eq.(5.23) shows.

$$Br = \frac{\mu u_{av}^2}{\dot{q} D_h} \quad (5.22)$$

$$\xi_{lim} = 2Re f Br \frac{H_{ch} W_{ch}}{D_h^2} \quad (5.23)$$

where ξ_{lim} is the maximum allowable ratio (e.g. 5) between temperature rise due to viscous dissipation and temperature rise due to solid-fluid heat transfer.

The Maranzana number is defined as the ratio between axial heat conduction in the solid walls and heat convection in the fluid

$$\begin{aligned} M &= \frac{k_s [(H_{base} + H_{ch}) W_{pitch} - H_{ch} W_{ch}] / L_x}{\rho c_p H_{ch} W_{ch} u_{av}} \\ &= \frac{k_s D_h}{k_f L_x} \left[\frac{(H_{base} + H_{ch}) W_{pitch}}{H_{ch} W_{ch}} - 1 \right] \frac{1}{Re Pr} \end{aligned} \quad (5.24)$$

where k_s is the thermal conductivity of solid. And the conjugate heat transfer should be considered when $M > 0.01$ [162]. After accounting for these scaling effects, some insignificant factors can be neglected and the following assumptions are made to simplify analysis:

- Single phase, incompressible and laminar flow;
- Constant solid properties;
- Gravity effect as well as heat transfer due to radiation and natural convection are neglected;
- Surface roughness of the micro-channels is neglected (as it is determined by fabrication process).

5.3 Integrated Micro-channel Cooling for SiC Power Module

5.3.1 AlN-based Micro-channel Heat Sink

Recent progress in AlN processing technologies makes it possible to fabricate micro-channels inside the AlN-layer of DBC by wet chemical etching, high density plasma etching, diamond-tipped dicing saw or laser cutting. Hence, the DBC can also serve as the heat sink. The AlN-based MCHS in DBC for application

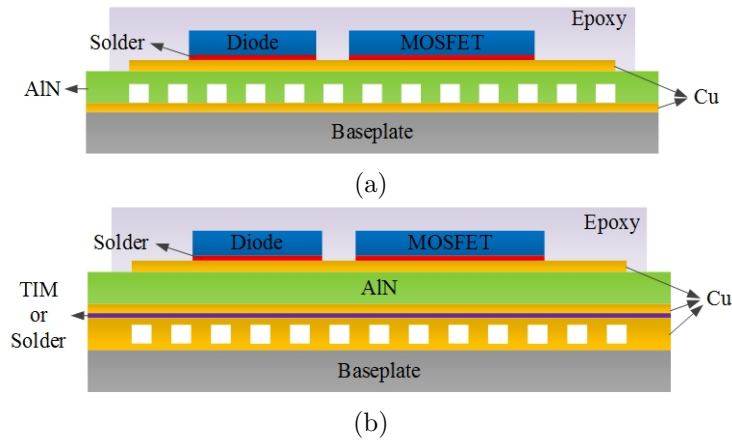


Figure 5.3: Cross-sections of packaging structures with MCHS: (a) proposed structure, (b) conventional structure.

in a military HEV was first proposed and fabricated in [95, 96]. However, the mechanism and geometry optimization are still lacking to further improve the performance. In present work, heat transfer and fluid dynamics mechanisms of the AlN-based MCHS are studied for the first time with commercial CFD solver ANSYS Fluent. The scaling effects, including temperature-dependent fluid properties, entrance effect, viscous dissipation and conjugate heat transfer, are considered. The importance of these scaling effects for the present work is evaluated. Although the classical fluid dynamics theories for macro-channel are not precise enough to predict the performances of micro-channel, it can still be used to explain the phenomenon and mechanism.

Figure 5.3(a) shows the proposed packaging structure with the AlN-based MCHS. The micro-channels can be fabricated by the methods aforementioned. The AlN-based MCHS is sandwiched between two thick Cu films by the mature AlN-Cu bonding process. Figure 5.3(b) shows the conventional structure, in which the Cu-based MCHS is bonded to the backside of DBC by the TIM or solder. Au80Sn20 is a promising solder material due to the high thermal conductivity, high melting point (280 °C) and CTE close to that of Cu. For both structures, the power module is soldered on the top side of DBC and then sealed with encapsulant and metal case for hermitical packaging. Due to the poor thermal conductivity of encapsulant, the top side of power module can be approximated as adiabatic. Other heat transfer mechanisms including radiation and natural convection are neglected. So the MCHS with liquid coolant flowing inside provides the sole path

Table 5.2: Thermal conductivity of packaging materials.

Material	Al ₂ O ₃	AlN	Au80Sn20	Cu	TiM
k_s (W/mK)	24	170	57	387.6	1

for heat removal. The thermal conductivity of the packaging materials used in this work is given in Table 5.2.

Liquid water is used as the working fluid with variable material properties. The temperature-dependent density is given by the Thiesen-Scheel-Diesselhorst equation [163]. Dependence of dynamic viscosity on temperature is defined by [164]. Expressions for specific heat capacity and thermal conductivity are obtained by third-order polynomial fitting results of data [165]. The expressions of temperature-dependent thermophysical properties are given by

$$\rho(T) = 1000 \left[1 - \frac{T + 15.9414}{508929.2(T - 204.87037)}(T - 276.9863)^2 \right] \quad (5.25)$$

$$\mu(T) = 1.005 \times 10^{-3} \left(\frac{T}{293} \right)^{8.9} \exp [4700(T^{-1} - 293^{-1})] \quad (5.26)$$

$$c_p(T) = 3908 + 3.826T - 0.01674T^2 + 2.330 \times 10^{-5}T^3 \quad (5.27)$$

$$k_f(T) = -1.579 + 0.01544T - 3.515 \times 10^{-5}T^2 + 2.678 \times 10^{-8}T^3 \quad (5.28)$$

The computational region with half-channel is shown in Figure 5.4. Such geometry parameters are fixed: $H_b = 335 \mu\text{m}$, $H_{ch} = 300 \mu\text{m}$ and $L_x = L_z = 1 \text{ cm}$. The temperature-dependent thermophysical properties of liquid water are defined by the user defined functions (UDF) provided by ANSYS Fluent. Entrance effect

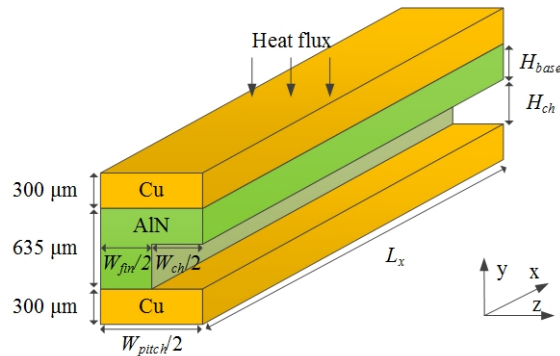


Figure 5.4: Computational region of AlN-based MCHS.

and conjugate heat transfer are automatically taken into account by the numerical model. Viscous dissipation is defined in the source term of energy equation.

Due to the high thermal conductivity of AlN and Cu, the H1 boundary condition (constant axial wall heat flux and constant circumferential wall temperature) can be assumed with four sides heated. The boundary conditions are described as below. At the inlet, the velocity component normal to inlet surface is specified and velocity inlet is adopted.

$$u = 2 \text{ m/s}, v = 0, w = 0, T = 300 \text{ K} \quad (5.29)$$

At the outlet, the fully developed laminar flow is assumed and pressure outlet is adopted with atmosphere pressure (P_0).

$$\frac{\partial u}{\partial x} = 0, v = 0, w = 0, P = P_o \quad (5.30)$$

At the fluid-solid interface, no-slip boundary condition is assumed.

$$u = 0, v = 0, w = 0, T_f = T_s, -k_f \frac{T_f}{\partial n} = -k_s \frac{\partial T_s}{\partial n} \quad (5.31)$$

Uniform heat flux is assumed at the top of computational region.

$$-k_s \frac{\partial T_s}{\partial n} = 200 \text{ W/cm}^2 \quad (5.32)$$

The bottom of computational region and solid parts of the inlet and outlet surfaces are assumed as adiabatic boundaries. The left and right surfaces are

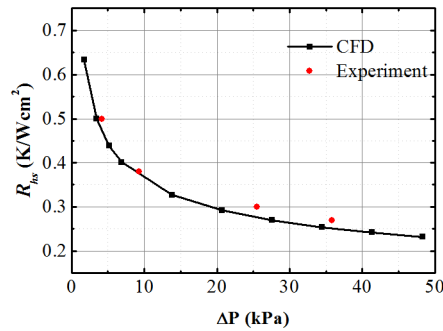


Figure 5.5: Comparison between CFD simulation and experimental results.

assigned with symmetric boundaries.

$$-k_s \frac{\partial T}{\partial n} = 0 \quad (5.33)$$

The experimental results in [96] are studied as a comparison with the results of CFD simulation. Computational region of the AlN-based MCHS are shown in Figure 5.5, with quadrilateral mesh of $181 \times 41 \times 41$ grid lines. Water is used as the working fluid with the inlet temperature 298 K. Constant heat flux of 100 W/cm^2 is assumed at the top of computational region. Boundary conditions of pressure inlet ($P = P_i$) and pressure outlet ($P = P_0$) are adopted. The pressure at the inlet varies and the temperature at the outlet is monitored. The CFD results show in good agreement with that of experiment.

5.3.2 Geometry Optimization

Typical thickness of AlN of DBC for power electronics packaging is $635 \mu\text{m}$, with $300 \mu\text{m}$ typical thickness of Cu on both sides. Deep trenches (i.e, large aspect ratio) are always desirable to enhance heat transfer efficiency, which are limited by fabrication process. The base of MCHS needs to be thick enough to meet the requirements of mechanical strength and electrical isolation capability. Hence, the channel depth is kept constant with the value of $300 \mu\text{m}$, while the channel width as well as the fin width varies to find the optimized geometry in this work. During the geometry optimization, the mechanical and manufacturing limits of

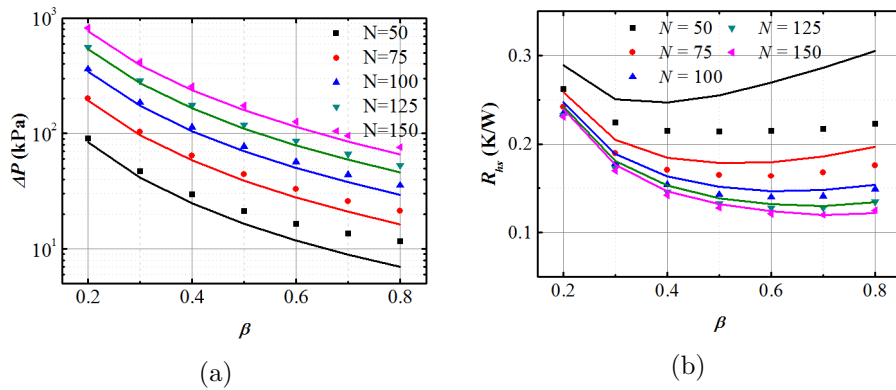


Figure 5.6: Optimization of channel width ratio with simulation (dots) and analytical (lines) results: (a) pressure drop versus channel width ratio, (b) thermal resistance versus channel width ratio.

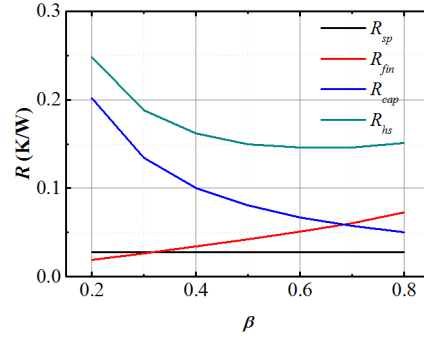


Figure 5.7: Thermal resistance versus channel width ratio.

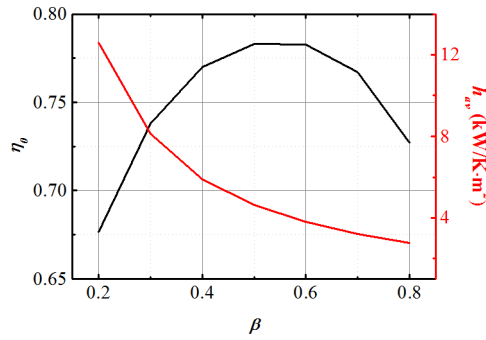


Figure 5.8: Fin efficiency and average heat transfer coefficient versus channel width ratio.

channel width and fin width are not considered in order to purely investigate the optimal geometry. To optimize the trade-off between CPU resource and accuracy, the quadrilateral mesh with grid lines of $181 \times 62 \times 41$ is selected as the optimized trade-off.

From Figure 5.6, ΔP decreases monotonically with β increasing, because the increase of channel cross-section area and decrease of Poiseuille number. R_{hs} decreases initially with β increasing before the optimized value of β . And further increasing of channel width will lead to increase of R_{hs} . As the channel number gets smaller, the curve of R_{hs} versus β is flatter and optimized value of β is smaller. The discrepancy between CFD and analytical results is largest for low N and large β . This is due to negligence of entrance effect, especially for high Reynolds number, which will be addressed later. The three components (R_{sp} , R_{cap} , and R_{fin}) of R_{hs} from the analytical study of one case ($N = 100$) is shown in Figure 5.7. R_{sp} keeps constant and constitutes the smallest fraction. For narrow channel, R_{cap} is the dominant factor, and it keeps decreasing due to the increase

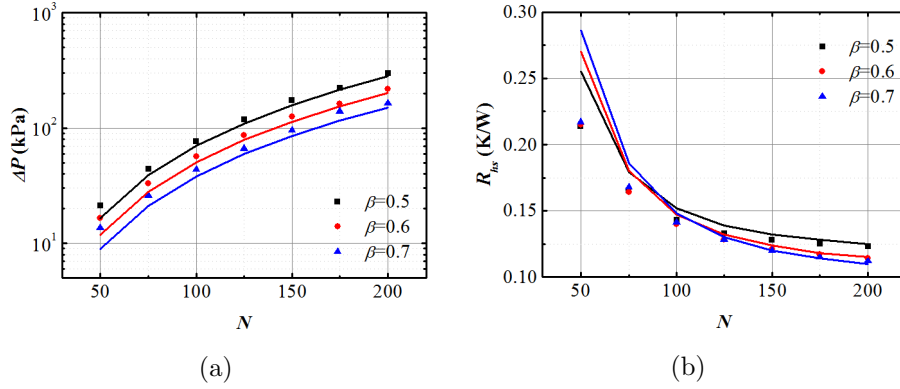


Figure 5.9: Optimization of channel number with simulation (dots) and analytical (lines) results: (a) pressure drop versus channel number, (b) thermal resistance versus channel number.

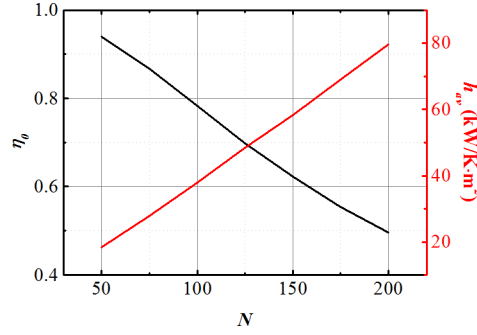


Figure 5.10: Fin efficiency and average heat transfer coefficient versus channel number.

of channel cross-section area with β increasing, which leads to initial decrease of R_{hs} . After the optimized value of β , R_{hs} increases with β increasing due to that R_{fin} becomes comparable with R_{cap} . Figure 5.8 shows that η_0 reaches maximum when $\beta = 0.5$, while h_{av} decreases with β increasing from analytical model. As α decreases when the channel becomes wider, it gives rise to the decrease of Nu . The decreasing Nu and increasing D_h lead to decrease of h_{av} . In addition, the variance of η_0 as well as A_{eff} is less significant compared with that of h_{av} . Hence, R_{fin} is mainly dependent on h_{av} and increases with the channel width increasing.

From Figure 5.9, ΔP increases and R_{fin} decreases monotonically with N increasing. It can also be found that the discrepancy between CFD and analytical results is largest for small N and large β . For constant β , R_{cap} keeps independent

of variance of N . Hence R_{hs} is only determined by R_{fin} . Figure 5.10 shows that η_0 keeps decreasing while h_{av} increasing from the analytical model of one case ($\beta = 0.6$). As α increases when the channel becomes narrower, it gives rise to the increase of Nu . The increasing Nu and decreasing D_h lead to increase of h_{av} . Besides, A_{eff} also keeps increasing, and the variance of η_0 is less significant compared with that of h_{av} and A_{eff} . Hence R_{fin} keeps decreasing and it seems to be always desirable to increase N . However, the extremely large pressure drop for high N makes it impractical to further increase the channel number after a critical value. When N reaches 125, R_{fin} becomes small enough and the decreasing tendency of R_{hs} becomes less significant.

The discrepancy between results from analytical and CFD studies shown in Figure 5.6 and Figure 5.9 makes it clear that scaling effects must be accounted for. For low Reynolds number (< 100), conjugate heat transfer effect tends to reduce average Nusselt number below the fully developed Nu_∞ . Entrance effect becomes considerable with the increase of Reynolds number (> 100) and increases average Nusselt number. Further increase of Reynolds number (> 1000) makes viscous dissipation becomes significant, which tends to reduce average Nusselt number [160]. Since the Reynolds number in this study varies from 70 to 900, entrance effect is the major factor (e.g. for $N = 50$ and $\beta = 0.5$, $Gz = 29$, $\xi_{lim} = 0.00033$, $M = 0.0066$). The results from CFD study also shows no difference no matter whether viscous dissipation is considered in the energy equation.

The hydrodynamical entry length where velocity profile is fully developed is given by $L_h = 0.05ReD_h$. Even for the case $N = 50$ and $\beta = 0.8$ which has largest Re and D_h , L_h is still smaller than the entire channel length. Hence, velocity profile is fully developed before leaving the channel. The apparent friction factor which accounts for pressure drop due to friction and entrance effect is defined and the pressure drop across the entire channel is modified by

$$\Delta P = \frac{2\mu_{av}L_xRe f_{app}}{D_h^2}u_{av} = \frac{2\mu_{av}L_xRe f_\infty}{D_h^2}u_{av} + \kappa(\infty)\frac{\rho u_{av}^2}{2} \quad (5.34)$$

where $\kappa(\infty)$ is the Hagenbach factor and related to the geometry [166]

$$\kappa(\infty) = 0.6796 + \frac{1.2197}{\alpha} + \frac{3.3089}{\alpha^2} - \frac{9.5921}{\alpha^3} + \frac{8.9089}{\alpha^4} - \frac{2.9959}{\alpha^5} \quad (5.35)$$

The thermal entry length where temperature profile is fully developed is given by $L_t = 0.1RePrD_h$. The average Nusselt number, which takes entrance effect into

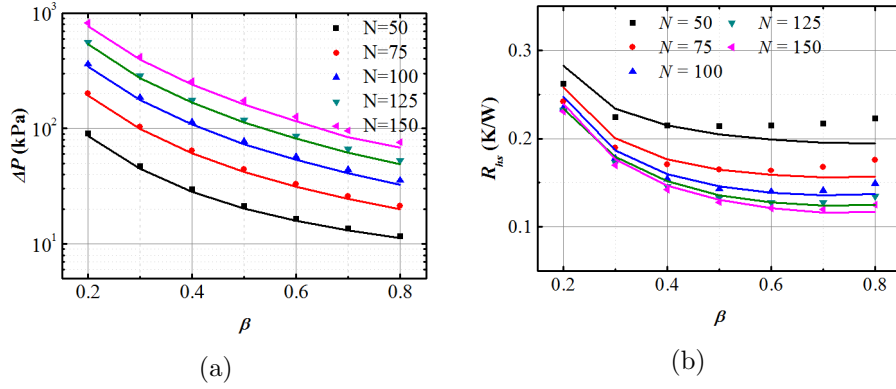


Figure 5.11: Comparison between CFD results (dots) and analytical results with improved corrections (lines): (a) pressure drop versus channel width ratio, (b) thermal resistance versus channel width ratio.

account, is given by the Hausen correlation [167]

$$Nu = Nu_{\infty} + \frac{0.14Gz}{1 + 0.05Gz^{2/3}} \quad (5.36)$$

The analytical results after taking the correlations of entrance effect are shown in Figure 5.11. The pressure drop of analytical study agrees well with that of CFD study even for high Reynolds number. The two curves of thermal resistance coincide for low and moderate Reynolds number. Although the discrepancy can still be observed for high Reynolds number, maximum error has been reduced to 13%, almost 1/3 compared with the fully developed analytical model. Current correlations of entrance effect tend to overestimate the average Nusselt number for high Reynolds number.

5.3.3 Simulation Verification

From the discussions above, the optimal geometry for the trade-off between pressure drop and thermal resistance is: $\beta = 0.7$ ($W_{ch} = 56 \mu\text{m}$, $W_{fin} = 24 \mu\text{m}$) and $N = 125$ with $R_{hs} = 0.128 \text{ K/W}$ and $\Delta P = 66.6 \text{ kPa}$, which coincides with the numerical result conducted by [167]. From Eq.(5.9), the pumping power is estimated to be 0.32 W to cool the 200 W power module with an area of $1 \text{ cm} \times 1 \text{ cm}$. Based on the optimal geometry, effect of channel depth on thermal performance is investigated with $H_{base} = 335 \mu\text{m}$. From Figure 5.12, ΔP shows a very slight increasing (almost constant) with H_{ch} increasing, because the variation of D_h is

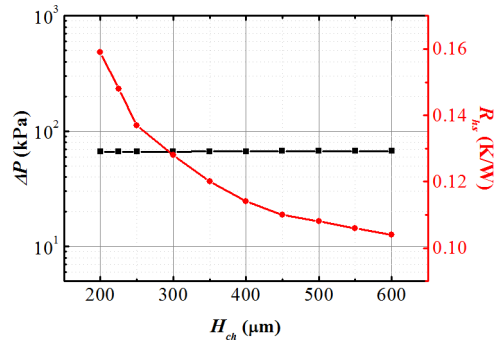


Figure 5.12: Pressure drop and thermal resistance versus channel depth.

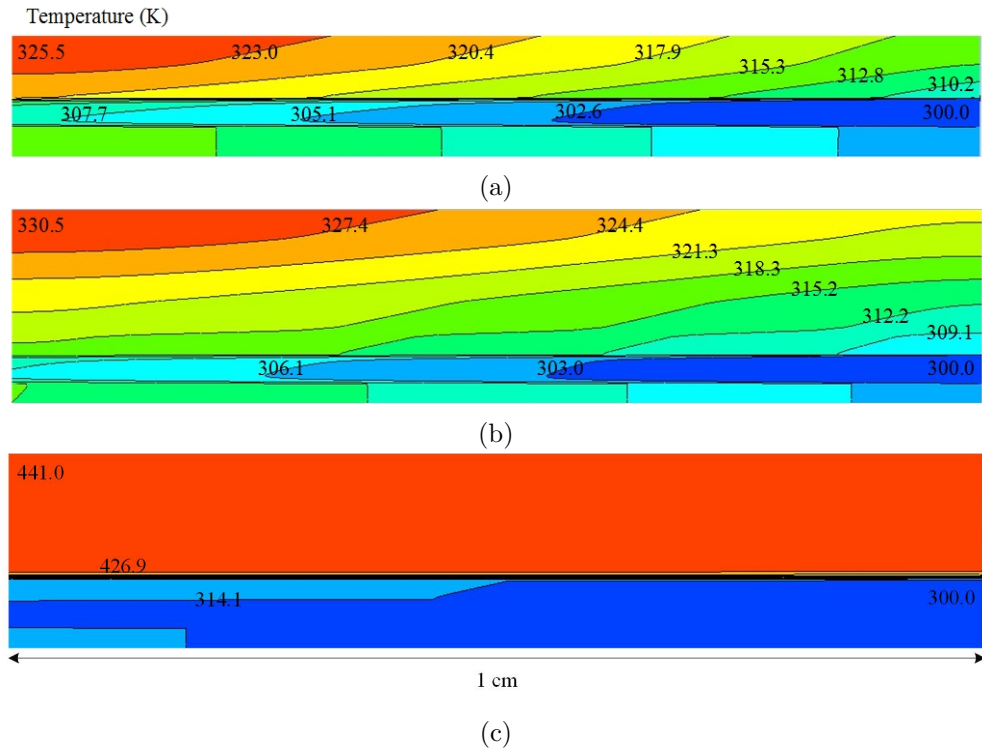


Figure 5.13: Temperature distribution: (a) proposed structure, (b) conventional structure with Au80Sn20 solder, (c) conventional structure with TIM.

insignificant for high aspect ratio channel and Poiseuille number shows a slight increasing with aspect ratio. R_{hs} keeps decreasing with H_{ch} increasing and shows a deduction of 20% for a double increase of H_{ch} from 300 μm . Hence, further increase of aspect ratio only promises an insignificant improvement in thermal performance. The commercial DBC substrate with 300 μm Cu - 635 μm AlN -

300 μm Cu is good enough for fabrication of the proposed AlN-based MCHS.

For the conventional structure shown by Figure 5.3(b), the heat dissipated by the power module needs to pass through DBC and 50 μm Au80Sn20 solder or TIM, before removed by the Cu-based MCHS. Different types of solid materials have little influence on the performance of MCHS due to the high thermal conductivity. So the geometry of the Cu-based MCHS is similar to that of AlN-based MCHS ($H_{base} = 200 \mu\text{m}$, $H_{ch} = 300 \mu\text{m}$, $W_{ch} = 56 \mu\text{m}$, $W_{fin} = 24 \mu\text{m}$ and $N = 125$). Figure 5.13 shows the temperature profile of the three structures with the same boundary conditions. The AlN-based MCHS shows a reduction of thermal resistance by 15% and 80% compared to the conventional structure with Au80Sn20 solder and TIM, respectively. Hence, use of TIM should always be avoided in high power applications.

5.4 Double-side Micro-channel Cooling

As Figure 5.14(a) shows, the sandwich packaging structure, in which the power devices are sandwiched by two DBC substrates, is proposed for double-side cooling and elimination of wirebonding. In addition, it allows 3-D packaging technology to further increase power density. The circuitry of power converter is pre-patterned on the Cu foil of DBC substrate to replace wirebonding, while the micro-channel is directly fabricated on the other side. The power devices can be mounted on the substrates by Au80Sn20 solder in the reflowing process.

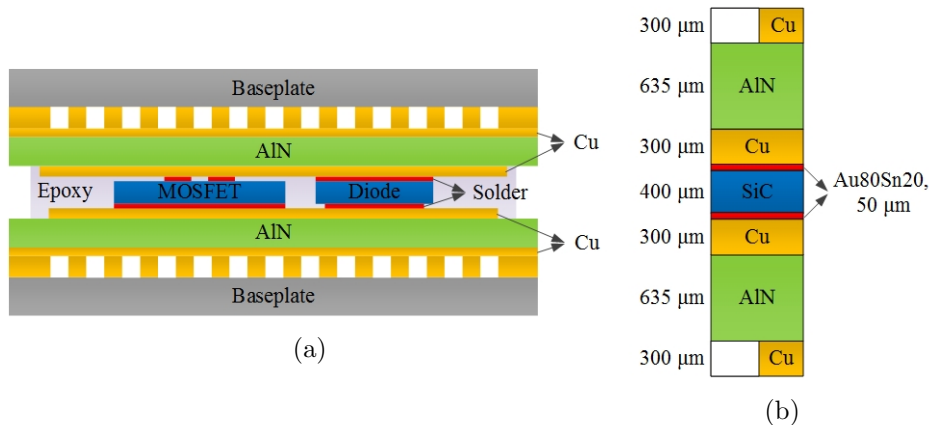


Figure 5.14: Cross-section of packaging structure with double-side micro-channel cooling: (a) detailed structure, (b) simplified structure with thickness of packaging layers.

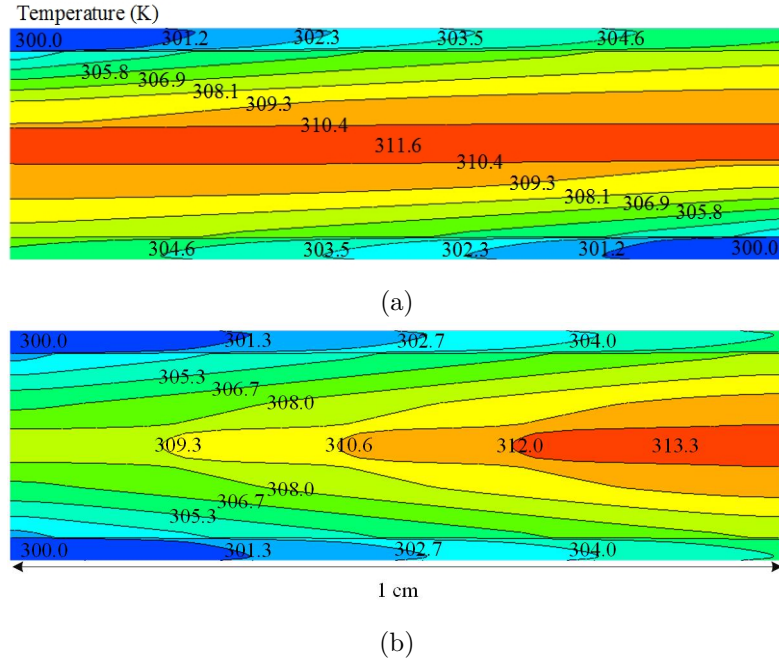


Figure 5.15: Temperature distribution of double-side cooling: (a) counter flow, (b) unidirectional flow.

The detailed packaging structure is further simplified with assumptions of constant and uniform power density. Hence, both the power module and solder are modelled by the rectangular block, which has the same size ($1 \text{ cm} \times 1 \text{ cm}$) as the DBC substrate, as Figure 5.14(b) shows. Assuming the power dissipation inside the module is 200 W , a source term is set in the SiC part with a constant power density of $5 \times 10^3 \text{ W/cm}^3$ during CFD simulation. Based on the discussion of the previous section, the optimized geometry of MCHS with $\beta = 0.7$, $N = 125$ and $H_{ch} = 300 \text{ }\mu\text{m}$ is adopted. In addition, the same boundary conditions, like the velocity inlet and pressure outlet, are adopted again.

The direction of fluid flow through top and bottom DBC substrates can be opposite or unidirectional. Both cooling strategies are of interest for double-side cooling. As Figure 5.15(a) shows, with the opposite flows, the temperature distribution inside the module is almost uniform. The thermal resistance is calculated to be 0.058 K/W with a pressure drop of 90.6 kPa . For the unidirectional flow shown in Figure 5.15(b), the temperature difference inside the module is around 4 K , and the temperature at the outlet is the highest point. The thermal resistance is calculated to be 0.067 K/W with a pressure drop of 92.3 kPa . The opposite

flows permits a smaller thermal resistance than the unidirectional flow. Compared with the single-side cooling in previous section, the pressure drop for double-side cooling is higher. It is because the viscosity of water decreases with the temperature increasing. In the real situation, considering that the gate and source pads are smaller in size than the drain pad, the heat transfer efficiency from the top and bottom sides of power module is a little asymmetrical actually.

5.5 Conclusion

The conclusions of this chapter are summarized below.

Firstly, based on the classic heat transfer and fluid dynamics theories, an analytical model of the macro-channel heat sink is developed for geometry optimization. Then the analytical model of the micro-channel heat sink is improved after considering various scaling effects, with the entrance effect being the dominant factor.

Secondly, the single-phase, laminar flow, rectangular and AlN-based MCHS with water coolant is designed and optimized. The analytical model after accounting for the entrance effect coincides well with the CFD model apart from the thermal resistance at high Reynolds number. A thermal resistance of 0.128 K/W is achieved at a pressure drop of 66.6 kPa. It shows a reduction of thermal resistance by 15% and 80% compared with the two conventional structures, in which the Cu-based MCHS is bonded to DBC substrate by solder or TIM respectively.

Finally, a double-side packaging structure with micro-channel cooling is proposed to further improve the cooling performance. In addition, it also allows 3-D packaging technology to further increase power density. Both the opposite and unidirectional flows are investigated, with the approach of opposite flows resulting in a uniform temperature distribution and the smallest thermal resistance of 0.058 K/W.

Chapter 6

Switching Characterization of SiC Power Devices

In this chapter, the experiment details of switching characterization of SiC power devices including SiC Schottky diode, SiC MOSFET and SiC power module are demonstrated.

6.1 Introduction to Double Pulse Testing Circuit

As Figure 6.1 shows, a classical DPT circuit with clamped inductive load is normally used for switching characterization of power devices. It can be used to test discrete devices as well as half bridge power module. The HS transistor M_H is always off and the LS transistor M_L is active, so that the dynamic characteristics of the MOSFET and its body diode can be obtained. When M_H is replaced by a freewheeling diode, this circuit becomes to be a typical chopper. Then the dynamic characteristics of freewheeling diode can be obtained.

The control signal is generated by a TMS320F28335 DSP from Texas Instruments. It consists of two pulses to avoid heating up the device under test (DUT). During the first long pulse (typically 10~100 μ s), the DC-link capacitor starts to charge the inductor via M_L to set up the inductor current, and it is given by

$$I_L = \frac{V_{DC}}{L_{load}} \Delta t \quad (6.1)$$

where V_{DC} is the DC-bus voltage, L_{load} is the load inductance, and Δt is the duration of first pulse. At the end of first pulse, the current commutates from

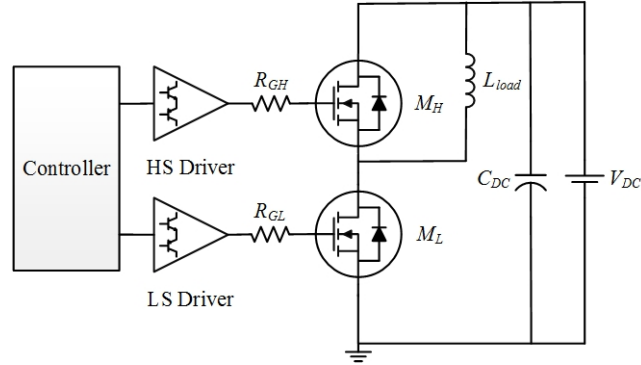


Figure 6.1: Schematic of double pulse testing circuit.

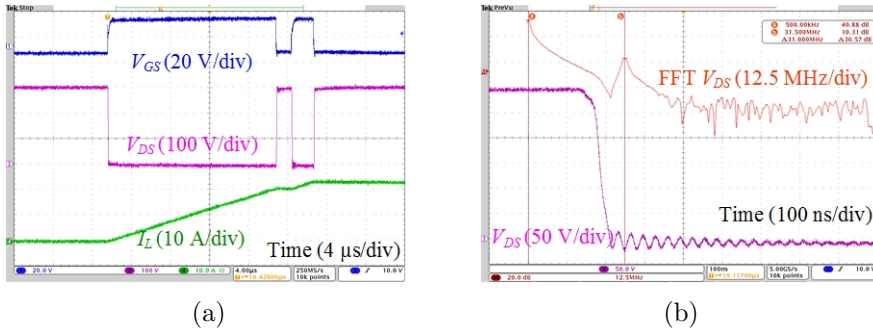


Figure 6.2: Example of double pulse testing experiment: (a) all waveforms ; (b) voltage ringing.

M_L to the body diode of M_H . Hence, the turn-off characteristics of MOSFET can be measured during this transition. A blanking time of $2 \mu\text{s}$ between the two pulses is set, and it should be long enough to allow the voltage and current to settle out. The second narrow pulse only lasts $2 \mu\text{s}$. At the start of second pulse, the current commutates back to M_L . In contrary to the end of first pulse, the turn-on characteristics of MOSFET and reverse recovery process of body diode can be measured during this transition. An experiment example of switching characterization is shown in Figure 6.2(a).

During switching transitions, the output capacitance of M_H or M_L will form a resonant circuit with the stray inductance of power loop. It leads to current overshoot during turn-on transition and voltage overshoot during turn-off transition. The current and voltage overshoots will increase the switching loss. In addition, the ringing during switching transitions lead to EMI issues, as the FFT results in Figure 6.2(b) shows.

6.1.1 Passive Devices

Since the SiC power devices are expected to switch at a higher frequency than the Si counterparts, the parasitic parameters of the testing circuit will have a more significant influence on the switching characteristics. Hence, the parasitic parameters of the passive devices, including the equivalent parallel capacitance (EPC) of load inductor and the equivalent series inductance (ESL) of DC-link capacitor, should be minimized so as to accurately measure switching characteristics.

A. Load Inductor

The EPC of inductor is the sum of distributed capacitances of turn-to-turn and turn-to-core. In this work, a single-layer winding, air core inductor is made to ensure a low EPC [168]. The Hewlett-Packard impedance analyzer 4194A with a maximum sweeping frequency of 40 MHz is used for measurement. The inductance is measured to be 246 μH at a sweep frequency from 1 kHz to 100 kHz. The resonant frequency is measured to be 7.21 MHz. Hence the EPC is calculated to be 2 pF.

B. DC-link Capacitor

The DC-link capacitor (or C snubber) needs to be put as close as possible to the converter phase-leg to form a minimized current commutation loop. In this work, two kinds of high voltage DC-link capacitors are mainly used, as given by Table 6.1. And the ESL is also measured by impedance analyzer.

Table 6.1: Parameters of high voltage DC-link capacitors.

Part No	Type	Capacitance	Voltage	ESL
MKP1848C54090JK2	Film	4 μF	900 V	21 nH
C1812V104KDRAC	MLCC	0.1 μF	1 kV	4.5 nH

6.1.2 High-speed Measurement Technology

The high switching speed of SiC power devices introduce a new challenge to the existing current and voltage measurement technologies. The analog bandwidth of oscilloscope and probe is defined by the frequency at which the measured amplitude of sine wave is 3 dB lower than the actual amplitude. To ensure a low-error (below 1%) measurement, it is a rule of thumb to use a measurement device with 5 times bandwidth of the measured signal [169, 170]. Although the typical switching frequency of SiC power converters is around 20~200 kHz, the resonant frequency during switching transitions may be above 30 MHz. The accurate

switching characterization is crucial for the calculation of switching loss as well as energy conversion efficiency. Hence, the bandwidth of oscilloscope and probe is recommended to be 150 MHz at least.

Another important parameter of measurement is the rise/fall time. A rough estimation of the relationship between rise/fall time and bandwidth is given by [169]

$$t_r = t_f = \frac{0.35}{BW} \quad (6.2)$$

where the factor 0.35 is based on the single pole model (like low pass RC filter). For a signal with 50 ns rise time (which is a typical value in SiC power devices), the equivalent bandwidth is 7 MHz. Similarly, a measurement equipment with 35 MHz bandwidth above is required to ensure an error of less than 1%.

A. Current Measurement

The conventional current measurement strategy with the bulky current probe is no longer suitable in switching characterization. In this work, a simple scaled-down current transformer (CT) is made. The primary side of CT only comprises a single turn, while the secondary side comprises 10 turns of isolated wire wound on a ferrite toroid. Based on the turn ratio between the primary and secondary windings, the measured current mapped on the secondary side is given by

$$I_2 = \frac{N_1}{N_2} I_1 = \frac{I_1}{N_2} \quad (6.3)$$

The output terminal of secondary side of CT is connected with Tektronix current probe TCP0030 (30A, 120MHz). The pin of discrete device is inserted

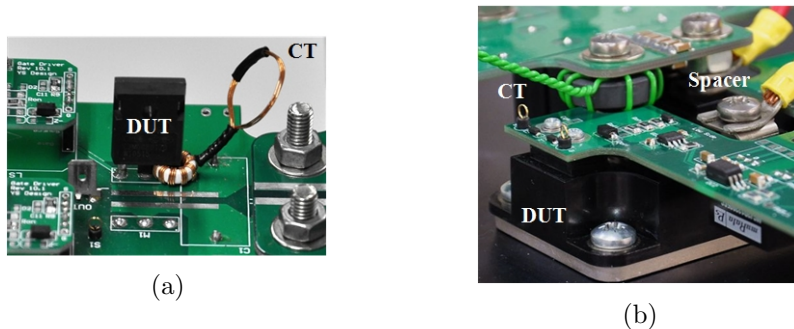


Figure 6.3: Installation of current transformer on DUT: (a) discrete device, (b) power module.

into the ferrite toroid, as Figure 6.3(a) shows. For the module, a similar CT is made with a bigger ferrite toroid, as Figure 6.3(b) shows. The CT is installed on the S2 terminal. In addition, a spacer is also installed on the D1 terminal to fasten the CT as well as DC-bus. The use of CT will introduce an extra stray inductance to the loop stray inductance.

The CT has the advantages of low cost and easy implementation. It also provides a reliable isolation between DUT and oscilloscope. One disadvantage of CT is the saturation issue at high DC current. Hence, CT can only be used to measure the transient current.

B. Voltage Measurement

The long ground clip of high voltage passive probe may affect the accuracy of high-speed measurement [170]. The stray inductance of ground clip will form a resonant circuit with the input capacitance of voltage probe. In the high-speed digital circuit, it will add significant overshoot and ringing to the measured signal. Compared with the digital circuit, although dv/dt in SiC power converters is even higher, the rise/fall time is also significantly longer (more than 10 times). Hence, the influence of ground clip length on high voltage measurement is insignificant. In this work, the Tektronix high voltage passive probe TPP0850 (1 kV, 800 MHz) is used, which can measure the signal with 160 MHz bandwidth and 2.2 ns rise/fall time (less than 1% error). The probe with original probe tip and ground clip shown in Figure 6.4(a) is compared with two types of modified probes shown in Figure 6.4(b). The length of the ground clip for the modified probes (5 cm, 3 cm) are much shorter than the original one (30 cm).

As Figure 6.5 shows, the experimental waveform measured by the original setup shows no significant difference with the waveforms measured by modified

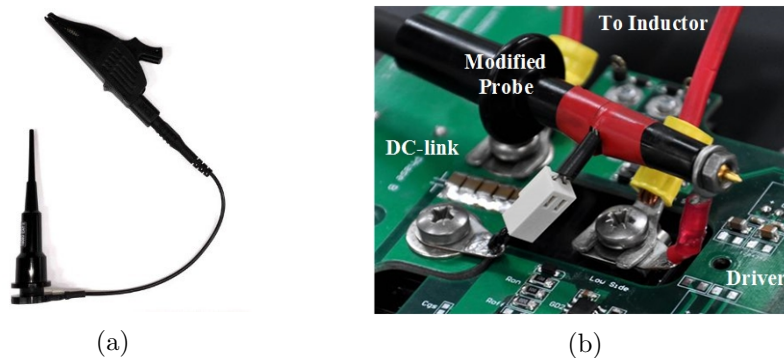


Figure 6.4: High voltage passive probe: (a) original, (b) modified.

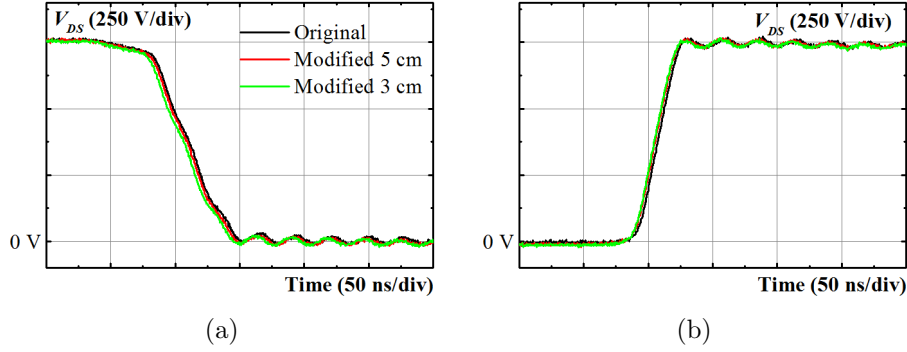


Figure 6.5: Waveforms of drain-source voltage with 3 types of voltage probe: (a) turn-off, (b) turn-on.

probes. For the original setup which has the longest ground return path, it shows the longest delay time. Hence, the probe deskew or post-processing of data is required.

6.2 Stray Inductance Modeling and Extraction

The half bridge configuration with lumped parasitic parameters is shown in Figure 6.6, which consists of three current loops. To drive SiC power devices with high-speed switching, the stray inductance becomes a more and more important factor. The interaction between the junction capacitance of power device and stray inductance of the PCB layout and package results in EMI issues of overshoot and ringing during switching transitions. Hence, the stray inductance needs to be modeled and extracted for accurate switching characterization of SiC power devices. In this work, the stray inductances of PCB layout and package are simulated by the parasitic parameter extraction tool Ansys Q3D.

As Figure 6.7(a) shows, the alternating current in trace 1 will generate an alternating magnetic field in trace 2, resulting in a coupling current with opposite direction according to the basic electromagnetic theory [171]. The equivalent circuit is shown in 6.7(b), and the total stray inductance is given by

$$L = L_1 + L_2 - 2M \quad (6.4)$$

$$M = k\sqrt{L_1L_2} \quad (6.5)$$

where L_1 and L_2 are the self-inductances, M is the mutual-inductance and k is the

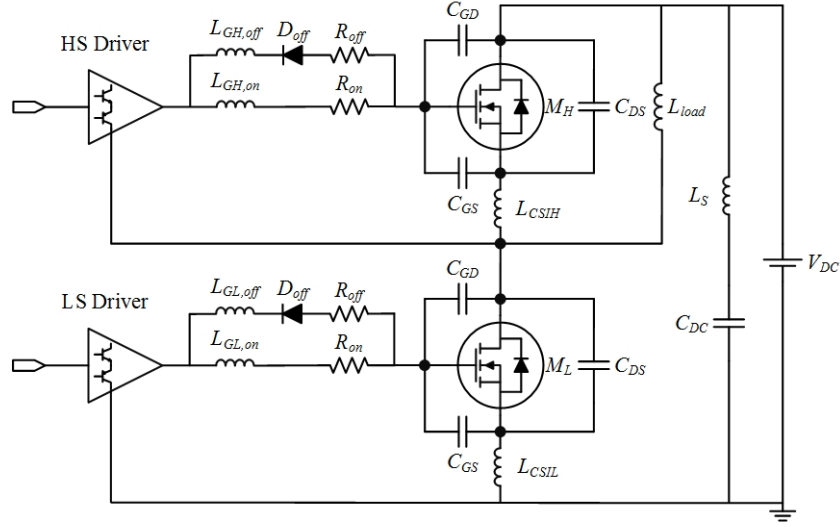


Figure 6.6: Equivalent circuit of half bridge configuration with lumped parasitic parameters.

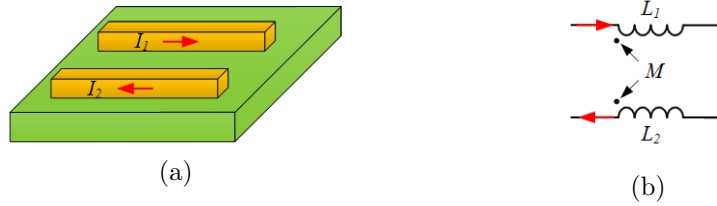


Figure 6.7: Two coupled PCB traces: (a) 3D model, (b) equivalent circuit.

coupling coefficient. Hence, a strong coupling coefficient between the two traces helps to reduce the stray inductance. And the current loop should be minimized in layout design.

6.2.1 PCB Stray Inductance Extraction

In this section, two kinds of PCBs are investigated, including gate driver developed in Chapter 4 and half bridge circuit for discrete devices testing. The PCB layout is directly imported from Altium Designer.

A. Gate Driver

Although the gate voltage ringing is not so sensitive to the gate inductance compared with common source inductance L_{CSI} , it still needs to be minimized to avoid the potential risk of EMI issues. Due to the use of turn-off diode in present work, the discharging path of gate capacitor is different as the charging

Table 6.2: Stray inductance of gate drivers.

	Single Gate Driver	Half Bridge Gate Driver	
		HS	LS
Turn-on	6.78 nH	4.08 nH	4.26 nH
Turn-off	8.00 nH	4.58 nH	4.61 nH

path. And therefore the two loops are investigated separately. The gate stray inductances for the single and half bridge gate drivers are summarized in Table 6.2. The half bridge gate driver shows a smaller stray inductance due to the use of 4-layer PCB. For the 2-layer PCB, the ground plane is 1.6 mm to the top layer (FR4 layer thickness), while the distance for the 4-layer PCB reduces to 0.127 mm (PP layer thickness). Hence, it permits a stronger coupling effect.

B. Half Bridge Circuit for Discrete Devices

A half bridge circuit for discrete device testing is developed in this work, which is adaptable to both TO-220 and TO-247 packages, as Figure 6.8 shows. In addition, it is also flexible to build various types of topologies by employing it as a power electronics building block (PEBB). Either the film capacitor or multi-layer ceramic capacitor (MLCC) can be adopted as DC-link to decouple the stray inductance. Since the MLCC has the smallest ESL among all kinds of high voltage capacitors, it is put nearest to the MOSFET and then followed by the film capacitor. And the stray inductance of minimal power loop (consisting of MLCC, M_H and M_L) is extracted. In addition, the stray inductance of two driver loops is also extracted, as Table 6.3 illustrates.

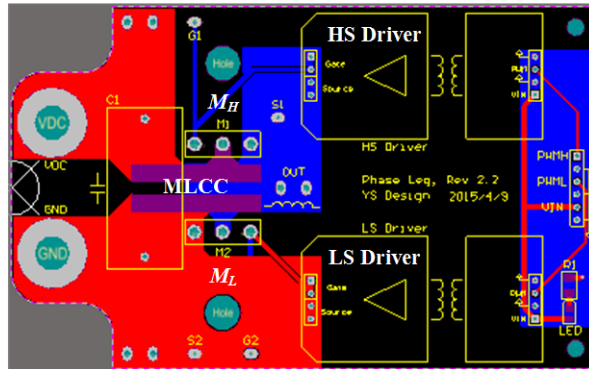


Figure 6.8: Layout of half bridge circuit for discrete devices.

Table 6.3: Stray inductance of half bridge circuit.

Power Loop	Driver Loop	
	HS	LS
7.14 nH	19.35 nH	12.68 nH

6.2.2 Package Stray Inductance Extraction

In this section, three kinds of packages are investigated, including TO-220 (SiC Schottky diode), TO-247 (SiC MOSFET) and module. The 3D models of packages are re-drawn in Ansys Q3D according to their physical dimensions.

A. TO-220 and TO-247 Packages

As a conventional package for discrete power devices, the stray inductance of transistor outline (TO) package relies on the pin length. Hence, it is a rule of thumb to cut the pin as short as possible when soldering the device on PCB. The 3D models of TO-220 and TO-247 packages are shown in Figure 6.9.

For TO-220 package, there is no need to separate the stray inductances of anode and cathode pins. And total stray inductance of SiC Schottky diode in TO-220 package is simulated in Ansys Q3D by varying the pin length. The stray inductance is proportional to the pin length at a ratio of 0.35 nH/mm, as Figure 6.10(a) shows.

For the MOSFET in TO-247 package, the source pin is shared by power loop and driver loop. Hence, it is necessary to separate the stray inductances of three pins in order to evaluate the impact of L_{CSI} . There are three self-inductances $L_{G,self}$, $L_{D,self}$, $L_{S,self}$ and three mutual-inductance M_{GD} , M_{GS} , M_{DS} . Three independent equivalent stray inductances L_G , L_D and L_S are assumed to be

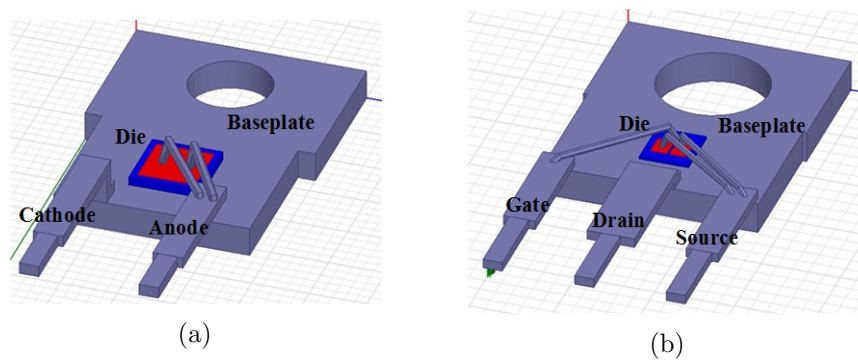


Figure 6.9: 3D models of package for discrete device: (a) TO-220, (b) TO-247.

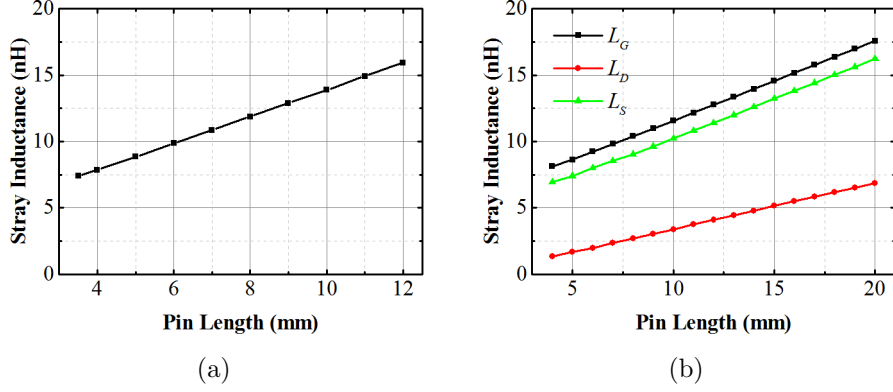


Figure 6.10: Relationship between stray inductance and pin length: (a) TO-220, (b) TO-247.

series with gate, drain and source terminals respectively. The effect of mutual-inductance is considered into the equivalent stray inductance by the following expressions

$$L_G + L_D = L_{G,self} + L_{D,self} - 2M_{GD} \quad (6.6)$$

$$L_G + L_S = L_{G,self} + L_{S,self} - 2M_{GS} \quad (6.7)$$

$$L_D + L_S = L_{D,self} + L_{S,self} - 2M_{DS} \quad (6.8)$$

Hence, the expressions of equivalent stray inductance can be derived

$$L_G = L_{G,self} - M_{GD} - M_{GS} + M_{DS} \quad (6.9)$$

$$L_D = L_{D,self} - M_{GD} - M_{DS} + M_{GS} \quad (6.10)$$

$$L_S = L_{S,self} - M_{GS} - M_{DS} + M_{GD} \quad (6.11)$$

The relationship between equivalent stray inductance and pin length for TO-247 package is shown in Figure 6.10(b). Both L_G and L_S are proportional to the pin length at a ratio of 0.6 nH/mm, while L_D is proportional to the pin length at a ratio of 0.35 nH/mm. The drain terminal shows the smallest stray inductance as its pin and pad are directly soldered on the baseplate. In addition, the drain pin is in the middle position for a smaller current loop, so that the coupling effect is also stronger.

B. Module Package

The layout design of SiC half bridge module on the DBC substrate is shown

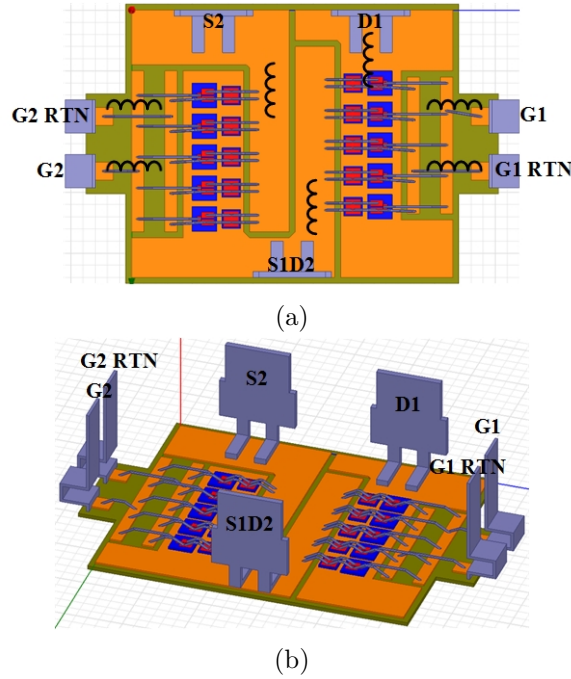


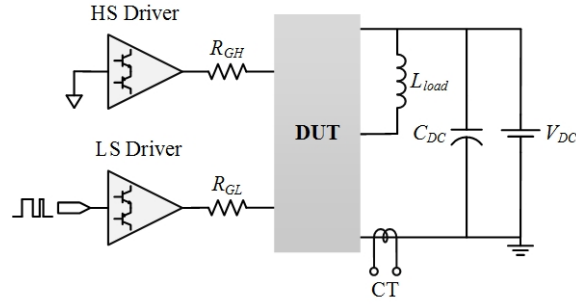
Figure 6.11: 3D model of module package: (a) top view, (b) trimetric view.

in Figure 6.11. The top electrode pads are interconnected by the aluminum wire-bonding. As the Kelvin source is adopted to separate the gate driver loop from the power loop, L_{CSI} is assumed to be zero. The total stray inductance of power module (from terminal D1 to terminal S2) is extracted to be 18.27 nH, which is very close to the value of 20 nH from the datasheet.

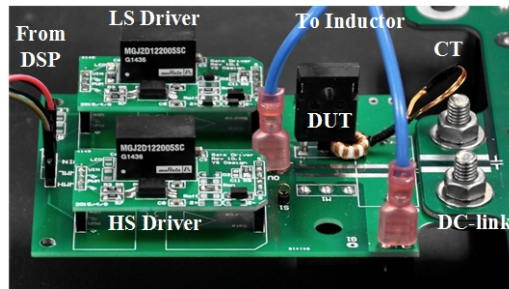
6.3 Switching Characterization of SiC Discrete Power Devices

In this section, a switching characterization is conducted on the commercial SiC discrete power devices including SiC Schottky diode (Cree C4D20120, 1.2 kV, 20 A) and SiC MOSFET (Cree C2M0080120, 1.2 kV, 30 A).

As a majority carrier device, there is no minority carrier holes stored in the drift region of SiC Schottky diode during switching transitions. However, the junction capacitance still leads to overshoot and ringing during current commutation, which is similar to the reverse recovery process for its bipolar PiN counterpart. This kind of reverse recovery process for SiC Schottky diode is of interest, since



(a)



(b)

Figure 6.12: Double pulse testing for discrete devices: (a) schematic, (b) experimental setup.

it directly impacts the switching loss of SiC Schottky diode and SiC MOSFET.

The MOSFET channel can work in the reverse conduction when applying a positive gate voltage, which is called as synchronous rectification (SR). This concept has been extensively implemented in the low voltage (< 100 V) DC/DC converters in switching-mode power supply (SMPS) application to replace the diode rectifier for lower conduction loss. Compared with the forward voltage drop across the PN junction of diode, SR permits a smaller voltage drop at a certain range of current. During the dead time, the freewheeling current will flow through the intrinsic body diode of MOSFET working as SR, which is a bipolar PiN diode. Once the MOSFET working as the main switch is triggered on, the minority carrier stored in the body diode has to be swiped out of the drift region, leading to a current overshoot across the main switch due to the reverse recovery process of PiN diode. Hence, the performance of body diode of SiC MOSFET is of great interest to assess the potential application of SiC MOSFET in SR converter.

The switching characterization of DUT shown in Figure 6.12 is conducted

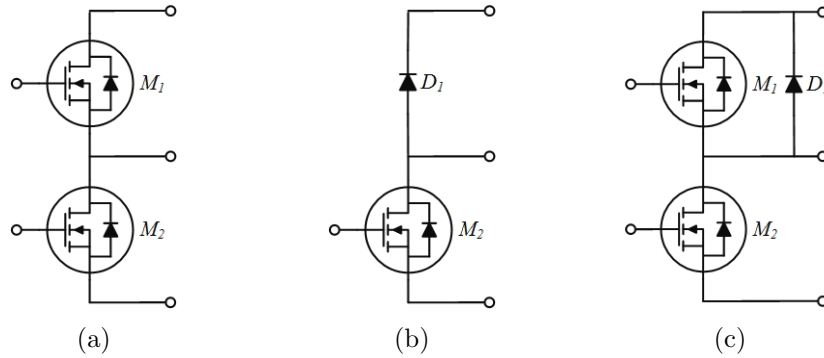


Figure 6.13: Schematics of device under test: (a) case A with MOSFET half bridge, (b) case B1 and B2 with chopper, (c) case C with hybrid chopper.

under 4 different cases, as Figure 6.13 shows. For case A, it is a half bridge configuration consisting of two MOSFETs to evaluate the performance of body diode of MOSFET. The typical chopper with a MOSFET and a diode is investigated in case B1 and B2. And the 1.2 kV, 20 A SiC Schottky diode C4D20120A from Cree and 1.2 kV, 30 A Si ultrafast diode STTH3012D from STMicroelectronics are used in case B1 and B2, respectively. For case C, it is a hybrid chopper, in which the HS device consists of a MOSFET and an anti-parallel SiC Schottky diode. It is a typical circuit configuration in SiC power module or converter to suppress the conduction of body diode. Since the external FWD tends to increase the total output capacitance, its impact on switching characteristics needs to be evaluated. The FWD is directly soldered on the pin of MOSFET to minimize the stray inductance. And a gate resistance of 10Ω is used for all cases.

From the switching waveforms shown in Figure 6.14, case A shows a bit higher reverse recovery current than case B1, however, both are almost negligible compared with case B2. It also brings in an insignificant current overshoot at turn-on. In addition, it is almost independent of load current. Hence, the body diode of SiC MOSFET almost exhibits a zero reverse recovery process similar to SiC Schottky diode, as Figure 6.15 shows. It makes SiC MOSFET attractive in application of SR converter.

The presence of anti-parallel FWD in case C will increase the effective output capacitance, leading to a smaller voltage overshoot at turn-off, while a higher reverse recovery current and therefore a larger current overshoot at turn-on compared with case A. Hence, the extra anti-parallel FWD in SiC inverter tends to reduce turn-off loss but increase turn-on loss. Considering the turn-on loss is the

CHAPTER 6. SWITCHING CHARACTERIZATION OF SiC POWER DEVICES

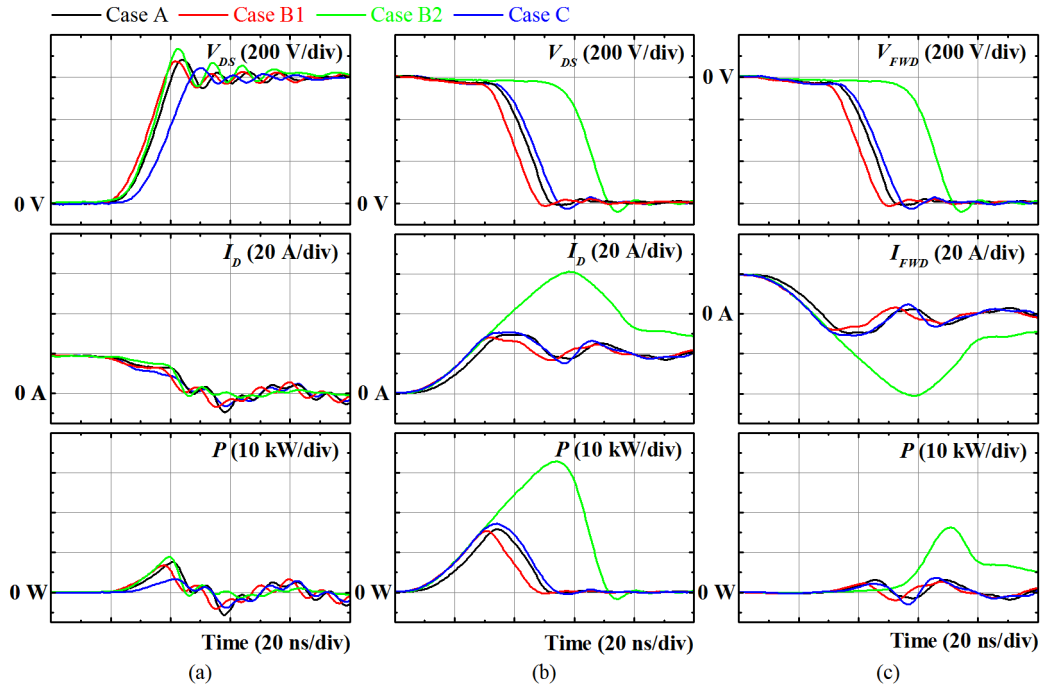


Figure 6.14: Switching waveforms: (a) turn-off, (b) turn-on, (c) reverse recovery process.

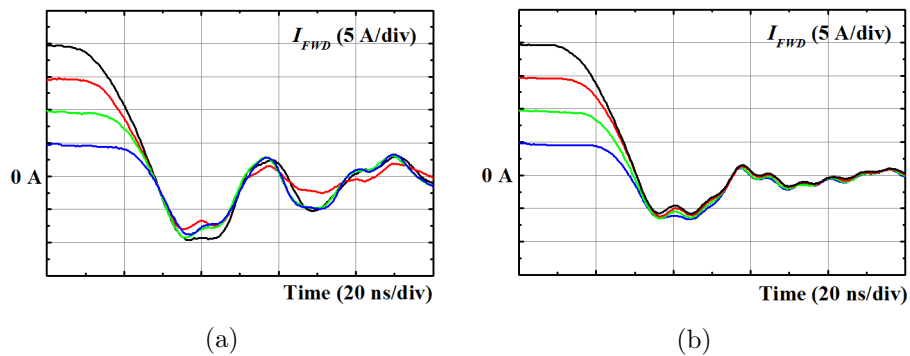


Figure 6.15: Reverse recovery process: (a) body diode of SiC MOSFET, (b) SiC Schottky diode.

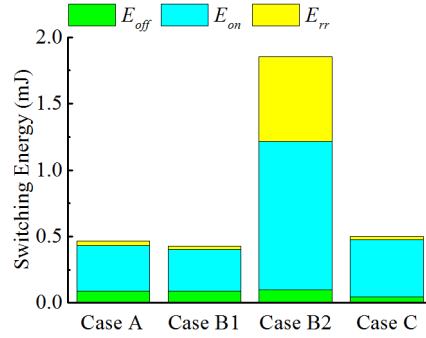


Figure 6.16: Switching energy at 600 V and 20 A.

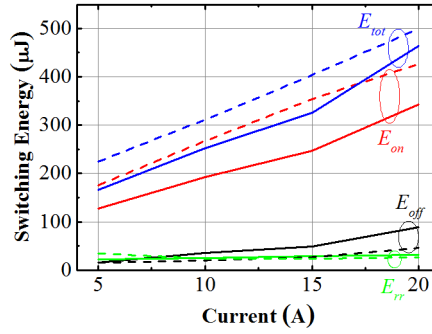


Figure 6.17: Switching loss versus load current, solid lines are case A, dashed lines are case C.

dominant factor of switching loss, case A can permit a higher efficiency compared with case C, as Figure 6.16 shows.

The relationship between the switching loss and load current is given by Figure 6.17. The turn-off loss of case C is always smaller than that of case A, but the turn-on loss is opposite. For low load current, the total loss of case C is higher, and the two curves tend to overlap at high load current. The polynomial correlations between the total switching loss and load current is given by

$$E_{tot,A} = 0.519i^2 + 6.395i + 124.4 \text{ } (\mu J) \quad (6.12)$$

$$E_{tot,C} = 0.091i^2 + 16.06i + 142.1 \text{ } (\mu J) \quad (6.13)$$

6.4 Switching Characterization of SiC Power Module

In this section, a switching characterization is conducted on the commercial SiC power module (Cree CAS100H12AM1, 1.2 kV, 100 A), as Figure 6.18 shows.

The DC-bus for half bridge module used in DPT can inherit its design from the DC-bus of SiC three-phase inverter. The laminated bus bar is widely used to reduce the stray inductance contributed by DC-bus [172–174]. The positive- and negative-planes are made to overlap with each other, with an isolation layer between the two planes. Thus, the two planes are strongly coupled to give a large mutual inductance. The laminated DC-bus PCB is designed to exactly fit the power module CAS100H12AM1. The thickness of copper layer is 9 oz to ensure a current capability up to 100 A, and the thickness of FR4 layer is 2 mm. And the DC-link capacitors consist of 10 parallel 900 V, 4 μ F film capacitors.

Firstly, the influence of gate resistance on the switching characteristics is evaluated as it is a tradeoff between the switching loss and EMI issue. The switching waveforms at 750 V/100 A with 5 different values of R_{on} and 4 different values of R_{off} are shown in Figure 6.19. Both the dv/dt and di/dt ratios keep decreasing with the increase of gate resistance. During the turn-off transition, the voltage overshoot decreases from 113 V to 78 V when R_{off} increases from 5 Ω to 13.3 Ω . Both the ringing and overshoot for voltage and current show an insignificant decreasing tendency with R_{off} increasing. During the turn-off transition, the current overshoot decreases from 38 A to 18 A when R_{on} increases from 4.3 Ω to 13.3 Ω . The current ring and overshoot show a significant decreasing tendency with R_{on} increasing, while the voltage ringing is damped quickly. Hence, the high voltage overshoot at turn-off becomes the bottleneck to limit the switching speed when this SiC power module is expected to operate at its rated current. Since the

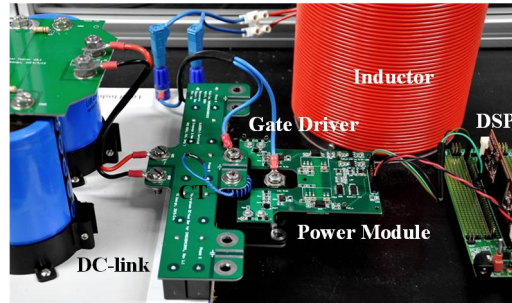


Figure 6.18: Experimental setup of double pulse testing for SiC power module.

CHAPTER 6. SWITCHING CHARACTERIZATION OF SiC POWER DEVICES

Table 6.4: dv/dt and di/dt at 750 V and 100 A for switching characterization of SiC power module.

	Unit	Turn-off	Turn-on
dv/dt	V/ns	16.1	21.1
di/dt	A/ns	4	3.5

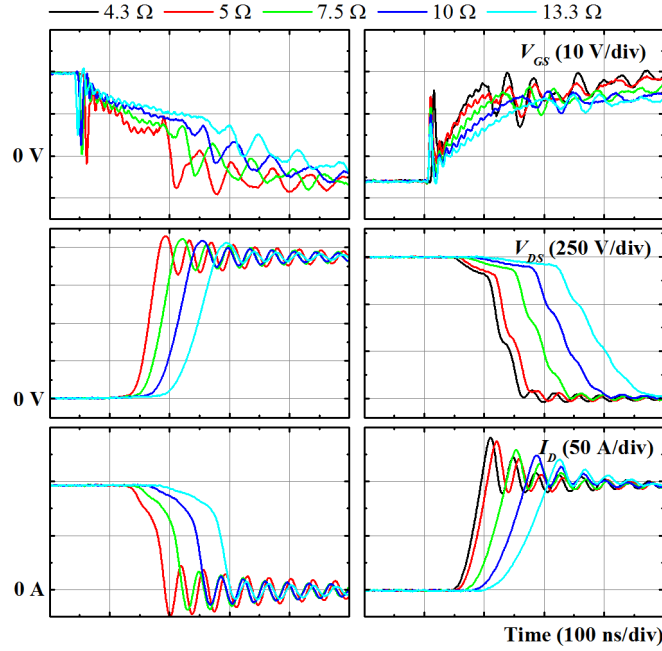


Figure 6.19: Effect of gate resistance on switching characteristics.

blocking voltage of DC-link capacitor is only 900 V, a narrow margin is allowed for the voltage overshoot and R_{off} should be larger than R_{on} to slow down the turn-off speed. In this work, R_{on} is selected to be 4.3 Ω while R_{off} is selected to be 10 Ω . The dv/dt and di/dt ratios are given in Table 6.4.

The switching energy with variation of gate resistance is extracted, as Figure 6.20 shows. Both E_{on} and E_{off} are approximately proportional to the gate resistance. And E_{on} is much larger than E_{off} due to the significant current overshoot at turn-on. In addition, E_{rr} decreases slightly with R_G increasing due to the reduced peak reverse recovery current. The actual switching energy should be smaller than the measured results, since the use of CT is unnecessary in a practical power converter.

The switching characterization is further conducted after removing CT. As

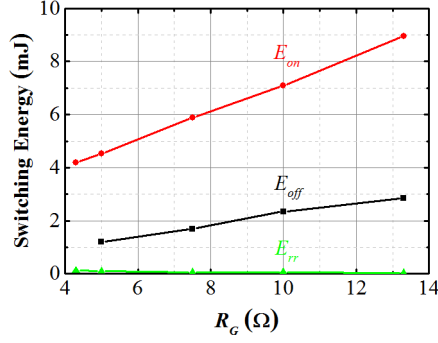


Figure 6.20: Switching loss at different gate resistances.

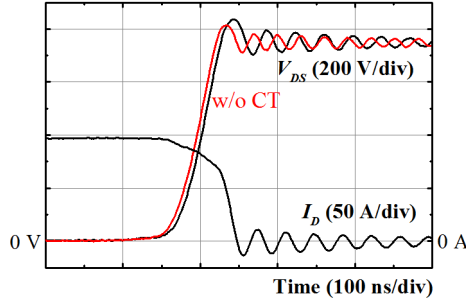


Figure 6.21: Effect of current transformer on voltage overshoot at turn-off.

Figure 6.21 shows, the voltage overshoot at turn-off is reduced from 92 V to 64 V when CT is removed. Applying FFT to the voltage waveform with and without CT, the resonant frequencies are found to be 27 MHz and 33 MHz respectively. And stray inductance L_S can be calculated according to

$$L_S = \frac{1}{(2\pi f)^2 C_{oss}} \quad (6.14)$$

Substituting $C_{oss} = 970$ pF at 750 V, the loop stray inductances with and without CT are calculated to be 35.8 nH and 24 nH respectively. Hence, using of CT will introduce an extra stray inductance of 11.8 nH. Considering the 20 nH stray inductance of power module from the datasheet, the DC-bus designed in this work only contributes a stray inductance of 4 nH. Hence, the module package constitutes the majority of loop stray inductance. And the SiC power module with lower stray inductance package is needed for further improvement in switching speed.

The switching loss of FWD is normally dominated by the reverse recovery

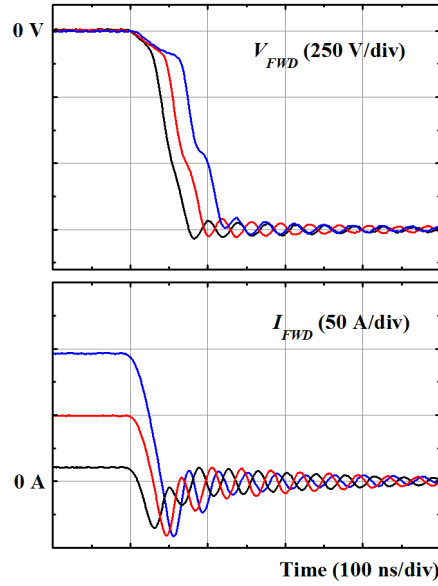


Figure 6.22: Reverse recovery process of SiC power module.

process. The FWD of commercial SiC power module is a combination of body diode of SiC MOSFET and anti-parallel SiC Schottky diode. As discussed in previous section, the reverse recovery process of both diodes are independent of load current. Hence, it can be concluded that the switching loss of FWD is almost independent of load current, as Figure 6.22 shows. In addition, the waveforms of voltage drop across FWD only show slight difference due to Ldi/dt effect.

Furthermore, the influence of load current (10 A, 50 A and 100 A) on the switching characteristics is evaluated, as Figure 6.23 shows. During the turn-off transition, both dv/dt and di/dt ratios will increase significantly with load current increasing. It is because the turn-off speed of MOSFET is dominated by the turn-on speed of its complementary FWD. A higher load current leads to a faster charging process of junction capacitor of diode. During the turn-on transition, the dv/dt and di/dt almost remain constant. Due to the use of high driving voltage in SiC MOSFET, the influence of changing load current on dv/dt can be offset, as Eq.(2.27) illustrates. And di/dt at turn-on is totally independent of load current, as Eq.(2.20) illustrates. The current overshoot is due to the reverse recovery current of HS SiC Schottky diode, resulting in an increased turn-on loss. As discussed in previous section, the reverse recovery process of FWD is almost independent of load current, so do the reverse recovery charge and current overshoot.

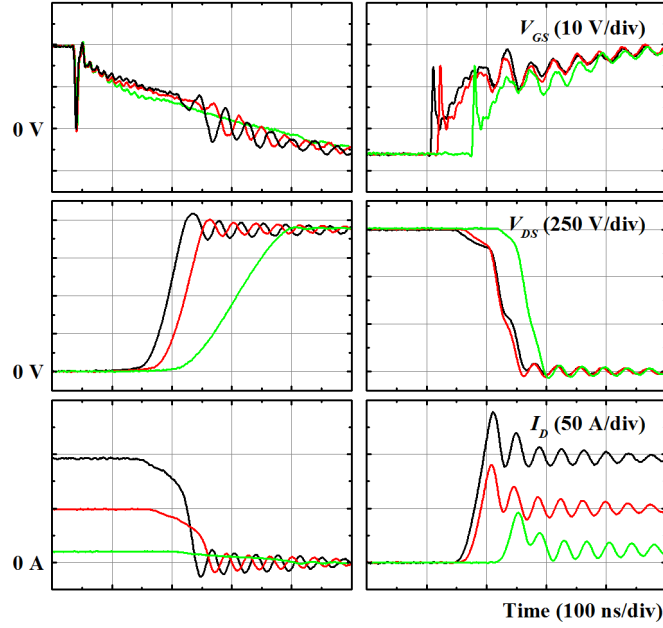


Figure 6.23: Influence of load current on switching characteristics.

The relationship between switching energy and load current is derived, as Figure 6.24 shows. A 2nd-order polynomial curve fitting is applied to the data points and the analytical equations are given by Eq.(6.15)~(6.17). The MOSFET switching loss consists of turn-on loss E_{on} and turn-off loss E_{off} . And the diode switching loss only considers the reverse recovery loss E_{rr} . Both E_{on} and E_{off} increase significantly with load current increasing, meanwhile E_{rr} remains constant as aforementioned. E_{on} is the dominant factor while E_{rr} is the smallest fraction of total switching loss.

$$E_{on} = 8.101 \times 10^{-5} I^2 + 0.0267 I + 0.628 \text{ (mJ)} \quad (6.15)$$

$$E_{off} = 5.686 \times 10^{-5} I^2 + 0.0156 I + 0.0696 \text{ (mJ)} \quad (6.16)$$

$$E_{rr} = -4.666 \times 10^{-7} I^2 + 1.067 \times 10^{-4} I + 0.116 \text{ (mJ)} \quad (6.17)$$

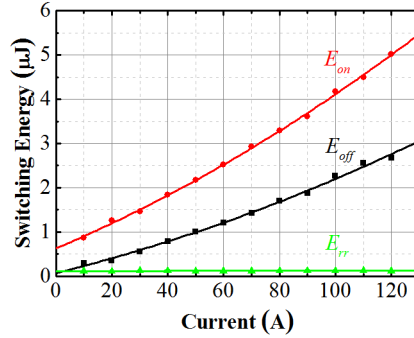


Figure 6.24: Switching energy versus load current at 750 V, dots are experimental results and lines are polynomial fitting results.

6.5 Conclusion

The conclusions of this chapter are summarized below.

Firstly, a universal double pulse testing circuit is set up for switching characterization of SiC power devices. The ESL of DC-link capacitor and EPC of load inductor are minimized in order to obtain a more accurate switching characterization. In addition, the current transformer is used to measure the current.

Secondly, a comprehensive stray inductance modeling and extraction procedure is conducted using Ansys Q3D, including the PCB and packaging stray inductances. The layout of testing circuit is optimized to minimize the power loop and stray inductance. Moreover, the relationship between the stray inductance and lead length for TO-220 and TO-247 packages is modeled. And the stray inductance of SiC power module is also extracted, which matches well with the datasheet.

Thirdly, the reverse recovery process of both SiC Schottky diode and body diode of SiC MOSFET is characterized, which is almost independent of load current. Hence, the body diode can perform as an ideal FWD as SiC Schottky diode. It is also found that the half bridge configuration with only SiC MOSFET shows a higher efficiency than that with extra anti-parallel FWD.

Finally, the switching characterization of SiC power module is conducted with several different turn-on and turn-off resistances to optimize the switching transitions. In addition, the relationship between the switching loss and load current is modeled, which can be used for the power loss calculation in the converter.

CHAPTER 6. SWITCHING CHARACTERIZATION OF SIC POWER
DEVICES

Chapter 7

Development of High Power Density SiC Three-phase Voltage Source Inverter

The last chapter in this work demonstrates two prototypes of SiC two-level three-phase voltage source inverter (VSI), which are implemented in discrete devices and power module respectively. The VSI with discrete devices is based on synchronous rectification to eliminate the use of freewheeling diode. The VSI with power module is designed for aerospace high power density converter application and tested up to 50 kW. In addition, an accurate analytical model for power loss and efficiency calculation of three-phase two-level VSI with SiC MOSFET is also developed.

7.1 Introduction

The pulse-width-modulated (PWM) VSI is widely used in AC motor drive and AC grid-tied converter to produce a sinusoidal AC output whose magnitude as well as frequency can be controlled [51]. Si IGBT used to dominate the application in VSI due to the high voltage and high current capabilities. However, the high switching loss of Si IGBT limits its application where high frequency and high power density are required. And switching frequency of Si IGBT is normally limited below 20 kHz. Replacement of Si IGBT with SiC MOSFET makes it possible to push the switching frequency up to 100 kHz, and therefore to reduce the size of passive devices in filter significantly.

The operation principle of conventional two-level three-phase VSI has been extensively discussed in textbooks and replacement of Si IGBT with the newly emerging SiC MOSFET brings no difference in operation. Hence, the high efficiency and high power density advantages of SiC-based VSI need to be accurately modeled and evaluated instead of its operation. Lots of early works have been conducted on the system-level benefits of SiC power devices compared with Si counterpart.

In [175], the effect of SiC MOSFET and SiC Schottky diode in PWM inverter used in HEV was evaluated with an analytical model of power loss. And it was found that SiC inverter shows a high efficiency of 95% compared with the fluctuated efficiency of 80~90% for Si inverter. In [176], an electro-thermal model for three-phase VSI with SiC JFET was presented. It shows a 8% higher efficiency and 1/8 heat sink size compared with Si inverter. This electro-thermal model for SiC JFET VSI was further investigated for application in HEV [177]. The work in [178] further considered and modeled the reverse conduction mode of SiC normally-off JFET. It was shown that the conduction loss can be reduced significantly by using JFETs in reverse conduction in parallel with diode. In [179], a complete comparison between various Si and SiC power devices was conducted for HEV application. And it was concluded that SiC devices can lead to a reduction in semiconductor losses by more than 50%.

In this work, the three-phase VSI based on the commercial SiC MOSFET, SiC Schottky diode and SiC power module is investigated and prototyped. An accurate analytical model for fast estimation of power loss and efficiency is proposed firstly. The reverse conduction mode of SiC MOSFET and dead time operation mode are both modeled properly. A VSI based on SR with purely 6 SiC MOSFETs is developed and tested, which shows a higher efficiency than the conventional VSI with FWD. Finally, a high power density VSI using SiC power module is designed. It shows a 98% efficiency when operating at 50 kW output power and 60 kHz switching frequency.

7.2 Analytical Model for Power Loss and Efficiency Estimation in SiC Three-phase VSI

To evaluate the efficiency of SiC power converter, the power loss needs to be accurately calculated based on the operating conditions, which is also beneficial for

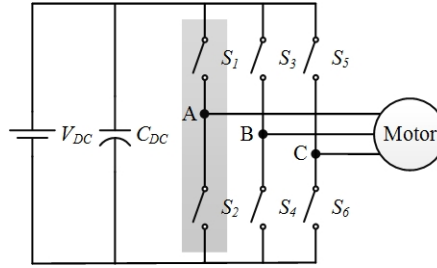


Figure 7.1: Schematic of three-phase inverter for motor drive application.

heat sink design. There are two strategies for power loss calculation: simulation and analytical correlation. The simulation-based strategy requires an accurate circuit simulation model, and is normally implemented in the circuit simulator like PSpice as discussed in Chapter 3. However, an extremely high CPU resource is required since the power loss is calculated during each switching cycle. Hence, the analytical correlation based on averaging method is adopted in this work [175, 180, 181].

The three-phase VSI consists of 6 switches, as Figure 7.1 shows. The sinusoidal reference wave is modulated by a triangle carrier wave to control the HS and LS switches to conduct alternatively. Considering the turn-on and turn-off times of power semiconductor devices, a dead time is required to avoid the arm shoot-through. Although the dead time tends to deteriorate the output harmonics, it ensures the safe operation of power converter. During the dead time, both HS and LS switches are off. For VSI with SR (VSI-SR), the freewheeling current will flow via body diode, while for VSI with FWD (VSI-FWD), it will flow via FWD. Hence, the major difference between these two kinds of inverter is the operation during dead time. In the following section, the ideal VSI with zero dead time is discussed firstly, then followed by the two different operation modes after considering dead time.

A. Ideal Three-phase VSI with Zero Dead Time

Firstly, the power loss of ideal three-phase VSI with zero dead time can be analyzed by the equivalent chopper shown by Figure 7.2. During the positive half-wave cycle, S_1 and S_2 conduct alternatively. When S_1 is off and S_2 is on, the DC-link capacitor starts to charge the inductor via S_2 . When S_1 is on and S_2 is off, the inductor current freewheels via S_1 . Considering the circuit symmetry, only the positive half-wave cycle is discussed in the following work. Since the switching frequency f_s is apparently higher than the modulating frequency f_0 , the reference

CHAPTER 7. DEVELOPMENT OF HIGH POWER DENSITY SIC
THREE-PHASE VOLTAGE SOURCE INVERTER



Figure 7.2: Operation principle of chopper: (a) S_1 off and S_2 on, (b) S_1 on and S_2 off.

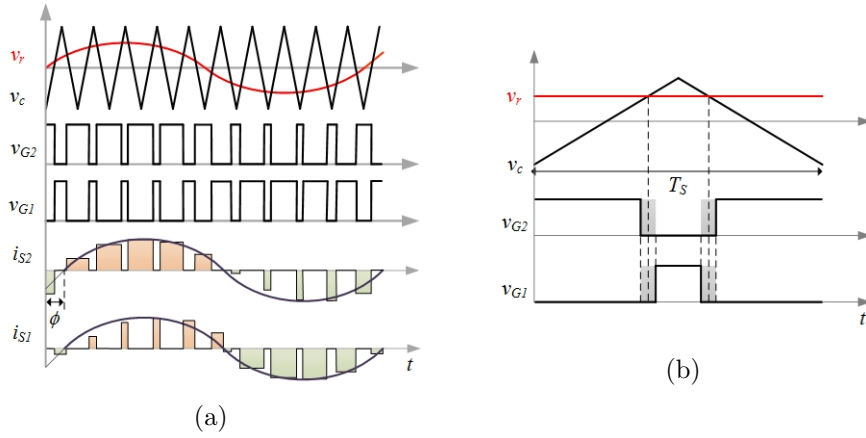


Figure 7.3: Switching waveforms: (a) entire fundamental cycle, (b) one switching cycle during the positive half-wave cycle.

voltage and current flowing via the devices during one switching cycle can be approximated by constant, as Figure 7.3(a) shows. Then the continuous reference voltage and sinusoidal output current can be discretized into

$$v_r(n) = V_r \sin \theta_n \quad (7.1)$$

$$i_o(n) = I_P \sin(\theta_n - \phi) \quad (7.2)$$

$$\theta_n = \frac{2\pi}{N}n, n = 1, 2, \dots, N \quad (7.3)$$

where V_r is the magnitude of reference signal, I_P is the peak value of phase current, N is the frequency modulation ratio and given by $N = f_s/f_0$, and ϕ is the phase angle. From Figure 7.3(b), the duty cycles are derived without consideration of

the dead time

$$D_n' = \frac{V_c - v_r(n)}{2V_c} = \frac{1}{2}(1 - m_a \sin \theta_n) \quad (7.4)$$

$$D_n = 1 - D_n' = \frac{1}{2}(1 + m_a \sin \theta_n) \quad (7.5)$$

where m_a is the amplitude modulation ratio and given by $m_a = V_r/V_c$. During the positive half-wave cycle, the conduction energy of S_2 is a sum of loss for the $N/2$ switching cycles, as given by

$$E_{cond,S2} = \sum_1^{N/2} i_o(n)^2 R_{DS,on} D_n T_s = I_P^2 R_{DS,on} T_0 \left(\frac{1}{8} + \frac{m_a \cos \phi}{3\pi} \right) \quad (7.6)$$

where $R_{DS,on}$ is the on-resistance of SiC MOSFET operating in the 1st quadrant.

During the freewheeling period, the inductor current will freewheel via S_1 as aforementioned. Considering the real circuit configuration in inverter, the current freewheeling path will be different for VSI-SR and VSI-FWD. Due to the high forward voltage drop of SiC body diode, it will never conduct when the reverse channel of MOSFET is conducting or an external FWD is parallel with it. Hence, the freewheeling current will always flow via MOSFET channel for VSI-SR, as Figure 7.4(a) shows. By comparison, the situation for VSI-FWD is a little complicated, since both M_1 and D_1 may conduct, as Figure 7.4(b) shows. At low load current, M_1 shunts the majority of current due to the forward voltage drop across D_1 . With the load current increasing, the freewheeling current shifts from M_1 to D_1 gradually since the MOSFET enters into the saturation region at high current. Considering the typical forward voltage drop of SiC Schottky diode is

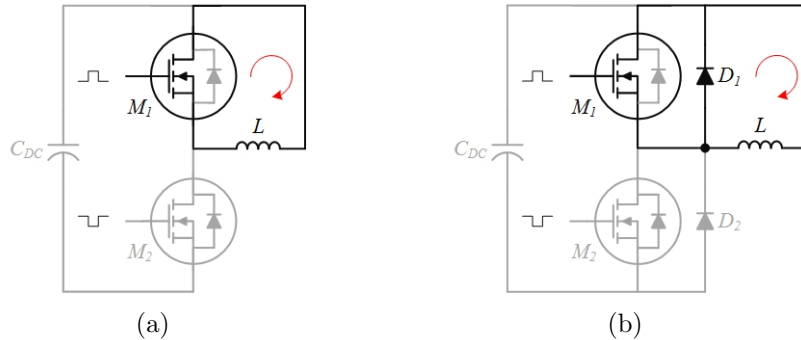


Figure 7.4: Operation principle during freewheeling period: (a) VSI-SR, (b) VSI-FWD.

around 0.8 V, M_1 shunts the majority of freewheeling current when the device is operated below the rated current. Thus the channel current is the dominant factor for 3rd quadrant conduction. Hence, the third quadrant on-resistance $R_{SD,on}$ is used to model the conduction loss. Similar to the discussion above, the conduction energy of S_1 is given by

$$E_{cond,S1} = \sum_1^{N/2} i_o(n)^2 R_{SD,on} D_n' T_s = I_P^2 R_{SD,on} T_0 \left(\frac{1}{8} - \frac{m_a \cos \phi}{3\pi} \right) \quad (7.7)$$

The total conduction loss of the SiC-based three-phase inverter is six times of the sum of Eq.(7.6) and (7.7), then times the modulating frequency

$$\begin{aligned} P_{cond,M} &= 6 (E_{cond,S2} + E_{cond,S1}) f_0 \\ &= 6I_P^2 \left[\frac{1}{8} (R_{DS,on} + R_{SD,on}) + \frac{m_a \cos \phi}{3\pi} (R_{DS,on} - R_{SD,on}) \right] \end{aligned} \quad (7.8)$$

For the switching loss calculation, the physical-based switching loss model proposed in [175,181,182] lacks the accuracy due to the neglect of stray inductance. In addition, it requires several physical parameters of power devices, which are rarely provided by the device manufacturer. Hence, the switching loss calculation mostly relies on the switching energy provided by the datasheet [183]. Assuming the switching energy is a linear function of both voltage and current, it is a scaled value of that from the datasheet. It provides a rough and fast estimation for switching loss calculation. To further improve the accuracy, the switching loss should be obtained from the switching characterization.

The total switching energy of a switch (e.g. S_2) during one switching cycle can be approximated by a polynomial function of output current

$$E_{sw}(n) = ai^2(n) + bi(n) + c \quad (7.9)$$

where a , b and c are the fitting parameters. The switching energy is a sum of loss for the $N/2$ switching cycles

$$E_{sw,S2} = \sum_1^{N/2} E_{sw}(n) = N \left(\frac{aI_P^2}{4} + \frac{bI_P}{\pi} + \frac{c}{2} \right) \quad (7.10)$$

The total switching loss of switch is therefore six times of Eq.(7.10), then times

the modulating frequency

$$P_{sw} = 6E_{sw,S_2}f_0 = 6 \left(\frac{aI_P^2}{4} + \frac{bI_P}{\pi} + \frac{c}{2} \right) f_s \quad (7.11)$$

B. Three-phase VSI with Synchronous Rectification

The operation principle of three-phase VSI-SR can be approached by the chopper shown in Figure 7.5(a). During the dead time when both M_1 and M_2 are off, the inductor current freewheels via body diode of M_1 . Due to the large forward voltage of body diode of SiC MOSFET, the conduction loss dissipated by the body diode becomes no longer negligible, as given by

$$E_{cond,BD1} = 2 \sum_1^{N/2} i_o(n) [V_{BD} + i_o(n) R_{BD}] T_d = N \left(\frac{2I_P V_{BD}}{\pi} + \frac{I_P^2 R_{BD}}{2} \right) T_d \quad (7.12)$$

where V_{BD} is the knee voltage, R_{BD} is the on-resistance of body diode, and the factor 2 is because there are two times of current commutation in one switching cycle. In real situation, the conduction time of body diode should be smaller than the dead time T_d after considering the switching time of MOSFET. To simplify analysis, the worst assumption is made in this work. And the total conduction loss of body diode is given by

$$P_{cond,BD} = 6E_{cond,BD1}f_0 = 6 \left(\frac{2I_P V_{BD}}{\pi} + \frac{I_P^2 R_{BD}}{2} \right) T_d f_s \quad (7.13)$$

C. Three-phase VSI with Freewheeling Diode

The operation principle of three-phase VSI-FWD also can be approached by

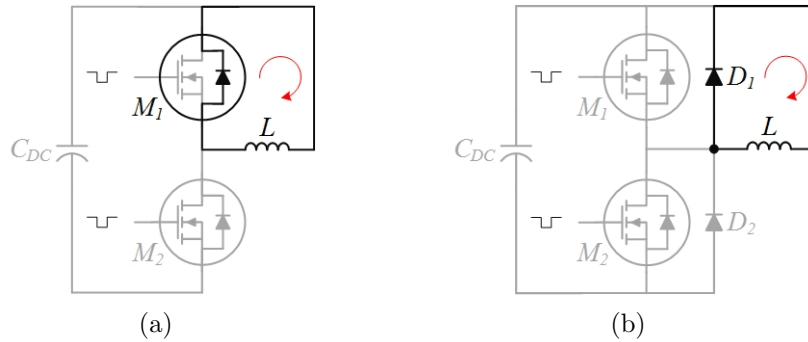


Figure 7.5: Operation principle during dead time: (a) VSI-SR, (b) VSI-FWD.

the chopper shown in Figure 7.5(b). During the dead time when both M_1 and M_2 are off, the inductor current freewheels via D_1 . Similar to previous discussion, the total conduction loss dissipated by FWD is given by

$$P_{cond,D} = 6 \left(\frac{2I_P V_D}{\pi} + \frac{I_P^2 R_D}{2} \right) T_d f_s \quad (7.14)$$

where V_D is the knee voltage, R_D is the on-resistance of FWD.

D. Efficiency Calculation

According to the discussion above, the total power loss of VSI-SR is a sum of Eq.(7.8), (7.11), (7.13)

$$P_{loss} = P_{cond,M} + P_{sw} + P_{cond,BD} \quad (7.15)$$

Similarly, the total power loss of VSI-FWD is given by

$$P_{loss} = P_{cond,M} + P_{sw} + P_{cond,D} \quad (7.16)$$

The output power of three-phase VSI is given by

$$P_{out} = 3V_{LN,rms} I_{LN,rms} \cos \phi \quad (7.17)$$

where $V_{LN,rms}$ and $I_{LN,rms}$ are the rms values of line-to-neutral voltage and current, respectively. Converting the rms value to the peak value, the output power can be rewritten as

$$P_{out} = \frac{3}{2} V_{LN} I_{LN} \cos \phi \quad (7.18)$$

where V_{LN} is the peak value of phase voltage and is given by [51]

$$V_{LN} = m_a \frac{V_{DC}}{2} \quad (7.19)$$

Finally, the inverter efficiency is given by

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} \quad (7.20)$$

7.3 A High-efficiency SiC Three-phase VSI Using Synchronous Rectification

The reactive power in power converter with inductive load requires a current commutation path for the freewheeling current. Due to the high voltage drop of body diode of SiC MOSFET, a SiC Schottky diode is normally recommended as the anti-parallel freewheeling diode for SiC MOSFET to suppress the conduction of body diode. However, since the SiC MOSFET can also function as synchronous rectifier, the freewheeling diode will only conduct during the dead time, leading to a low utilization rate of the device.

The body diode of Si MOSFET suffers from high reverse recovery current and switching loss when used in SR converter. An anti-parallel Schottky diode is normally adopted to suppress the reverse recovery even though it only conducts during the dead time. In Chapter 6, the body diode of SiC MOSFET has been proven to have excellent reverse recovery process, which shows comparable switching performances compared with SiC Schottky diode. Hence, the use of anti-parallel SiC Schottky diode becomes not so indispensable in SiC converter. Although the SiC body diode has a higher forward voltage drop (2.5 V) compared with Si counterpart (0.7 V), the dead time can be minimized to reduce the conduction loss dissipated by the body diode after considering the high speed switching that SiC MOSFET can achieve. Hence, it is of great interest to investigate the benefits to remove the SiC Schottky diode from the existing SiC power converter.

7.3.1 Efficiency Evaluation

The operation conditions of inverter are given by Table 7.1. A unit power factor is assumed. And a narrow dead time of 200 ns is set according to the switching characterization so as to avoid arm shoot-through during current commutation.

Table 7.1: Operation condition of three-phase VSI using discrete SiC devices.

Parameter	Value
V_{DC}	600 V
$\cos \phi$	1
M_a	0.8
f_0	400 Hz
T_d	200 ns

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Table 7.2: Device parameters of SiC MOSFET C2M0080120D and SiC Schottky diode C4D20120A.

Device	Parameter	Value
C2M0080120D	$R_{DS,on}$	89 m Ω
	$R_{SD,on}$	78 m Ω
	V_{BD}	2.2 V
	R_{BD}	38 m Ω
C4D20120A	V_D	0.9 V
	R_D	31 m Ω

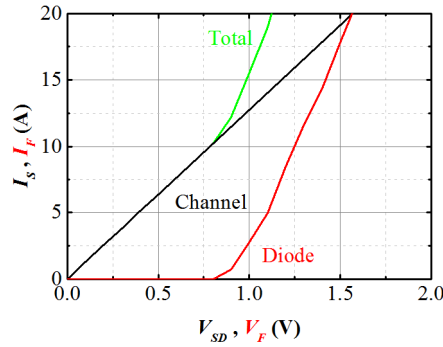


Figure 7.6: Comparison between the 3rd quadrant characteristics of C2M0080120D at 20 V gate bias and the $I - V$ characteristics of C4D20120A.

The 1.2 kV, 20 A SiC MOSFET C2M0080120D and 1.2 kV, 20 A SiC Schottky diode C4D20120A from Cree are used. And the device parameters for efficiency calculation are list in Table 7.2. It can be found that the SiC MOSFET provides an even lower channel resistance when conducting in the 3rd quadrant, which is due to substrate bias effect (body effect) [184]. As Figure 7.6 shows, the reverse channel of SiC MOSFET always shows a lower voltage drop than that of SiC Schottky diode when operating below the rated current of 20 A. Thus it is reasonable to approximate the conduction loss during freewheeling period by the on-resistance of 3rd quadrant of SiC MOSFET.

According to the previous discussion, the fractions of conduction loss for both VSI-SR and VSI-FWD are shown in Figure 7.7. The switching loss is calculated according to the switching characterization results presented in Chapter 6, where case A and C correspond to VSI-SR and VSI-FWD respectively. And the switching loss is shown in Figure 7.8. Due to the high forward voltage drop of body diode, the conduction loss of body diode is always higher than that of FWD. And

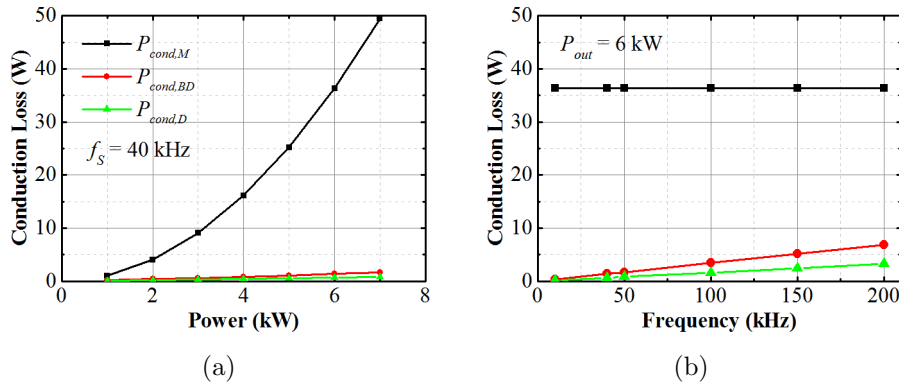


Figure 7.7: Conduction loss at different output power (a) and switching frequency (b).

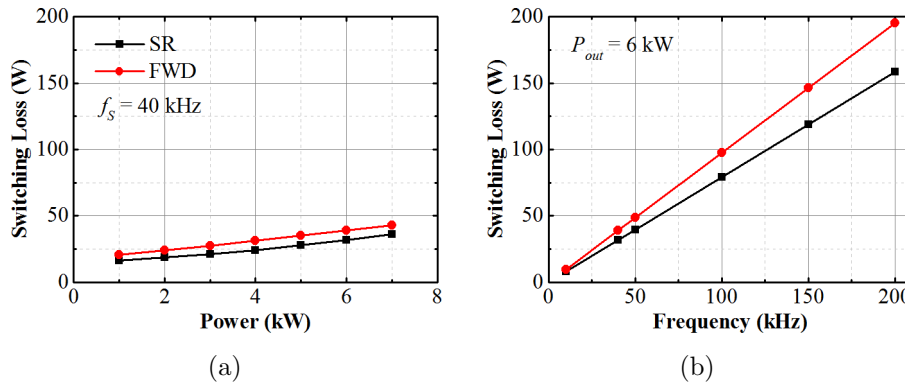


Figure 7.8: Switching loss at different output power (a) and switching frequency (b).

this difference continues to increase with the increasing of output power as well as switching frequency. However, both are negligible compared with the conduction loss of MOSFET. By removing FWD, the VSI-SR shows the advantage in switching loss, especially at light load and high frequency.

When comparing the efficiency of two inverters, VSI-SR always shows a higher efficiency than VSI-FWD no matter at different output power or switching frequency, as shown in Figure 7.9. Even though the conduction loss of body diode is higher than that of FWD during the dead time, it is still much smaller than the switching loss. Hence, it can be easily offset by the lower switching loss of VSI-SR. The two inverters show a similar efficiency at full load, however, the VSI-SR gradually differs from VSI-FWD with frequency increasing.

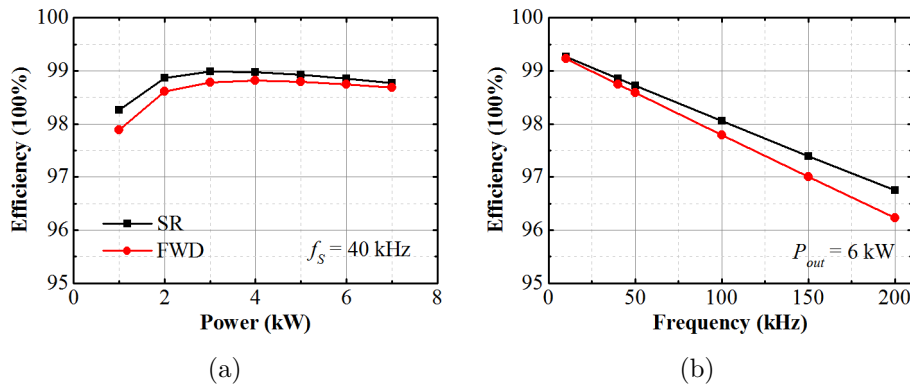


Figure 7.9: Inverter efficiency at different output power (a) and switching frequency (b).

7.3.2 Experimental Verification

The prototype of the three-phase VSI-SR consists of one DC-bus, three phase legs and six gate drivers, all of which are connected with each other by PCB connectors or screws. A clear separation between the controller side and converter side is made so as to avoid the EMI issue. The six SiC MOSFETs are mounted onto a heat sink by screw. And it is cooled by forced air convection.

The experimental setup to test the prototype is shown in Figure 7.10. The open-loop test is conducted with SPWM control and implemented by TI DSP TMS320F28335. The AC output side of inverter is connected to an LC output filter and then followed by a resistive load with Y-connection. The values of

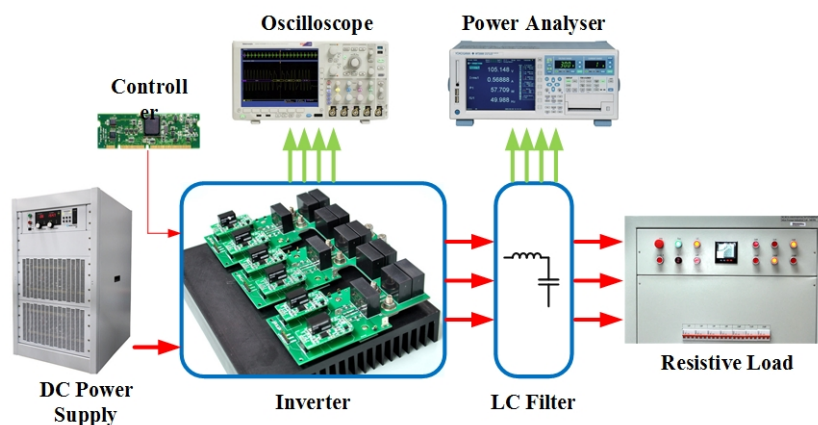


Figure 7.10: Experimental setup for prototype testing.

inductance and AC capacitance are $100 \mu\text{H}$ and $2 \mu\text{F}$, respectively. The inductor is made of E-type amorphous core and Litz wire conductor to suppress the skin effect. A large enough inductance is selected to keep the freewheeling current during the current commutation transition. The DC input voltage V_{DC} , DC input current i_{DC} , phase voltage including v_{AN} , v_{BN} and v_{CN} , phase current including i_A , i_B and i_C are monitored by Yokogawa WT3000 power analyzer.

The prototype is tested up to an output power of 7 kW at a fixed switching frequency of 40 kHz, and the other operation conditions are given by Table 7.1. The experimental waveforms of grid-side (after LC filter) phase voltage and current are shown in Figure 7.11. The total efficiency including converter and filter is measured to be 96.3%. After moving the probes of power analyzer to the converter-side (before LC filter), the pure converter efficiency is found to be 97.7%, and the efficiency predicted by the analytical model is 98.8%. The comparison between analytical model and experimental results are shown in Figure 7.12. Hence, the analytical model predicts around 1% efficiency higher than the measuring results of power analyzer. It is because the bandwidth of current probe used in this work is 120 MHz, which is just a bit higher than the 80 MHz resonant frequency of current ringing. Hence, the current measuring error may lead to the under-estimated current overshoot and ringing, hence predict a higher efficiency.

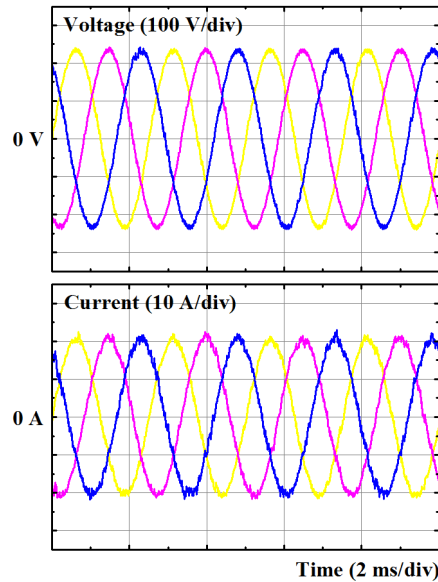


Figure 7.11: Experimental waveforms of grid-side line-to-neutral voltage and current at 7 kW output power.

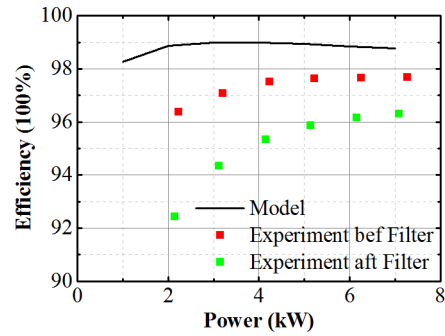


Figure 7.12: Efficiency versus output power at 40 kHz.

7.4 Demonstration of 50 kW SiC High Power Density Converter

In this section, the network side converter (NSC) that connected to the AC grid of aircraft is designed and tested.

The 1st generation prototype of high power density converter is developed based on the commercial SiC power module CAS100H12AM1 (1.2 kV, 100 A). It consists of three SiC power modules, three isolated half bridge gate drivers, a DC-bus bar and a custom-made cold plate, as Figure 7.13 shows. The dimension of 1st generation prototype is 270 mm \times 165 mm \times 35 mm with a volume of 1.56 L. The future generation will integrate more features like controller board, current and voltage sensors for close-loop control, protection schemes in the gate driver unit, output/EMI filters and housing.

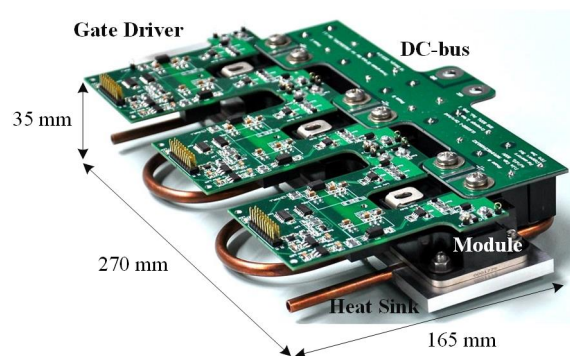


Figure 7.13: Prototype of 1st generation SiC high power density converter.

7.4.1 Efficiency Evaluation

The operation conditions of HPDC are list in Table 7.3. A unit power factor is also assumed similar to previous section. To obtain the line-to-neutral rms voltage of 230 V, the modulation index is calculated be 0.867 as given by the following equation.

$$V_{LN,rms} = m_a \frac{V_{DC}}{2\sqrt{2}} \quad (7.21)$$

Table 7.4 lists the device parameters of SiC power module CAS100H12AM1 for conduction loss calculation. Applying a positive gate bias of 20 V, the $I - V$ characteristics of module working in 1st and 3rd quadrants is shown in Figure 7.14(a). I_D shows a linear relationship with V_{DS} for the continuous operating current between -60 A and 60 A. Based on a linear fit, $R_{DS,on}$ and $R_{SD,on}$ are extracted to be 16.5 m Ω and 13.3 m Ω , respectively. Although $R_{SD,on}$ will decrease at high current above 60 A due to the effect of FWD, the worst situation is assumed to simplify analysis. Similarly, the $I - V$ characteristics of FWD can be obtained by applying a -5 V gate bias, as Figure 7.14(b) shows. Based on a linear fit, R_D and V_D are extracted to be 9.64 m Ω and 0.943 V, respectively.

The switching loss calculation of HPDC is same as VSI-FWD discussed in

Table 7.3: Operation condition of HPDC.

Parameter	Value
P_{out}	50 kW
V_{DC}	± 375 V
$\cos \phi$	1
M_a	0.867
$V_{LN,rms}$	230 V
f_0	400 Hz
f_s	60 kHz
T_d	570 ns

Table 7.4: Device parameters of SiC power module CAS100H12AM1.

Device	Parameter	Value
CAS100H12AM1	$R_{DS,on}$	16.5 m Ω
	$R_{SD,on}$	13.3 m Ω
	V_D	0.943 V
	R_D	9.64 m Ω

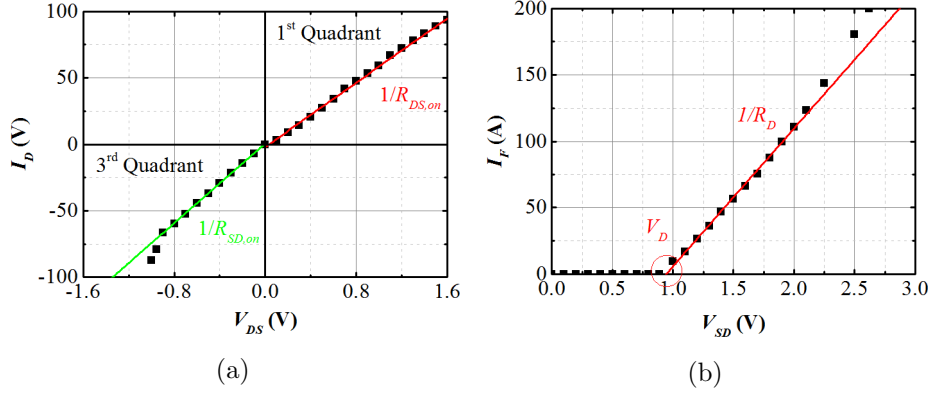


Figure 7.14: $I - V$ characteristics of SiC power module CAS100H12AM1: (a) 1st and 3rd quadrants at $V_{GS} = 20$ V; (b) freewheeling diode at $V_{GS} = -5$ V.

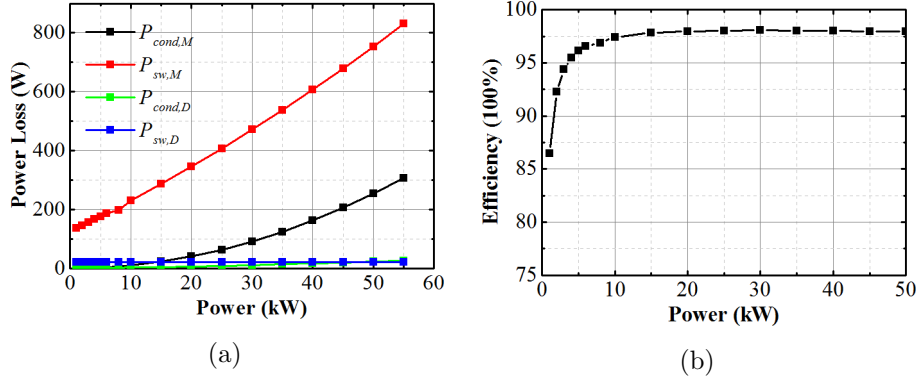


Figure 7.15: Power loss (a) and efficiency (b) with the variation of output power at a constant switching frequency of 60 kHz.

previous section. And the loss dissipated by MOSFET and FWD is discussed separately. The total switching energy of MOSFET is a sum of Eq. (6.15) and (6.16), as discussed in Chapter 6.

$$E_M = 1.3787 \times 10^{-4} I^2 + 0.0423 I + 0.6976 \text{ (mJ)} \quad (7.22)$$

As Figure 7.15 shows, at a constant switching frequency of 60 kHz, the MOSFET conduction loss, MOSFET switching loss and diode conduction loss increase with the output power increasing. However, the diode switching loss keeps constant, since the reverse recovery process of SiC Schottky diode is independent of load current. For the power rating between 10~55 kW, the converter efficiency is above 97%. As Figure 7.16 shows, at a constant output power of 50 kW, the

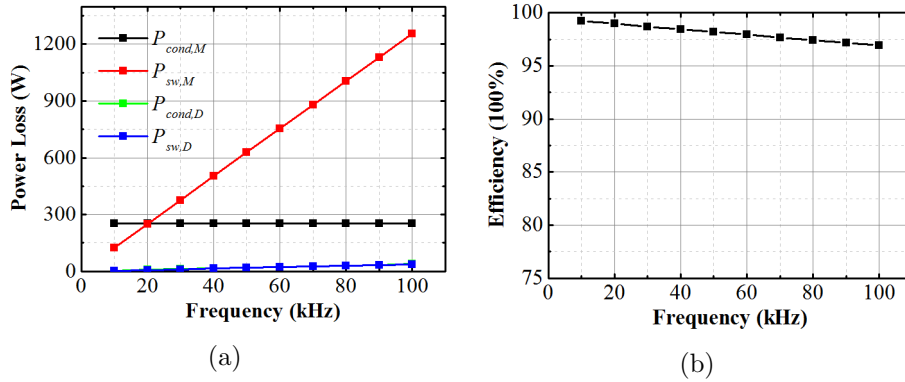


Figure 7.16: Power loss (a) and efficiency (b) with the variation of switching frequency at a constant output power of 50 kW.

MOSFET conduction loss remains constant while the other three values of power loss increase linearly with the switching frequency increasing. For the switching frequency between 10~80 kHz, the converter efficiency is above 97%. Generally, the MOSFET switching loss is the dominant component of total power loss, the only exception is at a low switching frequency (e.g. 10 kHz). In addition, the diode loss, especially conduction loss, is almost negligible compared with the MOSFET loss.

7.4.2 Experimental Verification

The prototype of 1st generation SiC-based HPDC is tested in a similar way as presented in previous section. An open-loop testing is conducted on this prototype with the SPWM control. The AC output side of inverter is connected to an LCL output filter and then followed by an R load with Y-connection. The values of converter-side inductance, AC capacitance and grid-side inductance are 80 μH , 10 μF and 10 μH , respectively. The inductor is made of E-type amorphous core and copper foil conductor to suppress the skin effect. The resistance of R load can vary between 2.7~160 Ω with maximum power up to 60 kW. The DC input voltage V_{DC} , DC input current i_{DC} , grid-side line-to-neutral voltage including v_{AN} , v_{BN} and v_{CN} , grid-side line-to-neutral current including i_{AN} , i_{BN} and i_{CN} are monitored by Yokogawa WT3000 power analyzer. The liquid-cooled heat sink is connected to a heat exchanger with the water coolant at room temperature. And the maximum cooling capacity is 5 kW in power and 5 L in volume. This experimental setup is shown in Figure 7.17.

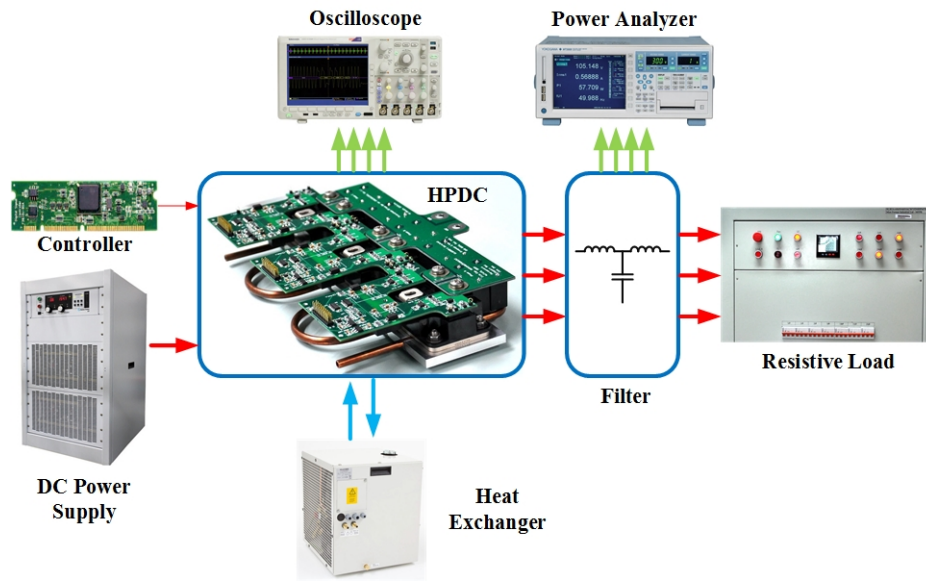


Figure 7.17: Experimental setup for prototype testing.

This prototype is tested up to 50 kW. The measuring results of power analyzer for an input power of 50 kW is shown in Figure 7.18. At this input power, the total efficiency is found to be 97.02%. After moving the power analyzer to the converter-side, the pure converter efficiency is found to be 97.77%, which matches perfect with the analytical model of 97.94%. Hence, the converter loss is the dominant factor of total power loss.

The relationship between efficiency and input power at a fixed switching frequency of 60 kHz is evaluated, as Figure 7.19 shows. The experiment shows that this prototype can still permit a high efficiency above 97% even after considering the power loss of output filter at an input power of 20~50 kW and a switching frequency of 60 kHz. In addition, the experimental result of pure converter efficiency excluding LCL filter shows exactly same as the analytical model.

CHAPTER 7. DEVELOPMENT OF HIGH POWER DENSITY SIC
THREE-PHASE VOLTAGE SOURCE INVERTER

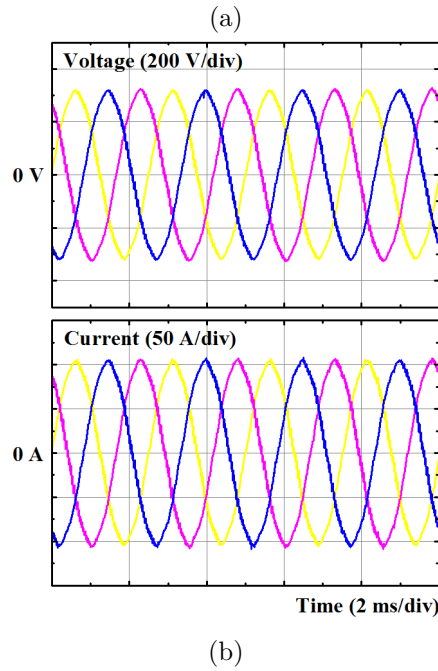
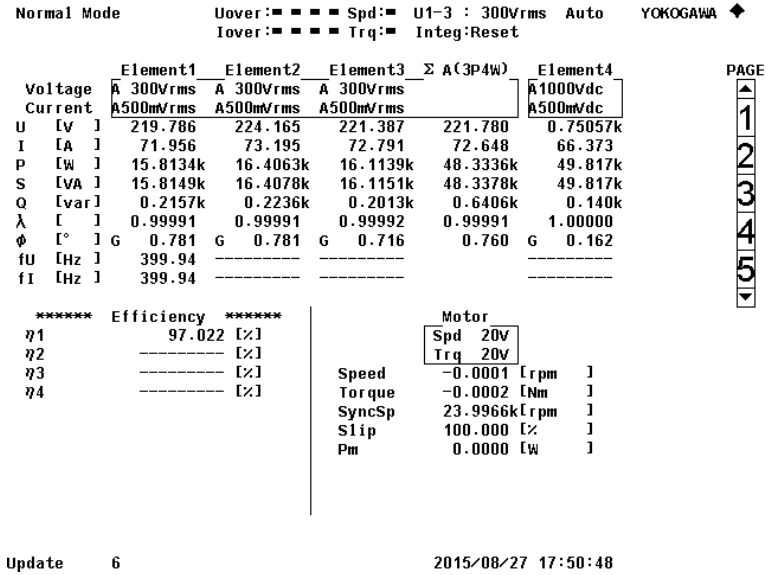


Figure 7.18: Measurement results of power analyzer: (a) numeric, (b) waveform.

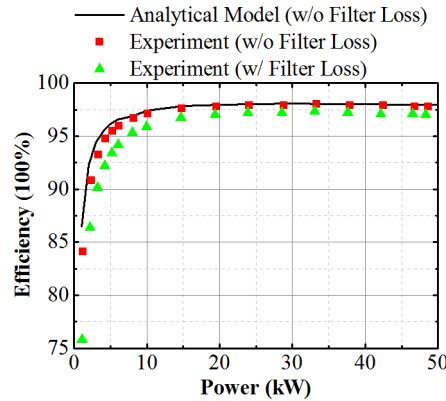


Figure 7.19: Efficiency versus output power at 60 kHz.

7.5 Conclusion

The conclusions of this chapter are summarized below.

Firstly, an accurate analytical model for fast estimation of power loss and efficiency in three-phase VSI is presented. By considering the 3rd quadrant characteristics of SiC MOSFET, two types of VSI (using SR and FWD) are investigated.

Secondly, a three-phase VSI using SR is developed with 6 SiC MOSFETs and tested up to 7 kW. It shows a 98% efficiency when operating at a switching frequency of 40 kHz. Compared with the conventional VSI with FWD, it shows reduced switching loss, especially at light load and high switching frequency. By removing the anti-parallel SiC Schottky diode, the power density in terms of weight as well as volume will increase. In addition, it brings additional benefits including reduced cost, improved system reliability and simplified converter layout design.

Finally, the prototype of 1st generation SiC-based HPDC for MEA application is developed and tested to the maximum power of 50 kW, hence it permits a maximum power density of 32 kW/L. It achieves a high efficiency up to 97.77% at 60 kHz switching frequency. On the other hand, the efficiency predicted by the model is 97.9%, which agrees well with the experiment.

Chapter 8

Conclusion and Future Work

8.1 Conclusion

In this thesis, the key technologies related to the development of a SiC-based high power density converter for application in more electric aircraft are investigated. The conclusions of this work are summarized as below.

The accurate circuit simulation models for the commercial SiC Schottky diode, MOSFET and half bridge power module from Cree are developed and implemented in the circuit simulator PSpice. For the SiC Schottky diode, a physics-based and temperature-dependent circuit simulation model is developed. A parameter extraction procedure is proposed and the geometry as well as physical parameters can be extracted from the $I - V$ and $C - V$ characteristics. For both the SiC MOSFET and module, the behavior-based circuit simulation models are developed. An accurate model for the nonlinear Miller capacitance is proposed, which accounts for the different doping concentrations in the JFET and drift regions. And the circuit simulation model shows a good agreement with the experimental results obtained from double pulse testing.

The SiC MOSFET is normally driven with high-speed switching to minimize the switching loss. However, the high dv/dt and di/dt during the switching transition will bring new challenges in high-speed gate driver design. A novel gate assisted circuit is proposed to eliminate the Cdv/dt effect with a local low impedance path for the Cdv/dt current. In addition, it also bypasses the discharging current and thus improves the turn-off speed as well as reduces the turn-off loss.

The use of high gate driving voltage and fast rise time in gate driver design results in a rapid current rise at turn-on, which tends to aggravate any short-

circuit fault. A novel high-speed short-circuit protection scheme for SiC MOSFET is presented. By monitoring the gate charge, the proposed circuit shows fast response time as well as reduced peak current. From the simulation verification, it shows a response time of less than 200 ns to shut down the short-circuit current when subjected to HSF and FUL conditions.

To further increase the converter power density from the point of view of thermal design, the integrated micro-channel heat sink is proposed for SiC power module. A single-phase, laminar flow, rectangular and AlN-based MCHS with water coolant is designed and optimized. For a pressure drop of 66.6 kPa, a thermal resistance of 0.128 K/W from junction to ambient is achieved, which is substantially lower than the junction to case thermal resistance (0.22 K/W) of the commercial SiC power module. To further improve the cooling efficiency, a double-sided packaging structure with micro-channel cooling is proposed. In addition, it also allows 3-D packaging technology to further increase power density. With the opposite fluid flows, it shows a uniform temperature distribution and the smallest thermal resistance (0.058 K/W). In addition, an analytical model for micro-channel heat sink considering various scaling effects is developed for fast geometry optimization without the need of time-consuming CFD simulation.

For the SiC power converter operating at high frequency, the stray inductance has become a more and more important factor in limiting the overall system performance. The stray inductance needs to be minimized with a careful layout design. The stray inductances of the PCB as well as packaging (TO-220, TO-247 and module) are modeled and extracted by Ansys Q3D. And it is concluded that the packaging stray inductance is the dominant component of the loop inductance.

The comprehensive switching characterizations are conducted on SiC Schottky diode, MOSFET and power module using a universal double pulse testing setup. The reverse recovery process of both SiC Schottky diode and body diode of SiC MOSFET are found to be almost independent of load current. Hence, the body diode can perform as an ideal FWD as SiC Schottky diode. In addition, the switching characterization of SiC power module is conducted with several different turn-on and turn-off resistances to optimize the switching transitions. The relationship between the switching loss and load current is modeled, which can be used for the power loss calculation in the converter.

An accurate analytical model for fast estimation of power loss and efficiency in three-phase VSI is presented. It fully considers the 3rd quadrant operation model of SiC MOSFET. Two kinds of VSIs with and without external FWD are

investigated and modeled.

A prototype of 7 kW three-phase VSI using SR is developed, which only consists of 6 SiC MOSFETs. It shows a 98% efficiency when operating at a switching frequency of 40 kHz. Compared with the conventional VSI with FWD, it shows reduced switching loss, especially at light load and high switching frequency. It proves the system-level benefits to remove the anti-parallel SiC Schottky diode from existing VSI.

A prototype of 1st generation SiC-based HPDC for MEA application is developed and tested to the maximum power of 50 kW. It shows a maximum power density of 32 kW/L. It achieves a high efficiency up to 97.77% at 60 kHz switching frequency. This value also shows a good agreement with that predicted by model.

8.2 Future Work

Based on the work conducted for this thesis, the recommended further works are summarized below.

A. Next Generation HPDC with Higher Power Density and More Features

The 1st generation HPDC prototype developed in this work is based on the 1st generation commercial SiC half bridge module from Cree. Since Cree has just released the 2nd generation module with higher current rating, lower stray inductance and lower thermal inductance, the power module should be replaced in the next generation HPDC. The prototype of 2nd generation HPDC has already been developed and the testing is on-going, as Figure 8.1 shows. In addition, to develop a more complete power converter system, the future generation HPDC should integrate more features like the current and voltage sensors for close-loop control, protection circuits, output filter, advanced heat sink and housing.

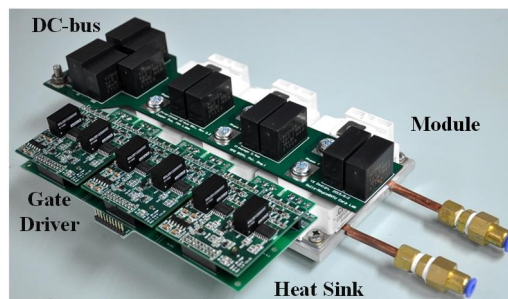


Figure 8.1: Prototype of 2nd generation HPDC.

B. Power Electronics Packaging

The packaging stray inductance of the commercial module has become the bottleneck to further increase the switching frequency of SiC power converter. Several recent studies have demonstrated packaging approaches that can reduce module stray inductance to just under 5 nH. Hence, the custom-made module with advanced power electronics packaging technology for low stray inductance is the primary goal.

Although SiC can allow a theoretical junction temperature up to 600 °C, the lack of high temperature packaging technology still limits the overall junction temperature of module below 200 °C. Hence, development of high temperature packaging technology is desired for the harsh environment that exists in aerospace application. To further reduce the size of cooling system, it is desired to integrate the heat sink inside the module, thus to minimize the conductive thermal resistance of conventional multi-layer packaging structure. By integration of micro-channel heat sink, the size can be minimized and cooling efficiency can be maximized, which is the ultimate goal for thermal design in HPDC.

C. Hardware Implementation of Short-circuit Protection Scheme

The short-circuit protection scheme based on gate charge detection is proposed in this work. Due to the complexity of the high-speed analog circuit design, it is difficult to implement in hardware. Nevertheless, it is a promising technology for reliable short-circuit protection due to the fast response time. In addition, it does not require any additional components to obtain the feedback signal from the power converter circuit. It is completely practical to integrate the function block of gate charge detection inside the gate driver IC. Hence, hardware implementation by IC design may be a possible solution.

D. Multilevel Inverter

To further increase switching frequency and reduce EMI issues, the multilevel inverter becomes an attractive solution. The neutral point clamping (NPC) and T-type three-level inverters have been investigated in our early work [116] and will be considered for the further generation of HPDC.

E. Power Electronics Building Block

The concept of PEBB was proposed to improve the quality, reliability and reduce cost in power electronics system by an integrated approach [185]. It permits a standard and plug-and-play interface to fasten the development and prototyping of power converter. SiC is especially attractive for PEBB application due to the high switching frequency and high junction temperature.

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- [1] **Shan Yin**, K. J. Tseng, C. F. Tong, R. Simanjorang, and *et al.*, "Design and optimization of SiC synchronous rectification voltage source inverter by switching characterization", submitted to IEEE Trans. Power Electron.
- [2] **Shan Yin**, K. J. Tseng, C. F. Tong and R. Simanjorang, "High-speed gate driver design to reduce switching loss and eliminate dv/dt effect for SiC power module", submitted to IEEE Trans. Power Electron.
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