

Power-Efficient Explicit-Pulsed Dual-Edge Triggered Sense-Amplifier Flip-Flops

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Abstract—A novel explicit-pulsed dual-edge triggered sense-amplifier flip-flop (DET-SAFF) for low-power and high-performance applications is presented in this paper. By incorporating the dual-edge triggering mechanism in the new fast latch and employing conditional precharging, the DET-SAFF is able to achieve low-power consumption that has small delay. To further reduce the power consumption at low switching activities, a clock-gated sense-amplifier (CG-SAFF) is engaged. Extensive post-layout simulations proved that the proposed DET-SAFF exhibits both the low-power and high-speed properties, with delay and power reduction of up to 43.3% and 33.5% of those of the prior art, respectively. When the switching activity is less than 0.5, the proposed CG-SAFF demonstrates its superiority in terms of power reduction. During zero input switching activity, CG-SAFF can realize up to 86% in power saving. Lastly, a modification to the proposed circuit has led to an improved common-mode rejection ratio (CMRR) DET-SAFF.

Index Terms—Clock-gated, high-performance, low-power, sense-amplifier flip-flop.

I. INTRODUCTION

IN many digital very large scale integration (VLSI) designs, the clock system that includes clock distribution network and flip-flops, is one of the most power consumption components. It accounts for 30% to 60% of the total system power, where 90% of which is consumed by the flip-flops and the last branches of the clock distribution network that is driving the flip-flop [1]. With the recent trend in frequency scaling and deep pipelining, this clocking system power may be even more pronounced. As the power budget of today's portable digital circuit is severely limited, it is important to reduce the power dissipation in both clock distribution networks and flip-flops. Moreover, because of the tight timing budget at high frequency operation, the latency of the flip-flops should be minimized. Hence, the ability to achieve a design that ensures both power consumption and small latency is essential in modern VLSI technology.

The dual-edge triggering is an important technique to reduce the power consumption in the clock distribution network. By

utilizing dual-edge triggering, the flip-flop is capable of sampling data on both rising and falling edges of the clock so that only half the clock frequency is needed to obtain the same data throughput of single edge-triggered flip-flops (SETFFs) [2]. Recently, several low-power high-speed DETFF structures have been proposed [3]–[10].

In this work, we extensively studied the operation of existing flip-flop architectures, analyzed their weaknesses and proposed new sense-amplifier based flip-flop circuits (hereinafter, referred to as a “SAFF” circuit) due to its differential characteristics, fast operation speed, and low-power consumption. This SAFF circuit is implemented by various approaches within digital circuits such as microprocessors, digital signal processing units, and the like. The first flip-flop achieves substantial power reduction by concurrently incorporating dual-edge triggering and conditional precharging. It also minimizes the latency by making use of a fast symmetrical latch. By using our first proposed design as the baseline circuit, we developed a novel clock gating flip-flop circuit to further reduce the power dissipation and at low input switching activity, the second proposed design promises an even greater amount of power savings.

For the rest of the paper, we organize our discussions in the following manner. In Section II, the recently published state-of-the-art dual-edge triggered flip-flops (DETFFs) are reviewed. Section III presents the structure and operating principle of the two proposed designs. In Section IV, the simulation methodology employed for flip-flop comparison with recently published designs, namely, the static output-controlled discharge flip-flop (SCDFF) [8], the dual-edge triggered static pulsed flip-flop (DSPFF) [9], and the adaptive clocking dual-edge triggered sense amplifier flip-flop (ACSFAFF) [10], respectively. In Section V, we describe a modified version of the DET-SAFF that showed an improved common-mode rejection ratio (CMRR). Finally, we draw our conclusion in Section VI.

II. REVIEW OF STATE-OF-THE-ART DUAL-EDGE TRIGGERED FLIP-FLOPS

A. Static Output-Controlled Discharge Flip-Flop

The schematic diagram of the static output-controlled discharge flip-flop (SCDFF) is illustrated in Fig. 1. SCDFF involves an explicit pulse generator and a latch that captures the pulse signal. The latch structure of SCDFF consists of two static stages. In the first stage, input D is used to drive the precharge transistor so that node X follows D during the sampling period. In addition, the conditional discharging technique is implemented by inserting a QB-controlled nMOS in the discharge

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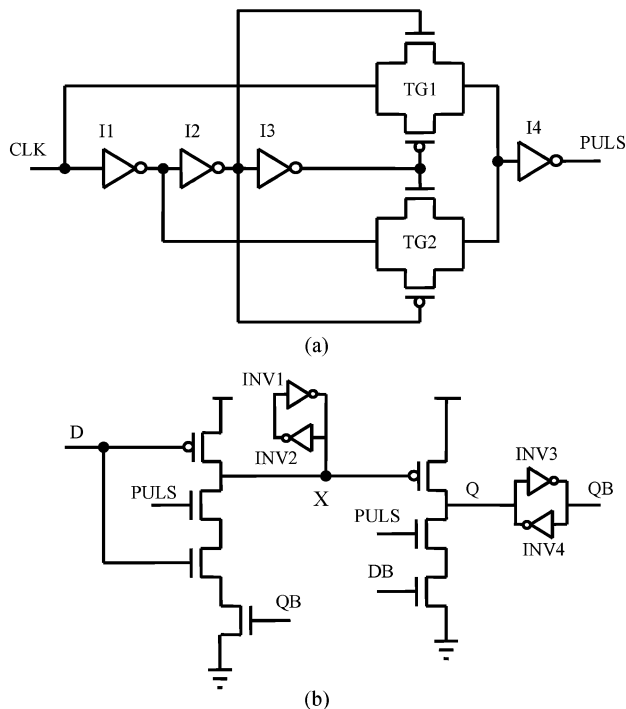


Fig. 1. Static output-controlled discharge flip-flop (SCDFF): (a) dual pulse generator and (b) static latch.

path, which prevents unnecessary discharging at node X as long as the input remains high. The major advantage of SCDFF is low power consumption and soft-edge property. However, a delay is always presented between Q and QB due to the single-ended nature of SCDFF.

B. Dual Edge-Triggered Static-Pulsed Flip-Flop

The dual-edge triggered static pulsed flip-flop (DSPFF) is shown in Fig. 2. In its pulse generator, the four inverters are used to generate the inverted and delayed clock signals. These signals along with two nMOS pass transistors create a narrow sampling window at both the rising and falling edges of the clock. Once the PULS signal is generated, both pass transistors, N1 and N2, are turned on to capture the inputs data so that either SB or RB will be discharged. A smaller delay can be obtained since DB and D are directly fed to the nodes, SB and RB, respectively. The pMOS transistors, P1 and P2, together with two weak nMOS transistors, N3 and N4, effectively avoid the floating of nodes SB and RB when the flip-flop is opaque, thereby providing a fully static operation. The explicit pulse generator is simple and suitable for dual-edge triggering. The static feature of DSPFF eliminates unnecessary transitions. Symmetrical output delays can be obtained by carefully sizing the transistors' aspect ratios. However, the flip-flop latency may be degraded due to the large capacitive loads at the SB and RB nodes. On top of that, DSPFF suffers from high leakage current. This is caused by a high-voltage drop across either transistor N3 or N4, when they are off.

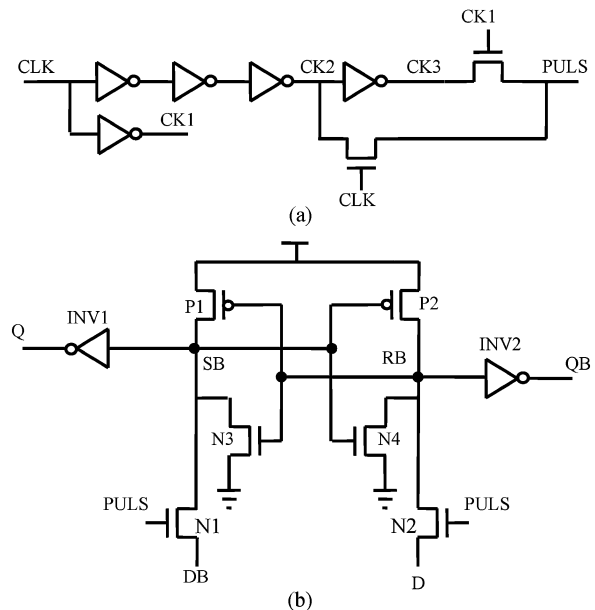


Fig. 2. Dual edge-triggered static pulsed flip-flop (DSPFF): (a) dual pulse generator, and (b) static latch.

C. Adaptive Clocking Dual Edge-Triggered Sense-Amplifier Flip-Flop

The schematic diagram of adaptive clocking dual-edge triggered sense amplifier flip-flop (ACSAAF) is presented in Fig. 3. ACSAAF is an implicit dual-edge triggered sense amplifier flip-flop. It consists of three stages, i.e., the adaptive clock inverting stage, the front-end sensing stage and the Nikolic's latch [11] stage. The adaptive clock inverter chain is designed to disable some internal clocked transistors when the data switching activity is low. The signal derived from node NC of the sensing stage is used to implement adaptive clocking. If input D is different from output Q, node NC will be pulled up, to turn on transistors N1 and N2. Consequently, the desired inverted and delayed signals, CLK3 and CLK4, will be produced so that a narrow transparent window is created on the rising or falling edges of the clock. Either SB or RB will be discharged during this transparent period, changing the output state in the latching stage. Once the output state is altered, the charging path of NC is blocked and NC will be discharged through either N3 and N4 or N5 and N6, thereby disabling the inverter chain. When D is the same as Q, node NC is low and the flip-flop is opaque. ACSAAF obtains great power reduction at low switching activity. Nevertheless, the adaptive clocking requires more transistors and hence causing the circuit to be more complex. This will lead to greater power consumption at high switching activity and the degradation of the flip-flop speed.

Since the front-end sensing stage of ACSAAF [see Fig. 3(a)] is a differential pair like the sense-amplifier, the ratio of the desired differential-mode gain (A_{dm}) to the undesired common-mode gain (A_{cm}) is analyzed. The magnitude of this ratio is defined as the common mode rejection ratio (CMRR) [12]

$$CMRR = \left| \frac{A_{dm}}{A_{cm}} \right|. \quad (1)$$

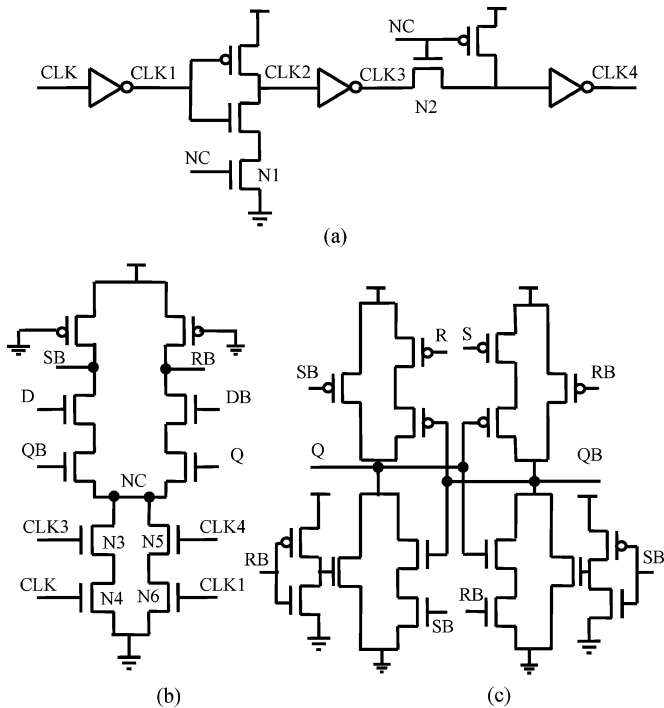


Fig. 3. Adaptive clocking dual edge-triggered sense-amplifier flip-flop: (a) adaptive clocking inverter chain; (b) front end sensing stage; and (c) Nikolic's latch.

CMRR serves as a measure of the amount of wanted signal to the unwanted corruption that appears at the output when the input contains both the differential component and common-mode noise. The CMRR of ACSAFF [10] is the same as that of conventional differential amplifier and is given as follows [12]:

$$\text{CMRR}_{\text{ACSAFF}} = \left| \frac{A_{\text{dm}}}{A_{\text{cm}}} \right| = 1 + 2(g_m + g_{mb})R_{\text{Total}} \quad (2)$$

where g_m and g_{mb} are the transconductance and body-effect transconductance of the common-source amplifier, respectively. R_{Total} is the total resistor of the tailed transistors (N3–N6).

III. PROPOSED DUAL-EDGE TRIGGERED FLIP-FLOPS

In this section, two new dual edge-triggered sense-amplifier flip-flops are constructed and discussed. The first proposed flip-flop is named the dual edge-triggered sense-amplifier flip-flop (DET-SAFF) and the second one, the clock gating sense-amplifier flip-flop (CG-SAFF).

A. Dual-Edge Triggered Sense-Amplifier Flip-Flop

The schematic diagram of the proposed DET-SAFF is given in Fig. 4. It consists of three stages: the pulse generating stage, the sensing stage and the latching stage. The simple pulse generator used in DETSAFF is the same as that of [13]. The dual edge-triggered pulse generator produces a brief pulse signal synchronized at the rising and falling clock edges. The pulse generator can be shared by multiple flip-flop circuits when a group of flip-flops are located closely.

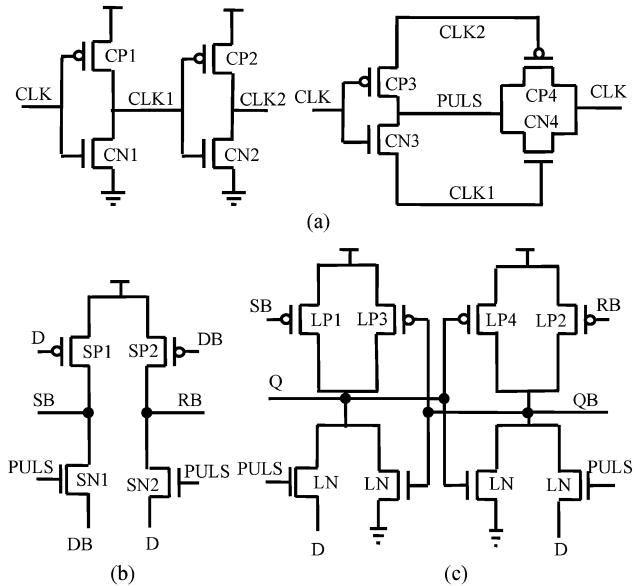


Fig. 4. Proposed dual edge-triggered sense-amplifier flip-flop: (a) dual pulse generator; (b) sensing stage; and (c) symmetric latch.

For a sense amplifier based flip-flop, in the evaluation phase, as soon as D is low, SB will be set to high, and if D is high, RB will be set to high. Therefore, the conditional precharging technique is applied in the sensing stage of DET-SAFF, to avoid redundant transitions at major internal nodes. Two input controlled pMOS transistors, SP1 and SP2, are embedded in the precharge paths of nodes SB and RB, respectively. In this case, if D remains high for n cycles, SB may only be discharged in the first cycle. For the following $(n - 1)$ cycles, SB will be floating when PULS is low or fed to the low state DB when PULS is high. As for RB, it only needs to be precharged in the first cycle and remains at its high state for the remaining cycles. Since the precharging activity is conditionally controlled, the critical pull down path of SB and RB is simplified, consisting of only one signal transistor. This helps to reduce the discharging time significantly. As such, the resulting sensing stage possesses low-power and high-speed features.

To further improve the operating speed, a fast symmetric latch is developed. Similar to the Nikolic's latch and Strollo's latch [14], the new latch makes use of SB and RB to pull up the output nodes. But the pull down path is modified. It composes a PULS-controlled nMOS pass transistor, through which D (DB) is directly fed to the Q (QB) node. This topology significantly speeds up the high-to-low output transition because the output latch immediately captures the input value once the PULS signal is generated. On the other hand, the low-to-high latency will also be improved. This is because the output node will not only be charged by the pull-up transistors, LP1 and LP2, but also the pass transistors, LN1 and LN2. Note that the pass transistors cannot fully charge a node to high, but it can assist with the pull-up transition. The four inner transistors, LP3, LP4, LN3, and LN4, are of minimum sizes, serving the purpose of maintaining the output state when the flip-flop is opaque.

For the proposed DETSAFF and previously mentioned dual-edge designs, such as the SCDF and DSPFF, the power saving

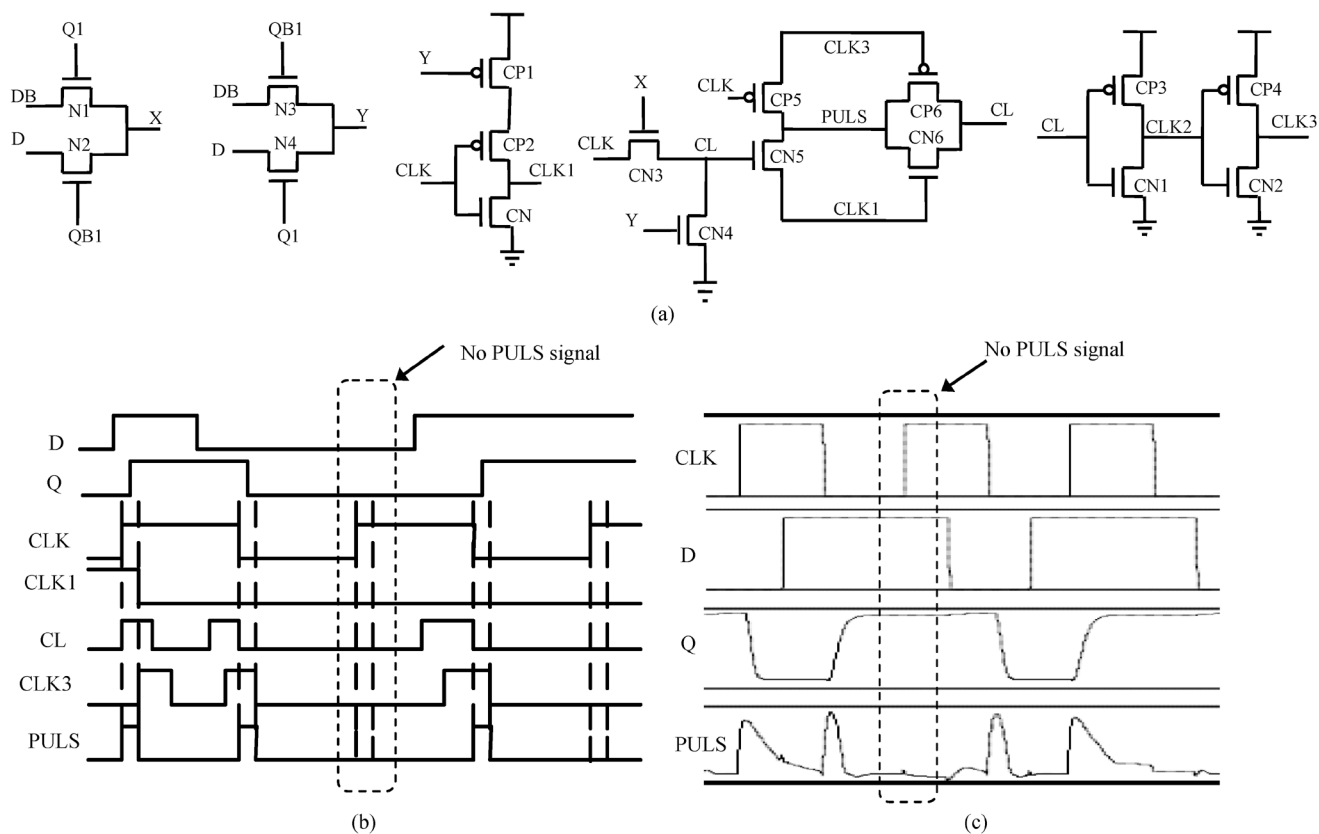


Fig. 5. Proposed clock-gated pulse generator: (a) schematic diagram; (b) timing diagram; and (c) simulated waveform.

techniques are only applicable for the latch part of the flip-flops. As the switching activity of the clock signal is 1, the pulse generator will always be operating even when the input invokes no output changes. These unnecessary transitions cause a lot of power to be wasted, especially at low input switching activities.

B. Clock-Gated Sense-Amplifier Flip-Flop

In order to eliminate the redundant transitions in the pulse generator, the CG-SAFF is constructed. It utilizes the DET-SAFF design as a baseline and incorporates the clock gating technique.

In CG-SAFF, the clock gating technique is implemented by embedding a control circuit in the explicit pulse generator so that the PULS signal generation is disabled in a redundant event. The schematic and timing diagrams of the clock gated pulse generator are shown in Fig. 5.

In order to compare the previous and current input values, two comparators are applied to produce signals X and Y, by using the differential inputs, D and DB, and the buffered outputs, Q1 and QB1, as control signals. If D is different from the output Q1 (Q), X will be pulled up to high and Y to low. Transistor CN3 is turned on to allow the clock signal to pass through as CL. CL is known as the gated clock. At the same time, CP1 is on and drive the CLK1 signal to high before the rising edge of the clock. At the rising edge of the clock, CL is high and its delayed signal CLK3 remains low. Therefore, transistor CN5 and the transmission gate are turned on, driving the PULS signal to high. After a short period, the transparent window is closed as CLK1 goes low and CLK3 is pulled up. Thus, a short transparent

period is created at the rising edge of the clock. Note that signal CLK1 is used for pulse generation rather than CLK2. Such design aims to ensure that the flip-flop only captures the data at the triggering edge of the clock, thereby preventing race problems. At the falling edge of the clock, CL is low and CLK3 is high. Transistor CP5 is selected and generates a high PULS signal. The sampling window is shut down once CLK3 is low. When the input D remains the same in consecutive clock cycles, X is low and Y is high. CL is pulled down by CN4 so that the corresponding CLK3 will be low regardless of the CLK signal. CLK1 may only be discharged at the first clock cycle and maintains its low state in the remaining clock cycles. As a result, the flip-flop will remain opaque and thus, the power can be saved.

The sensing and latching stages of the proposed CG-SAFF are illustrated in Fig. 6. The sensing stage is the same as DET-SAFF. Since the generated PULS signal is more heavily loaded than that of DET-SAFF, a modified Nikolic's latch [15] is used. It does not require any clock signal and provides the most stable operation. The inner holding topology is modified to obtain buffered differential outputs, Q1 and QB1, with reduced load capacitances. In the clocking stage, Q1 and QB1 are used to generate X and Y instead of using Q and QB. This helps to improve the performance of CG-SAFF significantly.

The CMRR performance of the front-end sensing stage of the proposed SAFF is also analyzed and $CMRR_{Proposed}$ is unity. This is because the differential gain (A_{dm}) and common mode gain (A_{cm}) of the proposed sensing stage are the same. A detailed small-signal analysis of $CMRR_{Proposed}$ is given in the Appendix.

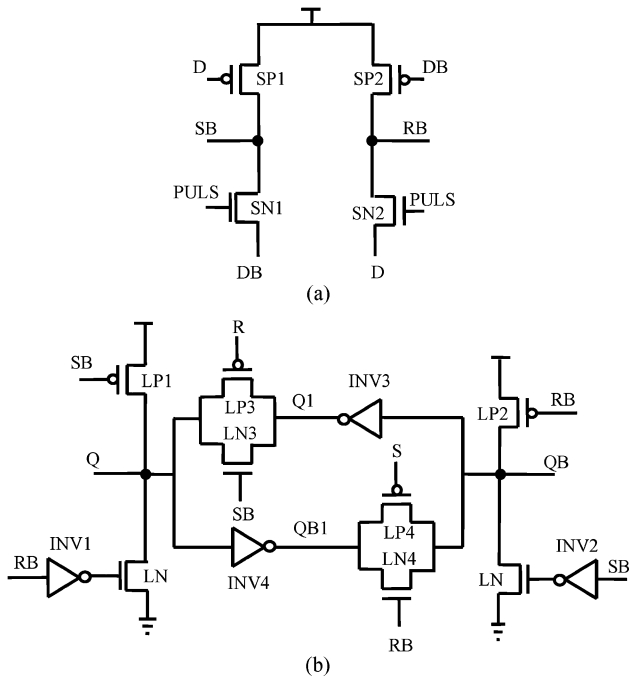


Fig. 6. Proposed clock-gated sense-amplifier flip-flop: (a) sensing stage, and (b) latching stage.

IV. SIMULATION METHODOLOGY AND PERFORMANCE COMPARISONS

To evaluate the performance of the proposed flip-flops, comparisons had been performed with other dual edge-triggered designs, including SCDF [8], DSPFF [9], and ACSAFF [10]. All the flip-flops were designed using Chartered Semiconductor Limited’s 0.18- μm CMOS process technology, at an operating temperature of 27 $^{\circ}\text{C}$ and a supply voltage of 1.8 V, using Cadence SPECTRE. The designs were optimized for a clock frequency of 0.8 GHz. A load capacitance of 100 fF was used for all outputs. All the measurements were taken over a 16-cycle data sequence of alternating 1’s and 0’s. The performances of all the flip-flops were measured based on their post-layouts results with all parasitic extracted and backannotated in the circuit simulation environment.

Fig. 7 presents the comparison results on power dissipation at different input switching activities. The proposed DET-SAFF has the minimum power consumption when the switching activity is greater than 0.5. At maximum input switching activity, DET-SAFF offers 20.3%, 23.2%, 33.5%, and 26% power reductions as compared to SCDF [8], DSPFF [9], ACSAFF [10], and the proposed CG-SAFF. ACSAFF and CG-SAFF consume more power at high input switching activities due to the addition of the control circuits in the pulse generating paths. However, CGSAFF exhibits its superiority in power saving when the input switching activity is less than 0.5. With an input switching activity of 0.25, the power consumption of CG-SAFF is 20.8%, 27.6%, 7%, and 7.6% less than SCDF, DSPFF, ACSAFF, and the proposed DET-SAFF, respectively. The highest reduction of power consumption is achieved when D is idle. And in this case, the power saving is more than 75% as compared to all other reported flip-flops.

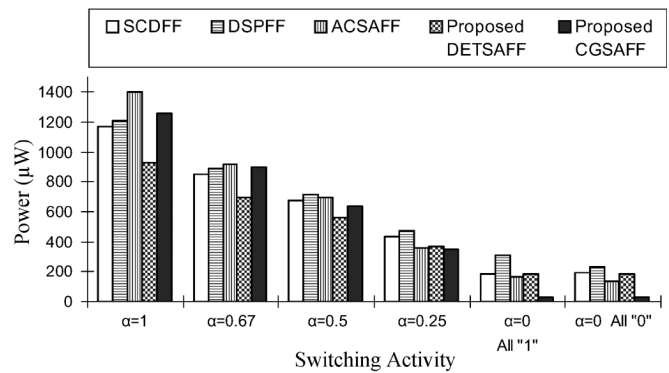


Fig. 7. Power consumption versus data switching activities.

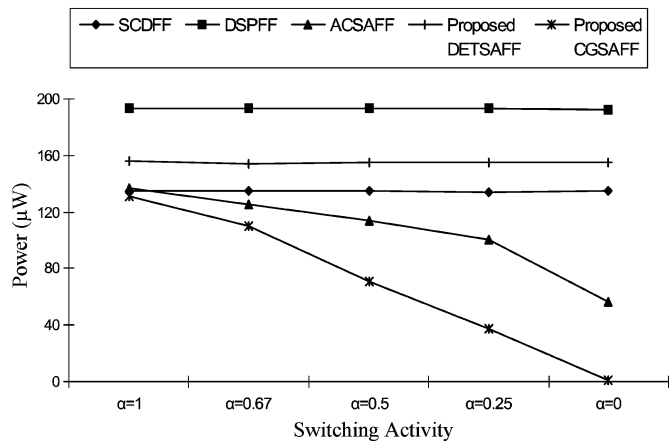


Fig. 8. Power consumption of pulse generator versus data switching activities.

To further explore the effect of clock gating, the power consumptions of the pulse generator at different switching activities are measured and the results are shown in Fig. 8. For SCDF, DSPFF and the proposed DET-SAFF, the power dissipation of the pulse generator are unchanged for all input switching activities. This is because the switching activity of the clock signal is always 1 regardless of the input patterns.

For CG-SAFF and ACSAFF, the pulse generator is conditionally controlled and the power dissipation decreases with the input data switching activity.

The power consumption of CG-SAFF is reported as a linear function of input switching activity as all the redundant transitions are eliminated. ACSAFF, on the other hand, does not exhibit this linear property. This is because the signal CLK1 will be generated regardless of the input switching activity. Therefore, CG-SAFF is more power efficient.

Table I summarizes the performance metrics of the reviewed flip-flops and proposed designs, at input switching activity of $\alpha = 1$. The proposed DET-SAFF and CG-SAFF have the smallest CLK-to-Q delay among the simulated flip-flops. DETSAFF achieves 23% to 43.3% reduction in delay. For CG-SAFF, this improvement is 11.6% to 26.3%, respectively. The relationship of CLK-to-Q delay with respect to the D-CLK delay is presented in Fig. 9, which describes the operation regions of the simulated flip-flops. In the meta-stable region, the CLK-to-Q delay of DET-SAFF increases slower with respect to the decrease of the D-to-CLK delay. This indicates

TABLE I
PERFORMANCE COMPARISON OF FLIP-FLOPS

Designs	SCDFF [8]	DSPFF [9]	ACSAFF [10]	DET-SAFF	CG-SAFF
CLK-to-Q delay (ps)	172.4	206.9	176.4	117.2	152.4
Min D-to-Q delay (ps)	169.4	157.8	421.1	93.42	307
Setup time (ps)	-98	-128	180	-70	90
Hold time (ps)	357	252	222	258	199
MOCF* (GHz)	1	1.43	0.83	1	1.25
# of transistors	29	24	39	22	40
Total width (μm)	55.64	66.82	114.46	55.59	96.52
Layout Area (μm^2)	199.5	189.9	261.7	157.85	267.6

*MOCF: Maximum Operating Clock Frequency is the highest clock frequency at which the outputs are able to maintain 90% of the output full swing at maximum data activity.

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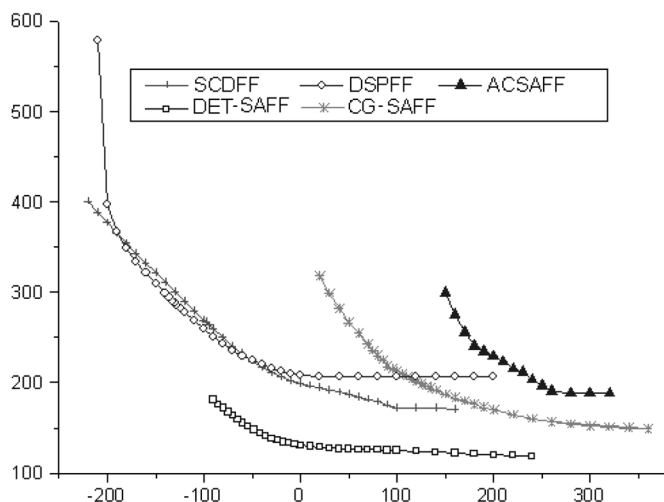


Fig. 9. CLK-to-Q delay as a function of D-to-CLK delay.

that the proposed DET-SAFF provides more design flexibility and robustness against large uncertainties of clock signal. For CG-SAFF, its CLK-to-Q delay is extended mainly due to the implementation of clock gating technique.

The setup time can be referred in Fig. 10, which shows the relationship of the average D-to-Q delay with respect to the D-to-CLK delay. Due to the pulse-triggered structure, DET-SAFF has a negative setup time of -70 ps. This provides the soft clock edge property, to allow time borrowing between adjacent pipeline stages. Moreover, the D-to-Q curve of DET-SAFF is relatively flat around the optimal setup time point, which provides certain level of absorption for clock uncertainty. The setup time of CGSAFF is positive. This is caused by the circuit structure, i.e., the input D should propagate through the comparator and gating logic before the triggering edge of the clock, so as

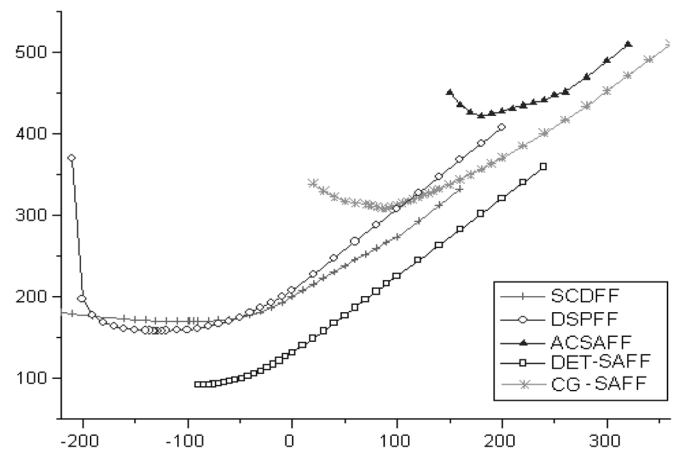


Fig. 10. D-to-Q delay as a function of D-to-CLK delay.

TABLE II
NUMERICAL RESULTS OF PDP AT $\alpha = 0.667$ AND $\alpha = 0.25$

Designs	SCDFF [8]	DSPFF [9]	ACSAFF [10]	DET-SAFF	CG-SAFF
PDP (fJ) @ $\alpha=0.667$	147.1	185	162.8	81.5	136.6
PDP (fJ) @ $\alpha=0.25$	74.8	98.3	63.8	43.7	52.4

to decide the passage of the clock signal. The setup time can be reduced by making use of the monotonic differential inputs.

For our analysis on hold times, SCDFF, DSPFF and the proposed DET-SAFF are noted to have larger hold time values. A traded off between the setup time and hold time is inevitable and the consequence of widening the transparent window has resulted in a more negative setup time as well as an increase in the hold time.

Both DET-SAFF and CG-SAFF are robust at high frequency operation. With regards to the area occupation, the layout of DET-SAFF consumes 16.9% and 20.9% less silicon area than SCDFF and DSPFF, respectively, while CG-SAFF occupies the most silicon area.

The power-delay-product (PDP) is calculated to evaluate the tradeoff between the power and CLK-to-Q delay. As shown in Table II, the proposed flip-flops have the smallest PDP. DET-SAFF is able to attain a maximum PDP improvement of 55.6%.

V. PROPOSED DUAL EDGE-TRIGGERED SENSE-AMPLIFIER BASED FLIP-FLOP WITH IMPROVED COMMON-MODE REJECTION RATIO

In an attempt to improve the CMRR of the proposed DET-SAFF, which has been analyzed to be 1 (refer to Appendix), we modified the sensing stage of the proposed DET-SAFF. An additional pMOS transistor SP3 is added to the proposed design (see Fig. 11) and the circuit is renamed mDET-SAFF. In mDET-SAFF, transistors SN1 and SN2 are controlled by D and DB, respectively. The additional transistor SP3 is triggered by the clock pulse signal PLUS, thus reducing the load on the clock pulse from two transistors to one transistor and with improved

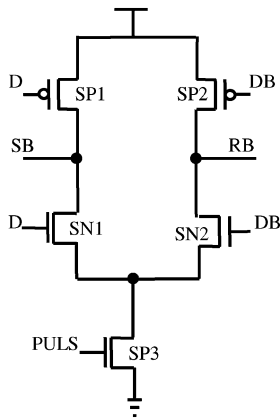


Fig. 11. Modified version of sensing stage of the proposed DET-SAFF.

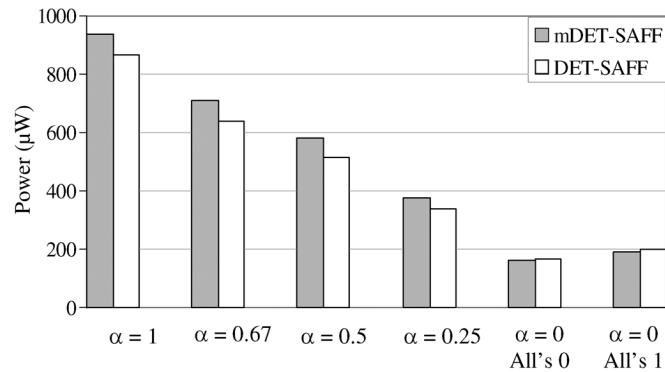


Fig. 12. Power consumption comparison between original and modified versions of the proposed DET-SAFFs at different input activities.

CMRR. The CMRR of mDET-SAFF is now the same as that of the conventional differential amplifier and is given as follows [12]:

$$CMRR_{mDET-SAFF} = \left| \frac{A_{dm}}{A_{cm}} \right| = 1 + 2(g_m + g_{mb})R_{Total} \quad (3)$$

where g_m and g_{mb} are the transconductance and body-effect transconductance of the common-source amplifier, respectively. R_{Total} is the total resistor of the tailed transistor (SP3). Fig. 12 presents the comparison results on power dissipation at different input switching activities between the proposed DET-SAFF and mDET-SAFF. With respect to PDP, the mDET-SAFF consumes 6.5% more PDP as compared to the proposed DET-SAFF. However, the modified version of the proposed DET-SAFF has a much improved CMRR than that of the proposed DET-SAFF.

VI. CONCLUSION

This paper presents two novel dual-edge triggered flip-flops for low power and high performance applications. DET-SAFF achieves substantial power reduction by incorporating dual-edge triggering and conditional precharging. It also minimizes latency by utilizing a fast latch. In addition, it has a negative setup time of 70 ps which provide useful attribute to time borrowing and clock uncertainty absorption. CGSAFF

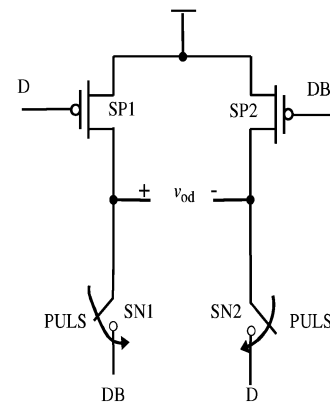


Fig. 13. Proposed SAFF's front-end sensing stage with differential input.

is superior in power saving at low switching activities. As compared to ACSAFF, which also has a power saving pulse generator, CG-SAFF outperforms in terms of power consumption (maximum of 75%), latency (27%), setup time (50%) and operation stability. Furthermore, a modified version of the DET-SAFF is introduced, which significantly improves the CMRR. Although this modified version consumes about 5% more power than the proposed DET-SAFF, both versions of the proposed DET-SAFFs have conclusively proved their robustness and suitability of applications when low power and high speed are of equal importance. But for low input switching activities, CG-SAFF is still preferred in the non-critical paths.

APPENDIX

A detailed analysis of CMRR for the proposed SAFF is given in this Appendix. The schematic diagram of its front-end sensing stage of Fig. 4(b) is redrawn (see Fig. 13) with the common-mode input voltages set to zero so we can consider the effect of differential-mode data input “D” and “DB” by itself. In the evaluation phase, as soon as D is low, SB will be set to high, and vice versa. During the transparency period, nMOS transistors SN1 and SN2 are considered as switches. When PULS is high, nodes SB and RB are shorted to DB and D, respectively. The small-signal characteristic is considered whereby the input signals D and DB transits from high-to-low or low-to-high.

Because the inputs are driven by equal and opposite voltages, when one side pulls up, the other side pulls down. Hence, the response to small-signal differential inputs can be determined by analyzing one side of the circuit. This simplified circuit, shown in Fig. 14(a) is called the differential-mode half circuit and its equivalent small-signal model is illustrated in Fig. 14(b). By inspection of Fig. 14(b), we recognize this circuit as the small-signal equivalent of a common-source amplifier. Therefore

$$v_{od} = -g_m \cdot r_0 \cdot v_{id} \quad (4)$$

$$A_{dm} = \left. \frac{v_{od}}{v_{id}} \right|_{v_{ic}=0} = -g_m \cdot r_0. \quad (5)$$

The circuit is now considered from a small-signal common-mode standpoint. Setting inputs $D = DB = v_{ic}$, the circuit is

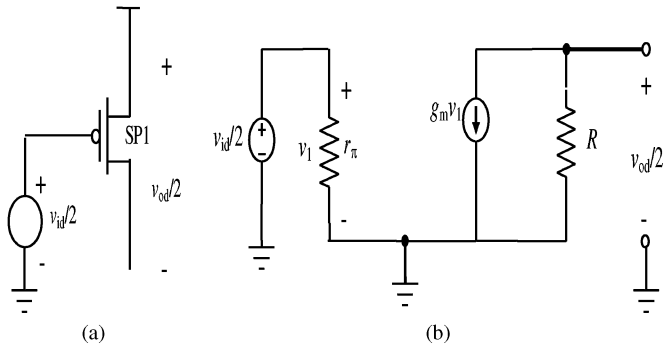


Fig. 14. (a) Differential-mode half circuit and (b) small-signal equivalent circuit.

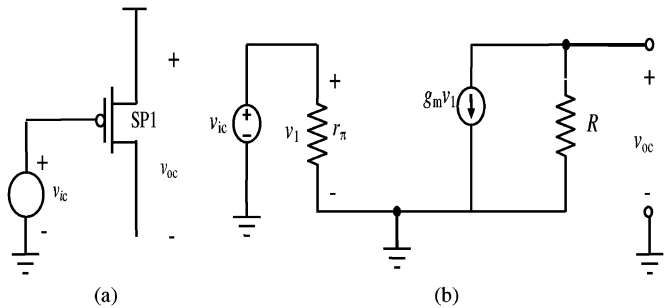


Fig. 15. (a) Common-mode half circuit and (b) small-signal equivalent circuit.

redrawn in Fig. 15(a) and its small-signal equivalent circuit is shown in Fig. 15(b).

Similarly, by inspection of Fig. 15(b), we recognize this circuit as the small-signal equivalent of a common-source amplifier. Therefore, the value of A_{cm} is same as that of A_{dm} and $CMRR_{Proposed}$ becomes unity.

We have also analyzed the power-supply rejection ratio (PSRR) of the proposed SAFF and its equivalent circuit of the front-end sensing stage with varying power supply voltages is shown in Fig. 16. The small-signal variation on positive power supply is v_{dd} . If $v_{ic} = 0$ is assumed during transparency period for simplicity, the resulting small-signal sensing stage output voltage is

$$v_0 = A_{dm}v_{id} + A^+v_{dd} \quad (6)$$

where A^+ is the small-signal gain from the positive power supply to the output. The (5) is then rewritten as

$$v_0 = A_{dm} \left(v_{id} + \frac{A^+}{A_{dm}} v_{dd} \right) \quad (7)$$

$$= A_{dm} \left(v_{id} + \frac{v_{dd}}{PSRR^+} \right) \quad (8)$$

where

$$PSRR^+ = \frac{A_{dm}}{A^+}.$$

The CMRR and PSRR for proposed SAFFs are also analyzed in this paper. The analyses provide good physical insights of the various parameters affecting the circuit design performce. This helps circuit designer to understand the operation of the

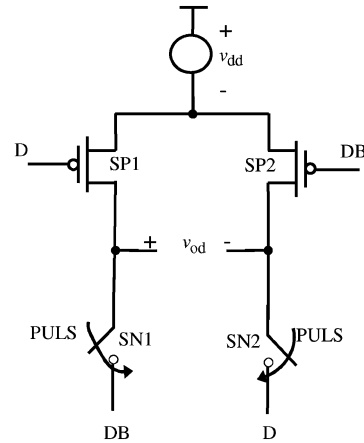


Fig. 16. Schematic of proposed SAFF sensing stage with supply variation model.

sense-amplifier based flip-flop circuits and makes further improvement on the circuit performance.

REFERENCES

- [1] H. Kawaguchi and T. Sakurai, "A reduced clock-swing flip-flop (RCSFF) for 63% power reduction," *IEEE J. Solid State Circuits*, vol. 33, no. 5, pp. 807–811, May 1998.
- [2] N. Nedovic, M. Aleksic, and V. G. Oklobdzija, "Conditional precharge techniques for power-efficient dual-edge clocking," in *Proc. 2002 Int. Symp. Low Power Electronics Design (ISPLED 2002)*, 2002, pp. 56–59.
- [3] C.-C. Yu, "Design of low-power double edge-triggered flip-flop circuit," in *Proc. 2nd IEEE Conf. Industrial Electronics Applications (ICIEA 2007)*, May 2007, pp. 2054–2057.
- [4] C. S. Kim, J. S. Kong, Y. S. Moon, and Y. H. Jun, "Presetting pulse-based flip-flop," in *Proc. IEEE Int. Symp. Circuits Systems (ISCAS 2008)*, May 2008, pp. 588–591.
- [5] P. Zhao *et al.*, "Low-power clock branch sharing double edge-triggered flip-flop," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 15, no. 3, pp. 338–345, Mar. 2007.
- [6] P. Zhao, T. K. Darwish, and M. A. Bayoumi, "High-performance and low-power conditional discharge flip-flop," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 12, no. 5, pp. 477–484, May 2004.
- [7] B. S. Kong, S. S. Kim, and Y. H. Jun, "Conditional-capture flip-flop for statistical power reduction," *IEEE J. Solid-State Circuits*, vol. 36, no. 8, pp. 1263–1271, Aug. 2001.
- [8] M. W. Phyu, W. L. Goh, and K. S. Yeo, "A low-power static dual edge-triggered flip-flop using an output-controlled discharge configuration," in *Proc. IEEE Int. Symp. Circuits Systems (ISCAS 2005)*, May 2005, vol. 3, pp. 2429–2432.
- [9] G. Aliakbar and M. Hamid, "Dual-edge triggered static pulsed flip-flops," in *Proc. 18th Int. Conf. VLSI Design 2005*, Jan. 2005, pp. 846–849.
- [10] Y. T. Liu, L. Y. Chiou, and S. J. Chang, "Energy-efficient adaptive clocking dual edge sense-amplifier flip-flop," in *Proc. IEEE Int. Symp. Circuits Systems (ISCAS 2006)*, May 2006, pp. 4329–4332.
- [11] B. Nikolic, V. G. Oklobdzija, V. Stajanovic, W. Jia, J. K. Chiu, and M. M. Leung, "Improved sense-amplifier based flip-flop: Design and measurements," *IEEE J. Solid-State Circuits*, vol. 35, no. 6, pp. 876–883, Jun. 2000.
- [12] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuit*. New York: Wiley, 2000.
- [13] J. I. Kim and B. S. Kong, "Dual edge-triggered flip-flop with modified NAND keeper for high-performance VLSI," *Current Appl. Phys.*, vol. 4, no. 1, pp. 49–53, Feb. 2004.
- [14] A. G. M. Strollo, D. De Caro, E. Napoli, and N. Petra, "A novel high-speed sense-amplifier-based flip-flop," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 11, pp. 1266–1274, Nov. 2005.
- [15] C. K. The, M. Hamada, T. Fujita, H. Hara, N. Ikumi, and Y. Oowaki, "Conditional data mapping flip-flops for low-power and high-performance systems," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 12, pp. 1379–1383, Dec. 2006.

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