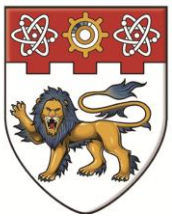

NANYANG TECHNOLOGICAL UNIVERSITY

LOW-POWER NON-BINARY SAR ADC WITH A TWO-MODE COMPARATOR

By

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ABSTRACT

For implantable medical devices like artificial pacemakers, high power efficiency is demanded because they are supposed to work 5 to 10 years on a battery. ADC is one of the major blocks as the interface between analog signals and digital logic. Hence, low power ADC with low speed and medium resolution is needed for such applications. These requirements make SAR ADC a suitable choice due to its simple structure and serial operation. However, there is still room for future power efficiency improvement.

To lower the power consumption, the method of applying a two-mode comparator was proposed, where the first few steps are completed in the comparator's low accuracy mode, and the last few steps are completed in the high accuracy mode. However, more errors are resulted in the first few steps, when the comparator is working with low accuracy. To resolve this problem, a generalized non-binary algorithm is applied. The capacitance values of the DAC array were adjusted to achieve better static performance.

In this project, an SAR ADC applying the generalized non-binary algorithm with a two-mode comparator is proposed. The capacitance values of the DAC array were adjusted to achieve better static performance, and hence the performance of the proposed ADC is improved. A non-binary ADC with the conventional structure is also constructed for performance comparison. Both ADCs were designed and simulated using GF 40nm technology. The simulation results show that with comparable static performance, the non-binary ADC with a two-mode comparator shows better power efficiency.

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Chapter 1

Introduction

1.1 Background

There is increasing demand in portable electronic biomedical devices in the past few years. These devices are important because they implement physiological signal recording for monitoring human or nonhuman subjects without restricting their mobility [1] [19] [20]. Generally, such devices are applied for detecting and monitoring biomedical signals such as pulse-oximetry, electrocardiographic (ECG), electroencephalography (EEG), and electromyography (EMG). Many of these devices are now integrated into personal area networks (PAN) for wireless health monitoring systems. The demand has given rise to an increasing popularity in the design of wireless sensing devices for implantable, portable and wearable applications.

The acquisition system is a crucial part in these devices, since it plays the role of converting analog signals into digital signals so that they can be better processed. In an acquisition system, Analog Front-End (AFE) is a power consuming and crucial building block because it determines the quality of the extracted signals. AFE consists of a pre-amplifier, a low pass filter, a programmable gain amplifier and an ADC, as shown in Fig. 1.1. Since many other artifact signals may be picked up by the recording electrodes, or the physiological electronics are too weak to detect, an amplifier and a low pass filter (LPF) are applied to reduce the common mode noise, amplify the signal and realize different low cutoff frequencies for different physiological signals. The signal is then transferred to ADC to be converted to

a digital signal. After that, the digital signal is passed to microprocessors. Low frequency, low noise and low power are three main design targets of AFE for implantable or portable physiological monitoring applications.

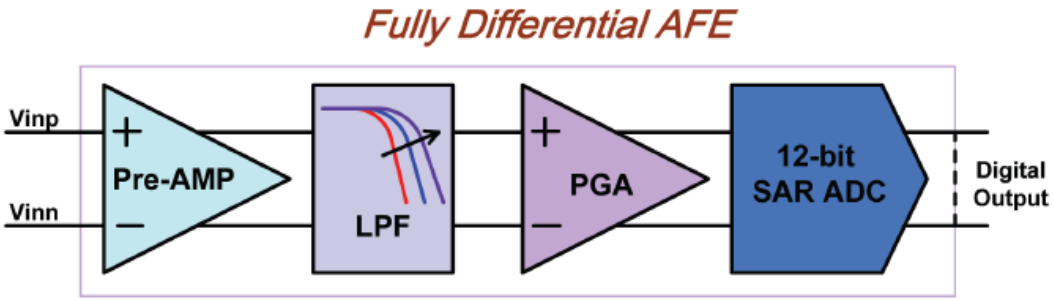


Fig. 1.1 Fully differential AFE architecture [25]

1.2 Motivation

High power efficiency and long battery life are primary goals for the implantable and portable devices. Particularly, ADC is a crucial part of the AFE because it provides the interface between the physical world and digital processing, and it needs a microwatt operation to run on a small battery for more than ten years. For ADC design, energy efficiency is the paramount design goal.

The requirements for the ADC performing the digitization are moderate resolution (8-12 bits) and low sampling rate (1-1000kS/s) [4] [21] [22]. SAR ADC is a suitable choice for biomedical applications due to its low power consumption and simplicity [4]. No static power is consumed if no pre-amplifier is used. The simple structure of SAR ADC's makes it suited for such requirements. Besides, it is also able to scale with technology because many of its blocks are digital.

In this thesis, a 10-bit, 307kS/s ([4] [21] [22]) SAR ADC is designed. In this SAR ADC, a two-mode

comparator is applied to improve power efficiency. To ensure high resolution, the generalized non-binary algorithm is applied. The SAR ADC is designed and simulated in the GF 40nm technology.

1.3 Thesis Outline

In this thesis, Chapter 2 introduces the fundamentals of ADCs, including some performance parameters of ADCs. In Chapter 3, the major blocks in an SAR ADC are discussed. In Chapter 4, a generalized non-binary algorithm with error correction ability is introduced and discussed. In Chapter 5, a two-mode comparator is proposed and in Chapter 6, the design of DAC is presented and discussed. In Chapter 7, the design of SAR is discussed and in Chapter 8, an SAR ADC with the generalized non-binary algorithm and the two-mode comparator is presented and simulated in the GF 40nm technology. Further research to be done is introduced in Chapter 9.

Chapter 2

ADC's Performance Metrics

In Chapter 2, some ADC metrics frequently mentioned in the thesis are briefly introduced and discussed.

2.1 Quantization Error

In Fig. 2.1 shows the quantization error of an ideal 3-bit ADC. The X-axis shows the analog input, V_{IN}, and the Y-axis shows the digital output code. Since the analog input is an infinite valued quantity and the output is a discrete value, an error will be produced as a result of the quantization. This error, known as quantization error, Q_e, is defined as the difference between the actual analog input and the value of the output (staircase) given in voltage [27]. It is calculated as

$$Q_e = v_{in} - V_{staircase}. \qquad (2.1)$$

The value of the staircase output, $V_{staircase}$, can be calculated as shown in Table 2.1.

Table 2.1 V_{OUT} values corresponding to digital codes

Digital Word	V_{OUT}
000	0
001	1/8
010	2/8
011	3/8
100	4/8
101	5/8
110	6/8
111	7/8

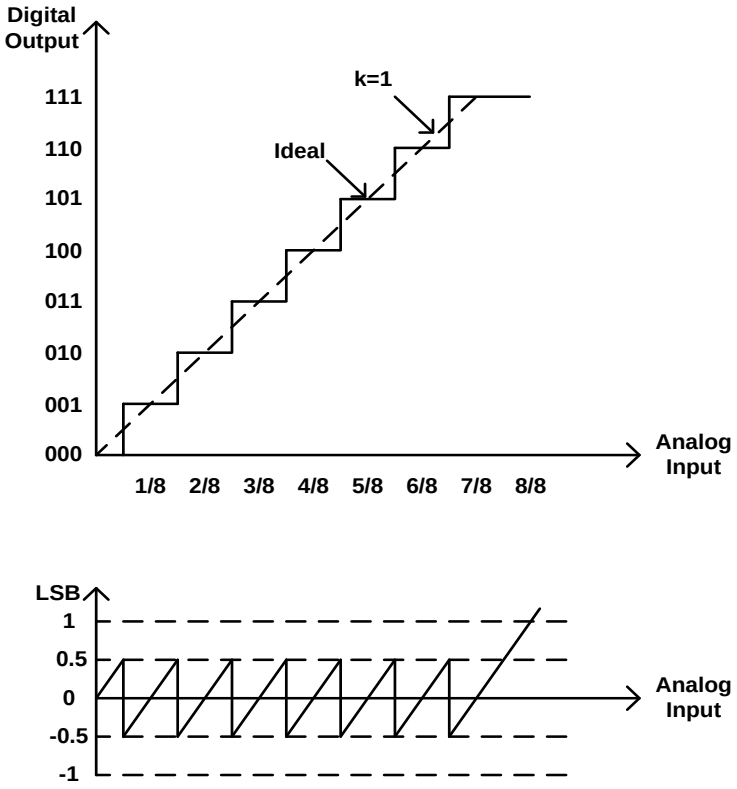


Fig. 2.1 Illustrations of quantization error of a 3-bit ADC

It should be noted that quantization error cannot be avoided, and it exists even in an ideal ADC.

2.2 Static Performance

In this section, some metrics to evaluate the static performance of the ADC are introduced.

2.2.1 Differential Nonlinearity (DNL)

For an ideal transfer curve, step size of each digital code is equal to 1LSB. In other words, in an ADC, the transition values are precisely 1LSB apart. Differential nonlinearity is defined as the variation in analog step sizes away from 1LSB [28]. The DNL of a 3-bit ADC is calculated as shown in Fig. 2. The dashed line is the transfer curve of an ideal 3-bit ADC. The solid line is the transfer curve of a non-ideal ADC with DNL errors. The staircases of the ideal transfer curve have the same width, 1LSB, for all digital output codes. However, the staircases of the non-ideal curve have different widths for different output codes. For example, for codes 010 and 100, the width are 2LSB and 0.5LSB, respectively. Therefore, for 010 and 100, the DNL are respectively:

$$DNL_{010} = 2 - 1 = 1LSB$$

$$DNL_{100} = 0.5 - 1 = -0.5LSB$$

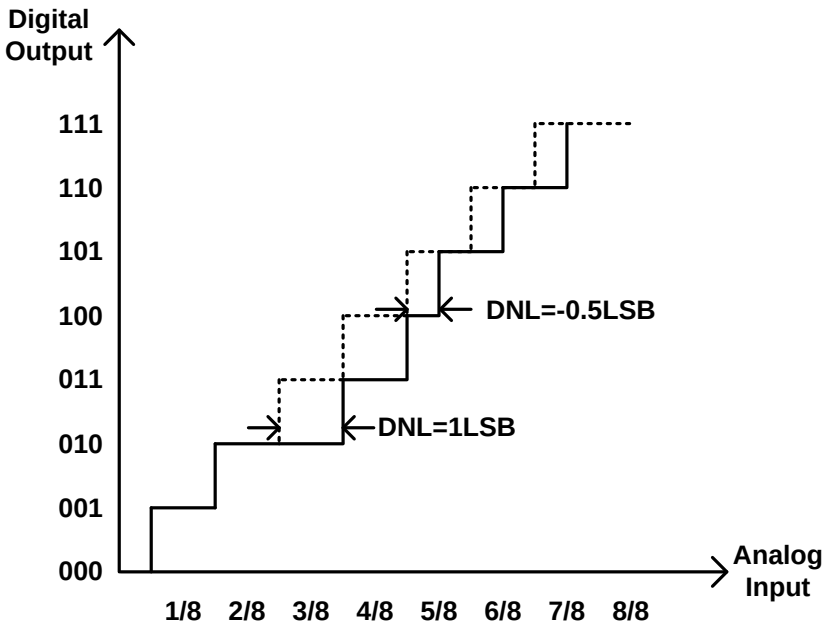


Fig. 2.2 Illustrations of DNL of a 3-bit ADC

2.2.2 Integral Nonlinearity (INL)

INL is defined to be the deviation from a straight line. Another important static parameter is the integral nonlinearity (INL). INL is the integral value of DNL. INL defines the difference between the transition point of a real conversion step and the ideal line [28], as shown in Fig. 2.3. The dashed line shows the transfer curve of an ideal 3-bit ADC, and the solid line shows the transfer curve of a non-ideal 3-bit ADC. A straight line connecting all the transition point of an ideal ADC is also shown in the figure. The INL of of code 011 is calculated as an example. For code 011, the distance between the actual transition point, A, and the ideal transition point, B, is 1LSB. So INL011=1LSB. The INL for code 100, 101, and 110 can be calculated in the same way.

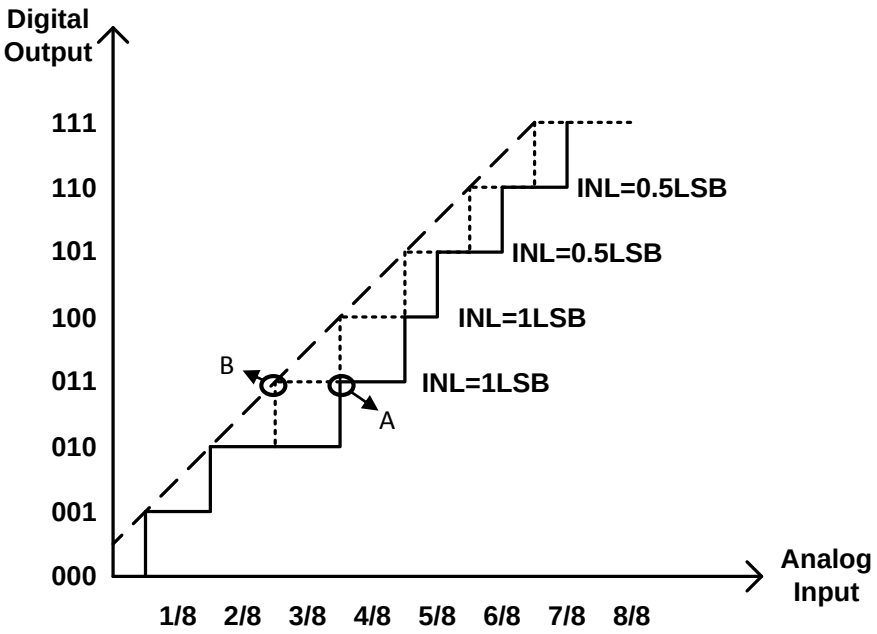


Fig. 2.3 Illustrations of INL of a 3-bit ADC

2.2.3 Offset

In an ideal ADC, the digital output should be 0 when the analog input is 0. However, if offset exists, the output is not 0 for a 0 input. Offset will shift the transfer curve with a certain value, as shown in Fig. 2.4.

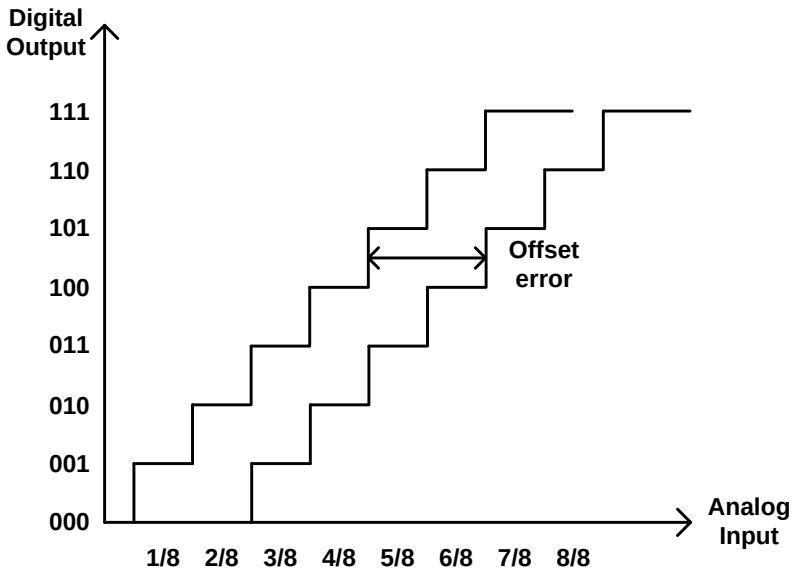


Fig. 2.4 Illustrations of offset of a 3-bit ADC

2.2.4 Gain Error

For an ADC, the equivalent gain error, GE, is given by

$$E_{gain(A/D)} = \left(\frac{V_{1...1}}{V_{LSB}} - \frac{V_{0...01}}{V_{LSB}} \right) - \left(2^N - 2 \right) \qquad (2.2)$$

The V_{OUT} values corresponding to each output code are shown in Table. 2.2. Graphical illustrations of gain error are shown in Fig. 2.5 [28].

Table 2.2 V_{OUT} values corresponding to each digital word

Digital Word	V_{OUT}
V_{000}	0
V_{001}	1/8
V_{010}	2/8
V_{011}	3/8
V_{100}	4/8
V_{101}	5/8
V_{110}	6/8
V_{111}	7/8

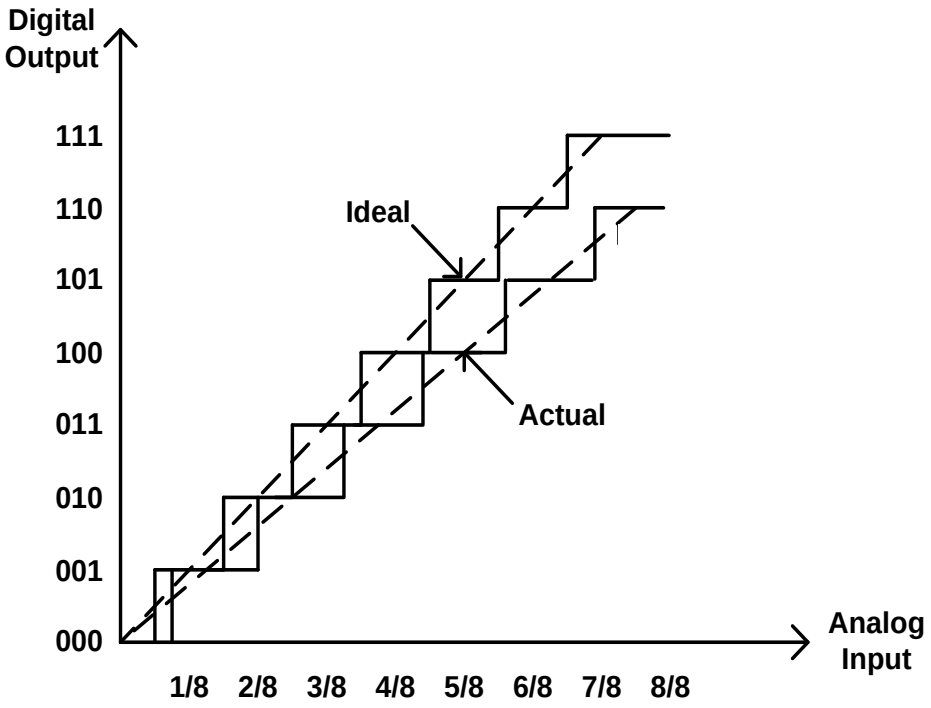


Fig. 2.5 Illustrations of gain error of a 3-bit ADC

2.3 Dynamic Performance

In this section, some ADC metrics to evaluate the dynamic performance of the ADC are introduced.

2.3.1 Signal to Noise Ratio (SNR)

SNR is defined as the ratio of the largest RMS input signal into the ADC to the RMS value of the noise. SNR is given in dB. Define the power of the input signal as P_S, and the power of the noise P_N. SNR is expressed as below.

$$SNR = 10\log_{10}\frac{P_S}{P_N} \qquad (2.3)$$

2.3.2 Signal to Noise and Distortion (SINAD)

SINAD is defined as the power of the input signal over the sum of the power of harmonics and noise at

the output. If the sample frequency is named f_s, then the noise bandwidth is $f_s/2$. Name the power of all harmonic components, P_D, which is expressed as below

$$P_D = V_2^2 + ... + V_N^2 \qquad (2.4)$$

SINAD can be expressed as:

$$SINAD = 20\log_{10}\frac{P_S}{P_N + P_D} \qquad (2.5)$$

2.3.3 Resolution & Effective Number of Bits (ENOB)

The resolution of the ADC is the number of bits at the output of the ADC. For an ideal ADC with resolution N, the smallest detectable voltage difference is $V_{LSB}=V_{REF}/2^N$. However, in real ADCs, due to different error sources, the output number of bits is smaller than N. ENOB is introduced as the resolution of an ideal ADC that would have the same resolution as the system under consideration. ENOB is a good indication of the dynamic performance of the ADC.

ENOB is normally calculated using SNR.

$$ENOB = \frac{(SNR - 1.76)dB}{6.02dB} \qquad (2.6)$$

However, since SINAD includes all distortion components (excluding the DC component) and noise, SINAD is commonly used instead of SNR to get a more precise ENOB.

$$ENOB = \frac{(SINAD - 1.76)dB}{6.02dB} \qquad (2.7)$$

2.4 Summary

In this chapter, some important metrics of ADC are introduced. These metrics include the quantization

error, and the metrics to describe ADC’s dynamic and static performances.

Chapter 3

Brief Introduction of Successive Approximation Register ADC (SAR ADC)

In this chapter, the operation of the successive approximation algorithm is first discussed, followed by a brief introduction of the major building blocks in an SAR ADC.

3.1 Successive Approximation Algorithm

For an N-bit resolution SAR ADC, there are N comparison cycles. The conversion algorithm is explained with a 3-bit SAR ADC in this section. The three output digital bits are named as D2, D1, and D0. The input voltage and reference voltage are named V_{IN} and V_{REF} respectively. The reference voltage of the 3 comparison cycles are *V (1)*, *V (2)*, and *V (3)*. The digitized output value is D_{OUT}. The operation of the successive approximation algorithm is explained with an example as shown in Fig. 3.1. In this case, $V_{IN}=7V_{REF}/16$. At first, the input voltage V_{IN} is sampled. In the first comparison cycle, *V (1)* is set to $V_{REF}/2$. The input voltage is compared with the reference voltage. If V_{IN} is larger than *V(1)*, the first bit D2, also known as MSB, is set to 1. However, if V_{IN} is smaller than *V(1)*, the first bit D2 is set to 0. In this case, $V_{IN}=7V_{REF}/16$ is smaller than *V(1)*$=V_{REF}/2$, thus D2 is set to 0. The reference voltage of the second comparison cycle *V(2)* is determined by D2. If D2=1, *V(2)* is set to *V(1)*$+V_{REF}/4=3V_{REF}/4$. If D2=0, *V(2)* is set to *V(1)*$-V_{REF}/4=V_{REF}/4$. In this case, D2=0, *V(2)* is set to $V_{REF}/4$. $V_{IN}=7V_{REF}/16$ is larger than *V(2)*$=V_{REF}/4$, thus D1 is set to 1. If D1= 1, *V(3)* is set to *V(2)*$+V_{REF}/8$. If D1=0, *V(3)* is set to *V(2)*$-V_{REF}/8$. In this case, D1=1, thus *V(3)* is set to $3V_{REF}/8$. $V_{IN}=7V_{REF}/16$ is larger than

V(3)=$3V_{REF}/8$, thus D0 is set to 1. After the three cycles, the three bit digital output is D2 D1 D0=011, which makes $D_{OUT}= 3V_{REF}/8$.

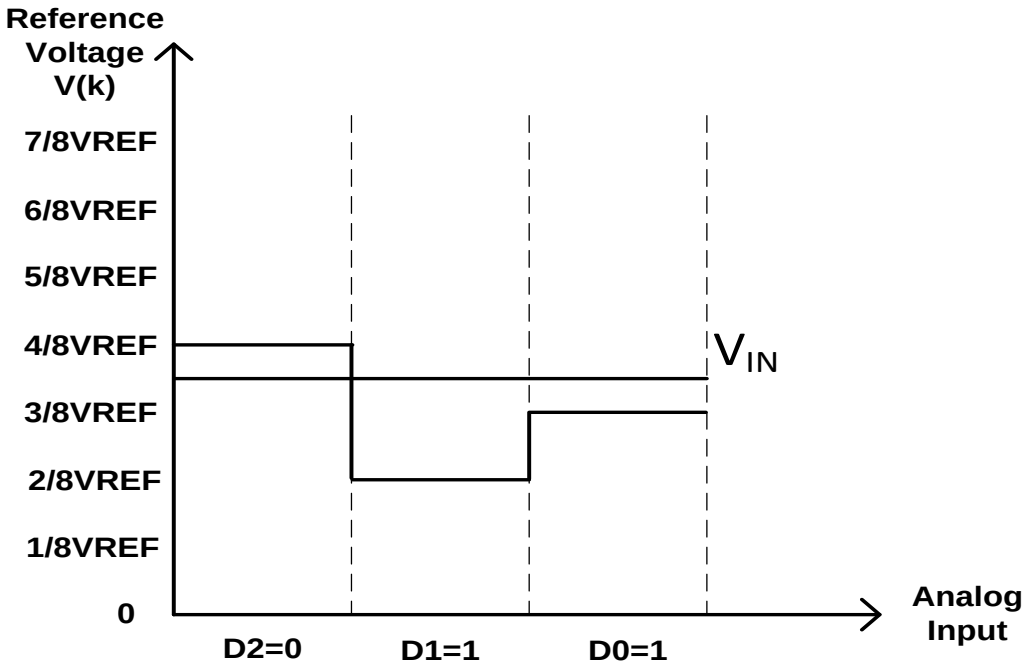


Fig. 3.1 Operation of the SA algorithm in a 3-bit ADC

3.2 Architecture of SAR ADC

The architecture of a conventional SAR ADC is illustrated in Fig. 3.2. A conventional SAR ADC consists of a sample and hold circuit, a DAC array, a comparator and a successive approximation register.

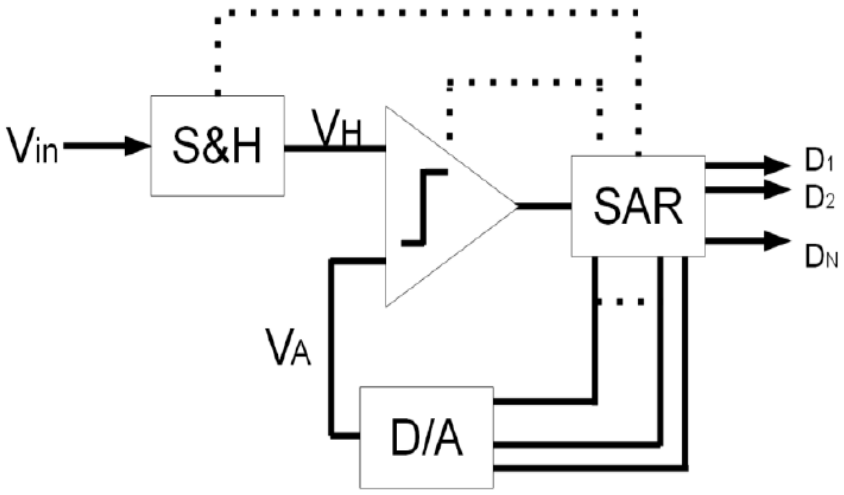


Fig. 3.2 Architecture of a conventional SAR ADC

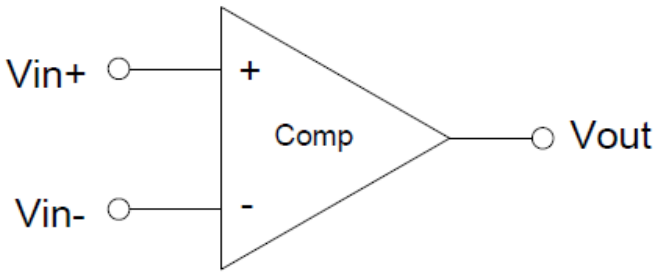
3.2.1 Sample and Hold (S&H)

The function of S&H circuit is to sample the input signal at the beginning of the whole conversion cycle and keeps the value for the rest of the cycle for comparison with the reference voltage. The S&H contains a switch and a capacitor. It has two working modes, namely the “sample” and “hold” mode. The two working modes are shifted by a control signal. When the switch is turned on, the input signal is stored by the capacitor. When the switch is turned off, the input signal is held by the capacitor. In an ideal sample and hold circuit, the output signal should be the same as the input signal and remains still in the hold mode. The sample and hold circuit has a great impact on the dynamic performance of the ADC.

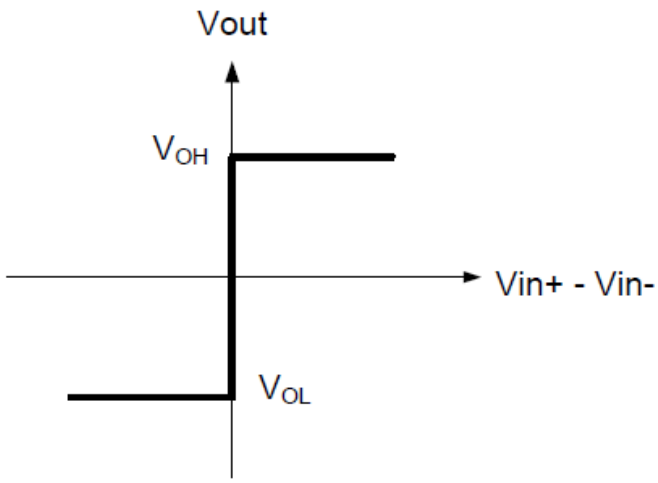
3.2.2 Comparator

Fig. 3.3 illustrates the comparator and the voltage transfer curve of an ideal comparator. An ideal comparator has infinite gain. A logic high output is produced when the input voltage is larger than the reference voltage, while a logic low output is produced when the input voltage is lower than the

reference voltage. The comparator is the only analog block in an SAR ADC. It performs comparisons between the sampled input signal and the reference voltage generated by DAC array. It generates “0” or “1”, which will be used by the SAR logic. Accuracy, offset and speed are important performance indicators for comparator. Accuracy determines the smallest difference a comparator can resolve. Offset shifts the transfer curve with a certain value. Comparator’s speed should be fast enough to complete the comparison and generate valid digital outputs during one comparison cycle. The design of the comparator will be further discussed in Chapter 5.



(a)



(b)

Fig. 3.3(a)Block diagram of a comparator. (b)Transfer curve of an ideal comparator

3.2.3 Successive Approximation Register

Successive approximation register logic, which will be referred as the SAR logic for the rest of the

thesis, is in fact a state machine. The SAR contains N registers for an N-bit ADC. In the first step, MSB is set to 1 and other bits are reset to 0. The digital word is converted to an analog value through the DAC array. The analog signal at the output of DAC array is presented at the input of the comparator and is compared with the sampled input signal. The MSB value is determined by the output of the comparator. If the sampled input is larger than the analog output of DAC array, the MSB remains at "1". Otherwise, the MSB remains at "0". The rest N-1 bits are determined in the same manner. In the (N+1)-th cycle, the N bits are stored. Therefore, an N-bit conversion is completed in N+1 cycles. The design of the SAR logic will be discussed in Chapter 7.

3.2.4 Digital to Analog Capacitor Array

The DAC array converts the digital word of the SAR logic into an analog value. The analog value is compared with the input signal by the comparator. There are two types of DAC arrays, namely charge sharing DAC arrays and charge redistribution DAC arrays. A DAC array with inherent sample and hold circuit is called charge redistribution DAC, because the sampling operation is conducted by the DAC array. The design of a charge redistribution DAC will be discussed in Chapter 6.

3.3 Summary

In this chapter, the successive approximation algorithm of SAR ADC is presented, and the major building blocks of the SAR ADC are also presented.

Chapter 4

Review of Non-Binary Algorithms and an SAR ADC with a Two-Mode Comparator

In this project, the author proposes to employ a two-mode comparator to an SAR ADC using the generalized non-binary algorithm. In this chapter, the conventional binary algorithm is first reviewed, followed by the introduction of the generalized non-binary algorithm. A different algorithm that uses a two-mode comparator for an SAR ADC is reviewed in the last section of this chapter.

4.1 Review of Binary Searching Algorithm

The conventional binary algorithm is reviewed in this section. Using a binary searching algorithm, N steps are needed for an N-bit SAR ADC. Assume that the analog input voltage is normalized from 0 to 2^N-1. The input voltage is V_{IN}, and the reference voltage of the *k*-th step is *V (k)*, the output of the comparator in the *k*-th step *d(k)*, and the digitized ADC output value D_{OUT}.

The reference voltage of the first step *V(1)* is given as:

$$V(1)=2^{N-1} \qquad (4.1)$$

The comparator compares V_{IN} and *V(k)* in the *k*-th step, and its output *d(k)* is defined by:

$$d(k)=1 \quad (\text{when } V_{IN} > V(k)) \qquad (4.2)$$

$$d(k)=0 \quad (\text{when } V_{IN} < V(k)) \qquad (4.3)$$

However, if *d(k)*=1 when $V_{IN} < V(k)$, or *d(k)*=0 when $V_{IN} > V(k)$, there is a decision error in the *k*-th

step. If the comparator's output of the *(k-1)*-th step *d(k-1)=1*, the reference voltage of the next step *V(k)* is given by

$$V(k)=V(k-1)+2^{N-k} \qquad (4.4)$$

If the comparator's output of the *(k-1)* -the step *d(k-1)=0*, then the reference voltage of the next step *V(k)* is given by

$$V(k)=V(k-1)-2^{N-k} \qquad (4.5)$$

Thus, *V(k)* can be given as

$$V(k)=2^{N-1}+\sum_{i=2}^{k}\left(\left(2d\left(k-1\right)-1\right)2^{N-i}\right) \qquad (4.6)$$

The N-bit output digital word is

$$d(1)d(2)\ldots d(N)$$

Then, the digitized ADC output value D_{OUT} is given as

$$D_{OUT}=d(1)2^{N-1}+d(2)2^{N-2}+\ldots+d(N)2^{0} \qquad (4.7)$$

For an N-bit SAR ADC applying the binary algorithm, there are 2^N patterns for the N-bit output digital word. These 2^N patterns are mapped to 2^N digitized values, which forms a one-to-one mapping. If one decision error occurs, a different digital word will be obtained. A wrong digitized output is resulted.

4.2 Review of the First Non-Binary Searching Algorithm

The non-binary searching algorithm was first proposed in [2]. In the algorithm, there are M steps for a N-bit SAR ADC (M > N). In this algorithm, $\gamma=2^{N/M}$ is named radix of the capacitance values. Assume that the digital output of the *k*-th comparison cycle is *d(k)*. The reference voltage in the *k*-th step *V(k)* is given as

$$V(k)=2^{N-1}+\sum_{i=2}^{k}\left(\left(2d\left(k-1\right)-1\right)\gamma^{M-i}\right) \qquad (4.8)$$

The digitized output value D_{OUT} is given as

$$D_{OUT} = 2^{N-1} + \sum_{i=2}^{k} \left(\left(2d\left(k-1\right) - 1 \right) \gamma^{M-i} \right) + d\left(k-1\right) - 1 \qquad (4.9)$$

Non-binary algorithm was first applied to a 14-bit 50kS/s SAR ADC [6]. The approach was applied in [7] [8] [9] [10] [11]. In the non-binary algorithm, M steps are required for an N-bit (M > N) resolution ADC. In the binary algorithm, the radix of 2 is applied. However, in the non-biary algorithm, the radix of $2^{N/M}$ is applied. It means that unlike a binary algorithm, the value for addition or subtraction to get the reference voltage of the next step is not an integer. Therefore, in actual non-binary ADCs, the capacitors in a DAC array are not integer-ratioed. As a result, the capacitor matching of the DAC array is poorer, compared with their integer ratioed counterparts in conventional structures.

The advantage of non-binary algorithm over the binary algorithm is that by including redundancy, the algorithm provides tolerance for decision errors ($d(k)$=1 when $V_{IN} < V(k)$, or $d(k)$=0 when $V_{IN} > V(k)$). In this algorithm, a decision mistake made in the previous steps can be corrected in later steps. The reason why the algorithm has error tolerance is explained in section 4.3.

4.3 Review of Generalized Non-Binary Searching Algorithm

As mentioned in section 4.3, in the prior non-binary searching algorithm, the radix of $2^{N/M}$ is applied, which makes the capacitors in the DAC array suffer more from capacitor mismatches. To solve the problem, a generalized non-binary algorithm was proposed [3]. Using the algorithm, the capacitor values are integer-ratioed, but they are not restricted to $2^{N/M}$, thus relieving the capacitor mismatches constraints. The generalized non-binary algorithm will be discussed in detail in the following part. The generalized non-binary algorithm will be referred as generalized NB algorithm for short.

In the generalized NB algorithm, M steps are performed for an N-bit (M > N) SAR ADC. The reference voltage of the *k*-th comparison cycle is *V(k)*, and the digital output of the *k*-th cycle is *d(k)*. *p(i)* is the value for addition or subtraction from the reference voltage.

$$V(k) = 2^{N-1} + \sum_{i=2}^{k}\left(\left(2d\left(k-1\right)-1\right)p\left(i\right)\right) \qquad (4.10)$$

The digitized ADC output D_{OUT} is

$$D_{OUT} = 2^{N-1} + \sum_{i=2}^{M}\left(\left(2d\left(k-1\right)-1\right)p\left(i\right)\right) + d\left(M\right) - 1 \qquad (4.11)$$

From equation (4.10) and (4.11), it can be found that when $p(i)=(2^{N/M})^{M-i}$, the generalized algorithm is the same as the conventional non-binary algorithm with a radix γ, in which $\gamma=2^{N/M}$. If N=M and $p(i)=2^{N-i}$, the generalized non-binary algorithm is the same as the binary algorithm.

p(i) must meet the following requirements

$$p\left(1\right) = 2^{N-1} \qquad (4.12)$$

$$\sum_{i=1}^{M} p\left(i\right) = 2^{N} - 1 + \left(over - range\right) \qquad (4.13)$$

The definition of over-range is explained with an example below. Fig. 4.1 shows the reference voltages of a 5-bit 6-step SAR ADC applying the generalized non-binary algorithm. In this ADC, *p(1)*=16, *p(2)*=7, *p(3)*=5, *p(4)*=3, *p(5)*=2, *p(6)*=1. For a conventional 5-bit SAR ADC, the generalized output range is from 0 to 31. However, the output range of the ADC shown in Fig. 4.1 is from -3 to 34. Here the range from -3 to -1 and the range from 32 to34 are called over-range (± 3LSB) and the over-range equals 3LSB.

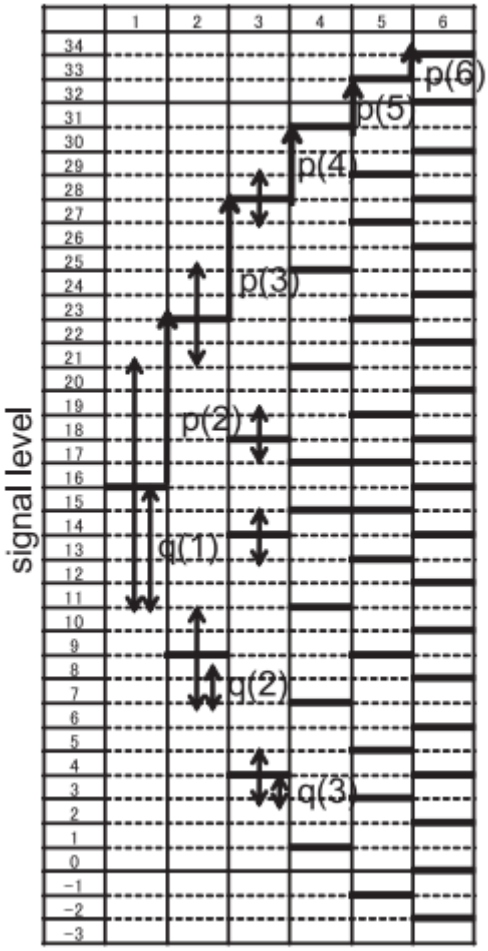


Fig. 4.1 Generalized NB algorithm of a 5-bit 6 steps SAR ADC

For a conventional N-bit resolution SAR ADC, N comparison steps are needed. There are 2^N digital patterns. These output patterns are mapped to 2^N analog output levels. The digital patterns and the analog levels form a one-to-one mapping. If a decision mistake is made, the digital pattern will not be the same, and a wrong analog output will be resulted. The mistake cannot be recovered. For a generalized non-binary algorithm, there are 2^M digital patterns. These 2^M patterns are mapped to 2^N analog output levels. The digital patterns and the analog levels form a multiple-to-one mapping. This means that two or more different digital patterns are mapped to the same analog output level.

To further discuss the generalized NB algorithm, *q(k)* is introduced as "the redundancy of the *k*-th

comparison step". *q(k)* indicates the overlap between output ranges of one comparison pattern and the next pattern for the *k*-th step. *q(k)* decides the error correction ability of the *k*-th step. As long as the difference between input voltage V_{IN} and the reference voltage of the *k*-th step *V(k)* is smaller than *q(k)*, the decision mistake in this step can be corrected in later steps. The relationship can be expressed as

$$\left|V_{in}-V(k)\right|<q(k) \tag{4.14}$$

However, *q(k)* must meet the following requirements

$$2^{M}-2^{N}=\left(\sum_{i=1}^{M-1}2^{i}q(i)\right)+2\bullet over-range \tag{4.15}$$

After the values of *q(k)* is set, we can infer the *p(k)* values using the equation given below

$$q(k)=-p(k)+1+\sum_{i=k+2}^{M}p(i) \tag{4.16}$$

Fig. 4.2 shows the example of a conventional 5-bit SAR ADC. In this case, the generalized input is 22.5. If no error occurs in all the 5 steps, the output code is 0

10110

Which makes

D_{OUT}=22.

However, if an error occurs during the second step as shown in Fig. 4.2, the comparison result happens to be 1 instead of 0. The wrong output code is

11000

This error cannot be corrected, and

D_{OUT}=24

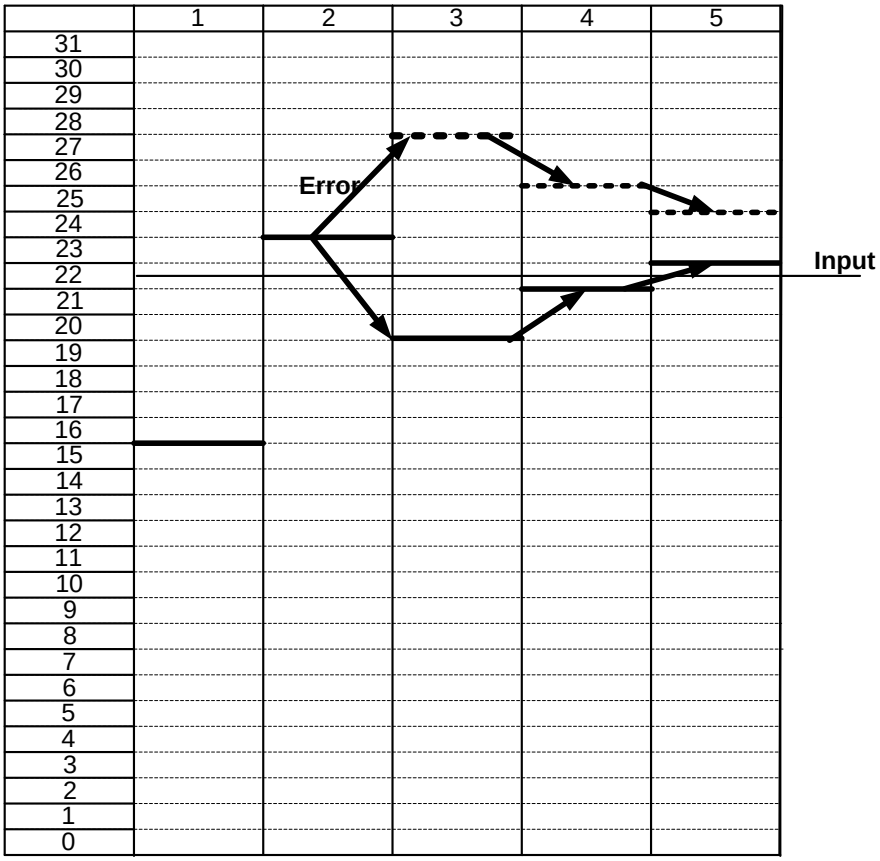


Fig. 4.2 Conversion of a 5-bit SAR ADC using the binary searching algorithm

Fig. 4.3 shows an example of a 5-bit 6-step SAR ADC using the generalized non-binary algorithm. $p(1)$=16, $p(2)$=7, $p(3)$=4, $p(4)$=2, $p(5)$=1, $p(6)$=1, $q(1)$=2, $q(2)$=1, $q(3)$=1, $q(4)$=1, $q(5)$=0, $q(6)$=0. If no error occurs, the output code is

101110

In this case, using equation 4.11, the final output is

$$D_{OUT}=22$$

If the same error mentioned above is assumed and an error occurs during the second step, the output code is

110000

The final output is

D_{OUT}=22

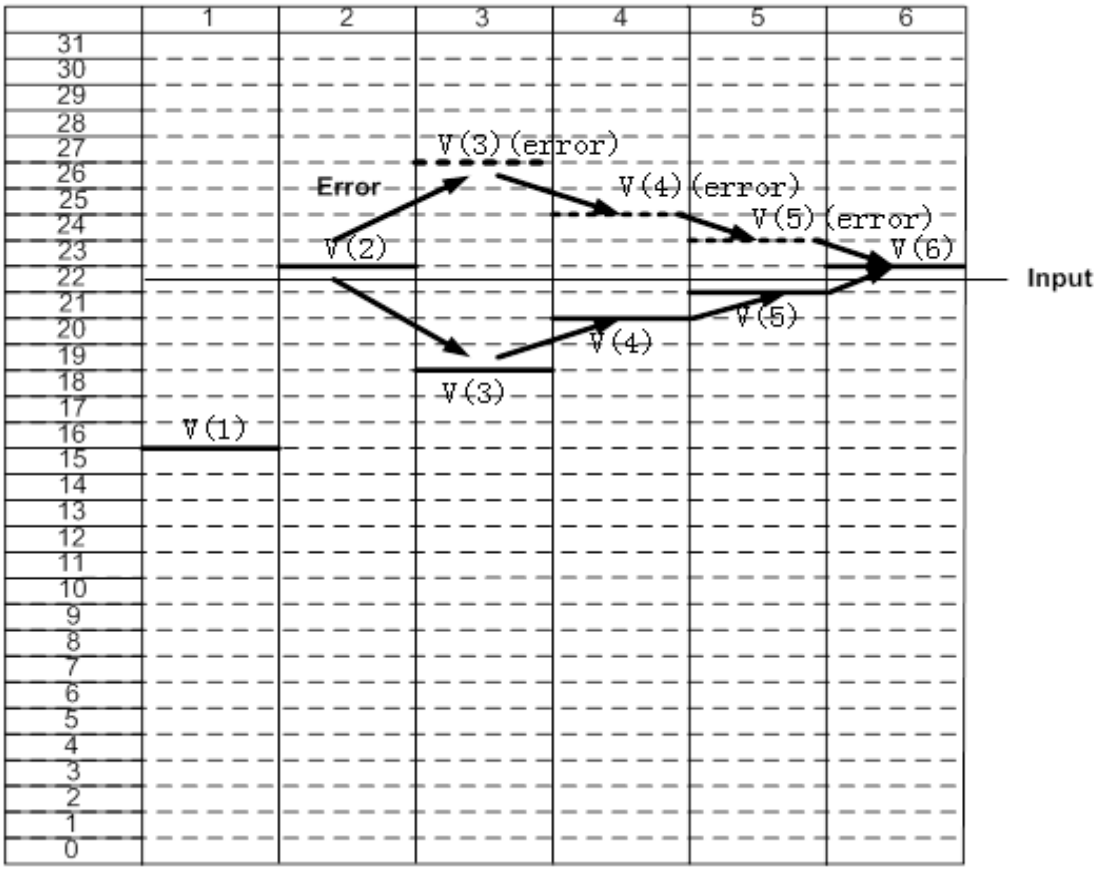


Fig. 4.3 Conversion of a 5-bit 6 step SAR ADC using the generalized NB algorithm

Even if there is a decision error, the correct output (D_{OUT}=22) is still obtained, independent on whether error exists in the second step. This is due to the error correction capability of the algorithm. In this case, the error occurs in the second step. *q(2)*=1. The reference voltage of the second step is *V(2)*=23 (as shown in Fig. 4.3). The difference between the input voltage and *V(2)* is

$$\left|V_{IN}-V(2)\right|=\left|23-22.5\right|=0.5<1$$

This satisfies equation (4.14). Therefore, the error made in the second cycle can be recovered and the correct output can be obtained.

4.4 Review of an SAR ADC with a Two-Mode Comparator

Fig. 4.4 shows the power consumption breakdown of the comparator, the SAR logic and the DAC array in a conventional SAR ADC [4].

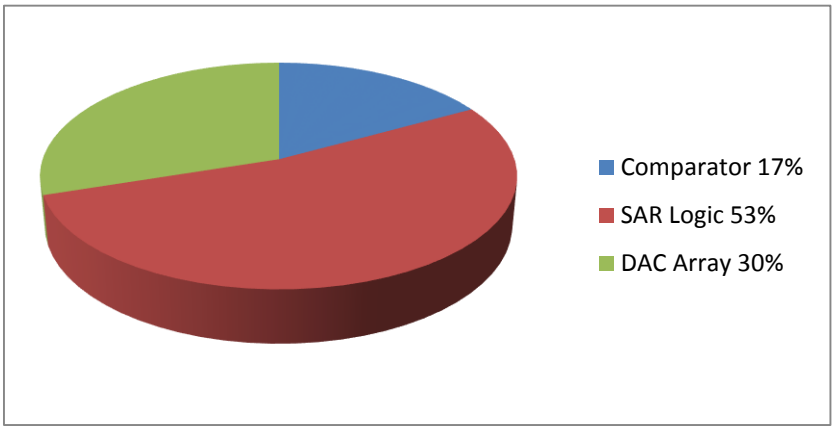


Fig. 4.4 The breakdown of power consumption of a conventional SAR ADC from [4]

It is true that the power consumed by the comparator contributes less than 20% of the whole ADC power consumption. However, in the design of implantable and portable biomedical devices, reducing power consumption of the entire device is the main goal. Effort should be spent to reduce power in all ADC blocks. Much effort has already been spent to reduce power in SAR and CDAC in the past few years [4] [5], pushing them towards the physical limits. But not enough effort has been spent on comparator, which is the third power hungry block in the device. The design goal in this thesis is to reduce the comparator's power without damaging the accuracy.

Normally, comparators with high accuracy have high power consumption. To achieve high accuracy, a comparator with high power is used. For high resolution SAR ADCs, comparators can be quite power consuming. Reducing the power consumption of comparator remains a challenging problem.

A method to reduce the power consumption in comparator was proposed by Harpe [12]. In his work, a

two-mode comparator is used. The comparator has different power and accuracy when working in the two modes. A similar idea was proposed by Giannini [13], but at the expense of two comparators. One comparator has low power and low accuracy, and the other has high power and high accuracy.

The schematic of the comparator in Harpe's design is shown as Fig. 4.5. This is a two-stage comparator. For the two-stage dynamic comparator, power consumption and input referred noise (IRN) are dominated by the first stage. Since the power of the first stage scales proportional to C_a, and the IRN scales with $1/C_a$. Thus varying C_a is enough to compromise the power and accuracy of the two modes. When S1 is turned off, C_a is not connected to the comparator. The comparator works at low power low accuracy mode. When S1 is turned on, C_a is loaded onto the comparator. The comparator works at high power high accuracy mode. To further reduce the power consumption, a two-step comparison scheme was proposed that makes use of the two-mode comparator. In the two-step scheme, the comparator works at low power low accuracy mode in the first few steps, and works at high power high accuracy mode for the last few steps. The comparator is more vulnerable to decision errors in the first few steps due to its low accuracy. To correct those errors, an error correction method was used.

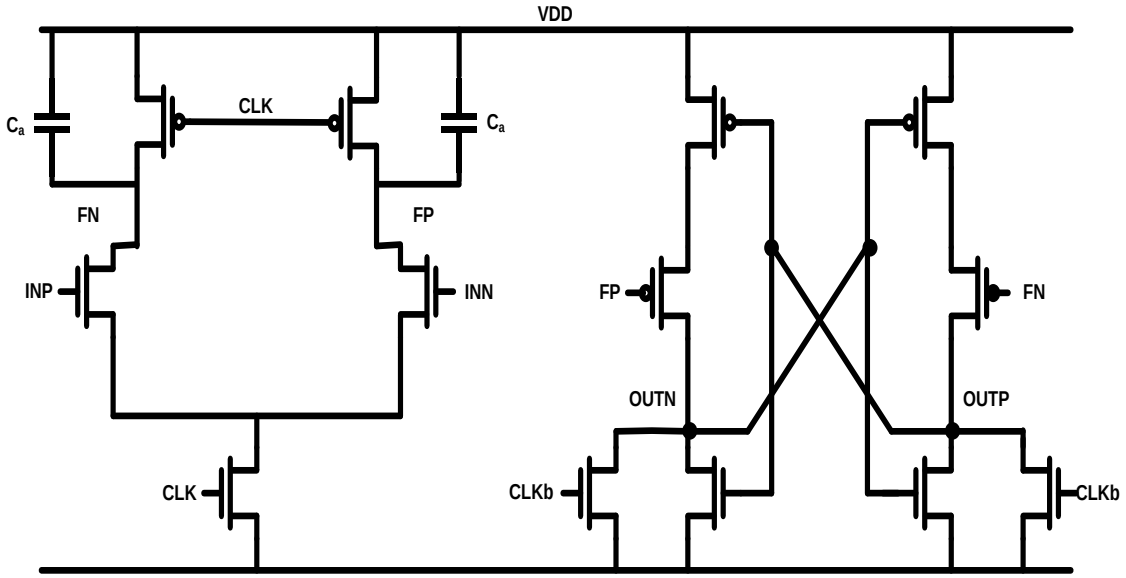


Fig. 4.5 Schematic of the two-mode comparator proposed in [12]

The details of the scheme are discussed below and will be explained with an example in the next paragraph. Among all the reference voltages during the whole conversion process, the reference voltages right above and below the input signal are named V_h and V_l, respectively. The difference between input signal, V_{in}, and the two reference voltages should be within 1LSB. If the comparison results are correct in these two comparisons, the correct digital output can be obtained. As comparator works in the low accuracy mode other than the last step, error may occur during one of the earlier comparisons. So to correct the error, a redundant comparison step is added at the end of the whole binary comparison process.

For a 5-bit SAR ADC, assume that the input voltage is 23.5, as shown in Fig. 4.6. If no mistake is made during the whole comparison process, the digital output is 10111. In this case, in the 5th comparison step, the reference voltage is 23 and the output is 1. If no error occurs in previous steps, V_{in} is between 23 and 24. To get the correct output, it should be ensured that $23<V_{in}<24$. Since comparison between intput signal and 23 is already made, an additional comparison between intput and 24 is needed. In this

case, a comparison between V_{in} and 24 is made in the additional step. The output of the additional step is 0. The digital output, including the additional bit is 101110. The last two comparison results, 1 and 0, indicate that $23<V_{in}<24$. The correct output is obtained, and the final ADC output is 23 (1x16+0x8+1x4+1x2+1x1=23, equation (4.7)). This is the case when no mistake is made. However, when a mistake is made, the conversion is shown in Fig. 4.6 where the dashed line shows the reference voltages. When a mistake is made in the second step, the output for this case is 11000. In the 5th comparison step, the reference voltage is 25 and the output is 0, which indicates $V_{in}<25$. To verify $24<V_{in}<25$, the last redundancy comparison is made between V_{in} and 24. However, in this comparison, the output is 0, which indicates $V_{in}<24$ and is contradicting to the proposed $24<V_{in}<25$. Therefore, correction is needed as according to Table 4.1. After the correction, the final output is 10111. So even if an error occurs in the previous steps, the correct ADC output can still be obtained.

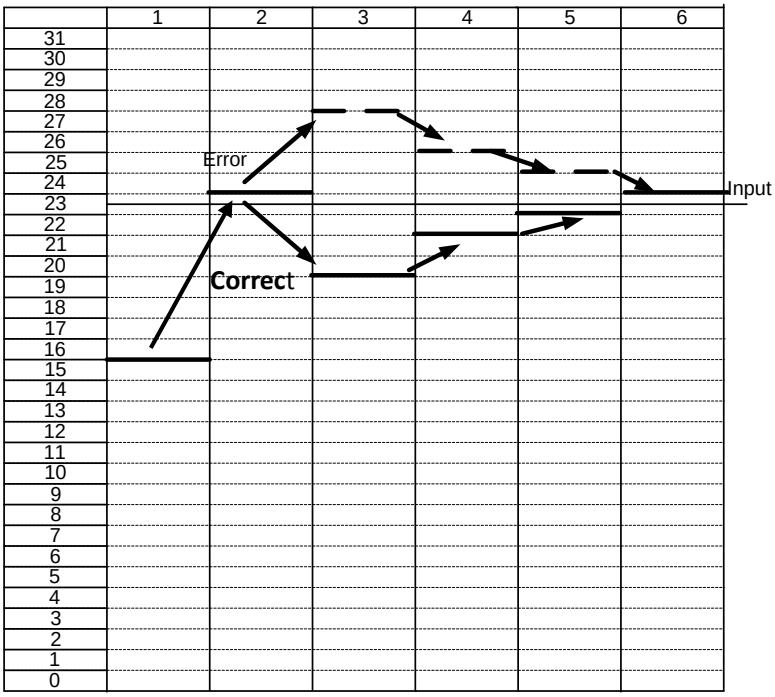


Fig. 4.6 Conversion of a 5-bit SAR ADC using the error correction method from [12] & [13]

Table 4.1 Correction algorithm proposed in [12] & [13]

Digital output of the *N*-th comparison cycle *d(N)*	Digital output of the *(N+1)*-th comparison cycle *d(N+1)*	Correction method to the digitized result
0	1	NA
1	0	NA
1	1	+1
0	0	-1

To ensure that the algorithm works, two requirements must be met.

1. The decision error occurs in the step whose reference voltage is quite close to input signal (difference between the reference voltage and the input signal within 1LSB).

2. The final reference voltage is either V_h or V_l.

These conditions work better for high resolution SAR ADCs. Take an example of a 4-bit SAR ADC as shown in Fig. 4.6. Assume that the V_{in}=13.2. If no mistake is made during all steps, the output code is 1101 and the digitized output is 13 (1x8+1x4+0x2+1x1=13, equation 4.7). If one mistake occurs in the second step, according to the error correction algorithm, the final output is 12, which is not correct. In this case, the error correction scheme does not take effect. The reason is that the error occurs when the difference between V_{in} and the reference voltage is larger than 1LSB. Besides, the reference voltage of the last step is neither V_h or V_l. Hence, to ensure that the method works, two requirements must be met.

1. The comparator must be properly sized to allow only one decision error, and it occurs only when the difference between V_{in} and reference voltage is smaller than 1LSB.
2. The resolution should be high enough to make sure that the reference voltage of the last step is either Vh or Vl.

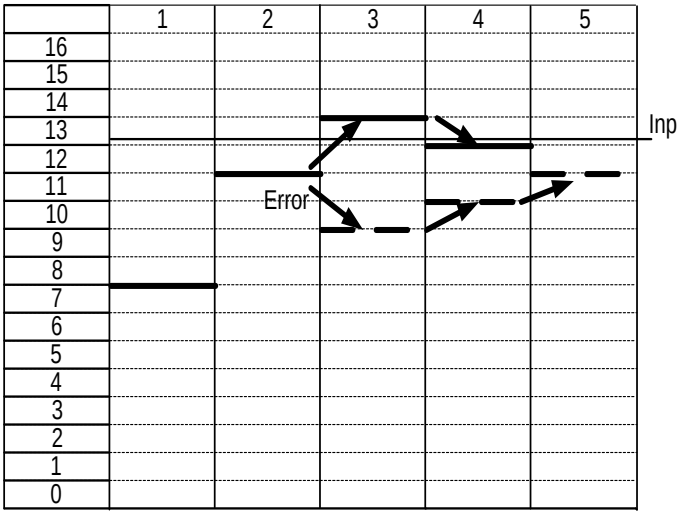


Fig. 4.7 Example of a 4-bit SAR ADC using the correction algorithm from [12] & [13]

To implement this scheme, complexity is introduced to the SAR logic and DAC array design. A signal is needed to switch the working modes of the comparator. An adder is needed to perform the correction shown in Table 4.1. However, since comparators are quite programmable for different resolution

requirements, the idea of using reconfigurable comparator has great potential.

4.5 Summary

In this chapter, the prior non-binary algorithm is introduced, followed by the generalized non-binary algorithm, which is applied in this project. A two-mode comparator is also reviewed.

Chapter 5

The Design of a Two-Mode Comparator

Some basic information about the comparator has been introduced in Chapter 3. The design of the comparator is critical because it dominates the overall power consumption (17%). In this section, a dynamic comparator with two working modes is designed. When working in one mode, the comparator has low accuracy and consumes low power. When working in the other mode, the comparator has high accuracy and consumes high power. Normally, for a conventional 10-bit SAR ADC, 10 steps are performed, each in the high accuracy level. High power consumption is resulted by such a method. In this project, using a 2-step conversion scheme (to be introduced in Chapter 7), 11 steps are performed to achieve 10-bit accuracy. The first 8 steps are performed in the low accuracy level and consume low power, while the last 3 steps are performed in the high accuracy level and consume high power. Power efficiency is improved by such a method. The design of the comparator is discussed and some simulation results are shown below.

5.1 Introduction of the Dynamic Comparator used in the Project

The schematic of the comparator in this project is shown in Fig. 4.5. The structure was first proposed in [14], and was made reconfigurable in [12]. The original structure without two working modes is shown in Fig. 5.1. This is a dynamic comparator, thus no static power is consumed. Besides, there is no power consumption when the comparator is not active. Its high power efficiency makes it a suitable choice for

this project.

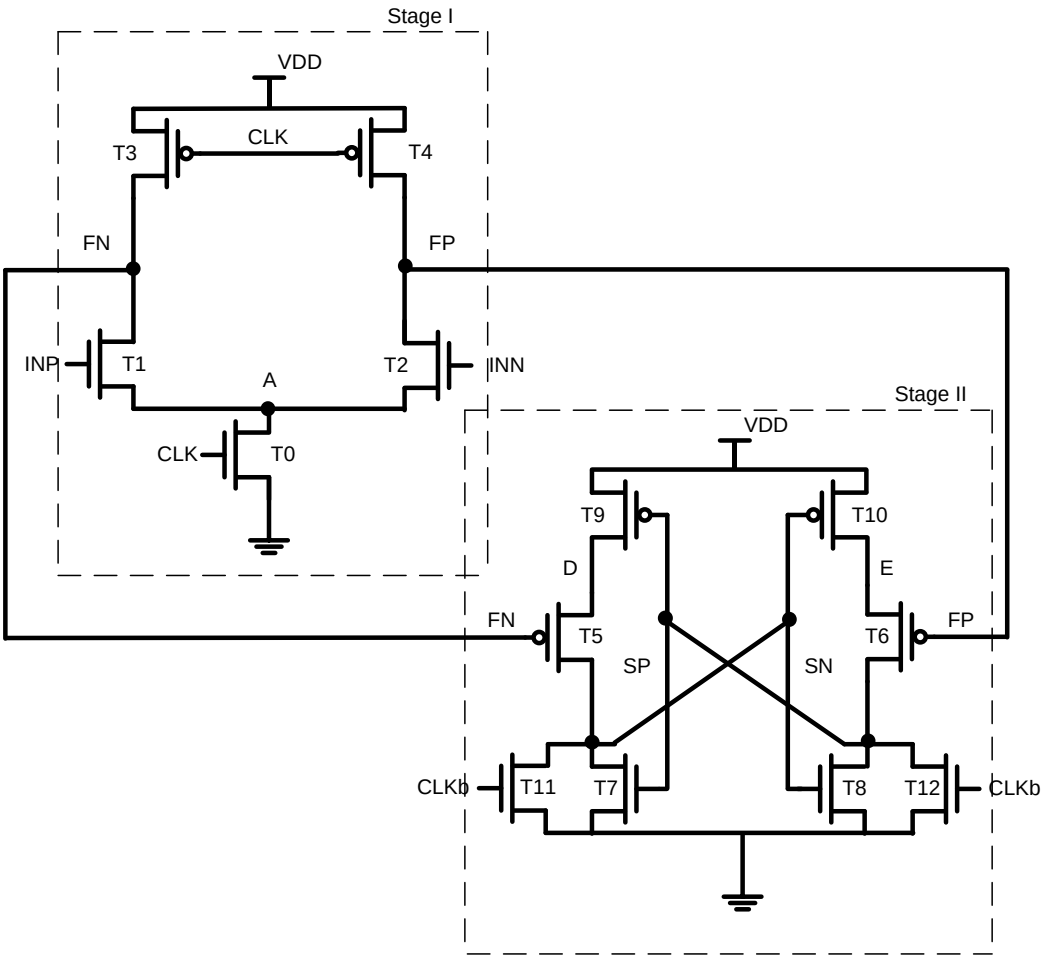
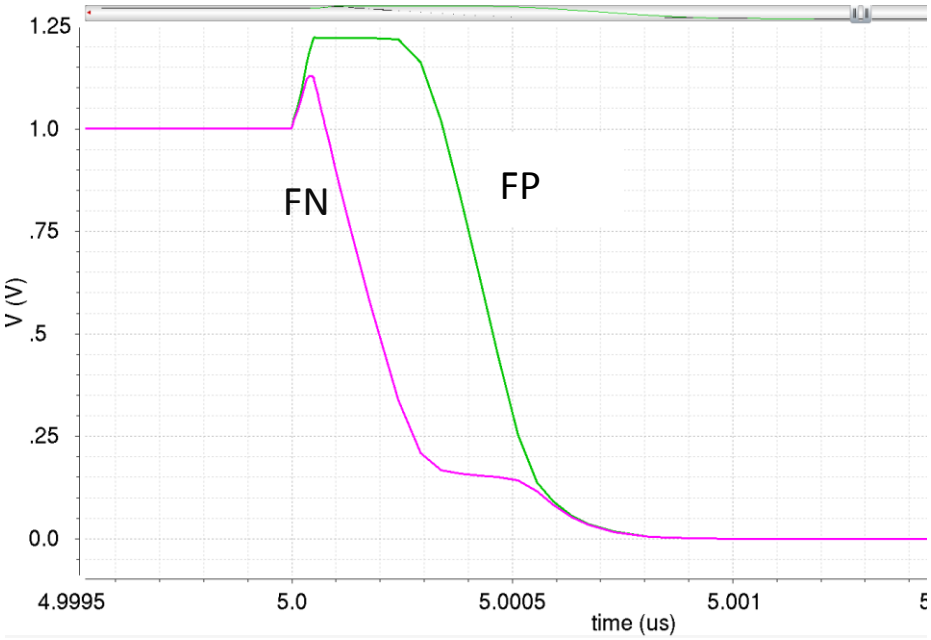


Fig. 5.1 Schematic of the original comparator proposed in [14]

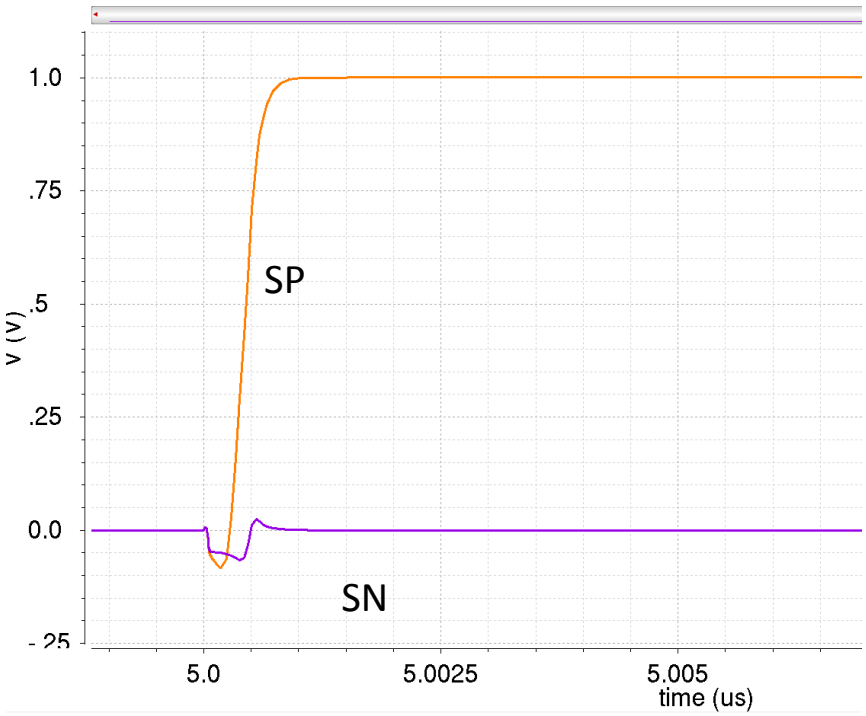
The comparator consists of two stages. The first stage consists of transistors T0, T1, T2, T3, and T4. The first stage is an amplification stage. It has INP and INN as differential inputs, and FN and FP as differential outputs. The second stage consists of T5~T12 and it is a latch. The second stage has inputs FP and FN, and provides rail-to-rail digital outputs SP and SN by the positive feedback.

The comparator has two phases, namely the “reset” phase and “evaluation” phase. When clock signal CKL is 0, the comparator works in the reset phase. Nodes FP, FN are precharged to 1, and SP, SN are reset to 0. When CLK is 1, the comparator works in the evaluation phase. The differential inputs are

INP and INN respectively. In this case, assume INP > INN. INP > INN makes the discharging current at node FN larger than that at node FP. Voltage at FN is decreasing faster than that at FP. When voltage at FN first reaches the threshold voltage of T5 V_{tp}, T5 is turned on, and pulls voltage at SP to1. When voltage at SP is increased to the threshold voltage of T6, denoted as V_{tn}, T6 is turned on and forces voltage at SN to go to 0. Transistor T7 is kept on by SN, and this makes voltage at SP stay at 1. The voltage at nodes FP, FN, SP, and SN during the conversion are shown as Fig. 5.2. The CMOS process for the simulations in this chapter is GF 40nm, and the corner is TT, 27°C.



(a)



(b)

Fig. 5.2 (a) Voltage at nodes FP and FN during evaluation phase. (b) Voltage at nodes SP and SN during evaluation phase

In the evaluation phase (CLK=1), the power consumption of the first stage stops when the parasitic capacitances at all the nodes of the stage are fully discharged. The power consumption of the second stage stops when full-scale outputs are obtained. In the reset phase (CLK=0), all parasitic capacitors are precharged to their original values. No power is consumed when the comparator is not activated (CLK=0).

5.2 Power Calculations of the Comparator

In the evaluation phase (CLK=1), the power consumption of the first stage stops when the parasitic capacitances at all the nodes of the stage are fully discharged. The power consumption of the second stage stops when full-scale outputs are obtained. In the reset phase (CLK=0), all parasitic capacitors are precharged to their original values. No power is consumed when the comparator is not activated

(CLK=0). The power is mainly consumed to charge the parasitic capacitance of the operating nodes A, FP, FN, B, C, SP and SN. The power is calculated and discussed in this section.

For a capacitor *C*, assume that the voltage difference over the two plates at time t_1 and t_2 are V_1 and V_2 respectively. The energy stored in capacitor C over time (t_2-t_1) is E. E is described as the equation shown below.

$$E = \frac{1}{2}CV_2^2 - \frac{1}{2}CV_1^2$$

As shown in Fig. 5.1, since FN and FP are the outputs for stage I and are the inputs for stage II, stage II can be regarded as the load for stage I. Power of stage I is consumed to drive the load, namely to charge the parasitic capacitance at nodes FP and FN for SP and SN to reach rail-to-rail outputs.

As shown in Fig. 5.1, the differential input voltages are INP and INN, respectively. In the following calculations, INP > INN is assumed. The parasitic capacitors are shown as in Fig. 5.3. The gate-source and gate-drain parasitic capacitors of PMOS are referred to as C_{p1} and C_{p2}. The gate-source and gate-drain parasitic capacitors of NMOS are referred to as C_{n1} and C_{n2}. The energy consumed by the parasitic capacitors over the evaluation period is determined by the voltage difference at the beginning and the end of the evaluation phase. The voltage at operation nodes A, FN, FP, SN, SP, B, and C are shown in Table 5.1.

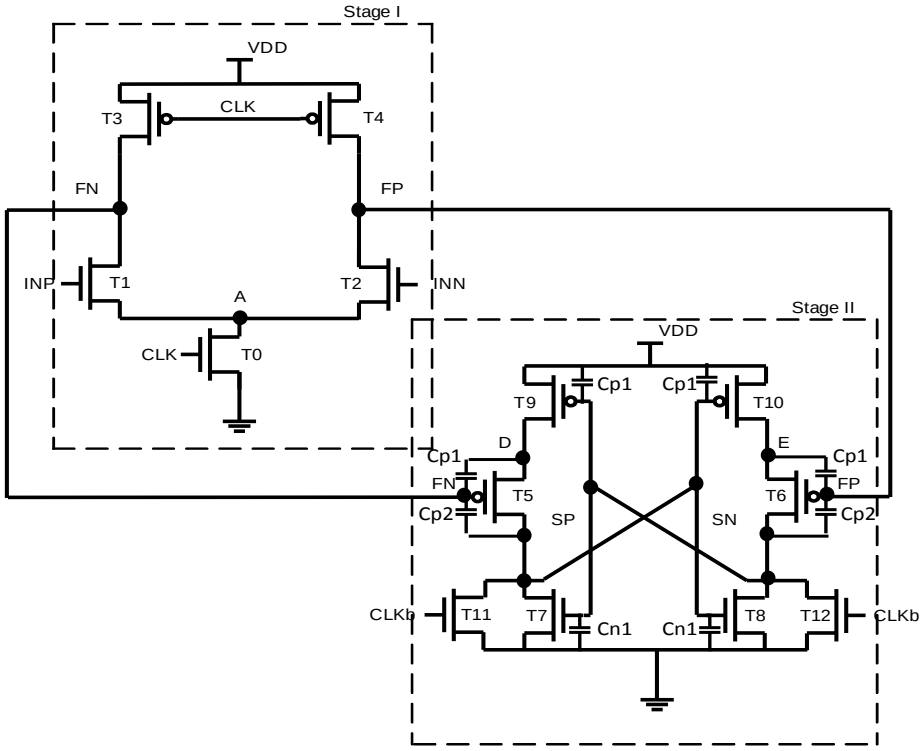


Fig. 5.3 Schematic of the comparator with parasitic capacitors

Table 5.1 Voltages at the beginning and the end of evaluation phase

Nodes	Voltage at the beginning of evaluation phase	Voltage at the end of evaluation phase
A	V_A	0
FP	V_{DD}	0
FN	V_{DD}	0
SP	0	V_{DD}
SN	0	0
D	V_{DD}	V_{DD}
E	V_{DD}	V_{DD}

The power consumption in stage II is consumed to charge parasitic capacitors of T5 and T6, and to

charge parasitic capacitors of T8 and T10. Since in this case, INP > INN has been assumed, SP is 1 and SN is 0 at the end of the evaluation phase. SN is not changed over the evaluation phase, so no power is consumed to charge the parasitic capacitors of T9 and T7. The voltage difference at the beginning and the end of evaluation phase is shown in Table 5.2. f_{cmp} is denoted as the frequency of comparator clock signal.

Table 5.2 Energy consumed by parasitic capacitors

	Voltage difference at beginning of evaluation phase	Voltage difference at end of evaluation phase	Energy consumption over evaluation phase	Power of the evaluation phase
C_{p1} (T5)	0	V_{DD}	$E_1 = \frac{1}{2} C_{p1} V_{DD}^2$	$P_1 = \frac{1}{2} C_{p1} V_{DD}^2 f_{cmp}$
C_{p2} (T5)	V_{DD}	V_{DD}	$E_2 = 0$	$P_2 = 0$
C_{p1} (T6)	0	V_{DD}	$E_3 = \frac{1}{2} C_{p1} V_{DD}^2$	$P_3 = \frac{1}{2} C_{p1} V_{DD}^2 f_{cmp}$
C_{p2} (T6)	V_{DD}	0	$E_4 = \frac{1}{2} C_{p2} V_{DD}^2$	$P_4 = \frac{1}{2} C_{p2} V_{DD}^2 f_{cmp}$
C_{p1} (T10)	V_{DD}	0	$E_5 = \frac{1}{2} C_{p1} V_{DD}^2$	$P_5 = \frac{1}{2} C_{p1} V_{DD}^2 f_{cmp}$
C_{n1} (T8)	0	V_{DD}	$E_6 = \frac{1}{2} C_{n1} V_{DD}^2$	$P_6 = \frac{1}{2} C_{n1} V_{DD}^2 f_{cmp}$
C_{p1} (T9)	V_{DD}	V_{DD}	$E_7 = 0$	$P_7 = 0$
C_{n1} (T7)	0	0	$E_8 = 0$	$P_8 = 0$

Name the power consumed by the parasitic capacitors of this original comparator as P_{PC}. Then

$$P_{PC} = P_1 + P_2 + P_3 + P_4 + P_5 + P_6 + P_7 + P_8$$

$$P_{PC} = \frac{1}{2} C_{p1} {V_{DD}}^2 f_{cmp} + \frac{1}{2} C_{p1} {V_{DD}}^2 f_{cmp} + \frac{1}{2} C_{p2} {V_{DD}}^2 f_{cmp} + \frac{1}{2} C_{p1} {V_{DD}}^2 f_{cmp} + \frac{1}{2} C_{n1} {V_{DD}}^2 f_{cmp}$$

The values of the parasitic capacitance are approximated as

$$C_{p1} = C_{p2} = 2C_{n1} = 2C_{n2}$$

After the approximation, power is expressed as

$$P_{PC} = \frac{1}{2} C_{p1} V_{DD}{}^2 f_{cmp} \times \left(4 + \frac{1}{2} \right)$$

In [26], the requirement for ADC cell for low speed low power biomedical applications is less than 1uW. According to the power breakdown in each block in [4], the power allocated to the comparator (17%) is about 170nW. If we can make the power consumed by comparator less than 60nW, the power efficiency can be improved by 60%.

$$P_{PC} \leq 60nW$$

f_{cmp}=4MHz. Therefore,

$$C_{p1} \leq 7\,fF$$

is required.

From simulation results, it is found that the parasitic capacitance of PMOS transistor (W/L)=(800/80)n is approximately 7fF.

The sizes of the comparator are shown as Fig. 5.4. The power consumption of the comparator is 52nW, according to simulation results.

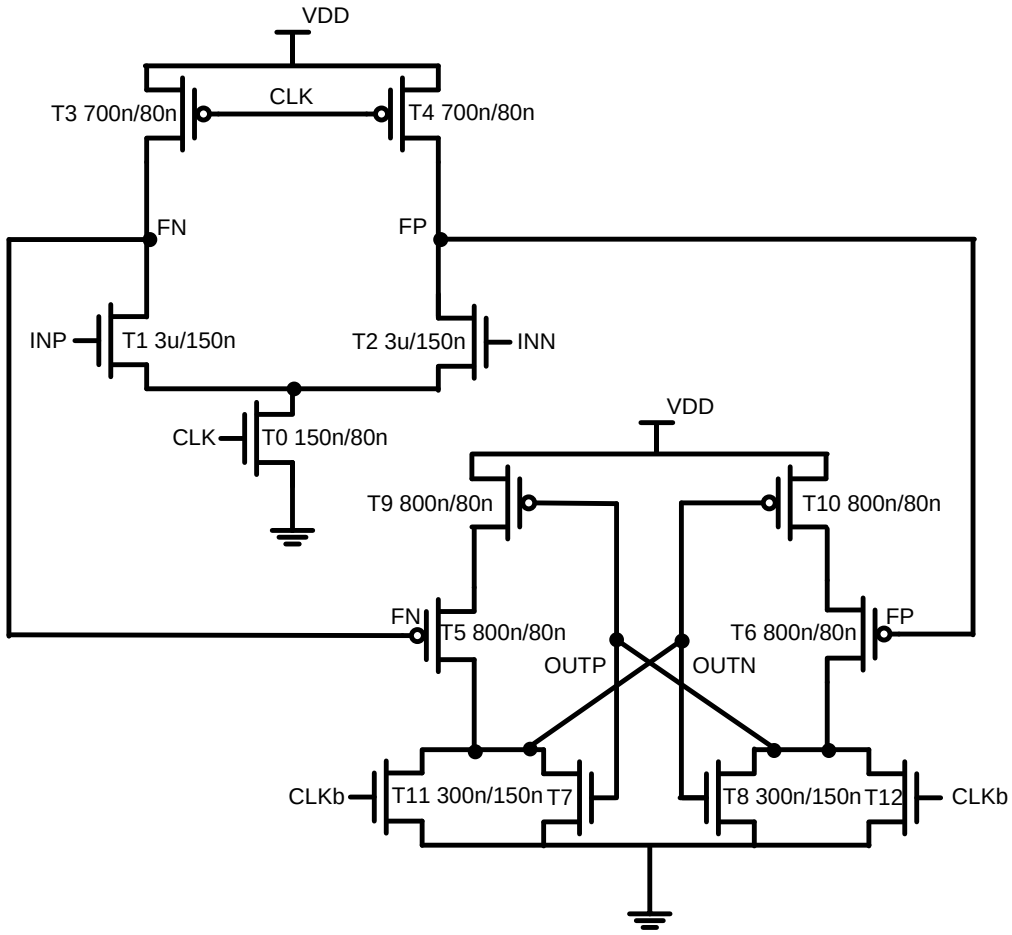


Fig. 5.4 Sizes of the transistors of the comparator

5.3 Noise Calculations of the Comparator

The discussions below are based on the comparator shown in Fig. 5.5, which is the same schematic as Fig. 5.1. Since the voltage amplification is performed in stage I, this stage is critical in deciding the overall noise and power efficiency of the comparator. The noise is dominantly contributed by the differential input pair. The thermal noise is calculated in this section.

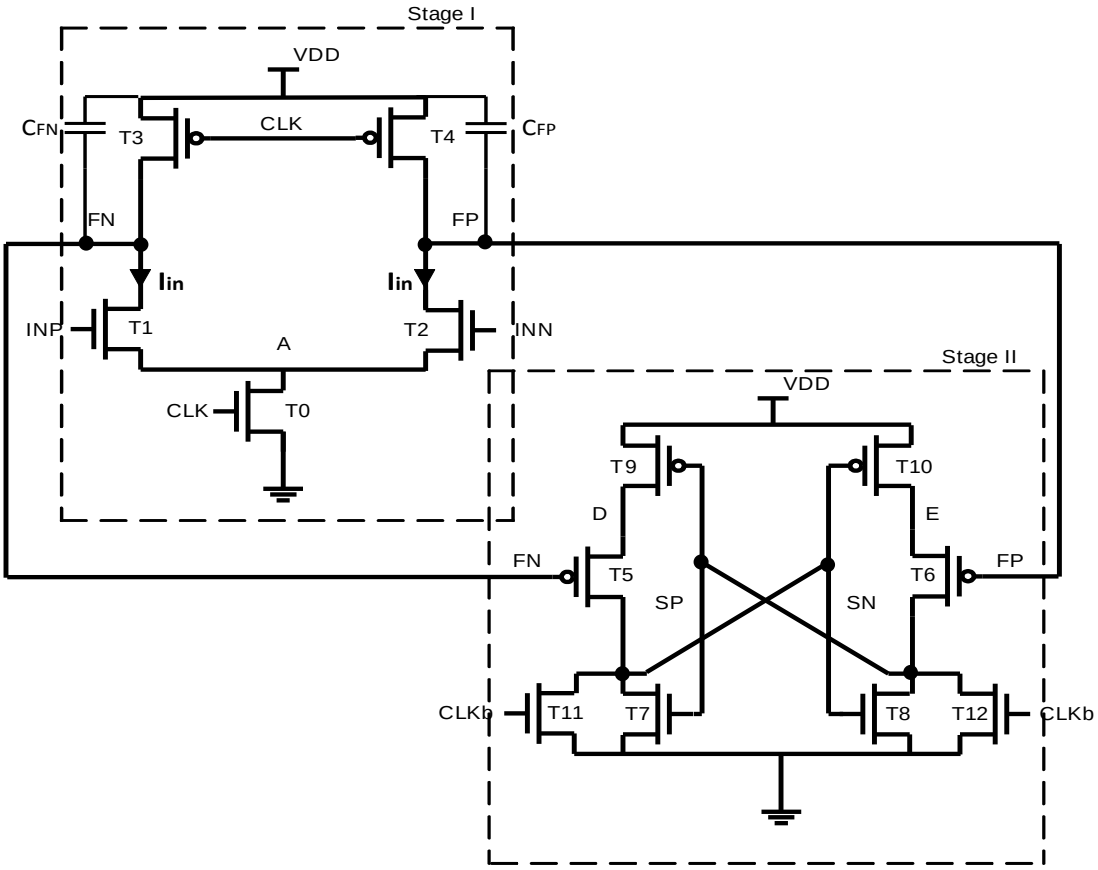


Fig. 5.5 Schematic of the dynamic comparator

At the beginning of the evaluation phase, the input pair T1 and T2 are working in the saturation region. The thermal noise is due to the resistive channel of a MOS transistor in the active region. When it is working in the saturation region, the equivalent resistance of the channel $R_{n,\,MOS}$ can be regarded as

$$R_{n,MOS} = \frac{1}{\frac{2}{3} g_m} \qquad (5.1)$$

The equivalent noise resistor of each of the input transistors T1 and T2 are in series with the DAC output. The equivalent noise resistor of the input pair R_n is

$$R_n = 2R_{n,MOS} = \frac{3}{g_m} \qquad (5.2)$$

According to [15], for a resistor R, the equivalent input referred noise Vn(f), is denoted as

$$V_n^2(f) = 4kTR \qquad (5.3)$$

Where k is Boltzmann's constant(1.38×10^{-23} JK^{-1}), T is the temperature in Kelvins. Therefore, the equivalent voltage noise of the input pair T1 and T2, $V_{n,\,ip}$ is

$$V_{n,ip}^2(f) = 4kTR_n = 4kT\frac{3}{g_m} \tag{5.4}$$

$V_{n,ip}^2(f)$ is the spectral density of input referred noise. NBW is the noise bandwidth, the input-equivalent integrated noise can be estimated by

$$\sigma = \sqrt{4kTR_n \bullet NBW} = \sqrt{4kT\frac{3}{g_m} \bullet NBW} \tag{5.5}$$

The derivation of noise bandwidth NBW has been done in [16] and is shown as below. Assume that the integration time of the noise signal is T_{int}. The noise in time domain can be expressed as

$$H(t) = \frac{1}{T_{\text{int}}} \int_{-\frac{T_{\text{int}}}{2}}^{\frac{T_{\text{int}}}{2}} \delta(t)\,dt \tag{5.6}$$

And in the frequency domain it is expressed as

$$H(f) = sinc(\pi f T_{\text{int}}) \tag{5.7}$$

The equivalent noise bandwidth is defined as (see [17]) as

$$NBW = \frac{\int_0^{\infty} |H(f)|^2\,df}{|H(f)|_{\max}^2} = \frac{1}{2T_{\text{int}}} \tag{5.8}$$

The voltages at the output nodes of the first stage FP and FN are sampled when they have changed by the threshold voltage of its input pair $V_{threshold}$. The current through each of the input transistors T1 and T2, I_{in} is used to charge the parasitic capacitance at nodes FP and FN, namely C_{FP} and C_{FN}. C_{FP}= C_{FN} is assumed. The integration time T_{int} is estimated as

$$T_{\text{int}} = \frac{V_{threshold}C_{FP}}{I_{in}} = \frac{V_{threshold}C_{FN}}{I_{in}} \tag{5.9}$$

Thus, NBW can be expressed as

$$NBW = \frac{I_{in}}{2V_{threshold}C_{FP}} \tag{5.10}$$

Insert (5.10) into (5.5), the result is shown as below

$$\sigma = \sqrt{4kT\frac{3}{g_m}\frac{I_{in}}{2V_{threshold}C_{FP}}} \tag{5.11}$$

Since in saturation region,

$$g_m \approx \frac{I_{in}}{INP} \approx \frac{I_{in}}{INN}$$

Approximate INP and INN to V_{CM}, the common mode voltage

$$g_m \approx \frac{I_{in}}{V_{CM}}$$

Thus, the IRN can be expressed as

$$\sigma = \sqrt{6kT\frac{V_{CM}}{V_{threshold}C_{FP}}} \tag{5.12}$$

Given a desired maximum noise level, the required minimum C_{FP} and C_{FN} value can be expressed as

$$C_{FP} \geq \frac{6kTV_{CM}}{\sigma^2 V_{threshold}}$$

From the equation above, it can be seen that the IRN (input referred noise) is proportional to $1/\sqrt{C_{FP}}$. Therefore, varying the value of C_{FP} is enough to optimize the IRN of the comparator.

According to the requirements of the project, there are two modes in the comparator. One mode is the low power and low accuracy mode, and the other is the high power and high accuracy mode. In the low accuracy mode, the accuracy level is 8-bit level. When working the high accuracy mode, the accuracy level is 10-bit level. Hence, the IRN of the low accuracy mode should be 4 times that of the high accuracy mode. According to the calculations above, IRN can be varied by changing the load capacitor. Therefore, the approach to implement two different working modes is to add a load capacitor C_a at FP

and FN, as shown in Fig. 5.6 below. Denote the IRN of the low accuracy mode and high accuracy mode as σ_l and σ_h, respectively, thus

$$\sigma_l = 4\sigma_h$$

Therefore, according to equation 5.12, the following equation should be met.

$$\sqrt{6kT\frac{V_{CM}}{V_{threshold}C_{FP}}} = 4\sqrt{6kT\frac{V_{CM}}{V_{threshold}\left(C_{FP}+C_a\right)}}$$

$$\frac{C_{FP}+C_a}{C_{FP}} = 16$$

As discussed in section 5.2, in the comparator,

$$C_{FP} = C_{FN} \approx 7\,fF\ .$$

Therefore,

$$C_a \approx 100\,fF$$

is assumed.

5.4 Performance of the Proposed Comparator

As discussed above, a two-mode comparator is designed. The schematic of the comparator and the sizes of the transistors are shown in Fig. 5.6. The two working modes are switched by signal CTL. CTL is produced by a latch in SAR logic, and it is discussed in detail in Chapter 7. When CTL=1, C_a is not loaded to the comparator, and the comparator works in the low accuracy and low power mode. When CTL=0, C_a is loaded to the comparator, and the comparator works in the high accuracy and high power mode as shown in Table 5.3. The IRN and power of each mode are shown in Table 5.4.

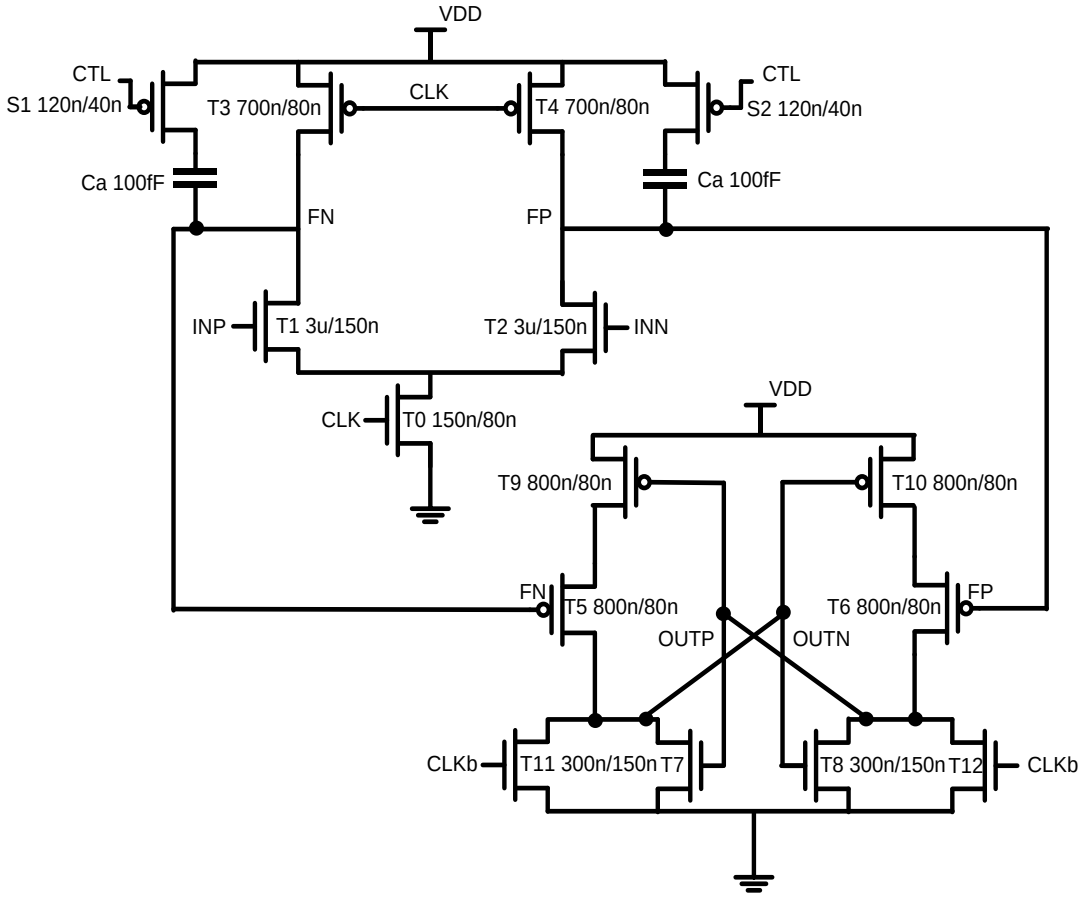


Fig. 5.6 Schematic of the proposed two-mode comparator

Table 5.3 Explanation of the two working modes

Step	CTL	Working mode
1 to 8	CTL=1	Low accuracy and low power mode
9 to 11	CTL=0	High accuracy and high power mode

Table 5.4 Power and IRN of the two modes

Accuracy setting	Energy per sample	IRN
Low-accuracy low-power mode	12.92fJ	0.306mVrms
High-accuracy high-power mode	214.15fJ	0.0736mVrms

As introduced in the beginning of the chapter, for a conventional 10b SAR ADC, all the 10 steps are performed in the high accuracy mode. In this manner, the energy consumed is 214.2x10=2142fJ. For the two-step scheme, the first 8 steps are performed in the low accuracy mode, while the last 3 steps are in the high accuracy mode. In this manner, the energy consumed is 12.92x8+214.2x3=745.96fJ. The two-step scheme provides about 65% energy reduction compared to a conventional scheme. The energy comparison between the two methods is shown as Table 5.5.

Table 5.5 Energy Comparison between the Conventional and the Two-Step Searching Scheme

	Energy
Conventional searching scheme	2142fJ
Two-step searching scheme	745.96fJ
Energy Reduction	65%

5.5 Summary

In this chapter, the design of a two-mode comparator is presented. The calculations of its power and IRN are performed. By adding a load capacitor C_a, the comparator has lower IRN but higher power. The two working modes are interlaced by controlling C_a.

Chapter 6

The Design of a DAC Array

In this chapter, the design of a DAC array is presented. The conventional switching scheme cannot be applied to implement the non-binary algorithm. Therefore, a monotonic switching scheme is applied. The details will be talked about in this chapter.

6.1 Structure of a Conventional DAC Array

The structure of a conventional DAC array for a 3-bit SAR ADC is shown in Fig. 6.1. The differential inputs of the comparator, V_p and V_n, are provided at the top plates of two DAC arrays.

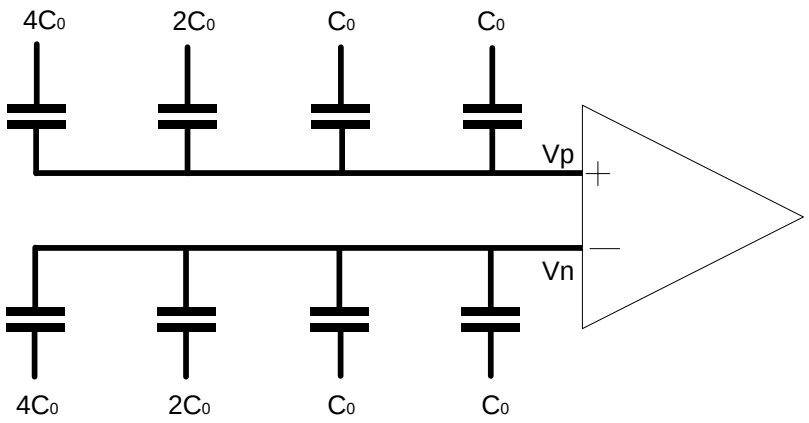


Fig. 6.1 Conventional DAC array for a 3-bit SAR ADC

Name the common mode voltage and differential inputs of a conventional SAR ADC V_{cm}, V_{ip} and V_{in}, respectively. In the *k*-th step, if $V_p > V_n$, the comparator output *d(k)* =0. Otherwise, if $V_p < V_n$, *d(k)* =1. V_p and V_n are expressed as follows

$$V_p = V_{cm} - V_{ip} + \left(2^{-1} + \sum_{i=2}^{k} \left(2d\left(k-1\right) - 1 \right) 2^{-i} \right) V_{ref} \qquad (6.1)$$

$$V_n = V_{cm} - V_{in} + \left(2^{-1} - \sum_{i=2}^{k} \left(2d\left(k-1\right) - 1 \right) 2^{-i} \right) V_{ref} \qquad (6.2)$$

For the DAC array in Fig. 6.1, there are two phases, namely sampling phase and comparison phase. Sampling phase takes place before the conversion phase. In the sampling phase, the top plates are charged to common mode voltage V_{cm}. Differential input pair V_{ip} and V_{in} are sampled and charges the capacitors. The operation of a conventional DAC array for a 3-bit SAR ADC is shown as Fig. 6.2.

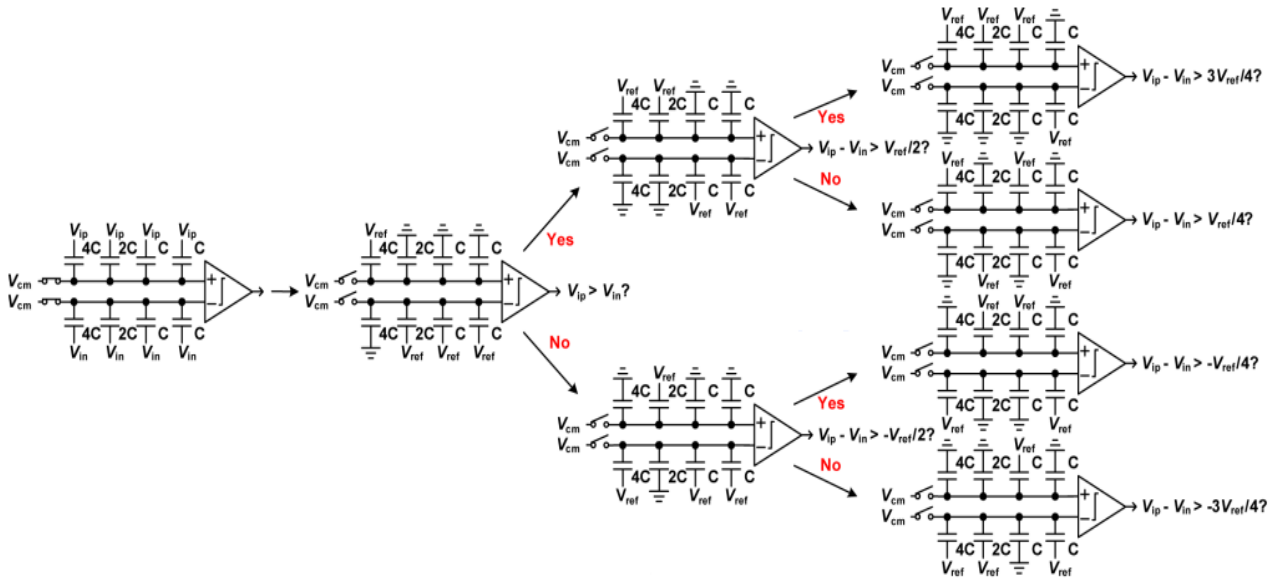


Fig. 6.2 Operation of a conventional 3-bit SAR ADC

In the switching procedure, the DAC array operates like a balance. The weights of the two plates are adjusted, and they are closer to each other every time they are adjusted. At the end of one conversion cycle, the difference between the voltages of the two top plates, V_p and V_n is less than 1LSB.

The switching operation of the DAC array is bi-directional, which means that V_p and V_n are changing at the same time. It can be seen from equation (6.2) that when V_p is reduced by $2^{-i}V_{ref}$, V_n will be increased by $2^{-i}V_{ref}$. The conventional DAC array has a simple structure and easy to operate. However,

such a structure is not adopted in this project. The bi-directional switching method cannot be used to implement a non-binary algorithm, as will be explained with an example below.

Take an example of a 3-bit SAR ADC using the generalized NB algorithm. The weights of the DAC array is p(1)=4, p(2)=1, p(3)=1, p(4)=1, as shown in Fig. 6.3.

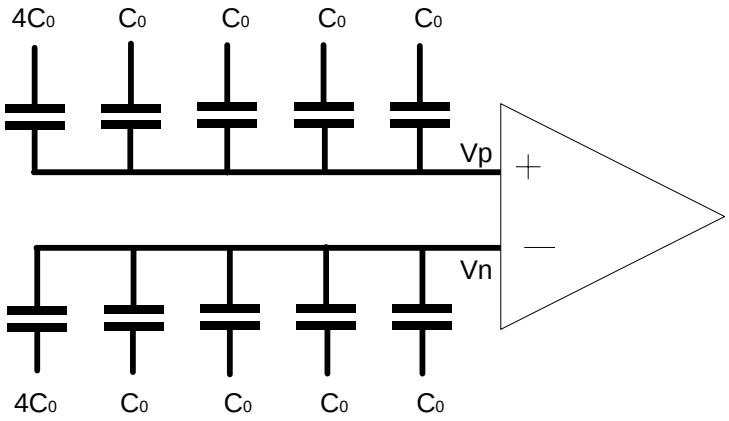


Fig. 6.3 DAC array of a 3-bit generalized NB SAR ADC using the conventional structure

The operation of the 3-bit ADC is explained as below and the operation is shown in Fig. 6.4.

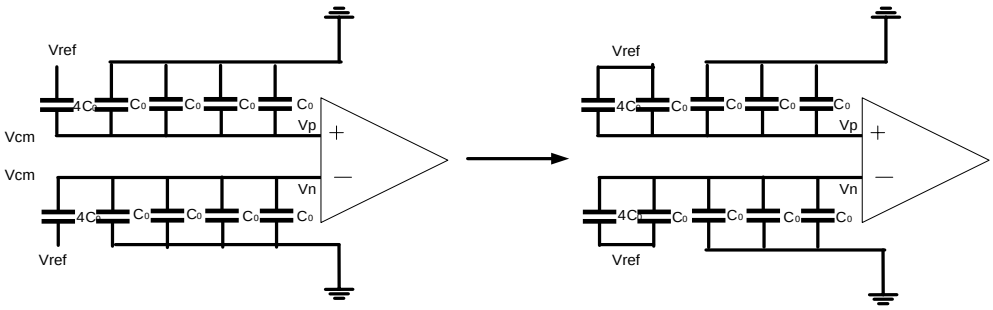


Fig. 6.4 DAC array of a 3-bit generalized NB SAR ADC using the conventional structure

Assume that $V_{ip}= 11V_{ref}/12$ and $V_{in}=V_{ref}/12$ respectively. In the first step, V_p and V_n are

$$V_p = V_{cm} - V_{ip} + \frac{1}{2}V_{ref}$$

$$V_n = V_{cm} - V_{in} + \frac{1}{2}V_{ref}$$

$V_p > V_n$ is resulted. In the second step, V_p should be decreased while V_n should be increased. To make a

correct comparison, the values of V_p and V_n should be

$$V_p = V_{cm} - V_{ip} + \frac{1}{2}V_{ref} - \frac{1}{8}V_{ref}$$

$$V_n = V_{cm} - V_{in} + \frac{1}{2}V_{ref} + \frac{1}{8}V_{ref}$$

However, the control switches are put as shown in Fig. 6.4, which makes the values of V_p and V_n.

$$V_p = V_{cm} - V_{ip} + \frac{1}{8}V_{ref}$$

$$V_n = V_{cm} - V_{in} + \frac{7}{8}V_{ref}$$

The values are not correct. The conventional structure fails to implement the generalized NB algorithm. The failure arises from the bi-directional switching nature of the structure. Therefore, the conventional structure cannot be adopted in this project.

To implement the generalized NB algorithm, a monotonic switching scheme [5] is used. The structure and the operation procedure of the switching scheme is explained below using the example of a 3-bit SAR ADC. In the example, the differential inputs are V_{ip}= 11V_{ref}/12 and V_{in}=V_{ref}/12, respectively. The operation is shown in Fig. 6.5.

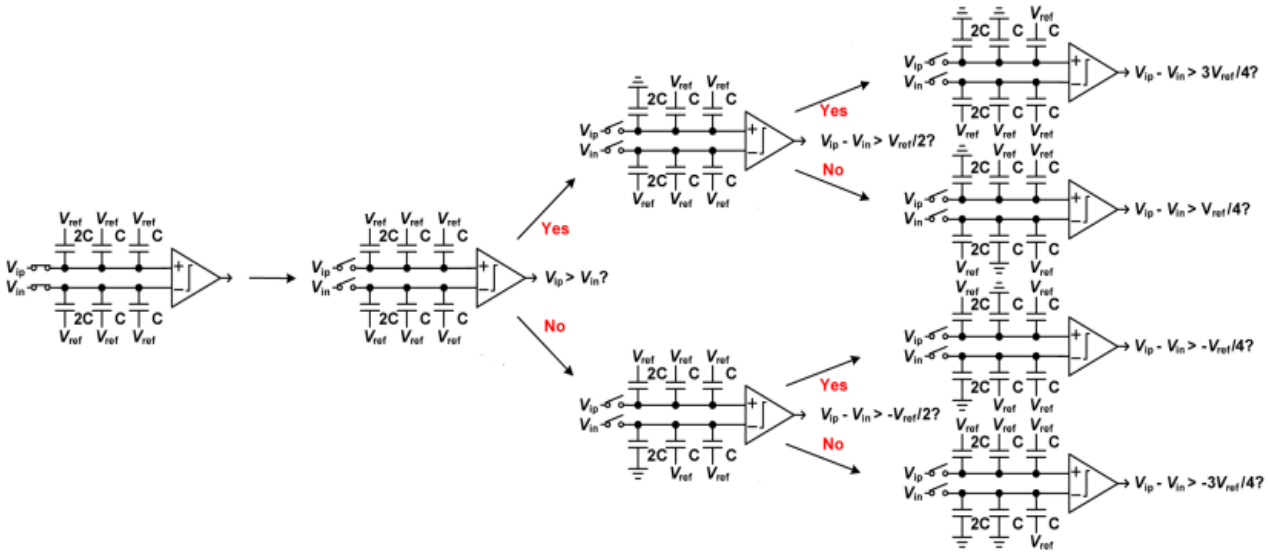


Fig. 6.5 Operation of the monotonic switching scheme of a 3-bit NB ADC

The same as mentioned above, the voltages on the two top plates are V_p and V_n. *d(k)* is the comparator output in the *k*-th step. If $V_p > V_n$, *d(k)*= 0. If $V_p < V_n$, *d(k)*=1. V_p and V_n can be expressed as

$$V_p = V_{ip} - \sum_{i=2}^{k} \left(2d\left(i-1\right) p\left(i\right)\right) V_{ref}$$

$$V_n = V_{in} + \sum_{i=2}^{k} \left(2d\left(i-1\right) p\left(i\right)\right) V_{ref}$$

The switching scheme is operating in a monotonic manner, which is different from a conventional structure. The voltages of the two top plates V_p and V_n are not changing at the same time. Its monotonic operation is a proper choice to implement the generalized NB algorithm. Take the example of a 3-bit NB ADC. In the ADC, *p(1)*=4, *p(2)*=1, *p(3)*=1, *p(4)*=1, as shown in Fig. 6.6. The differential inputs are V_{ip}= 11V_{ref}/12 and V_{in}=V_{ref}/12.

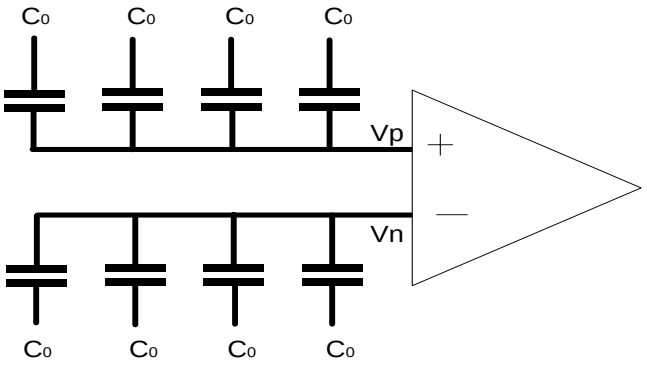


Fig. 6.6 DAC array of a 3-bit NB SAR ADC

The operation procedure is explained in Fig. 6.7.

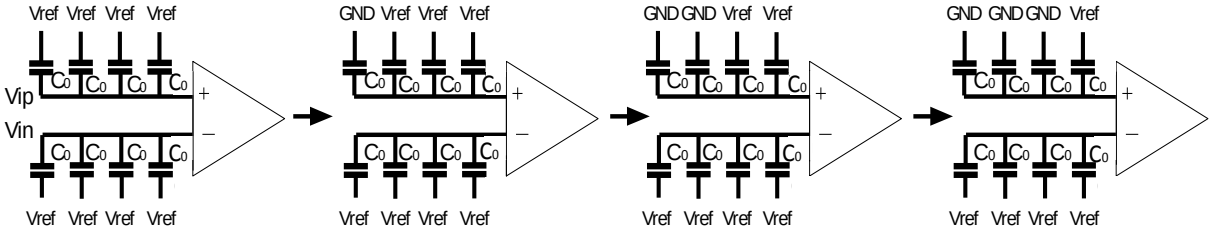


Fig. 6.7 The operation of the monotonic switching scheme

In the first step

$$V_p=11V_{ref}/12$$

$$V_n=V_{ref}/12$$

Vp > Vn and *d(1)*=1. In the second step,

$$V_p=8V_{ref}/12$$

$$V_n=V_{ref}/12$$

$V_p > V_n$ and *d(2)*=1. In the third step,

$$V_p=5V_{ref}/12$$

$$V_n=V_{ref}/12.$$

$V_p > V_n$ and *d(3)*=1. In the fourth step,

$$V_p=2V_{ref}/12$$

$$V_n=V_{ref}/12.$$

$V_p > V_n$ and *d(4)*=1. The 4-bit digital output is 1111, which, according to equation (4.11), makes the digitized output $D_{OUT}=7V_{ref}/8$. The output is a correct value, which proves that the monotonic switching method can be used to implement the generalized NB algorithm.

6.2 The Design of Switches

The operation of the control switches of the bottom plate of the DAC array is shown as Table 6.1.

Table 6.1 Operation of Bottom Switches

Sample Signal	Comparison Result	Voltage at Bottom Plate
1	-	V_{ref}
0	1	GND
0	0	V_{ref}

NMOS switches can pass a strong 0 and PMOS switches can pass a strong 1. Combined with logic gates, the control circuit of the bottom plate is shown as Fig. 6.8. “Smp” is an external signal source, and the settings are shown as Fig. 6.9(a). “Smpb” is generated by “Smp” through an inverter as shown in Fig. 6.9(b). “Cmp” is the comparator result. In this design, V_{ref} is set to V_{DD}, so PMOS is used for V_{ref}.

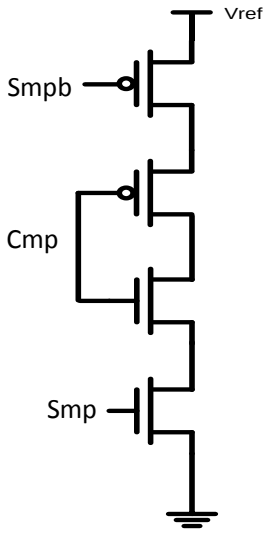
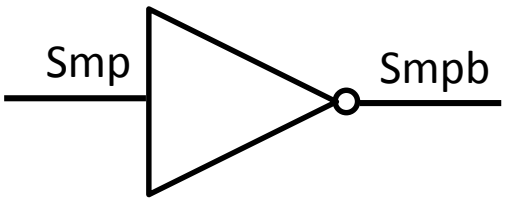


Fig. 6.8 Schematic of control switches

CDF Parameter	Value	Display
Frequency name for 1/period		off
Noise file name		off
Number of noise/freq pairs	0	off
DC voltage		off
AC magnitude		off
AC phase		off
XF magnitude		off
PAC magnitude		off
PAC phase		off
Voltage 1	0 V	off
Voltage 2	1 V	off
Period	3.25u s	off
Delay time	100p s	off
Rise time	100p s	off
Fall time	100p s	off
Pulse width	250n s	off

(a)



(b)

Fig. 6.9(a) Settings of Smp. (b) How Smpb is generated

The charging current of the capacitors should be large enough to charge the capacitors, so that the capacitors can settle down before the comparator makes a decision.

6.3 Summary

In this chapter, the design of the DAC array is introduced. The conventional switching scheme is discussed and the reason why it cannot be applied to implement the non-binary algorithm is also explained. A monotonic switching scheme is introduced and applied to implement the non-binary algorithm.

Chapter 7

The Design of the SAR Logic

As briefly introduced in Chapter 5, a two-step scheme is used in this project. In this chapter, the operation of the two-step scheme is illustrated in detail. The design of the SAR logic is also introduced.

7.1 Operation of the Two-Step Scheme

For a conventional 10-bit SAR ADC, 10 steps are performed. 10-bit accuracy level is required in each step to achieve the required resolution. After the 10 steps, the searching interval is resolved within 1LSB. However, for the two-step scheme, the first 8 steps are performed in the 8-bit accuracy level. In an ideal case without noise consideration, after 8 steps, the searching interval is resolved within 4LSB. In this case, two more steps in the 10-bit accuracy level are required to narrow the interval to 1LSB. However, in reality, after the first 8 steps, the interval is within 4LSB+ Δ. Δ is due to the noise of the comparator and for the 8-bit accuracy mode, Δ is within 2LSB. This means that the maximum value of the interval is 6LSB. To narrow the 6 LSB to the final 1LSB, at least 3 more steps in the 10-bit accuracy level are needed. The explanation above is illustrated in Fig. 7.1. Therefore, theoretically, using the two-step scheme, 11 steps can be resolved.

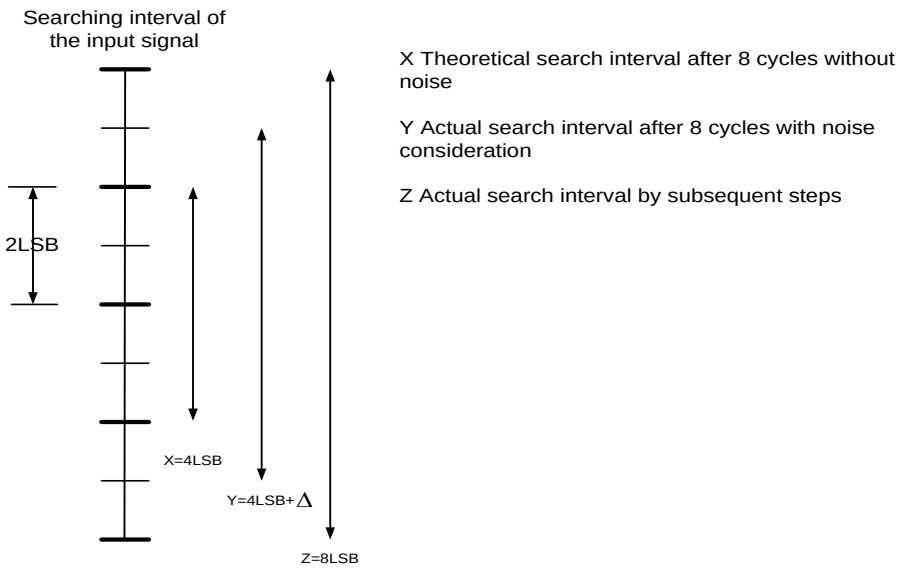


Fig. 7.1 Illustrations of the two-step scheme for a 10-bit SAR ADC

Different from the conventional scheme, 11 instead of 10 steps are required in the two-step scheme. To implement the additional step, the generalized non-binary algorithm reviewed in Chapter 4 is applied. It was mentioned in Chapter 4 that in the generalized non-binary algorithm, M steps are required for an N-bit SAR ADC (M > N). In this project, N=10, M=11.

7.2 Design of the SAR logic

In this section, the conventional SAR structure is first reviewed, followed by the design of the SAR used in this project.

7.2.1 The Conventional Structure of SAR

The block diagram of a conventional SAR logic is shown as Fig. 7.2.

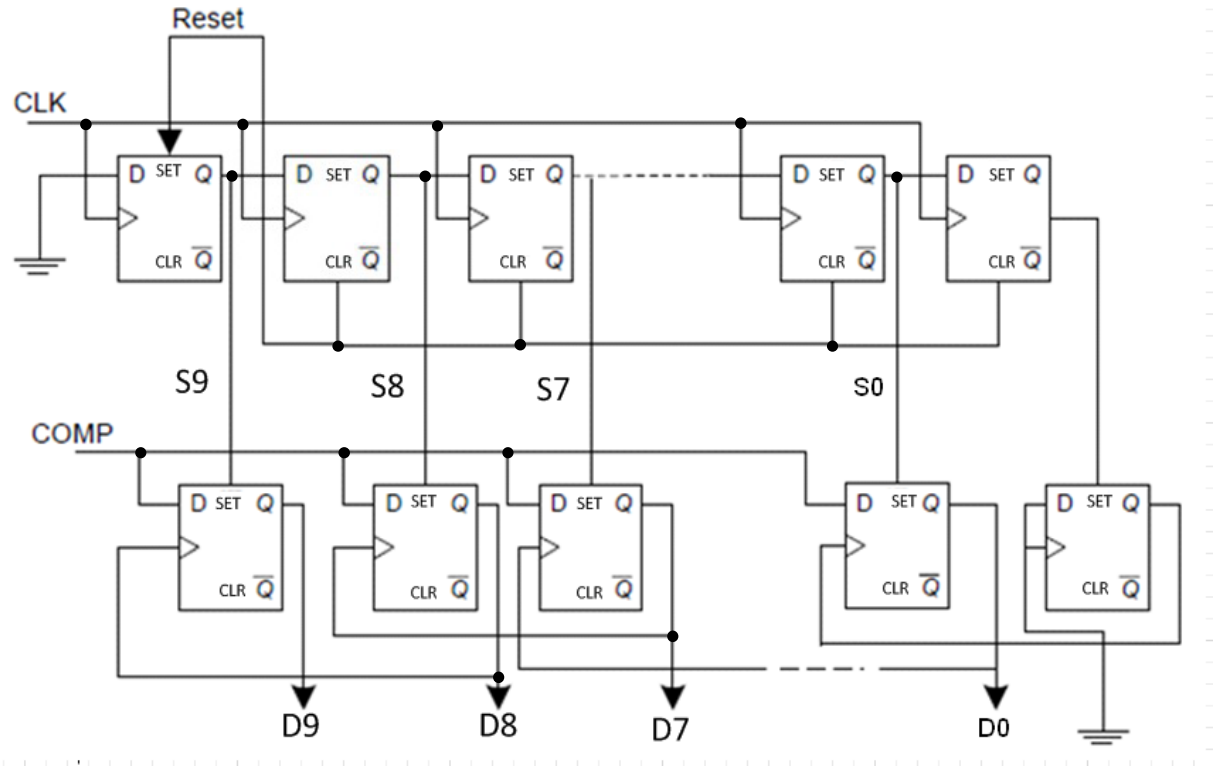


Fig. 7.2 Block diagram of a conventional 10-bit SAR ADC

The SAR logic is formed by 2N+2 flip flops for an N-bit SAR ADC, and it is actually a state machine. The digital outputs of the SAR logic D9-D0 are applied to the control switches of DAC array. In clock cycle 0, the sample signal Smp=1 (settings of Smp is in section 6.2 in pages 53-54) and the input signal of SAR ADC is sampled. At the same time, the reset signal Reset=1, which resets S9-S0 and D9-D0 to 0. For the rest of the cycles Smp=0, and Reset=0. Settings of Reset s shown in Fig. 7.3. In clock cycle1, the most significant flip flop is set to 1, which makes the MSB of the digital word set to 1. Then in each of the rest cycles, the counter shifts "1" through the flip flops from MSB to LSB. In each clock cycle, one of the outputs in the ring counter sets a flip flop in the code register. The output of this flip flop which is set by the ring counter is used as the clock signal of the previous flip flop. At the rising edge of the clock, the output of the comparator is loaded to the previous flip flop. Therefore, for this SAR logic, N+2 cycles are needed for an N-bit conversion. The operation and signals of the SAR are explained in Table 7.1. In Table 7.1, Cmp indicates the output of the comparator.

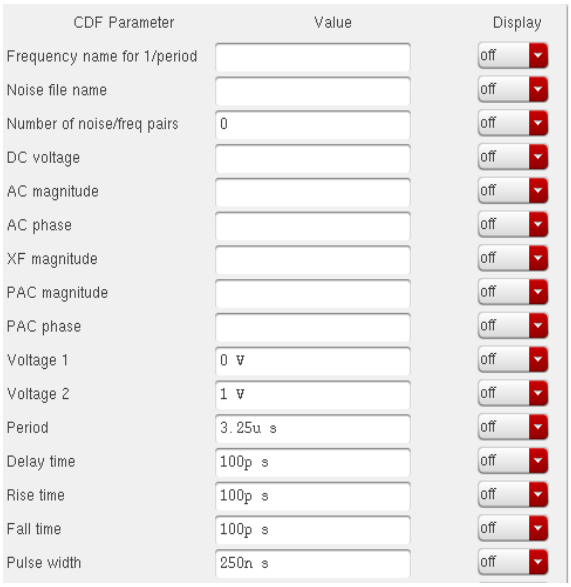


Fig. 7.3 Settings of Reset

Table 7.1 Outputs of the SAR Logic

Cycle	Smp	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Cmp
0	1	0	0	0	0	0	0	0	0	0	0	-
1	0	1	0	0	0	0	0	0	0	0	0	D9
2	0	D9	1	0	0	0	0	0	0	0	0	D8
3	0	D9	D8	1	0	0	0	0	0	0	0	D7
4	0	D9	D8	D7	1	0	0	0	0	0	0	D6
5	0	D9	D8	D7	D6	1	0	0	0	0	0	D5
6	0	D9	D8	D7	D6	D5	1	0	0	0	0	D4
7	0	D9	D8	D7	D6	D5	D4	1	0	0	0	D3
8	0	D9	D8	D7	D6	D5	D4	D3	1	0	0	D2
9	0	D9	D8	D7	D6	D5	D4	D3	D2	1	0	D1
10	0	D9	D8	D7	D6	D5	D4	D3	D2	D1	1	D0
11	0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	-

Table 7.1 shows the operation of the SAR. In clock cycle 0, Smp=1, Reset=1, and outputs D9-D0 are reset to 0. In the following cycles, Smp=0, Reset=0. “1” is shifted through flip flops from MSB to LSB by the counter. At the rising edge of each clock cycle, the comparator output is loaded to the flip flops one by one. After 12 clock cycles, results of the 10 comparison steps are loaded to the flip flops D9-D0. For an N-bit comparison, N+2 cycles are needed.

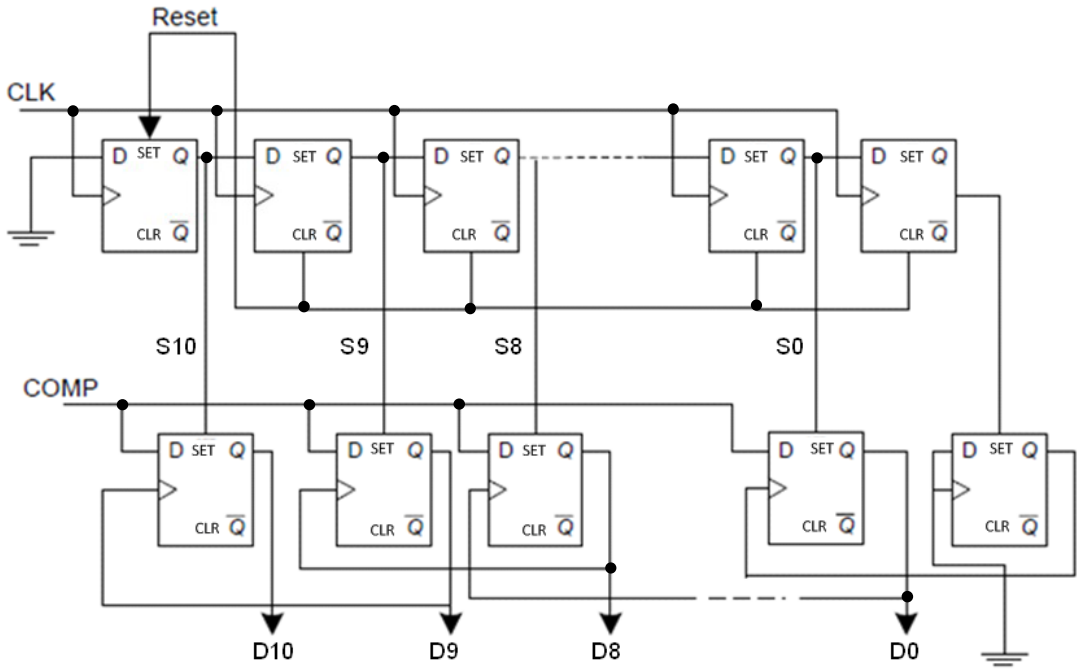
7.2.2 Design of the SAR in this Project

In this project, to implement the two-step scheme, a control signal (CTL as introduced in Chapter 5) is needed. This signal is used to shift the working modes of the comparator. When CTL=1, the comparator works in the low accuracy mode. When CTL=0, the comparator works in the high accuracy mode. In this project, the comparator works in the low accuracy mode for the first 8 steps and works in the high accuracy mode in the last 3 steps. Therefore, CTL remains 1 in the first 8 steps while it remains 0 in the last 3 steps as shown in Table 7.2.

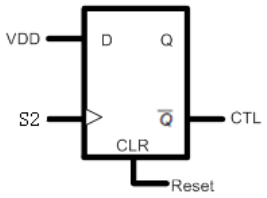
Table 7.2 Explanation of the two working modes

Step	CTL	Working mode
1 to 8	CTL=1	Low accuracy and low power mode
9 to 11	CTL=0	High accuracy and high power mode

To generate CTL, an additional flip flop is added in a conventional SAR logic. The SAR together with the additional flip flop is shown in Fig. 7.3.



(a)



(b)

Fig. 7.3 (a) Block diagram of the SAR for this project. (b) The added latch to get CTL signal

The outputs of the proposed SAR with the new added CTL are shown in Table 7.3. The operation of the proposed SAR is explained below Table 7.3.

Table 7.3 Outputs and CTL of the SAR

Cycle	Smp	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	CTL	Cmp
0	1	0	0	0	0	0	0	0	0	0	0	0	1	-
1	0	1	0	0	0	0	0	0	0	0	0	0	1	D10
2	0	D10	1	0	0	0	0	0	0	0	0	0	1	D9
3	0	D10	D9	1	0	0	0	0	0	0	0	0	1	D8
4	0	D10	D9	D8	1	0	0	0	0	0	0	0	1	D7
5	0	D10	D9	D8	D7	1	0	0	0	0	0	0	1	D6
6	0	D10	D9	D8	D7	D6	1	0	0	0	0	0	1	D5
7	0	D10	D9	D8	D7	D6	D5	1	0	0	0	0	1	D4
8	0	D10	D9	D8	D7	D6	D5	D4	1	0	0	0	1	D3
9	0	D10	D9	D8	D7	D6	D5	D4	D3	1	0	0	0	D2
10	0	D10	D9	D8	D7	D6	D5	D4	D3	D2	1	0	0	D1
11	0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	1	0	D0
12	0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	-

The flip flop of Fig. 7.3 (b) uses S2, an output from the ring counter as its clock signal. In clock cycle 0, S2 is set 0 and remains 0 until clock cycle 9. At the same time, CTL is set 1 by Reset. CTL stays 1 for the first 8 cycles until cycle 9 is triggered. In clock cycle 9, S2 is set 1. At the rising edge of S2, the clock loads V_{DD} and CTL is turned to 0. In this manner, CTL remains 0 for cycles 9, 10, 11, and 12 until the next conversion cycle comes. For the porposed SAR, because a redundant cycle is included to implement the non-binary algorithm, 13 instead of 12 cycles are needed for the 10-bit ADC.

7.3 Summary

In this chapter, the two-step scheme used in the project is explained and discussed in detail. The conventional structure of SAR is reviewed, followed by the SAR design of the project.

Chapter 8

Performance Evaluation

The implementation of the sub blocks of the SAR ADC is discussed in previous chapters. In this chapter, simulation results of the SAR ADC are shown and the performance of the system are discussed. The SAR ADC has 10-bit resolutoin, and its sampling frequency is 307kHz. The system is implemented in schematic level.

8.1 Generalized NB ADCs with Different DAC Array Values

Generalized non-binary algorithm is applied in this thesis. 1 redundant bit step is included for a conventional 10-bit ADC, so 11 steps are performed. According to the equations 4.13, 4.15 and 4.16 in Chapter 4, several sets of *p(k)* and *q(k)* values can be obtained, as shown in Table 8.1. Among all these cases, the conventional binary algorithm is applied in case 0 as a reference.

Table 8.1 SAR ADCs with different DAC array values

Case 0		Case 1		Case 2		Case 3		Case 4		Case5	
p(k)	*q(k)*	*p(k)*	*q(k)*	*p(k)*	*q(k)*	*p(k)*	*q(k)*	*p(k)*	*q(k)*	*p(k)*	*q(k)*
512	0	512	50	512	56	512	60	512	64	512	64
256	0	231	25	228	26	226	28	224	16	224	30
128	0	128	15	129	15	129	15	136	8	129	13
64	0	69	6	70	5	71	4	72	4	73	4
32	0	39	3	40	3	41	3	38	2	41	3
16	0	21	2	21	2	21	2	20	2	21	2
8	0	11	1	11	1	11	1	10	2	11	1
4	0	6	1	6	1	6	1	5	1	6	1
2	0	3	0	3	0	3	0	3	0	3	0
1	0	2	0	2	0	2	0	2	0	2	0
-	-	1	-	1	-	1	-	1	-	1	-

Table 8.1 shows various settings of a 10-bit 11-step ADC with different *p(k)* and *q(k)* values. *p(k)* values are the weight values of the capacitor array. *q(k)* values indicate the error tolerance of *k*-th step. With different settings, case 0-5 have different error correction abilities. The details are explained in section 4.3 in pages 21-22.

SAR ADCs with different capacitor array parameters shown in Table 8.1 are built. In these ADCs, only the comparator is implemented in schematic level, and all the other blocks are implemented in

Verilog A code.

To get DNL and INL results, the transfer curve of the ADC is required. The analog signal should be a ramp signal from 0 to the reference voltage, V_{ref}. The transfer curve of an ideal ADC and a non-ideal ADC are shown in Fig. 2.2. In an ideal ADC, no error occurs and the width of all staircases are 1LSB. However, in a non-ideal ADC, there is nonlinearity in the capacitor array and the comparator may make decision errors. Therefore, the widths of the staircases of a non-ideal transfer curve are not always 1LSB. DNL is the difference between the width of the staircase and 1LSB, as explained in section 2.2.1 and 2.2.2 (pages 6-8). For a 10-bit ADC, there are 2^{10}=1024 quantization levels, which means there are 1024 staircases. The higher accuracy we need, the more samples should be taken per digital word, then the longer time is needed by the simulator. In this thesis, only 2 samples are taken per digital word, so the DNL accuracy is 0.5LSB. This is not quite precise, but it is enough to give an indication of the DNL performances between ADCs. If 2 samples are taken per digital word, the total number of all samples is 1024x2=2048. The time needed for each sample is 3.25μs, so the total time needed to take all these samples is 3.25μsx2048=6.8ms. The corner used in the simulations is TT, 27ºC, VDD=1V. The settings of the input ramp signal is shown as Fig. 8.1.

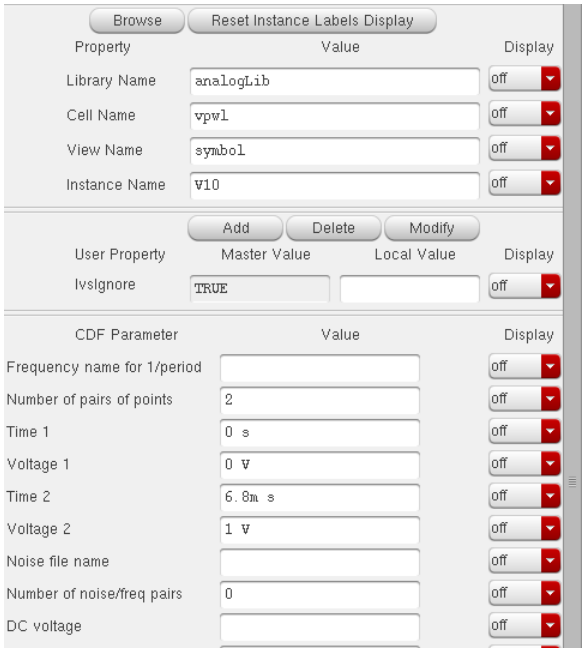


Fig. 8.1 Settings of V_{in} when simulating DNL/INL of ADC

The static performances of the ADCs are shown below in Table 8.2 and Table 8.3. Table 8.2 shows the static performance when the comparator is working in the high accuracy mode for all steps, while Table 8.3 shows the static performance when the two-step scheme is used.

Table 8.2 DNL/INL comparison with the conventional structure in Verilog-A

	Configurations	min DNL	max DNL	min INL	max INL
Binary	Case 0	-0.39	0.98	-0.9	1.12
Generalized non-binary	Case 1	-0.20	0.63	-0.50	0.47
	Case 2	-0.11	0.51	-0.48	0.50
	Case 3	-0.10	0.48	-0.48	0.45
	Case 4	-0.15	0.61	-0.50	0.48
	Case 5	-0.09	0.43	-0.47	0.44

Table 8.3 DNL/INL performance comparison using the two-step scheme in Verilog-A

	Configurations	min DNL	max DNL	min INL	max INL
Binary	Case 0	-0.59	1.20	-0.98	1.40
Generalized non-binary	Case 1	-0.20	0.90	-0.90	0.90
	Case 2	-0.11	0.73	-0.72	0.60
	Case 3	-0.10	0.67	-0.65	0.59
	Case 4	-0.16	0.86	-0.80	0.81
	Case 5	-0.09	q0.61	-0.62	0.49

From Table 8.2 and Table 8.3, it can be seen that for different settings, DNL/INL performances are different. All non-binary cases (case1-5) have better static performances than the binary one (case 0). Among all these cases, case 5 has the best static performance, no matter using the high-accuracy mode for all steps or using the two-step scheme. The author is still working on how the NB ADC's static performances are affected by the *p(k)* and *q(k)* values. The problem will be the major task of future research.

8.2 A NB ADC Using a Two-Mode Comparator

From the simulation results shown in Table 8.3, it can be seen that even when case1 is working in the high accuracy mode in all steps and case 5 is using the two-step scheme, the static performance of the latter is still better. It is proven in Chapter 5 that the two-step scheme shows better energy efficiency than the conventional one. Therefore, it is assumed that an SAR ADC using the two-step scheme and the DAC weights of case 5 will show better power efficiency than an SAR ADC using the conventional

scheme and the DAC weights of case 1, without damaging the static performance. To test the assumption, two ADCs are implemented in schematic level. One ADC is using the DAC weights of case 5 and the two-step scheme, while the other is using the DAC weights of case1 and works in the high accuracy mode in all steps. The DAC implementation was discussed in Chapter 6. The settings of the two ADCs are illustrated in Table 8.4. For the two ADCs, the reference voltage is 1V. The requirements for the project is for artificial pacemakers, which is low power biomedical applications, the sampling frequency is set 307kS/s [4] [21] [22].

Table 8.4 Settings of the Two ADCs

Proposed NB ADC			Conventional NB ADC		
	Step *k*	Weight *p(k)* (case6)		Step *k*	Weight *p(k)* (case1)
Low power and low accuracy mode	1	512	High power and high accuracy mode	1	512
	2	224		2	231
	3	129		3	128
	4	73		4	69
	5	41		5	39
	6	21		6	21
	7	11		7	11
	8	6		8	6
High power and high accuracy mode	9	3		9	3
	10	2		10	2
	11	1		11	1

The input signal to simulate DNL of the two ADCs is the same as shown in Fig. 8.1. The corner used is TT, 27 ºC, VDD=1V. DNL performances of the proposed NB ADC and the conventional NB ADC are shown in Fig. 8.2 and Fig. 8.3 below.

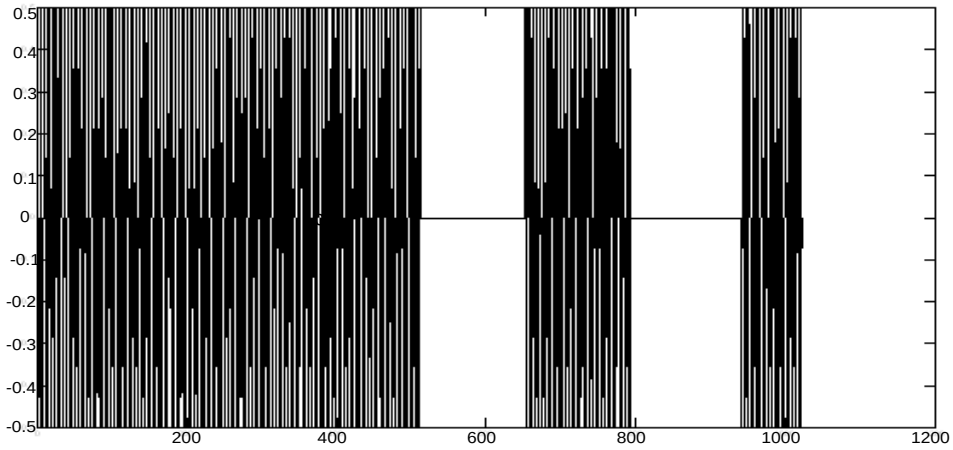


Fig. 8.2 DNL performance of the proposed NB ADC

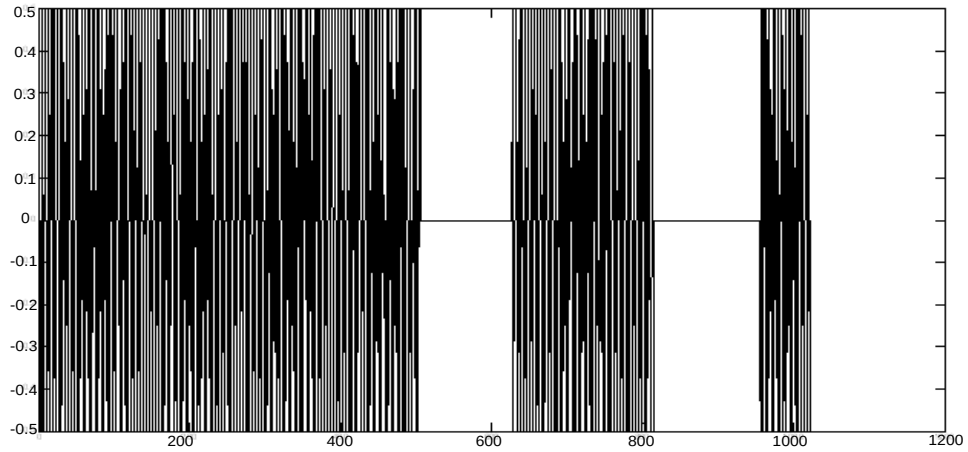


Fig. 8.3 DNL performance of the conventional NB ADC

The proposed NB ADC has more ”0”s, which implies better static performance. Since the DNL resolution is 0.5LSB, the value of DNL can only be 0, +_0.5, +_1….. From Fig. 8.2and Fig. 8.3, only -0.5, 0, and +0.5 are detected for DNL values. The numbers of each value’s appearance are calculated as shown in Fig. 8.4 and Fig. 8.5.

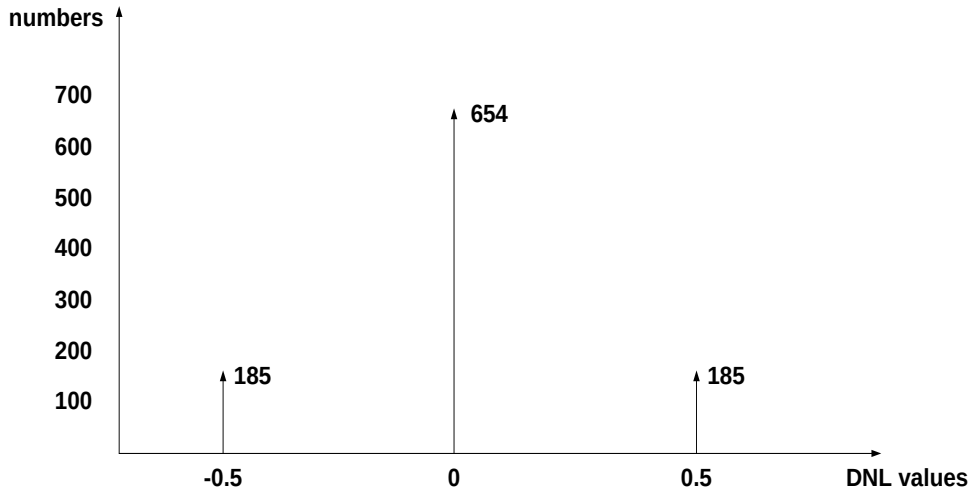


Fig. 8.4 Statistical illustration of the DNL performance of the proposed NB ADC

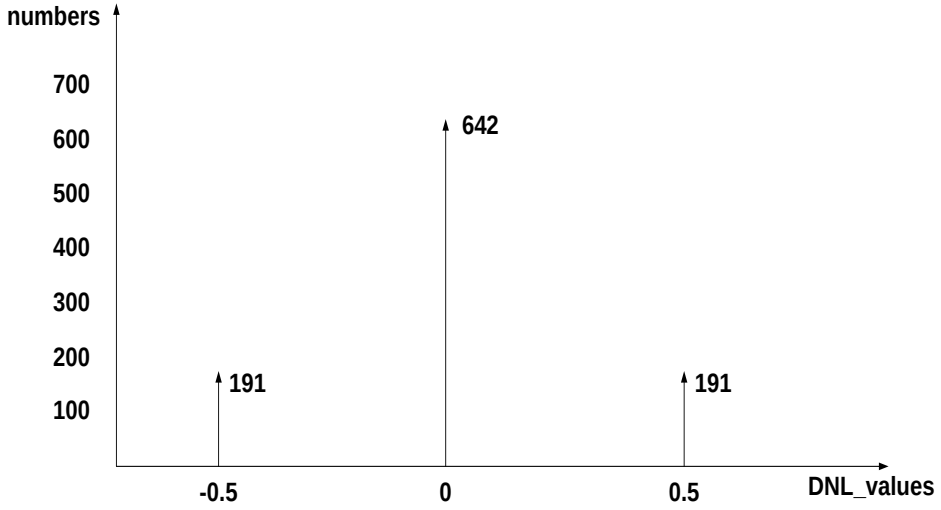


Fig. 8.5 Statistical illustration of the DNL performance of the conventional NB ADC

The simulations are conducted in schematic level. The nonlinearity in an actual capacitor array may introduce more errors, compared to a behavioral level ADC where all modules are implemented with Verilog A codes. Therefore, the static performances of the ADCs are worsened in schematic level simulations. It is seen from Fig. 8.4 and Fig. 8.5 that the proposed ADC has more “0”s than the conventional one, which indicates better static performance. The results are coherent with the assumption that better static performances are achieved by the proposed NB ADC. However, to better evaluate the performances of the two ADCs, dynamic performances are also necessary. Simulations are

conducted to obtain the ENOBs of the two ADCs.

When simulating the ENOB of the ADC, the input signal is a sinwave with frequency *f*, and the sampling frequency, *fs*, is sampling at Nyquist rate, namely twice the input signal frequency. *fs=2f* is resulted. The sampling frequency f for the proposed ADC is *fs*=307kS/s, so the frequency of the input sinwave signal is *f=fs/2*=153.5kS/s. Amplitude of the sinewave is 1V, as shown in Fig. 8.6. The corner used in the simulations is TT, 27 ºC. The ENOBs of the two ADCs are shown as Table 8.5.

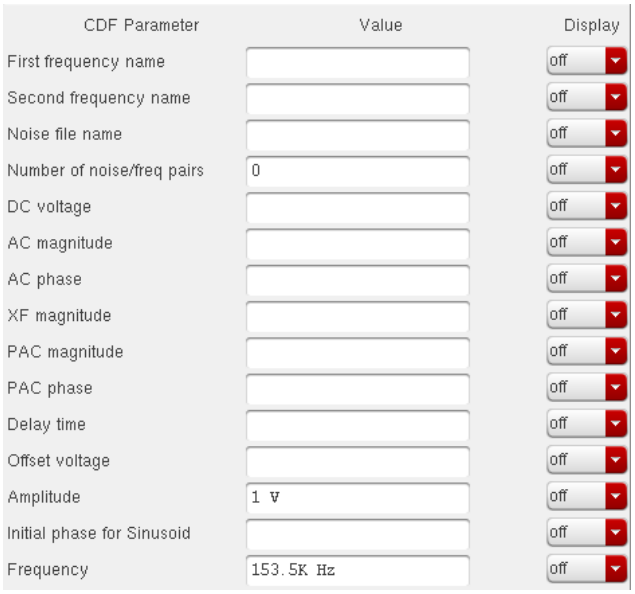


Fig. 8.6 Settings of the input sinewave

Table 8.5 ENOB Comparison between the Proposed and Conventional NB ADC

	ENOB
Proposed NB ADC	9.8665
Conventional NB ADC	9.8652

Simulation results in Fig. 8.4 and Fig. 8.5 indicate better, or comparable static performance are achieved by the proposed NB ADC. It is assumed that comparable dynamic performance should also be achieved by the proposed NB ADC. The simulation results in Table 8.5 indicate comparable dynamic

performances are achieved by the proposed NB ADC, which is coherent with the assumption.

To test the assumption that better power efficiency is provided by the proposed NB ADC than the conventional NB ADC, the power of these two ADCs are both simulated. Since Power=Voltage x Current and the supply voltage is always 1V. Therefore, to obtain the average power consumption, the average value of current, I, is needed. In the simulations settings, the input signal is a ramp signal as shown in Fig. 8.1. Functions “clip” and “average” are applied to get the average current I, as shown as Fig. 8.7. Once the average current I is calculated, Power, P, can be obtained by P=1(V) x I. The power simulation results are shown in Table 8.6.

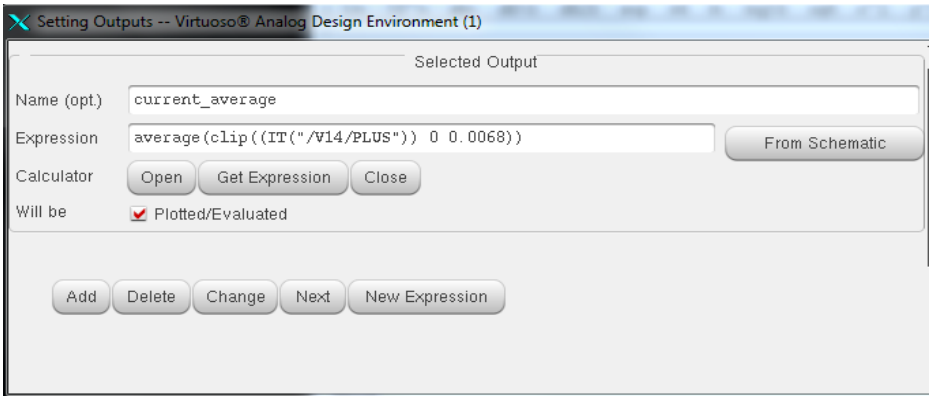


Fig. 8.7 Expression to get the average current flowing through power supply

Table 8.6 Power Consumption Comparison

	Power
Conventional Binary ADC	6.215μW
Conventional NB ADC	6.334μW
Proposed NB ADC	5.403μW
Power Reduction (between Conventional and Proposed NB ADC)	17%

From the above simulation results, it is concluded that comparable static and dynamic performances are

shown by the proposed NB ADC and the conventional NB ADC. However, the proposed NB ADC has the advantage of 17% higher power efficiency.

8.3 Summary

In this chapter, NB SAR ADCs with different DAC array values are implemented in Verilog A code, and their static performance are shown. A NB SAR ADC with a two-mode comparator is implemented in schematic level. A NB SAR ADC with the conventional structure is also constructed for performance comparison. Both ADCs are designed and simulated using GF 40nm technology. The simulation results show that with comparable static and dynamic performance, the NB ADC with a two-mode comparator shows better power efficiency.

Chapter 9

Summary and Future Work

9.1 Summary

In this thesis, the first work is to explain why SAR ADC is chosen and to introduce the motivation of the project. The motivation is to improve the power efficiency of the SAR ADC without worsening its static performance. To achieve this goal, a two-mode comparator is applied to lower the power consumption, and a generalized non-binary is applied to compensate for the errors resulted by the two-mode comparator. In Chapter 5, a two-mode comparator is designed. In Chapter 6, a monotonic switching scheme is applied to implement the non-binary algorithm. In Chapter 7, the SAR ADC is designed. In Chpater 8, a generalized NB (non-binary) SAR ADC with the conventional structure is first designed, followed by the proposed ADC with a two-mode comparator. The redundancy parameters for the proposed ADC are chosen such that it has the comparable static performance as the conventional generalized NB ADC. The two ADCs are implemented in schematic level using GF40nm process. Simulation results show that the ADC with proposed structure shows better power efficiency without worsening the static performance.

9.2 Future Work

The objective of the work is to reduce the power consumption by using a two-mode comparator, and to compensate for the errors resulted by the comparator with a generalized non-binary algorithm. Part of the goal has been achieved. In order to push further down in context of ultra-low power consumption,

to adjust the ADC to lower power supply is needed. The positive power supply for this work is V_{DD}=1V. The V_{DD} for low power applications has been lowered to 0.6V, or even 0.4V. The future work of the author is to lower V_{DD} to 0.4V~0.6V.

To reduce the comparator's power consumption is just the first step for further power reduction. A future research topic could be to combine the power reduction schemes in SAR and CDAC with the two-mode comparator proposed in this thesis.

Research Publications

Li Jianni, Yelaka Sunilgavaskar Reddy, Yvonne Y. H. Lam, “Non-Binary SAR ADC with a Two-Mode Comparator,” accepted by RFIT 2014

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