NANYANG TECHNOLOGICAL UNIVERSITY

NOVEL HIGH-K DIELECTRICS FOR NANOELECTRONICS

VANESSA CHONG MENG MENG
SCHOOL OF MATERIALS SCIENCE & ENGINEERING
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VANESSA CHONG MENG MENG

School of Materials Science & Engineering

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ABSTRACT

The aggressive downsizing in metal-oxide-semiconductor field effect transistors (MOSFET) has been the driving force for performance progress in microelectronics. In association with device parameters related to MOSFET, SiO_2 based oxide has already faced to its limit in further thinning due to excess gate leakage current. However, further scaling in equivalent oxide thickness (EOT) down to 0.5 nm or less requires a gate stack with a high k insulating layer. Till date, an EOT below 0.5 nm has been obtained with a careful deposition of a high-k combined with an optimized heat treatment to suppress the SiO_x-based low k interfacial layer growth. In addition to this process optimization, studies have revealed that rare earth oxide can achieve a direct contact of a high-k with Si substrate by forming RE-silicates at the interface, which produce dielectric constants of 8 to 20 pending on the amount of incorporated silicon.

Nevertheless, developing an alternative gate material with suitable high dielectric constants for approaching CMOS generations is one of the most challenging problems in the continuous development of electronics. The criteria for these materials are stringent.

On top of the basic and absolute requirement for higher permittivity (k)-values, the energy band offsets to silicon, interface and bulk charges and thermal stability, are among the various essential properties that need to satisfy the demands set by MOS production processes.

This work features the use of titanium oxide (TiO_2) and gadolinium silicate (GdSiO) as passivation layers to suppress the undesirable interfacial layer formation when high-k material is in contact with silicon substrate. In addition, to ensure the uniformity and conformality of these thin films, atomic layer deposition (ALD) is chosen to be the most suitable deposition technique to ensure good controllability of the thickness of these passivation layers.

The CeO_2/TiO_2 showed comparable dielectric constants but severe leakage degradation due to the interfacial layer and silicide formation post-annealing. As for CeO_2/GdSiO samples, although the k-value is lower (~13) but the leakage current is improved by 4-5 orders of magnitude as compared to CeO_2/TiO_2. Furthermore, leakage current conduction mechanism showed that upon annealing, the mechanism switches from Schottky to Poole-Frenkel emission for CeO_2/GdSiO samples due to bulk CeO_2 being dominant caused by oxidation state change of Ce^{2+} to Ce^{3+} which leads to oxygen vacancies.

1. INTRODUCTION

1.1 Motivations for High-k Dielectrics

Current literature reveals that metal oxide semiconductor field effect transistors (MOSFETs) on SiC are promising for high temperature and high power applications. For efficient functioning of the MOSFET system, a high quality gate insulator with low density of interface states, fixed oxide charges, and oxide traps is critical. In the past, surface oxides obtained through thermal oxidation of SiC revealed excellent properties for this purpose. However, even if SiO_2/SiC structures with low defect and trap densities can be achieved, the high operational electric fields for SiC-based devices will high field in SiO_2 causing reliability problems due to degradation effects. In order to attain improved performance of the SiC based devices, one should be able to apply an electric field with strength in proximity to critical value for SiC without degradation of the gate insulating layer. According to boundary condition within the oxide/SiC interface, studies have shown that the problem could be resolved by implementation of dielectrics with higher ε (high-K) [1-13].

Recently, rare earth metal oxides have attracted huge interest among researchers as potential candidates to replace SiO_2 in complementary metal oxide semiconductor (CMOS) technology, primarily owning to further scaling of CMOS devices requiring gate oxide equivalent thickness (EOT) below 1.2 nm for channel length of 70 nm. According to Moore's Law [2, 3, 14, 15], transistor and feature size are scaled to increase the speed and functionality of integrated circuit by doubling every 18-24 months. In order to maintain the electrostatic control of transistor channel by the gate, the gate oxide has to be decreased simultaneously with channel length [2, 16-19].

$$I_{on} = [(\mu_{eff} C_{ox,\,inv})/2] (W/L) (V_{gs} - V_T)^2 \quad (1)$$

From Equation (1), it is shown that one of the ways to improve the performance of transistor [20] is by increasing the oxide capacitance (C_{ox}).

$$C = (\varepsilon_0 \, k \, A)/t \quad (2)$$

Hence, in order to increase the capacitance, the conventional method was to decrease the thickness (d) of the gate oxide or increase the dielectric constant (k) as shown in Equation (2) [20].

However, as the thickness of silicon dioxide (SiO_2) approaches about 1.5nm or about 4 atomic layers of silicon and oxygen [1, 2, 15, 19, 21-25], reliability issues arise due to exponential increase in leakage current (beyond 100 A/cm^2 at 1 V) caused by direct tunnelling as depicted in Fig. 1 [15, 26, 27]. Issues such as the increase in power dissipation and also degradation of device performance and circuit stability are consequences of gate leakage current. Due to this undesirable high off state leakage current, conventional SiO_2 with sub-nanometer thickness has to be substituted and rare earth metal oxides seem to fulfil such requirements since they exhibit a high dielectric constant, a high band gap, and suitable band offsets with respect to Si.

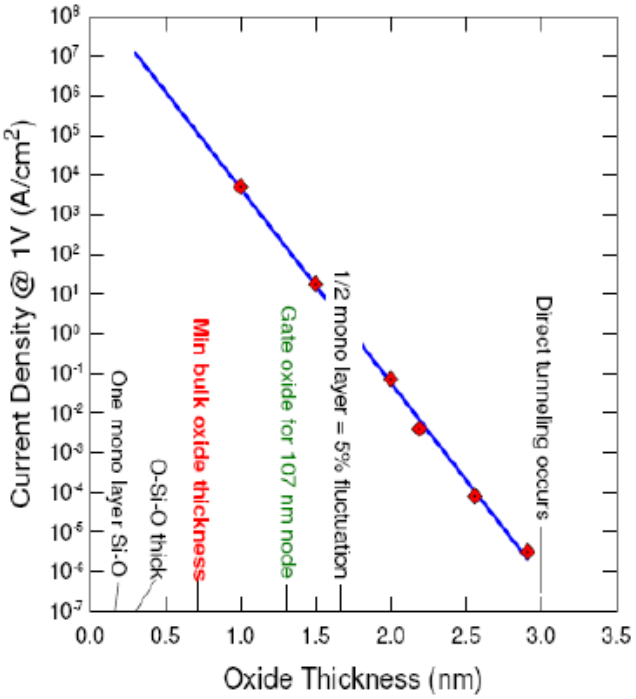

Fig. 1: Schematic plot indicating direct tunnelling current increases exponentially as the gate oxide becomes thinner. Oxide thinner than 1.2 nm would result in a too large leakage current and difficulties in process control: high-k materials must be adopted instead. [28]

1.2 Existing High-k Dielectrics

In 2004, the International Technology Roadmap of Semiconductors (ITRS) revealed that there is an urgent need to find an appropriate high-k dielectric for complementary metal-oxide-semiconductor (CMOS) technology in order to keep pace with Moore's Law [29]. This excerpt was taken from ITRS – 'early availability of manufacturing-worthy high-k dielectrics' is one of the difficult challenges in process integration for highly scaled metal-oxide-semiconductor field effect transistors (MOSFETs) and it is 'necessary to meet stringent gate leakage and performance requirements' which shows the urgency and complexity required to find a substitute for SiO_2 [2, 3, 15, 17, 29].

Studies have shown suitable candidates for future gate oxide such as hafnium oxide (HfO_2) [30], zirconium oxide (ZrO_2) [30] and trivalent lanthanide oxides (Ln_2O_3) as

seen in table 1. These single-component oxides that have simple phase diagrams and thus, make modelling simple for both experimental and theoretical approaches [31]. Ternary systems such as gadolinium scandate ($GdScO_3$) and lanthanum aluminate ($LaAlO_x$) are favourable due to their ability to maintain amorphous throughout temperature cycling [31].

High-k dielectrics are used to substitute conventional SiO_2 in order to suppress gate leakage current and maintain gate capacitance.

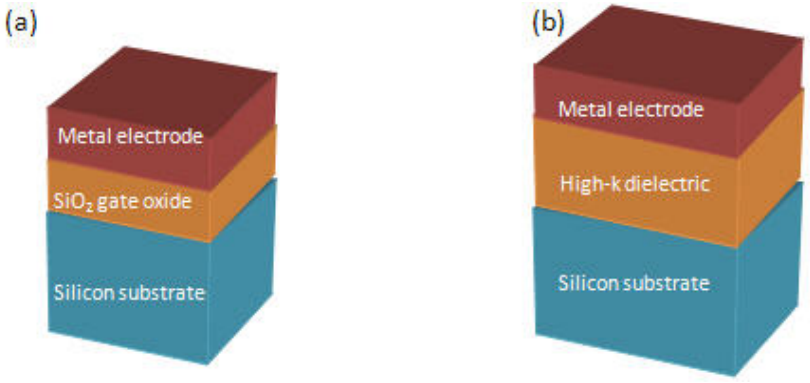

Fig. 2: Schematic diagram of metal-oxide-semiconductor (MOS) with (a) conventional SiO_2 gate oxide and (b) high-k dielectric

As shown in Fig. 2, by replacing SiO_2 with high-k dielectrics, the same amount of capacitance can be achieved with increased thickness that helps reduce the gate leakage.

$$EOT = (\varepsilon_{SiO_2} / k)\, t_{hi\text{-}k} \qquad (3)$$

This is displayed in Equation (3) whereby using high-k dielectrics help achieve the same capacitance as sub-nanometer thickness SiO_2 but with allowed relatively larger physical thickness which is defined as equivalent oxide thickness (EOT) [20].

Relevant high k-values achieved

Oxide	*k*
La_2O_3	30 [2] 27 [15]
Ce_2O_3	21.2 [6] ~ 15 [16]
CeO_2	16.6 [5]
Pr_2O_3 (Amor.)	15.5 [6]
Pr_2O_3 (Hex.)	25.4 [6]
Sm_2O_3	11.4 [26] 15 [26]
Eu_2O_3	13.7 [5]
Gd_2O_3	13.6 [5]
Dy_2O_3	13.1 [5]
Ho_2O_3	13.1 [5]
Er_2O_3	13 [5]
Yb_2O_3	13.4 [5]
Lu_2O_3	12.5 [5]
HfO_2	25 [2]
Ta_2O_5 (Amor.)	22 [2] 25 [6]
Ta_2O_5 (Hex.)	~60 [6]
Y_2O_3	15 [2]
ZrO_2	25 [2]
Nb_2O_5	29–50 [5]
TiO_2	86 [5] 80 [2]
$LaAlO_3$	30 [2] 27 [5]
La_2CuO_4	45 [5]
$LiNbO_3$	43.9 [5]
$GdScO_3$	22 [22]
$DyScO_3$	22 [22]
$LaScO_3$	22 [22]
Sc_2O_3	14 [24]

Relevant Literatures:

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[26] Jeon S, Im K, Yang H, Lee H, Sim H, Choi S, et al. Excellent electrical characteristics of lanthanide (Pr, Nd, Sm, Gd, and Dy) oxide and lanthanide-doped oxide for MOS gate dielectric applications. In: International Electron Devices Meeting. Technical Digest, IEDM 2001. p. 471–4.

Table 1: Permittivity of high k-values metal oxides based on various literatures [26, 32]

1.3 Current Issues with High-k Dielectrics

Substituting the conventional SiO_2 with high-k seems relatively simple as shown in Equation (3) but there are still other considerations required when selecting a suitable high-k material besides the dielectric constant value (k). Research worldwide has been focusing on attaining amorphous materials with higher dielectric constants but studies have indicated challenges remained in keeping the material amorphous after post deposition high temperature processing [19]. Most of the high k oxides tend to become polycrystalline with grain boundaries leading to higher leakage

currents. In addition, the semiconductor/ dielectrics interface properties can impact the device performance significantly. Often, the interface is not stable and subjected to changes during and after the growth. The interface structure will determine the density of defects that have been known to serve as deep trapping centers which is undesirable. Hence, one of the critical issues is that the alternative gate oxide has to remain thermodynamically stable when in contact with silicon substrate [18, 26, 33]. It is important to prevent the formation of undesired Si-O interfacial layer which generates interface states and defects that are detrimental to MOS devices while limiting the lowest achievable EOT [2]. In addition, the formation of silicide (metal-Si) bonds is also undesirable as these metallic bonds act as precursor for interface traps [1, 2, 34, 35].

In addition, majority of the high-k material possess relatively narrow band gap and smaller conduction band offset (CBO) due to the *d* state electrons and high coordination ionic bond [34, 35]. This leads to large leakage current due to electron hopping and tunnelling into conduction band [3, 26]. High-k materials such as HfO_2 and ZrO_2 have low crystallization temperature which leads to grain boundary formation creating high oxide trap density. On the other hand, materials with low oxidation temperature are likely to form large amount of oxygen vacancies which are also active oxide trap centers [3, 15, 34]. Hence, it is essential to suppress the oxygen concentration at the interface. One possible way is to introduce proper gate electrode materials which have low diffusion constants of oxygen atoms, for instance, metal nitrides or silicides. Another alternative will be selecting a proper rare earth (RE) silicate material, which shows low oxygen diffusion constant or possesses a high dielectric constant. Therefore, high-k materials with small lattice mismatch which improves interfacial properties and may be possible for epitaxial film growth is

desirable as it reduces the interface and oxide traps as well as suppressing leakage current [15, 18, 36].

It has been reported that elemental oxides (e.g. TiO_2 and HfO_2) are unable to meet the requirements of future CMOS technology due to the interface, thermodynamic and electrical instabilities [1, 2, 37]. This is due to its intrinsic property of having *d* state electrons that are partially unfilled and loosely bounded as well as high coordination ionic bonds as shown in Fig. 3 [3, 8, 17, 35, 38]. The underlying physics for the undesirable properties of high k dielectric materials summarized in Fig. 3 is governed primarily by the ionic nature of the transition metal and rare earth metal oxygen bonds. The ionic or polarized metal oxygen bonds are also the reason for higher k values and for the presence of soft optical phonons, which further induce a large leakage current and channel mobility degradation. Hence, complex oxides such as silicates, alloys and doped-oxide are possible candidates to overcome these instabilities. Meanwhile, depending on the temperature, materials, and processing conditions, the thermal treatment of the high k metal oxides may yield the following results; repairing the defects (for instance, oxygen vacancies) created during deposition, crystallization, forming interface oxide and silicate layers, bond decompositions, interface strain releasing, phase separation of silicate and interface strain enhancement [19].

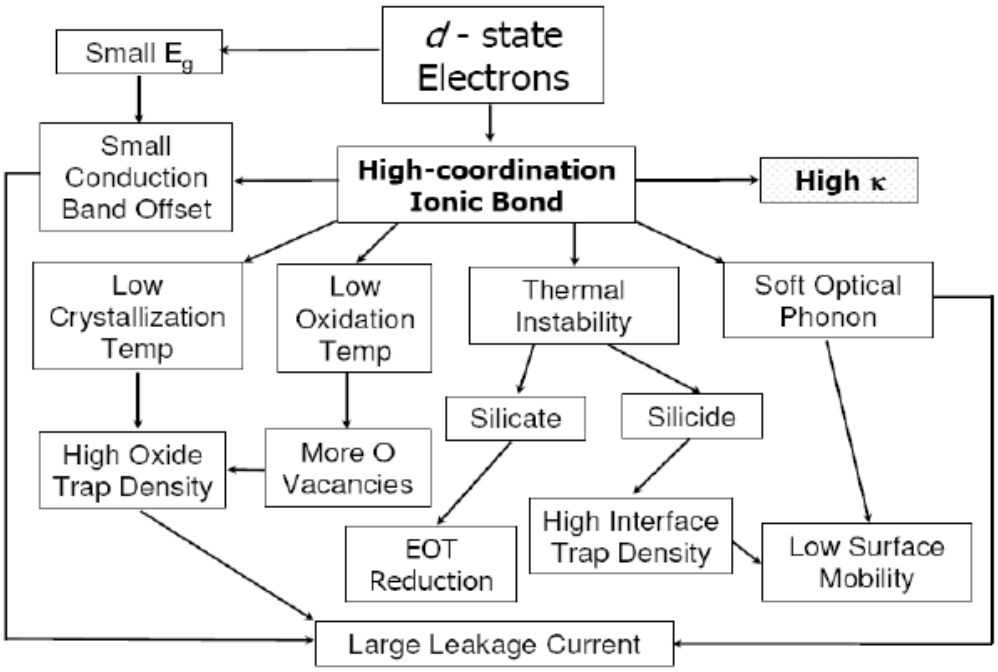


Fig. 3: Issues on high k metal oxides. The high dielectric constant of transition metal oxides comes from their ionic metal-oxygen bond constituted by their d-state electrons. Most of the disadvantages are also associated with this feature. [28]

1.4 Research Objectives and Scope

Based on the need for high-k dielectrics in future CMOS technology and the difficulty in integration, studies have to be done to understand the compatibility of high-k dielectrics with silicon substrate and its properties which may improve or degrade certain transistor performances.

1.4.1 Deposition of Thin Gate Dielectrics (<10nm)

As the material properties of lanthanide/rare earth oxides vary, it is important to understand its effect on MOS devices. Hence, studies are to be done by varying the rare earth oxide using cerium, gadolinium and neodymium oxides to study the physical properties and its influence on electrical performance. The purpose of

comparing these different materials is to better understand the performance of the lighter oxides which is deemed to have higher-k value such as that of lanthanum. The cerium oxide is deposited via pulsed laser deposition (PLD) due to precursor limitation whereas; neodymium oxide is studied using a dip-coating technique which is a simple and convenient method for initial research and development of the material. In addition, gadolinium oxide is also being studied due to its chemical and thermodynamic stability because of having a half-filled valence state. There are many contradictory studies on rare earth oxide due to the deposition technique and precursor used causing electrical performance to vary. Hence, this report is to establish a baseline electrical performance for the oxides using the deposition technique adopted in this study.

1.4.2 Study of passivation layer in nanolaminate form

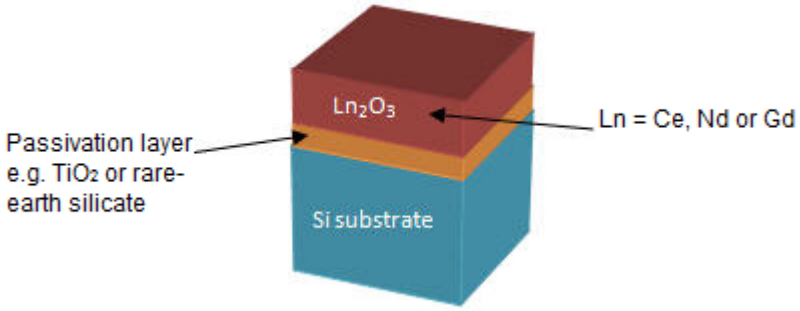


Fig. 4: Schematic of passivation layer in nanolaminate form

Due to large interface traps and undesirable Si-O interfacial layer formation that also limits the EOT [34], passivation layer is used to suppress the formation of interfacial layer. Hence, the purpose of this research is to study and eliminate the interfacial problems between high-k dielectrics with silicon substrate. Nanolaminate structures are to be studied using passivation layer of hafnium oxide, titanium oxide and gadolinium silicate that is deposited using atomic layer deposition (ALD) to form

conformal, uniform and smooth thin films prior to rare earth oxide deposition via pulsed laser deposition (PLD). Investigation is to be done on the film properties and traps within oxides and interface in order to better understand the interfacial issues and its influence towards electrical performance of transistors [1].

Rare earth silicate is chosen as an alternative passivation layer to integrate high-k into MOS devices by forming a complex with reduced k-value due to presence of Si atoms [8]. These silicate films can be deposited using silyl-amide complexes via atomic layer deposition. The films are to be studied for their physical properties and influence on electrical performance as well as traps generation. The study done in this report is to verify the effectiveness of this passivation layer and its effects on the electrical properties such as leakage current conduction mechanism.

1.4.3 Novelties

- Comparison of REOs (CeO_2, Nd_2O_3 and Gd_2O_3) due to thermodynamic stability, high-k values and lattice matching with Si but limited studies done to better understand the properties of film deposited – using various methods dip-coating and pulsed laser deposition
- Study of passivation layer to suppress the interfacial SiO_x layer by improving the overall capacitance and reduce interface traps
- Silicate (GdSiO) as passivation layer due to improved crystallization temperature and reduced hygroscopicity – transition layer between high-k oxide and Si without compromising the total dielectric constant; deposited using atomic layer deposition (ALD) using silyl-amide precursors with water
- Study of leakage current conduction mechanism is crucial for interfacial engineering as there are limited studies on bilayer gate dielectric stacks – to better understand the dominant mechanism in such structures which results

in local compositional and structural inhomogeneities and would substantially influence the conduction process

2. LITERATURE REVIEW

Many studies have been done on high-k dielectrics but there are still areas that require much attention in order to successfully implement high-k materials as gate oxides. Among the issues are the interfacial problems, selecting rare earth oxides and silicates for gate oxide as well as deposition techniques.

2.1 Processing Techniques/Deposition Methods of Gate Dielectrics

Various studies and reports have shown deposition of high-k dielectrics using diverse methods – generally classified into physical or chemical deposition. Some of the physical deposition methods reported are e-beam evaporation, sputtering and even pulsed laser deposition (PLD) [39]. These methods have the capability of depositing a large range of materials and are also relatively simple and clean [40]. The only drawback for these tools is that deposition is in line-of-sight and hence, films have limited uniformity and non-conformal over large areas [33] and with increased roughness. In addition, the deposition via PLD may also have 'splashing' effect – whereby large particles [33] are deposited onto the sample which may be detrimental for electronic applications.

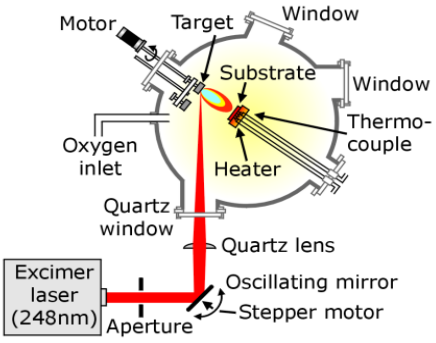


Fig. 5: Schematic diagram of PLD system [40]

As for chemical deposition techniques, those reported are chemical vapour deposition (CVD) and atomic layer deposition (ALD) [39]. Both methods utilize the

vapours of precursors to react and form films on silicon substrate. However, atomic layer deposition is a much improved version of CVD which uses alternating precursors and purging in between pulses to improve the quality of films. This sequential pulsing and purging enables self-limiting growth of films because sufficient precursor molecules satisfy the adsorption sites on the surface and excess/unreacted precursors are purged by inert gas [41].

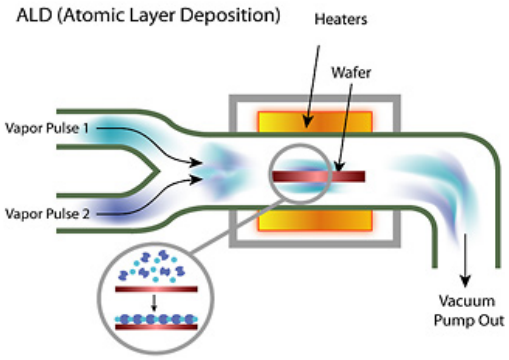


Fig. 6: Schematic diagram of ALD system [42]

Due to the self-limiting mechanism, ALD enables deposition of conformal and uniform films over large areas with simple thickness control as well as dense and pinhole-free films [41, 42]. In atomic layer deposition, in order for one cycle to complete, there are four steps to it as shown in Fig. 7. Firstly, the substrate surface is exposed to the first precursor and chemical absorption occurs. After that, an inert gas, usually nitrogen (N_2) is flowed into the chamber to remove the excess unreacted precursors. The second precursor is then introduced into the chamber to react with the initial absorbed species on the substrate. This forms a complete atomic layer deposition and finally, inert gas is being flowed in to remove the gaseous reaction by-products and unreacted precursors [39].

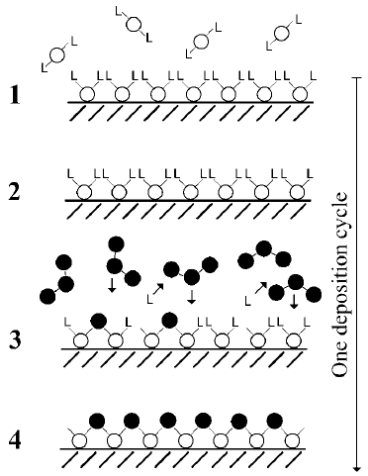


Fig. 7: Schematic illustration of an ALD growth cycle (1-4) leading to the formation of an imaginary binary oxide film of metal (o) and oxygen (•). L refers to the precursor ligand. [41]

As with CVD processes, there are also many key factors to be considered and optimized in atomic layer deposition (ALD) such as temperature. Suntola *et. al.*[43] has introduced the concept of 'ALD window' to indicate the temperature range whereby thin film growth follows the surface-control mechanism in ALD mode as shown in Fig. 8.

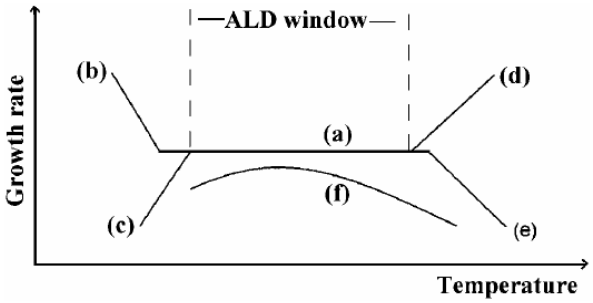


Fig. 8: Scheme of (a) an ALD processing window limited by (b) precursor condensation, (c) insufficient reactivity, (d) precursor decomposition and (e) precursor desorption. If the deposition rate is dependent on the number of available sites as in (f), actual ALD window cannot be observed. [41]

The ALD window describes that ALD growth only occurs within the (a) region. When temperature is too low, self-limiting mechanism is not observed either due to the condensation of gaseous precursors which forms island-like growth or there is insufficient reactivity between the precursors shown in (b) and (c), respectively. In the scenario where temperature is too high, precursors may decompose leading to uncontrolled growth or probably absorbed species on surface may desorbed leading to low growth rate as shown in (d) and (e).

Atomic Layer Deposition has its limitations as well such as being a slow process due to low deposition rates, difficulty in processing ternary or complicated compounds which requires constituent precursors to volatilize and react within common temperature (ALD window) because reactor temperature cannot be changed and precursor chemistry [41]. The slow process is no longer a critical issue in high-k oxide deposition because of the continuous scaling of the thin films. As for a good ALD precursor, there are several requirements to fulfil which includes sufficient volatility, no self-decomposition at deposition temperature, sufficient reactivity towards the other precursor and no etching of substrate or growing film. The widely used precursors for ALD growth include halides, β-diketonate complexes, metal alkoxides and organometallics such as alkylamide and cyclopentadienyl precursors [41]. Most studies on rare earth oxides deposited via ALD uses β-diketonate (thd-complexes) which are weakly reactive precursors, hence requires strong oxidizer such as ozone (O_3) [20]. Besides being detrimental to health and environment, ozone has been considered not well-suited for high-k oxide depositions due to interfacial oxide formation which increases the EOT value [44]. However, Park *et. al.* [45] showed that electrical properties of HfO_2 were improved by using O_3 instead of H_2O.

Alkylamide complexes are recently gaining attention and there are reports indicating that there has been successful deposition of rare earth oxide/silicate films using

volatile bis(trimethylsilyl)amide compounds [21]. Among the films demonstrated to have grown via ALD using this complex are lanthanum oxide (La_2O_3) using lanthanum tris[bis(trimethylsilyl)amide], $La[N(SiMe_3)_2]_3$ [27, 31] and praseodymium oxide (Pr_2O_3) [46, 47] using similar structure complex and H_2O. There are two methods for depositing rare earth silicate films using ALD. The first approach is by using Si-containing rare earth precursors whereas the other technique is by using a precursor for Si and another rare earth element precursor [48]. The former method is more appealing as it does not require Si precursors which are often delivered as flammable, toxic and explosive [48]. Lutetium silicate films were reportedly deposited by Scarel *et. al.* [48, 49], using synthesized tris[bis(trimethylsilyl)amide] lutetium which revealed the incorporation of Si in films. These silicate films showed wider band gaps and conduction band offsets which imply lower leakage current. In addition, the lutetium silicate films showed high crystallization temperature and high transverse optical (TO) mode frequencies, thus having moderate remote phonon scattering [48].

Dip-coating of Nd_2O_3 is a patented deposition [50] which demonstrates the use of inorganic nitrate precursors followed by a mild and sputter-free decomposition which enables the deposition of carbon-free Nd_2O_3 films. The deposition technique described in study offers many advantages such as simplicity in precursor synthesis and deposition, thermal stability of the precursor material, corrosive-free and large area deposition. As compared to other reports and techniques such as molecular beam epitaxy (MBE), pulsed laser deposition (PLD) and metal-organic chemical vapour deposition (MOCVD), all these have issues such as oxygen reaction with substrates, limited area uniformity and precursor availability and stability [51].

2.2 Interfacial Problems

Integration of high-k dielectrics in CMOS technology comes with several critical problems such as the growth of interfacial layer during deposition or heat treatments, fixed charges within high-k film and interface states and defects at interface/film [52, 53]. Most of the issues mentioned are due to the interface between high-k film and underlying silicon. Hence, many studies had been conducted to understand and rectify this problem. Majority of the high-k dielectrics studied have unstable interfaces with Si – reacting with silicon substrate under equilibrium conditions to form undesirable interfacial layer. As each dangling bond on silicon surface contains one electron, this gives rise to an interfacial two electron pair bond with an oxygen/nitrogen atom [54]. Since, most high-k materials are generally more ionic and highly coordinated on average than SiO_2, *heterovalent* interfaces are formed at high-k/Si interface with quantitative mismatch between bond and nuclear charge leading to interfacial traps and fixed charges [54].

Studies on interface engineering mainly focuses on preventing or at least minimizing the reaction of high-k films with underlying silicon [16], hence some reported the use of interfacial SiO_2 or silicon oxynitride (SiO_xN_y) layer (grown thermally) which also helps to minimize channel mobility degradation. However, the use of SiO_2 interfacial layer or materials with low k-value will limit the highest possible gate stack capacitance achievable [44, 54].

$$1/C_{tot} = 1/C_1 + 1/C_2 \quad (4)$$

As shown in Equation (4), C_1 and C_2 refer to high-k dielectric and interfacial layer respectively. Hence, if considering C_2 being SiO_2 interfacial layer, it is expected that the overall total capacitance will be lower than that of high-k dielectric film only. This will in turn limit the lowest achievable EOT as shown in Equation (5) where t_{SiO_2}, k_{ox}

are the thickness and dielectric constant of silicon oxide and $t_{high\text{-}k}$, $k_{high\text{-}k}$ are the thickness and dielectric constant of high-k dielectric, respectively [54].

$$EOT = t_{SiO_2} + (k_{ox} / k_{high\text{-}k}) t_{high\text{-}k} \quad (5)$$

Using SiO_2 layer has the benefit of maintaining high channel carrier mobility and reducing bulk charge and effective fixed charge effect which occurs at high-k/Si interface due to the unparalleled quality of SiO_2-Si interface. However, as we approach future CMOS technology, it is required that EOT ≤ 1nm which implies that SiO_2 layer has to be approximately 5Å. This extremely thin layer may cause deleterious effects because even at low applied voltages, a large amount of charge trapping may be induced by the sufficiently large electric field. Moreover, the thin interfacial layer will allow direct tunnelling of electron into the high-k dielectric [16].

Another proposed method is using yttrium oxide (Y_2O_3) as buffer layer which has been reported to suppress interfacial layer formation between silicon substrate and lanthanum oxide (La_2O_3) film [55]. The main aim of any potential high-k dielectrics is to achieve sufficiently high quality interface with Si, as close as possible to that of SiO_2 which has mid-gap interface state density, D_{it} of approximately $2x10^{10}$ states/cm^2 whereas papers reported high-k materials having D_{it} ~ 10^{11}-10^{12} states/cm^2 [16, 56]. There have also been reports stating that the growth of interfacial layer can be suppressed by low temperature long time annealing for dysprosium oxide (Dy_2O_3) on Si [57]. It is believed that for thinner films, there is lower number of charge traps expected [58]. Kim *et. al.* reported that surface passivation methods showed promising electrical results on Ge- and GaAs-based transistors [20]. In addition, high-k thin film with low lattice mismatch with silicon is desirable because it helps provide good interface properties.

One of the reasons for poor high-k/Si interface is due to bonding constraints. Lucovsky *et. al.* [59] has reported that if average number of bonds per atom, N_{av}>3, the interface defect density increases proportionally. Metal oxides with elements of high coordination (high N_{av}) form over-constrained interface whereas cations with low coordination causes under-constrained systems which also leads to high density of defects near interface [59].

Highly coordinated metals such as niobium, vanadium and manganese are not only over-constrained but also have several different stable oxidation states, which lead to oxygen vacancies and electron trap sites [59]. This is one of the main problems faced in early 70-80s whereby attempts to introduce high-k dielectrics were delayed due to high defect concentrations, particularly oxygen vacancies which resulted in charge trapping, transient threshold voltage shifts and carrier mobility degradation due to Coulombic scattering or remote phonon scattering [60, 61].

Generation of neutral electron traps is believed to cause gate oxide breakdown and many have tried to explain the mechanism by which these traps are generated. The two often cited models are anode hole injection (AHI) model and interfacial hydrogen release (HR) model [62]. Both models agree that tunnelling electrons upon entering the anode have excess kinetic energy to dissipate. AHI model describes that electron-hole pairs are generated from the tunnelling electrons in the silicon/polysilicon anode. Hence, the most energetic of the generated holes are injected into the oxide serving as precursors for neutral electron trap generation. This model explains the reason of time-to-breakdown, t_{BD} being polarity-dependent. For instance, the Fermi level in the anode of NMOS devices under negative bias lies within the valence band, hence more energetic holes can be generated as compared to positive bias [62].

Based on the HR model, at the Si-SiO_2 interface, tunnelling electrons break the Si=H bonds which releases hydrogen species that diffuse through the gate oxide and act as trap generation [62]. During channel hot carrier stressing, the breaking of Si=H bonds at interface is an important degradation mechanism, hence suggesting a correlation between the resistance of device towards gate oxide wear-out and hot carrier induced degradation. Therefore, the dangling bonds at Si-SiO_2 interface are usually passivated using hydrogen by forming gas anneal but studies have shown that deuterium (D) may be a better option as it is more difficult for the energetic electrons to break Si=D bonds than Si=H bonds [62]. Moreover, MOSFETs undergone deuterium annealing showed more resistance towards channel hot carrier induced degradation which implies that deuterium improves gate oxide reliability [62].

In order to adjust the dielectric and insulating properties of high-k dielectrics, studies have been done to vary the composition or sub-layer thickness of binary oxides in nanomixture structure (binary oxides mixed homogeneously) and nanolaminate (alternating sub-layers of binary oxides) [45].

Defect affects reliability of MOSFET devices and hence is one of the extensively studied areas for integration of high-k dielectrics due to the interface traps and oxide traps present. 'Oxide traps' are referred to as any defects in the high-k layer of device and 'interface traps' are defects that lies precisely at the high-k/Si interface [63]. Fleetwood *et. al.* has revised the defect nomenclature by separately defining 'fixed states' as defects that do not exchange charge with Si and 'switching states' as defects which exchange charge with Si. In addition, near interfacial oxide traps known as 'border traps' function as switching states during measurements. Hence, 'traps' are referred to as defect location and 'states' being reserved for discussion of

electrical response – e.g. more than one 'switching states' may be associated with a single physical trap [63]. Therefore, it is important to determine the number of oxide traps acting as switching states can be strongly related to time scale and bias conditions of measurements. For instance, an oxide trap interaction with underlying Si decreases exponentially when the distance of trap in high-k layer increase and hence, reducing the exchange charge between oxide traps and Si during high frequency measurements compared to low frequency [63]. Furthermore, an electron can easily enter a 'border trap' when surface potential is positive rather than negative and vice versa to due electrostatic reasons [63]. Hence, it is important to determine the problems associated with interfacial layer formed as electrical performance of MOS devices is highly dependent on interfacial characteristics and bulk properties of oxide [64].

2.3 Properties of Titanium Oxide (TiO_2) and Applications

As cited in most literatures, beyond 65 nm design rule, the conventional SiO_2 based materials cannot be used as gate dielectrics in CMOS devices as a result of its high leakage current due to direct tunnelling. Among the various materials proposed, HfO_2 and other rare earth based oxide materials offered promising advantages as high k gate dielectric films in the future CMOS devices. However, the interface between the high-k materials and Si is not perfect as compared to those of SiO_2/Si interface. Physical and electrical defects at the high-k material (HfO_2)/Si interface will lead to creation of undesirable electronic device performance [4-9].

Therefore, studies have shown that one major challenge in implementing high k gate dielectric in Si metal-oxide-semiconductor devices is the engineering of ultrathin interfacial layer (IL) between high k and Si substrate. It has been reported that a thin SiO_2 IL grown on Si before the formation of the high-k material (HfO_2) film will aid in

prevention of performance degradation resulted by the physical and electrical defects associated with the interface of high k and Si substrate [5]. Meanwhile decreasing or eliminating the overall thickness of the SiO_2 like lower-k IL is necessary to ensure the mentioned SiO_2 like IL will not dominate the overall gate capacitance because capacitances in series add in reciprocal fashion, thus the dielectric properties of the IL often dominate the characteristics of the entire gate stack, limiting the scaling benefits of incorporating the high k layer in the device [4, 6]. Therefore, the IL regardless of whether intentionally added or formed as a consequence of metal oxide (MO) deposition itself, can have a profound effect on the behaviour of the MO/IL/Si structure.

Recently, a promising result has been identified whereby thickness of the SiO_2-based IL between high k and Si substrate can be engineered using oxygen gettering metal over layers after deposition of a high k metal oxide film. The suggested approach makes use of the thermodynamic properties of reactive metals which can dissolve large amount of oxygen (>10 at. %) without forming a new oxide phase [6, 9]. It has been noticed that deposition of Ti layer on $HfO_2/SiO_2/Si$ and subsequently annealing at 300 °C would be an effective technique to control the thickness of the interfacial SiO_2 layer. Oxygen ions from the IL diffuse across the continuous high k dielectric layers (HfO_2) and dissolve into the Ti overlayer at temperature near 300 °C. On the other hand, Si atoms in the IL appear to be reincorporated in the surface of the Si substrate as the SiO_2 based IL decomposes [5]. Meanwhile, TiO_2 has also been known as high k dielectric material which exhibits a high dielectric constant 80 for the rutile crystalline phase. As mentioned in the research by Kim et al, the SiO_2 layer is reduced by 0.2 nm after deposition of the Ti overlayer and a further reduction was observed upon annealing at 330 °C where the amount of reduction depends on the thickness of the Ti overlayer. The research team had also discovered considerable oxygen

depletion up to approximately 50% in the HfO_2 layer after annealing with thicker Ti layers [6]. The kinetics of the process appears to be limited by the oxygen permeability of the metal oxide film [4].

Although Kim et al [5, 6], reported effective removal of the SiO_2 IL at 300 °C using a Ti overlayer, the chemical bonding structure and electrical properties associated with the high-k/Si interface after IL removal have not been studied in detail. Meanwhile in some reports, investigations had been carried out on the chemical bonding at the HfO_2/Si interface after the SiO_2 IL is gettered by a Ti metal overlayer. It was found that ultra thin SiO_2-like IL persists at the HfO_2/Si interface of Ti-electroded capacitors, but it is significantly thinner than the initial IL. In addition, removal of a part of SiO_2 IL by Ti overlayer does not promote the noticeable interfacial trap density.

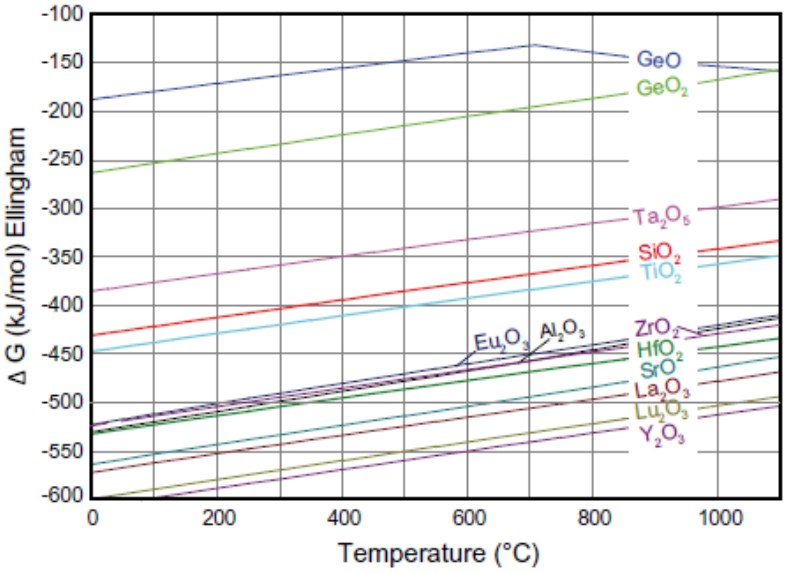


Fig. 9: Ellingham diagram of the Gibbs free energy of formation vs. temperature at 1013 hPa for several metal oxides in comparison to SiO2 and TiO2. Elements with their oxides at more negative level can reduce above lying oxides to elemental form under oxidation of the reactant. [8]

Ellingham diagram in Fig. 9 shows the oxides of several candidates – the oxidation of M to MO_x is highly likely to occur when the Gibbs free energy of formation in the

compound MO_x is lower than that of element AO_x which will be easily reduced. Al and Ti are possible options for EOT scavenging because both have the ability to reduce SiO_2 which forms oxygen vacancies in the high-k film. Below is a reaction showing the reduction of SiO_2 by Al:

$$2Al + 1.5SiO_2 \xrightarrow{\Delta G_f^{400\,^\circ C} = -282\ kJ} Al_2O_3 + 1.5Si$$

2.4 Rare Earth Oxides/Silicates as Gate Oxide

Many have found that group IVB metal oxides are potential candidates for gate oxide application. One of the most promising substitutes for gate oxide which had been extensively studied is hafnium oxide (HfO_2) as it fulfils the criteria of having high k-value (~20-25) as well as sufficiently wide band gap [65]. However, HfO_2 tends to crystallize at relatively low temperature (400°C) which induces leakage current through grain boundaries [38]. Another possible candidate is zirconium oxide (ZrO_2) but similarly has low crystallization temperature and high oxygen diffusion rate [66]. This in turn causes oxygen to diffuse through the dielectric and react with underlying silicon substrate which reduces the k-value effectively. With its high k-value (~80-110), titanium oxide (TiO_2) has also been found to be an attractive material selection for gate dielectrics. It is also proposed that Ti layer can act as oxygen getter to reduce or eliminate oxidation of Si substrate [44]. However, titanium appears in several oxidation states of Ti^{3+} and Ti^{4+} which poses problems such as reduced oxide whereby it acts as carrier traps and leakage paths due to oxygen vacancies formed [16]. In addition, TiO_2 crystallizes easily above 400°C as well [67].

Aluminium oxide (Al_2O_3) is also extensively studied as it is a very stable and robust material with favourable properties such as large band gap (~10eV), thermodynamic stability on Si and remains amorphous up to high temperatures [66]. Moreover, Al_2O_3 is a unique case whereby Al cations bond within the network (alternating Al-O

tetrahedra and octahedra) [67]. However, the only setback for Al_2O_3 is that its k-value is relatively low ~8-10 which is not a long-term solution in CMOS technology [66].

Hence, rare earth oxides are suggested for gate oxide in future CMOS technology. Rare earth oxides are known to meet the requirements of having high dielectric constant, thermodynamic stability with silicon and wide band gap with large conduction band offsets. However, they are also known for their hygroscopic properties which may cause changes to the film physically and electrically due to moisture absorption [55]. One of the proposed solutions is by using a passivation layer or coating with metal film [55]. In addition, it is also reported that Y_2O_3 and La_2O_3 are under-constrained hence it may form high defect densities at channel interface. This somehow contradicts with Kakushima *et. al.*[55] reports about using Y_2O_3 as buffer layer for interfacial layer suppression.

Generally, rare earth metals are very reactive with oxygen in ambient atmosphere; hence the most stable rare earth compounds are in the form of oxides [68]. Many efforts have been done in establishing the trend between structure and dielectric properties. It has been reported that dielectric constant is the sum of electronic and ionic contribution. The latter has a factor of 2-5 larger than that of electronic contribution and is caused by polarization formed by ionic displacements [69]. Based on Clausius-Mossotti equation reported by Park *et. al.* [70], shown below, it implies that the k-value will increase by decreasing the molar volume, $V_{m.}$

$$\varepsilon = \left(V_m + 2\alpha_D \frac{4\pi}{3}\right) \Big/ \left(V_m - \alpha_D \frac{4\pi}{3}\right) \tag{6}$$

Equation (6) provides a direct relationship between dielectric constant (ε), molecular dielectric polarizability (α_D) and molar volume (V_m) and is capable of predicting

dielectric constant only when the detailed crystal structures of the materials are clearly known in order to accurately estimate the molar volume [71].

Hence, Xue *et. al.*[71] presented another work which deals from the most fundamental parameters of constituent atoms of materials which is the corresponding atomic numbers for constituent atoms or ions. However, this method is only restricted to crystal series with uniform crystal symmetry.

$$\varepsilon = 1 + \left[\left(\sum N_i \alpha_i / \varepsilon_0 \right) \Big/ \left(1 - \sum \gamma N_i \alpha_i / \varepsilon_0 \right) \right] \tag{7}$$

In Equation (7), N_i is the number of atoms of species *i* per unit volume, ε_0 is the free-space permittivity and γ is the Lorentz factor. Equation (7) may be expressed simply as below as α_i is considered to be linearly related to atomic number (Z).

$$\varepsilon = (a - bZ_{\text{av}})^{-1} \qquad \text{or} \qquad \varepsilon = a' - b'Z_{\text{av}} \tag{8}$$

In Equation (8), *a* and *b* or *a'* and *b'*, respectively are constants for each group of solids whereas Z_{av} refers to the mean of the corresponding atomic numbers of constituent atoms. Based on Xue *et. al.* report, of all rare-earth compounds examined, the values of dielectric constant decrease with increasing atomic number (lanthanum to lutetium) [71]. Moreover, it is also shown that the atomic radius and molar volume also decrease with increasing atomic number. Hence, in all these compounds studied, decrease in ion polarizability due to reduced molar volume may be due to increasing bond strength for electrons responsible for polarizability [71]. The findings reported are found to be in contrast with that of the assumptions made by Park *et. al.*[70] whereby increase in k-value was by reducing molar volume.

Though there is contrast between both reports, there is also similar factor which both papers have considered which is the volume occupied per molecule (V_m). Hence, it is considered that the material structure whether amorphous or crystalline

geometries in different arrangement may have significant influence [72, 73]. Conversely, Päiväsaari *et. al.* demonstrated that the lanthanide oxide films does not follow the reported trend of k-value decreasing from La_2O_3 to Lu_2O_3 [74]. In addition, the reaction between rare earth metal and silicon at interface increases with increasing ionic radius of rare earth element. This may lead to unavoidable interfacial layer formation for elements with large ion radius such as La^{3+} (0.117nm) as compared to Y^{3+} (0.104nm) which is reported to suppress interface reaction [75, 76].

High-k oxides are to remain amorphous and attempts have been made to maintain dielectrics in the phase especially after post-deposition annealing to avoid increase in surface roughness and leakage due to grain boundaries formation [54]. Most of the known high-k materials are highly ionic and according to general trends, dielectric constant increases with ionic character whereas crystallization temperature decreases. Hence, suggestions to reduce ionicity include alloying the metal oxides with aluminium or silicon in order to increase crystallization temperature [35, 54].

It has been reported that by adding the minimum necessary SiO_2 into high-k films, forming a multi-component dielectric silicate which is able to stabilize the amorphous phase of dielectrics and having the desired interface characteristics which may lead to low fixed charge [66]. With moderate dielectric constants (~10-14) and superior leakage properties (4-5 orders of magnitude reduction) as compared to conventional SiO_2 with the same EOT, rare earth silicates are potential gate dielectrics [75]. Silicate films can be formed by various methods such as oxidation of silicides obtained by metal deposition, e-beam evaporation of mixtures of SiO_2 and rare earth oxides and deposition of rare earth oxides on SiO_2 with subsequent heating [75, 77]. With high crystallization temperature, silicates tend to remain amorphous and are advantageous in reducing leakage currents along grain boundaries [78]. Furthermore, silicate films are stable against Si diffusion but oxygen may diffuse through them [77]. However, due to the presence of SiO_2 which has low

k-value, the dielectric constant of the silicates will also be reduced leading to scalability challenge [66].

Reports by Manchanda *et. al.*[66] demonstrated that for doped aluminium oxide films using zirconium or silicon, 0.5-5 wt.%, the leakage current and mid-gap interface-trap density have been reduced. It is believed that dopants function as network modifiers that help quench the dangling bonds of excess oxygen in aluminium or metal oxides, thus the conduction current and interface state density are reduced. In addition, the network modifiers also help to stabilize the amorphous phase of metal oxides [66].

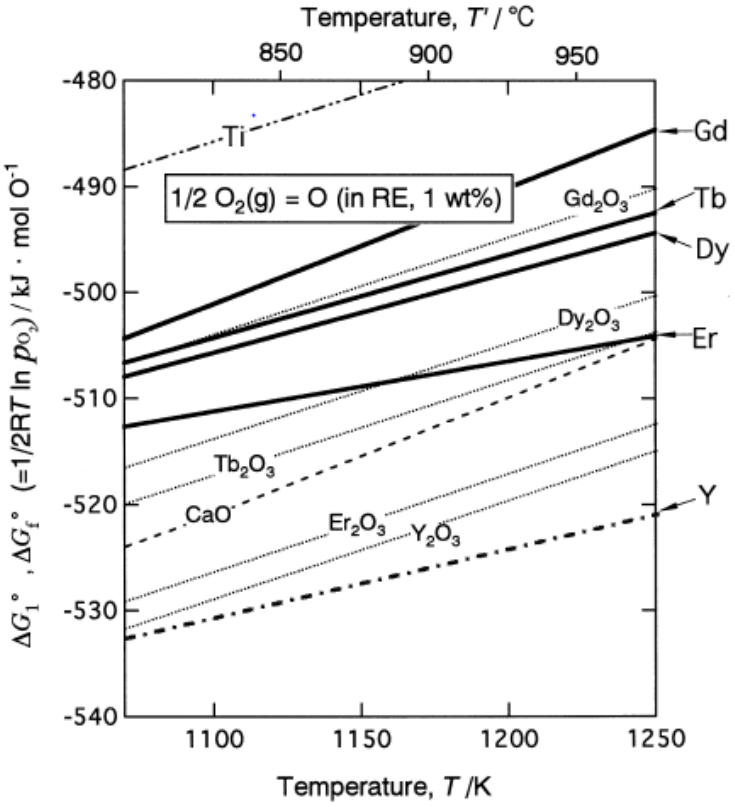


Fig. 10: Temperature dependence of the standard Gibbs energy change for oxygen dissolution, ΔG_1, in rare earth metals obtained in this study. The standard Gibbs energy of formation of selected oxides, ΔG°_{f}, are also shown for comparison. [9]

Fig. 10 indicates that the oxygen affinity of the metals decreases in the order Y>Er>Dy>Tb>Gd>Ti. Gibbs free energy dissolution of oxygen is lower with increasing atomic number for rare earth metals [9]. Hence, rare earth metals seemed to be better alternatives to reduce SiO_2 and prevent interfacial layer formation.

2.5 Bilayer Structure of Gate Oxides for Electronics Applications

Numerous attempts had been focusing on providing an oxide thickness similar to that of a very thin SiO_2 layer according to Moore's law requirement; sputtered and CVD deposited high k oxide gate materials suffer from the formation of low-k interfacial layers. The low k interfacial layer, in turn will reduce the overall capacitance of the dielectric stack due to series capacitor effects. Hence, there remains a critical need for improved scaling techniques by which high k dielectric materials can be employed in formation of gate dielectric layers while mitigating or preventing the adverse effects of low k interfacial layers [7, 10-13].

Inventions related to the modification in the design of gate dielectric structures for MOSFET devices had been intensively studied. One aspect of the invention involves using bilayer gate dielectric stack structures, where a first layer in the stack comprises of a nitride layer deposited over the substrate. Some common examples of nitrides which been employed are hafnium silicon nitride, zirconium silicon nitride, hafnium nitride, and zirconium nitride. An oxide layer is then deposited over the nitride layer, which can be of any high k material, such as tantalum pentoxide, titanium dioxide, hafnium oxide, zirconium oxide, aluminium oxide, hafnium silicon oxide, zirconium aluminium oxide, rare earth oxide and others. Researchers had discovered that this method can be used to eliminate or reduce the formation of a low k interfacial oxide layer significantly due to the absence or reduced presence of reactive oxygen during the initial nitride layer deposition process [7, 10-13]. Hence, the invention enables

gate dielectric stack formation without low k interfacial layer formation found in conventional dielectric stacks. Alternatively or in combination, the nitride layer thickness may be adjusted relative to that of the oxide layer so as to permit a reduced oxidation of the underlying Si substrate relative to the conventional case whereby no nitride layer been created. This technique will ensure that the initial layers in the stack comprise a controllable amount of silicon dioxide, to mitigate or prevent mobility degradations associated with metal at the interface.

Meanwhile, research had also been conducted to investigate ways in improving the permittivity of some high k dielectric materials such as ZrO_2 through the fabrication of binary oxides such as ZrO_2-TiO_2 composite films [79-81]. The addition of TiO_2 can improve the crystallization temperature, while the nanolaminate structure can tailor the electrical properties of the dielectric stacks which further improve applications in areas such as storage capacitors, non volatile memories and transparent thin film transistors. On the other hand, Ti has been known as oxygen getter which could limit the formation of the SiO_2 to a suitable thickness which will improve high k dielectric materials compatibility with the Si interface and to prevent low-k interfacial layer (SiO_2) dominating the capacitance in series [6, 82].

Another ongoing studies on bilayer structures of gate oxide involved using Al_2O_3-HfO_2 laminated layer as the gate dielectric for GAN based devices. Owning to its high dielectric constant (20-25), HfO_2 has been well received as the promising high k dielectric material for current devices [83]. However, it tends to change from the amorphous to the polycrystalline state at 500 °C, which will increase the grain boundary leakage and lead to thermal stability concerns for the devices. On the contrary, Al_2O_3 which has a lower dielectric constant (9), has a larger band gap (8.8 eV) and better thermal stability (will remain amorphous even up to 1000 °C) and

display ideal passivation effect on GaN. In order to enjoy the collective advantages of both dielectrics, they had been interposed on each other through pulsed laser deposition (PLD) technique and their effectiveness as a gate insulator as well as a surface passivation layer been clearly demonstrated by Park et al. and Yue et al [24, 79, 84-87].

In summary, attractive topics generated among introduction of suitable bilayer dielectrics materials centralized on the purpose of interfacial engineering [22-25]. The general objectives of these mentioned reports aim to improve the interface quality through various surface treatments (NH_3 and O_3 treatments) [24, 84-88]. As suggested by most literatures, NH_3 surface treatment will be favoured instead of O_3 treatment as aggressive scaling requires prevention of further interface layer growth and achieving higher dielectric constant of the interface layer.

3. EXPERIMENTAL PROCEDURES

The samples were cleaned and prepared prior to deposition either by pulsed laser deposition (PLD) or atomic layer deposition (ALD). Procedures of preparation and deposition (Fig. 10) as well as the synthesis of precursor are discussed in this section.

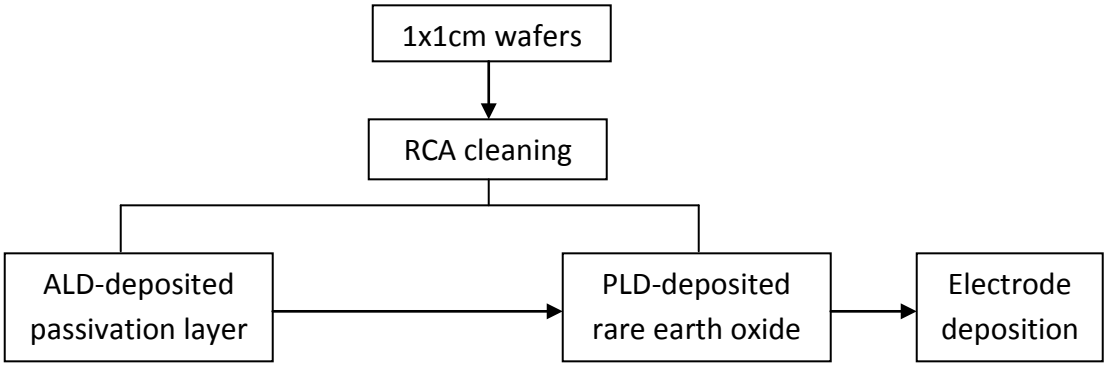


Fig. 11: Schematic of experimental procedure

3.1 Sample Preparation

Silicon wafers that are boron-doped were being cut into 1x1cm samples prior to RCA cleaning. SC1 solution of deionized water, ammonium hydroxide (NH_4OH) and hydrogen peroxide (H_2O_2) with ratio 5:1:1 is being prepared and heated to 80°C. The cut samples were being soaked in SC1 solution for 5min. After that, the samples were removed and transferred to SC2 solution comprising of deionized water, hydrochloric acid (HCl) and hydrogen peroxide (H_2O_2) with ratio 6:1:1 that was being heated to 80°C for another 5mins. The samples were then being dipped in diluted hydrofluoric (HF) acid for 15sec. The first step is a process to remove organic contaminants followed by SC2 being used to eliminate ionic contamination. The HF dip is also known as oxide strip whereby thin native oxide that is formed on silicon is being removed. As shown in Fig. 12 below, the Si *2p* peaks based on XPS data confirmed that the native oxide on Si substrate had been removed after cleaning.

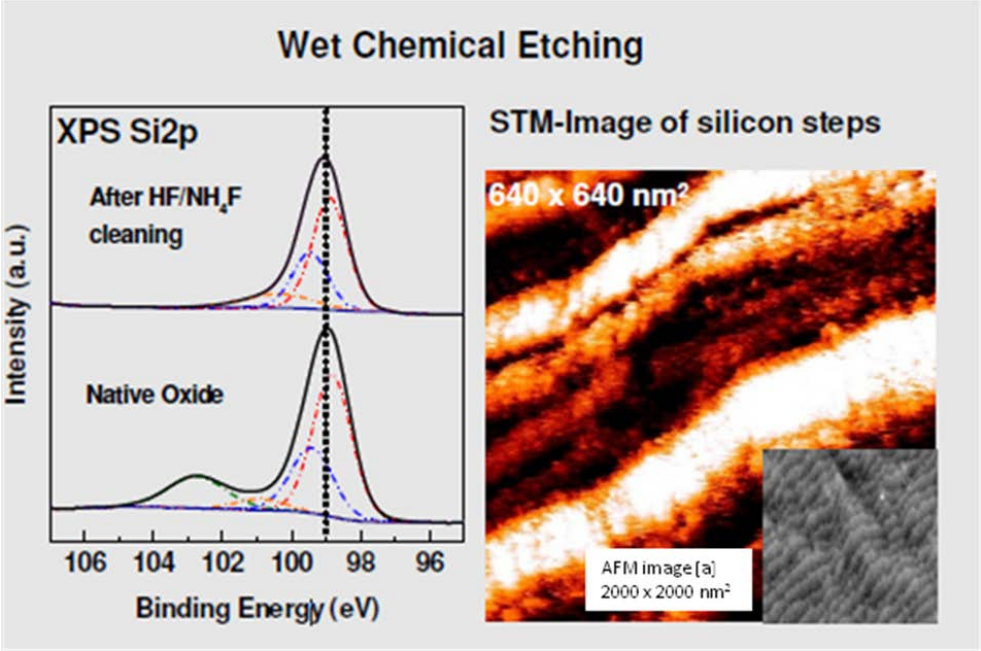


Fig 12: XPS result pre and post RCA clean [89]

3.2 Oxide Deposition

3.2.1 Passivation Layer

Prior to the high-k deposition, a thin passivation layer of titanium oxide (TiO_2) or gadolinium silicate (GdSiO) of 2-3nm was deposited by atomic layer deposition (ALD). The precursor and water were being pulsed separately into the reaction chamber which was heated to 100°C with nitrogen purge in between. This passivation layer acts as an interfacial layer to suppress SiO_2 interfacial layer formation and improve EOT value because TiO_2 has a dielectric constant of approximately 80-100 whereas GdSiO is known to have higher k-value than SiO_2 as well as better interface compatibility. In addition, the TiO_2 layer deposited via ALD is hoped to improve interface quality between high-k and underlying silicon.

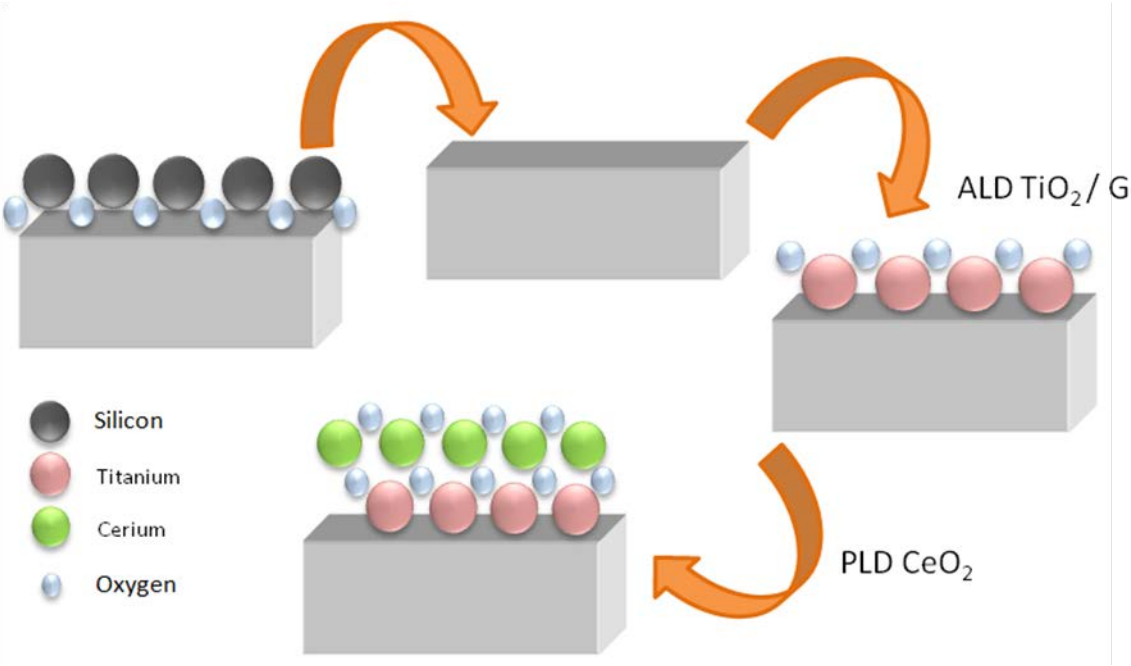


Fig. 13: Schematic of the process flow for the bilayer gate stack deposition

3.2.2 Gate Oxide Film

The rare earth oxide layer of cerium oxide and gadolinium oxide were being deposited onto the silicon samples using pulsed laser deposition (PLD). These samples are to establish the standards of rare earth oxides deposited using PLD under certain conditions. Prior to pulsed laser deposition, rare earth targets had to be formed using the 2.5cm die with rare earth oxide powders. The rare earth oxide powders such as CeO_2 and Gd_2O_3 were filled into the die and then compressed using hydraulic press for 15-20 min. The targets were then sintered in a furnace with continuous nitrogen flow at 1100°C for 10 hours.

For lanthanide oxide film of neodymium oxide deposited via dip-coating, the samples are dipped into $Nd(NO_3)_3 \bullet 6H_2O$ in $CH_3(CH_2)_3OH$ solution of 0.005 M concentration after RCA cleaning. The decomposition of the nitrate to form oxide and removal of

the residual solvent are done in the furnace at 600 °C which is below H-Si decomposition, under argon ambient conditions.

Samples deposited then undergo rapid thermal annealing (RTA) at 400°C, 600°C and 800°C for 1 min each, respectively.

3.3 Electrode Deposition

The samples are then being sputtered with either platinum or gold to form the top and back electrodes. The top electrodes are of 0.3mm in diameter hence having an area of approximately 0.07mm^2.

3.4 Nano-Structural and Physical Characterization

The samples deposited with or without passivation layer are then being characterized both physically and electrically using various techniques.

Through physical characterization, data of the film morphology, thickness, roughness and structure can be determined.

Atomic Force Microscopy (AFM) is used to measure the surface roughness of the deposited films. It is reported that with every 0.1nm increase in root-mean-square, the leakage current through 1nm-thick oxide increases by a factor of 10.

Thin Film X-Ray Diffraction (XRD) helps determine the phase (crystalline or amorphous) of the films. It is important to ensure that the film remains amorphous even after annealing because grain boundaries in crystalline films act as leakage paths for current to flow through.

X-Ray Photoelectron Spectroscopy (XPS) is used to determine elemental composition of film, contamination on sample surface as well as electronic state of each element.

This is to ensure the composition of the film and determine if there is any contamination or inter-mixing between film and substrate.

Rutherford Backscattering Spectrometry (RBS) is capable of characterizing structure and composition of materials as well as thickness of film. This technique helps determine if there is any interfacial layer form as well as determining the stoichiometry of the film.

Transmission Electron Microscopy (TEM) helps capture the fine details of the film as well as elemental analysis through energy dispersive x-ray spectroscopy (EDX). It is important to capture the image of the film to accurately determine film thickness as well as to observe the interfacial roughness and defects.

3.5 Electrical Performance Characterization

The results from electrical characterization provides information of the device performance such as dielectric constant value, leakage current and interface density of states/defects (D_{it}).

3.5.1 *Capacitance – Voltage (C-V) Measurements*

By using Keithley 4200 Semiconductor Parameter Analyzer, profiling of capacitance-voltage can be achieved. This method uses the technique of creating a depletion region (region that is empty of conducting electrons and holes but may contain ionized donors and electrically active defects or traps) using a metal-semiconductor junction, p-n junction or a MOSFET [90]. This depletion region acts as a capacitor with ionized charges within it and by changing the voltage applied; the depletion width can be varied.

Measurements are done in DC mode to derive the C-V profile which is crucial in determining gate oxide dielectric constant value. The capacitance observed in

accumulation is used to calculate the k-value of high-k dielectric used. This is an important parameter to determine the model device performance and capability. The capacitance-voltage measurement varies with frequency due to the dielectric polarization whereby upon applying bias, the charges within dielectric are displaced and shifted instead of flowing through the material [90].

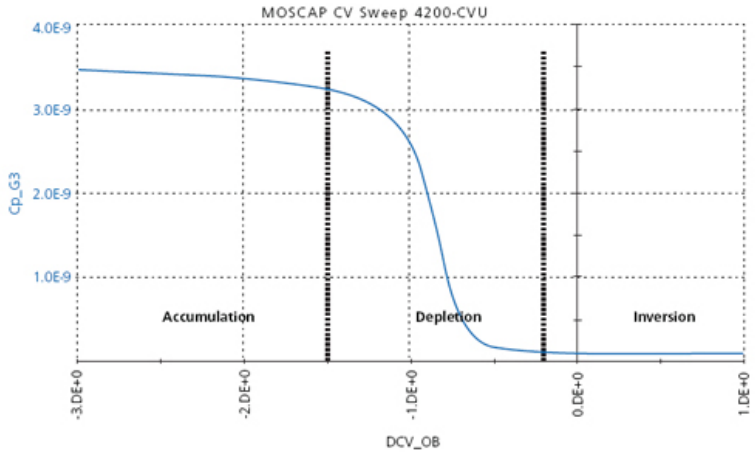


Fig. 14: C-V profile at high frequency of p-type MOS [90]

Based on Fig. 14, at accumulation region, when negative bias is applied, majority of the holes (carriers) are attracted towards the gate and hence accumulating these holes at substrate-oxide interface [90]. Capacitance is essentially constant and 'flat' at accumulation when voltage applied is sufficiently negative. However, for thin oxides does not saturate to a plateau hence the capacitance measured differs from true oxide capacitance. Another problem with C-V measurement is that in the case of leaky devices, capacitive impedance is being overwhelmed by resistive impedance causing the C value to be lost in the noise. Therefore, in ultrathin oxides, the leakage may increase and quickly degrade the accuracy of capacitance measurement. However, measurements at higher frequencies may solve this issue resulting capacitance current is higher and more easily measured [90].

As bias voltage increases (move towards positive bias), carriers (holes) are being repelled from oxide interface hence, a carrier-depleted area forms beneath oxide, creating an insulator (depletion region) [90].

An inversion region forms when the applied gate voltage increases beyond the threshold voltage whereby the minority carriers (electron) are attracted towards the gate and accumulate at the oxide interface creating an inversion layer due to inverted carrier polarity. High frequency analyzer measures both oxide capacitance and depletion capacitance and during inversion, electron-hole pair generation cannot keep up with high frequency measurement hence, when depletion region reaches a maximum depth, the capacitance measured is still based on majority carrier position and distribution [90].

3.5.2 *Leakage Current – Voltage (I-V) Measurements*

The leakage current-voltage profile (Fig. 15) can also be obtained from Keithley 4200 Analyzer. One of the critical issues in gate oxide scaling is the leakage current due to electron tunnelling through dielectric causing large power consumption and eventually breakdown of the gate oxide [90]. Considering that conventional SiO_2 leakage current increases exponentially with reducing thickness – at 1V, SiO_2 thickness of 3.5nm has leakage current of $10^{-12}A/cm^2$ and increases to $10A/cm^2$ at 1.5nm thickness [91]. The reported acceptable gate leakage for 22nm node for low standby power operation with oxide EOT ~5Å at 1V is of about $10^{-2}A/cm^2$ [72]. Hence, using the analyzer, bias is applied and swept across to determine the amount of current that leaks through the gate dielectric.

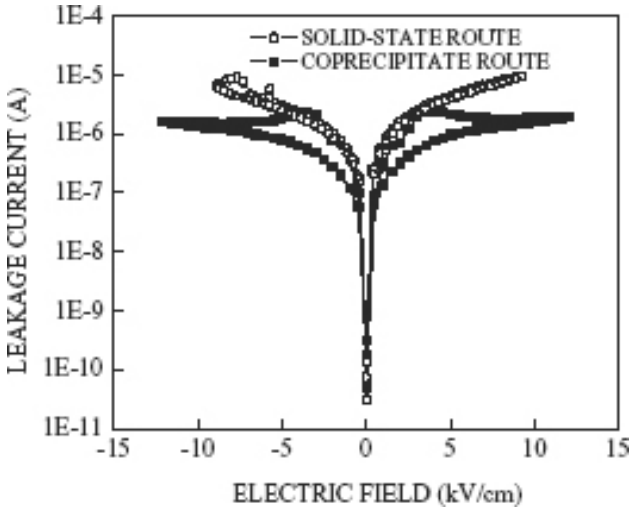


Fig. 15: Example of I-V curve [48]

3.5.3 *Interface Defects/Traps*

Interface traps and density of states (D_{it}) were reportedly derived from two commonly known methods. One of the methods is charge pumping (CP) which is widely used to study interface traps for more than 30 years [92]. During CP measurements, source and drain are usually grounded or have a small reverse bias applied. Pulses are applied to the gate periodically to drive channel region into inversion and accumulation conditions cyclically. The measured DC charge pumping current from substrate is recognized as recombination of trapped electrons and holes [93]. The DC charge pumping current reaches its maximum ($I_{CP, MAX}$) at a certain pulse base voltage (V_{base}) when pulse amplitude (V_a) is kept constant and V_{base} is swept from flatband voltage (V_{FB}) to threshold voltage (V_{th}) or vice versa. $I_{CP, MAX}$ is expressed as

$$I_{CP,\ MAX} = q\ f\ A_G\ N_{it} \quad (9)$$

where q is electron charge, f being frequency of applied pulses, A_G is the effective channel area and N_{it} represents the area density of traps within the detectable energy and spatial ranges for a given CP measurement condition. Though,

information of spatial and energy distribution of traps can easily be derived from CP measurements, there is a limiting factor to it which is its inability to conduct measurements on MOS devices due to lack of source and drain region [92, 93].

The other technique used was known as conductance method [94]. The interface traps are calculated based on a single high frequency capacitance-voltage profile and corresponding conductance-voltage measurement. Since 1959, several approaches have been employed to determine interface state densities which include capacitance measurements methods and conductance measurements that are more accurate. By analyzing the changes in recombination statistics caused by time-dependent changes in Fermi-Dirac statistics, the conductance behaviour can be derived. From the conductance-voltage (G-V) plot, approximate maximum density of surface states can be determine from maximum value of measured conductance (G_m/ω) [94].

4. DEPOSITION OF THIN GATE DIELECTRICS (<10NM)

4.1 Introduction

Based on the described literature review, rare earth oxides in the lanthanide series demonstrate different physical and electrical properties due to factors such as the valence states and atomic size/structure. Furthermore, the various deposition techniques adopted will have a certain degree of impact towards the film properties as well, due to the stoichiometry, density, conformality and uniformity of the film.

In this chapter, the main concept of study is to study and investigate the different lanthanide oxides as well as the technique used in depositing the films. Cerium oxide (CeO_2) and gadolinium oxide (Gd_2O_3) is formed via pulsed laser deposition due to the availability of such oxide targets. On the other hand, neodymium oxide is deposited using a dip-coating technique which is a simple method that enables preliminary studies of film to be done with reduced cost and time.

4.2 Experimental Details

As described in Chapter 3, these rare earth oxides are either deposited via pulsed laser deposition (PLD) or dip-coating technique. Prior to deposition, the Si substrates are cleaned using the standard RCA cleaning procedure and dipped in diluted HF to remove any native oxide that is present.

Films deposited are then annealed at varying temperatures and then top electrodes are sputtered onto the films using a 99.999% gold target to form the contact.

4.3 Results and Discussion

In order to investigate the properties and characteristics of lanthanide oxide films which are of high research interests owning to vital criteria such as high-k and ideal stability as cited in literatures; cerium oxide (CeO_2), neodymium oxide (Nd_2O_3) and

gadolinium oxide (Gd_2O_3) were chosen. The 10nm thin films are deposited via PLD for CeO_2 and Gd_2O_3 due to it being a simple process and capability of depositing a large range of materials. The Nd_2O_3 film is deposited on Si substrate using dip-coating which is a clean and simple process. Both the PLD and dip-coating are chosen deposition processes as it is suitable for research and preliminary studies purposes. Physical and electrical characterizations are done on the samples to analyze their structure, composition and electrical performance.

4.3.1 Physical Characterization

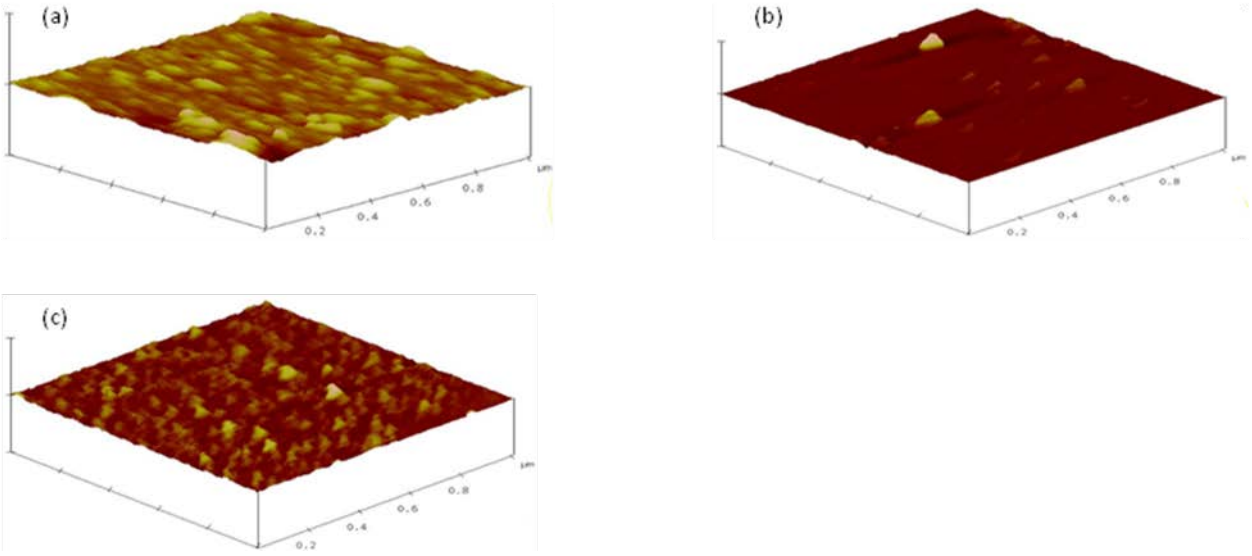


Fig. 16: 1µm x 1µm scan of post annealing at 600°C for (a) CeO_2 RMS~0.75nm; (b) Gd_2O_3 RMS~0.66nm; (c) Nd_2O_3 RMS~0.68nm

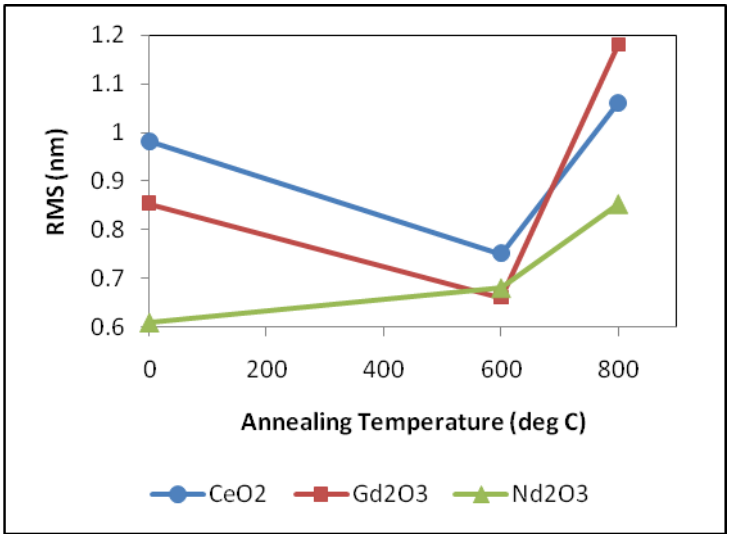


Fig. 17: Plot of roughness (RMS) vs. annealing temperature for CeO_2, Gd_2O_3 and Nd_2O_3

Based on the Atomic Force Microscopy (AFM) scan on the specimens, both CeO_2 and Gd_2O_3 samples annealed at 600°C has reduced roughness which is due to rapid thermal annealing (RTA) in nitrogen ambient helping to densify the film and reducing defects [95] as observed in Fig. 17. As-deposited PLD films is rougher due to PLD 'splashing' effect (large particles deposited) which seems to have reduced upon annealing at 600°C attributed to reduced defects and densification of the films upon RTA. Areas with these 'splashing' or particles [33] create sudden step heights and roughness which could be detrimental to device performance. However, annealing demonstrates that the film is densified and able to resolve the 'splashing' issues as long as the temperature does not cause film to crystallize. As for dip-coated Nd_2O_3 sample, the roughness is lower as compared to PLD samples and upon annealing at 600°C, roughness is still comparable to as-deposited samples. However, when further annealing of up to 800°C is performed, the films appear to have increased roughness. This is due to formation of grains as it appears that Gd_2O_3 has significant increase in roughness and it has been reported to have lower crystallization temperature due to higher lattice energy [96] compared to Nd_2O_3 and CeO_2.

Roughness is a fundamental characteristic that has to be considered during dielectrics integration. It is reported that with every 0.1nm increase in root-mean-square, the leakage current through a 1nm-thick oxide increases by approximately a factor of 10 [97]. Hence, the interface roughness must be controlled at atomic scale to enable the integration of thin oxides. Samples annealed at 600°C showed promising results as the roughness is lower or comparable to that of as-deposited substrates.

X-ray photoelectron spectroscopy was utilized to characterize as deposited CeO_2 films. The Ce 3*d* spectrum is analyzed and compared to that reported in literature [98].

Table 2: Comparison between typical binding energies for CeO_2 films [99] and experimental results

Peak	Binding energy (eV)	
	Literature	Experiment
Ce $3d_{5/2}$ principal	881.2	882.6
Ce $3d_{3/2}$ principal	899.5	898.6
Satellite 2	902.5	901.0
Satellite 3	915.8	916.8
C 1*s*	284.7	284.0

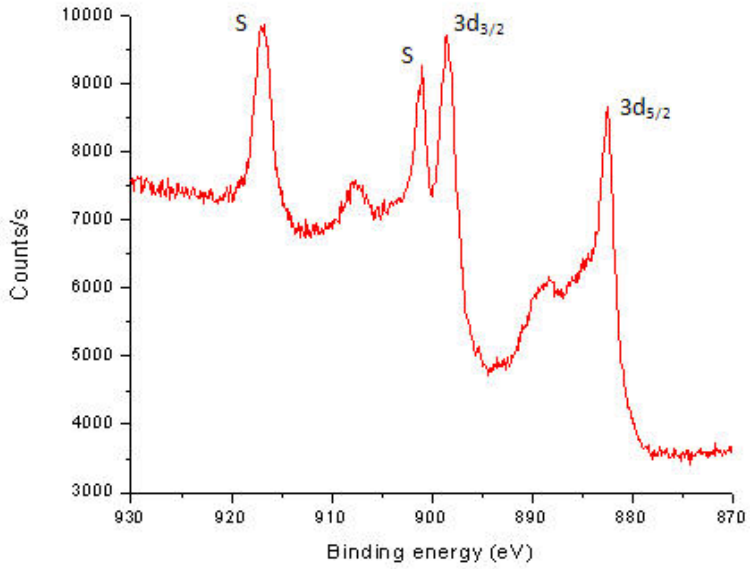


Fig. 18: XPS spectrum of Ce 3*d* of as-deposited CeO_2 sample

The XPS spectrum of deposited CeO_2 samples conforms to the results indicated in literature, indicating the presence of cerium oxide thin film on silicon substrate. However, there are slight deviations such as the $3d_{5/2}$ peak (Fig. 18) was found to be at 882.6eV which differs from value given in Table 2. This implies that the film is oxygen deficient as the value is closer to that of pure Ce having $3d_{5/2}$ peak at approximately 883.9eV [98]. The result suggests that there is interaction between the oxide film and underlying Si which may have created some oxygen vacancies by diffusing to the interface to form undesired interfacial layer oxide. The $3d_{3/2}$ peak is at 898.6eV, hence having the spin-orbit splitting of 14.7eV. The satellite line (S) at 901.0eV can be attributed as 'shake down' satellites whereas the line at 916.8eV is due to cerium (IV) impurity in sample which is also reported by Sundaram *et. al.*[98]

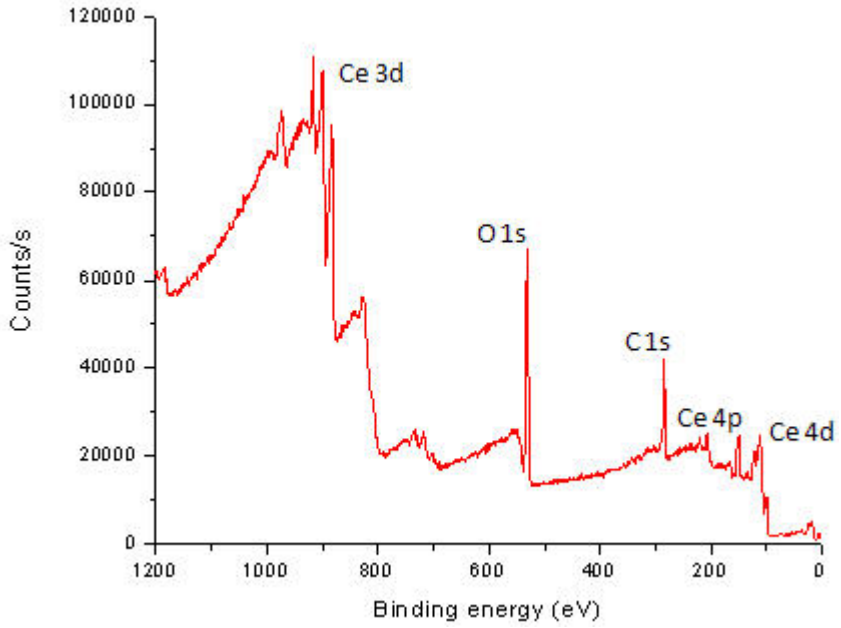


Fig. 19: XPS spectrum of as-deposited CeO_2 on silicon substrate

The appearance of C 1s at 284.0eV in Fig. 19 is likely an artefact due to exposure to ambient atmosphere [99].

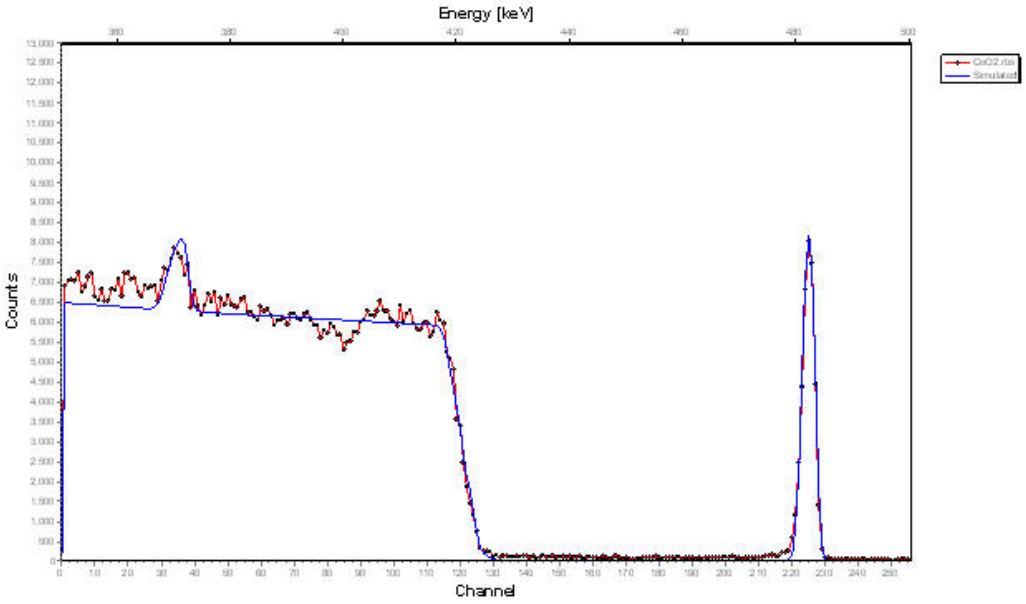


Fig. 20: RBS spectrum of as-deposited CeO_2 sample

Based on the RBS characterization (Fig. 20), the thickness of CeO_2 is approximately 3nm. The data indicates that the film is not pure CeO_2 and contains silicon within based on SIMNRA simulation. As it is known that Ce has oxidation states of +3 and +4 [68], hence intermediate phases may appear and the non-stoichiometric film is found to be due to loss of oxygen from normal oxygen sites. These oxygen vacancies act as trapping sites for electrons released at the time the oxide ion leaves [92]. This agrees well with the shift in $3d_{5/2}$ peak observed in XPS spectrum. A thin non-stoichiometric Si-O layer (~2nm thick) is found at interface which supports the expected interaction between the oxide film and underlying Si as shown in the mismatch of simulated and raw data in Fig. 20.

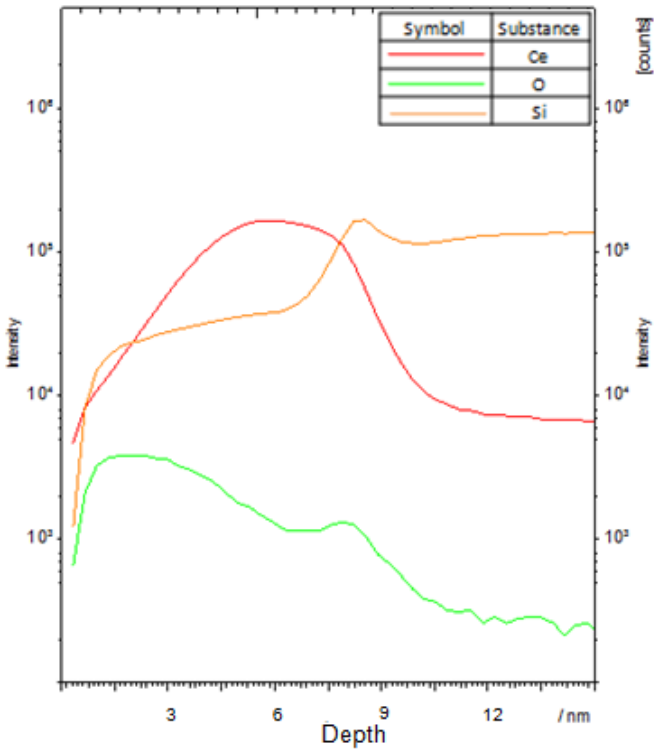


Fig. 21: TOF-SIMS data of CeO_2 on Si substrate

TOF-SIMS result as shown in Fig. 21 also coincides with the XPS and RBS findings, due to observable O peak at CeO_2/Si interface. This interfacial layer oxide is caused by

CeO_2 being an ionic compound and having weak chemical bonds with ions, thus leading to large amount of oxygen vacancies [100].

Due to the varying properties of lanthanide materials, it is important to study the physical properties and its effect on the electrical performance. This section compares the characteristics of dip-coated Nd_2O_3 with Gd_2O_3 and CeO_2 deposited via PLD; as these lanthanides have different intrinsic properties (atomic weight and ionic radius). This study is to determine the physical properties and electrical performance between the oxides. The samples are characterized both physically and electrically to analyze their structure, composition and performance.

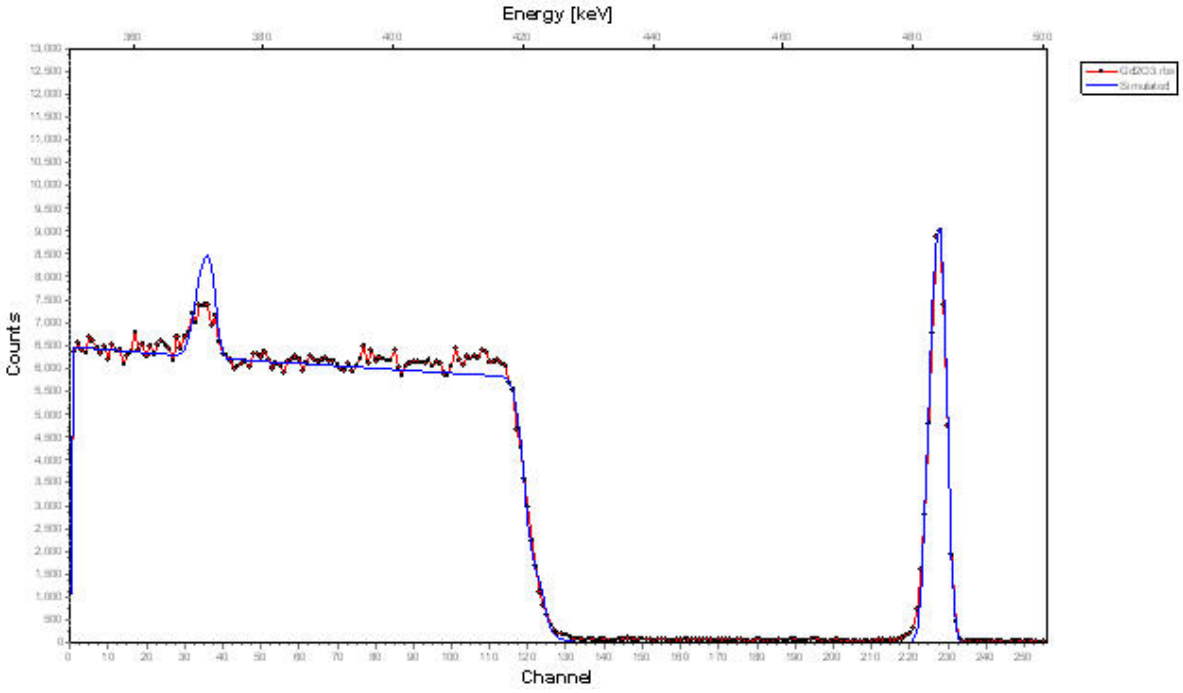


Fig. 22: RBS spectrum of as-deposited Gd_2O_3 film

The RBS spectrum (Fig. 22) shows that the gadolinium oxide film also contain traces of silicon which is due to the interaction between Gd_2O_3 with silicon substrate at interface. It is also found that a thin non-stoichiometric silicon oxide film is formed at

interface with thickness approximately 1nm. It is predicted that Gd_2O_3 would less likely form interfacial oxide due to its intrinsic high energy 5d shell which only allows one electron to occupy and the oxidation state of +3 only. Hence, less likely to form mixed oxide stoichiometries and limits interfacial traps [101].

However, the RBS data based on this study contradicts from theory as a thin undesirable interfacial layer had formed between Gd_2O_3/Si substrate.

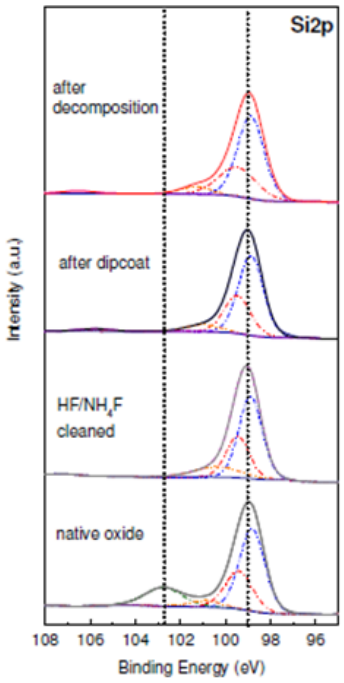


Fig. 23: XPS data of Si 2p of Nd_2O_3 on Si substrate after decomposition

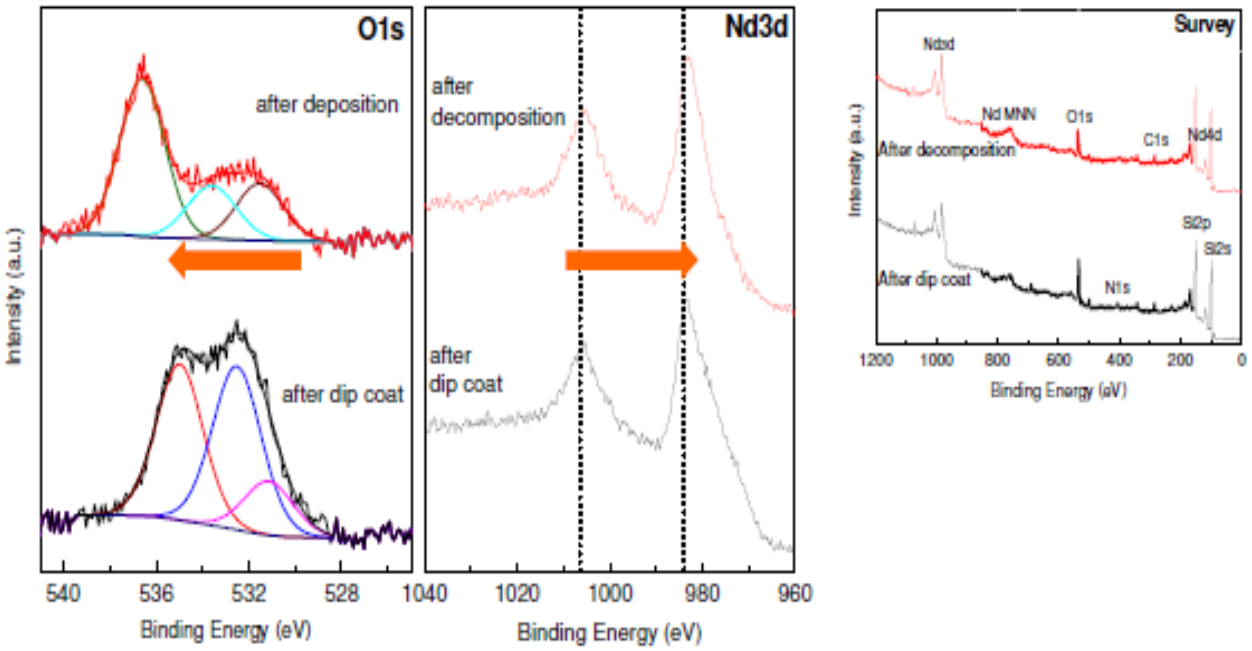


Fig. 24: XPS of O1s, Nd 3d and survey scan of Nd_2O_3 after dip-coating (black) and post decomposition (red) on Si substrate

Based on the XPS data (Fig. 24) for Nd_2O_3 sample, it is shown that the Si 2p peak after dip-coating and decomposition is not observed which indicates that there is no interfacial layer formation.

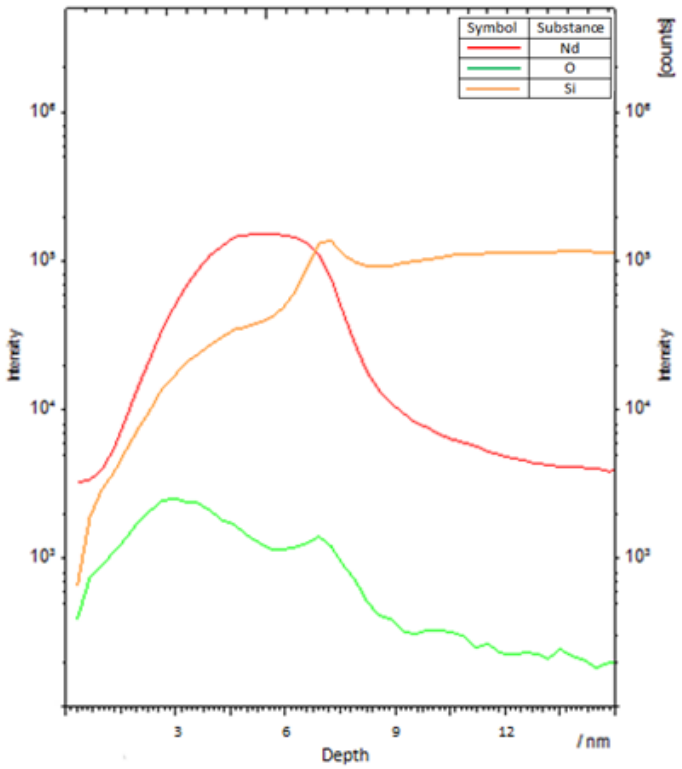


Fig. 25: TOF-SIMS data of Nd_2O_3 on Si substrate

However, upon annealing, the TOF-SIMS result in Fig. 25 indicates that a thin layer of undesirable SiO_x film had formed as well. Similar to earlier mentioned CeO_2 samples, Nd_2O_3 suffers the same predicament of being an ionic compound which generates high concentration of oxygen vacancies which thus leads to the interfacial SiO_x [100]. Apart from degrading the overall capacitance, the presence of this interfacial layer is also said to increase interface roughness, leakage current and stress-induced hole traps [102, 103].

4.3.2 Electrical Characterization

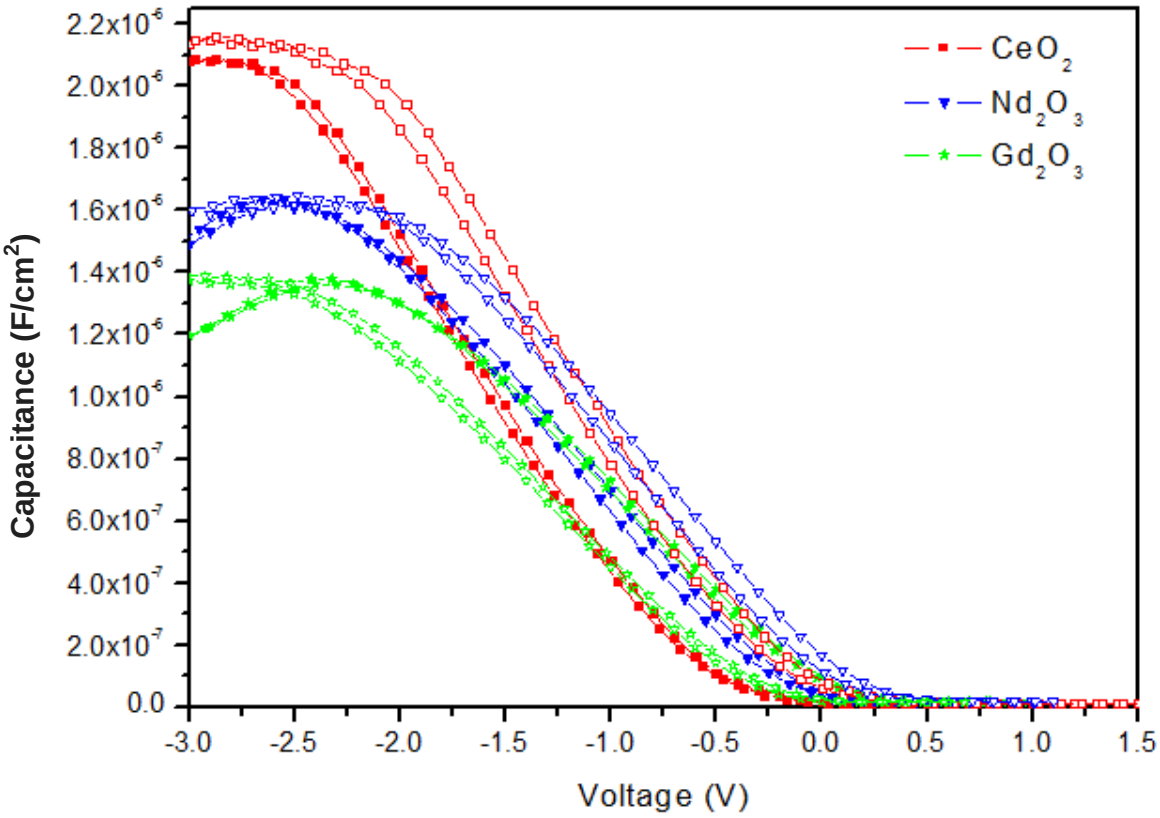


Fig. 26: C-V curve of CeO_2, Nd_2O_3 and Gd_2O_3 annealed at 600°C (filled) and 800°C (open)

Table 3: Summary of k-value, EOT and leakage current density of CeO_2, Nd_2O_3 and Gd_2O_3 annealed at 600°C

Samples	k-value	EOT	Leakage current density -1V	Leakage current density +1V
CeO_2	17.1	2.28	8.94×10^{-6}	2.34×10^{-7}
Nd_2O_3	14.7	2.65	2.62×10^{-5}	1.95×10^{-7}
Gd_2O_3	11.5	3.39	6.23×10^{-6}	2.43×10^{-8}

As seen from the capacitance-voltage (C-V) plot in Fig. 26 of the lanthanide oxides, CeO_2 film has the highest capacitance value followed by Nd_2O_3 and Gd_2O_3, there is a slight improvement in the capacitance and reduced hysteresis observed for samples annealed at 600°C. This is due to the densification of films upon annealing which help reduces defects such as pinhole and also decrease the interface traps. In addition, the accumulation region of the as-deposited oxide does not form a flat curve which is likely due to high leakage current as measured capacitance is affected by poor metal contact formation or when there is high leakage current. The slope improves upon annealing, which also concludes that the film is densified with reduced defects for current to leak through [95]. Upon annealing, the C-V curve shows a slight flatband voltage (V_{FB}) shift to the left which is likely due to two possible reasons – (i) fixed positive fixed charge generated in the dielectric and (ii) large interface states density could be expected because no post-metallization forming gas annealing was performed [104]. This phenomenon could be induced by the interaction of cerium oxide and silicon at the interface which may create oxygen vacancies within film due to undesired non-stoichiometric interfacial layer formation [68] as reported earlier in the XPS results. It is also possible that the high density of positive charges is formed due to moisture adsorption [101].

Based on the C-V profile in Fig. 26, the measurement for all rare earth oxide films annealed at 600°C shows little hysteresis indicating minimal interfacial traps present. The as-deposited CeO_2 and Nd_2O_3 have higher capacitance due to the presence of fixed charges within oxide that induced stronger polarization. In addition, the slope at accumulation region is not flat suggests that the film contains defect that causes it to be leaky.

As shown in Fig. 26, the flatband voltage shift is quite significant due to the traps and charges [93] which is observed for all lanthanide films annealed at 800°C.

Gadolinium oxide (Gd_2O_3) is one of the rare earth oxides extensively studied due to having a half-filled 4f shell leading to its wide band gap (~5. 6eV) [78] and also a intrinsic high energy of 5d shell which allows only one electron occupancy. It is proposed as a possible candidate for high-k dielectrics due to its predicted thermodynamic stability on Si with large band gap expected arising from the half-filled 4f shell of Gd. In addition, gadolinium has a unique oxidation number (=3) that helps avoid mixed oxide stoichiometries and the 2:3 ratio of metal to oxygen stoichiometry which promotes low charge neutrality level and hence large conduction band offsets with Si. However, due to its higher lattice energy as compared to lighter lanthanide elements, Gd_2O_3 is also expected to crystallize at lower temperature [96].

Based on the C-V measurements, the Gd_2O_3 shows little hysteresis as compared to CeO_2 and Nd_2O_3; which coincides well with prediction that it has intrinsic high energy of 5d shell and its low occupancy (only one electron for Gd).

The 800°C Gd_2O_3 annealed sample may be undergoing crystallization which induces a higher k-value compared to annealed at 600°C sample. The AFM image supports this finding as the surface appears to be rougher likely due to grain boundary formation similar to reported Y_2O_3 [105]. The C-V plot shows flatband voltage shift induced by traps and charges within film and at interface.

The C-V measurements show that Gd_2O_3 has a lower k-value than Nd_2O_3 and CeO_2, and k-values obtained at accumulation after annealing at 600°C are as shown in Table 3.

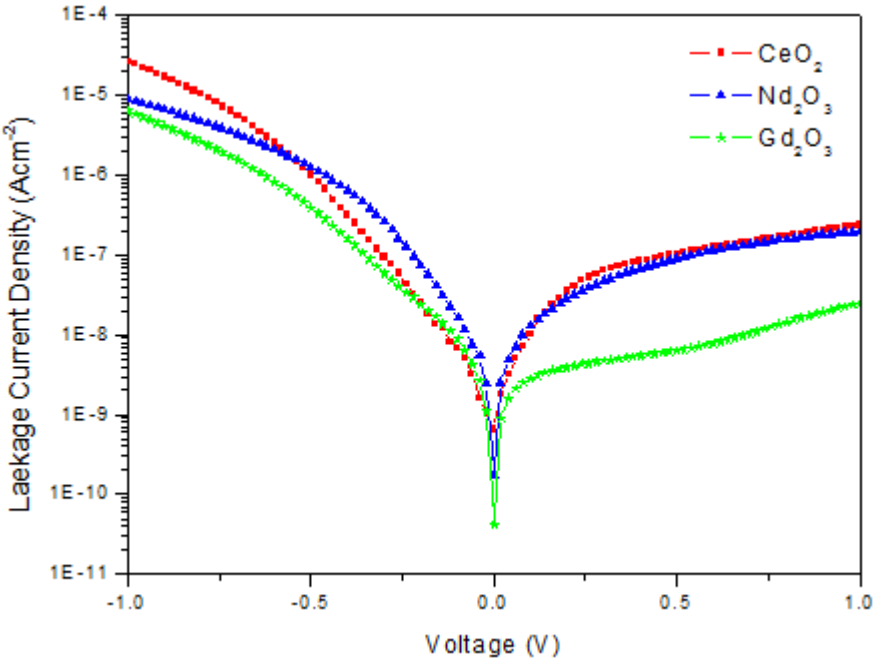


Fig. 27: I-V curve of CeO_2, Nd_2O_3 and Gd_2O_3 annealed at 600°C

The I-V curve of CeO_2, Nd_2O_3 and Gd_2O_3 in Fig. 27 agrees well with the C-V measurements as there is little shift for off-state at 0V. Based on Fig. 26, the leakage current is still within the acceptable range reported in ITRS 2009 [106].

It is observed that leakage current is reduced after annealing at 600°C. Reduction of current leakage is likely due to the reduction of physical defects within film (e.g. pinhole) however, the leakage current under positive bias seems to contradict this. Hence, this interesting phenomenon needs to be further studied. The leakage current at -1V and +1V is summarized in Table 3.

As for Gd_2O_3 sample, the leakage current increased with annealing and can be explained by the lower crystallization temperature of Gd_2O_3 that may have induced grain boundary formation upon annealing. The leakage current of 800°C annealed sample is higher compared to the others due to the formation of grains that may

induce leaky paths for current to tunnel through. Table 3 shows the leakage current of Gd_2O_3 samples at -1V and +1V.

4.4 Summary (Analytical review)

In this chapter, the benchmark for the electrical performance and properties of rare earth oxides (CeO_2, Nd_2O_3 and Gd_2O_3) are established. All oxides prove to be possible candidates for SiO_2 substitution as gate oxide due to the high k-value (~16 for Gd_2O_3; ~22 for Nd_2O_3 and ~26 for CeO_2). The thin oxides of thickness ~3nm for CeO_2, Nd_2O_3 and Gd_2O_3 demonstrated to have acceptable leakage current and roughness of about less than 1nm even after annealing.

5. TITANIUM OXIDE (TiO_2) FABRICATED VIA ALD AS PASSIVATION LAYER

In order to suppress the formation of Si-O interfacial layer and improve the EOT, a higher dielectric constant material (TiO_2) is deposited using ALD to form a passivation layer. The novelty presented in this chapter is the application of passivation layer deposited via ALD to form a smooth, conformal and uniform thin film prior to PLD-deposited cerium oxide (CeO_2) to prevent formation of large particles and rough interface between oxide and Si substrate. A cerium oxide (CeO_2) film is deposited using PLD on a RCA-cleaned sample to act as a control whereas another sample is with passivation layer titanium oxide (TiO_2) deposited.

5.1 Results and Discussion

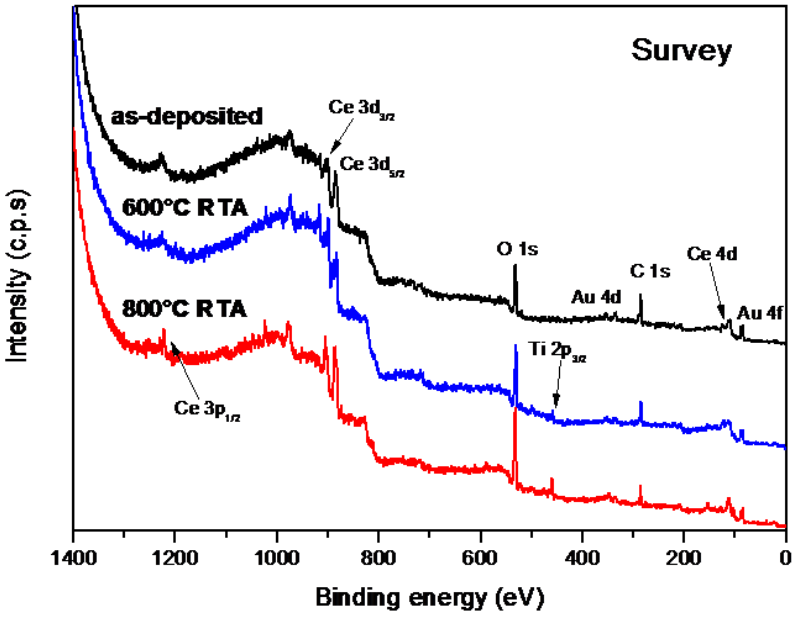


Fig. 28: XPS survey scan of CeO_2/TiO_2 bilayer film stack on Si substrate

The XPS survey scan in Fig. 28 confirms the presence of cerium, oxygen and titanium with gold electrodes as the calibration.

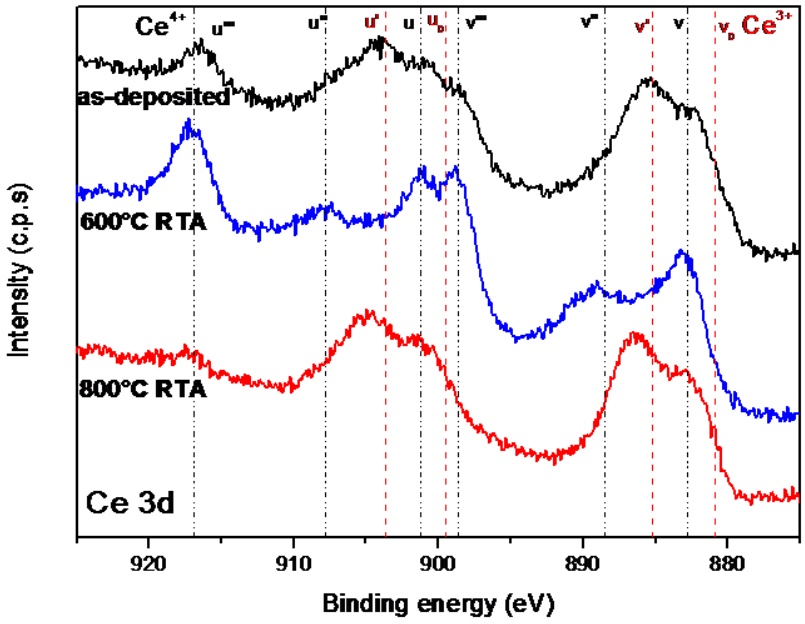


Fig. 29: XPS data of Ce 3d characteristic peaks for CeO_2/TiO_2 bilayer sample

From the 3d signals of cerium in Fig. 29, it is observed that there is a shift from Ce^{4+} to Ce^{3+} upon annealing at 800°C. The u''' characteristic of Ce^{4+} is missing for 800°C annealed sample suggesting the change in oxidation state. This implies that there is a change of the CeO_2 sample to Ce_2O_3[107-109].

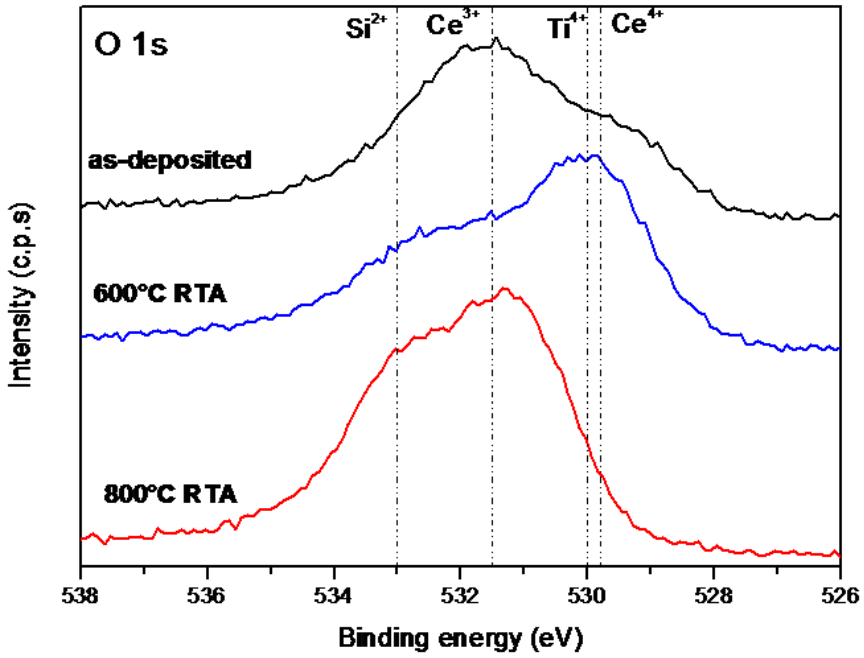


Fig. 30: XPS data of O 1s peaks for CeO_2/TiO_2 bilayer sample

The O 1s signals from Fig. 30 further confirmed that the annealing at 800°C caused cerium oxide to shift from CeO_2 to Ce_2O_3. This indicates the change in Ce oxidation state which is likely to induce higher interface trap density and also undesirable SiO_x interfacial layer formation as describe by Hubbard *et. al.*[110]

As seen from the capacitance-voltage (C-V) plot of the CeO_2 film with and without annealing in Fig. 31, there is improvement in the capacitance and reduced hysteresis observed for samples annealed at 600°C. This is due to the densification of films upon annealing which help reduces defects such as pinhole and also decrease the interface traps. In addition, the accumulation region of the as-deposited oxide does not form a flat curve which is likely due to high leakage current as measured capacitance is affected by poor metal contact is formation or when there is high leakage current. The slope improves upon annealing, which also concludes that the film is densified with reduced defects for current to leak through [111]. Upon

annealing, the C-V curve shows a slight flatband voltage (V_{FB}) shift to the left which is likely due to two possible reasons – (i) fixed positive fixed charge generated in the dielectric and (ii) large interface states density could be expected because no post-metallization forming gas annealing was performed [104]. This phenomenon could be induced by the interaction of cerium oxide and silicon at the interface which may create oxygen vacancies within film due to undesired non-stoichiometric interfacial layer formation [68] as reported earlier in the XPS results. It is also possible that the high density of positive charges is formed due to moisture adsorption [101].

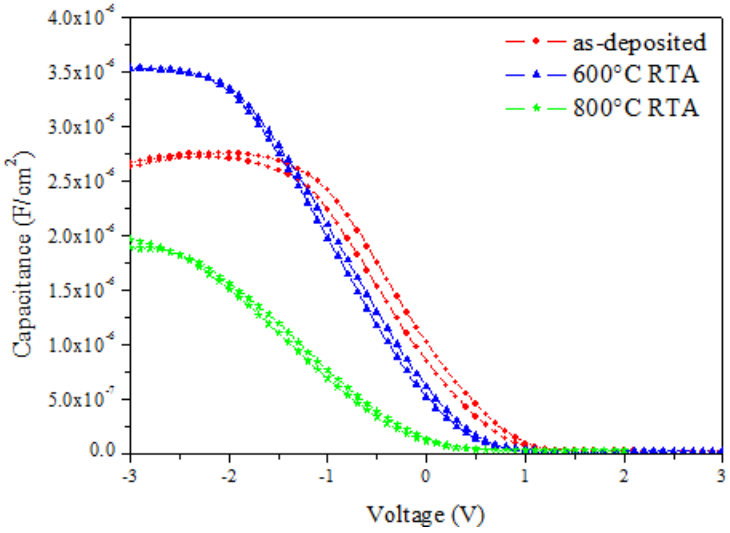


Fig. 31(a): C-V plot of CeO_2/TiO_2 sample at varying annealing temperatures

Samples	k-value	EOT	D_{it}
As deposited	14.7	1.67 nm	4.9×10^{12} cm^{-2} eV^{-1}
600°C RTA	18.0	1.36 nm	5.2×10^{12} cm^{-2} eV^{-1}
800°C RTA	11.3	2.17 nm	2.1×10^{13} cm^{-2} eV^{-1}

Fig. 31(b): Matrix of summarized electrical properties for annealed CeO_2/TiO_2 film

In Fig. 31, the C-V plot shows the electrical performance of CeO_2 with TiO_2 interfacial layer. It is observed that there is a decrease in overall capacitance of samples with

TiO_2 interfacial layer. This is due to the effect of series capacitance [16] as shown in Equation 4. However, this decrease in capacitance is not significant compared to that of CeO_2 only. From the C-V curve, it is observed that annealed sample has a more significant hysteresis compared to as-deposited sample. This implies that there is interface traps found at high-k/Si interface for annealed sample. Upon annealing, the capacitance is slightly improved and C-V curve is shifted towards more positive bias (closer to 0V) due to the densification of film, reduction of defects in film and decrease in fixed oxide charges in the bulk oxide. Both samples of 800°C-annealed and without annealing demonstrates a not 'flat' curve at accumulation region that is due to the high leakage current as it is known that TiO_2 has small band gap (~3eV) and conduction band offsets which promotes electron-tunnelling [67] as well as the crystallization of TiO_2 which acts as 'leaky' paths.

With good interface properties, interfacial layer is able to improve mismatch at high-k/Si interface by reducing dangling bonds and Si-O strained bonds. Hence, trap generation and localized physical damage near interface which is found to degrade gate oxide and trigger dielectric soft breakdown can be reduced [52].

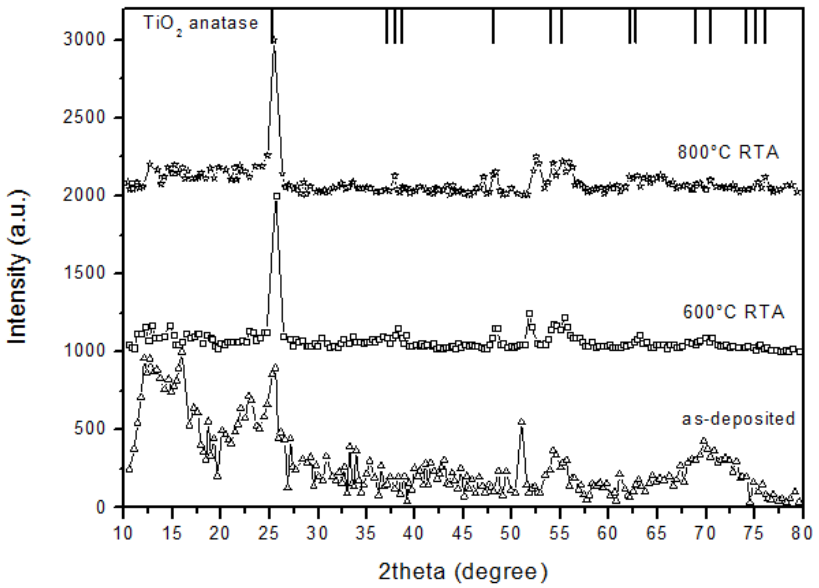


Fig. 32: XRD plot of TiO_2 at various annealing temperature

Based on Fig. 32, the 800°C annealed sample the stretching of C-V curve is highly plausible due to Fermi level pinning which infers the high level of interface trap density which concurs with D_{it} value in Table 4. This trap density is thus caused by the formation of titanium silicide and SiO_2 interfacial layer which is detrimental to the overall gate oxide performance. This matches the thermodynamic studies done by Hubbard *et. al.* (Table 4) which describes that when silicon is in contact with TiO_2, it is highly probable for titanium silicide and SiO_2 to form.

Table 4: Thermodynamic stability of binary oxides in contact with silicon at 1000K [110]

$Si + MO_x$ ---> $M + SiO_2$	
Element	Thermodynamics Gibbs Free Energy: G_{1000}
CeO_2	+36.290
TiO_2	+7.527

$Si + MO_x$ ---> $MSi_z + SiO_2$	
Element	Thermodynamics Gibbs Free Energy: G_{1000}
CeO_2	-7.908
TiO_2	-23.014

Moreover, lattice mismatch of TiO_2 with silicon (Table 5) can also lead to the high interface trap density. Furthermore, based on XRD done on TiO_2 film of 100nm thickness, crystallization occurs upon annealing which leads to high leakage current as grain boundaries act as 'leaky' paths.

Table 5: Lattice parameter of Si, CeO_2 and TiO_2 [109]

Element	Lattice parameter	
	(a)	(c)
Si	5.43Å	
CeO_2	5.41Å	
TiO_2 (Anatase)	3.74Å	9.39Å
TiO_2 (Rutile)	4.59Å	2.96Å

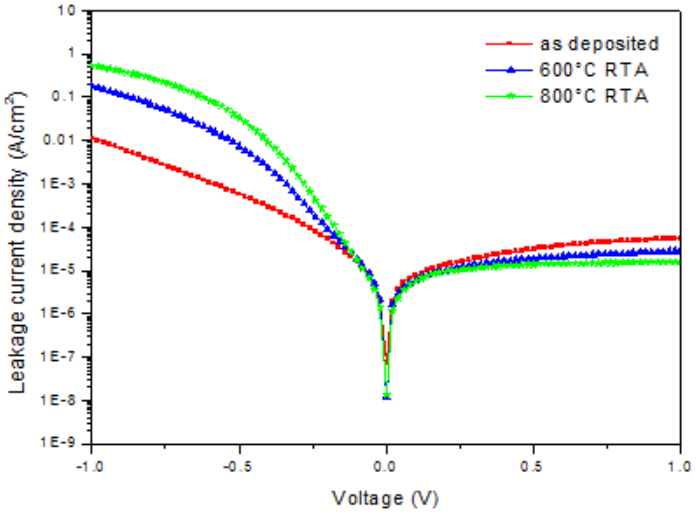


Fig. 33(a): I-V plot of CeO_2/TiO_2 sample at varying annealing temperatures

Samples	Leakage current density	
	-1V	+1V
As-deposited	1.13×10^{-2}	5.44×10^{-5}
600°C RTA	0.177	2.81×10^{-5}
800°C RTA	0.542	1.58×10^{-5}

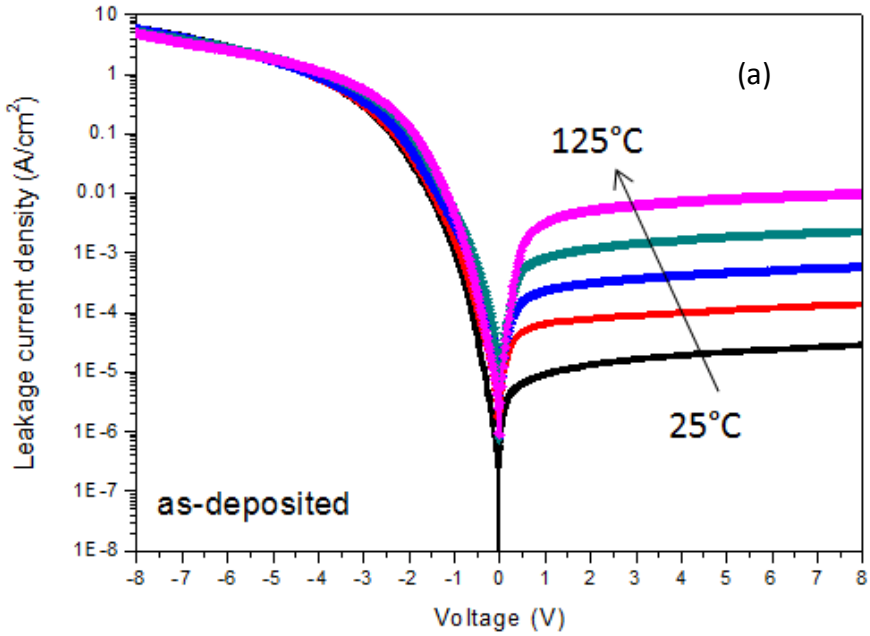
Fig. 33(b): Summarized leakage current density of CeO_2/TiO_2 samples annealed at varying temperature

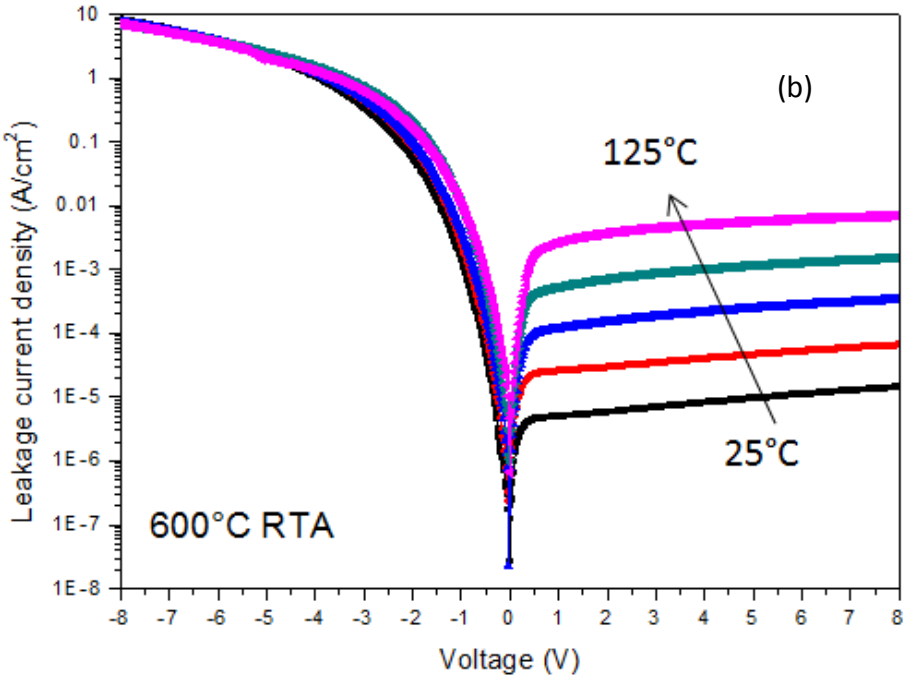
The I-V data in Fig. 33 coincides well with the earlier finding with regards to TiO_2 crystallization and probable silicide formation which induces higher leakage current for the annealed samples. The leakage current at -1V is extremely high and unsuitable for gate oxide application.

5.2 Leakage Current Conduction Mechanism

In order to better understand the leakage conduction mechanism of the bilayer CeO_2/TiO_2 gate dielectric, a temperature dependent I-V measurement from 25°C to 125°C had been done for the different annealed samples. It is important to

understand the conduction mechanism in novel high-k materials in order to select and integrate the suitable material for transistor application.





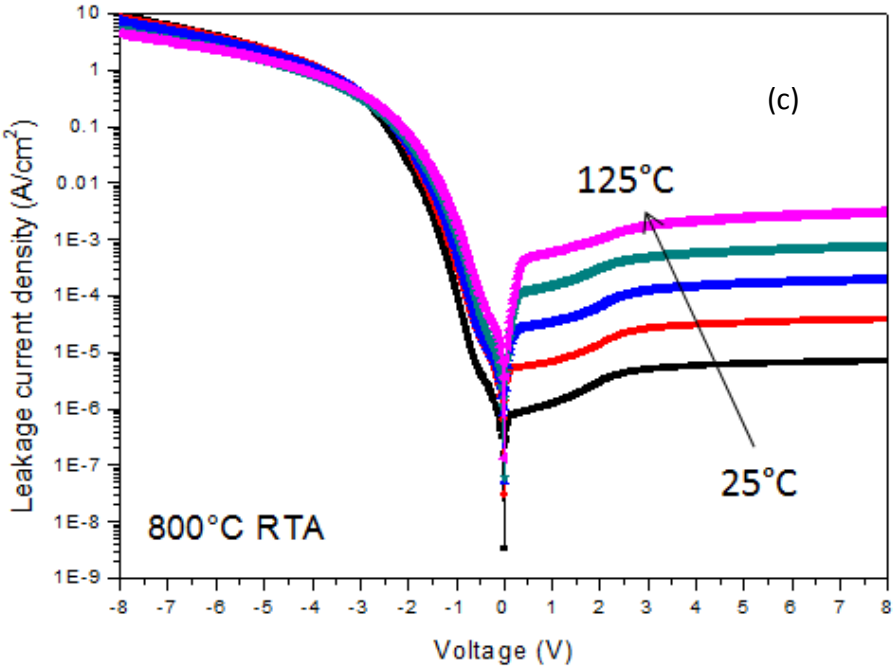


Fig. 34: Temperature dependent I-V curve from 25°C to 125°C for CeO_2/TiO_2 bilayer stack of (a) as-deposited, (b) 600°C annealed and (c) 800°C annealed samples

From the temperature dependent I-V curve in Fig.34, it is observed that the off-state is temperature dependent. In addition, polarity assymetry in the I-V curves are observed. These observations further confirm the interfacial layer formation which leads to the E-field near the injecting interface to be modified by trapped charges. Another interesting observation is that annealed samples have lower leakage current at the off-state which can be explained by the additional interfacial layer formation which inadvertently reduces overall capacitance as well.

Although 800°C annealed samples have rougher surfaces shown via AFM and crystallization as detected in XRD, the expected higher leakage was not observed and thus leads to the hypothesis of interfacial layer formation [112, 113]. This undesirable layer also reduces the overall capacitance as shown in C-V measurement collected.

TEM images of the CeO_2/TiO_2 bilayer stack annealed at 600°C (Fig. 35) and 800°C (Fig. 36) confirmed the undesirable interfacial layer formation which matches the hypothesis with regards to lower overall capacitance and leakage current finding.

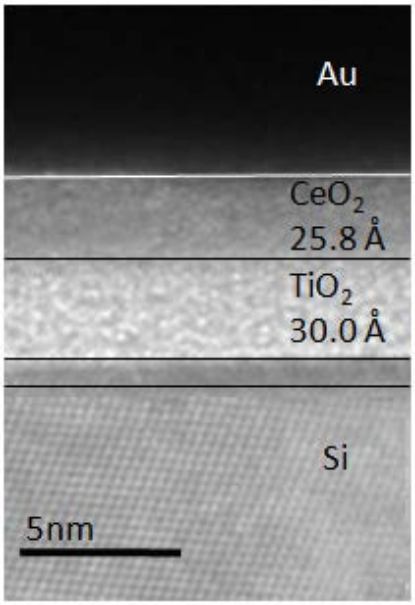


Fig. 35: TEM image of CeO_2/TiO_2 bilayer film stack on Si substrate after annealing at 600°C

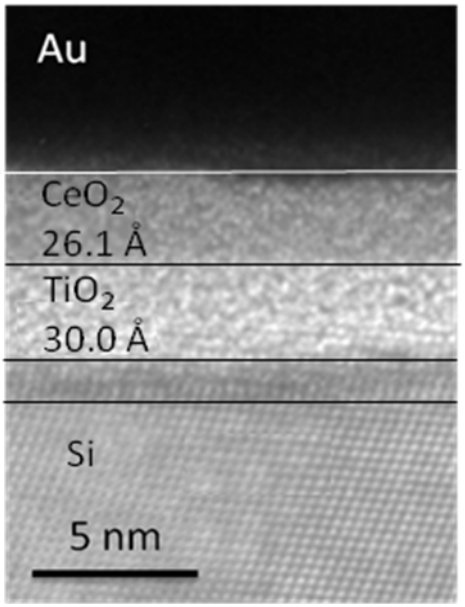


Fig. 36: TEM image of CeO_2/TiO_2 bilayer film stack on Si substrate after annealing at 800°C

Based on this study, it is noted that the mixing of two or more high-k materials can result in local compositional and structural inhomogeneties, especially in varying annealing conditions such as oxygen ambient or different oxygen partial pressure. This is because at different annealing conditions, the possibility of interfacial layer formation and changes in the high-k material oxidation state may vary. These different features can be complicated since multi-layer film stack may induce a combination of several leakage current conduction mechanisms as well as dependent on growth conditions.

For instance, CeO_2/TiO_2 bilayer gate dielectric being annealed at 600°C has showed approximately 4 times higher k-value than that of SiO_2. The presence of undesirable interfacial layer has lead to observable polarity asymmetry of I-V temperature curves, changes in film oxidation state as well as reduced overall capacitance. However, the expected lower leakage current for annealed samples was not observed due to the IL formation.

The leakage current vs. voltage profile as shown in Fig. 33 proves that TiO_2 passivation layer does increase the leakage current compared to the sample without passivation layer. This is as previously mentioned due to the small conduction band offsets and band gap of titanium oxide. The leakage current of sample with TiO_2 passivation layer is about 4-5 orders of magnitude higher. However, Fig. 33 coincides with the C-V measurement prediction of little or no interface traps present as the off-state (lowest leakage current) is at 0V. It is reported in other demonstrated experiments [93] that the large amount of charged defects in high-k dielectrics is observed through shift of flatband voltage (V_{FB}) in I-V and C-V measurements.

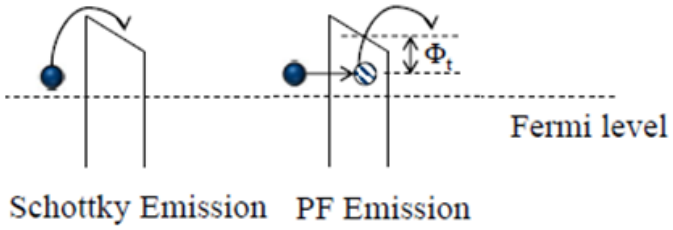
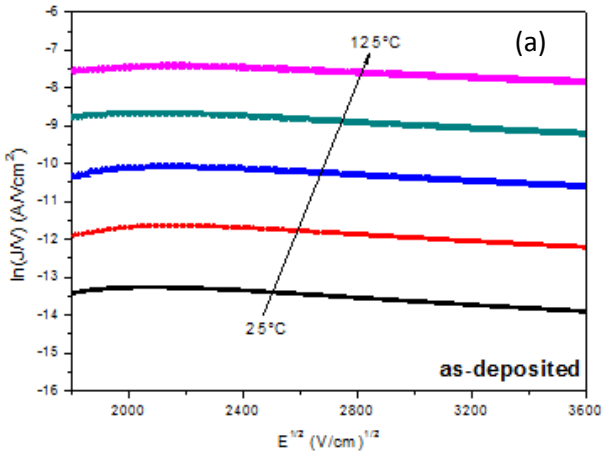
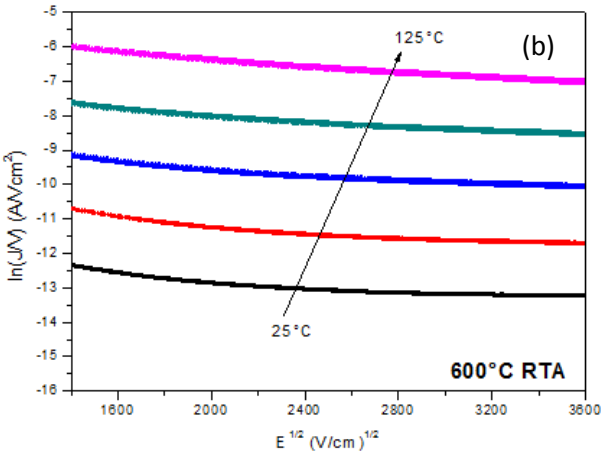


Fig. 37: Leakage current conduction mechanism of Schottky and Poole-Frenkel emission

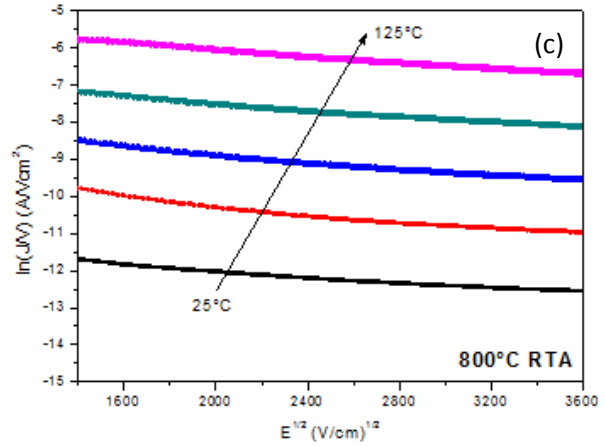
$$2\beta_{pf} = \beta_{sc} = \sqrt{\frac{q}{4\pi\varepsilon_0\varepsilon_r}} \tag{10}$$



Calculated $\sqrt{\frac{q}{4\pi\varepsilon_0\varepsilon_r}}$ (eV.V$^{1/2}$.m$^{1/2}$)	From plot β_{SC} (eV.V$^{1/2}$.m$^{1/2}$)	From plot $2\beta_{PF}$ (eV.V$^{1/2}$.m$^{1/2}$)
1.04 x 10^{-5}	6.69 x 10^{-6}	1.34 x 10^{-5}
Trap levels – 1.6eV		



Calculated $\sqrt{\frac{q}{4\pi\varepsilon\varepsilon_r}}$ (eV.V$^{1/2}$.m$^{1/2}$)	From plot β_{SC} (eV.V$^{1/2}$.m$^{1/2}$)	From plot $2\beta_{PF}$ (eV.V$^{1/2}$.m$^{1/2}$)
7.75 x 10^{-6}	7.61 x 10^{-6}	1.52 x 10^{-5}
Intrinsic barrier height – 1.56 eV		



Calculated $\sqrt{\frac{q}{4\pi\varepsilon\varepsilon_r}}$ (eV.V$^{1/2}$.m$^{1/2}$)	From plot β_{SC} (eV.V$^{1/2}$.m$^{1/2}$)	From plot $2\beta_{PF}$ (eV.V$^{1/2}$.m$^{1/2}$)
8.78 x 10^{-6}	8.89 x 10^{-6}	1.78 x 10^{-5}
Intrinsic barrier height – 1.44 eV		

Fig. 38: Plot of ln J/V vs. $E^{1/2}$ for CeO_2/TiO_2 bilayer film stack of (a) as-deposited, (b) 600°C annealed and (c) 800°C annealed samples with extracted field lowering coefficient (β)

As described by Nataraj *et. al.* [114], by matching the equation 10 with the field lowering coefficient (β), which is extracted from slope against e/kT, the main

mechanism contributing to the leakage current conduction can be determined. As shown in equation 10, coefficient β is the essential factor in determining the mechanism obtained from the slope of ln(J/V) vs. $E^{1/2}$ which is then compared to calculated β value $\sqrt{\frac{q}{4\pi\varepsilon_0\varepsilon_r}}$. In addition, the intrinsic barrier height for the electrons to hop over the conduction band can be determined from the slope of $\ln(J/T^2)$ vs. 1/T. Based on the plots as shown in Fig. 38, as-deposited sample showed Poole-Frenkel emission mechanism as the $2\beta_{PF}$ value is closer to the calculated β value. As for annealed samples (both 600°C and 800°C), the leakage current conduction mechanism is predominantly Schottky emission. This change in mechanism is plausible due to interfacial layer formation which induced higher interface trap density that is likely to trap charges at a certain energy level before hopping over the conduction band (Fig. 37).

$$\ln(J/V) = \ln B + \frac{\gamma\sqrt{E} - q\phi_{pf}}{kT} \tag{11}$$

5.3 Summary (Analytical Review)

This chapter demonstrated the application of TiO_2 as a passivation layer between CeO_2 and Si substrate deposited via atomic layer deposition using $TiCl_4$ and water as precursors. Studies showed that although the dielectric constant for 600°C annealed sample is the highest (~18) however, the leakage current density had increased which is caused by the interfacial oxide formation as well as the possibility of silicide formation. Due to the high leakage current, it is found that CeO_2/TiO_2 is not suitable for gate dielectrics application. However, it is still of interest to understand the leakage current conduction mechanism and based on our studies, it is shown that upon annealing, Schottky emission becomes the dominating factor which correlates to thermionic effect influenced by interface properties.

6. GADOLINIUM SILICATE (GdSiO) VIA ALD AS PASSIVATION LAYER

Due to the moderate dielectric constants and superior leakage properties as well as interface stability with Si substrate, silicates (complex oxide) are potential gate dielectrics for future CMOS technology. One of the possible silicate deposition techniques is via ALD using silyl-amide complexes which react with water. NMR plot (Fig. 39) confirms the presence of *methyl* peak of the precursor which enables the formation of silicate.

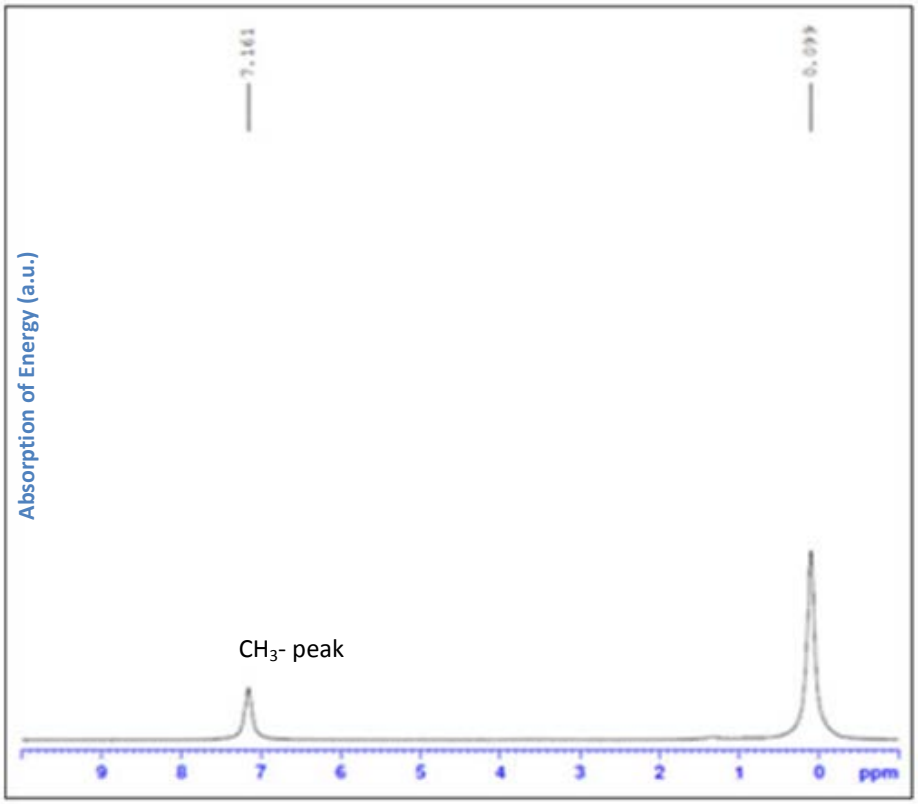


Fig. 39: NMR plot of commercially available $[(Me_3Si)_2N]_3Gd$

Gadolinium oxide has shown promising results with high-k values and low leakage current. In addition, it has higher thermodynamic stability due to the half-filled *d* states. However, in order to improve the interfacial properties with silicon, it is proposed that gadolinium silicate to be used as passivation layer due to small lattice

mismatch and presence of Si which helps to suppress the undesirable SiO_x interfacial layer from forming.

6.1 Results and Discussion

As described in Chapter 3, the gadolinium silicate passivation film is deposited via atomic layer deposition (ALD), followed by deposition of CeO_2 via pulsed laser deposition (PLD). This chapter shall compare the performance of Gd-silicate passivation layer against that of TiO_2 which was discussed in Chapter 5.

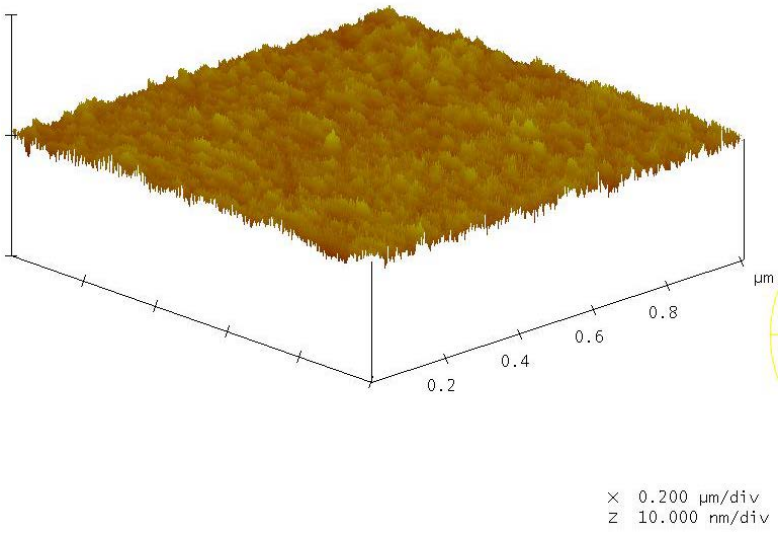


Fig. 40: AFM image of 1x1µm of CeO_2/GdSiO sample annealed at 600°C (RMS~0.82nm)

Based on AFM data as shown in Fig. 40, the films are conformal and smooth for CeO_2/GdSiO bilayer stack.

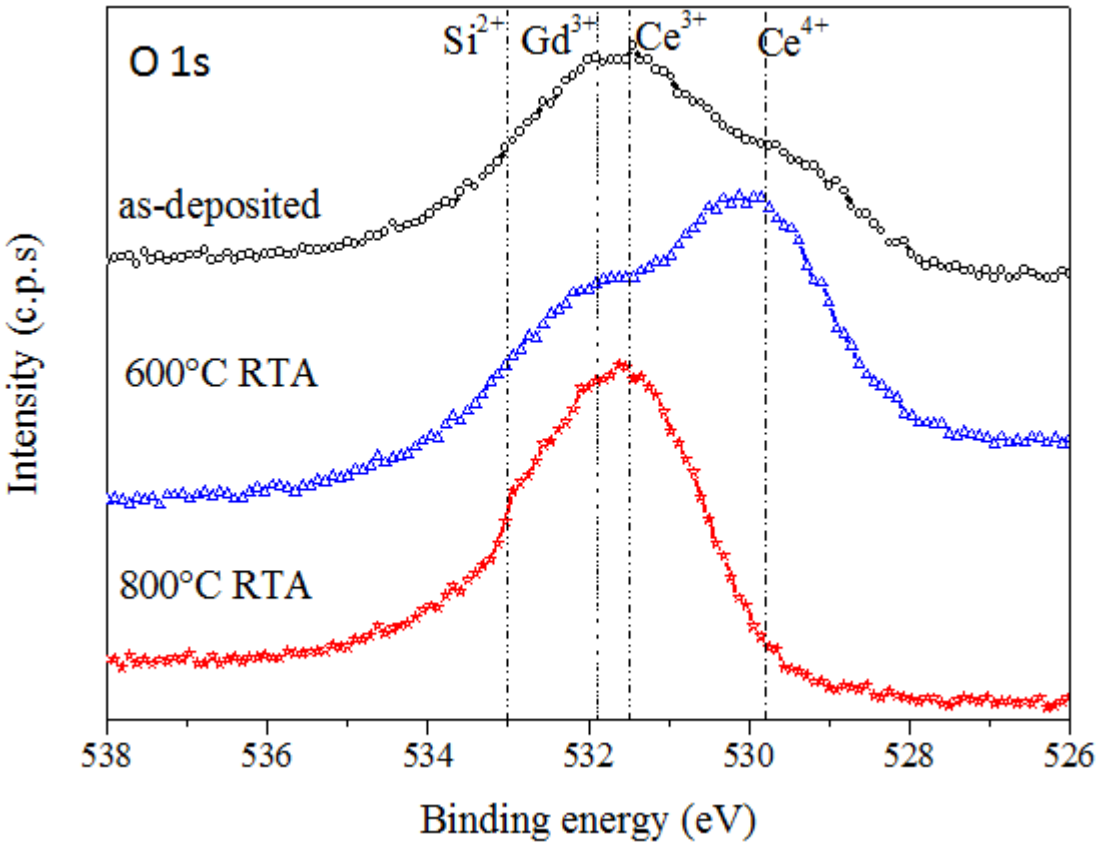


Fig. 41: XPS data of O 1s peak for CeO_2/GdSiO bilayer film stack on Si substrate

XPS data shown in Fig. 41, it is shown that there is no change in oxidation state in cerium oxide for annealed samples. This implies the thermodynamic stability of the film stack which infers that there is no interfacial layer formation for the sample as changes in oxidation state creates oxygen vacancies which leads to SiO_x formation.

However, sample annealed at 800°C showed that the O1s peak for Ce^{4+} had diminished and instead Ce^{3+} is observed. As compared to CeO_2/TiO_2 sample, the CeO_2/GdSiO sample remain stable upon annealing at 600°C, this implies that it is likely that TiO_2 induces the interfacial layer/silicide formation which indirectly caused the change in CeO_2 oxidation state.

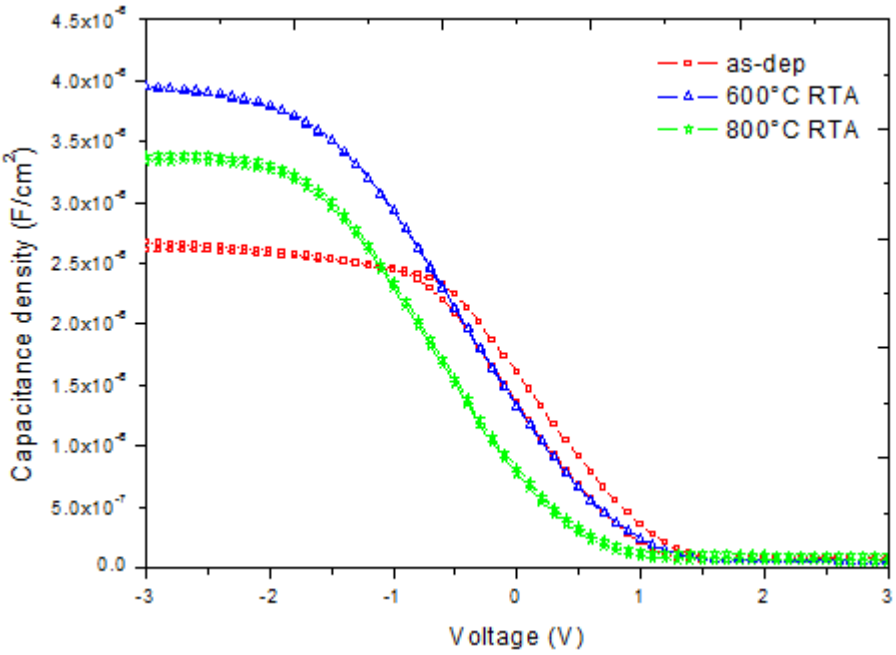


Fig. 42(a): C-V plot of CeO_2/GdSiO sample at varying annealing temperatures

Samples	k-value	EOT	D_{it}
As-deposited	7.44	2.97	2.7×10^{12} cm^{-2} eV^{-1}
600°C RTA	12.8	1.72	7.9×10^{11} cm^{-2} eV^{-1}
800°C RTA	9.30	2.37	9.5×10^{11} cm^{-2} eV^{-1}

Fig. 42(b): Matrix of summarized electrical properties for annealed CeO_2/GdSiO film

Capacitance-voltage (C-V) curves in Fig. 42 indicated that the k-value of CeO_2/Gd-silicate bilayer stack has a lower k-value than that of CeO_2 only film due to *capacitance series*. However, the annealed samples showed minimal hysteresis which is reflected by the low D_{it} due to film densification and reduced defects.

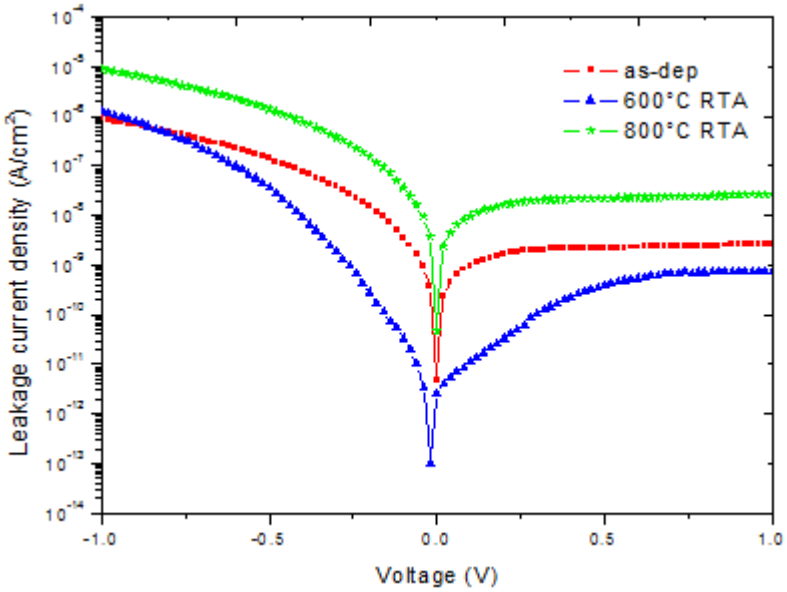


Fig. 43(a): I-V plot of CeO_2/GdSiO sample at varying annealing temperatures

Samples	Leakage current density	
	-1V	+1V
As-deposited	8.85×10^{-7}	2.64×10^{-9}
600°C RTA	1.31×10^{-6}	7.32×10^{-10}
800°C RTA	9.21×10^{-6}	2.49×10^{-8}

Fig. 43(b): Summarized leakage current density of CeO_2/GdSiO samples annealed at varying temperature

From Fig. 43, the I-V curves had shown promising result of lower leakage current density even as compared to that of CeO_2/TiO_2 samples. The leakage current for 600°C annealed sample is even lower than as-deposited sample due to the mitigation of defects and improved film densification. The leakage current level shows that CeO_2/GdSiO sample are suitable for nanaoelectronics application but the k-value has to be improved.

The temperature dependent I-V measurement shows similar results as that of CeO_2/TiO_2 whereby only the off-state is affected by the temperature changes. Hence, the leakage current conduction mechanism is also mainly focused on the off-state using the same equation by Nataraj *et. al.* [114] as mentioned earlier.

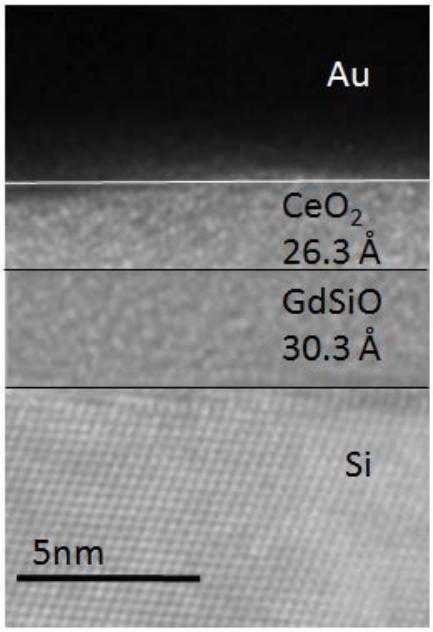


Fig. 44: TEM image of CeO_2/Gd-silicate bilayer film stack on Si substrate after annealing at 800°C

Fig. 44 showed that there is no additional undesirable interfacial layer between Gd-silicate and silicon even for samples annealed up to 800°C. This is due to the small lattice mismatch as well as presence of Si atoms in Gd-silicate as mentioned which helped in preventing the IL formation [100].

XPS of Si 2p peaks comparison for CeO_2/TiO_2 and CeO_2/GdSiO (Fig. 45) sample had further confirmed the presence of interfacial layer formation which matches well with our TEM and electrical data.

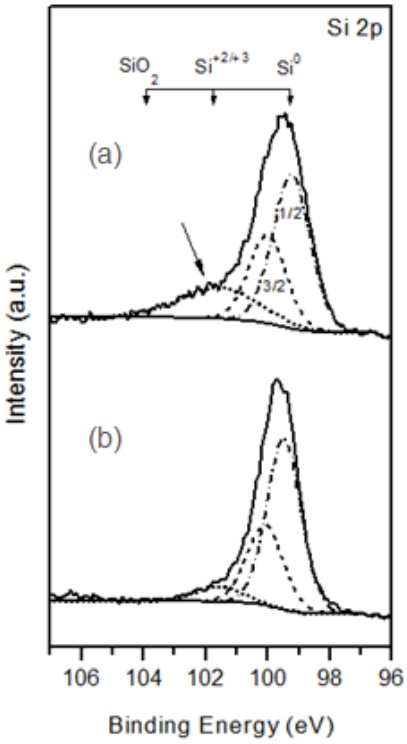
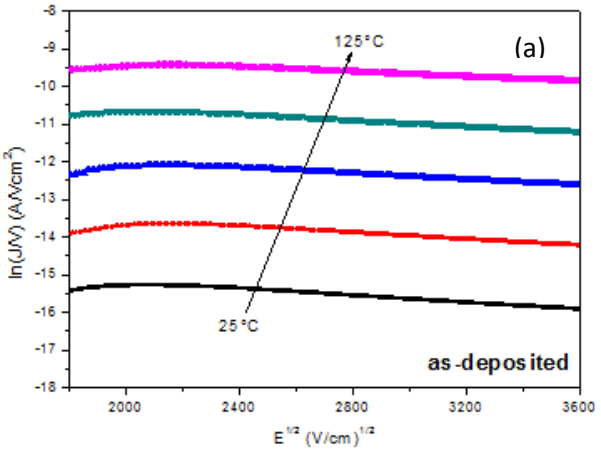
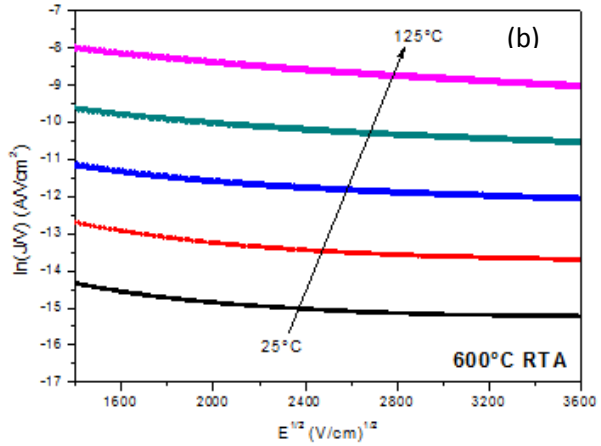


Fig. 45: Comparison of XPS – Si 2p peak data between (a) CeO_2/TiO_2 and (b) CeO_2/GdSiO bilayer film stack after annealing at 800°C

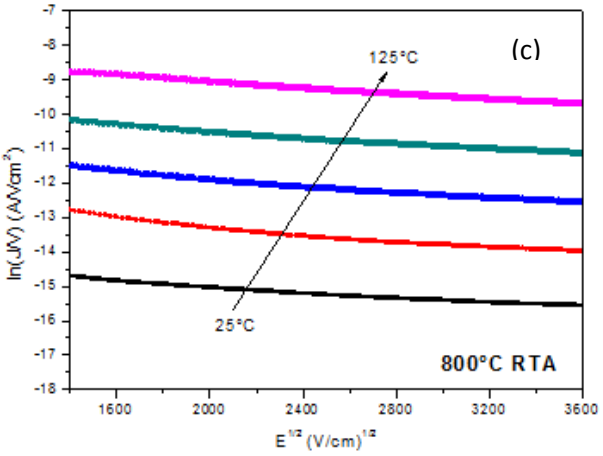
6.2 Leakage Current Conduction Mechanism



Calculated $\sqrt{\frac{q}{4\pi\varepsilon_0\varepsilon_r}}$ (eV.V$^{1/2}$.m$^{1/2}$)	From plot β_{SC} (eV.V$^{1/2}$.m$^{1/2}$)	From plot $2\beta_{PF}$ (eV.V$^{1/2}$.m$^{1/2}$)
1.39 x 10^{-5}	1.02 x 10^{-5}	2.05 x 10^{-5}
Intrinsic barrier height – 1.78 eV		



Calculated $\sqrt{\frac{q}{4\pi\varepsilon_0\varepsilon_r}}$ (eV.V$^{1/2}$.m$^{1/2}$)	From plot β_{SC} (eV.V$^{1/2}$.m$^{1/2}$)	From plot $2\beta_{PF}$ (eV.V$^{1/2}$.m$^{1/2}$)
1.06 x 10^{-5}	9.87 x 10^{-6}	1.97 x 10^{-5}
Intrinsic barrier height – 2.12 eV		



Calculated $\sqrt{\frac{q}{4\pi\varepsilon_0\varepsilon_r}}$ (eV.V$^{1/2}$.m$^{1/2}$)	From plot β_{SC} (eV.V$^{1/2}$.m$^{1/2}$)	From plot $2\beta_{PF}$ (eV.V$^{1/2}$.m$^{1/2}$)
1.24 x 10^{-5}	6.90 x 10^{-6}	1.38 x 10^{-5}
Trap levels – 0.87eV		

Fig. 46: Plot of ln J/V vs. $E^{1/2}$ for CeO_2/GdSiO bilayer film stack of (a) as-deposited, (b) 600°C annealed and (c) 800°C annealed samples with extracted field lowering coefficient (β)

Similar to CeO_2/TiO_2 sample, temperature dependent I-V data had been collected for leakage current conduction mechanism study as well. Based on equation 10 [114], it is found that for as-deposited and 600°C annealed sample, both are dominated by Schottky emission which is due to the gadolinium silicate film properties. However, for sample annealed at 800°C, the mechanism is observed to be Poole-Frenkel dominated due to the change in oxidation state of the bulk CeO_2 to Ce_2O_3. The change in oxidation state of the CeO_2 is likely to form O traps which is capable of

trapping electrons. As described by Zhao *et. al.*, Poole-Frenkel mechanism occurs due to thermal electrons being excited into the conduction band of an insulator when a field is applied [102]. This agrees with the finding of Ce change in oxidation state from Ce^{2+} to Ce^{3+} which leads to O traps formation [115].

Based on the calculated β coefficient and the β extracted from slope of ln(J/V) vs. $E^{1/2}$, the as-deposited and 600°C annealed samples are shown to be a closer match to Schottky emission. This is due to the use of silicate passivation layer which dominates the overall electrical performance of the film stack. Based on TEM result of CeO_2/GdSiO sample, there is no interfacial layer oxide formation and hence, unlikely to have interface traps issue which would then result in Poole-Frenkel emission instead. The leakage current conduction mechanism agrees with the finding as the dominant mechanism is Schottky emission.

6.3 Summary (Analytical Review)

This chapter shows the deposition of Gd-silicate passivation layer via atomic layer deposition (ALD) using silyl-amide precursor with water. The dielectric constant is reduced due to the silicate film but leakage current had improved by approximately 4-5 orders of magnitude as compared to CeO_2/TiO_2 samples. With further investigation, it was found that Gd-silicate managed to suppress interfacial layer formation based on TEM and XPS result. However, upon further investigation of the leakage current conduction mechanism, Schottky emission demonstrated by as-deposited and 600°C annealed samples switched to Poole-Frenkel upon higher annealing temperatures due to the change in oxidation state of Ce^{2+} to Ce^{3+} which leads to oxygen vacancies trapping electrons which are being excited into conduction band when electric field is applied.

7. CONCLUSION

Chip performance has tremendously increased during the past decades, advanced forward by the International Technology Roadmap for semiconductors (ITRS) that projects a doubling of the amount of transistors on a chip every two years. This achievement been mainly accomplished by downscaling the dimensions of the transistor, inclusive of the gate dielectric thickness to few atomic layers. As a result, the gate leakage current densities have reached undesirable levels leading to reliability issues in the devices. Hence, a specific class of alternative dielectrics known as rare earth oxides been studied both as binary and ternary compounds. These materials are being explored for their property to shift the work function of a metal gate towards n-type, which provide possibilities to engineer a proper transistor threshold voltage. In addition, they offer desirable thermal stability which enables a material to remain amorphous during the entire CMOS process. Finally they have been shown to reduce the thickness of the low-k interfacial layer between high-k and silicon substrate, which is currently one of the vital challenges to be resolve in order to reach ultimate EOT scaling.

As indicated in the ITRS in current century, the urge to develop an appropriate high k dielectric for the CMOS-technology in order to keep up with the Moore's law in the near future is critical. The various important properties listed for the gate dielectric include sufficient high permittivity, large band gap and band offsets, thermodynamic stability in contact with Si up to 1000 °C, a desirable film morphology, a high interface quality, compatibility with other materials deployed within the CMOS process and the long term reliability of the films. Although various high-k dielectrics have been investigated in the past such as ZrO_2, $LaAlO_3$ and HfO_2 as shown in Table 01 but none of them seems to satisfy the entire necessary requirements.

In our studies, from the previous section, it is shown that by having a passivation layer of TiO_2 at interface, the overall capacitance is reduced due to *series* capacitance and hysteresis in C-V curve increased with annealing. This is contradicts from initial hypothesis that TiO_2 is acting as an oxygen getter thus suppressing the interaction between CeO_2 film with underlying silicon substrate. Instead, XPS and TEM result indicates an undesired interfacial oxide layer formation which creates interface traps and defects that degrades the gate oxide performance. Due to the lattice mismatch and thermodynamics as described by Hubbard *et. al.*, TiO_2 could possibly react with Si to form silicide to form oxide at the interface. Furthermore, TiO_2 having small band gap and conduction offsets, with low crystallization temperature causes the leakage current to increase.

Proposed silyl-amide complex which reacts with water has better interface properties, as well as being thermodynamically stable with Si and having low leakage current (preserving the amorphous phase, wide band gap and CBO). Based on the NMR results, the $Si\text{-}CH_3$ peak of commercial gadolinium precursor at 0.09 was verified. Deposition of gadolinium silicate (GdSiO) was performed via atomic layer deposition. Bilayer film stack of CeO_2/GdSiO was formed and TEM/XPS results had indicated that even upon annealing up to 600°C, no undesirable interfacial layer was formed. Although the overall capacitance is lower due to *series* capacitance, the overall leakage is much lower by approximately 5 orders of magnitude from that of CeO_2/TiO_2 sample. In addition, the interface trap density estimated by conductance method is significantly lower than that of CeO_2/TiO_2 as well which coincides with no formation of interfacial layer oxide.

The temperature-dependence I-V was performed to better understand the leakage current conduction mechanism of bilayer stacks dielectric material mainly CeO_2/TiO_2

and CeO_2/GdSiO samples. Based on Nataraj *et. al.* equation, it is found that after annealing the CeO_2/TiO_2 samples, Schottky emission was the dominant mechanism which infers that it is electrode-limited and mainly influenced by interface properties. This finding matches well with the XPS and TEM data which showed that the CeO_2/TiO_2 samples had undesirable interfacial layer formation. As for CeO_2/GdSiO samples, the leakage current conduction mechanism was predominantly Schottkly emission due to Gd-silicate acting as the interface between CeO_2 and Si substrate and there is no undesirable layer formation. However, upon annealing up to 800°C, the sample switches to Poole-Frenkel emission due to the change in CeO_2 oxidation state from +4 to +3 as indicated in the XPS result. As a result of the change in oxidation state, changes in O vacancy could have led to trapped electrons within the bulk CeO_2.

8. FUTURE WORK

8.1 Study of Leakage Current Mechanism (Low Temperature)

The differing nature of chemical bonds, microstructure, crystallinity and composition at interface causes interfacial defect states, stresses and localized high fields that lead to charge trapping, hysteresis and high frequency dispersion effects [105].

Hence with the introduction of passivation layer (e.g. TiO_2 and GdSiO), it would be crucial to better understand the leakage current conduction mechanism of such bilayer film stacks for the purpose of material selection and integration. With the earlier studies done on thermally assisted leakage current conduction mechanism (Poole-Frenkel and Schottky emission), it would also be of interest to further investigate leakage current mechanisms such as field-assisted tunnelling and Fowler-Nordheim conduction) which requires low temperature measurements to suppress temperature activated process.

8.2 Study of Different Lanthanide Materials

Rare earth oxides of cerium, gadolinium and lutetium are studied to analyze their physical properties and electrical performance to verify with that reported in literature. This is due to debatable lanthanide trend reported by Park *et. al.* [30] and Xue *et. al.* [31]. In addition, some reports contradict on the physical properties of CeO_2, making it a less studied gate oxide candidate.

Results showed that Nd_2O_3 and Gd_2O_3 are potential gate dielectrics with high k-value and relatively smooth films as well as acceptable leakage current.

It is important to study the influence of physical properties of varying lanthanide materials towards electrical performance. Hence, characterization by physical and

electrical techniques are employed such as XPS, RBS and C-V as well as I-V measurements to better understand the film properties, interface traps/defects and their effect on the device performance.

Another area that requires more studies is the deposition of silicate films via atomic layer deposition using silyl-amide complexes. This is due to the attractive characteristics of ALD that leads to conformal and uniform thickness with easy thickness control due to its self-limiting process [40]. In addition, silicate films have benefits such as wide band gap, thermodynamically stable on Si, better interface with underlying silicon thus reducing the formation of undesired SiO_2 interfacial layer which limits the lowest achievable EOT. Few have reported the success of deposition of silicate films using silyl-amide complexes and thus it is important to establish the feasibility of depositing silicate films using this precursor.

Based on the NMR result, commercially available gadolinium precursor shows methyl peak at 0.09.

The silicate films due to presence of Si atoms, will have reduced k-value, hence methods to increase k-value will be explored. One of the proposed approaches is by doping the films as mentioned earlier in literature review whereby aluminium oxide is doped with zirconium [66]. It is found that dopants act as network modifiers [66]. Improving the dielectric constant of silicate films has yet to be reported and hence, more studies have to be done.

Another alternative to form complex oxides without the need of passivation layer is by forming nanomixture structures by mixing high-k materials such as titanium oxide homogenously with rare earth oxide to form alloy such as Lu-Ti-O (Fig. 29). These

alloys may compensate the lacking of certain properties – for instance Lu-Ti-O nanomixture, Ti helps in improving the k-value whereas Lu helps to increase the band gap [67]. Studies have to be done on varying lanthanide oxides – mainly cerium, gadolinium and lutetium to analyze their electrical performance and physical properties.

However, these nanomixture structures may have issues such as introducing more defects/traps and charges into the oxide. Hence, the characterization of defects in bulk and interface is also an important research area that needs to be further studied as there is lacking of this study in the area of rare earth nanolaminate and nanomixture structures. This is due to the detrimental effects of these defects that may lead to oxide breakdown and degraded performance.

8.3 Study of Different Substrate Materials

Due to the rapid down-scaling of transistors, to achieve the expected electrical performance of the device is becoming more difficult if the substrate remains as Si. Hence, more studies are now being done to substitute the substrate with that of other materials such as Germanium or SiGe substrates.

Hence, it would be interesting to study the performance of such high-k dielectrics or bilayer film stack on alternate substrates as these will be the future devices and material compatibility/integration is important.

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